XMC5100/5200 MCU registers

Reference manual

About this document

Scope and purpose

The XMC5100/XMC5200 MCU registers reference manual provides reference information for registers and contains respective programming details.

Intended audience

This manual is for system designer and programmers who are designing or programming using XMC5100/ XMC5200 parts.

Table of contents

About this document . . . 1
Register mapping . . . 4
Table of contents . . . 2
1 CPU subsystem (CPUSS) . . . 9
1.1 CPUSS registers . . . 30
2 Interprocessor communication (IPC) . . . 640
2.1 IPC registers . . . 643
3 Protection unit . . . 655
3.1 Protection unit registers . . . 660
4 Direct memory access (DMA) . . . 703
4.1 Direct memory access (DMA) registers . . . 774
5 FLASH . . . 845
5.1 FLASH registers . . . 846
6 Supervisory Flash (SFLASH) . . . 897
6.1 SFLASH registers . . . 899
7 Fault subsystem . . . 948
7.1 Fault subsystem registers . . . 950
8 System resources subsystem (SRSS) . . . 973
8.1 SRSS registers . . . 977
9 Peripheral . . . 1095
9.1 Peripheral registers . . . 1341
10 BACKUP . . . 2373
10.1 BACKUP registers . . . 2373
11 IO subsystem . . . 2395
11.1 IO subsystem registers . . . 2417
12 Controller area network flexible datarate (CANFD) . . . 2648
12.1 CANFD registers . . . 2666
13 Serial Communication Block (SCB) . . . 2776
13.1 SCB registers . . . 2792
14 Timer, counter, and pulse width modulator (TCPWM) . . . 2906
14.1 TCPWM registers . . . 3001
15 Cryptography block (CRYPTO) . . . 3064
15.1 CRYPTO registers . . . 3066
16 Event generator (EVTGEN) . . . 3138

Table of contents

16.1 EVTGEN registers 3140

17 Programmable analog subsystem (PASS) 3155

17.1 PASS registers 3199

Revision history 3262

Trademarks 3263

Disclaimer 3264

Register mapping

The Register mapping section discusses the registers of the XMC5100_5200. This document should be used in conjunction with XMC5000 architecture reference manual. The register mapping section lists all the registers in mapping tables, in address order.

Register general conventions

The register conventions specific to this section and the register reference chapter are listed below table.

Convention	Description	Explanation
RW	Read/Write	These bits can be both read and written.
R	Read only	These bits can only be read. Writing has no effect on the bit value.
W	Write only	These bits can only be written. Reading the bit returns the reset value.
RW1C	Read/Write ‘1’ to clear	These bits can be read as well as cleared by writing ‘1’. Writing ‘0’ has no effect on the bit value.
RW0C	Read/Write ‘0’ to clear	These bits can be read as well as cleared by writing ‘0’. Writing ‘1’ has no effect on the bit value.
RW1S	Read/Write ‘1’ to set	These bits can be read as well as set by writing ‘1’. Writing ‘0’ has no effect on the bit value.
A	Alias	This register is an additional alias or another register. This convention is used when a physical register is mapped to multiple addresses, typically for firmware debug purposes. See the corresponding register descriptions for more details.
None/ Reserved	Reserved bits	Keep these bits at the default value.
‘x’ in a register /bit field name	Multiple instances	Multiple instances/address ranges of the same register/bit field.

Acronyms

This table lists the acronyms used in this document.

Table 1 Acronyms and abbreviations

Acronym	Description
A/D	analog to digital
ABS	absolute
ADC	analog-to-digital converter
AES	Advanced Encryption Standard
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, Arm data transfer bus
Arm®	Advanced RISC Machine, a CPU architecture
BD	buffer descriptor
BOD	brown-out detection

(table continues...)

Table 1 (continued) Acronyms and abbreviations

Acronym	Description
CAN FD	controller area network with flexible data rate
CBS	credit-based shaping
CFI	canonical format indicator
CMOS	complementary metal-oxide-semiconductor
CPHA	(SPI) clock phase
CPOL	(SPI) clock polarity
CPU	central processing unit
CPUSS	CPU subsystem
CRC	cyclic redundancy check, an error-checking protocol
CSV	clock supervisor
DDR	double data rate (also see SDR)
DES	data encryption standard
DMA	direct memory access
DW	data wire, same as P-DMA
ECC	error correcting code
ECO	external crystal oscillator
EEE	Energy Efficient Ethernet (IEEE Std 802.3az)
EOF	end of frame
ETM	embedded trace macrocell
FCS	frame check sequence
FIFO	first in first out
FLL	frequency locked loop
FPU	floating point unit
GHS	Green Hills tool chain with IDE
GPIO	general-purpose input/output
HSIOM	high-speed I/O matrix
HSM	hardware security module
IF	interface
I/O	input/output
IP	Internet protocol
IPG	inter-packet gap
I2C	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator
IMO	internal main oscillator
IPC	inter-processor communication
IrDA	infrared interface

(table continues...)

Table 1 (continued) Acronyms and abbreviations

Acronym	Description
IRQ	interrupt request
JTAG	Joint Test Action Group
LAN	local area network (IEEE Std 802)
LIN	local interconnect network, a communications protocol
LLDP	link layer discovery protocol (IEEE Std 802.1AB)
LPI	low-power idle (IEEE Std 802.3az)
LVD	low-voltage detection
MAC	media access control (IEEE Std 802)
MCU	microcontroller Unit
MCWDT	multi-counter watchdog timer
M-DMA	memory-direct memory access
MDC	management data clock
MII	media independent interface
MISO	master-in slave-out
MMIO	memory mapped I/O
MOSI	master-out slave-in
MPU	memory protection unit
NSP	non-standard preamble
NVIC	nested vectored interrupt controller
OTA	over-the-air programming
OTP	one-time programmable
OVD	over voltage detection
P-DMA	peripheral-direct memory access same as DW
PCS	physical coding sublayer
PFC	priority-based flow control (IEEE Std 802.1Qbb)
PLL	phase-locked loop
PHY	physical sublayer
POR	power-on reset
PPB	private peripheral bus
PPPoE	point-to-point protocol over Ethernet
PPU	peripheral protection unit
PRNG	pseudo-random number generator
PTP	precision time protocol (IEEE Std 1588)
PWM	pulse-width modulation
RAM	random access memory
RISC	reduced-instruction-set computing

(table continues...)

Table 1 (continued) Acronyms and abbreviations

Acronym	Description
ROM	read-only memory
RTC	real-time clock
RX	reception
SAR	successive approximation register
SCB	serial communication block
SCL	I2C serial clock
SDA	I2C serial data
SDR	single data rate (also see DDR)
SECDED	single error correction double error detection
SerDes	serializer/deserializer
SHA	secure hash algorithm
SHE	secure hardware extension
SFD	start of frame delimiter
SGMII	serial Gigabit media independent interface
SMIF	serial memory interface
SMPU	shared memory protection unit
SNAP	subnetwork access protocol
SOF	start of frame
SPI	serial peripheral interface, a communications protocol
SRAM	static random-access memory
SWD	single wire debug
SYNC	LIN synchronization field
Tbit	bit period
TCP	transfer control protocol
TCPWM	timer/counter pulse-width modulator
TTL	transistor-transistor logic
TRNG	true random number generator
TS	timestamp
TSU	timestamp unit
TX	transmission
UART	universal asynchronous transmitter receiver, a communications protocol
UDP	user datagram protocol
VLAN	virtual LAN (IEEE Std 802.1Q)
WCO	watch crystal oscillator
WDT	watchdog timer reset
XIP	execute-in-place

(table continues...)

Table 1 (continued) Acronyms and abbreviations

Acronym	Description
XRES_L	external reset I/O pin (Active Low)
XTAL	crystal

1 CPU subsystem (CPUSS)

Register details

Register name	Address	Description
CPUSS_IDENTITY	0x40200000	Identity
CPUSS_CM4_STATUS	0x40200004	CM4 status
CPUSS_CM4_CLOCK_CTL	0x40200008	CM4 clock control
CPUSS_CM4_CTL	0x4020000C	CM4 control
CPUSS_CM4_INT0_STATUS	0x40200100	CM4 interrupt 0 status
CPUSS_CM4_INT1_STATUS	0x40200104	CM4 interrupt 1 status
CPUSS_CM4_INT2_STATUS	0x40200108	CM4 interrupt 2 status
CPUSS_CM4_INT3_STATUS	0x4020010C	CM4 interrupt 3 status
CPUSS_CM4_INT4_STATUS	0x40200110	CM4 interrupt 4 status
CPUSS_CM4_INT5_STATUS	0x40200114	CM4 interrupt 5 status
CPUSS_CM4_INT6_STATUS	0x40200118	CM4 interrupt 6 status
CPUSS_CM4_INT7_STATUS	0x4020011C	CM4 interrupt 7 status
CPUSS_CM4_VECTOR_TABLE_BASE	0x40200200	CM4 vector table base
CPUSS_CM4_NMI_CTL0	0x40200240	CM4 NMI control
CPUSS_CM4_NMI_CTL1	0x40200244	CM4 NMI control. See CPUSS_CM4_NMI_CTL0 for the details of bit fields.
CPUSS_CM4_NMI_CTL2	0x40200248	CM4 NMI control. See CPUSS_CM4_NMI_CTL0 for the details of bit fields.
CPUSS_CM4_NMI_CTL3	0x4020024C	CM4 NMI control. See CPUSS_CM4_NMI_CTL0 for the details of bit fields.
CPUSS_CM0_CTL	0x40201000	CM0+ control
CPUSS_CM0_STATUS	0x40201004	CM0+ status
CPUSS_CM0_CLOCK_CTL	0x40201008	CM0+ clock control
CPUSS_CM0_INT0_STATUS	0x40201100	CM0+ interrupt 0 status
CPUSS_CM0_INT1_STATUS	0x40201104	CM0+ interrupt 1 status
CPUSS_CM0_INT2_STATUS	0x40201108	CM0+ interrupt 2 status
CPUSS_CM0_INT3_STATUS	0x4020110C	CM0+ interrupt 3 status
CPUSS_CM0_INT4_STATUS	0x40201110	CM0+ interrupt 4 status
CPUSS_CM0_INT5_STATUS	0x40201114	CM0+ interrupt 5 status
CPUSS_CM0_INT6_STATUS	0x40201118	CM0+ interrupt 6 status
CPUSS_CM0_INT7_STATUS	0x4020111C	CM0+ interrupt 7 status
CPUSS_CM0_VECTOR_TABLE_BASE	0x40201120	CM0+ vector table base
CPUSS_CM0_NMI_CTL0	0x40201140	CM0+ NMI control
CPUSS_CM0_NMI_CTL1	0x40201144	CM0+ NMI control. See CPUSS_CM0_NMI_CTL0 for the details of bit fields.

Register name	Address	Description
CPUSS_CM0_NMI_CTL2	0x40201148	CM0+ NMI control. See CPUSS_CM0_NMI_CTL0 for the details of bit fields.
CPUSS_CM0_NMI_CTL3	0x4020114C	CM0+ NMI control. See CPUSS_CM0_NMI_CTL0 for the details of bit fields.
CPUSS_CM4_PWR_CTL	0x40201200	CM4 power control
CPUSS_CM4_PWR_DELAY_CTL	0x40201204	CM4 power control
CPUSS_RAM0_CTL0	0x40201300	RAM 0 control
CPUSS_RAM0_STATUS	0x40201304	RAM 0 status
CPUSS_RAM0_PWR_MACRO_CTL0	0x40201340	RAM 0 power control
CPUSS_RAM0_PWR_MACRO_CTL1	0x40201344	RAM 0 power control. See CPUSS_RAM0_PWR_MACRO_CTL0 for the details of bit fields.
CPUSS_RAM1_CTL0	0x40201380	RAM 1 control
CPUSS_RAM1_STATUS	0x40201384	RAM 1 status
CPUSS_RAM1_PWR_CTL	0x40201388	RAM 1 power control
CPUSS_RAM_PWR_DELAY_CTL	0x402013C0	Power up delay used for all SRAM power domains
CPUSS_ROM_CTL	0x402013C4	ROM control
CPUSS_ECC_CTL	0x402013C8	ECC control
CPUSS_PRODUCT_ID	0x40201400	Product identifier and version (same as CoreSight RomTables)
CPUSS_DP_STATUS	0x40201410	Debug port status
CPUSS_AP_CTL	0x40201414	Access port control
CPUSS_BUFF_CTL	0x40201500	Buffer control
CPUSS_SYSTICK_CTL	0x40201600	SysTick timer control
CPUSS_CAL_SUP_SET	0x40201800	Calibration support set and read
CPUSS_CAL_SUP_CLR	0x40201804	Calibration support clear and reset
CPUSS_CM0_PC_CTL	0x40202000	CM0+ protection context control
CPUSS_CM0_PC0_HANDLER	0x40202040	CM0+ protection context 0 handler
CPUSS_CM0_PC1_HANDLER	0x40202044	CM0+ protection context 1 handler
CPUSS_CM0_PC2_HANDLER	0x40202048	CM0+ protection context 2 handler
CPUSS_CM0_PC3_HANDLER	0x4020204C	CM0+ protection context 3 handler
CPUSS_PROTECTION	0x402020C4	Protection status
CPUSS_TRIM_ROM_CTL	0x40202100	ROM trim control
CPUSS_TRIM_RAM_CTL	0x40202104	RAM trim control
CPUSS_CM0_SYSTEM_INT_CTL0	0x40208000	CM0+ system interrupt control. This is the starting address of a register bank containing 353 registers (CPUSS_CM0_SYSTEM_INT_CTL0 to CPUSS_CM0_SYSTEM_INT_CTL352).

Register name	Address	Description
CPUSS_CM4_SYSTEM_INT_CTL0	0x4020A000	CM4 system interrupt control. This is the starting address of a register bank containing 353 registers (CPUSS_CM4_SYSTEM_INT_CTL0 to CPUSS_CM4_SYSTEM_INT_CTL352).
CM4_ITM_STIM0	0xE0000000	Stimulus Port registers. This is the starting address of a register bank containing 32 registers (CM4_ITM_STIM0 to CM4_ITM_STIM31).
CM4_ITM_TER	0xE0000E00	Trace Enable Register
CM4_ITM_TPR	0xE0000E40	ITM Trace Privilege Register
CM4_ITM_TCR	0xE0000E80	Trace Control Register
CM4_ITM_LAR	0xE0000FB0	Lock Access Register
CM4_ITM_LSR	0xE0000FB4	Lock Status Register
CM4_ITM_PID4	0xE0000FD0	Peripheral Identification Register 4.
CM4_ITM_PID5	0xE0000FD4	Peripheral Identification Register 5.
CM4_ITM_PID6	0xE0000FD8	Peripheral Identification Register 6.
CM4_ITM_PID7	0xE0000FDC	Peripheral Identification Register 7.
CM4_ITM_PID0	0xE0000FE0	Peripheral Identification Register 0.
CM4_ITM_PID1	0xE0000FE4	Peripheral Identification Register 1.
CM4_ITM_PID2	0xE0000FE8	Peripheral Identification Register 2.
CM4_ITM_PID3	0xE0000FEC	Peripheral Identification Register 3.
CM4_ITM_CID0	0xE0000FF0	Component Identification Register 0.
CM4_ITM_CID1	0xE0000FF4	Component Identification Register 1.
CM4_ITM_CID2	0xE0000FF8	Component Identification Register 2.
CM4_ITM_CID3	0xE0000FFC	Component Identification Register 3.
CM0P_DWT_DWT_CTRL	0xE0001000	Watchpoint Comparator Configuration
CM4_DWT_CTRL	0xE0001000	Control register
CM4_DWT_CYCCNT	0xE0001004	Cycle Count register
CM4_DWT_CPICNT	0xE0001008	CPI Count register
CM4_DWT_EXCCNT	0xE000100C	Exception Overhead Count register
CM4_DWT_SLEEPCNT	0xE0001010	Sleep Count register
CM4_DWT_LSUCNT	0xE0001014	LSU Count register
CM4_DWT_FOLDCNT	0xE0001018	Folded-instruction Count register
CM0P_DWT_DWT_PCSR	0xE000101C	Watchpoint Comparator PC Sample
CM4_DWT_PCSR	0xE000101C	Program Counter Sample Register
CM0P_DWT_DWT_COMP0	0xE0001020	Watchpoint Comparator Compare Value
CM4_DWT_COMP0	0xE0001020	Comparator registers
CM0P_DWT_DWT_MASK0	0xE0001024	Watchpoint Comparator Mask
CM4_DWT_MASK0	0xE0001024	Comparator Mask registers
CM0P_DWT_DWT_FUNCTION0	0xE0001028	Watchpoint Comparator Function

Register name	Address	Description
CM4_DWT_FUNCTION0	0xE0001028	Comparator Function registers
CM0P_DWT_DWT_COMP1	0xE0001030	Watchpoint Comparator Compare Value
CM4_DWT_COMP1	0xE0001030	Comparator registers
CM0P_DWT_DWT_MASK1	0xE0001034	Watchpoint Comparator Mask
CM4_DWT_MASK1	0xE0001034	Comparator Mask registers
CM0P_DWT_DWT_FUNCTION1	0xE0001038	Watchpoint Comparator Function. See CM0P_DWT_DWT_FUNCTION0 for the details of bit fields.
CM4_DWT_FUNCTION1	0xE0001038	Comparator Function registers
CM4_DWT_COMP2	0xE0001040	Comparator registers
CM4_DWT_MASK2	0xE0001044	Comparator Mask registers. See CM4_DWT_MASK1 for the details of bit fields.
CM4_DWT_FUNCTION2	0xE0001048	Comparator Function registers
CM4_DWT_COMP3	0xE0001050	Comparator registers. See CM4_DWT_COMP1 for the details of bit fields.
CM4_DWT_MASK3	0xE0001054	Comparator Mask registers. See CM4_DWT_MASK1 for the details of bit fields.
CM4_DWT_FUNCTION3	0xE0001058	Comparator Function registers
CM0P_DWT_DWT_PID4	0xE0001FD0	Watchpoint Unit CoreSight ROM Table Peripheral ID #4
CM4_DWT_PID4	0xE0001FD0	Peripheral Identification Register 4.
CM4_DWT_PID5	0xE0001FD4	Peripheral Identification Register 5.
CM4_DWT_PID6	0xE0001FD8	Peripheral Identification Register 6.
CM4_DWT_PID7	0xE0001FDC	Peripheral Identification Register 7.
CM0P_DWT_DWT_PID0	0xE0001FE0	Watchpoint Unit CoreSight ROM Table Peripheral ID #0
CM4_DWT_PID0	0xE0001FE0	Peripheral Identification Register 0.
CM0P_DWT_DWT_PID1	0xE0001FE4	Watchpoint Unit CoreSight ROM Table Peripheral ID #1
CM4_DWT_PID1	0xE0001FE4	Peripheral Identification Register 1.
CM0P_DWT_DWT_PID2	0xE0001FE8	Watchpoint Unit CoreSight ROM Table Peripheral ID #2
CM4_DWT_PID2	0xE0001FE8	Peripheral Identification Register 2.
CM0P_DWT_DWT_PID3	0xE0001FEC	Watchpoint Unit CoreSight ROM Table Peripheral ID #3
CM4_DWT_PID3	0xE0001FEC	Peripheral Identification Register 3.
CM0P_DWT_DWT_CID0	0xE0001FF0	Watchpoint Unit CoreSight ROM Table Component ID #0
CM4_DWT_CID0	0xE0001FF0	Component Identification Register 0.
CM0P_DWT_DWT_CID1	0xE0001FF4	Watchpoint Unit CoreSight ROM Table Component ID #1
CM4_DWT_CID1	0xE0001FF4	Component Identification Register 1.
CM0P_DWT_DWT_CID2	0xE0001FF8	Watchpoint Unit CoreSight ROM Table Component ID #2
CM4_DWT_CID2	0xE0001FF8	Component Identification Register 2.

Register name	Address	Description
CM0P_DWT_DWT_CID3	0xE0001FFC	Watchpoint Unit CoreSight ROM Table Component ID #3
CM4_DWT_CID3	0xE0001FFC	Component Identification Register 3.
CM0P_BP_BP_CTRL	0xE0002000	Breakpoint Unit Control
CM4_FPB_CTRL	0xE0002000	FlashPatch Control Register
CM4_FPB_REMAP	0xE0002004	FlashPatch Remap register
CM0P_BP_BP_COMP0	0xE0002008	Breakpoint Compare Register
CM4_FPB_COMP0	0xE0002008	FlashPatch Comparator register
CM0P_BP_BP_COMP1	0xE000200C	Breakpoint Compare Register
CM4_FPB_COMP1	0xE000200C	FlashPatch Comparator register. See CM4_FPB_COMP0 for the details of bit fields.
CM0P_BP_BP_COMP2	0xE0002010	Breakpoint Compare Register. See CM0P_BP_BP_COMP1 for the details of bit fields.
CM4_FPB_COMP2	0xE0002010	FlashPatch Comparator register. See CM4_FPB_COMP0 for the details of bit fields.
CM0P_BP_BP_COMP3	0xE0002014	Breakpoint Compare Register
CM4_FPB_COMP3	0xE0002014	FlashPatch Comparator register. See CM4_FPB_COMP0 for the details of bit fields.
CM4_FPB_COMP4	0xE0002018	FlashPatch Comparator register. See CM4_FPB_COMP0 for the details of bit fields.
CM4_FPB_COMP5	0xE000201C	FlashPatch Comparator register. See CM4_FPB_COMP0 for the details of bit fields.
CM4_FPB_COMP6	0xE0002020	FlashPatch Comparator register. See CM4_FPB_COMP0 for the details of bit fields.
CM4_FPB_COMP7	0xE0002024	FlashPatch Comparator register. See CM4_FPB_COMP0 for the details of bit fields.
CM0P_BP_BP_PID4	0xE0002FD0	Breakpoint Unit CoreSight ROM Table Peripheral ID #4
CM4_FPB_PID4	0xE0002FD0	Peripheral Identification Register 4.
CM4_FPB_PID5	0xE0002FD4	Peripheral Identification Register 5.
CM4_FPB_PID6	0xE0002FD8	Peripheral Identification Register 6.
CM4_FPB_PID7	0xE0002FDC	Peripheral Identification Register 7.
CM0P_BP_BP_PID0	0xE0002FE0	Breakpoint Unit CoreSight ROM Table Peripheral ID #0
CM4_FPB_PID0	0xE0002FE0	Peripheral Identification Register 0.
CM0P_BP_BP_PID1	0xE0002FE4	Breakpoint Unit CoreSight ROM Table Peripheral ID #1
CM4_FPB_PID1	0xE0002FE4	Peripheral Identification Register 1.
CM0P_BP_BP_PID2	0xE0002FE8	Breakpoint Unit CoreSight ROM Table Peripheral ID #2
CM4_FPB_PID2	0xE0002FE8	Peripheral Identification Register 2.
CM0P_BP_BP_PID3	0xE0002FEC	Breakpoint Unit CoreSight ROM Table Peripheral ID #3
CM4_FPB_PID3	0xE0002FEC	Peripheral Identification Register 3.
CM0P_BP_BP_CID0	0xE0002FF0	Breakpoint Unit CoreSight ROM Table Component ID #0

Register name	Address	Description
CM4_FPB_CID0	0xE0002FF0	Component Identification Register 0.
CM0P_BP_BP_CID1	0xE0002FF4	Breakpoint Unit CoreSight ROM Table Component ID #1
CM4_FPB_CID1	0xE0002FF4	Component Identification Register 1.
CM0P_BP_BP_CID2	0xE0002FF8	Breakpoint Unit CoreSight ROM Table Component ID #2
CM4_FPB_CID2	0xE0002FF8	Component Identification Register 2.
CM0P_BP_BP_CID3	0xE0002FFC	Breakpoint Unit CoreSight ROM Table Component ID #3
CM4_FPB_CID3	0xE0002FFC	Component Identification Register 3.
CM4_SCS_ACTLR	0xE000E008	Auxiliary Control Register
CM0P_SCS_SYST_CSR	0xE000E010	SysTick Control & Status
CM4_SCS_SYST_CSR	0xE000E010	SysTick Control and Status Register
CM0P_SCS_SYST_RVR	0xE000E014	SysTick Reload Value
CM4_SCS_SYST_RVR	0xE000E014	SysTick Reload Value Register
CM0P_SCS_SYST_CVR	0xE000E018	SysTick Current Value
CM4_SCS_SYST_CVR	0xE000E018	SysTick Current Value Register
CM0P_SCS_SYST_CALIB	0xE000E01C	SysTick Calibration Value
CM4_SCS_SYST_CALIB	0xE000E01C	SysTick Calibration value Register
CM0P_SCS_ISER	0xE000E100	Interrupt Set-Enable Register
CM4_SCS_NVIC_ISER0	0xE000E100	Interrupt Set-Enable Registers
CM4_SCS_NVIC_ISER1	0xE000E104	Interrupt Set-Enable Registers. See CM4_SCS_NVIC_ISER0 for the details of bit fields.
CM4_SCS_NVIC_ISER2	0xE000E108	Interrupt Set-Enable Registers. See CM4_SCS_NVIC_ISER0 for the details of bit fields.
CM4_SCS_NVIC_ISER3	0xE000E10C	Interrupt Set-Enable Registers. See CM4_SCS_NVIC_ISER0 for the details of bit fields.
CM4_SCS_NVIC_ISER4	0xE000E110	Interrupt Set-Enable Registers. See CM4_SCS_NVIC_ISER0 for the details of bit fields.
CM4_SCS_NVIC_ISER5	0xE000E114	Interrupt Set-Enable Registers. See CM4_SCS_NVIC_ISER0 for the details of bit fields.
CM4_SCS_NVIC_ISER6	0xE000E118	Interrupt Set-Enable Registers. See CM4_SCS_NVIC_ISER0 for the details of bit fields.
CM4_SCS_NVIC_ISER7	0xE000E11C	Interrupt Set-Enable Registers. See CM4_SCS_NVIC_ISER0 for the details of bit fields.
CM0P_SCS_ICER	0xE000E180	Interrupt Clear Enable Register
CM4_SCS_NVIC_ICER0	0xE000E180	Interrupt Clear-Enable Registers
CM4_SCS_NVIC_ICER1	0xE000E184	Interrupt Clear-Enable Registers. See CM4_SCS_NVIC_ICER0 for the details of bit fields.
CM4_SCS_NVIC_ICER2	0xE000E188	Interrupt Clear-Enable Registers. See CM4_SCS_NVIC_ICER0 for the details of bit fields.

Register name	Address	Description
CM4_SCS_NVIC_ICER3	0xE000E18C	Interrupt Clear-Enable Registers. See CM4_SCS_NVIC_ICER0 for the details of bit fields.
CM4_SCS_NVIC_ICER4	0xE000E190	Interrupt Clear-Enable Registers. See CM4_SCS_NVIC_ICER0 for the details of bit fields.
CM4_SCS_NVIC_ICER5	0xE000E194	Interrupt Clear-Enable Registers. See CM4_SCS_NVIC_ICER0 for the details of bit fields.
CM4_SCS_NVIC_ICER6	0xE000E198	Interrupt Clear-Enable Registers. See CM4_SCS_NVIC_ICER0 for the details of bit fields.
CM4_SCS_NVIC_ICER7	0xE000E19C	Interrupt Clear-Enable Registers. See CM4_SCS_NVIC_ICER0 for the details of bit fields.
CM0P_SCS_ISPR	0xE000E200	Interrupt Set-Pending Register
CM4_SCS_NVIC_ISPR0	0xE000E200	Interrupt Set-Pending Registers
CM4_SCS_NVIC_ISPR1	0xE000E204	Interrupt Set-Pending Registers. See CM4_SCS_NVIC_ISPR0 for the details of bit fields.
CM4_SCS_NVIC_ISPR2	0xE000E208	Interrupt Set-Pending Registers. See CM4_SCS_NVIC_ISPR0 for the details of bit fields.
CM4_SCS_NVIC_ISPR3	0xE000E20C	Interrupt Set-Pending Registers. See CM4_SCS_NVIC_ISPR0 for the details of bit fields.
CM4_SCS_NVIC_ISPR4	0xE000E210	Interrupt Set-Pending Registers. See CM4_SCS_NVIC_ISPR0 for the details of bit fields.
CM4_SCS_NVIC_ISPR5	0xE000E214	Interrupt Set-Pending Registers. See CM4_SCS_NVIC_ISPR0 for the details of bit fields.
CM4_SCS_NVIC_ISPR6	0xE000E218	Interrupt Set-Pending Registers. See CM4_SCS_NVIC_ISPR0 for the details of bit fields.
CM4_SCS_NVIC_ISPR7	0xE000E21C	Interrupt Set-Pending Registers. See CM4_SCS_NVIC_ISPR0 for the details of bit fields.
CM0P_SCS_ICPR	0xE000E280	Interrupt Clear-Pending Register
CM4_SCS_NVIC_ICPR0	0xE000E280	Interrupt Clear-Pending Registers
CM4_SCS_NVIC_ICPR1	0xE000E284	Interrupt Clear-Pending Registers. See CM4_SCS_NVIC_ICPR0 for the details of bit fields.
CM4_SCS_NVIC_ICPR2	0xE000E288	Interrupt Clear-Pending Registers. See CM4_SCS_NVIC_ICPR0 for the details of bit fields.
CM4_SCS_NVIC_ICPR3	0xE000E28C	Interrupt Clear-Pending Registers. See CM4_SCS_NVIC_ICPR0 for the details of bit fields.
CM4_SCS_NVIC_ICPR4	0xE000E290	Interrupt Clear-Pending Registers. See CM4_SCS_NVIC_ICPR0 for the details of bit fields.
CM4_SCS_NVIC_ICPR5	0xE000E294	Interrupt Clear-Pending Registers. See CM4_SCS_NVIC_ICPR0 for the details of bit fields.
CM4_SCS_NVIC_ICPR6	0xE000E298	Interrupt Clear-Pending Registers. See CM4_SCS_NVIC_ICPR0 for the details of bit fields.
CM4_SCS_NVIC_ICPR7	0xE000E29C	Interrupt Clear-Pending Registers. See CM4_SCS_NVIC_ICPR0 for the details of bit fields.
CM4_SCS_NVIC_IABR0	0xE000E300	Interrupt Active Bit Registers

Register name	Address	Description
CM4_SCS_NVIC_IABR1	0xE000E304	Interrupt Active Bit Registers. See CM4_SCS_NVIC_IABR0 for the details of bit fields.
CM4_SCS_NVIC_IABR2	0xE000E308	Interrupt Active Bit Registers. See CM4_SCS_NVIC_IABR0 for the details of bit fields.
CM4_SCS_NVIC_IABR3	0xE000E30C	Interrupt Active Bit Registers. See CM4_SCS_NVIC_IABR0 for the details of bit fields.
CM4_SCS_NVIC_IABR4	0xE000E310	Interrupt Active Bit Registers. See CM4_SCS_NVIC_IABR0 for the details of bit fields.
CM4_SCS_NVIC_IABR5	0xE000E314	Interrupt Active Bit Registers. See CM4_SCS_NVIC_IABR0 for the details of bit fields.
CM4_SCS_NVIC_IABR6	0xE000E318	Interrupt Active Bit Registers. See CM4_SCS_NVIC_IABR0 for the details of bit fields.
CM4_SCS_NVIC_IABR7	0xE000E31C	Interrupt Active Bit Registers. See CM4_SCS_NVIC_IABR0 for the details of bit fields.
CM0P_SCS_IPR0	0xE000E400	Interrupt Priority Registers
CM4_SCS_NVIC_IPR0	0xE000E400	Interrupt Priority Registers. This is the starting address of a register bank containing 60 registers (CM4_SCS_NVIC_IPR0 to CM4_SCS_NVIC_IPR59).
CM0P_SCS_IPR1	0xE000E404	Interrupt Priority Registers. See CM0P_SCS_IPR0 for the details of bit fields.
CM0P_SCS_IPR2	0xE000E408	Interrupt Priority Registers. See CM0P_SCS_IPR0 for the details of bit fields.
CM0P_SCS_IPR3	0xE000E40C	Interrupt Priority Registers. See CM0P_SCS_IPR0 for the details of bit fields.
CM0P_SCS_IPR4	0xE000E410	Interrupt Priority Registers. See CM0P_SCS_IPR0 for the details of bit fields.
CM0P_SCS_IPR5	0xE000E414	Interrupt Priority Registers. See CM0P_SCS_IPR0 for the details of bit fields.
CM0P_SCS_IPR6	0xE000E418	Interrupt Priority Registers. See CM0P_SCS_IPR0 for the details of bit fields.
CM0P_SCS_IPR7	0xE000E41C	Interrupt Priority Registers. See CM0P_SCS_IPR0 for the details of bit fields.
CM0P_SCS_CPUID	0xE000ED00	CPUID Register
CM4_SCS_CPUID	0xE000ED00	CPUID Base Register
CM0P_SCS_ICSR	0xE000ED04	Interrupt Control State Register
CM4_SCS_ICSR	0xE000ED04	Interrupt Control and State Register
CM0P_SCS_VTOR	0xE000ED08	Vector Table Offset Register
CM4_SCS_VTOR	0xE000ED08	Vector Table Offset Register
CM0P_SCS_AIRCR	0xE000ED0C	Application Interrupt and Reset Control Register
CM4_SCS_AIRCR	0xE000ED0C	Application Interrupt and Reset Control Register
CM0P_SCS_SCR	0xE000ED10	System Control Register
CM4_SCS_SCR	0xE000ED10	System Control Register
CM0P_SCS_CCR	0xE000ED14	Configuration and Control Register

Register name	Address	Description
CM4_SCS_CCR	0xE000ED14	Configuration and Control Register
CM4_SCS_SHPR1	0xE000ED18	System Handler Priority Register 1
CM0P_SCS_SHPR2	0xE000ED1C	System Handler Priority Register 2
CM4_SCS_SHPR2	0xE000ED1C	System Handler Priority Register 2
CM0P_SCS_SHPR3	0xE000ED20	System Handler Priority Register 3
CM4_SCS_SHPR3	0xE000ED20	System Handler Priority Register 3
CM0P_SCS_SHCSR	0xE000ED24	System Handler Control and State Register
CM4_SCS_SHCSR	0xE000ED24	System Handler Control and State Register
CM4_SCS_CFSR	0xE000ED28	Configurable Fault Status Register
CM4_SCS_HFSR	0xE000ED2C	HardFault Status Register
CM0P_SCS_DFSR	0xE000ED30	Debug Fault Status Register
CM4_SCS_DFSR	0xE000ED30	Debug Fault Status Register
CM4_SCS_MMFAR	0xE000ED34	MemManage Fault Address Register
CM4_SCS_BFAR	0xE000ED38	BusFault Address Register
CM4_SCS_AFSR	0xE000ED3C	Auxiliary Fault Status Register
CM4_SCS_CPACR	0xE000ED88	Coprocessor Access Control Register
CM0P_SCS_MPU_TYPE	0xE000ED90	MPU Type Register
CM4_SCS_MPU_TYPE	0xE000ED90	MPU Type Register
CM0P_SCS_MPU_CTRL	0xE000ED94	MPU Control Register
CM4_SCS_MPU_CTRL	0xE000ED94	MPU Control Register
CM0P_SCS_MPU_RNR	0xE000ED98	MPU Region Number Register
CM4_SCS_MPU_RNR	0xE000ED98	MPU Region Number Register
CM0P_SCS_MPU_RBAR	0xE000ED9C	MPU Region Base Address Register
CM4_SCS_MPU_RBAR	0xE000ED9C	MPU Region Base Address Register
CM0P_SCS_MPU_RASR	0xE000EDA0	MPU Region Attribute and Size Register
CM4_SCS_MPU_RASR	0xE000EDA0	MPU Region Attribute and Size Register
CM4_SCS_MPU_RBAR_A1	0xE000EDA4	MPU alias registers
CM4_SCS_MPU_RASR_A1	0xE000EDA8	MPU alias registers. See CM4_SCS_MPU_RBAR_A1 for the details of bit fields.
CM4_SCS_MPU_RBAR_A2	0xE000EDAC	MPU alias registers. See CM4_SCS_MPU_RBAR_A1 for the details of bit fields.
CM4_SCS_MPU_RASR_A2	0xE000EDB0	MPU alias registers. See CM4_SCS_MPU_RBAR_A1 for the details of bit fields.
CM4_SCS_MPU_RBAR_A3	0xE000EDB4	MPU alias registers. See CM4_SCS_MPU_RBAR_A1 for the details of bit fields.
CM4_SCS_MPU_RASR_A3	0xE000EDB8	MPU alias registers. See CM4_SCS_MPU_RBAR_A1 for the details of bit fields.
CM0P_SCS_DHCSR	0xE000EDF0	Debug Halting Control and Status Register
CM4_SCS_DHCSR	0xE000EDF0	Debug Halting Control and Status Register

Register name	Address	Description
CM0P_SCS_DCRSR	0xE000EDF4	Debug Core Register Selector Register
CM4_SCS_DCRSR	0xE000EDF4	Debug Core Register Selector Register
CM0P_SCS_DCRDR	0xE000EDF8	Debug Core Register Data Register
CM4_SCS_DCRDR	0xE000EDF8	Debug Core Register Data Register
CM0P_SCS_DEMCR	0xE000EDFC	Debug Exception and Monitor Control Register
CM4_SCS_DEMCR	0xE000EDFC	Debug Exception and Monitor Control Register
CM4_SCS_STIR	0xE000EF00	Software Triggered Interrupt Register
CM4_SCS_FPCCR	0xE000EF34	FP Context Control Register
CM4_SCS_FPCAR	0xE000EF38	FP Context Control Register. See CM4_SCS_FPCCR for the details of bit fields.
CM4_SCS_FPDSCR	0xE000EF3C	FP Context Control Register. See CM4_SCS_FPCCR for the details of bit fields.
CM0P_SCS_SCS_PID4	0xE000EFD0	System Control Space ROM Table Peripheral ID #4
CM4_SCS_PID4	0xE000EFD0	Peripheral Identification Register 4
CM4_SCS_PID5	0xE000EFD4	Peripheral Identification Register 5
CM4_SCS_PID6	0xE000EFD8	Peripheral Identification Register 6
CM4_SCS_PID7	0xE000EFDC	Peripheral Identification Register 7
CM0P_SCS_SCS_PID0	0xE000EFE0	System Control Space ROM Table Peripheral ID #0
CM4_SCS_PID0	0xE000EFE0	Peripheral Identification Register 0
CM0P_SCS_SCS_PID1	0xE000EFE4	System Control Space ROM Table Peripheral ID #1
CM4_SCS_PID1	0xE000EFE4	Peripheral Identification Register 1
CM0P_SCS_SCS_PID2	0xE000EFE8	System Control Space ROM Table Peripheral ID #2
CM4_SCS_PID2	0xE000EFE8	Peripheral Identification Register 2
CM0P_SCS_SCS_PID3	0xE000EFEC	System Control Space ROM Table Peripheral ID #3
CM4_SCS_PID3	0xE000EFEC	Peripheral Identification Register 3
CM0P_SCS_SCS_CID0	0xE000EFF0	System Control Space ROM Table Component ID #0
CM4_SCS_CID0	0xE000EFF0	Component Identification Register 0
CM0P_SCS_SCS_CID1	0xE000EFF4	System Control Space ROM Table Component ID #1
CM4_SCS_CID1	0xE000EFF4	Component Identification Register 1
CM0P_SCS_SCS_CID2	0xE000EFF8	System Control Space ROM Table Component ID #2
CM4_SCS_CID2	0xE000EFF8	Component Identification Register 2
CM0P_SCS_SCS_CID3	0xE000EFFC	System Control Space ROM Table Component ID #3
CM4_SCS_CID3	0xE000EFFC	Component Identification Register 3
CM4_ETM_CR	0xE0041000	Main Control Register
CM4_ETM_CCR	0xE0041004	Main Control Register
CM4_ETM_TRIGGER	0xE0041008	Trigger Event Register
CM4_ETM_SR	0xE0041010	ETM Status Register
CM4_ETM_SCR	0xE0041014	System Configuration Register

Register name	Address	Description
CM4_ETM_TEEVR	0xE0041020	TraceEnable Event Register
CM4_ETM_TECR1	0xE0041024	TraceEnable Control 1 Register
CM4_ETM_FFLR	0xE0041028	FIFOFULL Level Register
CM4_ETM_CNTRLDVR1	0xE0041140	Free-running counter reload value
CM4_ETM_SYNCFR	0xE00411E0	Synchronization Frequency Register
CM4_ETM_IDR	0xE00411E4	ID Register
CM4_ETM_CCER	0xE00411E8	Configuration Code Extension Register
CM4_ETM_TESSEICR	0xE00411F0	TraceEnable Start/Stop EmbeddedICE Control Register
CM4_ETM_TSEVR	0xE00411F8	Timestamp Event Register
CM4_ETM_TRACEIDR	0xE0041200	CoreSight Trace ID Register
CM4_ETM_IDR2	0xE0041208	ETM ID Register 2
CM4_ETM_PDSR	0xE0041314	Device Power-Down Status Register
CM4_ETM_ITMISCIN	0xE0041EE0	Integration Test Miscellaneous Inputs
CM4_ETM_ITTRIGOUT	0xE0041EE8	Integration Test Trigger Out
CM4_ETM_ITATBCTR2	0xE0041EF0	ETM Integration Test ATB Control 2
CM4_ETM_ITATBCTR0	0xE0041EF8	ETM Integration Test ATB Control 0
CM4_ETM_ITCTRL	0xE0041F00	Integration Mode Control Register
CM4_ETM_CLAIMSET	0xE0041FA0	Claim Tag Set Register
CM4_ETM_CLAIMCLR	0xE0041FA4	Claim Tag Clear Register
CM4_ETM_LAR	0xE0041FB0	Lock Access Register
CM4_ETM_LSR	0xE0041FB4	Lock Status Register
CM4_ETM_AUTHSTATUS	0xE0041FB8	Authentication Status Register
CM4_ETM_DEVTYPE	0xE0041FCC	CoreSight Device Type Register
CM4_ETM_PID4	0xE0041FD0	Peripheral Identification Register 4.
CM4_ETM_PID5	0xE0041FD4	Peripheral Identification Register 5.
CM4_ETM_PID6	0xE0041FD8	Peripheral Identification Register 6.
CM4_ETM_PID7	0xE0041FDC	Peripheral Identification Register 7.
CM4_ETM_PID0	0xE0041FE0	Peripheral Identification Register 0.
CM4_ETM_PID1	0xE0041FE4	Peripheral Identification Register 1.
CM4_ETM_PID2	0xE0041FE8	Peripheral Identification Register 2.
CM4_ETM_PID3	0xE0041FEC	Peripheral Identification Register 3.
CM4_ETM_CID0	0xE0041FF0	Component Identification Register 0.
CM4_ETM_CID1	0xE0041FF4	Component Identification Register 1.
CM4_ETM_CID2	0xE0041FF8	Component Identification Register 2.
CM4_ETM_CID3	0xE0041FFC	Component Identification Register 3.
CM4_CM4CTI_CTICONTROL	0xE0042000	CTI Control Register
CM4_CM4CTI_CTIINTACK	0xE0042010	CTI Interrupt Acknowledge Register

Register name	Address	Description
CM4_CM4CTI_CTIAPPSET	0xE0042014	CTI Application Trigger Set Register
CM4_CM4CTI_CTIAPPCLEAR	0xE0042018	CTI Application Trigger Clear Register
CM4_CM4CTI_CTIAPPPULSE	0xE004201C	CTI Application Pulse Register
CM4_CM4CTI_CTIINEN0	0xE0042020	CTI Trigger to Channel Enable Registers
CM4_CM4CTI_CTIINEN1	0xE0042024	CTI Trigger to Channel Enable Registers. See CM4_CM4CTI_CTIINEN0 for the details of bit fields.
CM4_CM4CTI_CTIINEN2	0xE0042028	CTI Trigger to Channel Enable Registers. See CM4_CM4CTI_CTIINEN0 for the details of bit fields.
CM4_CM4CTI_CTIINEN3	0xE004202C	CTI Trigger to Channel Enable Registers. See CM4_CM4CTI_CTIINEN0 for the details of bit fields.
CM4_CM4CTI_CTIINEN4	0xE0042030	CTI Trigger to Channel Enable Registers. See CM4_CM4CTI_CTIINEN0 for the details of bit fields.
CM4_CM4CTI_CTIINEN5	0xE0042034	CTI Trigger to Channel Enable Registers. See CM4_CM4CTI_CTIINEN0 for the details of bit fields.
CM4_CM4CTI_CTIINEN6	0xE0042038	CTI Trigger to Channel Enable Registers. See CM4_CM4CTI_CTIINEN0 for the details of bit fields.
CM4_CM4CTI_CTIINEN7	0xE004203C	CTI Trigger to Channel Enable Registers. See CM4_CM4CTI_CTIINEN0 for the details of bit fields.
CM4_CM4CTI_CTIOUTEN0	0xE00420A0	CTI Channel to Trigger Enable Registers
CM4_CM4CTI_CTIOUTEN1	0xE00420A4	CTI Channel to Trigger Enable Registers. See CM4_CM4CTI_CTIOUTEN0 for the details of bit fields.
CM4_CM4CTI_CTIOUTEN2	0xE00420A8	CTI Channel to Trigger Enable Registers. See CM4_CM4CTI_CTIOUTEN0 for the details of bit fields.
CM4_CM4CTI_CTIOUTEN3	0xE00420AC	CTI Channel to Trigger Enable Registers. See CM4_CM4CTI_CTIOUTEN0 for the details of bit fields.
CM4_CM4CTI_CTIOUTEN4	0xE00420B0	CTI Channel to Trigger Enable Registers. See CM4_CM4CTI_CTIOUTEN0 for the details of bit fields.
CM4_CM4CTI_CTIOUTEN5	0xE00420B4	CTI Channel to Trigger Enable Registers. See CM4_CM4CTI_CTIOUTEN0 for the details of bit fields.
CM4_CM4CTI_CTIOUTEN6	0xE00420B8	CTI Channel to Trigger Enable Registers. See CM4_CM4CTI_CTIOUTEN0 for the details of bit fields.
CM4_CM4CTI_CTIOUTEN7	0xE00420BC	CTI Channel to Trigger Enable Registers. See CM4_CM4CTI_CTIOUTEN0 for the details of bit fields.
CM4_CM4CTI_CTITRIGINSTATUS	0xE0042130	CTI Trigger In Status Register
CM4_CM4CTI_CTITRIGOUTSTATUS	0xE0042134	CTI Trigger Out Status Register
CM4_CM4CTI_CTICHINSTATUS	0xE0042138	CTI Channel In Status Register
CM4_CM4CTI_CTICHOUTSTATUS	0xE004213C	CTI Channel Out Status Register
CM4_CM4CTI_CTIGATE	0xE0042140	Enable CTI Channel Gate Register
CM4_CM4CTI_ASICCTL	0xE0042144	External Multiplexor Control Register
CM4_CM4CTI_ITCHINACK	0xE0042EDC	ITCHINACK Register
CM4_CM4CTI_ITTRIGINACK	0xE0042EE0	ITTRIGINACK Register
CM4_CM4CTI_ITCHOUT	0xE0042EE4	ITCHOUT Register

Register name	Address	Description
CM4_CM4CTI_ITTRIGOUT	0xE0042EE8	ITTRIGOUT Register
CM4_CM4CTI_ITCHOUTACK	0xE0042EEC	ITCHOUTACK Register
CM4_CM4CTI_ITTRIGOUTACK	0xE0042EF0	ITTRIGOUTACK Register
CM4_CM4CTI_ITCHIN	0xE0042EF4	ITCHIN Register
CM4_CM4CTI_ITTRIGIN	0xE0042EF8	ITTRIGIN Register
CM4_CM4CTI_ITCTRL	0xE0042F00	Integration Mode Control Register
CM4_CM4CTI_CLAIMSET	0xE0042FA0	Claim Tag Set Register
CM4_CM4CTI_CLAIMCLR	0xE0042FA4	Claim Tag Clear Register
CM4_CM4CTI_LOCKACCESS	0xE0042FB0	Lock Access Register
CM4_CM4CTI_LOCKSTATUS	0xE0042FB4	Lock Status Register
CM4_CM4CTI_AUTHSTATUS	0xE0042FB8	Authentication Status Register
CM4_CM4CTI_DEVID	0xE0042FC8	Device Configuration Register
CM4_CM4CTI_DEVTYPE	0xE0042FCC	Device Type Identifier Register
CM4_CM4CTI_PID4	0xE0042FD0	Peripheral Identification Register 4
CM4_CM4CTI_PID5	0xE0042FD4	Peripheral Identification Register 5
CM4_CM4CTI_PID6	0xE0042FD8	Peripheral Identification Register 6
CM4_CM4CTI_PID7	0xE0042FDC	Peripheral Identification Register 7
CM4_CM4CTI_PID0	0xE0042FE0	Peripheral Identification Register 0
CM4_CM4CTI_PID1	0xE0042FE4	Peripheral Identification Register 1
CM4_CM4CTI_PID2	0xE0042FE8	Peripheral Identification Register 2
CM4_CM4CTI_PID3	0xE0042FEC	Peripheral Identification Register 3
CM4_CM4CTI_CID0	0xE0042FF0	Component Identification Register 0
CM4_CM4CTI_CID1	0xE0042FF4	Component Identification Register 1
CM4_CM4CTI_CID2	0xE0042FF8	Component Identification Register 2
CM4_CM4CTI_CID3	0xE0042FFC	Component Identification Register 3
CM4_ROM_SCS	0xE007F000	CM4 CoreSight ROM Table Peripheral #0
CM4_ROM_DWT	0xE007F004	CM4 CoreSight ROM Table Peripheral #1
CM4_ROM_FPB	0xE007F008	CM4 CoreSight ROM Table Peripheral #2
CM4_ROM_ITM	0xE007F00C	CM4 CoreSight ROM Table Peripheral #3
CM4_ROM_CTI	0xE007F010	CM4 CoreSight ROM Table Peripheral #4
CM4_ROM_ETM	0xE007F014	CM4 CoreSight ROM Table Peripheral #5
CM4_ROM_CSMT	0xE007FFCC	CM4 CoreSight ROM Table Memory Type
CM4_ROM_PID4	0xE007FFD0	CM4 CoreSight ROM Table Peripheral ID #4
CM4_ROM_PID0	0xE007FFE0	CM4 CoreSight ROM Table Peripheral ID #0
CM4_ROM_PID1	0xE007FFE4	CM4 CoreSight ROM Table Peripheral ID #1
CM4_ROM_PID2	0xE007FFE8	CM4 CoreSight ROM Table Peripheral ID #2
CM4_ROM_PID3	0xE007FFEC	CM4 CoreSight ROM Table Peripheral ID #3
CM4_ROM_CID0	0xE007FFF0	CM4 CoreSight ROM Table Component ID #0

Register name	Address	Description
CM4_ROM_CID1	0xE007FFF4	CM4 CoreSight ROM Table Component ID #1
CM4_ROM_CID2	0xE007FFF8	CM4 CoreSight ROM Table Component ID #2
CM4_ROM_CID3	0xE007FFFC	CM4 CoreSight ROM Table Component ID #3
CM4_TRCCTI_CTICONTROL	0xE0080000	CTI Control Register
CM4_TRCCTI_CTIINTACK	0xE0080010	CTI Interrupt Acknowledge Register
CM4_TRCCTI_CTIAPPSET	0xE0080014	CTI Application Trigger Set Register
CM4_TRCCTI_CTIAPPCLEAR	0xE0080018	CTI Application Trigger Clear Register
CM4_TRCCTI_CTIAPPPULSE	0xE008001C	CTI Application Pulse Register
CM4_TRCCTI_CTIINEN0	0xE0080020	CTI Trigger to Channel Enable Registers
CM4_TRCCTI_CTIINEN1	0xE0080024	CTI Trigger to Channel Enable Registers. See CM4_TRCCTI_CTIINEN0 for the details of bit fields.
CM4_TRCCTI_CTIINEN2	0xE0080028	CTI Trigger to Channel Enable Registers. See CM4_TRCCTI_CTIINEN0 for the details of bit fields.
CM4_TRCCTI_CTIINEN3	0xE008002C	CTI Trigger to Channel Enable Registers. See CM4_TRCCTI_CTIINEN0 for the details of bit fields.
CM4_TRCCTI_CTIINEN4	0xE0080030	CTI Trigger to Channel Enable Registers. See CM4_TRCCTI_CTIINEN0 for the details of bit fields.
CM4_TRCCTI_CTIINEN5	0xE0080034	CTI Trigger to Channel Enable Registers. See CM4_TRCCTI_CTIINEN0 for the details of bit fields.
CM4_TRCCTI_CTIINEN6	0xE0080038	CTI Trigger to Channel Enable Registers. See CM4_TRCCTI_CTIINEN0 for the details of bit fields.
CM4_TRCCTI_CTIINEN7	0xE008003C	CTI Trigger to Channel Enable Registers. See CM4_TRCCTI_CTIINEN0 for the details of bit fields.
CM4_TRCCTI_CTIOUTEN0	0xE00800A0	CTI Channel to Trigger Enable Registers
CM4_TRCCTI_CTIOUTEN1	0xE00800A4	CTI Channel to Trigger Enable Registers. See CM4_TRCCTI_CTIOUTEN0 for the details of bit fields.
CM4_TRCCTI_CTIOUTEN2	0xE00800A8	CTI Channel to Trigger Enable Registers. See CM4_TRCCTI_CTIOUTEN0 for the details of bit fields.
CM4_TRCCTI_CTIOUTEN3	0xE00800AC	CTI Channel to Trigger Enable Registers. See CM4_TRCCTI_CTIOUTEN0 for the details of bit fields.
CM4_TRCCTI_CTIOUTEN4	0xE00800B0	CTI Channel to Trigger Enable Registers. See CM4_TRCCTI_CTIOUTEN0 for the details of bit fields.
CM4_TRCCTI_CTIOUTEN5	0xE00800B4	CTI Channel to Trigger Enable Registers. See CM4_TRCCTI_CTIOUTEN0 for the details of bit fields.
CM4_TRCCTI_CTIOUTEN6	0xE00800B8	CTI Channel to Trigger Enable Registers. See CM4_TRCCTI_CTIOUTEN0 for the details of bit fields.
CM4_TRCCTI_CTIOUTEN7	0xE00800BC	CTI Channel to Trigger Enable Registers. See CM4_TRCCTI_CTIOUTEN0 for the details of bit fields.
CM4_TRCCTI_CTITRIGINSTATUS	0xE0080130	CTI Trigger In Status Register
CM4_TRCCTI_CTITRIGOUTSTATUS	0xE0080134	CTI Trigger Out Status Register
CM4_TRCCTI_CTICHINSTATUS	0xE0080138	CTI Channel In Status Register
CM4_TRCCTI_CTICHOUTSTATUS	0xE008013C	CTI Channel Out Status Register

Register name	Address	Description
CM4_TRCCTI_CTIGATE	0xE0080140	Enable CTI Channel Gate Register
CM4_TRCCTI_ASICCTL	0xE0080144	External Multiplexor Control Register
CM4_TRCCTI_ITCHINACK	0xE0080EDC	ITCHINACK Register
CM4_TRCCTI_ITTRIGINACK	0xE0080EE0	ITTRIGINACK Register
CM4_TRCCTI_ITCHOUT	0xE0080EE4	ITCHOUT Register
CM4_TRCCTI_ITTRIGOUT	0xE0080EE8	ITTRIGOUT Register
CM4_TRCCTI_ITCHOUTACK	0xE0080EEC	ITCHOUTACK Register
CM4_TRCCTI_ITTRIGOUTACK	0xE0080EF0	ITTRIGOUTACK Register
CM4_TRCCTI_ITCHIN	0xE0080EF4	ITCHIN Register
CM4_TRCCTI_ITTRIGIN	0xE0080EF8	ITTRIGIN Register
CM4_TRCCTI_ITCTRL	0xE0080F00	Integration Mode Control Register
CM4_TRCCTI_CLAIMSET	0xE0080FA0	Claim Tag Set Register
CM4_TRCCTI_CLAIMCLR	0xE0080FA4	Claim Tag Clear Register
CM4_TRCCTI_LOCKACCESS	0xE0080FB0	Lock Access Register
CM4_TRCCTI_LOCKSTATUS	0xE0080FB4	Lock Status Register
CM4_TRCCTI_AUTHSTATUS	0xE0080FB8	Authentication Status Register
CM4_TRCCTI_DEVID	0xE0080FC8	Device Configuration Register
CM4_TRCCTI_DEVTYPE	0xE0080FCC	Device Type Identifier Register
CM4_TRCCTI_PID4	0xE0080FD0	Peripheral Identification Register 4
CM4_TRCCTI_PID5	0xE0080FD4	Peripheral Identification Register 5
CM4_TRCCTI_PID6	0xE0080FD8	Peripheral Identification Register 6
CM4_TRCCTI_PID7	0xE0080FDC	Peripheral Identification Register 7
CM4_TRCCTI_PID0	0xE0080FE0	Peripheral Identification Register 0
CM4_TRCCTI_PID1	0xE0080FE4	Peripheral Identification Register 1
CM4_TRCCTI_PID2	0xE0080FE8	Peripheral Identification Register 2
CM4_TRCCTI_PID3	0xE0080FEC	Peripheral Identification Register 3
CM4_TRCCTI_CID0	0xE0080FF0	Component Identification Register 0
CM4_TRCCTI_CID1	0xE0080FF4	Component Identification Register 1
CM4_TRCCTI_CID2	0xE0080FF8	Component Identification Register 2
CM4_TRCCTI_CID3	0xE0080FFC	Component Identification Register 3
CM4_CSTF_CSTFCTL	0xE008C000	Funnel Control Register
CM4_CSTF_CSTFPCTL	0xE008C004	Priority Control Register
CM4_CSTF_ITATBDATA0	0xE008CEEC	Integration Register
CM4_CSTF_ITATBCTR2	0xE008CEF0	Integration Register. See CM4_CSTF_ITATBDATA0 for the details of bit fields.
CM4_CSTF_ITATBCTR1	0xE008CEF4	Integration Register. See CM4_CSTF_ITATBDATA0 for the details of bit fields.
CM4_CSTF_ITATBCTR0	0xE008CEF8	Integration Register. See CM4_CSTF_ITATBDATA0 for the details of bit fields.

Register name	Address	Description
CM4_CSTF_ITCTRL	0xE008CF00	Integration Mode Control Register
CM4_CSTF_CLAIMSET	0xE008CFA0	Claim Tag Set Register
CM4_CSTF_CLAIMCLR	0xE008CFA4	Claim Tag Clear Register
CM4_CSTF_LOCKACCESS	0xE008CFB0	Lock Access Register
CM4_CSTF_LOCKSTATUS	0xE008CFB4	Lock Status Register
CM4_CSTF_AUTHSTATUS	0xE008CFB8	Authentication Status Register
CM4_CSTF_DEVID	0xE008CFC8	Device ID
CM4_CSTF_DEVTYPE	0xE008CFCC	Device Type Identifier Register
CM4_CSTF_PID4	0xE008CFD0	Peripheral Identification Register 4
CM4_CSTF_PID5	0xE008CFD4	Peripheral Identification Register 5
CM4_CSTF_PID6	0xE008CFD8	Peripheral Identification Register 6
CM4_CSTF_PID7	0xE008CFDC	Peripheral Identification Register 7
CM4_CSTF_PID0	0xE008CFE0	Peripheral Identification Register 0
CM4_CSTF_PID1	0xE008CFE4	Peripheral Identification Register 1
CM4_CSTF_PID2	0xE008CFE8	Peripheral Identification Register 2
CM4_CSTF_PID3	0xE008CFEC	Peripheral Identification Register 3
CM4_CSTF_CID0	0xE008CFF0	Component Identification Register 0
CM4_CSTF_CID1	0xE008CFF4	Component Identification Register 1
CM4_CSTF_CID2	0xE008CFF8	Component Identification Register 2
CM4_CSTF_CID3	0xE008CFFC	Component Identification Register 3
CM4_ETB_ETBRDP	0xE008D004	RAM Depth Register
CM4_ETB_ETBSTS	0xE008D00C	Status Register
CM4_ETB_ETBRRD	0xE008D010	RAM Read Data Register
CM4_ETB_ETBRRP	0xE008D014	RAM Read Pointer Register
CM4_ETB_ETBRWP	0xE008D018	RAM Write Pointer Register
CM4_ETB_ETBTRG	0xE008D01C	Trigger Counter Register
CM4_ETB_ETBCTL	0xE008D020	Control Register
CM4_ETB_ETBRWD	0xE008D024	RAM Write Data Register
CM4_ETB_ETBFFSR	0xE008D300	Formatter and Flush Status Register
CM4_ETB_ETBFFCR	0xE008D304	Formatter and Flush Control Register
CM4_ETB_ITMISCOP0	0xE008DEE0	Integration Register
CM4_ETB_ITTRFLINACK	0xE008DEE4	Integration Register. See CM4_ETB_ITMISCOP0 for the details of bit fields.
CM4_ETB_ITTRFLIN	0xE008DEE8	Integration Register
CM4_ETB_ITATBDATA0	0xE008DEEC	Integration Register. See CM4_ETB_ITTRFLIN for the details of bit fields.
CM4_ETB_ITATBCTR2	0xE008DEF0	Integration Register. See CM4_ETB_ITMISCOP0 for the details of bit fields.

Register name	Address	Description
CM4_ETB_ITATBCTR1	0xE008DEF4	Integration Register. See CM4_ETB_ITTRFLIN for the details of bit fields.
CM4_ETB_ITATBCTR0	0xE008DEF8	Integration Register. See CM4_ETB_ITTRFLIN for the details of bit fields.
CM4_ETB_ITCTRL	0xE008DF00	Integration Mode Control Register
CM4_ETB_CLAIMSET	0xE008DFA0	Claim Tag Set Register
CM4_ETB_CLAIMCLR	0xE008DFA4	Claim Tag Clear Register
CM4_ETB_LOCKACCESS	0xE008DFB0	Lock Access Register
CM4_ETB_LOCKSTATUS	0xE008DFB4	Lock Status Register
CM4_ETB_AUTHSTATUS	0xE008DFB8	Authentication Status Register
CM4_ETB_DEVID	0xE008DFC8	Device ID
CM4_ETB_DEVTYPE	0xE008DFCC	Device Type Identifier Register
CM4_ETB_PID4	0xE008DFD0	Peripheral Identification Register 4
CM4_ETB_PID5	0xE008DFD4	Peripheral Identification Register 5
CM4_ETB_PID6	0xE008DFD8	Peripheral Identification Register 6
CM4_ETB_PID7	0xE008DFDC	Peripheral Identification Register 7
CM4_ETB_PID0	0xE008DFE0	Peripheral Identification Register 0
CM4_ETB_PID1	0xE008DFE4	Peripheral Identification Register 1
CM4_ETB_PID2	0xE008DFE8	Peripheral Identification Register 2
CM4_ETB_PID3	0xE008DFEC	Peripheral Identification Register 3
CM4_ETB_CID0	0xE008DFF0	Component Identification Register 0
CM4_ETB_CID1	0xE008DFF4	Component Identification Register 1
CM4_ETB_CID2	0xE008DFF8	Component Identification Register 2
CM4_ETB_CID3	0xE008DFFC	Component Identification Register 3
CM4_TPIU_TPIU_SSPSR	0xE008E000	Supported Parallel Port Size Register
CM4_TPIU_TPIU_CSPSR	0xE008E004	Current Parallel Port Size Register
CM4_TPIU_TPIU_ACPR	0xE008E010	Asynchronous Clock Prescaler Register
CM4_TPIU_TPIU_SPPR	0xE008E0F0	Selected Pin Protocol Register
CM4_TPIU_TPIU_FFSR	0xE008E300	Formatter and Flush Status Register
CM4_TPIU_TPIU_FFCR	0xE008E304	Formatter and Flush Control Register
CM4_TPIU_TPIU_FSCR	0xE008E308	Formatter Synchronization Counter Register
CM4_TPIU_TRIGGER	0xE008EEE8	TRIGGER register
CM4_TPIU_FIFO_DATA_0	0xE008EEEC	Integration ETM Data
CM4_TPIU_ITATBCTR2	0xE008EEF0	Integration Register
CM4_TPIU_ITATBCTR0	0xE008EEF8	Integration Register. See CM4_TPIU_ITATBCTR2 for the details of bit fields.
CM4_TPIU_FIFO_DATA_1	0xE008EEFC	Integration ITM Data
CM4_TPIU_ITCTRL	0xE008EF00	Integration Mode Control Register
CM4_TPIU_CLAIMSET	0xE008EFA0	Claim Tag Set Register

Register name	Address	Description
CM4_TPIU_CLAIMCLR	0xE008EFA4	Claim Tag Clear Register
CM4_TPIU_DEVID	0xE008EFC8	Device ID
CM4_TPIU_DEVTYPE	0xE008EFCC	Device Type Identifier Register
CM4_TPIU_PID4	0xE008EFD0	Peripheral Identification Register 4
CM4_TPIU_PID5	0xE008EFD4	Peripheral Identification Register 5
CM4_TPIU_PID6	0xE008EFD8	Peripheral Identification Register 6
CM4_TPIU_PID7	0xE008EFDC	Peripheral Identification Register 7
CM4_TPIU_PID0	0xE008EFE0	Peripheral Identification Register 0
CM4_TPIU_PID1	0xE008EFE4	Peripheral Identification Register 1
CM4_TPIU_PID2	0xE008EFE8	Peripheral Identification Register 2
CM4_TPIU_PID3	0xE008EFEC	Peripheral Identification Register 3
CM4_TPIU_CID0	0xE008EFF0	Component Identification Register 0
CM4_TPIU_CID1	0xE008EFF4	Component Identification Register 1
CM4_TPIU_CID2	0xE008EFF8	Component Identification Register 2
CM4_TPIU_CID3	0xE008EFFC	Component Identification Register 3
CM0P_ROM_ROM_SCS	0xE00FF000	CM0+ CoreSight ROM Table Peripheral #0
CM4_ROMTABLE_TRC_CTI	0xE00FF000	CM4 CoreSight ROM Table Peripheral #0
CM0P_ROM_ROM_DWT	0xE00FF004	CM0+ CoreSight ROM Table Peripheral #1
CM4_ROMTABLE_TRC_CSTF	0xE00FF004	CM4 CoreSight ROM Table Peripheral #1
CM0P_ROM_ROM_BPU	0xE00FF008	CM0+ CoreSight ROM Table Peripheral #2
CM4_ROMTABLE_TRC_ETB	0xE00FF008	CM4 CoreSight ROM Table Peripheral #2
CM0P_ROM_ROM_END	0xE00FF00C	CM0+ CoreSight ROM Table End Marker
CM4_ROMTABLE_TRC_TPIU	0xE00FF00C	CM4 CoreSight ROM Table Peripheral #3
CM4_ROMTABLE_CM4	0xE00FF010	CM4 CoreSight ROM Table Peripheral #4
CM0P_ROM_ROM_CSMT	0xE00FFFCC	CM0+ CoreSight ROM Table Memory Type
CM4_ROMTABLE_CSMT	0xE00FFFCC	CM4 CoreSight ROM Table Memory Type
CM0P_ROM_ROM_PID4	0xE00FFFD0	CM0+ CoreSight ROM Table Peripheral ID #4
CM4_ROMTABLE_PID4	0xE00FFFD0	CM4 CoreSight ROM Table Peripheral ID #4
CM0P_ROM_ROM_PID0	0xE00FFFE0	CM0+ CoreSight ROM Table Peripheral ID #0
CM4_ROMTABLE_PID0	0xE00FFFE0	CM4 CoreSight ROM Table Peripheral ID #0
CM0P_ROM_ROM_PID1	0xE00FFFE4	CM0+ CoreSight ROM Table Peripheral ID #1
CM4_ROMTABLE_PID1	0xE00FFFE4	CM4 CoreSight ROM Table Peripheral ID #1
CM0P_ROM_ROM_PID2	0xE00FFFE8	CM0+ CoreSight ROM Table Peripheral ID #2
CM4_ROMTABLE_PID2	0xE00FFFE8	CM4 CoreSight ROM Table Peripheral ID #2
CM0P_ROM_ROM_PID3	0xE00FFFEC	CM0+ CoreSight ROM Table Peripheral ID #3
CM4_ROMTABLE_PID3	0xE00FFFEC	CM4 CoreSight ROM Table Peripheral ID #3
CM0P_ROM_ROM_CID0	0xE00FFFF0	CM0+ CoreSight ROM Table Component ID #0
CM4_ROMTABLE_CID0	0xE00FFFF0	CM4 CoreSight ROM Table Component ID #0

Register name	Address	Description
CM0P_ROM_ROM_CID1	0xE00FFFF4	CM0+ CoreSight ROM Table Component ID #1
CM4_ROMTABLE_CID1	0xE00FFFF4	CM4 CoreSight ROM Table Component ID #1
CM0P_ROM_ROM_CID2	0xE00FFFF8	CM0+ CoreSight ROM Table Component ID #2
CM4_ROMTABLE_CID2	0xE00FFFF8	CM4 CoreSight ROM Table Component ID #2
CM0P_ROM_ROM_CID3	0xE00FFFFC	CM0+ CoreSight ROM Table Component ID #3
CM4_ROMTABLE_CID3	0xE00FFFFC	CM4 CoreSight ROM Table Component ID #3
CM0P_ROMTABLE_ADDR0	0xF0000000	Link to Cortex M0+ ROM Table.
CM0P_ROMTABLE_ADDR1	0xF0000004	Link to CoreSight CTI Table.
CM0P_ROMTABLE_ADDR2	0xF0000008	Link to Cortex M0+ MTB Table.
CM0P_ROMTABLE_DID	0xF0000FCC	Device Type Identifier register.
CM0P_ROMTABLE_PID4	0xF0000FD0	Peripheral Identification Register 4.
CM0P_ROMTABLE_PID5	0xF0000FD4	Peripheral Identification Register 5.
CM0P_ROMTABLE_PID6	0xF0000FD8	Peripheral Identification Register 6.
CM0P_ROMTABLE_PID7	0xF0000FDC	Peripheral Identification Register 7.
CM0P_ROMTABLE_PID0	0xF0000FE0	Peripheral Identification Register 0.
CM0P_ROMTABLE_PID1	0xF0000FE4	Peripheral Identification Register 1.
CM0P_ROMTABLE_PID2	0xF0000FE8	Peripheral Identification Register 2.
CM0P_ROMTABLE_PID3	0xF0000FEC	Peripheral Identification Register 3.
CM0P_ROMTABLE_CID0	0xF0000FF0	Component Identification Register 0.
CM0P_ROMTABLE_CID1	0xF0000FF4	Component Identification Register 1.
CM0P_ROMTABLE_CID2	0xF0000FF8	Component Identification Register 2.
CM0P_ROMTABLE_CID3	0xF0000FFC	Component Identification Register 3.
CM0P_CTI_CTICONTROL	0xF0002000	CTI Control Register
CM0P_CTI_CTIINTACK	0xF0002010	CTI Interrupt Acknowledge Register
CM0P_CTI_CTIAPPSET	0xF0002014	CTI Application Trigger Set Register
CM0P_CTI_CTIAPPCLEAR	0xF0002018	CTI Application Trigger Clear Register
CM0P_CTI_CTIAPPPULSE	0xF000201C	CTI Application Pulse Register
CM0P_CTI_CTIINEN0	0xF0002020	CTI Trigger to Channel Enable Registers
CM0P_CTI_CTIINEN1	0xF0002024	CTI Trigger to Channel Enable Registers. See CM0P_CTI_CTIINEN0 for the details of bit fields.
CM0P_CTI_CTIINEN2	0xF0002028	CTI Trigger to Channel Enable Registers. See CM0P_CTI_CTIINEN0 for the details of bit fields.
CM0P_CTI_CTIINEN3	0xF000202C	CTI Trigger to Channel Enable Registers. See CM0P_CTI_CTIINEN0 for the details of bit fields.
CM0P_CTI_CTIINEN4	0xF0002030	CTI Trigger to Channel Enable Registers. See CM0P_CTI_CTIINEN0 for the details of bit fields.
CM0P_CTI_CTIINEN5	0xF0002034	CTI Trigger to Channel Enable Registers. See CM0P_CTI_CTIINEN0 for the details of bit fields.
CM0P_CTI_CTIINEN6	0xF0002038	CTI Trigger to Channel Enable Registers. See CM0P_CTI_CTIINEN0 for the details of bit fields.

Register name	Address	Description
CM0P_CTI_CTIINEN7	0xF000203C	CTI Trigger to Channel Enable Registers. See CM0P_CTI_CTIINEN0 for the details of bit fields.
CM0P_CTI_CTIOUTEN0	0xF00020A0	CTI Channel to Trigger Enable Registers
CM0P_CTI_CTIOUTEN1	0xF00020A4	CTI Channel to Trigger Enable Registers. See CM0P_CTI_CTIOUTEN0 for the details of bit fields.
CM0P_CTI_CTIOUTEN2	0xF00020A8	CTI Channel to Trigger Enable Registers. See CM0P_CTI_CTIOUTEN0 for the details of bit fields.
CM0P_CTI_CTIOUTEN3	0xF00020AC	CTI Channel to Trigger Enable Registers. See CM0P_CTI_CTIOUTEN0 for the details of bit fields.
CM0P_CTI_CTIOUTEN4	0xF00020B0	CTI Channel to Trigger Enable Registers. See CM0P_CTI_CTIOUTEN0 for the details of bit fields.
CM0P_CTI_CTIOUTEN5	0xF00020B4	CTI Channel to Trigger Enable Registers. See CM0P_CTI_CTIOUTEN0 for the details of bit fields.
CM0P_CTI_CTIOUTEN6	0xF00020B8	CTI Channel to Trigger Enable Registers. See CM0P_CTI_CTIOUTEN0 for the details of bit fields.
CM0P_CTI_CTIOUTEN7	0xF00020BC	CTI Channel to Trigger Enable Registers. See CM0P_CTI_CTIOUTEN0 for the details of bit fields.
CM0P_CTI_CTITRIGINSTATUS	0xF0002130	CTI Trigger In Status Register
CM0P_CTI_CTITRIGOUTSTATUS	0xF0002134	CTI Trigger Out Status Register
CM0P_CTI_CTICHINSTATUS	0xF0002138	CTI Channel In Status Register
CM0P_CTI_CTICHOUTSTATUS	0xF000213C	CTI Channel Out Status Register
CM0P_CTI_CTIGATE	0xF0002140	Enable CTI Channel Gate Register
CM0P_CTI_ASICCTL	0xF0002144	External Multiplexor Control Register
CM0P_CTI_ITCHINACK	0xF0002EDC	ITCHINACK Register
CM0P_CTI_ITTRIGINACK	0xF0002EE0	ITTRIGINACK Register
CM0P_CTI_ITCHOUT	0xF0002EE4	ITCHOUT Register
CM0P_CTI_ITTRIGOUT	0xF0002EE8	ITTRIGOUT Register
CM0P_CTI_ITCHOUTACK	0xF0002EEC	ITCHOUTACK Register
CM0P_CTI_ITTRIGOUTACK	0xF0002EF0	ITTRIGOUTACK Register
CM0P_CTI_ITCHIN	0xF0002EF4	ITCHIN Register
CM0P_CTI_ITTRIGIN	0xF0002EF8	ITTRIGIN Register
CM0P_CTI_ITCTRL	0xF0002F00	Integration Mode Control Register
CM0P_CTI_CLAIMSET	0xF0002FA0	Claim Tag Set Register
CM0P_CTI_CLAIMCLR	0xF0002FA4	Claim Tag Clear Register
CM0P_CTI_LOCKACCESS	0xF0002FB0	Lock Access Register
CM0P_CTI_LOCKSTATUS	0xF0002FB4	Lock Status Register
CM0P_CTI_AUTHSTATUS	0xF0002FB8	Authentication Status Register
CM0P_CTI_DEVID	0xF0002FC8	Device Configuration Register
CM0P_CTI_DEVTYPE	0xF0002FCC	Device Type Identifier Register
CM0P_CTI_PID4	0xF0002FD0	Peripheral Identification Register 4

Register name	Address	Description
CM0P_CTI_PID5	0xF0002FD4	Peripheral Identification Register 5
CM0P_CTI_PID6	0xF0002FD8	Peripheral Identification Register 6
CM0P_CTI_PID7	0xF0002FDC	Peripheral Identification Register 7
CM0P_CTI_PID0	0xF0002FE0	Peripheral Identification Register 0
CM0P_CTI_PID1	0xF0002FE4	Peripheral Identification Register 1
CM0P_CTI_PID2	0xF0002FE8	Peripheral Identification Register 2
CM0P_CTI_PID3	0xF0002FEC	Peripheral Identification Register 3
CM0P_CTI_CID0	0xF0002FF0	Component Identification Register 0
CM0P_CTI_CID1	0xF0002FF4	Component Identification Register 1
CM0P_CTI_CID2	0xF0002FF8	Component Identification Register 2
CM0P_CTI_CID3	0xF0002FFC	Component Identification Register 3
CM0P_MTB_POSITION	0xF0003000	POSITION register
CM0P_MTB_MASTER	0xF0003004	MASTER register
CM0P_MTB_FLOW	0xF0003008	FLOW register
CM0P_MTB_BASE	0xF000300C	BASE register
CM0P_MTB_LA	0xF0003FB0	Lock Access register
CM0P_MTB_LS	0xF0003FB4	Lock Status register
CM0P_MTB_AS	0xF0003FB8	Authentication Status register
CM0P_MTB_DARCH	0xF0003FBC	Device Architecture register
CM0P_MTB_DCFG	0xF0003FC8	Device Configuration register
CM0P_MTB_DID	0xF0003FCC	Device Type Identifier register.
CM0P_MTB_PID4	0xF0003FD0	Peripheral Identification Register 4.
CM0P_MTB_PID5	0xF0003FD4	Peripheral Identification Register 5.
CM0P_MTB_PID6	0xF0003FD8	Peripheral Identification Register 6.
CM0P_MTB_PID7	0xF0003FDC	Peripheral Identification Register 7.
CM0P_MTB_PID0	0xF0003FE0	Peripheral Identification Register 0.
CM0P_MTB_PID1	0xF0003FE4	Peripheral Identification Register 1.
CM0P_MTB_PID2	0xF0003FE8	Peripheral Identification Register 2.
CM0P_MTB_PID3	0xF0003FEC	Peripheral Identification Register 3.
CM0P_MTB_CID0	0xF0003FF0	Component Identification Register 0.
CM0P_MTB_CID1	0xF0003FF4	Component Identification Register 1.
CM0P_MTB_CID2	0xF0003FF8	Component Identification Register 2.
CM0P_MTB_CID3	0xF0003FFC	Component Identification Register 3.
SYSAP_ROMTABLE_DID	0xF1000FCC	Device Type Identifier register.. See CM0P_ROMTABLE_DID for the details of bit fields.
SYSAP_ROMTABLE_PID4	0xF1000FD0	Peripheral Identification Register 4.. See CM0P_ROMTABLE_PID4 for the details of bit fields.
SYSAP_ROMTABLE_PID5	0xF1000FD4	Peripheral Identification Register 5.. See CM0P_ROMTABLE_PID5 for the details of bit fields.

Register name	Address	Description
SYSAP_ROMTABLE_PID6	0xF1000FD8	Peripheral Identification Register 6.. See CM0P_ROMTABLE_PID6 for the details of bit fields.
SYSAP_ROMTABLE_PID7	0xF1000FDC	Peripheral Identification Register 7.. See CM0P_ROMTABLE_PID7 for the details of bit fields.
SYSAP_ROMTABLE_PID0	0xF1000FE0	Peripheral Identification Register 0.. See CM0P_ROMTABLE_PID0 for the details of bit fields.
SYSAP_ROMTABLE_PID1	0xF1000FE4	Peripheral Identification Register 1.. See CM0P_ROMTABLE_PID1 for the details of bit fields.
SYSAP_ROMTABLE_PID2	0xF1000FE8	Peripheral Identification Register 2.. See CM0P_ROMTABLE_PID2 for the details of bit fields.
SYSAP_ROMTABLE_PID3	0xF1000FEC	Peripheral Identification Register 3.. See CM0P_ROMTABLE_PID3 for the details of bit fields.
SYSAP_ROMTABLE_CID0	0xF1000FF0	Component Identification Register 0.. See CM0P_ROMTABLE_CID0 for the details of bit fields.
SYSAP_ROMTABLE_CID1	0xF1000FF4	Component Identification Register 1.. See CM0P_ROMTABLE_CID1 for the details of bit fields.
SYSAP_ROMTABLE_CID2	0xF1000FF8	Component Identification Register 2.. See CM0P_ROMTABLE_CID2 for the details of bit fields.
SYSAP_ROMTABLE_CID3	0xF1000FFC	Component Identification Register 3.. See CM0P_ROMTABLE_CID3 for the details of bit fields.

1.1 CPUSS registers

CPUSS_IDENTITY

Identity
Address: 0x40200000
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None		R	R
HW Access	W				None		W	W
Name	PC [7:4]				None [3:2]		NS	P
Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				MS [11:8]			
Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	None							

Bits	31	30	29	28	27	26	25	24
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 8	MS	This field specifies the bus master identifier of the transfer that reads the register. Default Value: Undefined
7 : 4	PC	This field specifies the protection context of the transfer that reads the register. Default Value: Undefined
1	NS	This field specifies the security setting ('0': secure mode; '1': non-secure mode) of the transfer that reads the register. Default Value: Undefined
0	P	This field specifies the privileged setting ('0': user mode; '1': privileged mode) of the transfer that reads the register. Default Value: Undefined

CPUSS_CM4_STATUS

CM4 status
Address: 0x40200004
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None		R	R
HW Access	None			W	None		W	W
Name	None [7:5]			PWR_DONE	None [3:2]		SLEEPDEEP	SLEEPING

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	PWR_DONE	After a PWR_MODE change this flag indicates if the new power mode has taken effect or not. Note: this flag can also change as a result of a change in debug power up req Default Value: 1
1	SLEEPDEEP	Specifies if the CPU is in Sleep or DeepSleep power mode. See SLEEPING field. Default Value: 1
0	SLEEPING	Specifies if the CPU is in Active, Sleep or DeepSleep power mode: - Active power mode: SLEEPING is '0'. - Sleep power mode: SLEEPING is '1' and SLEEPDEEP is '0'. - DeepSleep power mode: SLEEPING is '1' and SLEEPDEEP is '1'. Default Value: 1

CPUSS_CM4_CLOCK_CTL

CM4 clock control
Address: 0x40200008
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FAST_INT_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	FAST_INT_DIV	Specifies the fast clock divider (from the high frequency clock "clk_hf" to the peripheral clock "clk_fast"). Integer division by (1+FAST_INT_DIV). Allows for integer divisions in the range [1, 256] (FAST_INT_DIV is in the range [0, 255]). Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

CPUSS_CM4_CTL

CM4 control
Address: 0x4020000C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None		RW	RW	RW	RW	RW
HW Access	R	None		R	R	R	R	R
Name	IDC_MASK	None [30:29]		IXC_MASK	UFC_MASK	OFC_MASK	DZC_MASK	IOC_MASK

Bits	Name	Description
31	IDC_MASK	CPU FPU exception mask for the CPU's FPCSR.IDC "input denormalized" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Note: if the CPU FPCSR.FZ field is set to '1', denormalized inputs are "flushed to zero". Dependent on the FPU algorithm, this may or may not occur frequently. To prevent frequent CPU FPU interrupts as a result of denormalized inputs, this field may be set to '0'. Default Value: 0

28	IXC_MASK	CPU FPU exception mask for the CPU's FPCSR.IXC "inexact" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Note: the "inexact" condition is set as a result of rounding. Rounding may occur frequently and is typically not an error condition. To prevent frequent CPU FPU interrupts as a result of rounding, this field is typically set to '0'. Default Value: 0
27	UFC_MASK	CPU FPU exception mask for the CPU's FPCSR.UFC "underflow" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Default Value: 0
26	OFC_MASK	CPU FPU exception mask for the CPU's FPCSR.OFC "overflow" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Default Value: 0
25	DZC_MASK	CPU FPU exception mask for the CPU's FPCSR.DZC "divide by zero" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Default Value: 0

24	IOC_MASK	CPU floating point unit (FPU) exception mask for the CPU's FPCSR.IOC "invalid operation" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Note: the ARM architecture does NOT support FPU exceptions; i.e. there is no precise FPU exception handler. Instead, FPU conditions are captured in the CPU's FPCSR register and the conditions are provided as CPU interface signals. The interface signals are "masked" with the fields a provide by this register (CM7_0_CTL). The "masked" signals are reduced/OR-ed into a single CPU floating point interrupt signal. The associated CPU interrupt handler allows for imprecise handling of FPU exception conditions. Note: the CPU's FPCSR exception conditions are "sticky". Typically, the CPU FPU interrupt handler will clear the exception condition(s) to '0'. Note: by default, the FPU exception masks are '0'. Therefore, FPU exception conditions will NOT activate the CPU's floating point interrupt. Default Value: 0

CPUSS_CM4_INT0_STATUS

CM4 interrupt 0 status
Address: 0x40200100
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	SYSTEM_INT_VALID	None [30:24]						

Bits	Name	Description
31	SYSTEM_INT_VALID	See description of CM0_INT0_STATUS. Default Value: 0
9 : 0	SYSTEM_INT_IDX	Lowest CM4 activated system interrupt index for CPU interrupt 0. See description of CM0_INT0_STATUS. Default Value: Undefined

CPUSS_CM4_INT1_STATUS

CM4 interrupt 1 status
Address: 0x40200104
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	SYSTEM_INT_VALID	None [30:24]						

Bits	Name	Description
31	SYSTEM_INT_VALID	See description of CM0_INT0_STATUS. Default Value: 0
9 : 0	SYSTEM_INT_IDX	Lowest CM4 activated system interrupt index for CPU interrupt 1. See description of CM0_INT0_STATUS. Default Value: Undefined

CPUSS_CM4_INT2_STATUS

CM4 interrupt 2 status
Address: 0x40200108
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	SYSTEM_INT_VALID	None [30:24]						

Bits	Name	Description
31	SYSTEM_INT_VALID	See description of CM0_INT0_STATUS. Default Value: 0
9 : 0	SYSTEM_INT_IDX	Lowest CM4 activated system interrupt index for CPU interrupt 2. See description of CM0_INT0_STATUS. Default Value: Undefined

CPUSS_CM4_INT3_STATUS

CM4 interrupt 3 status
Address: 0x4020010C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	SYSTEM_INT_VALID	None [30:24]						

Bits	Name	Description
31	SYSTEM_INT_VALID	See description of CM0_INT0_STATUS. Default Value: 0
9 : 0	SYSTEM_INT_IDX	Lowest CM4 activated system interrupt index for CPU interrupt 3. See description of CM0_INT0_STATUS. Default Value: Undefined

CPUSS_CM4_INT4_STATUS

CM4 interrupt 4 status
Address: 0x40200110
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	SYSTEM_INT_VALID	None [30:24]						

Bits	Name	Description
31	SYSTEM_INT_VALID	See description of CM0_INT0_STATUS. Default Value: 0
9 : 0	SYSTEM_INT_IDX	Lowest CM4 activated system interrupt index for CPU interrupt 4. See description of CM0_INT0_STATUS. Default Value: Undefined

CPUSS_CM4_INT5_STATUS

CM4 interrupt 5 status
Address: 0x40200114
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	SYSTEM_INT_VALID	None [30:24]						

Bits	Name	Description
31	SYSTEM_INT_VALID	See description of CM0_INT0_STATUS. Default Value: 0
9 : 0	SYSTEM_INT_IDX	Lowest CM4 activated system interrupt index for CPU interrupt 5. See description of CM0_INT0_STATUS. Default Value: Undefined

CPUSS_CM4_INT6_STATUS

CM4 interrupt 6 status
Address: 0x40200118
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	SYSTEM_INT_VALID	None [30:24]						

Bits	Name	Description
31	SYSTEM_INT_VALID	See description of CM0_INT0_STATUS. Default Value: 0
9 : 0	SYSTEM_INT_IDX	Lowest CM4 activated system interrupt index for CPU interrupt 6. See description of CM0_INT0_STATUS. Default Value: Undefined

CPUSS_CM4_INT7_STATUS

CM4 interrupt 7 status
Address: 0x4020011C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	SYSTEM_INT_VALID	None [30:24]						

Bits	Name	Description
31	SYSTEM_INT_VALID	See description of CM0_INT0_STATUS. Default Value: 0
9 : 0	SYSTEM_INT_IDX	Lowest CM4 activated system interrupt index for CPU interrupt 7. See description of CM0_INT0_STATUS. Default Value: Undefined

CPUSS_CM4_VECTOR_TABLE_BASE

CM4 vector table base
Address: 0x40200200
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW						None	
HW Access							None	
Name	ADDR22 [15:10]						None [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	ADDR22 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	ADDR22 [31:24]							

Bits	Name	Description
31 : 10	ADDR22	Address of CM4 vector table. This register is used for CM4 warm and cold boot purposes: the CM0+ CPU initializes the CM4_VECTOR_TABLE_BASE register and the CM4 boot code uses the register to initialize the CM4 internal VTOR register. Note: the CM4 vector table is at an address that is a 1024 B multiple. Default Value: 0

CPUSS_CM4_NMI_CTL0

CM4 NMI control
Address: 0x40200240
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	SYSTEM_INT_IDX	System interrupt select for CPU NMI. The reset value ("1023") ensures that the CPU NMI is NOT connected to any system interrupt after DeepSleep reset. Default Value: 1023

CPUSS_CM0_CTL

CM0+ control
Address: 0x40201000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1S	R
Name	None [7:2]						ENABLED	SLV_STALL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VECTKEYSTAT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VECTKEYSTAT [31:24]							

Bits	Name	Description
31 : 16	VECTKEYSTAT	Register key (to prevent accidental writes). - Should be written with a 0x05fa key value for the write to take effect. - Always reads as 0xfa05. Note: Although the SW attribute for this field says ''R', SW need to write the key 0x05fa in this field for this register write to happen. This is a built in protection provided to prevent accidental writes from SW. Default Value: 0xFA05

1	ENABLED	Processor enable: '0': Disabled. Processor clock is turned off and reset is activated. After SW clears this field to '0', HW automatically sets this field to '1'. This effectively results in a CM0+ reset, followed by a CM0+ warm boot. '1': Enabled. Note: The intent is that this bit is modified only through an external probe or by the CM4 while the CM0+ is in Sleep or DeepSleep power mode. If this field is cleared to '0' by the CM0+ itself, it should be done under controlled conditions (such that undesirable side effects can be prevented). Note: The CM0+ CPU has a AIRCR.SYSRESETREQ register field that allows the CM0+ to reset the complete device (ENABLED only disables/enables the CM0+), resulting in a warm boot. This CPU register field has similar "built-in protection" as this CM0_CTL register to prevent accidental system writes (the upper 16-bits of the register need to be written with a 0x05fa key value; see CPU user manual for more details). Default Value: 1
0	SLV_STALL	Processor debug access control: '0': Access. '1': Stall access. This field is used to stall/delay debug accesses. This is useful to protect execution of code that needs to be protected from debug accesses. Default Value: 0

CPUSS_CM0_STATUS

CM0+ status
Address: 0x40201004
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						SLEEPDEEP	SLEEPING

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	SLEEPDEEP	Specifies if the CPU is in Sleep or DeepSleep power mode. See SLEEPING field. Default Value: 0
0	SLEEPING	Specifies if the CPU is in Active, Sleep or DeepSleep power mode: - Active power mode: SLEEPING is '0'. - Sleep power mode: SLEEPING is '1' and SLEEPDEEP is '0'. - DeepSleep power mode: SLEEPING is '1' and SLEEPDEEP is '1'. Default Value: 0

CPUSS_CM0_CLOCK_CTL

CM0+ clock control
Address: 0x40201008
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SLOW_INT_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	PERI_INT_DIV [31:24]							

Bits	Name	Description
31 : 24	PERI_INT_DIV	Specifies the peripheral clock divider (from the high frequency clock "clk_hf" to the peripheral clock "clk_peri"). Integer division by (1+PERI_INT_DIV). Allows for integer divisions in the range [1, 256] (PERI_INT_DIV is in the range [0, 255]). Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Note that Fperi <= Fperi_max. Fperi_max is likely to be smaller than Fhf_max. In other words, if Fhf = Fhf_max, PERI_INT_DIV should not be set to "0". Default Value: 0

15 : 8	SLOW_INT_DIV	Specifies the slow clock divider (from the peripheral clock "clk_peri" to the slow clock "clk_slow"). Integer division by (1+SLOW_INT_DIV). Allows for integer divisions in the range [1, 256] (SLOW_INT_DIV is in the range [0, 255]). Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

CPUSS_CM0_INT0_STATUS

CM0+ interrupt 0 status
Address: 0x40201100
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	SYSTEM_INT_VALID	None [30:24]						

Bits	Name	Description
31	SYSTEM_INT_VALID	Valid indication for SYSTEM_INT_IDX. When '0', no system interrupt for CPU interrupt 0 is valid/activated. Default Value: 0
9 : 0	SYSTEM_INT_IDX	Lowest CM0+ activated system interrupt index for CPU interrupt 0. Multiple system interrupts can be mapped on the same CPU interrupt. The selected system interrupt is the system interrupt with the lowest system interrupt index that has an activated interrupt request at the time of the fetch (system_interrupts[SYSTEM_INT_IDX] is '1'). The CPU interrupt handler SW can read SYSTEM_INT_IDX to determine the system interrupt that activated the handler. Default Value: Undefined

CPUSS_CM0_INT1_STATUS

CM0+ interrupt 1 status
Address: 0x40201104
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	SYSTEM_INT_VALID	None [30:24]						

Bits	Name	Description
31	SYSTEM_INT_VALID	See description of CM0_INT0_STATUS. Default Value: 0
9 : 0	SYSTEM_INT_IDX	Lowest CM0+ activated system interrupt index for CPU interrupt 1. See description of CM0_INT0_STATUS. Default Value: Undefined

CPUSS_CM0_INT2_STATUS

CM0+ interrupt 2 status
Address: 0x40201108
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	SYSTEM_INT_VALID	None [30:24]						

Bits	Name	Description
31	SYSTEM_INT_VALID	See description of CM0_INT0_STATUS. Default Value: 0
9 : 0	SYSTEM_INT_IDX	Lowest CM0+ activated system interrupt index for CPU interrupt 2. See description of CM0_INT0_STATUS. Default Value: Undefined

CPUSS_CM0_INT3_STATUS

CM0+ interrupt 3 status
Address: 0x4020110C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	SYSTEM_INT_VALID	None [30:24]						

Bits	Name	Description
31	SYSTEM_INT_VALID	See description of CM0_INT0_STATUS. Default Value: 0
9 : 0	SYSTEM_INT_IDX	Lowest CM0+ activated system interrupt index for CPU interrupt 3. See description of CM0_INT0_STATUS. Default Value: Undefined

CPUSS_CM0_INT4_STATUS

CM0+ interrupt 4 status
Address: 0x40201110
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	SYSTEM_INT_VALID	None [30:24]						

Bits	Name	Description
31	SYSTEM_INT_VALID	See description of CM0_INT0_STATUS. Default Value: 0
9 : 0	SYSTEM_INT_IDX	Lowest CM0+ activated system interrupt index for CPU interrupt 4. See description of CM0_INT0_STATUS. Default Value: Undefined

CPUSS_CM0_INT5_STATUS

CM0+ interrupt 5 status
Address: 0x40201114
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	SYSTEM_INT_VALID	None [30:24]						

Bits	Name	Description
31	SYSTEM_INT_VALID	See description of CM0_INT0_STATUS. Default Value: 0
9 : 0	SYSTEM_INT_IDX	Lowest CM0+ activated system interrupt index for CPU interrupt 5. See description of CM0_INT0_STATUS. Default Value: Undefined

CPUSS_CM0_INT6_STATUS

CM0+ interrupt 6 status
Address: 0x40201118
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	SYSTEM_INT_VALID	None [30:24]						

Bits	Name	Description
31	SYSTEM_INT_VALID	See description of CM0_INT0_STATUS. Default Value: 0
9 : 0	SYSTEM_INT_IDX	Lowest CM0+ activated system interrupt index for CPU interrupt 6. See description of CM0_INT0_STATUS. Default Value: Undefined

CPUSS_CM0_INT7_STATUS

CM0+ interrupt 7 status
Address: 0x4020111C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	SYSTEM_INT_VALID	None [30:24]						

Bits	Name	Description
31	SYSTEM_INT_VALID	See description of CM0_INT0_STATUS. Default Value: 0
9 : 0	SYSTEM_INT_IDX	Lowest CM0+ activated system interrupt index for CPU interrupt 7. See description of CM0_INT0_STATUS. Default Value: Undefined

CPUSS_CM0_VECTOR_TABLE_BASE

CM0+ vector table base
Address: 0x40201120
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	Address of CM0+ vector table. This register is used for CM0+ warm boot purposes: the CM0+ warm boot code uses the register to initialize the CM0+ internal VTOR register. Note: the CM0+ vector table is at an address that is a 256 B multiple. Default Value: 0

CPUSS_CM0_NMI_CTL0

CM0+ NMI control
Address: 0x40201140
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	SYSTEM_INT_IDX	System interrupt select for CPU NMI. The reset value ("1023") ensures that the CPU NMI is NOT connected to any system interrupt after DeepSleep reset. Default Value: 1023

CPUSS_CM4_PWR_CTL

CM4 power control
Address: 0x40201200
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VECTKEYSTAT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VECTKEYSTAT [31:24]							

Bits	Name	Description
31 : 16	VECTKEYSTAT	Register key (to prevent accidental writes). - Should be written with a 0x05fa key value for the write to take effect. - Always reads as 0xfa05. Note: Although the SW attribute for this field says ''R', SW need to write the key 0x05fa in this field for this register write to happen. This is a built in protection provided to prevent accidental writes from SW. Default Value: 0xFA05
1 : 0	PWR_MODE	Power mode. Default Value: 1
		0x0: OFF : Switch CM4 off Power off, clock off, isolate, reset and no retain.
		0x1: RESET : Reset CM4 Clock off, no isolated, no retain and reset. Note: The CM4 CPU has a AIRCR.SYSRESETREQ register field that allows the CM4 to reset the complete device (RESET only resets the CM4), resulting in a warm boot.

		0x2: RETAINED : Put CM4 in Retained mode This can only become effective if CM4 is in SleepDeep mode. Check PWR_DONE flag to see if CM4 RETAINED state has been reached. Power off, clock off, isolate, no reset and retain.
		0x3: ENABLED : Switch CM4 on. Power on, clock on, no isolate, no reset and no retain.

CPUSS_CM4_PWR_DELAY_CTL

CM4 power control
Address: 0x40201204
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	UP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						UP [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	UP	Number clock cycles delay needed after power domain power up Default Value: 0x12C

CPUSS_RAM0_CTL0

RAM 0 control
Address: 0x40201300
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						SLOW_WS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						FAST_WS [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [23:19]					ECC_INJ_EN	ECC_AUTO_CORRECT	ECC_EN

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18	ECC_INJ_EN	Enable error injection for system SRAM 0. When '1', the parity (ECC_CTL.PARITY) is used when a full 32-bit write is done to the ECC_CTL.WORD_ADDR word address of system SRAM 0. Default Value: 0
17	ECC_AUTO_CORRECT	HW ECC autocorrect functionality: '0': Disabled. '1': Enabled. HW automatically writes back SRAM with corrected data when a recoverable ECC error is detected. Default Value: 1
16	ECC_EN	Enable ECC checking: '0': Disabled. '1': Enabled. Default Value: 1
9 : 8	FAST_WS	Memory wait states for the fast clock domain ("clk_fast"). The number of wait states is expressed in "clk_hf" clock domain cycles. Default Value: 0

1 : 0	SLOW_WS	Memory wait states for the slow clock domain ("clk_slow"). The number of wait states is expressed in "clk_hf" clock domain cycles. Default Value: 1

CPUSS_RAM0_STATUS

RAM 0 status
Address: 0x40201304
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							WB_EMPTY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	WB_EMPTY	Write buffer empty. This information is used when entering DeepSleep power mode: WB_EMPTY must be '1' before a transition to system DeepSleep power mode. '0': Write buffer NOT empty. '1': Write buffer empty. Note: the SRAM controller write buffer is only used when ECC checking is enabled. (RAMi_CTL.ECC_EN is '1'). Default Value: 1

CPUSS_RAM0_PWR_MACRO_CTL0

RAM 0 power control
Address: 0x40201340
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VECTKEYSTAT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VECTKEYSTAT [31:24]							

Bits	Name	Description
31 : 16	VECTKEYSTAT	Register key (to prevent accidental writes). - Should be written with a 0x05fa key value for the write to take effect. - Always reads as 0xfa05. Note: Although the SW attribute for this field says ''R', SW need to write the key 0x05fa in this field for this register write to happen. This is a built in protection provided to prevent accidental writes from SW. Default Value: 0xFA05
1 : 0	PWR_MODE	SRAM Power mode. Default Value: 3
		0x0: OFF : Turn OFF the SRAM. This will trun OFF both array and periphery power of the SRAM and SRAM memory contents are lost.
		0x1: RESERVED : undefined

		0x2: RETAINED : Keep SRAM in Retained mode. This will turn OFF the SRAM periphery power, but array power is ON to retain memory contents. The SRAM contents will be retained in DeepSleep system power mode.
		0x3: ENABLED : Enable SRAM for regular operation. The SRAM contents will be retained in DeepSleep system power mode.

CPUSS_RAM1_CTL0

RAM 1 control
Address: 0x40201380
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						SLOW_WS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						FAST_WS [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [23:19]					ECC_INJ_EN	ECC_AUTO_CORRECT	ECC_EN

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18	ECC_INJ_EN	See RAM0_CTL. Default Value: 0
17	ECC_AUTO_CORRECT	See RAM0_CTL. Default Value: 1
16	ECC_EN	See RAM0_CTL. Default Value: 1
9 : 8	FAST_WS	See RAM0_CTL. Default Value: 0
1 : 0	SLOW_WS	See RAM0_CTL. Default Value: 1

CPUSS_RAM1_STATUS

RAM 1 status
Address: 0x40201384
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							WB_EMPTY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	WB_EMPTY	See RAM0_STATUS. Default Value: 1

CPUSS_RAM1_PWR_CTL

RAM 1 power control
Address: 0x40201388
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VECTKEYSTAT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VECTKEYSTAT [31:24]							

Bits	Name	Description
31 : 16	VECTKEYSTAT	See RAM0_PWR_MACRO_CTL. Default Value: 0xFA05
1 : 0	PWR_MODE	Power mode. Default Value: 3
		0x0: OFF : See RAM0_PWR_MACRO_CTL.
		0x1: RESERVED : undefined
		0x2: RETAINED : See RAM0_PWR_MACRO_CTL.
		0x3: ENABLED : See RAM0_PWR_MACRO_CTL.

CPUSS_RAM_PWR_DELAY_CTL

Power up delay used for all SRAM power domains
Address: 0x402013C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	UP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						UP [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	UP	Number clock cycles (clk_slow) delay needed after power domain power up Default Value: 0x96

CPUSS_ROM_CTL

ROM control
Address: 0x402013C4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						SLOW_WS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						FAST_WS [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	FAST_WS	Memory wait states for the fast clock domain ("clk_fast"). The number of wait states is expressed in "clk_hf" clock domain cycles. ROM_CTL.FAST_WS = '0' when clk_hf <= clk_hf_max. Default Value: 0

1 : 0	SLOW_WS	Memory wait states for the slow clock domain ("clk_slow"). The number of wait states is expressed in "clk_hf" clock domain cycles. Timing paths to and from the memory have a (fixed) minimum duration that always needs to be considered/met. The "clk_hf" clock domain frequency determines this field's value such that the timing paths minimum duration is met. ROM_CTL.SLOW_WS = '0' when clk_hf <=100 MHz. ROM_CTL.SLOW_WS = '1' when 100MHz < clk_hf <=clk_hf_max. Note: clk_hf_max depends on the target device. Refer datasheet. Default Value: 1

CPUSS_ECC_CTL

ECC control
Address: 0x402013C8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WORD_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WORD_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	WORD_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							RW
HW Access	R							R
Name	PARITY [31:25]							WORD_ADDR

Bits	Name	Description
31 : 25	PARITY	ECC parity to use for ECC error injection at address WORD_ADDR. Default Value: 0
24 : 0	WORD_ADDR	Specifies the word address where an error will be injected. - On a write transfer to this SRAM address and when the corresponding RAM0/RAM1/RAM2_CTL0.ECC_INJ_EN bit is '1', the parity (PARITY) is injected. This field needs to be written with the offset address within the memory, divided by 4. For example, if the RAM1 start address is 0x08010000, and an error is to be injected to address 0x08010040, then this field needs to configured to 0x000010. Default Value: 0

CPUSS_PRODUCT_ID

Product identifier and version (same as CoreSight RomTables)
Address: 0x40201400
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	FAMILY_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				FAMILY_ID [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	W				W			
Name	MINOR_REV [23:20]				MAJOR_REV [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 20	MINOR_REV	Minor Revision, starts with 1, increments with metal layer only tape-out (implemented with metal ECO-able tie-off) Default Value: Undefined
19 : 16	MAJOR_REV	Major Revision, starts with 1, increments with all layer tape-out (implemented with metal ECO-able tie-off) Default Value: Undefined
11 : 0	FAMILY_ID	Family ID. Common ID for a product family. Default Value: 257

CPUSS_DP_STATUS

Debug port status
Address: 0x40201410
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					SWJ_JTAG_SEL	SWJ_DEBUG_EN	SWJ_CONNECTED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	SWJ_JTAG_SEL	Specifies if the JTAG or SWD interface is selected. This signal is valid when DP_CTL.PTM_SEL is '0' (SWJ mode selected) and SWJ_CONNECTED is '1' (SWJ is connected). '0': SWD selected. '1': JTAG selected. Default Value: 1
1	SWJ_DEBUG_EN	Specifies if SWJ debug is enabled, i.e. CDBGPWRUPACK is '1' and thus debug clocks are on: '0': Disabled. '1': Enabled. Default Value: 0
0	SWJ_CONNECTED	Specifies if the SWJ debug port is connected; i.e. debug host interface is active: '0': Not connected/not active. '1': Connected/active. Default Value: 0

CPUSS_AP_CTL

Access port control
Address: 0x40201414
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					SYS_ENABLE	CM4_ENABLE	CM0_ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					R	R	R
Name	None [23:19]					SYS_DISABLE	CM4_DISABLE	CM0_DISABLE

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18	SYS_DISABLE	Disables the system AP interface: '0': Enabled. '1': Disabled. Typically, this field is set by the Cypress boot code with information from eFUSE. The access port is only enabled when SYS_DISABLE is '0' and SYS_ENABLE is '1'. Default Value: 0
17	CM4_DISABLE	Disables the CM4 AP interface: '0': Enabled. '1': Disabled. Typically, this field is set by the Cypress boot code with information from eFUSE. The access port is only enabled when CM4_DISABLE is '0' and CM4_ENABLE is '1'. Default Value: 0

16	CM0_DISABLE	Disables the CM0 AP interface: '0': Enabled. '1': Disabled. Typically, this field is set by the Cypress boot code with information from eFUSE. The access port is only enabled when CM0_DISABLE is '0' and CM0_ENABLE is '1'. Default Value: 0
2	SYS_ENABLE	Enables the system AP interface: '0': Disabled. '1': Enabled. Default Value: 0
1	CM4_ENABLE	Enables the CM4 AP interface: '0': Disabled. '1': Enabled. Default Value: 0
0	CM0_ENABLE	Enables the CM0 AP interface: '0': Disabled. '1': Enabled. Default Value: 0

CPUSS_BUFF_CTL

Buffer control
Address: 0x40201500
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							WRITE_BUFF

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	WRITE_BUFF	Specifies if write transfer can be buffered in the bus infrastructure bridges: '0': Write transfers are not buffered, independent of the transfer's bufferable attribute. '1': Write transfers can be buffered, if the transfer's bufferable attribute indicates that the transfer is a bufferable/posted write. Default Value: 1

CPUSS_SYSTICK_CTL

SysTick timer control
Address: 0x40201600
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TENMS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TENMS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TENMS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None				RW	
HW Access	R	R	None				R	
Name	NOREF	SKEW	None [29:26]				CLOCK_SOURCE [25:24]	

Bits	Name	Description
31	NOREF	Specifies if an external clock source is provided: '0': An external clock source is provided. '1': An external clock source is NOT provided and only the CPU internal clock can be used as SysTick timer clock source. Default Value: 0
30	SKEW	Specifies the precision of the clock source and if the TENMS field represents exactly 10 ms (clock source frequency is a multiple of 100 Hz). This affects the suitability of the SysTick timer as a SW real-time clock: '0': Precise. '1': Imprecise. Default Value: 1

25 : 24	CLOCK_SOURCE	Specifies an external clock source: "0": The low frequency clock "clk_lf" is selected. The precision of this clock depends on whether the low frequency clock source is a SRSS internal RC oscillator (imprecise) or a device external crystal oscillator (precise). "1": The internal main oscillator (IMO) clock "clk_imo" is selected. The MXS40 platform uses a fixed frequency IMO clock. o "2": The external crystal oscillator (ECO) clock "clk_eco" is selected. "3": The SRSS "clk_timer" is selected ("clk_timer" is a divided/gated version of "clk_hf" or "clk_imo"). Note: If NOREF is '1', the CLOCK_SOURCE value is NOT used. Note: It is SW's responsibility to provide the correct NOREF, SKEW and TENMS field values for the selected clock source. Default Value: 0
23 : 0	TENMS	Specifies the number of clock source cycles (minus 1) that make up 10 ms. E.g., for a 32,768 Hz reference clock, TENMS is 328 - 1 = 327. Default Value: 327

CPUSS_CAL_SUP_SET

Calibration support set and read
Address: 0x40201800
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Read without side effect, write 1 to set Default Value: 0

CPUSS_CAL_SUP_CLR

Calibration support clear and reset
Address: 0x40201804
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	A							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	A							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	A							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Read side effect: when read all bits are cleared, write 1 to clear a specific bit Note: no exception for the debug host, it also causes the read side effect Default Value: 0

CPUSS_CM0_PC_CTL

CM0+ protection context control
Address: 0x40202000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				VALID [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	VALID	Valid fields for the protection context handler CM0_PCi_HANDLER registers: Bit 0: Valid field for CM0_PC0_HANDLER. Bit 1: Valid field for CM0_PC1_HANDLER. Bit 2: Valid field for CM0_PC2_HANDLER. Bit 3: Valid field for CM0_PC3_HANDLER. Default Value: 0

CPUSS_CM0_PC0_HANDLER

CM0+ protection context 0 handler
Address: 0x40202040
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Address of the protection context 0 handler. This field is used to detect entry to Cypress "trusted" code through an exception/interrupt. Default Value: 0

CPUSS_CM0_PC1_HANDLER

CM0+ protection context 1 handler
Address: 0x40202044
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Address of the protection context 1 handler. Default Value: 0

CPUSS_CM0_PC2_HANDLER

CM0+ protection context 2 handler
Address: 0x40202048
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Address of the protection context 2 handler. Default Value: 0

CPUSS_CM0_PC3_HANDLER

CM0+ protection context 3 handler
Address: 0x4020204C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Address of the protection context 3 handler. Default Value: 0

CPUSS_PROTECTION

Protection status
Address: 0x402020C4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					STATE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	STATE	Protection state: "0": UNKNOWN. "1": VIRGIN. "2": NORMAL. "3": SECURE. "4": DEAD. The following state transitions are allowed (and enforced by HW): - UNKNOWN => VIRGIN/NORMAL/SECURE/DEAD - NORMAL => DEAD - SECURE => DEAD An attempt to make a NOT allowed state transition will NOT affect this register field. Default Value: 0

CPUSS_TRIM_ROM_CTL

ROM trim control
Address: 0x40202100
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					TRIM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

2 : 0	TRIM	For ARM ROMs the bits are defined as follows [2:0] EMA: Extra Margin Adjustment (0 is the fastest setting) Recommended default value: EMA=2 (ROM_TRIM_DEFAULT=0x0000_0002, ROM_TRIM_WIDTH=3) For Synopsys ROMs the bits are defined as follows: [3:0] RM: Read-Write margin control. This is used for setting the Read-Write margin. It programs the sense amplifier differential setting and allows the trade off between speed and robustness. - RM[1:0] values control access time and cycle time of the memory. RM[1:0] = "0" is the slowest possible mode of operation for the memory. This setting is required for VDDMIN operation. - RM[3:2] are factory pins reserved for debug mode and should be set to "0". [4] RME: Read-Write margin enable control. This selects between the default Read-Write margin setting, and the external pin Read-Write margin setting. Recommended default value for LP: RME=1, RM=2 (ROM_TRIM_DEFAULT=0x0000_0012, ROM_TRIM_WIDTH=5) Recommended default value for ULP: RME=1, RM=3 (ROM_TRIM_DEFAULT=0x0000_0013, ROM_TRIM_WIDTH=5) Default Value: 2

CPUSS_TRIM_RAM_CTL

RAM trim control
Address: 0x40202104
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TRIM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

7 : 0	TRIM	For ARM RAMs the bits are defined as follows [2:0] EMA: Extra Margin Adjustment (0 is the fastest setting) [4:3] EMAW: Extra Margin Adjustment for Writes (0 is the fastest setting) [7:5] CTL_BIAS: Control the bias circuit in the SRAM power switches for SRAMC0: 0=OFF, 7=max Recommended default value: CTL_BIAS=3, EMAW=0, EMA=2 (RAM_TRIM_DEFAULT=0x0000_0062, RAM_TRIM_WIDTH=8) For Synopsys RAMs the bits are defined as follows: [3:0] Read-Write margin control. This is used for setting the Read-Write margin. It programs the sense amplifier differential setting and allows the trade off between speed and robustness. - RM[1:0] values control access time and cycle time of the memory. RM[1:0] = "0" is the slowest possible mode of operation for the memory. This setting is required for VDDMIN operation. - RM[3:2] are factory pins reserved for debug mode and should be set to "0". [4] RME: Read-Write margin enable control. This selects between the default Read-Write margin setting, and the external RM[3:0] Read-Write margin setting. [7:5] WPULSE: Write Assist Pulse to control pulse width of negative voltage on SRAM bitline. [9:8] RA: Read Assist control for WL under-drive. [14:12] WA: Write assist enable control (Active High). - WA[2:0] Write Assist pins to control negative voltage on SRAM bitline. Recommended default value for LP: WA=4, RA=0, WPULSE=0, RME=1, RM=3 (RAM_TRIM_DEFAULT=0x0000_4013, RAM_TRIM_WIDTH=15) Recommended default value for ULP: WA=6, RA=0, WPULSE=0, RME=1, RM=2 (RAM_TRIM_DEFAULT=0x0000_6012, RAM_TRIM_WIDTH=15) Default Value: 98

CPUSS_CM0_SYSTEM_INT_CTL0

CM0+ system interrupt control
Address: 0x40208000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					CPU_INT_IDX [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	CPU_INT_VALID	None [30:24]						

Bits	Name	Description
31	CPU_INT_VALID	Interrupt enable: '0': Disabled. The system interrupt will NOT be mapped to any CPU interrupt. '1': Enabled. The system interrupt is mapped on CPU interrupt CPU_INT_IDX. Note: the CPUs have dedicated XXX_SYSTEM_INT_CTL registers. In other words, the CPUs can use different CPU interrupts for the same system interrupt. However, typically only one of the CPUs will have the ENABLED field of a specific system interrupt set to '1'. Default Value: 0

2 : 0	CPU_INT_IDX	CPU interrupt index (legal range [0, 7]). This field specifies to which CPU interrupt the system interrupt is mapped. E.g., if CPU_INT_IDX is "6", the system interrupt is mapped to CPU interrupt "6". Note: it is possible to map multiple system interrupts to the same CPU interrupt. It is advised to assign different priorities to the CPU interrupts and to assign system interrupts to CPU interrupts accordingly. Default Value: Undefined

CPUSS_CM4_SYSTEM_INT_CTL0

CM4 system interrupt control
Address: 0x4020A000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					CPU_INT_IDX [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	CPU_INT_VALID	None [30:24]						

Bits	Name	Description
31	CPU_INT_VALID	Default Value: 0
2 : 0	CPU_INT_IDX	Default Value: Undefined

CM4_ITM_STIM0

Stimulus Port registers
Address: 0xE0000000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	STIMULUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	STIMULUS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	STIMULUS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	STIMULUS [31:24]							

Bits	Name	Description
31 : 0	STIMULUS	Data write to the stimulus port FIFO, for forwarding as a software event packet. When read, bit[0] indicates whether the stimulus port FIFO can accept data: 0: Stimulus port FIFO full. 1: Stimulus port FIFO can accept at least one word. This bit is UNKNOWN after a Power-on reset. Default Value: X

CM4_ITM_TER

Trace Enable Register
Address: 0xE0000E00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	STIMENA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	STIMENA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	STIMENA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	STIMENA [31:24]							

Bits	Name	Description
31 : 0	STIMENA	For bit STIMENA[n]: 0: Stimulus port (n) disabled 1: Stimulus port (n) enabled Default Value: 0

CM4_ITM_TPR

ITM Trace Privilege Register
Address: 0xE0000E40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				PRIVMASK [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	PRIVMASK	Bit mask to enable tracing on ITM stimulus ports: bit [0] = stimulus ports [7:0] bit [1] = stimulus ports [15:8] bit [2] = stimulus ports [23:16] bit [3] = stimulus ports [31:24] Default Value: 0

CM4_ITM_TCR

Trace Control Register
Address: 0xE0000E80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			SWOENA	TXENA	SYNCENA	TSENA	ITMENA

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [15:12]				GTSFREQ [11:10]		TSPRESCALE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW						
HW Access	R	R						
Name	BUSY	TRACEBUSID [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	BUSY	Indicates whether the ITM is currently processing events: 0 ITM is not processing any events. 1 ITM events present and being drained. These bits are read-only. Default Value: 0
22 : 16	TRACEBUSID	Identifier for multi-source trace stream formatting. If multi-source trace is in use, the debugger must write a non-zero value to this field. For more information see CoreSight requirements for the TraceBusID field on TRM page C1-778. On a Power-on reset, the value of this field is UNKNOWN. Default Value: 0

11 : 10	GTSFREQ	Global timestamp frequency. Defines how often the ITM generates a global timestamp, based on the global timestamp clock frequency, or disables generation of global timestamps. The possible values are: 00 Disable generation of global timestamps. 01 Generate timestamp request whenever the ITM detects a change in global timestamp counter bits[47:7]. This is approximately every 128 cycles. 10 Generate timestamp request whenever the ITM detects a change in global timestamp counter bits[47:13]. This is approximately every 8192 cycles. 11 Generate a timestamp after every packet, if the output FIFO is empty. For more information see Global timestamping on Arm TRM page C1-771. A Power-on reset clears this field to zero. If the implementation does not support global timestamping then these bits are reserved, RAZ/WI. Default Value: 0
9 : 8	TSPRESCALE	Local timestamp prescaler, used with the trace packet reference clock. The possible values are: 00 No prescaling. 01 Divide by 4. 10 Divide by 16. 11 Divide by 64. If implemented, a Power-on reset clears this field to zero. If the processor does not implement the timestamp prescaler then these bits are reserved, RAZ/WI. Default Value: 0
4	SWOENA	Enables asynchronous clocking of the timestamp counter: 0 Timestamp counter uses the processor system clock. 1 Timestamp counter uses asynchronous clock from the TPIU interface. The timestamp counter is held in reset while the output line is idle. Which clocking modes are implemented is IMPLEMENTATION DEFINED. If the implementation does not support both modes this bit is either RAZ or RAO, to indicate the implemented mode. When this is a RW bit, on a Power-on reset, the value of this bit is UNKNOWN Default Value: 0

3	TXENA	Enables forwarding of hardware event packet from the DWT unit to the ITM for output to the TPIU: 0 Disabled. 1 Enabled. It is IMPLEMENTATION DEFINED whether the DWT discards packets that it cannot forward to the ITM. Note: If a debugger changes this bit from 0 to 1, the DWT might forward a hardware event packet that it has previously generated. A Power-on reset clears this bit to 0. Default Value: 0
2	SYNCENA	Enables Synchronization packet transmission for a synchronous TPIU: 0 Disabled. 1 Enabled. A Power-on reset clears this bit to 0. Note: If a debugger sets this bit to 1 it must also configure DWT_CTRL.SYNCTAP for the correct synchronization speed, see Control register, DWT_CTRL on Arm TRM page C1-797. Default Value: 0
1	TSENA	Enables Local timestamp generation: 0 Disabled. 1 Enabled. A Power-on reset clears this bit to 0. Default Value: 0
0	ITMENA	Enables the ITM: 0 Disabled. 1 Enabled. This is the master enable for the ITM unit. A debugger must set this bit to 1 to permit writes to all Stimulus Port registers. A Power-on reset clears this bit to 0. Default Value: 0

CM4_ITM_LAR

Lock Access Register
Address: 0xE0000FB0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				ACCESS_CODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	ACCESS_CODE	Write Access Code. A write of 0xC5ACCE55 enables further write access to this device. An invalid write will have the affect of removing write access. If LOCKSTATUS[2] is set, then only bits [7:0] of this register are implemented and lock access is obtained by consecutively writing 0xC5, 0xAC, 0xCE, 0x55. Bits [31:8] are unused and any writes to them ignored. Default Value: 0

CM4_ITM_LSR

Lock Status Register
Address: 0xE0000FB4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					IMPLEMENTS_8B	ACCESS_PERMITTED	EXISTS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	IMPLEMENTS_8B	This component implements an 8-bit Lock Access Register. Default Value: 0
1	ACCESS_PERMITTED	The values of this bit mean: 0 = Access permitted. 1 = Write access to the component is blocked. All writes to control registers are ignored. Reads are permitted Default Value: 0
0	EXISTS	Indicates that a lock control mechanism exists for this device Default Value: 0

CM4_ITM_PID4

Peripheral Identification Register 4.
Address: 0xE0000FD0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000004

CM4_ITM_PID5

Peripheral Identification Register 5.
Address: 0xE0000FD4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

CM4_ITM_PID6

Peripheral Identification Register 6.
Address: 0xE0000FD8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

CM4_ITM_PID7

Peripheral Identification Register 7.
Address: 0xE0000FDC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

CM4_ITM_PID0

Peripheral Identification Register 0.
Address: 0xE0000FE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000001

CM4_ITM_PID1

Peripheral Identification Register 1.
Address: 0xE0000FE4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x000000B0

CM4_ITM_PID2

Peripheral Identification Register 2.
Address: 0xE0000FE8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x0000003B

CM4_ITM_PID3

Peripheral Identification Register 3.
Address: 0xE0000FEC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None			
HW Access	R				None			
Name	ECOREVNUM [7:4]				None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	ECOREVNUM	ECO revision Default Value: 0x0

CM4_ITM_CID0

Component Identification Register 0.
Address: 0xE0000FF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x0000000D

CM4_ITM_CID1

Component Identification Register 1.
Address: 0xE0000FF4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x000000E0

CM4_ITM_CID2

Component Identification Register 2.
Address: 0xE0000FF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000005

CM4_ITM_CID3

Component Identification Register 3.
Address: 0xE0000FFC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x000000B1

CM0P_DWT_DWT_CTRL

Watchpoint Comparator Configuration
Address: 0xE0001000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R				None			
HW Access					None			
Name	NUMCOMP [31:28]				None [27:24]			

Bits	Name	Description
31 : 28	NUMCOMP	Number of comparators available Default Value: 2

CM4_DWT_CTRL

Control register
Address: 0xE0001000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				RW
HW Access	R			R				R
Name	POSTINIT [7:5]			POSTPRESET [4:1]				CYCCNTENA

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW		RW	RW
HW Access	None			R	R		R	R
Name	None [15:13]			PCSAMPLENA	SYNCTAP [11:10]		CYCTAP	POSTINIT

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW	RW	RW	RW	RW	RW	RW
HW Access	None	R	R	R	R	R	R	R
Name	None	CYCEVTENA	FOLDEVTENA	LSUEVTENA	SLEEPEVTENA	EXCEVTENA	CPIEVTENA	EXCTRCENA

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW	RW	RW	RW
HW Access	R				R	R	R	R
Name	NUMCOMP [31:28]				NOTRCPKT	NOEXTTRIG	NOCYCCNT	NOPRFCNT

Bits	Name	Description
31 : 28	NUMCOMP	Number of comparators implemented. A value of zero indicates no comparator support. These bits are read-only. Default Value: 4
27	NOTRCPKT	Shows whether the implementation supports trace sampling and exception tracing: 0 Trace sampling and exception tracing supported. 1 Trace sampling and exception tracing not supported. If this bit is RAZ, the NOCYCCNT bit must also RAZ. This bit is read-only. Default Value: 0
26	NOEXTTRIG	Shows whether the implementation includes external match signals, CMPMATCH[N]: 0 CMPMATCH[N] supported. 1 CMPMATCH[N] not supported. This bit is read-only. Default Value: 0

25	NOCYCCNT	Shows whether the implementation supports a cycle counter: 0 Cycle counter supported. 1 Cycle counter not supported. For more information see CYCCNT cycle counter and related timers on Arm TRM page C1-792. This bit is read-only. Default Value: 0
24	NOPRFCNT	Shows whether the implementation supports the profiling counters: 0 Supported. 1 Not supported. For more information see Profiling counter support on Arm TRM page C1-794. This bit is read-only. Default Value: 0
22	CYCEVTENA	Enables POSTCNT underflow Event counter packets generation: 0 No POSTCNT underflow packets generated. 1 POSTCNT underflow packets generated, if PCSAMPLENA set to 0. See The POSTCNT timer on Arm TRM page C1-792 for more information. This bit is UNK/SBZP if the NOTRCPKT bit is RAO or the NOCYCCNT bit is RAO. Default Value: 0
21	FOLDEVTENA	Enables generation of the Folded-instruction counter overflow event: 0 Disabled. 1 Enabled. This bit is UNK/SBZP if the NOPRFCNT bit is RAO. Default Value: 0
20	LSUEVTENA	Enables generation of the LSU counter overflow event. 0 Disabled. 1 Enabled. This bit is UNK/SBZP if the NOPRFCNT bit is RAO. Default Value: 0
19	SLEEPEVTENA	Enables generation of the Sleep counter overflow event. 0 Disabled. 1 Enabled. This bit is UNK/SBZP if the NOPRFCNT bit is RAO. Default Value: 0
18	EXCEVTENA	Enables generation of the Exception overhead counter overflow event: 0 Disabled. 1 Enabled. This bit is UNK/SBZP if the NOPRFCNT bit is RAO. Default Value: 0
17	CPIEVTENA	Enables generation of the CPI counter overflow event: 0 Disabled. 1 Enabled. This bit is UNK/SBZP if the NOPRFCNT bit is RAO. Default Value: 0

16	EXCTRCENA	Enables generation of exception trace: 0 Disabled. 1 Enabled. This bit is UNK/SBZP if the NOTRCPKT bit is RAO. Default Value: 0
12	PCSAMPLENA	Enables use of POSTCNT counter as a timer for Periodic PC sample packet generation: 0 No Periodic PC sample packets generated. 1 Periodic PC sample packets generated. See The POSTCNT timer on Arm TRM page C1-792 for more information. This bit is UNK/SBZP if the NOTRCPKT bit is RAO or the NOCYCCNT bit is RAO. Default Value: 0
11 : 10	SYNCTAP	Selects the position of the synchronization packet counter tap on the CYCCNT counter. This determines the Synchronization packet rate: 00 Disabled. No Synchronization packets. 01 Synchronization counter tap at CYCCNT[24]. 10 Synchronization counter tap at CYCCNT[26]. 11 Synchronization counter tap at CYCCNT[28]. For more information see The synchronization packet timer on Arm TRM page C1-794. This field is UNK/SBZP if the NOCYCCNT bit is RAO. Default Value: 0
9	CYCTAP	Selects the position of the POSTCNT tap on the CYCCNT counter: 0 POSTCNT tap at CYCCNT[6]. 1 POSTCNT tap at CYCCNT[10]. For more information see The POSTCNT timer on page C1-792. This bit is UNK/SBZP if the NOCYCCNT bit is RAO. Default Value: 0
8 : 5	POSTINIT	Initial value for the POSTCNT counter. For more information see Enabling POSTCNT, and behavior of accesses to the DWT_CTRL.POSTINIT field and The POSTCNT timer on Arm TRM page C1-792. This field is UNK/SBZP if the NOCYCCNT bit is RAO. Note This field was previously called POSTCNT. The changed name gives a better indication of its function. Default Value: 0

4 : 1	POSTPRESET	Reload value for the POSTCNT counter. For more information see The POSTCNT timer on Arm TRM page C1-792. This field is UNK/SBZP if the NOCYCCNT bit is RAO. Default Value: 0
0	CYCCNTENA	Enables CYCCNT: 0 Disabled. 1 Enabled. This bit is UNK/SBZP if the NOCYCCNT bit is RAO. Default Value: 0

CM4_DWT_CYCCNT

Cycle Count register
Address: 0xE0001004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CYCNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CYCNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	CYCNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	CYCNT [31:24]							

Bits	Name	Description
31 : 0	CYCNT	Incrementing cycle counter value. When enabled, CYCCNT increments on each processor clock cycle. On overflow, CYCCNT wraps to zero. Default Value: 0

CM4_DWT_CPICNT

CPI Count register
Address: 0xE0001008
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CPICNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CPICNT	Base instruction overhead counter. Counts one on each cycle when all of the following are true: - No instruction is executed. - No load-store operation is in progress, see LSU Count register, DWT_LSUCNT on page C1-803. - No exception-entry or exception-exit operation is in progress, see Exception Overhead Count register, DWT_EXCCNT on Arm TRM page C1-802. - Not in a power saving mode, see Sleep Count register, DWT_SLEEPCNT on page C1-802. The definition of "no instruction is executed" is IMPLEMENTATION DEFINED. ARM recommends that this counts each cycle on which no instruction is retired. An event is emitted on counter overflow. Initialized to zero when DWT_CTRL.CPIEVTENA transitions from 0 to 1. Default Value: 0

CM4_DWT_EXCCNT

Exception Overhead Count register
Address: 0xE000100C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EXCCNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EXCCNT	The exception overhead counter. Counts one on each cycle when all of the following are true: - No instruction is executed, see CPI Count register, DWT_CPICNT on Arm TRM page C1-801. - An exception-entry or exception-exit related operation is in progress. Exception-entry or exception-exit related operations include the stacking of registers on exception entry, unstacking of registers on exception exit, and preemption. An event is emitted on counter overflow. Initialized to zero when DWT_CTRL.EXCEVTENA transitions from 0 to 1. Default Value: 0

CM4_DWT_SLEEPCNT

Sleep Count register
Address: 0xE0001010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	SLEEPCNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	SLEEPCNT	Sleep counter. Counts one on each cycle when all of the following are true: - No instruction is executed, see CPI Count register, DWT_CPICNT on page C1-801. - No load-store operation is in progress, see LSU Count register, DWT_LSUCNT. - No exception-entry or exception-exit operation is in progress, see Exception Overhead Count register, DWT_EXCCNT on Arm TRM page C1-802. - In a power saving mode. Power saving modes include WFI, WFE, and Sleep on exit, see Power management on page B1-616. Default Value: 0

CM4_DWT_LSUCNT

LSU Count register
Address: 0xE0001014
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	LSUCNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	LSUCNT	Load-store overhead counter. Counts one on each cycle when all of the following are true: - No instruction is executed, see CPI Count register, DWT_CPICNT on page C1-801. - No exception-entry or exception-exit operation is in progress, see Exception Overhead Count register, DWT_EXCCNT on Arm TRM page C1-802. - A load-store operation is in progress. Default Value: 0

CM4_DWT_FOLDCNT

Folded-instruction Count register
Address: 0xE0001018
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	FOLDCNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	FOLDCNT	Foldedinstructioncounter.Countsoneachcyclewhenatleasttwoinstructionsare executed. The counter is incremented by the number of instructions executed, minus one. At least one instruction is executed is the opposite of No instruction is executed. See CPI Count register, DWT_CPICNT on Arm TRM page C1-801. An event is emitted on counter overflow. Initialized to zero when DWT_CTRL.LSUEVTENA transitions from 0 to 1. Default Value: 0

CM0P_DWT_DWT_PCSR

Watchpoint Comparator PC Sample
Address: 0xE000101C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	EIASAMPLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	EIASAMPLE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	EIASAMPLE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	EIASAMPLE [31:24]							

Bits	Name	Description
31 : 0	EIASAMPLE	Executed Instruction Address sample value Default Value: X

CM4_DWT_PCSR

Program Counter Sample Register
Address: 0xE000101C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EIASAMPLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	EIASAMPLE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	EIASAMPLE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	EIASAMPLE [31:24]							

Bits	Name	Description
31 : 0	EIASAMPLE	Executed Instruction Address sample value. Default Value: 0

CM0P_DWT_DWT_COMP0

Watchpoint Comparator Compare Value
Address: 0xE0001020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COMP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	COMP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	COMP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	COMP [31:24]							

Bits	Name	Description
31 : 0	COMP	Reference value for comparison. See The DWT comparators on Arm TRM page C1-341. Default Value: X

CM4_DWT_COMP0

Comparator registers
Address: 0xE0001020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COMP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	COMP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	COMP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	COMP [31:24]							

Bits	Name	Description
31 : 0	COMP	Reference value for comparison. Default Value: 0

CM0P_DWT_DWT_MASK0

Watchpoint Comparator Mask
Address: 0xE0001024
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MASK [31:24]							

Bits	Name	Description
31 : 0	MASK	The size of the ignore mask applied to address range matching. See The DWT comparators on page C1-341 for the usage model. The mask range is IMPLEMENTATION DEFINED. Writing all ones to this field and reading it back can be used to determine the maximum mask size supported. Default Value: X

CM4_DWT_MASK0

Comparator Mask registers
Address: 0xE0001024
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			MASK [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	MASK	The size of the ignore mask, 0-31 bits, applied to address range matching. The maximum mask size is IMPLEMENTATION DEFINED. A debugger can write 0b11111 to this field and then read the register back to determine the maximum mask size supported. Default Value: 0

CM0P_DWT_DWT_FUNCTION0

Watchpoint Comparator Function
Address: 0xE0001028
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				FUNCTION [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							RW
Name	None [31:25]							MATCHED

Bits	Name	Description
24	MATCHED	Comparator match. It indicates that the operation defined by FUNCTION has occurred since the bit was last read: 0 the associated comparator has matched. 1 the associated comparator has not matched. Reading the register clears this bit to 0. Default Value: 0
3 : 0	FUNCTION	Select action on comparator match. Default Value: 0
		0x0: DISABLE : Disabled
		0x4: IADDR : PC watchpoint event
		0x5: DADDR_RO : Watchpoint event
		0x6: DADDR_WO : Watchpoint event
		0x7: DADDR_RW : Watchpoint event

CM4_DWT_FUNCTION0

Comparator Function registers
Address: 0xE0001028
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None	RW	None	RW			
HW Access	R	None	R	None	R			
Name	CYCMATCH	None	EMITRANGE	None	FUNCTION [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW		RW	RW
HW Access	R				R		R	R
Name	DATAVADDR0 [15:12]				DATAVSIZE [11:10]		LNK1ENA	DATAVMATCH

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				DATAVADDR1 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							MATCHED

Bits	Name	Description
24	MATCHED	Comparator match: 0 No match. 1 Match. A value of 1 indicates that the operation defined by the FUNCTION field occurred since the last read of the register Reading the register clears this bit to 0. This bit is read-only. Default Value: 0
19 : 16	DATAVADDR1	When the DATAVMATCH and LNK1ENA bits are both 1, this field can hold the comparator number of a second comparator to use for linked address comparison. For more information see LinkAddr support on Arm TRM page C1-789. The DWT unit ignores the value of this field unless the LNK1ENA bit is RAO and the DATAVMATCH bit is set to 1. If LNK1ENA is RAZ, this field is RAZ/WI. Default Value: 0

15 : 12	DATAVADDR0	When the DATAVMATCH bit is set to 1 this field can hold the comparator number of a comparator to use for linked address comparison. For more information see LinkAddr support on Arm TRM page C1-789. The DWT unit ignores the value of this field if the DATAVMATCH bit is set to 0. Default Value: 0
11 : 10	DATAVSIZE	For data value matching, specifies the size of the required data comparison: 00 Byte. 01 Halfword. 10 Word. The value 0b11 is reserved. Using this value means behavior is UNPREDICTABLE. Default Value: 0
9	LNK1ENA	Indicates whether the implementation supports use of a second linked comparator: 0 Second linked comparator not supported. 1 Second linked comparator supported. When LNK1ENA is RAO, the DATAVADDR1 field specifies the comparator to use as the second linked comparator. This bit is read-only Default Value: 0
8	DATAVMATCH	Enables data value comparison, if supported: 0 Perform address comparison. 1 Perform data value comparison. For comparator 0, when the CYCMATCH is set to 1, DATAVMATCH must be set to 0 for it to perform cycle count comparison. See LNK1ENA, DATAVSIZE, DATAVADDR0 and DATAVADDR1 for related information. If the implementation does not support data value comparison this bit is RAZ/WI. Default Value: 0
7	CYCMATCH	DWT_FUNCTION0 only. If the implementation supports cycle counting, enable cycle count comparison for comparator 0: 0 No comparison is performed. 1 Compare DWT_COMP0 with the cycle counter, DWT_CYCCNT. If DWT_CTRL.NOCYCCNT is RAZ then this bit is UNK/SBZP. Default Value: 0

5	EMITRANGE	If the implementation supports trace sampling, enables generation of Data trace address packets, that hold Daddr[15:0]: 0 Data trace address packets disabled. 1 Enable Data trace address packet generation. For more information see Address comparison functions on Arm TRM page C1-781. If DWT_CTRL.NOTRCPKT is RAZ then this bit is UNK/SBZP. Default Value: 0
3 : 0	FUNCTION	Selects action taken on comparator match: 0000 = Disabled or LinkAddr(), see LinkAddr support on Arm TRM page C1-789. For non-zero values: - If DATAVMATCH is set to 1, see Table C1-16 on Arm TRM page C1-786 - If DATAVMATCH is set to 0 then: - If CYCMATCH is set to 0, see Table C1-14 on Arm TRM page C1-782 - If CYCMATCH is set to 1, see Table C1-15 on Arm TRM page C1-785. This field resets to zero. Default Value: 0

CM0P_DWT_DWT_COMP1

Watchpoint Comparator Compare Value
Address: 0xE0001030
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COMP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	COMP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	COMP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	COMP [31:24]							

Bits	Name	Description
31 : 0	COMP	Reference value for comparison. See The DWT comparators on Arm TRM page C1-341. Default Value: X

CM4_DWT_COMP1

Comparator registers
Address: 0xE0001030
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COMP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	COMP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	COMP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	COMP [31:24]							

Bits	Name	Description
31 : 0	COMP	Reference value for comparison. Default Value: 0

CM0P_DWT_DWT_MASK1

Watchpoint Comparator Mask
Address: 0xE0001034
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MASK [31:24]							

Bits	Name	Description
31 : 0	MASK	The size of the ignore mask applied to address range matching. See The DWT comparators on Arm TRM page C1-341 for the usage model. The mask range is IMPLEMENTATION DEFINED. Writing all ones to this field and reading it back can be used to determine the maximum mask size supported. Default Value: X

CM4_DWT_MASK1

Comparator Mask registers
Address: 0xE0001034
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			MASK [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	MASK	The size of the ignore mask, 0-31 bits, applied to address range matching. The maximum mask size is IMPLEMENTATION DEFINED. A debugger can write 0b11111 to this field and then read the register back to determine the maximum mask size supported. Default Value: 0

CM4_DWT_FUNCTION1

Comparator Function registers
Address: 0xE0001038
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None	RW	None	RW			
HW Access	R	None	R	None	R			
Name	CYCMATCH	None	EMITRANGE	None	FUNCTION [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW		RW	RW
HW Access	R				R		R	R
Name	DATAVADDR0 [15:12]				DATAVSIZE [11:10]		LNK1ENA	DATAVMATCH

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				DATAVADDR1 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							MATCHED

Bits	Name	Description
24	MATCHED	Comparator match: 0 No match. 1 Match. A value of 1 indicates that the operation defined by the FUNCTION field occurred since the last read of the register Reading the register clears this bit to 0. This bit is read-only. Default Value: 0
19 : 16	DATAVADDR1	When the DATAVMATCH and LNK1ENA bits are both 1, this field can hold the comparator number of a second comparator to use for linked address comparison. For more information see LinkAddr support on Arm TRM page C1-789. The DWT unit ignores the value of this field unless the LNK1ENA bit is RAO and the DATAVMATCH bit is set to 1. If LNK1ENA is RAZ, this field is RAZ/WI. Default Value: 0

15 : 12	DATAVADDR0	When the DATAVMATCH bit is set to 1 this field can hold the comparator number of a comparator to use for linked address comparison. For more information see LinkAddr support on Arm TRM page C1-789. The DWT unit ignores the value of this field if the DATAVMATCH bit is set to 0. Default Value: 0
11 : 10	DATAVSIZE	For data value matching, specifies the size of the required data comparison: 00 Byte. 01 Halfword. 10 Word. The value 0b11 is reserved. Using this value means behavior is UNPREDICTABLE. Default Value: 0
9	LNK1ENA	Indicates whether the implementation supports use of a second linked comparator: 0 Second linked comparator not supported. 1 Second linked comparator supported. When LNK1ENA is RAO, the DATAVADDR1 field specifies the comparator to use as the second linked comparator. This bit is read-only Default Value: 0
8	DATAVMATCH	Enables data value comparison, if supported: 0 Perform address comparison. 1 Perform data value comparison. For comparator 0, when the CYCMATCH is set to 1, DATAVMATCH must be set to 0 for it to perform cycle count comparison. See LNK1ENA, DATAVSIZE, DATAVADDR0 and DATAVADDR1 for related information. If the implementation does not support data value comparison this bit is RAZ/WI. Default Value: 0
7	CYCMATCH	DWT_FUNCTION0 only. If the implementation supports cycle counting, enable cycle count comparison for comparator 0: 0 No comparison is performed. 1 Compare DWT_COMP0 with the cycle counter, DWT_CYCCNT. If DWT_CTRL.NOCYCCNT is RAZ then this bit is UNK/SBZP. Default Value: 0

5	EMITRANGE	If the implementation supports trace sampling, enables generation of Data trace address packets, that hold Daddr[15:0]: 0 Data trace address packets disabled. 1 Enable Data trace address packet generation. For more information see Address comparison functions on Arm TRM page C1-781. If DWT_CTRL.NOTRCPKT is RAZ then this bit is UNK/SBZP. Default Value: 0
3 : 0	FUNCTION	Selects action taken on comparator match: 0000 = Disabled or LinkAddr(), see LinkAddr support on Arm TRM page C1-789. For non-zero values: - If DATAVMATCH is set to 1, see Table C1-16 on Arm TRM page C1-786 - If DATAVMATCH is set to 0 then: - If CYCMATCH is set to 0, see Table C1-14 on Arm TRM page C1-782 - If CYCMATCH is set to 1, see Table C1-15 on Arm TRM page C1-785. This field resets to zero. Default Value: 0

CM4_DWT_COMP2

Comparator registers
Address: 0xE0001040
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COMP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	COMP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	COMP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	COMP [31:24]							

Bits	Name	Description
31 : 0	COMP	Reference value for comparison. Default Value: 0

CM4_DWT_FUNCTION2

Comparator Function registers
Address: 0xE0001048
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None	RW	None	RW			
HW Access	R	None	R	None	R			
Name	CYCMATCH	None	EMITRANGE	None	FUNCTION [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW		RW	RW
HW Access	R				R		R	R
Name	DATAVADDR0 [15:12]				DATAVSIZE [11:10]		LNK1ENA	DATAVMATCH

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				DATAVADDR1 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							MATCHED

Bits	Name	Description
24	MATCHED	Comparator match: 0 No match. 1 Match. A value of 1 indicates that the operation defined by the FUNCTION field occurred since the last read of the register Reading the register clears this bit to 0. This bit is read-only. Default Value: 0
19 : 16	DATAVADDR1	When the DATAVMATCH and LNK1ENA bits are both 1, this field can hold the comparator number of a second comparator to use for linked address comparison. For more information see LinkAddr support on Arm TRM page C1-789. The DWT unit ignores the value of this field unless the LNK1ENA bit is RAO and the DATAVMATCH bit is set to 1. If LNK1ENA is RAZ, this field is RAZ/WI. Default Value: 0

15 : 12	DATAVADDR0	When the DATAVMATCH bit is set to 1 this field can hold the comparator number of a comparator to use for linked address comparison. For more information see LinkAddr support on Arm TRM page C1-789. The DWT unit ignores the value of this field if the DATAVMATCH bit is set to 0. Default Value: 0
11 : 10	DATAVSIZE	For data value matching, specifies the size of the required data comparison: 00 Byte. 01 Halfword. 10 Word. The value 0b11 is reserved. Using this value means behavior is UNPREDICTABLE. Default Value: 0
9	LNK1ENA	Indicates whether the implementation supports use of a second linked comparator: 0 Second linked comparator not supported. 1 Second linked comparator supported. When LNK1ENA is RAO, the DATAVADDR1 field specifies the comparator to use as the second linked comparator. This bit is read-only Default Value: 0
8	DATAVMATCH	Enables data value comparison, if supported: 0 Perform address comparison. 1 Perform data value comparison. For comparator 0, when the CYCMATCH is set to 1, DATAVMATCH must be set to 0 for it to perform cycle count comparison. See LNK1ENA, DATAVSIZE, DATAVADDR0 and DATAVADDR1 for related information. If the implementation does not support data value comparison this bit is RAZ/WI. Default Value: 0
7	CYCMATCH	DWT_FUNCTION0 only. If the implementation supports cycle counting, enable cycle count comparison for comparator 0: 0 No comparison is performed. 1 Compare DWT_COMP0 with the cycle counter, DWT_CYCCNT. If DWT_CTRL.NOCYCCNT is RAZ then this bit is UNK/SBZP. Default Value: 0

5	EMITRANGE	If the implementation supports trace sampling, enables generation of Data trace address packets, that hold Daddr[15:0]: 0 Data trace address packets disabled. 1 Enable Data trace address packet generation. For more information see Address comparison functions on Arm TRM page C1-781. If DWT_CTRL.NOTRCPKT is RAZ then this bit is UNK/SBZP. Default Value: 0
3 : 0	FUNCTION	Selects action taken on comparator match: 0000 = Disabled or LinkAddr(), see LinkAddr support on Arm TRM page C1-789. For non-zero values: - If DATAVMATCH is set to 1, see Table C1-16 on Arm TRM page C1-786 - If DATAVMATCH is set to 0 then: - If CYCMATCH is set to 0, see Table C1-14 on Arm TRM page C1-782 - If CYCMATCH is set to 1, see Table C1-15 on Arm TRM page C1-785. This field resets to zero. Default Value: 0

CM4_DWT_FUNCTION3

Comparator Function registers
Address: 0xE0001058
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None	RW	None	RW			
HW Access	R	None	R	None	R			
Name	CYCMATCH	None	EMITRANGE	None	FUNCTION [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW		RW	RW
HW Access	R				R		R	R
Name	DATAVADDR0 [15:12]				DATAVSIZE [11:10]		LNK1ENA	DATAVMATCH

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				DATAVADDR1 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							MATCHED

Bits	Name	Description
24	MATCHED	Comparator match: 0 No match. 1 Match. A value of 1 indicates that the operation defined by the FUNCTION field occurred since the last read of the register Reading the register clears this bit to 0. This bit is read-only. Default Value: 0
19 : 16	DATAVADDR1	When the DATAVMATCH and LNK1ENA bits are both 1, this field can hold the comparator number of a second comparator to use for linked address comparison. For more information see LinkAddr support on Arm TRM page C1-789. The DWT unit ignores the value of this field unless the LNK1ENA bit is RAO and the DATAVMATCH bit is set to 1. If LNK1ENA is RAZ, this field is RAZ/WI. Default Value: 0

15 : 12	DATAVADDR0	When the DATAVMATCH bit is set to 1 this field can hold the comparator number of a comparator to use for linked address comparison. For more information see LinkAddr support on Arm TRM page C1-789. The DWT unit ignores the value of this field if the DATAVMATCH bit is set to 0. Default Value: 0
11 : 10	DATAVSIZE	For data value matching, specifies the size of the required data comparison: 00 Byte. 01 Halfword. 10 Word. The value 0b11 is reserved. Using this value means behavior is UNPREDICTABLE. Default Value: 0
9	LNK1ENA	Indicates whether the implementation supports use of a second linked comparator: 0 Second linked comparator not supported. 1 Second linked comparator supported. When LNK1ENA is RAO, the DATAVADDR1 field specifies the comparator to use as the second linked comparator. This bit is read-only Default Value: 0
8	DATAVMATCH	Enables data value comparison, if supported: 0 Perform address comparison. 1 Perform data value comparison. For comparator 0, when the CYCMATCH is set to 1, DATAVMATCH must be set to 0 for it to perform cycle count comparison. See LNK1ENA, DATAVSIZE, DATAVADDR0 and DATAVADDR1 for related information. If the implementation does not support data value comparison this bit is RAZ/WI. Default Value: 0
7	CYCMATCH	DWT_FUNCTION0 only. If the implementation supports cycle counting, enable cycle count comparison for comparator 0: 0 No comparison is performed. 1 Compare DWT_COMP0 with the cycle counter, DWT_CYCCNT. If DWT_CTRL.NOCYCCNT is RAZ then this bit is UNK/SBZP. Default Value: 0

5	EMITRANGE	If the implementation supports trace sampling, enables generation of Data trace address packets, that hold Daddr[15:0]: 0 Data trace address packets disabled. 1 Enable Data trace address packet generation. For more information see Address comparison functions on Arm TRM page C1-781. If DWT_CTRL.NOTRCPKT is RAZ then this bit is UNK/SBZP. Default Value: 0
3 : 0	FUNCTION	Selects action taken on comparator match: 0000 = Disabled or LinkAddr(), see LinkAddr support on Arm TRM page C1-789. For non-zero values: - If DATAVMATCH is set to 1, see Table C1-16 on Arm TRM page C1-786 - If DATAVMATCH is set to 0 then: - If CYCMATCH is set to 0, see Table C1-14 on Arm TRM page C1-782 - If CYCMATCH is set to 1, see Table C1-15 on Arm TRM page C1-785. This field resets to zero. Default Value: 0

CM0P_DWT_DWT_PID4

Watchpoint Unit CoreSight ROM Table Peripheral ID #4
Address: 0xE0001FD0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 0x00000004

CM4_DWT_PID4

Peripheral Identification Register 4.
Address: 0xE0001FD0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000004

CM4_DWT_PID5

Peripheral Identification Register 5.
Address: 0xE0001FD4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

CM4_DWT_PID6

Peripheral Identification Register 6.
Address: 0xE0001FD8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

CM4_DWT_PID7

Peripheral Identification Register 7.
Address: 0xE0001FDC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

CM0P_DWT_DWT_PID0

Watchpoint Unit CoreSight ROM Table Peripheral ID #0
Address: 0xE0001FE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 0x0000000A

CM4_DWT_PID0

Peripheral Identification Register 0.
Address: 0xE0001FE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000002

CM0P_DWT_DWT_PID1

Watchpoint Unit CoreSight ROM Table Peripheral ID #1
Address: 0xE0001FE4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 0x000000B0

CM4_DWT_PID1

Peripheral Identification Register 1.
Address: 0xE0001FE4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x000000B0

CM0P_DWT_DWT_PID2

Watchpoint Unit CoreSight ROM Table Peripheral ID #2
Address: 0xE0001FE8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 0x0000000B

CM4_DWT_PID2

Peripheral Identification Register 2.
Address: 0xE0001FE8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x0000003B

CM0P_DWT_DWT_PID3

Watchpoint Unit CoreSight ROM Table Peripheral ID #3
Address: 0xE0001FEC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

CM4_DWT_PID3

Peripheral Identification Register 3.
Address: 0xE0001FEC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None			
HW Access	R				None			
Name	ECOREVNUM [7:4]				None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	ECOREVNUM	ECO revision Default Value: 0x0

CM0P_DWT_DWT_CID0

Watchpoint Unit CoreSight ROM Table Component ID #0
Address: 0xE0001FF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 0x0000000D

CM4_DWT_CID0

Component Identification Register 0.
Address: 0xE0001FF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x0000000D

CM0P_DWT_DWT_CID1

Watchpoint Unit CoreSight ROM Table Component ID #1
Address: 0xE0001FF4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 0x000000E0

CM4_DWT_CID1

Component Identification Register 1.
Address: 0xE0001FF4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x000000E0

CM0P_DWT_DWT_CID2

Watchpoint Unit CoreSight ROM Table Component ID #2
Address: 0xE0001FF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 0x00000005

CM4_DWT_CID2

Component Identification Register 2.
Address: 0xE0001FF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000005

CM0P_DWT_DWT_CID3

Watchpoint Unit CoreSight ROM Table Component ID #3
Address: 0xE0001FFC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 0x000000B1

CM4_DWT_CID3

Component Identification Register 3.
Address: 0xE0001FFC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x000000B1

CM0P_BP_BP_CTRL

Breakpoint Unit Control
Address: 0xE0002000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None		RW	RW
HW Access					None		R	R
Name	NUM_CODE [7:4]				None [3:2]		KEY	ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	NUM_CODE	The number of breakpoint comparators. If NUM_CODE is zero, the implementation does not support any comparators. Default Value: 4
1	KEY	RAZ on reads, SBO for writes. If written as zero, the write to the register is ignored. Default Value: 0
0	ENABLE	Enables the BPU: 0 BPU is disabled. 1 BPU is enabled. Default Value: 0

CM4_FPB_CTRL

FlashPatch Control Register
Address: 0xE0002000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				None		RW	RW
HW Access	R				None		R	R
Name	NUM_CODE_LO [7:4]				None [3:2]		KEY	ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW			RW			
HW Access	None	R			R			
Name	None	NUM_CODE_HI [14:12]			NUM_LIT [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				None			
HW Access	R				None			
Name	REV [31:28]				None [27:24]			

Bits	Name	Description
31 : 28	REV	Flash Patch Breakpoint architecture revision: 0000 Flash Patch Breakpoint version 1. 0001 Flash Patch Breakpoint version 2. Supports breakpoints on any location in the 4GB address range. Default Value: 0
14 : 12	NUM_CODE_HI	The most significant bits, being bits[6:4], of NUM_CODE, the number of instruction address comparators, see bits[7:4]. These bits are read only. Default Value: 0
11 : 8	NUM_LIT	The number of literal address comparators supported, starting from NUM_CODE upwards. UNK/SBZP if Flash Patch is not implemented. Flash Patch is not implemented if FP_REMAP[29] is 0. If this field is zero, the implementation does not support literal comparators. These bits are read-only. Default Value: 2

7 : 4	NUM_CODE_LO	The least significant bits, being bits[3:0], of NUM_CODE, the number of instruction address comparators. If NUM_CODE[6:0] is zero, the implementation does not support any instruction address comparators. These bits are read only. Default Value: 6
1	KEY	On any write to FP_CTRL, this bit must be 1. A write to the register with this bit set to zero is ignored. The Flash Patch Breakpoint unit ignores the write unless this bit is 1. This bit is RAZ. Default Value: 0
0	ENABLE	Enable bit for the FPB: 0 Flash Patch Breakpoint disabled. 1 Flash Patch Breakpoint enabled. A Power-on reset clears this bit to 0. Default Value: 0

CM4_FPB_REMAP

FlashPatch Remap register
Address: 0xE0002004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			None				
HW Access	R			None				
Name	REMAP [7:5]			None [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	REMAP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	REMAP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None	RW				
HW Access	R		None	R				
Name	RMPSPT [31:30]		None	REMAP [28:24]				

Bits	Name	Description
31 : 30	RMPSPT	Indicates whether the FPB unit supports flash patch remap: 0 Remapping not supported. The FPB only supports breakpoint functionality. 1 Hard-wired remap to SRAM region. These bits are read only. Default Value: 0
28 : 5	REMAP	If the FPB supports flash patch remap, this field: - Holds bits[28:5] of the base address in SRAM to which the FPB remaps the address. - Has an UNKNOWN value on reset. If the FPB only supports breakpoint functionality this field is UNK/SBZP. Default Value: 0

CM0P_BP_BP_COMP0

Breakpoint Compare Register
Address: 0xE0002008
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	RW
HW Access	R						None	R
Name	COMP_ADDR [7:2]						None	ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	COMP_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	COMP_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None	RW				
HW Access	R		None	R				
Name	MATCH [31:30]		None	COMP_ADDR [28:24]				

Bits	Name	Description
31 : 30	MATCH	BP_MATCH defines the behavior when the COMP address is matched. Default Value: X
		0x0: NONE : No breakpoint matching
		0x1: LOWER : Breakpoint on lower halfword, upper is unaffected.
		0x2: UPPER : Breakpoint on upper halfword, lower is unaffected.
		0x3: BOTH : Breakpoint on both lower and upper halfwords.
28 : 2	COMP_ADDR	Stores bits [28:2] of the comparison address. The comparison address is compared with the address from the Code memory region. Bits [31:29] and [1:0] of the comparison address are zero. Default Value: X
0	ENABLE	Enables the comparator: Note BP_CTRL.ENABLE must also be set to 1 to enable a comparator. Default Value: 0

CM4_FPB_COMP0

FlashPatch Comparator register
Address: 0xE0002008
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	See ARM documentation for details. Default Value: 0

CM0P_BP_BP_COMP1

Breakpoint Compare Register
Address: 0xE000200C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	RW
HW Access	R						None	R
Name	COMP_ADDR [7:2]						None	ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	COMP_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	COMP_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None	RW				
HW Access	R		None	R				
Name	MATCH [31:30]		None	COMP_ADDR [28:24]				

Bits	Name	Description
31 : 30	MATCH	BP_MATCH defines the behavior when the COMP address is matched. Default Value: X
		0x0: NONE : No breakpoint matching
		0x1: LOWER : Breakpoint on lower halfword, upper is unaffected.
		0x2: UPPER : Breakpoint on upper halfword, lower is unaffected.
		0x3: BOTH : Breakpoint on both lower and upper halfwords.
28 : 2	COMP_ADDR	Stores bits [28:2] of the comparison address. The comparison address is compared with the address from the Code memory region. Bits [31:29] and [1:0] of the comparison address are zero. Default Value: X
0	ENABLE	Enables the comparator: Note BP_CTRL.ENABLE must also be set to 1 to enable a comparator. Default Value: 0

CM0P_BP_BP_COMP3

Breakpoint Compare Register
Address: 0xE0002014
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	RW
HW Access	R						None	R
Name	COMP_ADDR [7:2]						None	ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	COMP_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	COMP_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None	RW				
HW Access	R		None	R				
Name	MATCH [31:30]		None	COMP_ADDR [28:24]				

Bits	Name	Description
31 : 30	MATCH	BP_MATCH defines the behavior when the COMP address is matched. Default Value: X
		0x0: NONE : No breakpoint matching
		0x1: LOWER : Breakpoint on lower halfword, upper is unaffected.
		0x2: UPPER : Breakpoint on upper halfword, lower is unaffected.
		0x3: BOTH : Breakpoint on both lower and upper halfwords.
28 : 2	COMP_ADDR	Stores bits [28:2] of the comparison address. The comparison address is compared with the address from the Code memory region. Bits [31:29] and [1:0] of the comparison address are zero. Default Value: X
0	ENABLE	Enables the comparator. Note BP_CTRL.ENABLE must also be set to 1 to enable a comparator. Default Value: 0

CM0P_BP_BP_PID4

Breakpoint Unit CoreSight ROM Table Peripheral ID #4
Address: 0xE0002FD0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 0x00000004

CM4_FPB_PID4

Peripheral Identification Register 4.
Address: 0xE0002FD0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000004

CM4_FPB_PID5

Peripheral Identification Register 5.
Address: 0xE0002FD4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

CM4_FPB_PID6

Peripheral Identification Register 6.
Address: 0xE0002FD8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

CM4_FPB_PID7

Peripheral Identification Register 7.
Address: 0xE0002FDC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

CM0P_BP_BP_PID0

Breakpoint Unit CoreSight ROM Table Peripheral ID #0
Address: 0xE0002FE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 0x0000000B

CM4_FPB_PID0

Peripheral Identification Register 0.
Address: 0xE0002FE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000003

CM0P_BP_BP_PID1

Breakpoint Unit CoreSight ROM Table Peripheral ID #1
Address: 0xE0002FE4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 0x000000B0

CM4_FPB_PID1

Peripheral Identification Register 1.
Address: 0xE0002FE4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x000000B0

CM0P_BP_BP_PID2

Breakpoint Unit CoreSight ROM Table Peripheral ID #2
Address: 0xE0002FE8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 0x0000000B

CM4_FPB_PID2

Peripheral Identification Register 2.
Address: 0xE0002FE8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x0000002B

CM0P_BP_BP_PID3

Breakpoint Unit CoreSight ROM Table Peripheral ID #3
Address: 0xE0002FEC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

CM4_FPB_PID3

Peripheral Identification Register 3.
Address: 0xE0002FEC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None			
HW Access	R				None			
Name	ECOREVNUM [7:4]				None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	ECOREVNUM	ECO revision Default Value: 0x0

CM0P_BP_BP_CID0

Breakpoint Unit CoreSight ROM Table Component ID #0
Address: 0xE0002FF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 0x0000000D

CM4_FPB_CID0

Component Identification Register 0.
Address: 0xE0002FF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x0000000D

CM0P_BP_BP_CID1

Breakpoint Unit CoreSight ROM Table Component ID #1
Address: 0xE0002FF4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 0x000000E0

CM4_FPB_CID1

Component Identification Register 1.
Address: 0xE0002FF4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x000000E0

CM0P_BP_BP_CID2

Breakpoint Unit CoreSight ROM Table Component ID #2
Address: 0xE0002FF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 0x00000005

CM4_FPB_CID2

Component Identification Register 2.
Address: 0xE0002FF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000005

CM0P_BP_BP_CID3

Breakpoint Unit CoreSight ROM Table Component ID #3
Address: 0xE0002FFC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 0x000000B1

CM4_FPB_CID3

Component Identification Register 3.
Address: 0xE0002FFC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x000000B1

CM4_SCS_ACTLR

Auxiliary Control Register
Address: 0xE000E008
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer the following ARM documents for details about CPU register descriptions: ARMV7M : http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0403e.d/index.html CM4 TRM : http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.100166_0001_00_en/index.html Default Value: 0

CM0P_SCS_SYST_CSR

SysTick Control & Status
Address: 0xE000E010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					CLKSOURCE	TICKINT	ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							RW
Name	None [23:17]							COUNTFLAG

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	COUNTFLAG	Indicates whether the counter has counted to "0" since the last read of this register: '0': counter has not counted to "0". '1': counter has counted to "0". COUNTFLAG is set to '1' by a count transition from "1" to "0". COUNTFLAG is cleared to '0' by a read of this register, and by any write to the SYST_CVR register. Default Value: 0
2	CLKSOURCE	Indicates the SysTick counter clock source: '0': SysTick uses the low frequency clock. For this mode to function, the low frequency clock should be less than half the frequency of "clk_sys". '1': SysTick uses the system/processor clock "clk_sys". Note: Low frequency clock can be selected using CPUSS_SYSTICK_CTL.CLOCK_SOURCE field. Default Value: 0

1	TICKINT	Indicates whether counting to "0" causes the status of the SysTick exception to change to pending: '0': count to "0" does not affect the SysTick exception status. '1': count to "0" changes the SysTick exception status to pending. Changing the value of the counter to "0" by writing zero to the SYST_CVR register to "0" never changes the status of the SysTick exception. Default Value: 0
0	ENABLE	Indicates the enabled status of the SysTick counter: '0': counter is disabled. '1': counter is operating. Default Value: 0

CM4_SCS_SYST_CSR

SysTick Control and Status Register
Address: 0xE000E010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_SYST_RVR

SysTick Reload Value
Address: 0xE000E014
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RELOAD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RELOAD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RELOAD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	RELOAD	The value to load into the SYST_CVR register when the counter reaches 0. Default Value: X

CM4_SCS_SYST_RVR

SysTick Reload Value Register
Address: 0xE000E014
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_SYST_CVR

SysTick Current Value
Address: 0xE000E018
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CURRENT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CURRENT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CURRENT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	CURRENT	Current counter value. This is the value of the counter at the time it is sampled. Default Value: X

CM4_SCS_SYST_CVR

SysTick Current Value Register
Address: 0xE000E018
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_SYST_CALIB

SysTick Calibration Value
Address: 0xE000E01C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TENMS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	TENMS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	TENMS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access		RW	None					
Name	NOREF	SKEW	None [29:24]					

Bits	Name	Description
31	NOREF	Indicates whether a implementation defined reference clock is provided: '0': the reference clock is provided. '1': the reference clock is not provided. When this bit is '1', the SYST_CSR.CLKSOURCEis forced to '1' and cannot be cleared to '0'. This field is controlled by CPUSS_SYSTICK_CTL.NOREF field. Default Value: 0
30	SKEW	Indicates whether the 10ms calibration value is exact: '0': 10ms calibration value is exact. '1': 10ms calibration value is inexact, because of the clock frequency. This field is controlled by CPUSS_SYSTICK_CTL.SKEW field. Default Value: X

23 : 0	TENMS	Optionally, holds a reload value to be used for 10ms (100Hz) timing, subject to system clock skew errors. If this field is "0", the calibration value is not known. This field is controlled by CPUSS_SYSTICK_CTL.TENMS field. Default Value: X

CM4_SCS_SYST_CALIB

SysTick Calibration value Register
Address: 0xE000E01C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_ISER

Interrupt Set-Enable Register
Address: 0xE000E100
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	R							
Name	SETENA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	R							
Name	SETENA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	R							
Name	SETENA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	R							
Name	SETENA [31:24]							

Bits	Name	Description
31 : 0	SETENA	Enables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt. Default Value: 0

CM4_SCS_NVIC_ISER0

Interrupt Set-Enable Registers
Address: 0xE000E100
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_ICER

Interrupt Clear Enable Register
Address: 0xE000E180
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	R							
Name	CLRENA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	CLRENA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	R							
Name	CLRENA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	CLRENA [31:24]							

Bits	Name	Description
31 : 0	CLRENA	Disables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt. Default Value: 0

CM4_SCS_NVIC_ICER0

Interrupt Clear-Enable Registers
Address: 0xE000E180
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_ISPR

Interrupt Set-Pending Register
Address: 0xE000E200
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	R							
Name	SETPEND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	R							
Name	SETPEND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	R							
Name	SETPEND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	R							
Name	SETPEND [31:24]							

Bits	Name	Description
31 : 0	SETPEND	Changes the state of one or more interrupts to pending. Each bit corresponds to the same numbered interrupt. Default Value: 0

CM4_SCS_NVIC_ISPR0

Interrupt Set-Pending Registers
Address: 0xE000E200
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_ICPR

Interrupt Clear-Pending Register
Address: 0xE000E280
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [31:24]							

Bits	Name	Description
31 : 0	CLRPEND	Changes the state of one or more interrupts to not pending. Each bit corresponds to the same numbered interrupt. Default Value: 0

CM4_SCS_NVIC_ICPR0

Interrupt Clear-Pending Registers
Address: 0xE000E280
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM4_SCS_NVIC_IABR0

Interrupt Active Bit Registers
Address: 0xE000E300
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_IPR0

Interrupt Priority Registers
Address: 0xE000E400
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

CM4_SCS_NVIC_IPR0

Interrupt Priority Registers
Address: 0xE000E400
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_CPUID

CPUID Register
Address: 0xE000ED00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access								
Name	PARTNO [7:4]				REVISION [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	PARTNO [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access								
Name	VARIANT [23:20]				CONSTANT [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	IMPLEMENTER [31:24]							

Bits	Name	Description
31 : 24	IMPLEMENTER	Implementer code for ARM. Default Value: 0x41
23 : 20	VARIANT	Implementation defined. In ARM implementations this is the major revision number n in the rn part of the rnpn revision status, Product revision status on Arm TRM page xii. Default Value: 0
19 : 16	CONSTANT	Indicates the architecture, ARMv6-M Default Value: 0xC
15 : 4	PARTNO	Indicates part number, Cortex-M0+ Default Value: 0xC60
3 : 0	REVISION	Indicates revision. In ARM implementations this is the minor revision number n in the pn part of the rnpn revision status, see Product revision status on Arm TRM page xii. For release r0p1. Default Value: 1

CM4_SCS_CPUID

CPUID Base Register
Address: 0xE000ED00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_ICSR

Interrupt Control State Register
Address: 0xE000ED04
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VECTACTIVE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				None			R
HW Access	RW				None			RW
Name	VECTPENDING [15:12]				None [11:9]			VECTACTIVE

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	None	R				
HW Access	RW	RW	None	RW				
Name	ISRPREEMPT	ISRPENDING	None	VECTPENDING [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	None		RW1S	RW1C	RW1S	RW1C	None
HW Access	RW	None		RW	R	RW	R	None
Name	NMIPENDSET	None [30:29]		PENDSVSET	PENDSVCLR	PENDSTSETb	PENDSTCLR	None

Bits	Name	Description
31	NMIPENDSET	Activates an NMI exception or reads back the current state. Because NMI is the highest priority exception, it activates as soon as it is registered. Default Value: 0
28	PENDSVSET	Sets a pending PendSV interrupt or reads back the current state. Use this normally to request a context switch. Writing PENDSVSET and PENDSVCLR to '1' concurrently is UNPREDICTABLE. Default Value: 0
27	PENDSVCLR	Clears a pending PendSV interrupt. Default Value: 0
26	PENDSTSETb	Sets a pending SysTick or reads back the current state. Writing PENDSTSET and PENDSTCLR to '1' concurrently is UNPREDICTABLE. Default Value: 0

25	PENDSTCLR	Clears a pending SysTick, whether set here or by the timer hardware. Default Value: 0
23	ISRPREEMPT	Indicates whether a pending exception will be serviced on exit from debug halt state. Default Value: 0
22	ISRPENDING	Indicates if an external configurable, NVIC generated, interrupt is pending. Default Value: 0
20 : 12	VECTPENDING	The exception number for the highest priority pending exception. 0= No pending exceptions. The pending state includes the effect of memory-mapped enable and mask registers. It does not include the PRIMASK special-purpose register qualifier. Default Value: 0
8 : 0	VECTACTIVE	The exception number for the current executing exception. 0= Thread mode. This is the same value as IPSR[8:0] Default Value: 0

CM4_SCS_ICSR

Interrupt Control and State Register
Address: 0xE000ED04
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_VTOR

Vector Table Offset Register
Address: 0xE000ED08
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TBLOFF [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TBLOFF [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	TBLOFF [31:24]							

Bits	Name	Description
31 : 8	TBLOFF	Table offset address. All bits of the Vector table address that are not defined by the VTOR are zero. Default Value: 0

CM4_SCS_VTOR

Vector Table Offset Register
Address: 0xE000ED08
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_AIRCR

Application Interrupt and Reset Control Register
Address: 0xE000ED0C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1C	None
HW Access	None					R	R	None
Name	None [7:3]					SYSRESETREQ	VECTCLRACTIVE	None

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access		None						
Name	ENDIANNESS	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VECTKEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VECTKEY [31:24]							

Bits	Name	Description
31 : 16	VECTKEY	Vector Key. The value 0x05FA must be written to this register, otherwise the register write is not performed. Default Value: X
15	ENDIANNESS	Indicates the memory system data endianness: 0 little endian 1 big endian. See Endian support on page A3-44 for more information. Default Value: 0
2	SYSRESETREQ	System Reset Request. Writing 1 to this bit asserts a signal to request a reset by the external system. This will cause a full system reset of the CPU and all other components in the device. See Reset management on Arm TRM page B1-240 for more information. Default Value: 0

1	VECTCLRACTIVE	Clears all active state information for fixed and configurable exceptions. The effect of writing a 1 to this bit if the processor is not halted in Debug state is UNPREDICTABLE. Default Value: 0

CM4_SCS_AIRCR

Application Interrupt and Reset Control Register
Address: 0xE000ED0C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_SCR

System Control Register
Address: 0xE000ED10
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	None
HW Access	None			R	None	R	R	None
Name	None [7:5]			SEVONPEND	None	SLEEPDEEP	SLEEPONEXIT	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	SEVONPEND	Determines whether an interrupt transition from inactive state to pending state is a wakeup event: 0: transitions from inactive to pending are not wakeup events. 1: transitions from inactive to pending are wakeup events. See WFE on Arm TRM page A6-197 for more information. Default Value: 0
2	SLEEPDEEP	An implementation can use this bit to select DeepSleep power modes upon execution of WFI/WFE: 0: Select Sleep mode 1: Select DeepSleep Default Value: 0
1	SLEEPONEXIT	Determines whether, on an exit from an ISR that returns to the base level of execution priority, the processor enters a sleep state: 0 do not enter sleep state. 1 enter sleep state. See Power management on Arm TRM page B1-240 for more information. Default Value: 0

CM4_SCS_SCR

System Control Register
Address: 0xE000ED10
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_CCR

Configuration and Control Register
Address: 0xE000ED14
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	None		
HW Access	None					None		
Name	None [7:4]				UNALIGN_TRP	None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	None
HW Access	None							None
Name	None [15:10]						STKALIGN	None

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	STKALIGN	1: On exception entry, the SP used prior to the exception is adjusted to be 8-byte aligned and the context to restore it is saved. The SP is restored on the associated exception return. Default Value: 1
3	UNALIGN_TRP	1: unaligned word and halfword accesses generate a HardFault exception. Default Value: 1

CM4_SCS_CCR

Configuration and Control Register
Address: 0xE000ED14
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM4_SCS_SHPR1

System Handler Priority Register 1
Address: 0xE000ED18
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_SHPR2

System Handler Priority Register 2
Address: 0xE000ED1C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_11 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_11	Priority of system handler 11, SVCall Default Value: 0

CM4_SCS_SHPR2

System Handler Priority Register 2
Address: 0xE000ED1C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_SHPR3

System Handler Priority Register 3
Address: 0xE000ED20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_14 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_15 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_15	Priority of system handler 15, SysTick Default Value: 0
23 : 22	PRI_14	Priority of system handler 14, PendSV Default Value: 0

CM4_SCS_SHPR3

System Handler Priority Register 3
Address: 0xE000ED20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_SHCSR

System Handler Control and State Register
Address: 0xE000ED24
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None						
HW Access	RW	None						
Name	SVCALLPENDED	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	SVCALLPENDED	0 SVCall is not pending. 1 SVCall is pending. This bit reflects the pending state on a read, and updates the pending state, to the value written, on a write. (Pending state bits are set to 1 when an exception occurs, and are cleared to 0 when an exception becomes active.) Default Value: 0

CM4_SCS_SHCSR

System Handler Control and State Register
Address: 0xE000ED24
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM4_SCS_CFSR

Configurable Fault Status Register
Address: 0xE000ED28
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM4_SCS_HFSR

HardFault Status Register
Address: 0xE000ED2C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_DFSR

Debug Fault Status Register
Address: 0xE000ED30
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None			RW1S	RW1S	RW1S	RW1S	RW1S
Name	None [7:5]			EXTERNAL	VCATCH	DWTTRAP	BKPT	HALTED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	EXTERNAL	Indicates an asynchronous debug event generated because of EDBGRQ being asserted: 0 no EDBGRQ debug event. 1 EDBGRQ debug event. Default Value: 0
3	VCATCH	Indicates whether a vector catch debug event was generated: 0 no vector catch debug event generated. 1 vector catch debug event generated. The corresponding FSR shows the primary cause of the exception. Default Value: 0
2	DWTTRAP	Indicates a debug event generated by the DWT: 0 no debug events generated by the DWT. 1 at least one debug event generated by the DWT. Default Value: 0

1	BKPT	Indicates a debug event generated by BKPT instruction execution or a breakpoint match in the BPU: 0 no breakpoint debug event. 1 at least one breakpoint debug event. Default Value: 0
0	HALTED	Indicates a debug event generated by a C_HALT or C_STEP request, triggered by a write to the DHCSR: 0 no active halt request debug event. 1 halt request debug event active. See Debug Halting Control and Status Register, DHCSR for more information. Default Value: 0

CM4_SCS_DFSR

Debug Fault Status Register
Address: 0xE000ED30
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM4_SCS_MMFAR

MemManage Fault Address Register
Address: 0xE000ED34
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM4_SCS_BFAR

BusFault Address Register
Address: 0xE000ED38
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM4_SCS_AFSR

Auxiliary Fault Status Register
Address: 0xE000ED3C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM4_SCS_CPACR

Coprocessor Access Control Register
Address: 0xE000ED88
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_MPU_TYPE

MPU Type Register
Address: 0xE000ED90
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							R
Name	None [7:1]							SEPARATE

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	DREGION [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	IREGION [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	IREGION	Instruction region. RAZ. ARMv6-M only supports a unified MPU. Default Value: 0
15 : 8	DREGION	Number of regions supported by the MPU. If this field reads-as-zero the processor does not implement an MPU. Default Value: 8
0	SEPARATE	Indicates support for separate instruction and data address maps. RAZ. ARMv6-M only supports a unified MPU. Default Value: 0

CM4_SCS_MPU_TYPE

MPU Type Register
Address: 0xE000ED90
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_MPU_CTRL

MPU Control Register
Address: 0xE000ED94
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					PRIVDEFENA	HFNMIENA	ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	PRIVDEFENA	When the ENABLE bit is set to 1, the meaning of this bit is: 0: Disables the default memory map. Any instruction or data access that does not access a defined region faults. 1: Enables the default memory map as a background region for privileged access. The system address map on Arm TRM page B3-258 describes the default memory map. When the ENABLE bit is set to 0, the processor ignores the PRIVDEFENA bit. Default Value: 0
1	HFNMIENA	The meaning of this bit is: 0: disables the MPU for HardFaults and NMIs. 1: when the ENABLE bit is set to 1, enables the MPU for HardFaults and NMIs. Note: If HFNMIENA is set to 1 when ENABLE is set to 0, behavior is UNPREDICTABLE. Default Value: 0

0	ENABLE	Enables the MPU: 0: The MPU is disabled. Privileged and unprivileged accesses use the default memory map. 1: The MPU is enabled. Default Value: 0

CM4_SCS_MPU_CTRL

MPU Control Register
Address: 0xE000ED94
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_MPU_RNR

MPU Region Number Register
Address: 0xE000ED98
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	REGION_M [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	REGION_M	Indicates the memory region accessed by MPU_RBAR and MPU_RSAR. Normally, software must write the required region number to MPU_RNR to select the required memory region, before accessing MPU_RBAR or MPU_RSAR. However, the MPU_RBAR.VALID bit provides an alternative way of writing to MPU_RBAR to update a region base address without first writing the region number to MPU_RNR, see MPU Region Base Address Register, MPU_RBAR. Default Value: X

CM4_SCS_MPU_RNR

MPU Region Number Register
Address: 0xE000ED98
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_MPU_RBAR

MPU Region Base Address Register
Address: 0xE000ED9C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW			
HW Access	None			R	R			
Name	None [7:5]			VALID	REGION [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 8	ADDR	Base address of the region. Default Value: X
4	VALID	On writes to the register, indicates whether the write must update the base address of the region identified by the REGION field. updating the MPU_RNR to indicate this new region: 0 Update the base address of the region indicated by MPU_RNR, ignoring the value of the REGION field. 1 Update the least-significant four bits of the MPU_RNR.REGION field with MPU_RBAR.REGION field value, writing 0b0000 to bits [7:4] of the MPU_RBAR.REGION field, and updating the base address of that region. This bit reads as zero Default Value: X
3 : 0	REGION	On writes, can specify the number of the region to update, see VALID field description. On reads, returns bits [3:0] of MPU_RNR. Default Value: X

CM4_SCS_MPU_RBAR

MPU Region Base Address Register
Address: 0xE000ED9C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_MPU_RASR

MPU Region Attribute and Size Register
Address: 0xE000EDA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					RW
HW Access	None		R					R
Name	None [7:6]		SIZE [5:1]					ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SRD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ATTRS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ATTRS [31:24]							

Bits	Name	Description
31 : 16	ATTRS	The MPU Region Attribute field, This field has the following subfields, defined in Region attribute control on Arm TRM page B3-300 of the ARMv6M Architecture manual (September 2010 version): XN MPU_RASR[28] AP[2:0] MPU_RASR[26:24] TEX[2:0] MPU_RASR[21:19] S MPU_RASR[18] C MPU_RASR[17] B MPU_RASR[16] Default Value: X
15 : 8	SRD	Subregion Disable. For regions of 256 bytes or larger, each bit of this field controls whether one of the eight equal subregions is enabled. 0: subregion enabled. 1: subregion disabled. Default Value: X

5 : 1	SIZE	Indicates the region size. The permitted values for SIZE are 7-31, that is 0b00111-0b11111. The associated region size, in bytes, is 2^(SIZE+1). SIZE field values less than 7 are reserved, because the smallest supported region size is 256 bytes. Default Value: X
0	ENABLE	Enables this region: 0: when the MPU is enabled, this region is disabled. 1: When the MPU is enabled, this region is enabled. Enabling a region has no effect unless the MPU_CTRL.ENABLE bit is set to 1, to enable the MPU. Default Value: X

CM4_SCS_MPU_RASR

MPU Region Attribute and Size Register
Address: 0xE000EDA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM4_SCS_MPU_RBAR_A1

MPU alias registers
Address: 0xE000EDA4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_DHCSR

Debug Halting Control and Status Register
Address: 0xE000EDF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				C_MASKINTS	C_STEP	C_HALT	C_DEBUGEN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W				R	R	R	R
HW Access	R				RW	RW	RW	RW
Name	DBG_KEY_P1 [23:20]				S_LOCKUP	S_SLEEP	S_HALT	S_REGRDY

Bits	31	30	29	28	27	26	25	24
SW Access	W						R	R
HW Access	R						RW	RW
Name	DBG_KEY_P2 [31:26]						S_RESET_ST	S_RETIRE_ST

Bits	Name	Description
31 : 26	DBG_KEY_P2	See description for Bit 20 Default Value: X
25	S_RESET_ST	Indicates whether the processor has been reset since the last read of DHCSR. This is a sticky bit, that clears to 0 on a read of DHCSR Default Value: 1

24	S_RETIRE_ST	When not in Debug state, indicates whether the processor has completed execution of at least one instruction since the last read of DHCSR. This is a sticky bit, that clears to 0 on a read of DHCSR. This bit is UNKNOWN: - after a Local reset, but is set to 1 as soon as the processor completes execution of an instruction - when S_LOCKUP is set to 1 - when S_HALT is set to 1. When the processor is not in Debug state, a debugger can check this bit to determine if the processor is stalled on a load, store or fetch access. Default Value: X
23 : 20	DBG_KEY_P1	Debug key: Software must write 0xA05F to [31:16] to enable write accesses to bits [15:0], otherwise the processor ignores the write access. Default Value: X
19	S_LOCKUP	Indicates whether the processor is locked up because of an unrecoverable exception. See Unrecoverable exception cases on Arm TRM page B1-238 for more information. This bit can only read as 1 when accessed by a remote debugger using the DAP. The bit clears to 0 when the processor enters Debug state. Default Value: 0
18	S_SLEEP	Indicates whether the processor is sleeping. The debugger must set the DHCSR.C_HALT bit to 1 to gain control, or wait for an interrupt or other wakeup event to wakeup the system. Default Value: 0
17	S_HALT	Indicates whether the processor is in Debug state. Default Value: 0
16	S_REGRDY	A handshake flag for transfers through the DCRDR: - Writing to DCRSR clears the bit to 0. - Completion of the DCRDR transfer then sets the bit to 1. For more information about DCRDR transfers see Debug Core Register Data Register, DCRDR on Arm TRM page C1-337. 0: There has been a write to the DCRDR, but the transfer is not complete. 1: The transfer to or from the DCRDR is complete. This bit is only valid when the processor is in Debug state, otherwise the bit is UNKNOWN. Default Value: X

3	C_MASKINTS	When debug is enabled, the debugger can write to this bit to mask PendSV, SysTick and external configurable interrupts. The effect of any attempt to change the value of this bit is UNPREDICTABLE unless both: - before the write to DHCSR, the value of the C_HALT bit is 1 - the write to the DHCSR that changes the C_MASKINTS bit also writes 1 to the C_HALT bit This means that a single write to DHCSR cannot set the C_HALT to 0 and change the value of the C_MASKINTS bit. The bit does not affect NMI. When DHCSR.C_DEBUGEN is set to 0, the value of this bit is UNKNOWN. For more information about the use of this bit see Table C1-7 on Arm TRM page C1-326. Default Value: X
2	C_STEP	Processor step bit. The effects of writes to this bit are: 0 Single-stepping disabled. 1 Single-stepping enabled. For more information about the use of this bit see Table C1-7 on Arm TRM page C1-326. Default Value: X
1	C_HALT	Processor halt bit. The effects of writes to this bit are: 0 Request a halted processor to run. 1 Request a running processor to halt. Table C1-7 on Arm TRM page C1-326 shows the effect of writes to this bit when the processor is in Debug state. Default Value: X
0	C_DEBUGEN	Halting debug enable bit. If a debugger writes to DHCSR to change the value of this bit from 0 to 1, it must also write 0 to the C_MASKINTS bit, otherwise behavior is UNPREDICTABLE. This bit can only be written from the DAP. Access to the DHCSR from software running on the processor is IMPLEMENTATION DEFINED. However, writes to this bit from software running on the processor are ignored. Default Value: 0

CM4_SCS_DHCSR

Debug Halting Control and Status Register
Address: 0xE000EDF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_DCRSR

Debug Core Register Selector Register
Address: 0xE000EDF4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			REGSEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							REGWNR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	REGWNR	Specifies the type of access for the transfer. Default Value: X
		0x0: READ : Read transfer
		0x1: WRITE : Write transfer
4 : 0	REGSEL	Specifies the ARM core register or special-purpose register to transfer. Default Value: X
		0x0: R0 : CPU R0
		0x1: R1 : CPU R1
		0x2: R2 : CPU R2
		0x3: R3 : CPU R3
		0x4: R4 : CPU R4
		0x5: R5 : CPU R5
		0x6: R6 : CPU R6
		0x7: R7 : CPU R7
		0x8: R8 : CPU R8
		0x9: R9 : CPU R9
		0xa: R10 : CPU R10

		0xb: R11 : CPU R11
		0xc: R12 : CPU R12
		0xd: SP : Current Stack Pointer
		0xe: LR : CPU LR
		0xf: DBG_RA : DebugReturnAddress: the address of the first instruction to be executed on exit from Debug state.
		0x10: XPSR : xPSR
		0x11: MSP : Main stack pointer, MSP.
		0x12: PSP : Process stack pointer, PSP
		0x14: C_P : [31:24]: CONTROL [7:0]: PRIMASK.

CM4_SCS_DCRSR

Debug Core Register Selector Register
Address: 0xE000EDF4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_DCRDR

Debug Core Register Data Register
Address: 0xE000EDF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DBGTMP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DBGTMP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DBGTMP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DBGTMP [31:24]							

Bits	Name	Description
31 : 0	DBGTMP	Data temporary cache, for reading and writing CPU registers. This register is UNKNOWN: - on reset - when DHCSR.S_HALT = 0. - when DHCSR.S_REGRDY = 0 during execution of a DCRSR based transaction that updates the register Default Value: X

CM4_SCS_DCRDR

Debug Core Register Data Register
Address: 0xE000EDF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_DEMCR

Debug Exception and Monitor Control Register
Address: 0xE000EDFC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							VC_CORERESET

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	None	
HW Access	None					R	None	
Name	None [15:11]					VC_HARDERR	None [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							DWTENA

Bits	Name	Description
24	DWTENA	Global enable for all features configured and controlled by the DWT unit. When DWTENA is set to 0 DWT registers return UNKNOWN values on reads. In addition, it is IMPLEMENTATION DEFINED whether the processor ignores writes to the DWT while DWTENA is 0. Default Value: 0
10	VC_HARDERR	Enable halting debug trap on a HardFault exception. If DHCSR.C_DEBUGEN is set to 0, the processor ignores the value of this bit. Default Value: 0
0	VC_CORERESET	Enable Reset Vector Catch. This causes a Local reset to halt a running system. If DHCSR.C_DEBUGEN is set to 0, the processor ignores the value of this bit. Default Value: 0

CM4_SCS_DEMCR

Debug Exception and Monitor Control Register
Address: 0xE000EDFC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM4_SCS_STIR

Software Triggered Interrupt Register
Address: 0xE000EF00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM4_SCS_FPCCR

FP Context Control Register
Address: 0xE000EF34
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0

CM0P_SCS_SCS_PID4

System Control Space ROM Table Peripheral ID #4
Address: 0xE000EFD0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 0x00000004

CM4_SCS_PID4

Peripheral Identification Register 4
Address: 0xE000EFD0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0x00000004

CM4_SCS_PID5

Peripheral Identification Register 5
Address: 0xE000EFD4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0x00000000

CM4_SCS_PID6

Peripheral Identification Register 6
Address: 0xE000EFD8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0x00000000

CM4_SCS_PID7

Peripheral Identification Register 7
Address: 0xE000EFDC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0x00000000

CM0P_SCS_SCS_PID0

System Control Space ROM Table Peripheral ID #0
Address: 0xE000EFE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 0x00000008

CM4_SCS_PID0

Peripheral Identification Register 0
Address: 0xE000EFE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0x0000000C

CM0P_SCS_SCS_PID1

System Control Space ROM Table Peripheral ID #1
Address: 0xE000EFE4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 0x000000B0

CM4_SCS_PID1

Peripheral Identification Register 1
Address: 0xE000EFE4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0x000000B0

CM0P_SCS_SCS_PID2

System Control Space ROM Table Peripheral ID #2
Address: 0xE000EFE8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 0x0000000B

CM4_SCS_PID2

Peripheral Identification Register 2
Address: 0xE000EFE8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0x0000000B

CM0P_SCS_SCS_PID3

System Control Space ROM Table Peripheral ID #3
Address: 0xE000EFEC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

CM4_SCS_PID3

Peripheral Identification Register 3
Address: 0xE000EFEC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None			
HW Access	R				None			
Name	ECOREVNUM [7:4]				None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	ECOREVNUM	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0x0

CM0P_SCS_SCS_CID0

System Control Space ROM Table Component ID #0
Address: 0xE000EFF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 0x0000000D

CM4_SCS_CID0

Component Identification Register 0
Address: 0xE000EFF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0x0000000D

CM0P_SCS_SCS_CID1

System Control Space ROM Table Component ID #1
Address: 0xE000EFF4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 0x000000E0

CM4_SCS_CID1

Component Identification Register 1
Address: 0xE000EFF4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0x000000E0

CM0P_SCS_SCS_CID2

System Control Space ROM Table Component ID #2
Address: 0xE000EFF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 0x00000005

CM4_SCS_CID2

Component Identification Register 2
Address: 0xE000EFF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0x00000005

CM0P_SCS_SCS_CID3

System Control Space ROM Table Component ID #3
Address: 0xE000EFFC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 0x000000B1

CM4_SCS_CID3

Component Identification Register 3
Address: 0xE000EFFC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARMv7M architecture spec and CM4 TRM documents. See links in CM4_SCS.ACTLR register. Default Value: 0x000000B1

CM4_ETM_CR

Main Control Register
Address: 0xE0041000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer the following ARM CM4 ETM TRM for register description: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0440c/index.html Default Value: 0

CM4_ETM_CCR

Main Control Register
Address: 0xE0041004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_TRIGGER

Trigger Event Register
Address: 0xE0041008
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_SR

ETM Status Register
Address: 0xE0041010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_SCR

System Configuration Register
Address: 0xE0041014
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_TEEVR

TraceEnable Event Register
Address: 0xE0041020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_TECR1

TraceEnable Control 1 Register
Address: 0xE0041024
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_FFLR

FIFOFULL Level Register
Address: 0xE0041028
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_CNTRLDVR1

Free-running counter reload value
Address: 0xE0041140
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_SYNCFR

Synchronization Frequency Register
Address: 0xE00411E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_IDR

ID Register
Address: 0xE00411E4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_CCER

Configuration Code Extension Register
Address: 0xE00411E8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_TESSEICR

TraceEnable Start/Stop EmbeddedICE Control Register
Address: 0xE00411F0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_TSEVR

Timestamp Event Register
Address: 0xE00411F8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_TRACEIDR

CoreSight Trace ID Register
Address: 0xE0041200
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_IDR2

ETM ID Register 2
Address: 0xE0041208
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_PDSR

Device Power-Down Status Register
Address: 0xE0041314
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_ITMISCIN

Integration Test Miscellaneous Inputs
Address: 0xE0041EE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_ITTRIGOUT

Integration Test Trigger Out
Address: 0xE0041EE8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_ITATBCTR2

ETM Integration Test ATB Control 2
Address: 0xE0041EF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_ITATBCTR0

ETM Integration Test ATB Control 0
Address: 0xE0041EF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_ITCTRL

Integration Mode Control Register
Address: 0xE0041F00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_CLAIMSET

Claim Tag Set Register
Address: 0xE0041FA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_CLAIMCLR

Claim Tag Clear Register
Address: 0xE0041FA4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_LAR

Lock Access Register
Address: 0xE0041FB0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_LSR

Lock Status Register
Address: 0xE0041FB4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_AUTHSTATUS

Authentication Status Register
Address: 0xE0041FB8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0

CM4_ETM_DEVTYPE

CoreSight Device Type Register
Address: 0xE0041FCC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0x00000013

CM4_ETM_PID4

Peripheral Identification Register 4.
Address: 0xE0041FD0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0x00000004

CM4_ETM_PID5

Peripheral Identification Register 5.
Address: 0xE0041FD4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0x00000000

CM4_ETM_PID6

Peripheral Identification Register 6.
Address: 0xE0041FD8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0x00000000

CM4_ETM_PID7

Peripheral Identification Register 7.
Address: 0xE0041FDC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0x00000000

CM4_ETM_PID0

Peripheral Identification Register 0.
Address: 0xE0041FE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0x00000025

CM4_ETM_PID1

Peripheral Identification Register 1.
Address: 0xE0041FE4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0x000000B9

CM4_ETM_PID2

Peripheral Identification Register 2.
Address: 0xE0041FE8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0x0000000B

CM4_ETM_PID3

Peripheral Identification Register 3.
Address: 0xE0041FEC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None			
HW Access	R				None			
Name	ECOREVNUM [7:4]				None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	ECOREVNUM	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0x0

CM4_ETM_CID0

Component Identification Register 0.
Address: 0xE0041FF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0x0000000D

CM4_ETM_CID1

Component Identification Register 1.
Address: 0xE0041FF4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0x00000090

CM4_ETM_CID2

Component Identification Register 2.
Address: 0xE0041FF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0x00000005

CM4_ETM_CID3

Component Identification Register 3.
Address: 0xE0041FFC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer ARM documentation. See links in CM4_ETM.CR register. Default Value: 0x000000B1

CM4_CM4CTI_CTICONTROL

CTI Control Register
Address: 0xE0042000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							GLBEN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	GLBEN	Enables or disables the ECT: 0 = disabled (reset) 1 = enabled. When disabled, all cross triggering mapping logic functionality is disabled for this processor. Default Value: 0

CM4_CM4CTI_CTIINTACK

CTI Interrupt Acknowledge Register
Address: 0xE0042010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	INTACK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	INTACK	Acknowledges the corresponding CTITRIGOUT output: 1 = CTITRIGOUT is acknowledged and is cleared when MAPTRIGOUT is LOW. 0 = no effect. There is one bit of the register for each CTITRIGOUT output. Default Value: 0

CM4_CM4CTI_CTIAPPSET

CTI Application Trigger Set Register
Address: 0xE0042014
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				APPSET [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	APPSET	Setting a bit HIGH generates a channel event for the selected channel. Read: 0 = application trigger inactive (reset) 1 = application trigger active. Write: 0 = no effect 1 = generate channel event. There is one bit of the register for each channel. Default Value: 0

CM4_CM4CTI_CTIAPPCLEAR

CTI Application Trigger Clear Register
Address: 0xE0042018
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				W			
HW Access	None				R			
Name	None [7:4]				APPCLEAR [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	APPCLEAR	Clears corresponding bits in the CTIAPPSET register. 1 = application trigger disabled in the CTIAPPSET register 0 = no effect. There is one bit of the register for each channel. Default Value: 0

CM4_CM4CTI_CTIAPPPULSE

CTI Application Pulse Register
Address: 0xE004201C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				W			
HW Access	None				R			
Name	None [7:4]				APPULSE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	APPULSE	Setting a bit HIGH generates a channel event pulse for the selected channel. Write: 1 = channel event pulse generated for one CTICLK period 0 = no effect. There is one bit of the register for each channel. Default Value: 0

CM4_CM4CTI_CTIINEN0

CTI Trigger to Channel Enable Registers
Address: 0xE0042020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGINEN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TRIGINEN	Enables a cross trigger event to the corresponding channel when an CTITRIGIN is activated. 1 = enables the CTITRIGIN signal to generate an event on the respective channel of the CTM. There is one bit of the register for each of the four channels. For example in register CTIINEN0, TRIGINEN[0] set to 1 enables CTITRIGIN onto channel 0. 0 = disables the CTITRIGIN signal from generating an event on the respective channel of the CTM. Default Value: 0

CM4_CM4CTI_CTIOUTEN0

CTI Channel to Trigger Enable Registers
Address: 0xE00420A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGOUTEN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TRIGOUTEN	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate an CTITRIGOUT output: 0 = the channel input (CTICHIN) from the CTM is not routed to the CTITRIGOUT output 1 = the channel input (CTICHIN) from the CTM is routed to the CTITRIGOUT output. There is one bit for each of the four channels. For example in register CTIOUTEN0, enabling bit 0 enables CTICHIN[0] to cause a trigger event on the CTITRIGOUT[0] output. Default Value: 0

CM4_CM4CTI_CTITRIGINSTATUS

CTI Trigger In Status Register
Address: 0xE0042130
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TRIGINSTATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	TRIGINSTATUS	Shows the status of the CTITRIGIN inputs: 1 = CTITRIGIN is active 0 = CTITRIGIN is inactive. Because the register provides a view of the raw CTITRIGIN inputs, the reset value is unknown. There is one bit of the register for each trigger input. Default Value: 0

CM4_CM4CTI_CTITRIGOUTSTATUS

CTI Trigger Out Status Register
Address: 0xE0042134
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TRIGOUTSTATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	TRIGOUTSTATUS	Shows the status of the CTITRIGOUT outputs. 1 = CTITRIGOUT is active 0 = CTITRIGOUT is inactive (reset). There is one bit of the register for each trigger output. Default Value: 0

CM4_CM4CTI_CTICHINSTATUS

CTI Channel In Status Register
Address: 0xE0042138
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				RW			
Name	None [7:4]				CTICHINSTATUS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	CTICHINSTATUS	Shows the status of the CTICHIN inputs: 1 = CTICHIN is active 0 = CTICHIN is inactive. Because the register provides a view of the raw CTICHIN inputs from the CTM, the reset value is unknown. There is one bit of the register for each channel input. Default Value: 0

CM4_CM4CTI_CTICHOUTSTATUS

CTI Channel Out Status Register
Address: 0xE004213C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				RW			
Name	None [7:4]				CTICHOUTSTATUS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	CTICHOUTSTATUS	Shows the status of the CTICHOUT outputs. 1 = CTICHOUT is active 0 = CTICHOUT is inactive (reset). There is one bit of the register for each channel output. Default Value: 0

CM4_CM4CTI_CTIGATE

Enable CTI Channel Gate Register
Address: 0xE0042140
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				CTIGATEEN3	CTIGATEEN2	CTIGATEEN1	CTIGATEEN0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	CTIGATEEN3	Enable CTICHOUT3. Set to 0 to disable channel propagation. Default Value: 1
2	CTIGATEEN2	Enable CTICHOUT2. Set to 0 to disable channel propagation. Default Value: 1
1	CTIGATEEN1	Enable CTICHOUT1. Set to 0 to disable channel propagation. Default Value: 1
0	CTIGATEEN0	Enable CTICHOUT0. Set to 0 to disable channel propagation. Default Value: 1

CM4_CM4CTI_ASICCTL

External Multiplexor Control Register
Address: 0xE0042144
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ASICCTL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	ASICCTL	Implementation-defined ASIC control, value written to the register is output on ASICCTL[7:0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM. See ECT CoreSight defined registers on Arm TRM page 4-28. Default Value: 0

CM4_CM4CTI_ITCHINACK

ITCHINACK Register
Address: 0xE0042EDC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				W			
HW Access	None				R			
Name	None [7:4]				CTCHINACK [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	CTCHINACK	Set the value of the CTCHINACK outputs Default Value: 0

CM4_CM4CTI_ITTRIGINACK

ITTRIGINACK Register
Address: 0xE0042EE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	CTTRIGINACK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CTTRIGINACK	Set the value of the CTTRIGINACK outputs Default Value: 0

CM4_CM4CTI_ITCHOUT

ITCHOUT Register
Address: 0xE0042EE4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				W			
HW Access	None				R			
Name	None [7:4]				CTCHOUT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	CTCHOUT	Set the value of the CTCHOUT outputs Default Value: 0

CM4_CM4CTI_ITTRIGOUT

ITTRIGOUT Register
Address: 0xE0042EE8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	CTTRIGOUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CTTRIGOUT	Set the value of the CTTRIGOUT outputs Default Value: 0

CM4_CM4CTI_ITCHOUTACK

ITCHOUTACK Register
Address: 0xE0042EEC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				CTCHOUTACK [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	CTCHOUTACK	Read the values of the CTCHOUTACK inputs Default Value: 0

CM4_CM4CTI_ITTRIGOUTACK

ITTRIGOUTACK Register
Address: 0xE0042EF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CTTRIGOUTACK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CTTRIGOUTACK	Read the values of the CTTRIGOUTACK inputs Default Value: 0

CM4_CM4CTI_ITCHIN

ITCHIN Register
Address: 0xE0042EF4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				CTCHIN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	CTCHIN	Read the values of the CTCHIN inputs Default Value: 0

CM4_CM4CTI_ITTRIGIN

ITTRIGIN Register
Address: 0xE0042EF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CTTRIGIN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CTTRIGIN	Read the values of the CTTRIGIN inputs Default Value: 0

CM4_CM4CTI_ITCTRL

Integration Mode Control Register
Address: 0xE0042F00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							MODE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	MODE	When set, the component enters integration mode, enabling topology detection or integration testing to be performed. At reset the component must enter functional mode. If no integration functionality is implemented, this register must read as zero. Default Value: 0

CM4_CM4CTI_CLAIMSET

Claim Tag Set Register
Address: 0xE0042FA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S			
HW Access	None				R			
Name	None [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TAG	A bit programmable register bank which sets the Claim Tag Value. A read will return a logic 1 for all implemented locations. Default Value: 0xF

CM4_CM4CTI_CLAIMCLR

Claim Tag Clear Register
Address: 0xE0042FA4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C			
HW Access	None				R			
Name	None [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TAG	A bit programmable register bank that is zero at reset. Default Value: 0

CM4_CM4CTI_LOCKACCESS

Lock Access Register
Address: 0xE0042FB0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				ACCESS_CODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	ACCESS_CODE	Write Access Code. A write of 0xC5ACCE55 enables further write access to this device. An invalid write will have the affect of removing write access. If LOCKSTATUS[2] is set, then only bits [7:0] of this register are implemented and lock access is obtained by consecutively writing 0xC5, 0xAC, 0xCE, 0x55. Bits [31:8] are unused and any writes to them ignored. Default Value: 0

CM4_CM4CTI_LOCKSTATUS

Lock Status Register
Address: 0xE0042FB4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					IMPLEMENTS_8B	ACCESS_PERMITTED	EXISTS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	IMPLEMENTS_8B	This component implements an 8-bit Lock Access Register. Default Value: 0
1	ACCESS_PERMITTED	The values of this bit mean: 0 = Access permitted. 1 = Write access to the component is blocked. All writes to control registers are ignored. Reads are permitted Default Value: 0
0	EXISTS	Indicates that a lock control mechanism exists for this device Default Value: 0

CM4_CM4CTI_AUTHSTATUS

Authentication Status Register
Address: 0xE0042FB8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R		R		R	
HW Access	W		W		W		W	
Name	SNIDBG [7:6]		SIDBG [5:4]		NSNIDBG [3:2]		NSIDBG [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SNIDBG	Secure Non-Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0
5 : 4	SIDBG	Secure Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0
3 : 2	NSNIDBG	Non-Secure Non-Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 1

1 : 0	NSIDBG	Non-Secure Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 1

CM4_CM4CTI_DEVID

Device Configuration Register
Address: 0xE0042FC8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			R				
Name	None [7:5]			NRMUXING [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	NRTRIG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				R			
Name	None [23:20]				NRCHAN [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	NRCHAN	Number of ECT channels available. Default Value: 4
15 : 8	NRTRIG	Number of ECT triggers available. Default Value: 8
4 : 0	NRMUXING	Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using ASICCTL. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog `define EXTMUXNUM that you must alter accordingly. Default Value: 0

CM4_CM4CTI_DEVTYPE

Device Type Identifier Register
Address: 0xE0042FCC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	SUB_TYPE [7:4]				CLASS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	SUB_TYPE	cross trigger Default Value: 0x1
3 : 0	CLASS	debug control logic component Default Value: 0x4

CM4_CM4CTI_PID4

Peripheral Identification Register 4
Address: 0xE0042FD0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000004

CM4_CM4CTI_PID5

Peripheral Identification Register 5
Address: 0xE0042FD4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

CM4_CM4CTI_PID6

Peripheral Identification Register 6
Address: 0xE0042FD8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

CM4_CM4CTI_PID7

Peripheral Identification Register 7
Address: 0xE0042FDC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

CM4_CM4CTI_PID0

Peripheral Identification Register 0
Address: 0xE0042FE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000006

CM4_CM4CTI_PID1

Peripheral Identification Register 1
Address: 0xE0042FE4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x000000B9

CM4_CM4CTI_PID2

Peripheral Identification Register 2
Address: 0xE0042FE8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x0000004B

CM4_CM4CTI_PID3

Peripheral Identification Register 3
Address: 0xE0042FEC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None			
HW Access	R				None			
Name	ECOREVNUM [7:4]				None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	ECOREVNUM	ECO revision for MTB Default Value: 0x0

CM4_CM4CTI_CID0

Component Identification Register 0
Address: 0xE0042FF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x0000000D

CM4_CM4CTI_CID1

Component Identification Register 1
Address: 0xE0042FF4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000090

CM4_CM4CTI_CID2

Component Identification Register 2
Address: 0xE0042FF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000005

CM4_CM4CTI_CID3

Component Identification Register 3
Address: 0xE0042FFC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x000000B1

CM4_ROM_SCS

CM4 CoreSight ROM Table Peripheral #0
Address: 0xE007F000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to SCS ROM Table Default Value: 0xFFF8F003

CM4_ROM_DWT

CM4 CoreSight ROM Table Peripheral #1
Address: 0xE007F004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to DWT ROM Table Default Value: 0xFFF82003

CM4_ROM_FPB

CM4 CoreSight ROM Table Peripheral #2
Address: 0xE007F008
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to FPB ROM Table Default Value: 0xFFF83003

CM4_ROM_ITM

CM4 CoreSight ROM Table Peripheral #3
Address: 0xE007F00C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to ITM ROM Table Default Value: 0xFFF81003

CM4_ROM_CTI

CM4 CoreSight ROM Table Peripheral #4
Address: 0xE007F010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to CTI ROM Table Default Value: 0xFFFC3003

CM4_ROM_ETM

CM4 CoreSight ROM Table Peripheral #5
Address: 0xE007F014
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to ETM ROM Table Default Value: 0xFFFC2003

CM4_ROM_CSMT

CM4 CoreSight ROM Table Memory Type
Address: 0xE007FFCC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Memory Type Default Value: 1

CM4_ROM_PID4

CM4 CoreSight ROM Table Peripheral ID #4
Address: 0xE007FFD0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 0x00000004

CM4_ROM_PID0

CM4 CoreSight ROM Table Peripheral ID #0
Address: 0xE007FFE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 0x000000C0

CM4_ROM_PID1

CM4 CoreSight ROM Table Peripheral ID #1
Address: 0xE007FFE4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 0x000000B4

CM4_ROM_PID2

CM4 CoreSight ROM Table Peripheral ID #2
Address: 0xE007FFE8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 0x0000000B

CM4_ROM_PID3

CM4 CoreSight ROM Table Peripheral ID #3
Address: 0xE007FFEC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

CM4_ROM_CID0

CM4 CoreSight ROM Table Component ID #0
Address: 0xE007FFF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 0x0000000D

CM4_ROM_CID1

CM4 CoreSight ROM Table Component ID #1
Address: 0xE007FFF4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 0x00000010

CM4_ROM_CID2

CM4 CoreSight ROM Table Component ID #2
Address: 0xE007FFF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 0x00000005

CM4_ROM_CID3

CM4 CoreSight ROM Table Component ID #3
Address: 0xE007FFFC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 0x000000B1

CM4_TRCCTI_CTICONTROL

CTI Control Register
Address: 0xE0080000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							GLBEN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	GLBEN	Enables or disables the ECT: 0 = disabled (reset) 1 = enabled. When disabled, all cross triggering mapping logic functionality is disabled for this processor. Default Value: 0

CM4_TRCCTI_CTIINTACK

CTI Interrupt Acknowledge Register
Address: 0xE0080010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	INTACK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	INTACK	Acknowledges the corresponding CTITRIGOUT output: 1 = CTITRIGOUT is acknowledged and is cleared when MAPTRIGOUT is LOW. 0 = no effect. There is one bit of the register for each CTITRIGOUT output. Default Value: 0

CM4_TRCCTI_CTIAPPSET

CTI Application Trigger Set Register
Address: 0xE0080014
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				APPSET [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	APPSET	Setting a bit HIGH generates a channel event for the selected channel. Read: 0 = application trigger inactive (reset) 1 = application trigger active. Write: 0 = no effect 1 = generate channel event. There is one bit of the register for each channel. Default Value: 0

CM4_TRCCTI_CTIAPPCLEAR

CTI Application Trigger Clear Register
Address: 0xE0080018
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				W			
HW Access	None				R			
Name	None [7:4]				APPCLEAR [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	APPCLEAR	Clears corresponding bits in the CTIAPPSET register. 1 = application trigger disabled in the CTIAPPSET register 0 = no effect. There is one bit of the register for each channel. Default Value: 0

CM4_TRCCTI_CTIAPPPULSE

CTI Application Pulse Register
Address: 0xE008001C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				W			
HW Access	None				R			
Name	None [7:4]				APPULSE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	APPULSE	Setting a bit HIGH generates a channel event pulse for the selected channel. Write: 1 = channel event pulse generated for one CTICLK period 0 = no effect. There is one bit of the register for each channel. Default Value: 0

CM4_TRCCTI_CTIINEN0

CTI Trigger to Channel Enable Registers
Address: 0xE0080020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGINEN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TRIGINEN	Enables a cross trigger event to the corresponding channel when an CTITRIGIN is activated. 1 = enables the CTITRIGIN signal to generate an event on the respective channel of the CTM. There is one bit of the register for each of the four channels. For example in register CTIINEN0, TRIGINEN[0] set to 1 enables CTITRIGIN onto channel 0. 0 = disables the CTITRIGIN signal from generating an event on the respective channel of the CTM. Default Value: 0

CM4_TRCCTI_CTIOUTEN0

CTI Channel to Trigger Enable Registers
Address: 0xE00800A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGOUTEN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TRIGOUTEN	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate an CTITRIGOUT output: 0 = the channel input (CTICHIN) from the CTM is not routed to the CTITRIGOUT output 1 = the channel input (CTICHIN) from the CTM is routed to the CTITRIGOUT output. There is one bit for each of the four channels. For example in register CTIOUTEN0, enabling bit 0 enables CTICHIN[0] to cause a trigger event on the CTITRIGOUT[0] output. Default Value: 0

CM4_TRCCTI_CTITRIGINSTATUS

CTI Trigger In Status Register
Address: 0xE0080130
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TRIGINSTATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	TRIGINSTATUS	Shows the status of the CTITRIGIN inputs: 1 = CTITRIGIN is active 0 = CTITRIGIN is inactive. Because the register provides a view of the raw CTITRIGIN inputs, the reset value is unknown. There is one bit of the register for each trigger input. Default Value: 0

CM4_TRCCTI_CTITRIGOUTSTATUS

CTI Trigger Out Status Register
Address: 0xE0080134
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TRIGOUTSTATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	TRIGOUTSTATUS	Shows the status of the CTITRIGOUT outputs. 1 = CTITRIGOUT is active 0 = CTITRIGOUT is inactive (reset). There is one bit of the register for each trigger output. Default Value: 0

CM4_TRCCTI_CTICHINSTATUS

CTI Channel In Status Register
Address: 0xE0080138
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				RW			
Name	None [7:4]				CTICHINSTATUS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	CTICHINSTATUS	Shows the status of the CTICHIN inputs: 1 = CTICHIN is active 0 = CTICHIN is inactive. Because the register provides a view of the raw CTICHIN inputs from the CTM, the reset value is unknown. There is one bit of the register for each channel input. Default Value: 0

CM4_TRCCTI_CTICHOUTSTATUS

CTI Channel Out Status Register
Address: 0xE008013C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				RW			
Name	None [7:4]				CTICHOUTSTATUS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	CTICHOUTSTATUS	Shows the status of the CTICHOUT outputs. 1 = CTICHOUT is active 0 = CTICHOUT is inactive (reset). There is one bit of the register for each channel output. Default Value: 0

CM4_TRCCTI_CTIGATE

Enable CTI Channel Gate Register
Address: 0xE0080140
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				CTIGATEEN3	CTIGATEEN2	CTIGATEEN1	CTIGATEEN0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	CTIGATEEN3	Enable CTICHOUT3. Set to 0 to disable channel propagation. Default Value: 1
2	CTIGATEEN2	Enable CTICHOUT2. Set to 0 to disable channel propagation. Default Value: 1
1	CTIGATEEN1	Enable CTICHOUT1. Set to 0 to disable channel propagation. Default Value: 1
0	CTIGATEEN0	Enable CTICHOUT0. Set to 0 to disable channel propagation. Default Value: 1

CM4_TRCCTI_ASICCTL

External Multiplexor Control Register
Address: 0xE0080144
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ASICCTL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	ASICCTL	Implementation-defined ASIC control, value written to the register is output on ASICCTL[7:0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM. See ECT CoreSight defined registers on Arm TRM page 4-28. Default Value: 0

CM4_TRCCTI_ITCHINACK

ITCHINACK Register
Address: 0xE0080EDC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				W			
HW Access	None				R			
Name	None [7:4]				CTCHINACK [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	CTCHINACK	Set the value of the CTCHINACK outputs Default Value: 0

CM4_TRCCTI_ITTRIGINACK

ITTRIGINACK Register
Address: 0xE0080EE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	CTTRIGINACK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CTTRIGINACK	Set the value of the CTTRIGINACK outputs Default Value: 0

CM4_TRCCTI_ITCHOUT

ITCHOUT Register
Address: 0xE0080EE4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				W			
HW Access	None				R			
Name	None [7:4]				CTCHOUT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	CTCHOUT	Set the value of the CTCHOUT outputs Default Value: 0

CM4_TRCCTI_ITTRIGOUT

ITTRIGOUT Register
Address: 0xE0080EE8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	CTTRIGOUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CTTRIGOUT	Set the value of the CTTRIGOUT outputs Default Value: 0

CM4_TRCCTI_ITCHOUTACK

ITCHOUTACK Register
Address: 0xE0080EEC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				CTCHOUTACK [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	CTCHOUTACK	Read the values of the CTCHOUTACK inputs Default Value: 0

CM4_TRCCTI_ITTRIGOUTACK

ITTRIGOUTACK Register
Address: 0xE0080EF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CTTRIGOUTACK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CTTRIGOUTACK	Read the values of the CTTRIGOUTACK inputs Default Value: 0

CM4_TRCCTI_ITCHIN

ITCHIN Register
Address: 0xE0080EF4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				CTCHIN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	CTCHIN	Read the values of the CTCHIN inputs Default Value: 0

CM4_TRCCTI_ITTRIGIN

ITTRIGIN Register
Address: 0xE0080EF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CTTRIGIN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CTTRIGIN	Read the values of the CTTRIGIN inputs Default Value: 0

CM4_TRCCTI_ITCTRL

Integration Mode Control Register
Address: 0xE0080F00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							MODE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	MODE	When set, the component enters integration mode, enabling topology detection or integration testing to be performed. At reset the component must enter functional mode. If no integration functionality is implemented, this register must read as zero. Default Value: 0

CM4_TRCCTI_CLAIMSET

Claim Tag Set Register
Address: 0xE0080FA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S			
HW Access	None				R			
Name	None [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TAG	A bit programmable register bank which sets the Claim Tag Value. A read will return a logic 1 for all implemented locations. Default Value: 0xF

CM4_TRCCTI_CLAIMCLR

Claim Tag Clear Register
Address: 0xE0080FA4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C			
HW Access	None				R			
Name	None [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TAG	A bit programmable register bank that is zero at reset. Default Value: 0

CM4_TRCCTI_LOCKACCESS

Lock Access Register
Address: 0xE0080FB0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				ACCESS_CODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	ACCESS_CODE	Write Access Code. A write of 0xC5ACCE55 enables further write access to this device. An invalid write will have the affect of removing write access. If LOCKSTATUS[2] is set, then only bits [7:0] of this register are implemented and lock access is obtained by consecutively writing 0xC5, 0xAC, 0xCE, 0x55. Bits [31:8] are unused and any writes to them ignored. Default Value: 0

CM4_TRCCTI_LOCKSTATUS

Lock Status Register
Address: 0xE0080FB4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					IMPLEMENTS_8B	ACCESS_PERMITTED	EXISTS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	IMPLEMENTS_8B	This component implements an 8-bit Lock Access Register. Default Value: 0
1	ACCESS_PERMITTED	The values of this bit mean: 0 = Access permitted. 1 = Write access to the component is blocked. All writes to control registers are ignored. Reads are permitted Default Value: 0
0	EXISTS	Indicates that a lock control mechanism exists for this device Default Value: 0

CM4_TRCCTI_AUTHSTATUS

Authentication Status Register
Address: 0xE0080FB8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R		R		R	
HW Access	W		W		W		W	
Name	SNIDBG [7:6]		SIDBG [5:4]		NSNIDBG [3:2]		NSIDBG [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SNIDBG	Secure Non-Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0
5 : 4	SIDBG	Secure Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0
3 : 2	NSNIDBG	Non-Secure Non-Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 1

1 : 0	NSIDBG	Non-Secure Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 1

CM4_TRCCTI_DEVID

Device Configuration Register
Address: 0xE0080FC8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			R				
Name	None [7:5]			NRMUXING [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	NRTRIG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				R			
Name	None [23:20]				NRCHAN [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	NRCHAN	Number of ECT channels available. Default Value: 4
15 : 8	NRTRIG	Number of ECT triggers available. Default Value: 8
4 : 0	NRMUXING	Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using ASICCTL. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog `define EXTMUXNUM that you must alter accordingly. Default Value: 0

CM4_TRCCTI_DEVTYPE

Device Type Identifier Register
Address: 0xE0080FCC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	SUB_TYPE [7:4]				CLASS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	SUB_TYPE	cross trigger Default Value: 0x1
3 : 0	CLASS	debug control logic component Default Value: 0x4

CM4_TRCCTI_PID4

Peripheral Identification Register 4
Address: 0xE0080FD0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000004

CM4_TRCCTI_PID5

Peripheral Identification Register 5
Address: 0xE0080FD4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

CM4_TRCCTI_PID6

Peripheral Identification Register 6
Address: 0xE0080FD8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

CM4_TRCCTI_PID7

Peripheral Identification Register 7
Address: 0xE0080FDC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

CM4_TRCCTI_PID0

Peripheral Identification Register 0
Address: 0xE0080FE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000006

CM4_TRCCTI_PID1

Peripheral Identification Register 1
Address: 0xE0080FE4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x000000B9

CM4_TRCCTI_PID2

Peripheral Identification Register 2
Address: 0xE0080FE8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x0000004B

CM4_TRCCTI_PID3

Peripheral Identification Register 3
Address: 0xE0080FEC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None			
HW Access	R				None			
Name	ECOREVNUM [7:4]				None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	ECOREVNUM	ECO revision for MTB Default Value: 0x0

CM4_TRCCTI_CID0

Component Identification Register 0
Address: 0xE0080FF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x0000000D

CM4_TRCCTI_CID1

Component Identification Register 1
Address: 0xE0080FF4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000090

CM4_TRCCTI_CID2

Component Identification Register 2
Address: 0xE0080FF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000005

CM4_TRCCTI_CID3

Component Identification Register 3
Address: 0xE0080FFC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x000000B1

CM4_CSTF_CSTFCTL

Funnel Control Register
Address: 0xE008C000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.100536_0302_01_en/index.html Default Value: 0

CM4_CSTF_CSTFPCTL

Priority Control Register
Address: 0xE008C004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0

CM4_CSTF_ITATBDATA0

Integration Register
Address: 0xE008CEEC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0

CM4_CSTF_ITCTRL

Integration Mode Control Register
Address: 0xE008CF00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0

CM4_CSTF_CLAIMSET

Claim Tag Set Register
Address: 0xE008CFA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0

CM4_CSTF_CLAIMCLR

Claim Tag Clear Register
Address: 0xE008CFA4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0

CM4_CSTF_LOCKACCESS

Lock Access Register
Address: 0xE008CFB0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0

CM4_CSTF_LOCKSTATUS

Lock Status Register
Address: 0xE008CFB4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x00000003

CM4_CSTF_AUTHSTATUS

Authentication Status Register
Address: 0xE008CFB8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0

CM4_CSTF_DEVID

Device ID
Address: 0xE008CFC8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x00000038

CM4_CSTF_DEVTYPE

Device Type Identifier Register
Address: 0xE008CFCC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x00000012

CM4_CSTF_PID4

Peripheral Identification Register 4
Address: 0xE008CFD0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x00000004

CM4_CSTF_PID5

Peripheral Identification Register 5
Address: 0xE008CFD4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x00000000

CM4_CSTF_PID6

Peripheral Identification Register 6
Address: 0xE008CFD8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x00000000

CM4_CSTF_PID7

Peripheral Identification Register 7
Address: 0xE008CFDC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x00000000

CM4_CSTF_PID0

Peripheral Identification Register 0
Address: 0xE008CFE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x00000008

CM4_CSTF_PID1

Peripheral Identification Register 1
Address: 0xE008CFE4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x000000B9

CM4_CSTF_PID2

Peripheral Identification Register 2
Address: 0xE008CFE8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x0000002B

CM4_CSTF_PID3

Peripheral Identification Register 3
Address: 0xE008CFEC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None			
HW Access	R				None			
Name	ECOREVNUM [7:4]				None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	ECOREVNUM	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x0

CM4_CSTF_CID0

Component Identification Register 0
Address: 0xE008CFF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x0000000D

CM4_CSTF_CID1

Component Identification Register 1
Address: 0xE008CFF4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x00000090

CM4_CSTF_CID2

Component Identification Register 2
Address: 0xE008CFF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x00000005

CM4_CSTF_CID3

Component Identification Register 3
Address: 0xE008CFFC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x000000B1

CM4_ETB_ETBRDP

RAM Depth Register
Address: 0xE008D004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0

CM4_ETB_ETBSTS

Status Register
Address: 0xE008D00C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x00000008

CM4_ETB_ETBRRD

RAM Read Data Register
Address: 0xE008D010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0

CM4_ETB_ETBRRP

RAM Read Pointer Register
Address: 0xE008D014
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0

CM4_ETB_ETBRWP

RAM Write Pointer Register
Address: 0xE008D018
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0

CM4_ETB_ETBTRG

Trigger Counter Register
Address: 0xE008D01C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0

CM4_ETB_ETBCTL

Control Register
Address: 0xE008D020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0

CM4_ETB_ETBRWD

RAM Write Data Register
Address: 0xE008D024
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0

CM4_ETB_ETBFFSR

Formatter and Flush Status Register
Address: 0xE008D300
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x00000002

CM4_ETB_ETBFFCR

Formatter and Flush Control Register
Address: 0xE008D304
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0

CM4_ETB_ITMISCOP0

Integration Register
Address: 0xE008DEE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0

CM4_ETB_ITTRFLIN

Integration Register
Address: 0xE008DEE8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0

CM4_ETB_ITCTRL

Integration Mode Control Register
Address: 0xE008DF00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0

CM4_ETB_CLAIMSET

Claim Tag Set Register
Address: 0xE008DFA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S			
HW Access	None				R			
Name	None [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TAG	A bit programmable register bank which sets the Claim Tag Value. A read will return a logic 1 for all implemented locations. Default Value: 0x0000000F

CM4_ETB_CLAIMCLR

Claim Tag Clear Register
Address: 0xE008DFA4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C			
HW Access	None				R			
Name	None [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TAG	A bit programmable register bank that is zero at reset. Default Value: 0

CM4_ETB_LOCKACCESS

Lock Access Register
Address: 0xE008DFB0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				ACCESS_CODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	ACCESS_CODE	Write Access Code. A write of 0xC5ACCE55 enables further write access to this device. An invalid write will have the affect of removing write access. If LOCKSTATUS[2] is set, then only bits [7:0] of this register are implemented and lock access is obtained by consecutively writing 0xC5, 0xAC, 0xCE, 0x55. Bits [31:8] are unused and any writes to them ignored. Default Value: 0

CM4_ETB_LOCKSTATUS

Lock Status Register
Address: 0xE008DFB4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					IMPLEMENTS_8B	ACCESS_PERMITTED	EXISTS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	IMPLEMENTS_8B	This component implements an 8-bit Lock Access Register. Default Value: 0
1	ACCESS_PERMITTED	The values of this bit mean: 0 = Access permitted. 1 = Write access to the component is blocked. All writes to control registers are ignored. Reads are permitted Default Value: 1
0	EXISTS	Indicates that a lock control mechanism exists for this device Default Value: 1

CM4_ETB_AUTHSTATUS

Authentication Status Register
Address: 0xE008DFB8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R		R		R	
HW Access	W		W		W		W	
Name	SNIDBG [7:6]		SIDBG [5:4]		NSNIDBG [3:2]		NSIDBG [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SNIDBG	Secure Non-Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0
5 : 4	SIDBG	Secure Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0
3 : 2	NSNIDBG	Non-Secure Non-Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0

1 : 0	NSIDBG	Non-Secure Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0

CM4_ETB_DEVID

Device ID
Address: 0xE008DFC8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R				
HW Access	None		R	R				
Name	None [7:6]		RAMCLK	EXTMUXNUM [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	RAMCLK	This bit returns 0 on reads to indicate that the ETB RAM operates synchronously to atclk. Default Value: 0
4 : 0	EXTMUXNUM	Number of external multiplexing available. Non-zero values indicate the type of ATB multiplexing on the input to the ATB. Only 0x00 is supported, that is, no multiplexing is present. This value helps detect the ATB structure. Default Value: 0

CM4_ETB_DEVTYPE

Device Type Identifier Register
Address: 0xE008DFCC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	SUB_TYPE [7:4]				CLASS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	SUB_TYPE	Trace buffer. Default Value: 0x2
3 : 0	CLASS	Trace sink component Default Value: 0x1

CM4_ETB_PID4

Peripheral Identification Register 4
Address: 0xE008DFD0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x00000004

CM4_ETB_PID5

Peripheral Identification Register 5
Address: 0xE008DFD4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x00000000

CM4_ETB_PID6

Peripheral Identification Register 6
Address: 0xE008DFD8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x00000000

CM4_ETB_PID7

Peripheral Identification Register 7
Address: 0xE008DFDC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x00000000

CM4_ETB_PID0

Peripheral Identification Register 0
Address: 0xE008DFE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x00000007

CM4_ETB_PID1

Peripheral Identification Register 1
Address: 0xE008DFE4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x000000B9

CM4_ETB_PID2

Peripheral Identification Register 2
Address: 0xE008DFE8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x0000003B

CM4_ETB_PID3

Peripheral Identification Register 3
Address: 0xE008DFEC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None			
HW Access	R				None			
Name	ECOREVNUM [7:4]				None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	ECOREVNUM	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x0

CM4_ETB_CID0

Component Identification Register 0
Address: 0xE008DFF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x0000000D

CM4_ETB_CID1

Component Identification Register 1
Address: 0xE008DFF4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x00000090

CM4_ETB_CID2

Component Identification Register 2
Address: 0xE008DFF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x00000005

CM4_ETB_CID3

Component Identification Register 3
Address: 0xE008DFFC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CoreSight TRM for details of register description. See link in TRC_CSTF.CSTFCTL register. Default Value: 0x000000B1

CM4_TPIU_TPIU_SSPSR

Supported Parallel Port Size Register
Address: 0xE008E000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	CM4 TPIU is used as TPIU. Refer CM4 TRM register descriptions: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.100166_0001_00_en/index.html Default Value: 0

CM4_TPIU_TPIU_CSPSR

Current Parallel Port Size Register
Address: 0xE008E004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. Default Value: 0x00000001

CM4_TPIU_TPIU_ACPR

Asynchronous Clock Prescaler Register
Address: 0xE008E010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. Default Value: 0

CM4_TPIU_TPIU_SPPR

Selected Pin Protocol Register
Address: 0xE008E0F0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. Default Value: 0x00000001

CM4_TPIU_TPIU_FFSR

Formatter and Flush Status Register
Address: 0xE008E300
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. Default Value: 0x00000008

CM4_TPIU_TPIU_FFCR

Formatter and Flush Control Register
Address: 0xE008E304
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. Default Value: 0x00000102

CM4_TPIU_TPIU_FSCR

Formatter Synchronization Counter Register
Address: 0xE008E308
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. Default Value: 0

CM4_TPIU_TRIGGER

TRIGGER register
Address: 0xE008EEE8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. Default Value: 0

CM4_TPIU_FIFO_DATA_0

Integration ETM Data
Address: 0xE008EEEC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. Default Value: 0

CM4_TPIU_ITATBCTR2

Integration Register
Address: 0xE008EEF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. Default Value: 0

CM4_TPIU_FIFO_DATA_1

Integration ITM Data
Address: 0xE008EEFC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. Default Value: 0

CM4_TPIU_ITCTRL

Integration Mode Control Register
Address: 0xE008EF00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							MODE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	MODE	When set, the component enters integration mode, enabling topology detection or integration testing to be performed. At reset the component must enter functional mode. If no integration functionality is implemented, this register must read as zero. Default Value: 0

CM4_TPIU_CLAIMSET

Claim Tag Set Register
Address: 0xE008EFA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S			
HW Access	None				R			
Name	None [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TAG	A bit programmable register bank which sets the Claim Tag Value. A read will return a logic 1 for all implemented locations. Default Value: 0xF

CM4_TPIU_CLAIMCLR

Claim Tag Clear Register
Address: 0xE008EFA4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C			
HW Access	None				R			
Name	None [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TAG	A bit programmable register bank that is zero at reset. Default Value: 0

CM4_TPIU_DEVID

Device ID
Address: 0xE008EFC8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R	R				
HW Access	R		R	R				
Name	FIFOSIZE [7:6]		CLKRELAT	MUXNUM [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				R	R	R	R
Name	None [15:12]				SWOUARTNRZ	SWOMAN	TCLKDATA	FIFOSIZE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SWOUARTNRZ	Indicates whether Serial Wire Output, UART or NRZ, is supported. Default Value: 1
10	SWOMAN	Indicates whether Serial Wire Output, Manchester encoded format, is supported. Default Value: 1
9	TCLKDATA	This bit Reads-As-Zero (RAZ), indicating that trace data and clock modes are supported Default Value: 0
8 : 6	FIFOSIZE	TPIU buffer size. This field value is 0b010 indicating 4 Bytes. Default Value: 2
5	CLKRELAT	Indicates the relationship between atclk and traceclkin. This bit is '1' indicating traceclkin can be asynchronos to atclk. Default Value: 1

4 : 0	MUXNUM	Indicates the level of input multiplexing. When non-zero, this value indicates the type of multiplexing on the input to the ATB. Currently only 0x00 is supported, that is, no multiplexing is present. This value helps detect the ATB structure. Default Value: 0

CM4_TPIU_DEVTYPE

Device Type Identifier Register
Address: 0xE008EFCC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	SUB_TYPE [7:4]				CLASS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	SUB_TYPE	Indicates that this component is a trace port component. Default Value: 0x1
3 : 0	CLASS	Indicates that this is trace sink component. Default Value: 0x1

CM4_TPIU_PID4

Peripheral Identification Register 4
Address: 0xE008EFD0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. Default Value: 0x00000004

CM4_TPIU_PID5

Peripheral Identification Register 5
Address: 0xE008EFD4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. Default Value: 0x00000000

CM4_TPIU_PID6

Peripheral Identification Register 6
Address: 0xE008EFD8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. Default Value: 0x00000000

CM4_TPIU_PID7

Peripheral Identification Register 7
Address: 0xE008EFDC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. Default Value: 0x00000000

CM4_TPIU_PID0

Peripheral Identification Register 0
Address: 0xE008EFE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. PID0 indicates this is M3-TPIU (but this is a non-issue) Default Value: 0x00000023

CM4_TPIU_PID1

Peripheral Identification Register 1
Address: 0xE008EFE4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. Default Value: 0x000000B9

CM4_TPIU_PID2

Peripheral Identification Register 2
Address: 0xE008EFE8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. Default Value: 0x0000003B

CM4_TPIU_PID3

Peripheral Identification Register 3
Address: 0xE008EFEC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None			
HW Access	R				None			
Name	ECOREVNUM [7:4]				None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	ECOREVNUM	Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. Default Value: 0x0

CM4_TPIU_CID0

Component Identification Register 0
Address: 0xE008EFF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. Default Value: 0x0000000D

CM4_TPIU_CID1

Component Identification Register 1
Address: 0xE008EFF4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. Default Value: 0x00000090

CM4_TPIU_CID2

Component Identification Register 2
Address: 0xE008EFF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. Default Value: 0x00000005

CM4_TPIU_CID3

Component Identification Register 3
Address: 0xE008EFFC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CM4 TRM and CoreSight TRM for register descriptions. See links in TRC_TPIU.SSPSR register. Default Value: 0x000000B1

CM0P_ROM_ROM_SCS

CM0+ CoreSight ROM Table Peripheral #0
Address: 0xE00FF000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to SCS ROM Table Default Value: 0xFFF0F003

CM4_ROMTABLE_TRC_CTI

CM4 CoreSight ROM Table Peripheral #0
Address: 0xE00FF000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to TRC CTI component Default Value: 0xFFF81003

CM0P_ROM_ROM_DWT

CM0+ CoreSight ROM Table Peripheral #1
Address: 0xE00FF004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to DWT ROM Table Default Value: 0xFFF02003

CM4_ROMTABLE_TRC_CSTF

CM4 CoreSight ROM Table Peripheral #1
Address: 0xE00FF004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to TRC funnel component. Default Value: 0xFFF8D003

CM0P_ROM_ROM_BPU

CM0+ CoreSight ROM Table Peripheral #2
Address: 0xE00FF008
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to BPU ROM Table Default Value: 0xFFF03003

CM4_ROMTABLE_TRC_ETB

CM4 CoreSight ROM Table Peripheral #2
Address: 0xE00FF008
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to ETB component. Default Value: 0xFFF8E003

CM0P_ROM_ROM_END

CM0+ CoreSight ROM Table End Marker
Address: 0xE00FF00C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	End marker in peripheral list Default Value: 0

CM4_ROMTABLE_TRC_TPIU

CM4 CoreSight ROM Table Peripheral #3
Address: 0xE00FF00C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to TPIU ROM Table Default Value: 0xFFF8F003

CM4_ROMTABLE_CM4

CM4 CoreSight ROM Table Peripheral #4
Address: 0xE00FF010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to CM4 ROM Table Default Value: 0xFFF80003

CM0P_ROM_ROM_CSMT

CM0+ CoreSight ROM Table Memory Type
Address: 0xE00FFFCC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Memory Type Default Value: 1

CM4_ROMTABLE_CSMT

CM4 CoreSight ROM Table Memory Type
Address: 0xE00FFFCC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Memory Type Default Value: 1

CM0P_ROM_ROM_PID4

CM0+ CoreSight ROM Table Peripheral ID #4
Address: 0xE00FFFD0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 0x00000004

CM4_ROMTABLE_PID4

CM4 CoreSight ROM Table Peripheral ID #4
Address: 0xE00FFFD0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 0x00000004

CM0P_ROM_ROM_PID0

CM0+ CoreSight ROM Table Peripheral ID #0
Address: 0xE00FFFE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 0x000000C0

CM4_ROMTABLE_PID0

CM4 CoreSight ROM Table Peripheral ID #0
Address: 0xE00FFFE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 0x000000C0

CM0P_ROM_ROM_PID1

CM0+ CoreSight ROM Table Peripheral ID #1
Address: 0xE00FFFE4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 0x000000B4

CM4_ROMTABLE_PID1

CM4 CoreSight ROM Table Peripheral ID #1
Address: 0xE00FFFE4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 0x000000B4

CM0P_ROM_ROM_PID2

CM0+ CoreSight ROM Table Peripheral ID #2
Address: 0xE00FFFE8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 0x0000000B

CM4_ROMTABLE_PID2

CM4 CoreSight ROM Table Peripheral ID #2
Address: 0xE00FFFE8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 0x0000000B

CM0P_ROM_ROM_PID3

CM0+ CoreSight ROM Table Peripheral ID #3
Address: 0xE00FFFEC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

CM4_ROMTABLE_PID3

CM4 CoreSight ROM Table Peripheral ID #3
Address: 0xE00FFFEC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

CM0P_ROM_ROM_CID0

CM0+ CoreSight ROM Table Component ID #0
Address: 0xE00FFFF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 0x0000000D

CM4_ROMTABLE_CID0

CM4 CoreSight ROM Table Component ID #0
Address: 0xE00FFFF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 0x0000000D

CM0P_ROM_ROM_CID1

CM0+ CoreSight ROM Table Component ID #1
Address: 0xE00FFFF4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 0x00000010

CM4_ROMTABLE_CID1

CM4 CoreSight ROM Table Component ID #1
Address: 0xE00FFFF4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 0x00000010

CM0P_ROM_ROM_CID2

CM0+ CoreSight ROM Table Component ID #2
Address: 0xE00FFFF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 0x00000005

CM4_ROMTABLE_CID2

CM4 CoreSight ROM Table Component ID #2
Address: 0xE00FFFF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 0x00000005

CM0P_ROM_ROM_CID3

CM0+ CoreSight ROM Table Component ID #3
Address: 0xE00FFFFC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 0x000000B1

CM4_ROMTABLE_CID3

CM4 CoreSight ROM Table Component ID #3
Address: 0xE00FFFFC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 0x000000B1

CM0P_ROMTABLE_ADDR0

Link to Cortex M0+ ROM Table.
Address: 0xF0000000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						R	R
Name	None [7:2]						FORMAT_32BIT	PRESENT

Bits	15	14	13	12	11	10	9	8
SW Access	R				None			
HW Access	R				None			
Name	ADDR_OFFSET [15:12]				None [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR_OFFSET [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR_OFFSET [31:24]							

Bits	Name	Description
31 : 12	ADDR_OFFSET	Address offset of the Cortex-M0 ROM Table base address (0xe00f:f000) wrt. Cypress chip specific ROM Table base address (0xf000:0000). ADDR_OFFSET[19:0] = 0xe00f:f - 0xf000:0 = 0xf00f:f. Default Value: 0xF00FF
1	FORMAT_32BIT	ROM Table format: '0: 8-bit format. '1': 32-bit format. Default Value: 1
0	PRESENT	Entry present. Default Value: 1

CM0P_ROMTABLE_ADDR1

Link to CoreSight CTI Table.
Address: 0xF0000004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						R	R
Name	None [7:2]						FORMAT_32BIT	PRESENT

Bits	15	14	13	12	11	10	9	8
SW Access	R				None			
HW Access	R				None			
Name	ADDR_OFFSET [15:12]				None [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR_OFFSET [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR_OFFSET [31:24]							

Bits	Name	Description
31 : 12	ADDR_OFFSET	Address offset of the Cortex-M0 ROM Table base address (0xe00f:f000) wrt. Cypress chip specific ROM Table base address (0xf000:0000). ADDR_OFFSET[19:0] = 0xe00f:f - 0xf000:0 = 0xf00f:f. Default Value: 0x00002
1	FORMAT_32BIT	ROM Table format: '0: 8-bit format. '1': 32-bit format. Default Value: 1
0	PRESENT	Entry present. Default Value: 1

CM0P_ROMTABLE_ADDR2

Link to Cortex M0+ MTB Table.
Address: 0xF0000008
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						R	R
Name	None [7:2]						FORMAT_32BIT	PRESENT

Bits	15	14	13	12	11	10	9	8
SW Access	R				None			
HW Access	R				None			
Name	ADDR_OFFSET [15:12]				None [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR_OFFSET [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR_OFFSET [31:24]							

Bits	Name	Description
31 : 12	ADDR_OFFSET	Address offset of the Cortex-M0 ROM Table base address (0xe00f:f000) wrt. Cypress chip specific ROM Table base address (0xf000:0000). ADDR_OFFSET[19:0] = 0xe00f:f - 0xf000:0 = 0xf00f:f. Default Value: 0x00003
1	FORMAT_32BIT	ROM Table format: '0: 8-bit format. '1': 32-bit format. Default Value: 1
0	PRESENT	Entry present. Default Value: 1

CM0P_ROMTABLE_DID

Device Type Identifier register.
Address: 0xF0000FCC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 0x00000001

CM0P_ROMTABLE_PID4

Peripheral Identification Register 4.
Address: 0xF0000FD0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	COUNT [7:4]				JEP_CONTINUATION [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	COUNT	Size of ROM Table is 2^COUNT * 4 KByte. Default Value: 0
3 : 0	JEP_CONTINUATION	JEP106 continuation code. This value is product specific and specified as part of the product definition in the CPUSS.JEPCONTINUATION parameter. Default Value: Undefined

CM0P_ROMTABLE_PID5

Peripheral Identification Register 5.
Address: 0xF0000FD4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 0

CM0P_ROMTABLE_PID6

Peripheral Identification Register 6.
Address: 0xF0000FD8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 0

CM0P_ROMTABLE_PID7

Peripheral Identification Register 7.
Address: 0xF0000FDC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 0

CM0P_ROMTABLE_PID0

Peripheral Identification Register 0.
Address: 0xF0000FE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	PN_MIN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PN_MIN	JEP106 part number. 4 lsbs of CPUSS.PARTNUMBER parameter. Default Value: Undefined

CM0P_ROMTABLE_PID1

Peripheral Identification Register 1.
Address: 0xF0000FE4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	JEPID_MIN [7:4]				PN_MAJ [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	JEPID_MIN	JEP106 vendor id. 4 lsbs of CPUSS.JEPID parameter. Default Value: Undefined
3 : 0	PN_MAJ	JEP106 part number. 4 msbs of CPUSS.PARTNUMBER parameter. Default Value: Undefined

CM0P_ROMTABLE_PID2

Peripheral Identification Register 2.
Address: 0xF0000FE8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None	R		
HW Access	R				None	R		
Name	REV [7:4]				None	JEPID_MAJ [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	REV	Major REVision number (chip specific). Identifies the design iteration of the component. For first tape out: 0x1. This field is incremented on subsequent tape outs. Default Value: Undefined
2 : 0	JEPID_MAJ	JEP106 vendor id. 4 msbs of CPUSS.JEPID parameter. Default Value: Undefined

CM0P_ROMTABLE_PID3

Peripheral Identification Register 3.
Address: 0xF0000FEC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	REV_AND [7:4]				CM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	REV_AND	Minor REVision number (chip specific). For first tape out: 0x1. This field is incremented on subsequent tape outs. Default Value: Undefined
3 : 0	CM	Default Value: 0

CM0P_ROMTABLE_CID0

Component Identification Register 0.
Address: 0xF0000FF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 0 of 4-byte component identification 0xB105:100D. Default Value: 0x0000000D

CM0P_ROMTABLE_CID1

Component Identification Register 1.
Address: 0xF0000FF4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 1 of 4-byte component identification 0xB105:100D. Component class: "ROM Table". Default Value: 0x00000010

CM0P_ROMTABLE_CID2

Component Identification Register 2.
Address: 0xF0000FF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 2 of 4-byte component identification 0xB105:100D. Default Value: 0x00000005

CM0P_ROMTABLE_CID3

Component Identification Register 3.
Address: 0xF0000FFC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 3 of 4-byte component identification 0xB105:100D. Default Value: 0x000000B1

CM0P_CTI_CTICONTROL

CTI Control Register
Address: 0xF0002000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							GLBEN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	GLBEN	Enables or disables the ECT: 0 = disabled (reset) 1 = enabled. When disabled, all cross triggering mapping logic functionality is disabled for this processor. Default Value: 0

CM0P_CTI_CTIINTACK

CTI Interrupt Acknowledge Register
Address: 0xF0002010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	INTACK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	INTACK	Acknowledges the corresponding CTITRIGOUT output: 1 = CTITRIGOUT is acknowledged and is cleared when MAPTRIGOUT is LOW. 0 = no effect. There is one bit of the register for each CTITRIGOUT output. Default Value: 0

CM0P_CTI_CTIAPPSET

CTI Application Trigger Set Register
Address: 0xF0002014
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				APPSET [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	APPSET	Setting a bit HIGH generates a channel event for the selected channel. Read: 0 = application trigger inactive (reset) 1 = application trigger active. Write: 0 = no effect 1 = generate channel event. There is one bit of the register for each channel. Default Value: 0

CM0P_CTI_CTIAPPCLEAR

CTI Application Trigger Clear Register
Address: 0xF0002018
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				W			
HW Access	None				R			
Name	None [7:4]				APPCLEAR [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	APPCLEAR	Clears corresponding bits in the CTIAPPSET register. 1 = application trigger disabled in the CTIAPPSET register 0 = no effect. There is one bit of the register for each channel. Default Value: 0

CM0P_CTI_CTIAPPPULSE

CTI Application Pulse Register
Address: 0xF000201C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				W			
HW Access	None				R			
Name	None [7:4]				APPULSE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	APPULSE	Setting a bit HIGH generates a channel event pulse for the selected channel. Write: 1 = channel event pulse generated for one CTICLK period 0 = no effect. There is one bit of the register for each channel. Default Value: 0

CM0P_CTI_CTIINEN0

CTI Trigger to Channel Enable Registers
Address: 0xF0002020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGINEN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TRIGINEN	Enables a cross trigger event to the corresponding channel when an CTITRIGIN is activated. 1 = enables the CTITRIGIN signal to generate an event on the respective channel of the CTM. There is one bit of the register for each of the four channels. For example in register CTIINEN0, TRIGINEN[0] set to 1 enables CTITRIGIN onto channel 0. 0 = disables the CTITRIGIN signal from generating an event on the respective channel of the CTM. Default Value: 0

CM0P_CTI_CTIOUTEN0

CTI Channel to Trigger Enable Registers
Address: 0xF00020A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGOUTEN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TRIGOUTEN	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate an CTITRIGOUT output: 0 = the channel input (CTICHIN) from the CTM is not routed to the CTITRIGOUT output 1 = the channel input (CTICHIN) from the CTM is routed to the CTITRIGOUT output. There is one bit for each of the four channels. For example in register CTIOUTEN0, enabling bit 0 enables CTICHIN[0] to cause a trigger event on the CTITRIGOUT[0] output. Default Value: 0

CM0P_CTI_CTITRIGINSTATUS

CTI Trigger In Status Register
Address: 0xF0002130
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TRIGINSTATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	TRIGINSTATUS	Shows the status of the CTITRIGIN inputs: 1 = CTITRIGIN is active 0 = CTITRIGIN is inactive. Because the register provides a view of the raw CTITRIGIN inputs, the reset value is unknown. There is one bit of the register for each trigger input. Default Value: 0

CM0P_CTI_CTITRIGOUTSTATUS

CTI Trigger Out Status Register
Address: 0xF0002134
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TRIGOUTSTATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	TRIGOUTSTATUS	Shows the status of the CTITRIGOUT outputs. 1 = CTITRIGOUT is active 0 = CTITRIGOUT is inactive (reset). There is one bit of the register for each trigger output. Default Value: 0

CM0P_CTI_CTICHINSTATUS

CTI Channel In Status Register
Address: 0xF0002138
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				RW			
Name	None [7:4]				CTICHINSTATUS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	CTICHINSTATUS	Shows the status of the CTICHIN inputs: 1 = CTICHIN is active 0 = CTICHIN is inactive. Because the register provides a view of the raw CTICHIN inputs from the CTM, the reset value is unknown. There is one bit of the register for each channel input. Default Value: 0

CM0P_CTI_CTICHOUTSTATUS

CTI Channel Out Status Register
Address: 0xF000213C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				RW			
Name	None [7:4]				CTICHOUTSTATUS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	CTICHOUTSTATUS	Shows the status of the CTICHOUT outputs. 1 = CTICHOUT is active 0 = CTICHOUT is inactive (reset). There is one bit of the register for each channel output. Default Value: 0

CM0P_CTI_CTIGATE

Enable CTI Channel Gate Register
Address: 0xF0002140
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				CTIGATEEN3	CTIGATEEN2	CTIGATEEN1	CTIGATEEN0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	CTIGATEEN3	Enable CTICHOUT3. Set to 0 to disable channel propagation. Default Value: 1
2	CTIGATEEN2	Enable CTICHOUT2. Set to 0 to disable channel propagation. Default Value: 1
1	CTIGATEEN1	Enable CTICHOUT1. Set to 0 to disable channel propagation. Default Value: 1
0	CTIGATEEN0	Enable CTICHOUT0. Set to 0 to disable channel propagation. Default Value: 1

CM0P_CTI_ASICCTL

External Multiplexor Control Register
Address: 0xF0002144
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ASICCTL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	ASICCTL	Implementation-defined ASIC control, value written to the register is output on ASICCTL[7:0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM. See ECT CoreSight defined registers on Arm TRM page 4-28. Default Value: 0

CM0P_CTI_ITCHINACK

ITCHINACK Register
Address: 0xF0002EDC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				W			
HW Access	None				R			
Name	None [7:4]				CTCHINACK [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	CTCHINACK	Set the value of the CTCHINACK outputs Default Value: 0

CM0P_CTI_ITTRIGINACK

ITTRIGINACK Register
Address: 0xF0002EE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	CTTRIGINACK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CTTRIGINACK	Set the value of the CTTRIGINACK outputs Default Value: 0

CM0P_CTI_ITCHOUT

ITCHOUT Register
Address: 0xF0002EE4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				W			
HW Access	None				R			
Name	None [7:4]				CTCHOUT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	CTCHOUT	Set the value of the CTCHOUT outputs Default Value: 0

CM0P_CTI_ITTRIGOUT

ITTRIGOUT Register
Address: 0xF0002EE8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	CTTRIGOUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CTTRIGOUT	Set the value of the CTTRIGOUT outputs Default Value: 0

CM0P_CTI_ITCHOUTACK

ITCHOUTACK Register
Address: 0xF0002EEC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				CTCHOUTACK [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	CTCHOUTACK	Read the values of the CTCHOUTACK inputs Default Value: 0

CM0P_CTI_ITTRIGOUTACK

ITTRIGOUTACK Register
Address: 0xF0002EF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CTTRIGOUTACK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CTTRIGOUTACK	Read the values of the CTTRIGOUTACK inputs Default Value: 0

CM0P_CTI_ITCHIN

ITCHIN Register
Address: 0xF0002EF4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				CTCHIN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	CTCHIN	Read the values of the CTCHIN inputs Default Value: 0

CM0P_CTI_ITTRIGIN

ITTRIGIN Register
Address: 0xF0002EF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CTTRIGIN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CTTRIGIN	Read the values of the CTTRIGIN inputs Default Value: 0

CM0P_CTI_ITCTRL

Integration Mode Control Register
Address: 0xF0002F00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							MODE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	MODE	When set, the component enters integration mode, enabling topology detection or integration testing to be performed. At reset the component must enter functional mode. If no integration functionality is implemented, this register must read as zero. Default Value: 0

CM0P_CTI_CLAIMSET

Claim Tag Set Register
Address: 0xF0002FA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S			
HW Access	None				R			
Name	None [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TAG	A bit programmable register bank which sets the Claim Tag Value. A read will return a logic 1 for all implemented locations. Default Value: 0xF

CM0P_CTI_CLAIMCLR

Claim Tag Clear Register
Address: 0xF0002FA4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C			
HW Access	None				R			
Name	None [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TAG	A bit programmable register bank that is zero at reset. Default Value: 0

CM0P_CTI_LOCKACCESS

Lock Access Register
Address: 0xF0002FB0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				ACCESS_CODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	ACCESS_CODE	Write Access Code. A write of 0xC5ACCE55 enables further write access to this device. An invalid write will have the affect of removing write access. If LOCKSTATUS[2] is set, then only bits [7:0] of this register are implemented and lock access is obtained by consecutively writing 0xC5, 0xAC, 0xCE, 0x55. Bits [31:8] are unused and any writes to them ignored. Default Value: 0

CM0P_CTI_LOCKSTATUS

Lock Status Register
Address: 0xF0002FB4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					IMPLEMENTS_8B	ACCESS_PERMITTED	EXISTS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	IMPLEMENTS_8B	This component implements an 8-bit Lock Access Register. Default Value: 0
1	ACCESS_PERMITTED	The values of this bit mean: 0 = Access permitted. 1 = Write access to the component is blocked. All writes to control registers are ignored. Reads are permitted Default Value: 0
0	EXISTS	Indicates that a lock control mechanism exists for this device Default Value: 0

CM0P_CTI_AUTHSTATUS

Authentication Status Register
Address: 0xF0002FB8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R		R		R	
HW Access	W		W		W		W	
Name	SNIDBG [7:6]		SIDBG [5:4]		NSNIDBG [3:2]		NSIDBG [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SNIDBG	Secure Non-Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0
5 : 4	SIDBG	Secure Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0
3 : 2	NSNIDBG	Non-Secure Non-Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0

1 : 0	NSIDBG	Non-Secure Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0

CM0P_CTI_DEVID

Device Configuration Register
Address: 0xF0002FC8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			R				
Name	None [7:5]			NRMUXING [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	NRTRIG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				R			
Name	None [23:20]				NRCHAN [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	NRCHAN	Number of ECT channels available. Default Value: 4
15 : 8	NRTRIG	Number of ECT triggers available. Default Value: 8
4 : 0	NRMUXING	Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using ASICCTL. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog `define EXTMUXNUM that you must alter accordingly. Default Value: 0

CM0P_CTI_DEVTYPE

Device Type Identifier Register
Address: 0xF0002FCC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	SUB_TYPE [7:4]				CLASS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	SUB_TYPE	cross trigger Default Value: 0x1
3 : 0	CLASS	debug control logic component Default Value: 0x4

CM0P_CTI_PID4

Peripheral Identification Register 4
Address: 0xF0002FD0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000004

CM0P_CTI_PID5

Peripheral Identification Register 5
Address: 0xF0002FD4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

CM0P_CTI_PID6

Peripheral Identification Register 6
Address: 0xF0002FD8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

CM0P_CTI_PID7

Peripheral Identification Register 7
Address: 0xF0002FDC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

CM0P_CTI_PID0

Peripheral Identification Register 0
Address: 0xF0002FE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x000000A6

CM0P_CTI_PID1

Peripheral Identification Register 1
Address: 0xF0002FE4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x000000B9

CM0P_CTI_PID2

Peripheral Identification Register 2
Address: 0xF0002FE8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x0000000B

CM0P_CTI_PID3

Peripheral Identification Register 3
Address: 0xF0002FEC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None			
HW Access	R				None			
Name	ECOREVNUM [7:4]				None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	ECOREVNUM	ECO revision for MTB Default Value: 0x0

CM0P_CTI_CID0

Component Identification Register 0
Address: 0xF0002FF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x0000000D

CM0P_CTI_CID1

Component Identification Register 1
Address: 0xF0002FF4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000090

CM0P_CTI_CID2

Component Identification Register 2
Address: 0xF0002FF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000005

CM0P_CTI_CID3

Component Identification Register 3
Address: 0xF0002FFC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x000000B1

CM0P_MTB_POSITION

POSITION register
Address: 0xF0003000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	None	
HW Access	RW					RW	None	
Name	POINTER [7:3]					WRAP	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	POINTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	POINTER [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	POINTER [31:24]							

Bits	Name	Description

31 : 3	POINTER	Trace packet location pointer. Because a packet consists of two words, the POINTER field is the location of the first word of a packet. This field contains bits [31:3] of the address, in the SRAM, where the next trace packet will be written. The field points to an unused location and is automatically incremented. A debug agent can calculate the system address, on the AHB-Lite bus, of the SRAM location pointed to by the POSITION register using the following equation: system address = BASE + ((P + (2^AWIDTH - (BASE MOD 2^AWIDTH))) MOD 2^AWIDTH). Where P = POSITION AND 0xFFFF_FFF8. Where BASE is the BASE register value. Note: - The size of the SRAM is parameterized and the most significant bits of the POINTER field can be RAZ/WI, depending on the AWIDTH parameter value. - POSITION register bits greater than or equal to AWIDTH are RAZ/WI, therefore, the active POINTER field bits are [AWIDTH-4:0]. - The POINTER field value is relative to the base address of the SRAM in the system memory map. Default Value: X
2	WRAP	This bit is set to 1 automatically when the POINTER value wraps as determined by the MASTER.MASK field in the MASTER Trace Control Register. Default Value: X

CM0P_MTB_MASTER

MASTER register
Address: 0xF0003004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW				
HW Access	R	R	R	R				
Name	SFRWPRIV	TSTOPEN	TSTARTEN	MASK [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						RW	R
Name	None [15:10]						HALTREQ	RAMPRIV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	EN	None [30:24]						

Bits	Name	Description

31	EN	Main trace enable bit. When this bit is 1 trace data is written into the SRAM memory location addressed by POSITION.POINTER. The POSITION.POINTER value auto increments after the trace data packet is written. The EN bit can be automatically set to 0 using the FLOW.WATERMARK field and the FLOW.AUTOSTOP bit. The EN bit is automatically set to 1 if the TSTARTEN bit is 1 and the TSTART signal is HIGH. The EN bit is automatically set to 0 if TSTOPEN bit is 1 and the TSTOP signal is HIGH. Note: If the EN bit is set to 0 because the FLOW.WATERMARK field is set, then it is not automatically set to 1 if the TSTARTEN bit is 1 and the TSTART input is HIGH. In this case tracing can only be restarted if the FLOW.WATERMARK or POSITION.POINTER value is changed by software. Default Value: 0
9	HALTREQ	Halt request bit. This bit is connected to the halt request signal of the trace logic, EDBGRQ. When HALTREQ is set to 1, EDBGRQ is asserted if DBGEN is also HIGH. The HALTREQ bit can be automatically set to 1 using the FLOW.WATERMARK field. Default Value: 0
8	RAMPRIV	SRAM Privilege bit. If this bit is 0, then User or Privileged AHB-Lite read and write accesses to the SRAM are permitted. If this bit is 1, then only Privileged AHB-Lite read and write accesses to the SRAM are permitted and User accesses are RAZ/WI. The HPROT[1] signal determines if an access is User or Privileged. Note This bit is implemented only if User/Privilege support is present in the MTB configuration. If User/Privilege support is absent, then the behavior of this bit is RAZ/WI and the value of the HPROT[1] signal is ignored. Default Value: 0

7	SFRWPRIV	Special Function Register Write Privilege bit. If this bit is 0, then User or Privileged AHB-Lite read and write accesses to the Special Function Registers are permitted. If this bit is 1, then only Privileged write accesses are permitted and User write accesses are ignored. The HPROT[1] signal determines if an access is User or Privileged. Note - SFR read accesses are not controlled by this bit and are always permitted. - This bit is implemented only if User/Privilege support is present in the MTB configuration. If User/ Privilege support is absent, then the behavior of this bit is RAZ/WI and the value of the HPROT[1] signal is ignored. Default Value: 1
6	TSTOPEN	Trace stop input enable. If this bit is 1 and the TSTOP signal is HIGH, then the EN bit is set to 0. If a trace packet is being written to memory, the write is completed before tracing is stopped. Default Value: 0
5	TSTARTEN	Trace start input enable. If this bit is 1 and the TSTART signal is HIGH, then the EN bit is set to 1. Tracing continues until a stop condition occurs. Default Value: 0
4 : 0	MASK	This value determines the maximum size of the trace buffer in SRAM. It specifies the most-significant bit of the POSITION.POINTER field that can be updated by automatic increment. If the trace tries to advance past this power of two, the POSITION.WRAP bit is set to 1, the POSITION.POINTER[MASK:0] bits are set to zero, and the POSITION.POINTER[AWIDTH-4:MASK+1] bits remain unchanged. This field causes the trace packet information to be stored in a circular buffer of size 2(MASK+4) bytes, that can be positioned in memory at multiples of this size. Valid values of this field are zero to AWIDTH-4. Values greater than the maximum have the same effect as the maximum. Default Value: X

CM0P_MTB_FLOW

FLOW register
Address: 0xF0003008
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None	RW	RW
HW Access	R					None	R	R
Name	WATERMARK [7:3]					None	AUTOHALT	AUTOSTOP

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WATERMARK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	WATERMARK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	WATERMARK [31:24]							

Bits	Name	Description
31 : 3	WATERMARK	WATERMARK value. This field contains an address in the same format as the POSITION.POINTER field. When the POSITION.POINTER matches the WATERMARK field value, actions defined by the AUTOHALT and AUTOSTOP bits are performed. Default Value: X
1	AUTOHALT	If this bit is 1 and WATERMARK is equal to POSITION.POINTER, then the MASTER.HALTREQ bit is automatically set to 1. If the DBGEN signal is HIGH, the MTB asserts this halt request to the Cortex-M0+ processor by asserting the EDBGRQ signal. Default Value: 0
0	AUTOSTOP	If this bit is 1 and WATERMARK is equal to POSITION.POINTER, then the MASTER.EN bit is automatically set to 0. This stops tracing. Default Value: 0

CM0P_MTB_BASE

BASE register
Address: 0xF000300C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	BASE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	BASE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	BASE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	BASE [31:24]							

Bits	Name	Description
31 : 0	BASE	The value provided is the value of the SRAMBASEADDR[31:0] signal. MTB SRAM base address in the processor memory map, which is fixed for this platform. Default Value: 0xF0010000

CM0P_MTB_LA

Lock Access register
Address: 0xF0003FB0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

CM0P_MTB_LS

Lock Status register
Address: 0xF0003FB4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

CM0P_MTB_AS

Authentication Status register
Address: 0xF0003FB8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R	R	R	R
HW Access	R				R	R	R	R
Name	AS_31to4 [7:4]				AS_3	NIDEN	AS_1	DBGEN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	AS_31to4 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	AS_31to4 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	AS_31to4 [31:24]							

Bits	Name	Description
31 : 4	AS_31to4	Default Value: 0x0000000
3	AS_3	Default Value: 1
2	NIDEN	Non-invasive debug enable Default Value: 0
1	AS_1	Default Value: 1
0	DBGEN	Invasive debug enable Default Value: 0

CM0P_MTB_DARCH

Device Architecture register
Address: 0xF0003FBC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	ARCH_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ARCH_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R			R	R			
HW Access	R			R	R			
Name	ARCHITECT [23:21]			RES_20	REVISION [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ARCHITECT [31:24]							

Bits	Name	Description
31 : 21	ARCHITECT	Architect ARM Default Value: 0x23B
20	RES_20	Reserved Default Value: 1
19 : 16	REVISION	Minor Architecture Revision Default Value: 0x0
15 : 0	ARCH_ID	Basic Trace Router Architecture Major Architecture Revision 0 Default Value: 0x0A31

CM0P_MTB_DCFG

Device Configuration register
Address: 0xF0003FC8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

CM0P_MTB_DID

Device Type Identifier register.
Address: 0xF0003FCC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	SUB_TYPE [7:4]				CLASS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	SUB_TYPE	Basic Trace Router Default Value: 0x3
3 : 0	CLASS	Trace Sink Default Value: 0x1

CM0P_MTB_PID4

Peripheral Identification Register 4.
Address: 0xF0003FD0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000004

CM0P_MTB_PID5

Peripheral Identification Register 5.
Address: 0xF0003FD4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

CM0P_MTB_PID6

Peripheral Identification Register 6.
Address: 0xF0003FD8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

CM0P_MTB_PID7

Peripheral Identification Register 7.
Address: 0xF0003FDC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

CM0P_MTB_PID0

Peripheral Identification Register 0.
Address: 0xF0003FE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000032

CM0P_MTB_PID1

Peripheral Identification Register 1.
Address: 0xF0003FE4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x000000B9

CM0P_MTB_PID2

Peripheral Identification Register 2.
Address: 0xF0003FE8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x0000001B

CM0P_MTB_PID3

Peripheral Identification Register 3.
Address: 0xF0003FEC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None			
HW Access	R				None			
Name	ECOREVNUM [7:4]				None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	ECOREVNUM	ECO revision for MTB Default Value: 0x0

CM0P_MTB_CID0

Component Identification Register 0.
Address: 0xF0003FF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x0000000D

CM0P_MTB_CID1

Component Identification Register 1.
Address: 0xF0003FF4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000090

CM0P_MTB_CID2

Component Identification Register 2.
Address: 0xF0003FF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000005

CM0P_MTB_CID3

Component Identification Register 3.
Address: 0xF0003FFC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x000000B1

2 Interprocessor communication (IPC)

Register details

Register name	Address	Description
IPC_STRUCT0_ACQUIRE	0x40220000	IPC acquire
IPC_STRUCT0_RELEASE	0x40220004	IPC release
IPC_STRUCT0_NOTIFY	0x40220008	IPC notification
IPC_STRUCT0_DATA0	0x4022000C	IPC data 0
IPC_STRUCT0_DATA1	0x40220010	IPC data 1
IPC_STRUCT0_LOCK_STATUS	0x4022001C	IPC lock status
IPC_STRUCT1_ACQUIRE	0x40220020	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT1_RELEASE	0x40220024	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT1_NOTIFY	0x40220028	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT1_DATA0	0x4022002C	IPC data 0. See IPC_STRUCT0_DATA0 for the details of bit fields.
IPC_STRUCT1_DATA1	0x40220030	IPC data 1. See IPC_STRUCT0_DATA1 for the details of bit fields.
IPC_STRUCT1_LOCK_STATUS	0x4022003C	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT2_ACQUIRE	0x40220040	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT2_RELEASE	0x40220044	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT2_NOTIFY	0x40220048	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT2_DATA0	0x4022004C	IPC data 0. See IPC_STRUCT0_DATA0 for the details of bit fields.
IPC_STRUCT2_DATA1	0x40220050	IPC data 1. See IPC_STRUCT0_DATA1 for the details of bit fields.
IPC_STRUCT2_LOCK_STATUS	0x4022005C	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT3_ACQUIRE	0x40220060	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT3_RELEASE	0x40220064	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT3_NOTIFY	0x40220068	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT3_DATA0	0x4022006C	IPC data 0. See IPC_STRUCT0_DATA0 for the details of bit fields.
IPC_STRUCT3_DATA1	0x40220070	IPC data 1. See IPC_STRUCT0_DATA1 for the details of bit fields.

Register name	Address	Description
IPC_STRUCT3_LOCK_STATUS	0x4022007C	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT4_ACQUIRE	0x40220080	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT4_RELEASE	0x40220084	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT4_NOTIFY	0x40220088	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT4_DATA0	0x4022008C	IPC data 0. See IPC_STRUCT0_DATA0 for the details of bit fields.
IPC_STRUCT4_DATA1	0x40220090	IPC data 1. See IPC_STRUCT0_DATA1 for the details of bit fields.
IPC_STRUCT4_LOCK_STATUS	0x4022009C	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT5_ACQUIRE	0x402200A0	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT5_RELEASE	0x402200A4	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT5_NOTIFY	0x402200A8	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT5_DATA0	0x402200AC	IPC data 0. See IPC_STRUCT0_DATA0 for the details of bit fields.
IPC_STRUCT5_DATA1	0x402200B0	IPC data 1. See IPC_STRUCT0_DATA1 for the details of bit fields.
IPC_STRUCT5_LOCK_STATUS	0x402200BC	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT6_ACQUIRE	0x402200C0	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT6_RELEASE	0x402200C4	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT6_NOTIFY	0x402200C8	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT6_DATA0	0x402200CC	IPC data 0. See IPC_STRUCT0_DATA0 for the details of bit fields.
IPC_STRUCT6_DATA1	0x402200D0	IPC data 1. See IPC_STRUCT0_DATA1 for the details of bit fields.
IPC_STRUCT6_LOCK_STATUS	0x402200DC	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT7_ACQUIRE	0x402200E0	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT7_RELEASE	0x402200E4	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT7_NOTIFY	0x402200E8	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.

Register name	Address	Description
IPC_STRUCT7_DATA0	0x402200EC	IPC data 0. See IPC_STRUCT0_DATA0 for the details of bit fields.
IPC_STRUCT7_DATA1	0x402200F0	IPC data 1. See IPC_STRUCT0_DATA1 for the details of bit fields.
IPC_STRUCT7_LOCK_STATUS	0x402200FC	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_INTR_STRUCT0_INTR	0x40221000	Interrupt
IPC_INTR_STRUCT0_INTR_SET	0x40221004	Interrupt set
IPC_INTR_STRUCT0_INTR_MASK	0x40221008	Interrupt mask
IPC_INTR_STRUCT0_INTR_MASKED	0x4022100C	Interrupt masked
IPC_INTR_STRUCT1_INTR	0x40221020	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT1_INTR_SET	0x40221024	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT1_INTR_MASK	0x40221028	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT1_INTR_MASKED	0x4022102C	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT2_INTR	0x40221040	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT2_INTR_SET	0x40221044	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT2_INTR_MASK	0x40221048	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT2_INTR_MASKED	0x4022104C	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT3_INTR	0x40221060	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT3_INTR_SET	0x40221064	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT3_INTR_MASK	0x40221068	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT3_INTR_MASKED	0x4022106C	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT4_INTR	0x40221080	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT4_INTR_SET	0x40221084	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT4_INTR_MASK	0x40221088	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.

Register name	Address	Description
IPC_INTR_STRUCT4_INTR_MASKED	0x4022108C	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT5_INTR	0x402210A0	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT5_INTR_SET	0x402210A4	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT5_INTR_MASK	0x402210A8	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT5_INTR_MASKED	0x402210AC	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT6_INTR	0x402210C0	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT6_INTR_SET	0x402210C4	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT6_INTR_MASK	0x402210C8	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT6_INTR_MASKED	0x402210CC	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT7_INTR	0x402210E0	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT7_INTR_SET	0x402210E4	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT7_INTR_MASK	0x402210E8	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT7_INTR_MASKED	0x402210EC	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.

2.1 IPC registers

IPC_STRUCT0_ACQUIRE

IPC acquire
Address: 0x40220000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None		R	R
HW Access	W				None		W	W
Name	PC [7:4]				None [3:2]		NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			

Bits	15	14	13	12	11	10	9	8
Name	None [15:12]				MS [11:8]			
Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	R	None						
HW Access	RW	None						
Name	SUCCESS	None [30:24]						

Bits	Name	Description
31	SUCCESS	Specifies if the lock is successfully acquired or not (reading the ACQUIRE register can have affect on SUCCESS and LOCK_STATUS.ACQUIRED): '0': Not successfully acquired; i.e. the lock was already acquired by another read transaction and not released. The P, NS, PC and MS fields reflect the access attributes of the transaction that previously successfully acuired the lock; the fields are NOT affected by the current access. '1': Successfully acquired. The P, NS, PC and MS fields reflect the access attributes of the current access. Note that this field is NOT SW writable. A lock is released by writing to the associated RELEASE register (irrespective of the write value). Default Value: 0
11 : 8	MS	This field specifies the bus master identifier that successfully acquired the lock. Default Value: Undefined
7 : 4	PC	This field specifies the protection context that successfully acquired the lock. Default Value: Undefined
1	NS	Secure/non-secure access control: '0': secure. '1': non-secure. This field is set with the secure/non-secure access control of the access that successfully acquired the lock. Default Value: Undefined

0	P	User/privileged access control: '0': user mode. '1': privileged mode. This field is set with the user/ privileged access control of the access that successfully acquired the lock. Default Value: Undefined

IPC_STRUCT0_RELEASE

IPC release
Address: 0x40220004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access								
Name	INTR_RELEASE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	INTR_RELEASE	Writing this field releases a lock and allows for the generation of release events to the IPC interrupt structures, but only when the lock is acquired (LOCK_STATUS.ACQUIRED is '1'). The IPC release cause fields associated with this IPC structure are set to '1', but only for those IPC interrupt structures for which the corresponding bit field in INTR_RELEASE[] is set to '1'. SW writes a '1' to the bit fields to generate a release event. Due to the transient nature of this event, SW always reads a '0' from this field. Default Value: 0

IPC_STRUCT0_NOTIFY

IPC notification
Address: 0x40220008
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access								
Name	INTR_NOTIFY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	INTR_NOTIFY	This field allows for the generation of notification events to the IPC interrupt structures. The IPC notification cause fields associated with this IPC structure are set to '1', but only for those IPC interrupt structures for which the corresponding bit field in INTR_NOTIFY[] is set to '1'. SW writes a '1' to the bit fields to generate a notify event. Due to the transient nature of this event, SW always reads a '0' from this field. Default Value: 0

IPC_STRUCT0_DATA0

IPC data 0
Address: 0x4022000C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	This field holds a 32-bit data element that is associated with the IPC structure. Default Value: Undefined

IPC_STRUCT0_DATA1

IPC data 1
Address: 0x40220010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	This field holds a 32-bit data element that is associated with the IPC structure. Default Value: Undefined

IPC_STRUCT0_LOCK_STATUS

IPC lock status
Address: 0x4022001C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None		R	R
HW Access	W				None		W	W
Name	PC [7:4]				None [3:2]		NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				MS [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	R	None						
Name	ACQUIRED	None [30:24]						

Bits	Name	Description
31	ACQUIRED	Specifies if the lock is acquired. This field is set to '1', if a ACQUIRE read transfer successfully acquires the lock (the ACQUIRE read transfer returns ACQUIRE.SUCCESS as '1'). If zero, P, NS, PC, and MS are not valid. Default Value: 0
11 : 8	MS	This field specifies the bus master identifier that successfully acquired the lock. Default Value: Undefined
7 : 4	PC	This field specifies the protection context that successfully acquired the lock. Default Value: Undefined
1	NS	This field specifies the secure/non-secure access control: '0': secure. '1': non-secure. Default Value: Undefined
0	P	This field specifies the user/ privileged access control: '0': user mode. '1': privileged mode. Default Value: Undefined

IPC_INTR_STRUCT0_INTR

Interrupt
Address: 0x40221000
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	RELEASE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	RW1S							
Name	NOTIFY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	NOTIFY	These interrupt cause fields are activated (HW sets the field to '1') when a IPC notification event is detected. One bit field for each master. SW writes a '1' to these field to clear the interrupt cause. Default Value: 0
7 : 0	RELEASE	These interrupt cause fields are activated (HW sets the field to '1') when a IPC release event is detected. One bit field for each master. SW writes a '1' to these field to clear the interrupt cause. Default Value: 0

IPC_INTR_STRUCT0_INTR_SET

Interrupt set
Address: 0x40221004
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	RELEASE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	A							
Name	NOTIFY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	NOTIFY	SW writes a '1' to this field to set the corresponding field in the INTR register. Default Value: 0
7 : 0	RELEASE	SW writes a '1' to this field to set the corresponding field in the INTR register. Default Value: 0

IPC_INTR_STRUCT0_INTR_MASK

Interrupt mask
Address: 0x40221008
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RELEASE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	NOTIFY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	NOTIFY	Mask bit for corresponding field in the INTR register. Default Value: 0
7 : 0	RELEASE	Mask bit for corresponding field in the INTR register. Default Value: 0

IPC_INTR_STRUCT0_INTR_MASKED

Interrupt masked
Address: 0x4022100C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RELEASE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	NOTIFY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	NOTIFY	Logical and of corresponding INTR and INTR_MASK fields. Default Value: 0
7 : 0	RELEASE	Logical and of corresponding request and mask bits. Default Value: 0

3 Protection unit

Register details

Register name	Address	Description
PROT_SMPU_MS0_CTL	0x40230000	Master 0 protection context control
PROT_SMPU_MS1_CTL	0x40230004	Master 1 protection context control
PROT_SMPU_MS2_CTL	0x40230008	Master 2 protection context control
PROT_SMPU_MS3_CTL	0x4023000C	Master 3 protection context control
PROT_SMPU_MS4_CTL	0x40230010	Master 4 protection context control
PROT_SMPU_MS14_CTL	0x40230038	Master 14 protection context control
PROT_SMPU_MS15_CTL	0x4023003C	Master 15 protection context control
PROT_SMPU_SMPU_STRUCT0_ADDR0	0x40232000	SMPU region address 0 (slave structure)
PROT_SMPU_SMPU_STRUCT0_ATT0	0x40232004	SMPU region attributes 0 (slave structure)
PROT_SMPU_SMPU_STRUCT0_ADDR1	0x40232020	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT0_ATT1	0x40232024	SMPU region attributes 1 (master structure)
PROT_SMPU_SMPU_STRUCT1_ADDR0	0x40232040	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT1_ATT0	0x40232044	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT1_ADDR1	0x40232060	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT1_ATT1	0x40232064	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT2_ADDR0	0x40232080	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT2_ATT0	0x40232084	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT2_ADDR1	0x402320A0	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT2_ATT1	0x402320A4	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT3_ADDR0	0x402320C0	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.

Register name	Address	Description
PROT_SMPU_SMPU_STRUCT3_ATT0	0x402320C4	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT3_ADDR1	0x402320E0	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT3_ATT1	0x402320E4	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT4_ADDR0	0x40232100	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT4_ATT0	0x40232104	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT4_ADDR1	0x40232120	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT4_ATT1	0x40232124	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT5_ADDR0	0x40232140	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT5_ATT0	0x40232144	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT5_ADDR1	0x40232160	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT5_ATT1	0x40232164	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT6_ADDR0	0x40232180	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT6_ATT0	0x40232184	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT6_ADDR1	0x402321A0	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT6_ATT1	0x402321A4	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT7_ADDR0	0x402321C0	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT7_ATT0	0x402321C4	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.

Register name	Address	Description
PROT_SMPU_SMPU_STRUCT7_ADDR1	0x402321E0	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT7_ATT1	0x402321E4	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT8_ADDR0	0x40232200	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT8_ATT0	0x40232204	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT8_ADDR1	0x40232220	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT8_ATT1	0x40232224	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT9_ADDR0	0x40232240	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT9_ATT0	0x40232244	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT9_ADDR1	0x40232260	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT9_ATT1	0x40232264	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT10_ADDR0	0x40232280	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT10_ATT0	0x40232284	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT10_ADDR1	0x402322A0	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT10_ATT1	0x402322A4	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT11_ADDR0	0x402322C0	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT11_ATT0	0x402322C4	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT11_ADDR1	0x402322E0	SMPU region address 1 (master structure)

Register name	Address	Description
PROT_SMPU_SMPU_STRUCT11_ATT1	0x402322E4	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT12_ADDR0	0x40232300	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT12_ATT0	0x40232304	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT12_ADDR1	0x40232320	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT12_ATT1	0x40232324	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT13_ADDR0	0x40232340	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT13_ATT0	0x40232344	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT13_ADDR1	0x40232360	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT13_ATT1	0x40232364	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT14_ADDR0	0x40232380	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT14_ATT0	0x40232384	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT14_ADDR1	0x402323A0	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT14_ATT1	0x402323A4	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT15_ADDR0	0x402323C0	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT15_ATT0	0x402323C4	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT15_ADDR1	0x402323E0	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT15_ATT1	0x402323E4	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_MPU0_MS_CTL	0x40234000	Master control

Register name	Address	Description
PROT_MPU0_MS_CTL_READ_MIR0	0x40234004	Master control read mirror. This is the starting address of a register bank containing 127 registers (PROT_MPU0_MS_CTL_READ_MIR0 to PROT_MPU0_MS_CTL_READ_MIR126).
PROT_MPU14_MS_CTL	0x40237800	Master control
PROT_MPU14_MS_CTL_READ_MIR0	0x40237804	Master control read mirror. This is the starting address of a register bank containing 127 registers (PROT_MPU14_MS_CTL_READ_MIR0 to PROT_MPU14_MS_CTL_READ_MIR126).
PROT_MPU15_MS_CTL	0x40237C00	Master control. See PROT_MPU14_MS_CTL for the details of bit fields.
PROT_MPU15_MS_CTL_READ_MIR0	0x40237C04	Master control read mirror. This is the starting address of a register bank containing 127 registers (PROT_MPU15_MS_CTL_READ_MIR0 to PROT_MPU15_MS_CTL_READ_MIR126). See PROT_MPU14_MS_CTL_READ_MIR0 for the details of bit fields.
PROT_MPU15_MPU_STRUCT0_ADDR	0x40237E00	MPU region address
PROT_MPU15_MPU_STRUCT0_ATT	0x40237E04	MPU region attrributes
PROT_MPU15_MPU_STRUCT1_ADDR	0x40237E20	MPU region address. See PROT_MPU15_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU15_MPU_STRUCT1_ATT	0x40237E24	MPU region attrributes. See PROT_MPU15_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU15_MPU_STRUCT2_ADDR	0x40237E40	MPU region address. See PROT_MPU15_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU15_MPU_STRUCT2_ATT	0x40237E44	MPU region attrributes. See PROT_MPU15_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU15_MPU_STRUCT3_ADDR	0x40237E60	MPU region address. See PROT_MPU15_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU15_MPU_STRUCT3_ATT	0x40237E64	MPU region attrributes. See PROT_MPU15_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU15_MPU_STRUCT4_ADDR	0x40237E80	MPU region address. See PROT_MPU15_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU15_MPU_STRUCT4_ATT	0x40237E84	MPU region attrributes. See PROT_MPU15_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU15_MPU_STRUCT5_ADDR	0x40237EA0	MPU region address. See PROT_MPU15_MPU_STRUCT0_ADDR for the details of bit fields.

Register name	Address	Description
PROT_MPU15_MPU_STRUCT5_ATT	0x40237EA4	MPU region attrributes. See PROT_MPU15_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU15_MPU_STRUCT6_ADDR	0x40237EC0	MPU region address. See PROT_MPU15_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU15_MPU_STRUCT6_ATT	0x40237EC4	MPU region attrributes. See PROT_MPU15_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU15_MPU_STRUCT7_ADDR	0x40237EE0	MPU region address. See PROT_MPU15_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU15_MPU_STRUCT7_ATT	0x40237EE4	MPU region attrributes. See PROT_MPU15_MPU_STRUCT0_ATT for the details of bit fields.

3.1 Protection unit registers

PROT_SMPU_MS0_CTL

Master 0 protection context control
Address: 0x40230000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [23:17]							PC_MASK_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

23 : 17	PC_MASK_15_TO_1	Protection context mask for protection contexts "15" down to "1". Bit PC_MASK_15_TO_1[i] indicates if the MPU MS_CTL.PC[3:0] protection context field can be set to the value "i+1": - PC_MASK_15_TO_1[i] is '0': MPU MS_CTL.PC[3:0] can NOT be set to "i+1"; and PC[3:0] is not changed. If the protection context of the write transfer is "0", protection is not applied and PC[3:0] can be changed. - PC_MASK_15_TO_1[i] is '1': MPU MS_CTL.PC[3:0] can be set to "i+1". Note: When CPUSS_CM0_PC_CTL.VALID[i] is '1' (the associated protection context handler is valid), write transfers to PC_MASK_15_TO_1[i-1] always write '0', regardless of data written. This ensures that when valid protection context handlers are used to enter protection contexts 1, 2 or 3 through (HW modifies MPU MS_CTL.PC[3:0] on entry of the handler), it is NOT possible for SW to enter those protection contexts (SW modifies MPU MS_CTL.PC[3:0]). Default Value: 0
16	PC_MASK_0	Protection context mask for protection context "0". This field is a constant '0': - PC_MASK_0 is '0': MPU MS_CTL.PC[3:0] can NOT be set to "0" and PC[3:0] is not changed. If the protection context of the write transfer is "0", protection is not applied and PC[3:0] can be changed. Default Value: 0
9 : 8	PRIO	Device wide bus arbitration priority setting ("0": highest priority, "3": lowest priority). Notes: The AHB-Lite interconnect performs arbitration on the individual beats/transfers of a burst (this optimizes latency over locality/bandwidth). The AXI-Lite interconnects performs a single arbitration for the complete burst (this optimizes locality/bandwidth over latency). Masters with the same priority setting form a "priority group". Within a "priority group", round robin arbitration is performed. Default Value: 3

1	NS	Security setting ('0': secure mode; '1': non-secure mode). Notes: This field is ONLY used for masters that do NOT provide their own secure/non-secure access control attribute. Note that the default/ reset field value provides non-secure mode access capabilities to all masters. Default Value: 1
0	P	Privileged setting ('0': user mode; '1': privileged mode). Notes: This field is ONLY used for masters that do NOT provide their own user/ privileged access control attribute. The default/reset field value provides privileged mode access capabilities. Default Value: 1

PROT_SMPU_MS1_CTL

Master 1 protection context control
Address: 0x40230004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							R
Name	None [23:17]							PC_MASK_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	PC_MASK_0	See MS0_CTL.PC_MASK_0. Default Value: 0
9 : 8	PRIO	See MS0_CTL.PRIO Default Value: 3

PROT_SMPU_MS2_CTL

Master 2 protection context control
Address: 0x40230008
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							R
Name	None [23:17]							PC_MASK_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	PC_MASK_0	See MS0_CTL.PC_MASK_0. Default Value: 0
9 : 8	PRIO	See MS0_CTL.PRIO Default Value: 3

PROT_SMPU_MS3_CTL

Master 3 protection context control
Address: 0x4023000C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							R
Name	None [23:17]							PC_MASK_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	PC_MASK_0	See MS0_CTL.PC_MASK_0. Default Value: 0
9 : 8	PRIO	See MS0_CTL.PRIO Default Value: 3

PROT_SMPU_MS4_CTL

Master 4 protection context control
Address: 0x40230010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							R
Name	None [23:17]							PC_MASK_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	PC_MASK_0	See MS0_CTL.PC_MASK_0. Default Value: 0
9 : 8	PRIO	See MS0_CTL.PRIO Default Value: 3

PROT_SMPU_MS14_CTL

Master 14 protection context control
Address: 0x40230038
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [23:17]							PC_MASK_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 17	PC_MASK_15_TO_1	See MS0_CTL.PC_MASK_15_TO_1. Default Value: 0
16	PC_MASK_0	See MS0_CTL.PC_MASK_0. Default Value: 0
9 : 8	PRIO	See MS0_CTL.PRIO Default Value: 3
1	NS	See MS0_CTL.NS. Default Value: 1
0	P	See MS0_CTL.P. Default Value: 1

PROT_SMPU_MS15_CTL

Master 15 protection context control
Address: 0x4023003C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [23:17]							PC_MASK_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 17	PC_MASK_15_TO_1	See MS0_CTL.PC_MASK_15_TO_1. Default Value: 0
16	PC_MASK_0	See MS0_CTL.PC_MASK_0. Default Value: 0
9 : 8	PRIO	See MS0_CTL.PRIO Default Value: 3
1	NS	See MS0_CTL.NS. Default Value: 1
0	P	See MS0_CTL.P. Default Value: 1

PROT_SMPU_SMPU_STRUCT0_ADDR0

SMPU region address 0 (slave structure)
Address: 0x40232000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. The region size is defined by ATT0.REGION_SIZE. A region of n Byte is always n Byte aligned. As a result, some of the lesser significant address bits of ADDR24 may be ignored in determining whether a bus transfer address is within an address region. E.g., a 64 KByte address region (REGION_SIZE is "15") is 64 KByte aligned, and ADDR24[7:0] are ignored. Default Value: Undefined

7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. E.g., a 64 KByte address region (ATT0.REGION_SIZE is "15") has eight 8 KByte subregions. The access control as defined by ATT0 applies if the bus transfer address is within the address region AND the addressed subregion is NOT disabled. Note that the smallest region size is 256 B and the smallest subregion size is 32 B. Default Value: Undefined

PROT_SMPU_SMPU_STRUCT0_ATT0

SMPU region attributes 0 (slave structure)
Address: 0x40232004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	RW	RW	RW	RW
HW Access	None	R	R	R	R	R	R	R
Name	None	NS	PX	PW	PR	UX	UW	UR

Bits	15	14	13	12	11	10	9	8
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [15:9]							PC_MASK_0

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	RW				
HW Access	R	R	None	R				
Name	ENABLED	PC_MATCH	None	REGION_SIZE [28:24]				

Bits	Name	Description
31	ENABLED	Region enable: '0': Disabled. A disabled region will never result in a match on the bus transfer address. '1': Enabled. Note: a disabled address region performs logic gating to reduce dynamic power consumption. Default Value: 0

30	PC_MATCH	This field specifies if the PC field participates in the "matching" process or the "access evaluation" process: '0': PC field participates in "access evaluation". '1': PC field participates in "matching". "Matching" process. For each protection structure, the process identifies if a transfer address is contained within the address range. This identifies the "matching" regions. "Access evaluation" process. For each protection structure, the process evaluates the bus transfer access attributes against the access control attributes. Note that it is possible to define different access control for multiple protection contexts by using multiple protection structures with the same address region and PC_MATCH set to '1'. Default Value: Undefined
28 : 24	REGION_SIZE	This field specifies the region size: "0"-"6": Undefined. "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "39": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: Undefined
15 : 9	PC_MASK_15_TO_1	This field specifies protection context identifier based access control. Bit i: protection context i+1 enable. If '0', protection context i+1 access is disabled; i.e. not allowed. If '1', protection context i+1 access is enabled; i.e. allowed. Default Value: Undefined
8	PC_MASK_0	This field specifies protection context identifier based access control for protection context "0". Default Value: 1

6	NS	Non-secure: '0': Secure (secure accesses allowed, non-secure access NOT allowed). '1': Non-secure (both secure and non-secure accesses allowed). Default Value: Undefined
5	PX	Privileged execute enable: '0': Disabled (privileged, execute accesses are NOT allowed). '1': Enabled (privileged, execute accesses are allowed). Default Value: Undefined
4	PW	Privileged write enable: '0': Disabled (privileged, write accesses are NOT allowed). '1': Enabled (privileged, write accesses are allowed). Default Value: Undefined
3	PR	Privileged read enable: '0': Disabled (privileged, read accesses are NOT allowed). '1': Enabled (privileged, read accesses are allowed). Default Value: Undefined
2	UX	User execute enable: '0': Disabled (user, execute accesses are NOT allowed). '1': Enabled (user, execute accesses are allowed). Default Value: Undefined
1	UW	User write enable: '0': Disabled (user, write accesses are NOT allowed). '1': Enabled (user, write accesses are allowed). Default Value: Undefined
0	UR	User read enable: '0': Disabled (user, read accesses are NOT allowed). '1': Enabled (user, read accesses are allowed). Default Value: Undefined

PROT_SMPU_SMPU_STRUCT0_ADDR1

SMPU region address 1 (master structure)
Address: 0x40232020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203296
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

PROT_SMPU_SMPU_STRUCT0_ATT1

SMPU region attributes 1 (master structure)
Address: 0x40232024
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	R	RW	R	R	RW	R
HW Access	None	R	R	R	R	R	R	R
Name	None	NS	PX	PW	PR	UX	UW	UR

Bits	15	14	13	12	11	10	9	8
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [15:9]							PC_MASK_0

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	R				
HW Access	R	R	None	R				
Name	ENABLED	PC_MATCH	None	REGION_SIZE [28:24]				

Bits	Name	Description
31	ENABLED	Region enable: '0': Disabled. A disabled region will never result in a match on the bus transfer address. '1': Enabled. Default Value: 0

30	PC_MATCH	This field specifies if the PC field participates in the "matching" process or the "access evaluation" process: '0': PC field participates in "access evaluation". '1': PC field participates in "matching". "Matching" process. For each protection structure, the process identifies if a transfer address is contained within the address range. This identifies the "matching" regions. "Access evaluation" process. For each protection structure, the process evaluates the bus transfer access attributes against the access control attributes. Note that it is possible to define different access control for multiple protection contexts by using multiple protection structures with the same address region and PC_MATCH set to '1'. Default Value: Undefined
28 : 24	REGION_SIZE	This field specifies the region size: "7": 256 B region (8 32 B subregions) Note: this field is read-only. Default Value: 0x07
15 : 9	PC_MASK_15_TO_1	This field specifies protection context identifier based access control. Bit i: protection context i+1 enable. If '0', protection context i+1 access is disabled; i.e. not allowed. If '1', protection context i+1 access is enabled; i.e. allowed. Default Value: Undefined
8	PC_MASK_0	This field specifies protection context identifier based access control for protection context "0". Default Value: 1
6	NS	Non-secure: '0': Secure (secure accesses allowed, non-secure access NOT allowed). '1': Non-secure (both secure and non-secure accesses allowed). Default Value: Undefined
5	PX	Privileged execute enable: '0': Disabled (privileged, execute accesses are NOT allowed). '1': Enabled (privileged, execute accesses are allowed). Note that this register is constant '0'; i.e. privileged execute accesses are NEVER allowed. Default Value: 0

4	PW	Privileged write enable: '0': Disabled (privileged, write accesses are NOT allowed). '1': Enabled (privileged, write accesses are allowed). Default Value: Undefined
3	PR	Privileged read enable: '0': Disabled (privileged, read accesses are NOT allowed). '1': Enabled (privileged, read accesses are allowed). Note that this register is constant '1'; i.e. privileged read accesses are ALWAYS allowed. Default Value: 1
2	UX	User execute enable: '0': Disabled (user, execute accesses are NOT allowed). '1': Enabled (user, execute accesses are allowed). Note that this register is constant '0'; i.e. user execute accesses are NEVER allowed. Default Value: 0
1	UW	User write enable: '0': Disabled (user, write accesses are NOT allowed). '1': Enabled (user, write accesses are allowed). Default Value: Undefined
0	UR	User read enable: '0': Disabled (user, read accesses are NOT allowed). '1': Enabled (user, read accesses are allowed). Note that this register is constant '1'; i.e. user read accesses are ALWAYS allowed. Default Value: 1

PROT_SMPU_SMPU_STRUCT1_ADDR1

SMPU region address 1 (master structure)
Address: 0x40232060
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203296
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

PROT_SMPU_SMPU_STRUCT2_ADDR1

SMPU region address 1 (master structure)
Address: 0x402320A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203296
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

PROT_SMPU_SMPU_STRUCT3_ADDR1

SMPU region address 1 (master structure)
Address: 0x402320E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203296
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

PROT_SMPU_SMPU_STRUCT4_ADDR1

SMPU region address 1 (master structure)
Address: 0x40232120
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203297
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

PROT_SMPU_SMPU_STRUCT5_ADDR1

SMPU region address 1 (master structure)
Address: 0x40232160
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203297
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

PROT_SMPU_SMPU_STRUCT6_ADDR1

SMPU region address 1 (master structure)
Address: 0x402321A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203297
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

PROT_SMPU_SMPU_STRUCT7_ADDR1

SMPU region address 1 (master structure)
Address: 0x402321E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203297
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

PROT_SMPU_SMPU_STRUCT8_ADDR1

SMPU region address 1 (master structure)
Address: 0x40232220
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203298
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

PROT_SMPU_SMPU_STRUCT9_ADDR1

SMPU region address 1 (master structure)
Address: 0x40232260
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203298
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

PROT_SMPU_SMPU_STRUCT10_ADDR1

SMPU region address 1 (master structure)
Address: 0x402322A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203298
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

PROT_SMPU_SMPU_STRUCT11_ADDR1

SMPU region address 1 (master structure)
Address: 0x402322E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203298
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

PROT_SMPU_SMPU_STRUCT12_ADDR1

SMPU region address 1 (master structure)
Address: 0x40232320
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203299
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

PROT_SMPU_SMPU_STRUCT13_ADDR1

SMPU region address 1 (master structure)
Address: 0x40232360
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203299
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

PROT_SMPU_SMPU_STRUCT14_ADDR1

SMPU region address 1 (master structure)
Address: 0x402323A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203299
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

PROT_SMPU_SMPU_STRUCT15_ADDR1

SMPU region address 1 (master structure)
Address: 0x402323E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203299
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

PROT_MPU0_MS_CTL

Master control
Address: 0x40234000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				RW			
Name	None [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				RW			
Name	None [23:20]				PC_SAVED [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	PC_SAVED	Saved protection context. Modifications to this field are constrained by the associated SMPU MS_CTL.PC_MASK_0 and MS_CTL.PC_MASK_15_TO_1[] fields. Note: this field is ONLY used by the CM0+. Default Value: 0

3 : 0	PC	Active protection context (PC). Modifications to this field are constrained by the associated SMPU MS_CTL.PC_MASK_0 and MS_CTL.PC_MASK_15_TO_1[] fields. In addition, a write transfer with protection context "0" can change this field (protection context 0 has unrestricted access). The CM0+ MPU MS_CTL register is special: the PC field is modifiable by BOTH HW and SW (for all other masters, the MPU MS_CTL.PC field is modifiable by SW ONLY. For CM0+ PC field HW modifications, the following holds: * On entry of a CM0_PC0/1/2/3_HANDLER exception/interrupt handler: IF (the new PC is the same as MS_CTL.PC) PC is not affected; PC_SAVED is not affected. ELSE IF (CM0_PC_CTL.VALID[MS_CTL.PC]) An AHB-Lite bus error is generated for the exception handler fetch; PC is not affected; PC_SAVED is not affected. ELSE PC = "new PC"; PC_SAVED = PC (push operation). * On entry of any other exception/interrupt handler: PC = PC_SAVED; PC_SAVED is not affected (pop operation). Note that the CM0_PC0/1/2/3_HANDLER and CM0_PC_CTL registers are part of repecitve CPUSS MMIO registers. Note: this field is NOT used by the DW controllers, DMA controller, AXI DMA controller, CRYPTO component and VIDEOSS. Default Value: 0

PROT_MPU0_MS_CTL_READ_MIR0

Master control read mirror
Address: 0x40234004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				PC_SAVED [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	PC_SAVED	Read-only mirror of MS_CTL.PC_SAVED Default Value: 0
3 : 0	PC	Read-only mirror of MS_CTL.PC Default Value: 0

PROT_MPU14_MS_CTL

Master control
Address: 0x40237800
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				RW			
Name	None [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

3 : 0	PC	Active protection context (PC). Modifications to this field are constrained by the associated SMPU MS_CTL.PC_MASK_0 and MS_CTL.PC_MASK_15_TO_1[] fields. In addition, a write transfer with protection context "0" can change this field (protection context 0 has unrestricted access). The CM0+ MPU MS_CTL register is special: the PC field is modifiable by BOTH HW and SW (for all other masters, the MPU MS_CTL.PC field is modifiable by SW ONLY. For CM0+ PC field HW modifications, the following holds: * On entry of a CM0_PC0/1/2/3_HANDLER exception/interrupt handler: IF (the new PC is the same as MS_CTL.PC) PC is not affected; PC_SAVED is not affected. ELSE IF (CM0_PC_CTL.VALID[MS_CTL.PC]) An AHB-Lite bus error is generated for the exception handler fetch; PC is not affected; PC_SAVED is not affected. ELSE PC = "new PC"; PC_SAVED = PC (push operation). * On entry of any other exception/interrupt handler: PC = PC_SAVED; PC_SAVED is not affected (pop operation). Note that the CM0_PC0/1/2/3_HANDLER and CM0_PC_CTL registers are part of repecitve CPUSS MMIO registers. Note: this field is NOT used by the DW controllers, DMA controller, AXI DMA controller, CRYPTO component and VIDEOSS. Default Value: 0

PROT_MPU14_MS_CTL_READ_MIR0

Master control read mirror
Address: 0x40237804
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	PC	Read-only mirror of MS_CTL.PC Default Value: 0

PROT_MPU15_MPU_STRUCT0_ADDR

MPU region address
Address: 0x40237E00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. The region size is defined by ATT.REGION_SIZE. A region of n Byte is always n Byte aligned. As a result, some of the lesser significant address bits of ADDR24 may be ignored in determining whether a bus transfer address is within an address region. E.g., a 64 KByte address region (REGION_SIZE is "15") is 64 KByte aligned, and ADDR24[7:0] are ignored. Default Value: Undefined

7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. E.g., a 64 KByte address region (REGION_SIZE is "15") has eight 8 KByte subregions. The access control as defined by MPU_REGION_ATT applies if the bus transfer address is within the address region AND the addressed subregion is NOT disabled. Note that the smallest region size is 256 B and the smallest subregion size is 32 B. Default Value: Undefined

PROT_MPU15_MPU_STRUCT0_ATT

MPU region attrributes
Address: 0x40237E04
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	RW	RW	RW	RW
HW Access	None	R	R	R	R	R	R	R
Name	None	NS	PX	PW	PR	UX	UW	UR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None		RW				
HW Access	R	None		R				
Name	ENABLED	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	ENABLED	Region enable: '0': Disabled. A disabled region will never result in a match on the bus transfer address. '1': Enabled. Note: a disabled address region performs logic gating to reduce dynamic power consumption. Default Value: 0
28 : 24	REGION_SIZE	This field specifies the region size: "0"-"6": Undefined. "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "39": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: Undefined

6	NS	Non-secure: '0': Secure (secure accesses allowed, non-secure access NOT allowed). '1': Non-secure (both secure and non-secure accesses allowed). Default Value: Undefined
5	PX	Privileged execute enable: '0': Disabled (privileged, execute accesses are NOT allowed). '1': Enabled (privileged, execute accesses are allowed). Default Value: Undefined
4	PW	Privileged write enable: '0': Disabled (privileged, write accesses are NOT allowed). '1': Enabled (privileged, write accesses are allowed). Default Value: Undefined
3	PR	Privileged read enable: '0': Disabled (privileged, read accesses are NOT allowed). '1': Enabled (privileged, read accesses are allowed). Default Value: Undefined
2	UX	User execute enable: '0': Disabled (user, execute accesses are NOT allowed). '1': Enabled (user, execute accesses are allowed). Default Value: Undefined
1	UW	User write enable: '0': Disabled (user, write accesses are NOT allowed). '1': Enabled (user, write accesses are allowed). Default Value: Undefined
0	UR	User read enable: '0': Disabled (user, read accesses are NOT allowed). '1': Enabled (user, read accesses are allowed). Default Value: Undefined

4 Direct memory access (DMA)

Register details

Register name	Address	Description
DW0_CTL0	0x40280000	Control
DW0_STATUS0	0x40280004	Status
DW0_ACT_DESCR_CTL0	0x40280020	Active descriptor control
DW0_ACT_DESCR_SRC0	0x40280024	Active descriptor source
DW0_ACT_DESCR_DST0	0x40280028	Active descriptor destination
DW0_ACT_DESCR_X_CTL0	0x40280030	Active descriptor X loop control
DW0_ACT_DESCR_Y_CTL0	0x40280034	Active descriptor Y loop control
DW0_ACT_DESCR_NEXT_PTR0	0x40280038	Active descriptor next pointer
DW0_ACT_SRC0	0x40280040	Active source
DW0_ACT_DST0	0x40280044	Active destination
DW0_ECC_CTL0	0x40280080	ECC control
DW0_CRC_CTL0	0x40280100	CRC control
DW0_CRC_DATA_CTL0	0x40280110	CRC data control
DW0_CRC_POL_CTL0	0x40280120	CRC polynomial control
DW0_CRC_LFSR_CTL0	0x40280130	CRC LFSR control
DW0_CRC_REM_CTL0	0x40280140	CRC remainder control
DW0_CRC_REM_RESULT0	0x40280148	CRC remainder result
DW0_CH_STRUCT0_CH_CTL	0x40288000	Channel control
DW0_CH_STRUCT0_CH_STATUS	0x40288004	Channel status
DW0_CH_STRUCT0_CH_IDX	0x40288008	Channel current indices
DW0_CH_STRUCT0_CH_CURR_PTR	0x4028800C	Channel current descriptor pointer
DW0_CH_STRUCT0_INTR	0x40288010	Interrupt
DW0_CH_STRUCT0_INTR_SET	0x40288014	Interrupt set
DW0_CH_STRUCT0_INTR_MASK	0x40288018	Interrupt mask
DW0_CH_STRUCT0_INTR_MASKED	0x4028801C	Interrupt masked
DW0_CH_STRUCT0_SRAM_DATA0	0x40288020	SRAM data 0
DW0_CH_STRUCT0_SRAM_DATA1	0x40288024	SRAM data 1
DW0_CH_STRUCT0_TR_CMD	0x40288028	Channel software trigger
DW0_CH_STRUCT1_CH_CTL	0x40288040	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT1_CH_STATUS	0x40288044	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT1_CH_IDX	0x40288048	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT1_CH_CURR_PTR	0x4028804C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT1_INTR	0x40288050	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT1_INTR_SET	0x40288054	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT1_INTR_MASK	0x40288058	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT1_INTR_MASKED	0x4028805C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT1_SRAM_DATA0	0x40288060	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT1_SRAM_DATA1	0x40288064	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT1_TR_CMD	0x40288068	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT2_CH_CTL	0x40288080	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT2_CH_STATUS	0x40288084	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT2_CH_IDX	0x40288088	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT2_CH_CURR_PTR	0x4028808C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT2_INTR	0x40288090	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT2_INTR_SET	0x40288094	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT2_INTR_MASK	0x40288098	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT2_INTR_MASKED	0x4028809C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT2_SRAM_DATA0	0x402880A0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT2_SRAM_DATA1	0x402880A4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT2_TR_CMD	0x402880A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT3_CH_CTL	0x402880C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT3_CH_STATUS	0x402880C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT3_CH_IDX	0x402880C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT3_CH_CURR_PTR	0x402880CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT3_INTR	0x402880D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT3_INTR_SET	0x402880D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT3_INTR_MASK	0x402880D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT3_INTR_MASKED	0x402880DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT3_SRAM_DATA0	0x402880E0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT3_SRAM_DATA1	0x402880E4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT3_TR_CMD	0x402880E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT4_CH_CTL	0x40288100	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT4_CH_STATUS	0x40288104	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT4_CH_IDX	0x40288108	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT4_CH_CURR_PTR	0x4028810C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT4_INTR	0x40288110	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT4_INTR_SET	0x40288114	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT4_INTR_MASK	0x40288118	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT4_INTR_MASKED	0x4028811C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT4_SRAM_DATA0	0x40288120	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT4_SRAM_DATA1	0x40288124	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT4_TR_CMD	0x40288128	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT5_CH_CTL	0x40288140	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT5_CH_STATUS	0x40288144	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT5_CH_IDX	0x40288148	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT5_CH_CURR_PTR	0x4028814C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT5_INTR	0x40288150	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT5_INTR_SET	0x40288154	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT5_INTR_MASK	0x40288158	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT5_INTR_MASKED	0x4028815C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT5_SRAM_DATA0	0x40288160	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT5_SRAM_DATA1	0x40288164	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT5_TR_CMD	0x40288168	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT6_CH_CTL	0x40288180	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT6_CH_STATUS	0x40288184	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT6_CH_IDX	0x40288188	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT6_CH_CURR_PTR	0x4028818C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT6_INTR	0x40288190	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT6_INTR_SET	0x40288194	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT6_INTR_MASK	0x40288198	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT6_INTR_MASKED	0x4028819C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT6_SRAM_DATA0	0x402881A0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT6_SRAM_DATA1	0x402881A4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT6_TR_CMD	0x402881A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT7_CH_CTL	0x402881C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT7_CH_STATUS	0x402881C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT7_CH_IDX	0x402881C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT7_CH_CURR_PTR	0x402881CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT7_INTR	0x402881D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT7_INTR_SET	0x402881D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT7_INTR_MASK	0x402881D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT7_INTR_MASKED	0x402881DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT7_SRAM_DATA0	0x402881E0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT7_SRAM_DATA1	0x402881E4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT7_TR_CMD	0x402881E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT8_CH_CTL	0x40288200	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT8_CH_STATUS	0x40288204	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT8_CH_IDX	0x40288208	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT8_CH_CURR_PTR	0x4028820C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT8_INTR	0x40288210	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT8_INTR_SET	0x40288214	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT8_INTR_MASK	0x40288218	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT8_INTR_MASKED	0x4028821C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT8_SRAM_DATA0	0x40288220	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT8_SRAM_DATA1	0x40288224	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT8_TR_CMD	0x40288228	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT9_CH_CTL	0x40288240	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT9_CH_STATUS	0x40288244	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT9_CH_IDX	0x40288248	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT9_CH_CURR_PTR	0x4028824C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT9_INTR	0x40288250	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT9_INTR_SET	0x40288254	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT9_INTR_MASK	0x40288258	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT9_INTR_MASKED	0x4028825C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT9_SRAM_DATA0	0x40288260	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT9_SRAM_DATA1	0x40288264	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT9_TR_CMD	0x40288268	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT10_CH_CTL	0x40288280	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT10_CH_STATUS	0x40288284	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT10_CH_IDX	0x40288288	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT10_CH_CURR_PTR	0x4028828C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT10_INTR	0x40288290	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT10_INTR_SET	0x40288294	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT10_INTR_MASK	0x40288298	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT10_INTR_MASKED	0x4028829C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT10_SRAM_DATA0	0x402882A0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT10_SRAM_DATA1	0x402882A4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT10_TR_CMD	0x402882A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT11_CH_CTL	0x402882C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT11_CH_STATUS	0x402882C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT11_CH_IDX	0x402882C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT11_CH_CURR_PTR	0x402882CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT11_INTR	0x402882D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT11_INTR_SET	0x402882D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT11_INTR_MASK	0x402882D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT11_INTR_MASKED	0x402882DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT11_SRAM_DATA0	0x402882E0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT11_SRAM_DATA1	0x402882E4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT11_TR_CMD	0x402882E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT12_CH_CTL	0x40288300	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT12_CH_STATUS	0x40288304	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT12_CH_IDX	0x40288308	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT12_CH_CURR_PTR	0x4028830C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT12_INTR	0x40288310	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT12_INTR_SET	0x40288314	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT12_INTR_MASK	0x40288318	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT12_INTR_MASKED	0x4028831C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT12_SRAM_DATA0	0x40288320	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT12_SRAM_DATA1	0x40288324	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT12_TR_CMD	0x40288328	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT13_CH_CTL	0x40288340	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT13_CH_STATUS	0x40288344	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT13_CH_IDX	0x40288348	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT13_CH_CURR_PTR	0x4028834C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT13_INTR	0x40288350	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT13_INTR_SET	0x40288354	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT13_INTR_MASK	0x40288358	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT13_INTR_MASKED	0x4028835C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT13_SRAM_DATA0	0x40288360	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT13_SRAM_DATA1	0x40288364	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT13_TR_CMD	0x40288368	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT14_CH_CTL	0x40288380	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT14_CH_STATUS	0x40288384	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT14_CH_IDX	0x40288388	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT14_CH_CURR_PTR	0x4028838C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT14_INTR	0x40288390	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT14_INTR_SET	0x40288394	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT14_INTR_MASK	0x40288398	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT14_INTR_MASKED	0x4028839C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT14_SRAM_DATA0	0x402883A0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT14_SRAM_DATA1	0x402883A4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT14_TR_CMD	0x402883A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT15_CH_CTL	0x402883C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT15_CH_STATUS	0x402883C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT15_CH_IDX	0x402883C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT15_CH_CURR_PTR	0x402883CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT15_INTR	0x402883D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT15_INTR_SET	0x402883D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT15_INTR_MASK	0x402883D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT15_INTR_MASKED	0x402883DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT15_SRAM_DATA0	0x402883E0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT15_SRAM_DATA1	0x402883E4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT15_TR_CMD	0x402883E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT16_CH_CTL	0x40288400	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT16_CH_STATUS	0x40288404	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT16_CH_IDX	0x40288408	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT16_CH_CURR_PTR	0x4028840C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT16_INTR	0x40288410	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT16_INTR_SET	0x40288414	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT16_INTR_MASK	0x40288418	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT16_INTR_MASKED	0x4028841C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT16_SRAM_DATA0	0x40288420	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT16_SRAM_DATA1	0x40288424	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT16_TR_CMD	0x40288428	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT17_CH_CTL	0x40288440	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT17_CH_STATUS	0x40288444	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT17_CH_IDX	0x40288448	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT17_CH_CURR_PTR	0x4028844C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT17_INTR	0x40288450	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT17_INTR_SET	0x40288454	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT17_INTR_MASK	0x40288458	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT17_INTR_MASKED	0x4028845C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT17_SRAM_DATA0	0x40288460	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT17_SRAM_DATA1	0x40288464	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT17_TR_CMD	0x40288468	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT18_CH_CTL	0x40288480	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT18_CH_STATUS	0x40288484	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT18_CH_IDX	0x40288488	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT18_CH_CURR_PTR	0x4028848C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT18_INTR	0x40288490	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT18_INTR_SET	0x40288494	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT18_INTR_MASK	0x40288498	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT18_INTR_MASKED	0x4028849C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT18_SRAM_DATA0	0x402884A0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT18_SRAM_DATA1	0x402884A4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT18_TR_CMD	0x402884A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT19_CH_CTL	0x402884C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT19_CH_STATUS	0x402884C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT19_CH_IDX	0x402884C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT19_CH_CURR_PTR	0x402884CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT19_INTR	0x402884D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT19_INTR_SET	0x402884D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT19_INTR_MASK	0x402884D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT19_INTR_MASKED	0x402884DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT19_SRAM_DATA0	0x402884E0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT19_SRAM_DATA1	0x402884E4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT19_TR_CMD	0x402884E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT20_CH_CTL	0x40288500	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT20_CH_STATUS	0x40288504	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT20_CH_IDX	0x40288508	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT20_CH_CURR_PTR	0x4028850C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT20_INTR	0x40288510	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT20_INTR_SET	0x40288514	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT20_INTR_MASK	0x40288518	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT20_INTR_MASKED	0x4028851C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT20_SRAM_DATA0	0x40288520	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT20_SRAM_DATA1	0x40288524	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT20_TR_CMD	0x40288528	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT21_CH_CTL	0x40288540	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT21_CH_STATUS	0x40288544	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT21_CH_IDX	0x40288548	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT21_CH_CURR_PTR	0x4028854C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT21_INTR	0x40288550	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT21_INTR_SET	0x40288554	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT21_INTR_MASK	0x40288558	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT21_INTR_MASKED	0x4028855C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT21_SRAM_DATA0	0x40288560	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT21_SRAM_DATA1	0x40288564	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT21_TR_CMD	0x40288568	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT22_CH_CTL	0x40288580	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT22_CH_STATUS	0x40288584	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT22_CH_IDX	0x40288588	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT22_CH_CURR_PTR	0x4028858C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT22_INTR	0x40288590	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT22_INTR_SET	0x40288594	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT22_INTR_MASK	0x40288598	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT22_INTR_MASKED	0x4028859C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT22_SRAM_DATA0	0x402885A0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT22_SRAM_DATA1	0x402885A4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT22_TR_CMD	0x402885A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT23_CH_CTL	0x402885C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT23_CH_STATUS	0x402885C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT23_CH_IDX	0x402885C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT23_CH_CURR_PTR	0x402885CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT23_INTR	0x402885D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT23_INTR_SET	0x402885D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT23_INTR_MASK	0x402885D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT23_INTR_MASKED	0x402885DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT23_SRAM_DATA0	0x402885E0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT23_SRAM_DATA1	0x402885E4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT23_TR_CMD	0x402885E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT24_CH_CTL	0x40288600	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT24_CH_STATUS	0x40288604	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT24_CH_IDX	0x40288608	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT24_CH_CURR_PTR	0x4028860C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT24_INTR	0x40288610	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT24_INTR_SET	0x40288614	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT24_INTR_MASK	0x40288618	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT24_INTR_MASKED	0x4028861C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT24_SRAM_DATA0	0x40288620	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT24_SRAM_DATA1	0x40288624	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT24_TR_CMD	0x40288628	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT25_CH_CTL	0x40288640	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT25_CH_STATUS	0x40288644	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT25_CH_IDX	0x40288648	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT25_CH_CURR_PTR	0x4028864C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT25_INTR	0x40288650	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT25_INTR_SET	0x40288654	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT25_INTR_MASK	0x40288658	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT25_INTR_MASKED	0x4028865C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT25_SRAM_DATA0	0x40288660	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT25_SRAM_DATA1	0x40288664	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT25_TR_CMD	0x40288668	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT26_CH_CTL	0x40288680	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT26_CH_STATUS	0x40288684	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT26_CH_IDX	0x40288688	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT26_CH_CURR_PTR	0x4028868C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT26_INTR	0x40288690	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT26_INTR_SET	0x40288694	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT26_INTR_MASK	0x40288698	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT26_INTR_MASKED	0x4028869C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT26_SRAM_DATA0	0x402886A0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT26_SRAM_DATA1	0x402886A4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT26_TR_CMD	0x402886A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT27_CH_CTL	0x402886C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT27_CH_STATUS	0x402886C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT27_CH_IDX	0x402886C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT27_CH_CURR_PTR	0x402886CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT27_INTR	0x402886D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT27_INTR_SET	0x402886D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT27_INTR_MASK	0x402886D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT27_INTR_MASKED	0x402886DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT27_SRAM_DATA0	0x402886E0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT27_SRAM_DATA1	0x402886E4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT27_TR_CMD	0x402886E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT28_CH_CTL	0x40288700	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT28_CH_STATUS	0x40288704	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT28_CH_IDX	0x40288708	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT28_CH_CURR_PTR	0x4028870C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT28_INTR	0x40288710	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT28_INTR_SET	0x40288714	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT28_INTR_MASK	0x40288718	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT28_INTR_MASKED	0x4028871C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT28_SRAM_DATA0	0x40288720	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT28_SRAM_DATA1	0x40288724	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT28_TR_CMD	0x40288728	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT29_CH_CTL	0x40288740	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT29_CH_STATUS	0x40288744	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT29_CH_IDX	0x40288748	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT29_CH_CURR_PTR	0x4028874C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT29_INTR	0x40288750	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT29_INTR_SET	0x40288754	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT29_INTR_MASK	0x40288758	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT29_INTR_MASKED	0x4028875C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT29_SRAM_DATA0	0x40288760	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT29_SRAM_DATA1	0x40288764	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT29_TR_CMD	0x40288768	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT30_CH_CTL	0x40288780	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT30_CH_STATUS	0x40288784	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT30_CH_IDX	0x40288788	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT30_CH_CURR_PTR	0x4028878C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT30_INTR	0x40288790	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT30_INTR_SET	0x40288794	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT30_INTR_MASK	0x40288798	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT30_INTR_MASKED	0x4028879C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT30_SRAM_DATA0	0x402887A0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT30_SRAM_DATA1	0x402887A4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT30_TR_CMD	0x402887A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT31_CH_CTL	0x402887C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT31_CH_STATUS	0x402887C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT31_CH_IDX	0x402887C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT31_CH_CURR_PTR	0x402887CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT31_INTR	0x402887D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT31_INTR_SET	0x402887D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT31_INTR_MASK	0x402887D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT31_INTR_MASKED	0x402887DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT31_SRAM_DATA0	0x402887E0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT31_SRAM_DATA1	0x402887E4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT31_TR_CMD	0x402887E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT32_CH_CTL	0x40288800	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT32_CH_STATUS	0x40288804	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT32_CH_IDX	0x40288808	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT32_CH_CURR_PTR	0x4028880C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT32_INTR	0x40288810	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT32_INTR_SET	0x40288814	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT32_INTR_MASK	0x40288818	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT32_INTR_MASKED	0x4028881C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT32_SRAM_DATA0	0x40288820	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT32_SRAM_DATA1	0x40288824	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT32_TR_CMD	0x40288828	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT33_CH_CTL	0x40288840	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT33_CH_STATUS	0x40288844	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT33_CH_IDX	0x40288848	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT33_CH_CURR_PTR	0x4028884C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT33_INTR	0x40288850	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT33_INTR_SET	0x40288854	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT33_INTR_MASK	0x40288858	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT33_INTR_MASKED	0x4028885C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT33_SRAM_DATA0	0x40288860	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT33_SRAM_DATA1	0x40288864	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT33_TR_CMD	0x40288868	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT34_CH_CTL	0x40288880	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT34_CH_STATUS	0x40288884	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT34_CH_IDX	0x40288888	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT34_CH_CURR_PTR	0x4028888C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT34_INTR	0x40288890	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT34_INTR_SET	0x40288894	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT34_INTR_MASK	0x40288898	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT34_INTR_MASKED	0x4028889C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT34_SRAM_DATA0	0x402888A0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT34_SRAM_DATA1	0x402888A4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT34_TR_CMD	0x402888A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT35_CH_CTL	0x402888C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT35_CH_STATUS	0x402888C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT35_CH_IDX	0x402888C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT35_CH_CURR_PTR	0x402888CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT35_INTR	0x402888D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT35_INTR_SET	0x402888D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT35_INTR_MASK	0x402888D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT35_INTR_MASKED	0x402888DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT35_SRAM_DATA0	0x402888E0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT35_SRAM_DATA1	0x402888E4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT35_TR_CMD	0x402888E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT36_CH_CTL	0x40288900	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT36_CH_STATUS	0x40288904	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT36_CH_IDX	0x40288908	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT36_CH_CURR_PTR	0x4028890C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT36_INTR	0x40288910	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT36_INTR_SET	0x40288914	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT36_INTR_MASK	0x40288918	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT36_INTR_MASKED	0x4028891C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT36_SRAM_DATA0	0x40288920	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT36_SRAM_DATA1	0x40288924	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT36_TR_CMD	0x40288928	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT37_CH_CTL	0x40288940	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT37_CH_STATUS	0x40288944	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT37_CH_IDX	0x40288948	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT37_CH_CURR_PTR	0x4028894C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT37_INTR	0x40288950	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT37_INTR_SET	0x40288954	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT37_INTR_MASK	0x40288958	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT37_INTR_MASKED	0x4028895C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT37_SRAM_DATA0	0x40288960	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT37_SRAM_DATA1	0x40288964	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT37_TR_CMD	0x40288968	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT38_CH_CTL	0x40288980	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT38_CH_STATUS	0x40288984	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT38_CH_IDX	0x40288988	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT38_CH_CURR_PTR	0x4028898C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT38_INTR	0x40288990	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT38_INTR_SET	0x40288994	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT38_INTR_MASK	0x40288998	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT38_INTR_MASKED	0x4028899C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT38_SRAM_DATA0	0x402889A0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT38_SRAM_DATA1	0x402889A4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT38_TR_CMD	0x402889A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT39_CH_CTL	0x402889C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT39_CH_STATUS	0x402889C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT39_CH_IDX	0x402889C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT39_CH_CURR_PTR	0x402889CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT39_INTR	0x402889D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT39_INTR_SET	0x402889D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT39_INTR_MASK	0x402889D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT39_INTR_MASKED	0x402889DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT39_SRAM_DATA0	0x402889E0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT39_SRAM_DATA1	0x402889E4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT39_TR_CMD	0x402889E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT40_CH_CTL	0x40288A00	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT40_CH_STATUS	0x40288A04	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT40_CH_IDX	0x40288A08	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT40_CH_CURR_PTR	0x40288A0C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT40_INTR	0x40288A10	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT40_INTR_SET	0x40288A14	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT40_INTR_MASK	0x40288A18	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT40_INTR_MASKED	0x40288A1C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT40_SRAM_DATA0	0x40288A20	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT40_SRAM_DATA1	0x40288A24	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT40_TR_CMD	0x40288A28	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT41_CH_CTL	0x40288A40	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT41_CH_STATUS	0x40288A44	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT41_CH_IDX	0x40288A48	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT41_CH_CURR_PTR	0x40288A4C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT41_INTR	0x40288A50	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT41_INTR_SET	0x40288A54	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT41_INTR_MASK	0x40288A58	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT41_INTR_MASKED	0x40288A5C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT41_SRAM_DATA0	0x40288A60	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT41_SRAM_DATA1	0x40288A64	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT41_TR_CMD	0x40288A68	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT42_CH_CTL	0x40288A80	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT42_CH_STATUS	0x40288A84	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT42_CH_IDX	0x40288A88	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT42_CH_CURR_PTR	0x40288A8C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT42_INTR	0x40288A90	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT42_INTR_SET	0x40288A94	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT42_INTR_MASK	0x40288A98	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT42_INTR_MASKED	0x40288A9C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT42_SRAM_DATA0	0x40288AA0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT42_SRAM_DATA1	0x40288AA4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT42_TR_CMD	0x40288AA8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT43_CH_CTL	0x40288AC0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT43_CH_STATUS	0x40288AC4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT43_CH_IDX	0x40288AC8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT43_CH_CURR_PTR	0x40288ACC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT43_INTR	0x40288AD0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT43_INTR_SET	0x40288AD4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT43_INTR_MASK	0x40288AD8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT43_INTR_MASKED	0x40288ADC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT43_SRAM_DATA0	0x40288AE0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT43_SRAM_DATA1	0x40288AE4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT43_TR_CMD	0x40288AE8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT44_CH_CTL	0x40288B00	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT44_CH_STATUS	0x40288B04	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT44_CH_IDX	0x40288B08	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT44_CH_CURR_PTR	0x40288B0C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT44_INTR	0x40288B10	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT44_INTR_SET	0x40288B14	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT44_INTR_MASK	0x40288B18	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT44_INTR_MASKED	0x40288B1C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT44_SRAM_DATA0	0x40288B20	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT44_SRAM_DATA1	0x40288B24	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT44_TR_CMD	0x40288B28	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT45_CH_CTL	0x40288B40	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT45_CH_STATUS	0x40288B44	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT45_CH_IDX	0x40288B48	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT45_CH_CURR_PTR	0x40288B4C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT45_INTR	0x40288B50	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT45_INTR_SET	0x40288B54	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT45_INTR_MASK	0x40288B58	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT45_INTR_MASKED	0x40288B5C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT45_SRAM_DATA0	0x40288B60	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT45_SRAM_DATA1	0x40288B64	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT45_TR_CMD	0x40288B68	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT46_CH_CTL	0x40288B80	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT46_CH_STATUS	0x40288B84	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT46_CH_IDX	0x40288B88	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT46_CH_CURR_PTR	0x40288B8C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT46_INTR	0x40288B90	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT46_INTR_SET	0x40288B94	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT46_INTR_MASK	0x40288B98	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT46_INTR_MASKED	0x40288B9C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT46_SRAM_DATA0	0x40288BA0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT46_SRAM_DATA1	0x40288BA4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT46_TR_CMD	0x40288BA8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT47_CH_CTL	0x40288BC0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT47_CH_STATUS	0x40288BC4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT47_CH_IDX	0x40288BC8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT47_CH_CURR_PTR	0x40288BCC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT47_INTR	0x40288BD0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT47_INTR_SET	0x40288BD4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT47_INTR_MASK	0x40288BD8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT47_INTR_MASKED	0x40288BDC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT47_SRAM_DATA0	0x40288BE0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT47_SRAM_DATA1	0x40288BE4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT47_TR_CMD	0x40288BE8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT48_CH_CTL	0x40288C00	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT48_CH_STATUS	0x40288C04	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT48_CH_IDX	0x40288C08	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT48_CH_CURR_PTR	0x40288C0C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT48_INTR	0x40288C10	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT48_INTR_SET	0x40288C14	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT48_INTR_MASK	0x40288C18	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT48_INTR_MASKED	0x40288C1C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT48_SRAM_DATA0	0x40288C20	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT48_SRAM_DATA1	0x40288C24	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT48_TR_CMD	0x40288C28	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT49_CH_CTL	0x40288C40	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT49_CH_STATUS	0x40288C44	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT49_CH_IDX	0x40288C48	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT49_CH_CURR_PTR	0x40288C4C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT49_INTR	0x40288C50	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT49_INTR_SET	0x40288C54	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT49_INTR_MASK	0x40288C58	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT49_INTR_MASKED	0x40288C5C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT49_SRAM_DATA0	0x40288C60	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT49_SRAM_DATA1	0x40288C64	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT49_TR_CMD	0x40288C68	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT50_CH_CTL	0x40288C80	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT50_CH_STATUS	0x40288C84	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT50_CH_IDX	0x40288C88	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT50_CH_CURR_PTR	0x40288C8C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT50_INTR	0x40288C90	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT50_INTR_SET	0x40288C94	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT50_INTR_MASK	0x40288C98	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT50_INTR_MASKED	0x40288C9C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT50_SRAM_DATA0	0x40288CA0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT50_SRAM_DATA1	0x40288CA4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT50_TR_CMD	0x40288CA8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT51_CH_CTL	0x40288CC0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT51_CH_STATUS	0x40288CC4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT51_CH_IDX	0x40288CC8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT51_CH_CURR_PTR	0x40288CCC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT51_INTR	0x40288CD0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT51_INTR_SET	0x40288CD4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT51_INTR_MASK	0x40288CD8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT51_INTR_MASKED	0x40288CDC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT51_SRAM_DATA0	0x40288CE0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT51_SRAM_DATA1	0x40288CE4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT51_TR_CMD	0x40288CE8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT52_CH_CTL	0x40288D00	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT52_CH_STATUS	0x40288D04	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT52_CH_IDX	0x40288D08	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT52_CH_CURR_PTR	0x40288D0C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT52_INTR	0x40288D10	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT52_INTR_SET	0x40288D14	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT52_INTR_MASK	0x40288D18	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT52_INTR_MASKED	0x40288D1C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT52_SRAM_DATA0	0x40288D20	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT52_SRAM_DATA1	0x40288D24	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT52_TR_CMD	0x40288D28	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT53_CH_CTL	0x40288D40	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT53_CH_STATUS	0x40288D44	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT53_CH_IDX	0x40288D48	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT53_CH_CURR_PTR	0x40288D4C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT53_INTR	0x40288D50	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT53_INTR_SET	0x40288D54	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT53_INTR_MASK	0x40288D58	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT53_INTR_MASKED	0x40288D5C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT53_SRAM_DATA0	0x40288D60	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT53_SRAM_DATA1	0x40288D64	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT53_TR_CMD	0x40288D68	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT54_CH_CTL	0x40288D80	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT54_CH_STATUS	0x40288D84	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT54_CH_IDX	0x40288D88	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT54_CH_CURR_PTR	0x40288D8C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT54_INTR	0x40288D90	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT54_INTR_SET	0x40288D94	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT54_INTR_MASK	0x40288D98	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT54_INTR_MASKED	0x40288D9C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT54_SRAM_DATA0	0x40288DA0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT54_SRAM_DATA1	0x40288DA4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT54_TR_CMD	0x40288DA8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT55_CH_CTL	0x40288DC0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT55_CH_STATUS	0x40288DC4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT55_CH_IDX	0x40288DC8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT55_CH_CURR_PTR	0x40288DCC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT55_INTR	0x40288DD0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT55_INTR_SET	0x40288DD4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT55_INTR_MASK	0x40288DD8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT55_INTR_MASKED	0x40288DDC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT55_SRAM_DATA0	0x40288DE0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT55_SRAM_DATA1	0x40288DE4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT55_TR_CMD	0x40288DE8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT56_CH_CTL	0x40288E00	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT56_CH_STATUS	0x40288E04	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT56_CH_IDX	0x40288E08	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT56_CH_CURR_PTR	0x40288E0C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT56_INTR	0x40288E10	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT56_INTR_SET	0x40288E14	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT56_INTR_MASK	0x40288E18	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT56_INTR_MASKED	0x40288E1C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT56_SRAM_DATA0	0x40288E20	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT56_SRAM_DATA1	0x40288E24	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT56_TR_CMD	0x40288E28	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT57_CH_CTL	0x40288E40	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT57_CH_STATUS	0x40288E44	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT57_CH_IDX	0x40288E48	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT57_CH_CURR_PTR	0x40288E4C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT57_INTR	0x40288E50	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT57_INTR_SET	0x40288E54	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT57_INTR_MASK	0x40288E58	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT57_INTR_MASKED	0x40288E5C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT57_SRAM_DATA0	0x40288E60	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT57_SRAM_DATA1	0x40288E64	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT57_TR_CMD	0x40288E68	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT58_CH_CTL	0x40288E80	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT58_CH_STATUS	0x40288E84	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT58_CH_IDX	0x40288E88	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT58_CH_CURR_PTR	0x40288E8C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT58_INTR	0x40288E90	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT58_INTR_SET	0x40288E94	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT58_INTR_MASK	0x40288E98	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT58_INTR_MASKED	0x40288E9C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT58_SRAM_DATA0	0x40288EA0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT58_SRAM_DATA1	0x40288EA4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT58_TR_CMD	0x40288EA8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT59_CH_CTL	0x40288EC0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT59_CH_STATUS	0x40288EC4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT59_CH_IDX	0x40288EC8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT59_CH_CURR_PTR	0x40288ECC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT59_INTR	0x40288ED0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT59_INTR_SET	0x40288ED4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT59_INTR_MASK	0x40288ED8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT59_INTR_MASKED	0x40288EDC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT59_SRAM_DATA0	0x40288EE0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT59_SRAM_DATA1	0x40288EE4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT59_TR_CMD	0x40288EE8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT60_CH_CTL	0x40288F00	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT60_CH_STATUS	0x40288F04	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT60_CH_IDX	0x40288F08	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT60_CH_CURR_PTR	0x40288F0C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT60_INTR	0x40288F10	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT60_INTR_SET	0x40288F14	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT60_INTR_MASK	0x40288F18	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT60_INTR_MASKED	0x40288F1C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT60_SRAM_DATA0	0x40288F20	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT60_SRAM_DATA1	0x40288F24	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT60_TR_CMD	0x40288F28	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT61_CH_CTL	0x40288F40	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT61_CH_STATUS	0x40288F44	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT61_CH_IDX	0x40288F48	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT61_CH_CURR_PTR	0x40288F4C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT61_INTR	0x40288F50	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT61_INTR_SET	0x40288F54	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT61_INTR_MASK	0x40288F58	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT61_INTR_MASKED	0x40288F5C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT61_SRAM_DATA0	0x40288F60	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT61_SRAM_DATA1	0x40288F64	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT61_TR_CMD	0x40288F68	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT62_CH_CTL	0x40288F80	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT62_CH_STATUS	0x40288F84	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT62_CH_IDX	0x40288F88	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT62_CH_CURR_PTR	0x40288F8C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT62_INTR	0x40288F90	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT62_INTR_SET	0x40288F94	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT62_INTR_MASK	0x40288F98	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT62_INTR_MASKED	0x40288F9C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT62_SRAM_DATA0	0x40288FA0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT62_SRAM_DATA1	0x40288FA4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT62_TR_CMD	0x40288FA8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT63_CH_CTL	0x40288FC0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT63_CH_STATUS	0x40288FC4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT63_CH_IDX	0x40288FC8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT63_CH_CURR_PTR	0x40288FCC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT63_INTR	0x40288FD0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT63_INTR_SET	0x40288FD4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT63_INTR_MASK	0x40288FD8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT63_INTR_MASKED	0x40288FDC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT63_SRAM_DATA0	0x40288FE0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT63_SRAM_DATA1	0x40288FE4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT63_TR_CMD	0x40288FE8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT64_CH_CTL	0x40289000	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT64_CH_STATUS	0x40289004	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT64_CH_IDX	0x40289008	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT64_CH_CURR_PTR	0x4028900C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT64_INTR	0x40289010	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT64_INTR_SET	0x40289014	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT64_INTR_MASK	0x40289018	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT64_INTR_MASKED	0x4028901C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT64_SRAM_DATA0	0x40289020	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT64_SRAM_DATA1	0x40289024	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT64_TR_CMD	0x40289028	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT65_CH_CTL	0x40289040	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT65_CH_STATUS	0x40289044	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT65_CH_IDX	0x40289048	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT65_CH_CURR_PTR	0x4028904C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT65_INTR	0x40289050	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT65_INTR_SET	0x40289054	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT65_INTR_MASK	0x40289058	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT65_INTR_MASKED	0x4028905C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT65_SRAM_DATA0	0x40289060	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT65_SRAM_DATA1	0x40289064	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT65_TR_CMD	0x40289068	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT66_CH_CTL	0x40289080	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT66_CH_STATUS	0x40289084	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT66_CH_IDX	0x40289088	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT66_CH_CURR_PTR	0x4028908C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT66_INTR	0x40289090	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT66_INTR_SET	0x40289094	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT66_INTR_MASK	0x40289098	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT66_INTR_MASKED	0x4028909C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT66_SRAM_DATA0	0x402890A0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT66_SRAM_DATA1	0x402890A4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT66_TR_CMD	0x402890A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT67_CH_CTL	0x402890C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT67_CH_STATUS	0x402890C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT67_CH_IDX	0x402890C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT67_CH_CURR_PTR	0x402890CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT67_INTR	0x402890D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT67_INTR_SET	0x402890D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT67_INTR_MASK	0x402890D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT67_INTR_MASKED	0x402890DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT67_SRAM_DATA0	0x402890E0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT67_SRAM_DATA1	0x402890E4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT67_TR_CMD	0x402890E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT68_CH_CTL	0x40289100	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT68_CH_STATUS	0x40289104	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT68_CH_IDX	0x40289108	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT68_CH_CURR_PTR	0x4028910C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT68_INTR	0x40289110	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT68_INTR_SET	0x40289114	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT68_INTR_MASK	0x40289118	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT68_INTR_MASKED	0x4028911C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT68_SRAM_DATA0	0x40289120	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT68_SRAM_DATA1	0x40289124	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT68_TR_CMD	0x40289128	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT69_CH_CTL	0x40289140	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT69_CH_STATUS	0x40289144	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT69_CH_IDX	0x40289148	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT69_CH_CURR_PTR	0x4028914C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT69_INTR	0x40289150	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT69_INTR_SET	0x40289154	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT69_INTR_MASK	0x40289158	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT69_INTR_MASKED	0x4028915C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT69_SRAM_DATA0	0x40289160	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT69_SRAM_DATA1	0x40289164	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT69_TR_CMD	0x40289168	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT70_CH_CTL	0x40289180	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT70_CH_STATUS	0x40289184	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT70_CH_IDX	0x40289188	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT70_CH_CURR_PTR	0x4028918C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT70_INTR	0x40289190	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT70_INTR_SET	0x40289194	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT70_INTR_MASK	0x40289198	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT70_INTR_MASKED	0x4028919C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT70_SRAM_DATA0	0x402891A0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT70_SRAM_DATA1	0x402891A4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT70_TR_CMD	0x402891A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT71_CH_CTL	0x402891C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT71_CH_STATUS	0x402891C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT71_CH_IDX	0x402891C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT71_CH_CURR_PTR	0x402891CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT71_INTR	0x402891D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT71_INTR_SET	0x402891D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT71_INTR_MASK	0x402891D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT71_INTR_MASKED	0x402891DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT71_SRAM_DATA0	0x402891E0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT71_SRAM_DATA1	0x402891E4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT71_TR_CMD	0x402891E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT72_CH_CTL	0x40289200	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT72_CH_STATUS	0x40289204	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT72_CH_IDX	0x40289208	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT72_CH_CURR_PTR	0x4028920C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT72_INTR	0x40289210	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT72_INTR_SET	0x40289214	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT72_INTR_MASK	0x40289218	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT72_INTR_MASKED	0x4028921C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT72_SRAM_DATA0	0x40289220	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT72_SRAM_DATA1	0x40289224	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT72_TR_CMD	0x40289228	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT73_CH_CTL	0x40289240	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT73_CH_STATUS	0x40289244	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT73_CH_IDX	0x40289248	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT73_CH_CURR_PTR	0x4028924C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT73_INTR	0x40289250	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT73_INTR_SET	0x40289254	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT73_INTR_MASK	0x40289258	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT73_INTR_MASKED	0x4028925C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT73_SRAM_DATA0	0x40289260	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT73_SRAM_DATA1	0x40289264	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT73_TR_CMD	0x40289268	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT74_CH_CTL	0x40289280	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT74_CH_STATUS	0x40289284	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT74_CH_IDX	0x40289288	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT74_CH_CURR_PTR	0x4028928C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT74_INTR	0x40289290	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT74_INTR_SET	0x40289294	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT74_INTR_MASK	0x40289298	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT74_INTR_MASKED	0x4028929C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT74_SRAM_DATA0	0x402892A0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT74_SRAM_DATA1	0x402892A4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT74_TR_CMD	0x402892A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT75_CH_CTL	0x402892C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT75_CH_STATUS	0x402892C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT75_CH_IDX	0x402892C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT75_CH_CURR_PTR	0x402892CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT75_INTR	0x402892D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT75_INTR_SET	0x402892D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT75_INTR_MASK	0x402892D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT75_INTR_MASKED	0x402892DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT75_SRAM_DATA0	0x402892E0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT75_SRAM_DATA1	0x402892E4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT75_TR_CMD	0x402892E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT76_CH_CTL	0x40289300	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT76_CH_STATUS	0x40289304	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT76_CH_IDX	0x40289308	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT76_CH_CURR_PTR	0x4028930C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT76_INTR	0x40289310	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT76_INTR_SET	0x40289314	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT76_INTR_MASK	0x40289318	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT76_INTR_MASKED	0x4028931C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT76_SRAM_DATA0	0x40289320	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT76_SRAM_DATA1	0x40289324	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT76_TR_CMD	0x40289328	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT77_CH_CTL	0x40289340	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT77_CH_STATUS	0x40289344	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT77_CH_IDX	0x40289348	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT77_CH_CURR_PTR	0x4028934C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT77_INTR	0x40289350	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT77_INTR_SET	0x40289354	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT77_INTR_MASK	0x40289358	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT77_INTR_MASKED	0x4028935C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT77_SRAM_DATA0	0x40289360	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT77_SRAM_DATA1	0x40289364	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT77_TR_CMD	0x40289368	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT78_CH_CTL	0x40289380	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT78_CH_STATUS	0x40289384	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT78_CH_IDX	0x40289388	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT78_CH_CURR_PTR	0x4028938C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT78_INTR	0x40289390	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT78_INTR_SET	0x40289394	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT78_INTR_MASK	0x40289398	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT78_INTR_MASKED	0x4028939C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT78_SRAM_DATA0	0x402893A0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT78_SRAM_DATA1	0x402893A4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT78_TR_CMD	0x402893A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT79_CH_CTL	0x402893C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT79_CH_STATUS	0x402893C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT79_CH_IDX	0x402893C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT79_CH_CURR_PTR	0x402893CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT79_INTR	0x402893D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT79_INTR_SET	0x402893D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT79_INTR_MASK	0x402893D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT79_INTR_MASKED	0x402893DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT79_SRAM_DATA0	0x402893E0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT79_SRAM_DATA1	0x402893E4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT79_TR_CMD	0x402893E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT80_CH_CTL	0x40289400	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT80_CH_STATUS	0x40289404	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT80_CH_IDX	0x40289408	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT80_CH_CURR_PTR	0x4028940C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT80_INTR	0x40289410	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT80_INTR_SET	0x40289414	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT80_INTR_MASK	0x40289418	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT80_INTR_MASKED	0x4028941C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT80_SRAM_DATA0	0x40289420	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT80_SRAM_DATA1	0x40289424	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT80_TR_CMD	0x40289428	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT81_CH_CTL	0x40289440	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT81_CH_STATUS	0x40289444	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT81_CH_IDX	0x40289448	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT81_CH_CURR_PTR	0x4028944C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT81_INTR	0x40289450	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT81_INTR_SET	0x40289454	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT81_INTR_MASK	0x40289458	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT81_INTR_MASKED	0x4028945C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT81_SRAM_DATA0	0x40289460	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT81_SRAM_DATA1	0x40289464	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT81_TR_CMD	0x40289468	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT82_CH_CTL	0x40289480	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT82_CH_STATUS	0x40289484	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT82_CH_IDX	0x40289488	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT82_CH_CURR_PTR	0x4028948C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT82_INTR	0x40289490	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT82_INTR_SET	0x40289494	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT82_INTR_MASK	0x40289498	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT82_INTR_MASKED	0x4028949C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT82_SRAM_DATA0	0x402894A0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT82_SRAM_DATA1	0x402894A4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT82_TR_CMD	0x402894A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT83_CH_CTL	0x402894C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT83_CH_STATUS	0x402894C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT83_CH_IDX	0x402894C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT83_CH_CURR_PTR	0x402894CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT83_INTR	0x402894D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT83_INTR_SET	0x402894D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT83_INTR_MASK	0x402894D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT83_INTR_MASKED	0x402894DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT83_SRAM_DATA0	0x402894E0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT83_SRAM_DATA1	0x402894E4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT83_TR_CMD	0x402894E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT84_CH_CTL	0x40289500	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT84_CH_STATUS	0x40289504	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT84_CH_IDX	0x40289508	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT84_CH_CURR_PTR	0x4028950C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT84_INTR	0x40289510	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT84_INTR_SET	0x40289514	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT84_INTR_MASK	0x40289518	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT84_INTR_MASKED	0x4028951C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT84_SRAM_DATA0	0x40289520	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT84_SRAM_DATA1	0x40289524	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT84_TR_CMD	0x40289528	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT85_CH_CTL	0x40289540	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT85_CH_STATUS	0x40289544	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT85_CH_IDX	0x40289548	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT85_CH_CURR_PTR	0x4028954C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT85_INTR	0x40289550	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT85_INTR_SET	0x40289554	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT85_INTR_MASK	0x40289558	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT85_INTR_MASKED	0x4028955C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT85_SRAM_DATA0	0x40289560	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT85_SRAM_DATA1	0x40289564	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT85_TR_CMD	0x40289568	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT86_CH_CTL	0x40289580	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT86_CH_STATUS	0x40289584	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT86_CH_IDX	0x40289588	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT86_CH_CURR_PTR	0x4028958C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT86_INTR	0x40289590	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT86_INTR_SET	0x40289594	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT86_INTR_MASK	0x40289598	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT86_INTR_MASKED	0x4028959C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT86_SRAM_DATA0	0x402895A0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT86_SRAM_DATA1	0x402895A4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT86_TR_CMD	0x402895A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT87_CH_CTL	0x402895C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT87_CH_STATUS	0x402895C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT87_CH_IDX	0x402895C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT87_CH_CURR_PTR	0x402895CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT87_INTR	0x402895D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT87_INTR_SET	0x402895D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT87_INTR_MASK	0x402895D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT87_INTR_MASKED	0x402895DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT87_SRAM_DATA0	0x402895E0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT87_SRAM_DATA1	0x402895E4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT87_TR_CMD	0x402895E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT88_CH_CTL	0x40289600	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT88_CH_STATUS	0x40289604	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT88_CH_IDX	0x40289608	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT88_CH_CURR_PTR	0x4028960C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT88_INTR	0x40289610	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT88_INTR_SET	0x40289614	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.

Register name	Address	Description
DW0_CH_STRUCT88_INTR_MASK	0x40289618	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT88_INTR_MASKED	0x4028961C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT88_SRAM_DATA0	0x40289620	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW0_CH_STRUCT88_SRAM_DATA1	0x40289624	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW0_CH_STRUCT88_TR_CMD	0x40289628	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CTL0	0x40290000	Control. See DW0_CTL0 for the details of bit fields.
DW1_STATUS0	0x40290004	Status
DW1_ACT_DESCR_CTL0	0x40290020	Active descriptor control. See DW0_ACT_DESCR_CTL0 for the details of bit fields.
DW1_ACT_DESCR_SRC0	0x40290024	Active descriptor source. See DW0_ACT_DESCR_SRC0 for the details of bit fields.
DW1_ACT_DESCR_DST0	0x40290028	Active descriptor destination. See DW0_ACT_DESCR_DST0 for the details of bit fields.
DW1_ACT_DESCR_X_CTL0	0x40290030	Active descriptor X loop control. See DW0_ACT_DESCR_X_CTL0 for the details of bit fields.
DW1_ACT_DESCR_Y_CTL0	0x40290034	Active descriptor Y loop control. See DW0_ACT_DESCR_Y_CTL0 for the details of bit fields.
DW1_ACT_DESCR_NEXT_PTR0	0x40290038	Active descriptor next pointer. See DW0_ACT_DESCR_NEXT_PTR0 for the details of bit fields.
DW1_ACT_SRC0	0x40290040	Active source. See DW0_ACT_SRC0 for the details of bit fields.
DW1_ACT_DST0	0x40290044	Active destination. See DW0_ACT_DST0 for the details of bit fields.
DW1_ECC_CTL0	0x40290080	ECC control. See DW0_ECC_CTL0 for the details of bit fields.
DW1_CRC_CTL0	0x40290100	CRC control. See DW0_CRC_CTL0 for the details of bit fields.
DW1_CRC_DATA_CTL0	0x40290110	CRC data control. See DW0_CRC_DATA_CTL0 for the details of bit fields.
DW1_CRC_POL_CTL0	0x40290120	CRC polynomial control. See DW0_CRC_POL_CTL0 for the details of bit fields.
DW1_CRC_LFSR_CTL0	0x40290130	CRC LFSR control. See DW0_CRC_LFSR_CTL0 for the details of bit fields.
DW1_CRC_REM_CTL0	0x40290140	CRC remainder control. See DW0_CRC_REM_CTL0 for the details of bit fields.
DW1_CRC_REM_RESULT0	0x40290148	CRC remainder result. See DW0_CRC_REM_RESULT0 for the details of bit fields.

Register name	Address	Description
DW1_CH_STRUCT0_CH_CTL	0x40298000	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT0_CH_STATUS	0x40298004	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT0_CH_IDX	0x40298008	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT0_CH_CURR_PTR	0x4029800C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT0_INTR	0x40298010	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT0_INTR_SET	0x40298014	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT0_INTR_MASK	0x40298018	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT0_INTR_MASKED	0x4029801C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT0_SRAM_DATA0	0x40298020	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT0_SRAM_DATA1	0x40298024	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT0_TR_CMD	0x40298028	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT1_CH_CTL	0x40298040	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT1_CH_STATUS	0x40298044	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT1_CH_IDX	0x40298048	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT1_CH_CURR_PTR	0x4029804C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT1_INTR	0x40298050	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT1_INTR_SET	0x40298054	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT1_INTR_MASK	0x40298058	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT1_INTR_MASKED	0x4029805C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT1_SRAM_DATA0	0x40298060	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.

Register name	Address	Description
DW1_CH_STRUCT1_SRAM_DATA1	0x40298064	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT1_TR_CMD	0x40298068	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT2_CH_CTL	0x40298080	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT2_CH_STATUS	0x40298084	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT2_CH_IDX	0x40298088	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT2_CH_CURR_PTR	0x4029808C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT2_INTR	0x40298090	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT2_INTR_SET	0x40298094	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT2_INTR_MASK	0x40298098	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT2_INTR_MASKED	0x4029809C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT2_SRAM_DATA0	0x402980A0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT2_SRAM_DATA1	0x402980A4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT2_TR_CMD	0x402980A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT3_CH_CTL	0x402980C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT3_CH_STATUS	0x402980C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT3_CH_IDX	0x402980C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT3_CH_CURR_PTR	0x402980CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT3_INTR	0x402980D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT3_INTR_SET	0x402980D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT3_INTR_MASK	0x402980D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.

Register name	Address	Description
DW1_CH_STRUCT3_INTR_MASKED	0x402980DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT3_SRAM_DATA0	0x402980E0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT3_SRAM_DATA1	0x402980E4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT3_TR_CMD	0x402980E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT4_CH_CTL	0x40298100	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT4_CH_STATUS	0x40298104	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT4_CH_IDX	0x40298108	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT4_CH_CURR_PTR	0x4029810C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT4_INTR	0x40298110	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT4_INTR_SET	0x40298114	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT4_INTR_MASK	0x40298118	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT4_INTR_MASKED	0x4029811C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT4_SRAM_DATA0	0x40298120	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT4_SRAM_DATA1	0x40298124	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT4_TR_CMD	0x40298128	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT5_CH_CTL	0x40298140	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT5_CH_STATUS	0x40298144	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT5_CH_IDX	0x40298148	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT5_CH_CURR_PTR	0x4029814C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT5_INTR	0x40298150	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.

Register name	Address	Description
DW1_CH_STRUCT5_INTR_SET	0x40298154	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT5_INTR_MASK	0x40298158	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT5_INTR_MASKED	0x4029815C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT5_SRAM_DATA0	0x40298160	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT5_SRAM_DATA1	0x40298164	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT5_TR_CMD	0x40298168	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT6_CH_CTL	0x40298180	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT6_CH_STATUS	0x40298184	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT6_CH_IDX	0x40298188	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT6_CH_CURR_PTR	0x4029818C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT6_INTR	0x40298190	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT6_INTR_SET	0x40298194	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT6_INTR_MASK	0x40298198	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT6_INTR_MASKED	0x4029819C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT6_SRAM_DATA0	0x402981A0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT6_SRAM_DATA1	0x402981A4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT6_TR_CMD	0x402981A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT7_CH_CTL	0x402981C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT7_CH_STATUS	0x402981C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT7_CH_IDX	0x402981C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

Register name	Address	Description
DW1_CH_STRUCT7_CH_CURR_PTR	0x402981CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT7_INTR	0x402981D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT7_INTR_SET	0x402981D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT7_INTR_MASK	0x402981D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT7_INTR_MASKED	0x402981DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT7_SRAM_DATA0	0x402981E0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT7_SRAM_DATA1	0x402981E4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT7_TR_CMD	0x402981E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT8_CH_CTL	0x40298200	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT8_CH_STATUS	0x40298204	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT8_CH_IDX	0x40298208	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT8_CH_CURR_PTR	0x4029820C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT8_INTR	0x40298210	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT8_INTR_SET	0x40298214	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT8_INTR_MASK	0x40298218	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT8_INTR_MASKED	0x4029821C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT8_SRAM_DATA0	0x40298220	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT8_SRAM_DATA1	0x40298224	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT8_TR_CMD	0x40298228	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT9_CH_CTL	0x40298240	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.

Register name	Address	Description
DW1_CH_STRUCT9_CH_STATUS	0x40298244	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT9_CH_IDX	0x40298248	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT9_CH_CURR_PTR	0x4029824C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT9_INTR	0x40298250	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT9_INTR_SET	0x40298254	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT9_INTR_MASK	0x40298258	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT9_INTR_MASKED	0x4029825C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT9_SRAM_DATA0	0x40298260	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT9_SRAM_DATA1	0x40298264	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT9_TR_CMD	0x40298268	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT10_CH_CTL	0x40298280	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT10_CH_STATUS	0x40298284	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT10_CH_IDX	0x40298288	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT10_CH_CURR_PTR	0x4029828C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT10_INTR	0x40298290	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT10_INTR_SET	0x40298294	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT10_INTR_MASK	0x40298298	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT10_INTR_MASKED	0x4029829C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT10_SRAM_DATA0	0x402982A0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT10_SRAM_DATA1	0x402982A4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.

Register name	Address	Description
DW1_CH_STRUCT10_TR_CMD	0x402982A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT11_CH_CTL	0x402982C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT11_CH_STATUS	0x402982C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT11_CH_IDX	0x402982C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT11_CH_CURR_PTR	0x402982CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT11_INTR	0x402982D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT11_INTR_SET	0x402982D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT11_INTR_MASK	0x402982D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT11_INTR_MASKED	0x402982DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT11_SRAM_DATA0	0x402982E0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT11_SRAM_DATA1	0x402982E4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT11_TR_CMD	0x402982E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT12_CH_CTL	0x40298300	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT12_CH_STATUS	0x40298304	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT12_CH_IDX	0x40298308	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT12_CH_CURR_PTR	0x4029830C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT12_INTR	0x40298310	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT12_INTR_SET	0x40298314	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT12_INTR_MASK	0x40298318	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT12_INTR_MASKED	0x4029831C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
DW1_CH_STRUCT12_SRAM_DATA0	0x40298320	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT12_SRAM_DATA1	0x40298324	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT12_TR_CMD	0x40298328	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT13_CH_CTL	0x40298340	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT13_CH_STATUS	0x40298344	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT13_CH_IDX	0x40298348	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT13_CH_CURR_PTR	0x4029834C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT13_INTR	0x40298350	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT13_INTR_SET	0x40298354	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT13_INTR_MASK	0x40298358	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT13_INTR_MASKED	0x4029835C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT13_SRAM_DATA0	0x40298360	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT13_SRAM_DATA1	0x40298364	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT13_TR_CMD	0x40298368	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT14_CH_CTL	0x40298380	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT14_CH_STATUS	0x40298384	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT14_CH_IDX	0x40298388	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT14_CH_CURR_PTR	0x4029838C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT14_INTR	0x40298390	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT14_INTR_SET	0x40298394	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.

Register name	Address	Description
DW1_CH_STRUCT14_INTR_MASK	0x40298398	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT14_INTR_MASKED	0x4029839C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT14_SRAM_DATA0	0x402983A0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT14_SRAM_DATA1	0x402983A4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT14_TR_CMD	0x402983A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT15_CH_CTL	0x402983C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT15_CH_STATUS	0x402983C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT15_CH_IDX	0x402983C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT15_CH_CURR_PTR	0x402983CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT15_INTR	0x402983D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT15_INTR_SET	0x402983D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT15_INTR_MASK	0x402983D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT15_INTR_MASKED	0x402983DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT15_SRAM_DATA0	0x402983E0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT15_SRAM_DATA1	0x402983E4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT15_TR_CMD	0x402983E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT16_CH_CTL	0x40298400	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT16_CH_STATUS	0x40298404	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT16_CH_IDX	0x40298408	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT16_CH_CURR_PTR	0x4029840C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.

Register name	Address	Description
DW1_CH_STRUCT16_INTR	0x40298410	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT16_INTR_SET	0x40298414	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT16_INTR_MASK	0x40298418	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT16_INTR_MASKED	0x4029841C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT16_SRAM_DATA0	0x40298420	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT16_SRAM_DATA1	0x40298424	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT16_TR_CMD	0x40298428	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT17_CH_CTL	0x40298440	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT17_CH_STATUS	0x40298444	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT17_CH_IDX	0x40298448	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT17_CH_CURR_PTR	0x4029844C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT17_INTR	0x40298450	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT17_INTR_SET	0x40298454	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT17_INTR_MASK	0x40298458	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT17_INTR_MASKED	0x4029845C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT17_SRAM_DATA0	0x40298460	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT17_SRAM_DATA1	0x40298464	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT17_TR_CMD	0x40298468	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT18_CH_CTL	0x40298480	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT18_CH_STATUS	0x40298484	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.

Register name	Address	Description
DW1_CH_STRUCT18_CH_IDX	0x40298488	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT18_CH_CURR_PTR	0x4029848C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT18_INTR	0x40298490	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT18_INTR_SET	0x40298494	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT18_INTR_MASK	0x40298498	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT18_INTR_MASKED	0x4029849C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT18_SRAM_DATA0	0x402984A0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT18_SRAM_DATA1	0x402984A4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT18_TR_CMD	0x402984A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT19_CH_CTL	0x402984C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT19_CH_STATUS	0x402984C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT19_CH_IDX	0x402984C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT19_CH_CURR_PTR	0x402984CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT19_INTR	0x402984D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT19_INTR_SET	0x402984D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT19_INTR_MASK	0x402984D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT19_INTR_MASKED	0x402984DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT19_SRAM_DATA0	0x402984E0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT19_SRAM_DATA1	0x402984E4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT19_TR_CMD	0x402984E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.

Register name	Address	Description
DW1_CH_STRUCT20_CH_CTL	0x40298500	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT20_CH_STATUS	0x40298504	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT20_CH_IDX	0x40298508	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT20_CH_CURR_PTR	0x4029850C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT20_INTR	0x40298510	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT20_INTR_SET	0x40298514	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT20_INTR_MASK	0x40298518	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT20_INTR_MASKED	0x4029851C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT20_SRAM_DATA0	0x40298520	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT20_SRAM_DATA1	0x40298524	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT20_TR_CMD	0x40298528	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT21_CH_CTL	0x40298540	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT21_CH_STATUS	0x40298544	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT21_CH_IDX	0x40298548	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT21_CH_CURR_PTR	0x4029854C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT21_INTR	0x40298550	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT21_INTR_SET	0x40298554	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT21_INTR_MASK	0x40298558	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT21_INTR_MASKED	0x4029855C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT21_SRAM_DATA0	0x40298560	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.

Register name	Address	Description
DW1_CH_STRUCT21_SRAM_DATA1	0x40298564	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT21_TR_CMD	0x40298568	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT22_CH_CTL	0x40298580	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT22_CH_STATUS	0x40298584	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT22_CH_IDX	0x40298588	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT22_CH_CURR_PTR	0x4029858C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT22_INTR	0x40298590	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT22_INTR_SET	0x40298594	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT22_INTR_MASK	0x40298598	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT22_INTR_MASKED	0x4029859C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT22_SRAM_DATA0	0x402985A0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT22_SRAM_DATA1	0x402985A4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT22_TR_CMD	0x402985A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT23_CH_CTL	0x402985C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT23_CH_STATUS	0x402985C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT23_CH_IDX	0x402985C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT23_CH_CURR_PTR	0x402985CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT23_INTR	0x402985D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT23_INTR_SET	0x402985D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT23_INTR_MASK	0x402985D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.

Register name	Address	Description
DW1_CH_STRUCT23_INTR_MASKED	0x402985DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT23_SRAM_DATA0	0x402985E0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT23_SRAM_DATA1	0x402985E4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT23_TR_CMD	0x402985E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT24_CH_CTL	0x40298600	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT24_CH_STATUS	0x40298604	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT24_CH_IDX	0x40298608	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT24_CH_CURR_PTR	0x4029860C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT24_INTR	0x40298610	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT24_INTR_SET	0x40298614	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT24_INTR_MASK	0x40298618	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT24_INTR_MASKED	0x4029861C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT24_SRAM_DATA0	0x40298620	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT24_SRAM_DATA1	0x40298624	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT24_TR_CMD	0x40298628	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT25_CH_CTL	0x40298640	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT25_CH_STATUS	0x40298644	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT25_CH_IDX	0x40298648	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT25_CH_CURR_PTR	0x4029864C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT25_INTR	0x40298650	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.

Register name	Address	Description
DW1_CH_STRUCT25_INTR_SET	0x40298654	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT25_INTR_MASK	0x40298658	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT25_INTR_MASKED	0x4029865C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT25_SRAM_DATA0	0x40298660	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT25_SRAM_DATA1	0x40298664	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT25_TR_CMD	0x40298668	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT26_CH_CTL	0x40298680	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT26_CH_STATUS	0x40298684	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT26_CH_IDX	0x40298688	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT26_CH_CURR_PTR	0x4029868C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT26_INTR	0x40298690	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT26_INTR_SET	0x40298694	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT26_INTR_MASK	0x40298698	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT26_INTR_MASKED	0x4029869C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT26_SRAM_DATA0	0x402986A0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT26_SRAM_DATA1	0x402986A4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT26_TR_CMD	0x402986A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT27_CH_CTL	0x402986C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT27_CH_STATUS	0x402986C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT27_CH_IDX	0x402986C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

Register name	Address	Description
DW1_CH_STRUCT27_CH_CURR_PTR	0x402986CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT27_INTR	0x402986D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT27_INTR_SET	0x402986D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT27_INTR_MASK	0x402986D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT27_INTR_MASKED	0x402986DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT27_SRAM_DATA0	0x402986E0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT27_SRAM_DATA1	0x402986E4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT27_TR_CMD	0x402986E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT28_CH_CTL	0x40298700	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT28_CH_STATUS	0x40298704	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT28_CH_IDX	0x40298708	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT28_CH_CURR_PTR	0x4029870C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT28_INTR	0x40298710	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT28_INTR_SET	0x40298714	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT28_INTR_MASK	0x40298718	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT28_INTR_MASKED	0x4029871C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT28_SRAM_DATA0	0x40298720	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT28_SRAM_DATA1	0x40298724	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT28_TR_CMD	0x40298728	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT29_CH_CTL	0x40298740	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.

Register name	Address	Description
DW1_CH_STRUCT29_CH_STATUS	0x40298744	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT29_CH_IDX	0x40298748	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT29_CH_CURR_PTR	0x4029874C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT29_INTR	0x40298750	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT29_INTR_SET	0x40298754	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT29_INTR_MASK	0x40298758	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT29_INTR_MASKED	0x4029875C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT29_SRAM_DATA0	0x40298760	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT29_SRAM_DATA1	0x40298764	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT29_TR_CMD	0x40298768	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT30_CH_CTL	0x40298780	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT30_CH_STATUS	0x40298784	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT30_CH_IDX	0x40298788	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT30_CH_CURR_PTR	0x4029878C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT30_INTR	0x40298790	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT30_INTR_SET	0x40298794	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT30_INTR_MASK	0x40298798	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT30_INTR_MASKED	0x4029879C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT30_SRAM_DATA0	0x402987A0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT30_SRAM_DATA1	0x402987A4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.

Register name	Address	Description
DW1_CH_STRUCT30_TR_CMD	0x402987A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT31_CH_CTL	0x402987C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT31_CH_STATUS	0x402987C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT31_CH_IDX	0x402987C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT31_CH_CURR_PTR	0x402987CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT31_INTR	0x402987D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT31_INTR_SET	0x402987D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT31_INTR_MASK	0x402987D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT31_INTR_MASKED	0x402987DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT31_SRAM_DATA0	0x402987E0	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT31_SRAM_DATA1	0x402987E4	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT31_TR_CMD	0x402987E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT32_CH_CTL	0x40298800	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT32_CH_STATUS	0x40298804	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT32_CH_IDX	0x40298808	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT32_CH_CURR_PTR	0x4029880C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT32_INTR	0x40298810	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT32_INTR_SET	0x40298814	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT32_INTR_MASK	0x40298818	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT32_INTR_MASKED	0x4029881C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
DW1_CH_STRUCT32_SRAM_DATA0	0x40298820	SRAM data 0. See DW0_CH_STRUCT0_SRAM_DATA0 for the details of bit fields.
DW1_CH_STRUCT32_SRAM_DATA1	0x40298824	SRAM data 1. See DW0_CH_STRUCT0_SRAM_DATA1 for the details of bit fields.
DW1_CH_STRUCT32_TR_CMD	0x40298828	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DMAC_CTL	0x402A0000	Control
DMAC_ACTIVE	0x402A0008	Active channels
DMAC_CH0_CTL	0x402A1000	Channel control
DMAC_CH0_IDX	0x402A1010	Channel current indices
DMAC_CH0_SRC	0x402A1014	Channel current source address
DMAC_CH0_DST	0x402A1018	Channel current destination address
DMAC_CH0_CURR	0x402A1020	Channel current descriptor pointer
DMAC_CH0_TR_CMD	0x402A1028	Channle software trigger
DMAC_CH0_DESCR_STATUS	0x402A1040	Channel descriptor status
DMAC_CH0_DESCR_CTL	0x402A1060	Channel descriptor control
DMAC_CH0_DESCR_SRC	0x402A1064	Channel descriptor source
DMAC_CH0_DESCR_DST	0x402A1068	Channel descriptor destination
DMAC_CH0_DESCR_X_SIZE	0x402A106C	Channel descriptor X size
DMAC_CH0_DESCR_X_INCR	0x402A1070	Channel descriptor X increment
DMAC_CH0_DESCR_Y_SIZE	0x402A1074	Channel descriptor Y size
DMAC_CH0_DESCR_Y_INCR	0x402A1078	Channel descriptor Y increment
DMAC_CH0_DESCR_NEXT	0x402A107C	Channel descriptor next pointer
DMAC_CH0_INTR	0x402A1080	Interrupt
DMAC_CH0_INTR_SET	0x402A1084	Interrupt set
DMAC_CH0_INTR_MASK	0x402A1088	Interrupt mask
DMAC_CH0_INTR_MASKED	0x402A108C	Interrupt masked
DMAC_CH1_CTL	0x402A1100	Channel control. See DMAC_CH0_CTL for the details of bit fields.
DMAC_CH1_IDX	0x402A1110	Channel current indices. See DMAC_CH0_IDX for the details of bit fields.
DMAC_CH1_SRC	0x402A1114	Channel current source address. See DMAC_CH0_SRC for the details of bit fields.
DMAC_CH1_DST	0x402A1118	Channel current destination address. See DMAC_CH0_DST for the details of bit fields.
DMAC_CH1_CURR	0x402A1120	Channel current descriptor pointer. See DMAC_CH0_CURR for the details of bit fields.
DMAC_CH1_TR_CMD	0x402A1128	Channle software trigger. See DMAC_CH0_TR_CMD for the details of bit fields.

Register name	Address	Description
DMAC_CH1_DESCR_STATUS	0x402A1140	Channel descriptor status. See DMAC_CH0_DESCR_STATUS for the details of bit fields.
DMAC_CH1_DESCR_CTL	0x402A1160	Channel descriptor control. See DMAC_CH0_DESCR_CTL for the details of bit fields.
DMAC_CH1_DESCR_SRC	0x402A1164	Channel descriptor source. See DMAC_CH0_DESCR_SRC for the details of bit fields.
DMAC_CH1_DESCR_DST	0x402A1168	Channel descriptor destination. See DMAC_CH0_DESCR_DST for the details of bit fields.
DMAC_CH1_DESCR_X_SIZE	0x402A116C	Channel descriptor X size. See DMAC_CH0_DESCR_X_SIZE for the details of bit fields.
DMAC_CH1_DESCR_X_INCR	0x402A1170	Channel descriptor X increment. See DMAC_CH0_DESCR_X_INCR for the details of bit fields.
DMAC_CH1_DESCR_Y_SIZE	0x402A1174	Channel descriptor Y size. See DMAC_CH0_DESCR_Y_SIZE for the details of bit fields.
DMAC_CH1_DESCR_Y_INCR	0x402A1178	Channel descriptor Y increment. See DMAC_CH0_DESCR_Y_INCR for the details of bit fields.
DMAC_CH1_DESCR_NEXT	0x402A117C	Channel descriptor next pointer. See DMAC_CH0_DESCR_NEXT for the details of bit fields.
DMAC_CH1_INTR	0x402A1180	Interrupt. See DMAC_CH0_INTR for the details of bit fields.
DMAC_CH1_INTR_SET	0x402A1184	Interrupt set. See DMAC_CH0_INTR_SET for the details of bit fields.
DMAC_CH1_INTR_MASK	0x402A1188	Interrupt mask. See DMAC_CH0_INTR_MASK for the details of bit fields.
DMAC_CH1_INTR_MASKED	0x402A118C	Interrupt masked. See DMAC_CH0_INTR_MASKED for the details of bit fields.
DMAC_CH2_CTL	0x402A1200	Channel control. See DMAC_CH0_CTL for the details of bit fields.
DMAC_CH2_IDX	0x402A1210	Channel current indices. See DMAC_CH0_IDX for the details of bit fields.
DMAC_CH2_SRC	0x402A1214	Channel current source address. See DMAC_CH0_SRC for the details of bit fields.
DMAC_CH2_DST	0x402A1218	Channel current destination address. See DMAC_CH0_DST for the details of bit fields.
DMAC_CH2_CURR	0x402A1220	Channel current descriptor pointer. See DMAC_CH0_CURR for the details of bit fields.
DMAC_CH2_TR_CMD	0x402A1228	Channle software trigger. See DMAC_CH0_TR_CMD for the details of bit fields.
DMAC_CH2_DESCR_STATUS	0x402A1240	Channel descriptor status. See DMAC_CH0_DESCR_STATUS for the details of bit fields.
DMAC_CH2_DESCR_CTL	0x402A1260	Channel descriptor control. See DMAC_CH0_DESCR_CTL for the details of bit fields.
DMAC_CH2_DESCR_SRC	0x402A1264	Channel descriptor source. See DMAC_CH0_DESCR_SRC for the details of bit fields.

Register name	Address	Description
DMAC_CH2_DESCR_DST	0x402A1268	Channel descriptor destination. See DMAC_CH0_DESCR_DST for the details of bit fields.
DMAC_CH2_DESCR_X_SIZE	0x402A126C	Channel descriptor X size. See DMAC_CH0_DESCR_X_SIZE for the details of bit fields.
DMAC_CH2_DESCR_X_INCR	0x402A1270	Channel descriptor X increment. See DMAC_CH0_DESCR_X_INCR for the details of bit fields.
DMAC_CH2_DESCR_Y_SIZE	0x402A1274	Channel descriptor Y size. See DMAC_CH0_DESCR_Y_SIZE for the details of bit fields.
DMAC_CH2_DESCR_Y_INCR	0x402A1278	Channel descriptor Y increment. See DMAC_CH0_DESCR_Y_INCR for the details of bit fields.
DMAC_CH2_DESCR_NEXT	0x402A127C	Channel descriptor next pointer. See DMAC_CH0_DESCR_NEXT for the details of bit fields.
DMAC_CH2_INTR	0x402A1280	Interrupt. See DMAC_CH0_INTR for the details of bit fields.
DMAC_CH2_INTR_SET	0x402A1284	Interrupt set. See DMAC_CH0_INTR_SET for the details of bit fields.
DMAC_CH2_INTR_MASK	0x402A1288	Interrupt mask. See DMAC_CH0_INTR_MASK for the details of bit fields.
DMAC_CH2_INTR_MASKED	0x402A128C	Interrupt masked. See DMAC_CH0_INTR_MASKED for the details of bit fields.
DMAC_CH3_CTL	0x402A1300	Channel control. See DMAC_CH0_CTL for the details of bit fields.
DMAC_CH3_IDX	0x402A1310	Channel current indices. See DMAC_CH0_IDX for the details of bit fields.
DMAC_CH3_SRC	0x402A1314	Channel current source address. See DMAC_CH0_SRC for the details of bit fields.
DMAC_CH3_DST	0x402A1318	Channel current destination address. See DMAC_CH0_DST for the details of bit fields.
DMAC_CH3_CURR	0x402A1320	Channel current descriptor pointer. See DMAC_CH0_CURR for the details of bit fields.
DMAC_CH3_TR_CMD	0x402A1328	Channle software trigger. See DMAC_CH0_TR_CMD for the details of bit fields.
DMAC_CH3_DESCR_STATUS	0x402A1340	Channel descriptor status. See DMAC_CH0_DESCR_STATUS for the details of bit fields.
DMAC_CH3_DESCR_CTL	0x402A1360	Channel descriptor control. See DMAC_CH0_DESCR_CTL for the details of bit fields.
DMAC_CH3_DESCR_SRC	0x402A1364	Channel descriptor source. See DMAC_CH0_DESCR_SRC for the details of bit fields.
DMAC_CH3_DESCR_DST	0x402A1368	Channel descriptor destination. See DMAC_CH0_DESCR_DST for the details of bit fields.
DMAC_CH3_DESCR_X_SIZE	0x402A136C	Channel descriptor X size. See DMAC_CH0_DESCR_X_SIZE for the details of bit fields.
DMAC_CH3_DESCR_X_INCR	0x402A1370	Channel descriptor X increment. See DMAC_CH0_DESCR_X_INCR for the details of bit fields.

Register name	Address	Description
DMAC_CH3_DESCR_Y_SIZE	0x402A1374	Channel descriptor Y size. See DMAC_CH0_DESCR_Y_SIZE for the details of bit fields.
DMAC_CH3_DESCR_Y_INCR	0x402A1378	Channel descriptor Y increment. See DMAC_CH0_DESCR_Y_INCR for the details of bit fields.
DMAC_CH3_DESCR_NEXT	0x402A137C	Channel descriptor next pointer. See DMAC_CH0_DESCR_NEXT for the details of bit fields.
DMAC_CH3_INTR	0x402A1380	Interrupt. See DMAC_CH0_INTR for the details of bit fields.
DMAC_CH3_INTR_SET	0x402A1384	Interrupt set. See DMAC_CH0_INTR_SET for the details of bit fields.
DMAC_CH3_INTR_MASK	0x402A1388	Interrupt mask. See DMAC_CH0_INTR_MASK for the details of bit fields.
DMAC_CH3_INTR_MASKED	0x402A138C	Interrupt masked. See DMAC_CH0_INTR_MASKED for the details of bit fields.

4.1 Direct memory access (DMA) registers

DW0_CTL0

Control
Address: 0x40280000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						ECC_INJ_EN	ECC_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description

31	ENABLED	IP enable: '0': Disabled. Disabling the IP activates the IP's Active logic reset: Active logic and non-retention MMIO registers are reset (retention MMIO registers are not affected). '1': Enabled. Default Value: 0
1	ECC_INJ_EN	Enable parity injection for SRAM. When '1', the parity (ECC_CTL.PARITY) is used when a full 32-bit write is done to the ECC_CTL.WORD_ADDR word address of the SRAM. Default Value: 0
0	ECC_EN	Enable ECC checking: '0': Disabled. '1': Enabled. Default Value: 1

DW0_STATUS0

Status
Address: 0x40280004
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None	R	R	R
HW Access	RW				None	RW	RW	RW
Name	PC [7:4]				None	B	NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	None	R	
HW Access	None				W	None	W	
Name	None [15:12]				PREEMPTABLE	None	PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None	R						
HW Access	None	W						
Name	None	CH_IDX [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	R	R			None			
HW Access	W	W			None			
Name	ACTIVE	STATE [30:28]			None [27:24]			

Bits	Name	Description
31	ACTIVE	Active channel present: '0': No. '1': Yes. Default Value: 0
30 : 28	STATE	State of the DW controller. "0": Default/inactive state. "1": Loading descriptor. "2": Loading data element from source location. "3": Storing data element to destination location. "4": CRC functionality (only used for CRC transfer descriptor type). "5": Update of active control information (e.g. source and destination addresses) and wait for trigger de-activation. "6": Error. Default Value: 0
22 : 16	CH_IDX	Active channel index. Default Value: Undefined
11	PREEMPTABLE	Active channel preemptable. Default Value: Undefined
9 : 8	PRIO	Active channel priority. Default Value: Undefined

7 : 4	PC	Active channel protection context. Default Value: Undefined
2	B	Active channel, non-bufferable/ bufferable access control: '0': non-bufferable '1': bufferable. Default Value: Undefined
1	NS	Active channel, secure/non-secure access control: '0': secure. '1': non-secure. Default Value: Undefined
0	P	Active channel, user/privileged access control: '0': user mode. '1': privileged mode. Default Value: Undefined

DW0_ACT_DESCR_CTL0

Active descriptor control
Address: 0x40280020
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description

31 : 0	DATA	Copy of DESCR_CTL of the currently active descriptor. [1:0] WAIT_FOR_DEACT Specifies whether the controller should wait for the input trigger to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controller with the agent that generated the trigger. This field is ONLY used at the completion of the transfer as specified by TR_IN. E.g., a TX FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the controller AND received by the agent. Furthermore, the agent's trigger may be delayed by a few cycles before it reaches the controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW controller performance. "0": Do not wait for trigger de-activation (for pulse sensitive triggers). "1": Wait for up to 4 cycles. "2": Wait for up to 16 cycles. "3": Wait indefinitely. This option may result in controller lockup if the trigger is not de-activated. [3:2] INTR_TYPE Specifies the input trigger type (not to be confused with the descriptor type): "0": A trigger results in the execution of a single transfer. The descriptor type can be single, 1D or 2D. "1": A trigger results in the execution of a single 1D transfer. - If the descriptor type is "single", the trigger results in the execution of a single transfer. - If the descriptor type is "1D" or "2D", the trigger results in the execution of a 1D transfer. "2": A trigger results in the execution of the current descriptor. "3": A trigger results in the execution of the current descriptor and continues (without requiring another input trigger) with the execution of the next descriptor using the next descriptor's information. [5:4] TR_OUT_TYPE Specifies when an output trigger is generated: "0": An output trigger is

		generated after a single transfer. "1": An output trigger is generated after a single 1D transfer. - If the descriptor type is "single", the output trigger is generated after a single transfer. - If the descriptor type is "1D", "CRC" or "2D", the output trigger is generated after the execution of a 1D transfer. "2": An output trigger is generated after the execution of the current descriptor. "3": An output trigger is generated after the execution of a descriptor list: after the execution of the current descriptor AND the current descriptor DESCR_NEXT_PTR.ADDR is "0'. [7:6] TR_IN_TYPE Specifies the input trigger type (not to be confused with the descriptor type): "0": A trigger results in the execution of a single transfer. The descriptor type can be single, 1D or 2D. "1": A trigger results in the execution of a single 1D transfer. - If the descriptor type is "single", the trigger results in the execution of a single transfer. - If the descriptor type is "1D" or "2D", the trigger results in the execution of a 1D transfer. "2": A trigger results in the execution of the current descriptor. "3": A trigger results in the execution of the current descriptor and continues (without requiring another input trigger) with the execution of the next descriptor using the next descriptor's information. [24] CH_DISABLE Specifies whether the channel is disabled or not after completion of the current descriptor (independent of the value of the DESCR_NEXT_PTR value): '0': Channel is not disabled. '1': Channel is disabled. Note: a disabled channel will ignore its input trigger. [26] SRC_TRANSFER_SIZE Specifies the bus transfer size to the source location: '0': As specified by DATA_SIZE. '1': Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus

		transfer size, but only provides a 16-bit data element. [27] DST_TRANSFER_SIZE Specifies the bus transfer size to the destination location: '0': As specified by DATA_SIZE. '1': Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. [29:28] DATA_SIZE Specifies the data element size: "0": Byte (8 bits). "1": Halfword (16 bits). "2": Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit. - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit. - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made "0"). - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made "0"). - DATA is 16 bit, SRC is 16 bit, DST is 16 bit. - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit. - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made "0"). - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made "0"). - DATA is 32 bit, SRC is 32 bit, DST is 32 bit. [31:30] DESCR_TYPE Specifies the descriptor type (not to be confused with the trigger type): "0": Single transfer. The DESCR_X_CTL and DESCR_Y_CTL registers are not present and DESCR_NEXT_PTR is at offset 0x0c. "1": 1D transfer. The DESCR_X_CTL register is present, the DESCR_Y_CTL is not present and DESCR_NEXT_PTR is at offset 0x10. A 1D transfer consists out of DESCR_X_CTL.X_COUNT single transfers. "2": 2D transfer. The DESCR_X_CTL and DESCR_Y_CTL registers are present and DESCR_NEXT_PTR is at offset 0x14.

		A 2D transfer consists of DESCR_X_CTL.X_COUNT*DESCR_Y_CTL.Y_COUNT single transfers. "3": CRC transfer. The DESCR_X_CTL register is present, theDESCR_Y_CTL is not present and DESCR_NEXT_PTR is at offset 0x10. A CRC transfer consists out of DESCR_X_CTL.X_COUNT single transfers. After the execution of the current descriptor, the DESCR_NEXT_PTR address is copied to the channel's CH_CURR_PTR address and CH_STATUS.X_IDX and CH_STATUS.Y_IDX are set to "0". Default Value: Undefined

DW0_ACT_DESCR_SRC0

Active descriptor source
Address: 0x40280024
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Copy of DESCR_SRC of the currently active descriptor. Base address of source location. Default Value: Undefined

DW0_ACT_DESCR_DST0

Active descriptor destination
Address: 0x40280028
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Copy of DESCR_DST of the currently active descriptor. Base address of destination location. Note: For a CRC transfer descriptor, this field should be programmed with the address of the CRC_LFSR_CTL register. The calculated CRC LFSR state is written to this address (through the CRYPTO AHB-Lite master interface) when the input trigger is processed. The write transfer will be submitted to the CPUSS and PERI protection schemes. Default Value: Undefined

DW0_ACT_DESCR_X_CTL0

Active descriptor X loop control
Address: 0x40280030
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description

31 : 0	DATA	Copy of DESCR_X_CTL of the currently active descriptor. [11:0] SRC_X_INCR Specifies increment of source address for each X loop iteration (in multiples of SRC_TRANSFER_SIZE). This field is a signed number in the range [-2048, 2047]. If this field is "0", the source address is not incremented. This is useful for reading from RX FIFO structures. [23:12] DST_X_INCR Specifies increment of destination address for each X loop iteration (in multiples of DST_TRANSFER_SIZE). This field is a signed number in the range [-2048, 2047]. If this field is "0", the destination address is not incremented. This is useful for writing to TX FIFO structures. Note: this field is not used for CRC transfer descriptors and must be set to "0". [31:24] X_COUNT Number of iterations (minus 1) of the "X loop" (X_COUNT+1 is the number of single transfers in a 1D transfer). This field is an unsigned number in the range [0, 255], representing 1 through 256 iterations. For a single transfer descriptor type, descriptor will not have X_CTL. Default Value: Undefined

DW0_ACT_DESCR_Y_CTL0

Active descriptor Y loop control
Address: 0x40280034
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Copy of DESCR_Y_CTL of the currently active descriptor. [11:0] SRC_Y_INCR Specifies increment of source address for each Y loop iteration (in multiples of SRC_TRANSFER_SIZE). This field is a signed number in the range [-2048, 2047]. [23:12] DST_Y_INCR Specifies increment of destination address for each Y loop iteration (in multiples of DST_TRANSFER_SIZE). This field is a signed number in the range [-2048, 2047]. [31:24] Y_COUNT Number of iterations (minus 1) of the "Y loop" (X_COUNT+1)*(Y_COUNT+1) is the number of single transfers in a 2D transfer). This field is an unsigned number in the range [0, 255], representing 1 through 256 iterations. For single, 1D and CRC transfer descriptor types, descriptor will not have Y_CTL. Default Value: Undefined

DW0_ACT_DESCR_NEXT_PTR0

Active descriptor next pointer
Address: 0x40280038
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 2	ADDR	Copy of DESCR_NEXT_PTR of the currently active descriptor. [31:2] ADDR Address of next descriptor in descriptor list. When this field is "0", this is the last descriptor in the descriptor list. Default Value: Undefined

DW0_ACT_SRC0

Active source
Address: 0x40280040
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SRC_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SRC_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	SRC_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	SRC_ADDR [31:24]							

Bits	Name	Description
31 : 0	SRC_ADDR	Current address of source location. Default Value: Undefined

DW0_ACT_DST0

Active destination
Address: 0x40280044
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DST_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DST_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DST_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DST_ADDR [31:24]							

Bits	Name	Description
31 : 0	DST_ADDR	Current address of destination location. Default Value: Undefined

DW0_ECC_CTL0

ECC control
Address: 0x40280080
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WORD_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						WORD_ADDR [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							None
HW Access	R							None
Name	PARITY [31:25]							None

Bits	Name	Description
31 : 25	PARITY	ECC parity to use for ECC error injection at address WORD_ADDR. Default Value: 0
9 : 0	WORD_ADDR	Specifies the word address where an error will be injected. - On a write transfer to this SRAM word address and when CTL.ECC_INJ_EN bit is '1', the parity (PARITY) is injected. Default Value: 0

DW0_CRC_CTL0

CRC control
Address: 0x40280100
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							DATA_REVERSE

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							REM_REVERSE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	REM_REVERSE	Specifies whether the remainder is bit reversed (reversal is performed after XORing): '0': No. '1': Yes. Default Value: 0
0	DATA_REVERSE	Specifies the bit order in which a data Byte is processed (reversal is performed after XORing): '0': Most significant bit (bit 1) first. '1': Least significant bit (bit 0) first. Default Value: 0

DW0_CRC_DATA_CTL0

CRC data control
Address: 0x40280110
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA_XOR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA_XOR	Specifies a byte mask with which each data byte is XOR'd. The XOR is performed before data reversal. Default Value: 0

DW0_CRC_POL_CTL0

CRC polynomial control
Address: 0x40280120
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [31:24]							

Bits	Name	Description
31 : 0	POLYNOMIAL	CRC polynomial. The polynomial is represented WITHOUT the high order bit (this bit is always assumed '1'). The polynomial should be aligned/shifted such that the more significant bits (bit 31 and down) contain the polynomial and the less significant bits (bit 0 and up) contain padding '0's. Some frequently used polynomials: - CRC32: POLYNOMIAL is 0x04c11db7 (x^32 + x^26 + x^23 + x^22 + x^16 + x^12 + x^11 + x^10 + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1). - CRC16: POLYNOMIAL is 0x80050000 (x^16 + x^15 + x^2 + 1, shifted by 16 bit positions). - CRC16 CCITT: POLYNOMIAL is 0x10210000 (x^16 + x^12 + x^5 + 1, shifted by 16 bit positions). Default Value: 0

DW0_CRC_LFSR_CTL0

CRC LFSR control
Address: 0x40280130
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	LFSR32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	LFSR32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	LFSR32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	LFSR32 [31:24]							

Bits	Name	Description
31 : 0	LFSR32	State of a 32-bit Linear Feedback Shift Registers (LFSR) that is used to implement CRC. This register needs to be initialized by SW to provide the CRC seed value. The seed value should be aligned such that the more significant bits (bit 31 and down) contain the seed value and the less significant bits (bit 0 and up) contain padding '0's. Note that SW can write this field. This functionality can be used prevent information leakage (through either CRC_LFSR_CTL or CRC_REM_RESULT). Default Value: 0

DW0_CRC_REM_CTL0

CRC remainder control
Address: 0x40280140
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	REM_XOR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	REM_XOR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	REM_XOR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	REM_XOR [31:24]							

Bits	Name	Description
31 : 0	REM_XOR	Specifies a mask with which the CRC_LFSR_CTL.LFSR32 register is XOR'd to produce a remainder. The XOR is performed before remainder reversal. Default Value: 0

DW0_CRC_REM_RESULT0

CRC remainder result
Address: 0x40280148
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	REM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	REM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	REM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	REM [31:24]							

Bits	Name	Description
31 : 0	REM	Remainder value. The alignment of the remainder depends on CRC_REM_CTL0.REM_REVERSE: '0': the more significant bits (bit 31 and down) contain the remainder. '1': the less significant bits (bit 0 and up) contain the remainder. Note: This field is combinatorially derived from CRC_LFSR_CTL.LFSR32, CRC_CTL.REM_REVERSE and CRC_REM_CTL.REM_XOR. Default Value: 0

DW0_CH_STRUCT0_CH_CTL

Channel control
Address: 0x40288000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				None	RW	RW	RW
HW Access	R				None	R	R	R
Name	PC [7:4]				None	B	NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	None	RW	
HW Access	None				R	None	R	
Name	None [15:12]				PREEMPTABLE	None	PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW1C	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	Channel enable: '0': Disabled. The channel's trigger is ignored and the channel cannot be made pending and therefore cannot be made active. If a pending channel is disabled, the channel is made non pending. If the activate channel is disabled, the channel is de-activated (bus transactions are completed). '1': Enabled. SW sets this field to '1' to enable a specific channel. HW sets this field to '0' on an error interrupt cause (the specific error is specified by CH_STATUS.INTR_CAUSE). Default Value: 0

11	PREEMPTABLE	Specifies if the channel is preemptable. '0': Not preemptable. '1': Preemptable. This field allows higher priority pending channels (from a higher priority group; i.e. an active channel can NOT be preempted by a pending channel in the same priority group) to preempt the active channel in between "single transfers" (a 1D transfer consists out of X_COUNT single transfers; a 2D transfer consists out of X_COUNT*Y_COUNT single transfers). Preemption will NOT affect the pending status of channel. As a result, after completion of a higher priority activated channel, the current channel may be reactivated. Default Value: Undefined
9 : 8	PRIO	Channel priority: "0": highest priority. "1" "2" "3": lowest priority. Channels with the same priority constitute a priority group. Priority decoding determines the highest priority pending channel. This channel is determined as follows. First, the highest priority group with pending channels is identified. Second, within this priority group, round robin arbitration is applied. Round robin arbitration (within a priority group) gives the highest priority to the lower channel indices (within the priority group). Default Value: 0
7 : 4	PC	Protection context. This field is set with the protection context of the transaction that writes this register; i.e. the 'write data' is ignored and instead the context is inherited from the write transaction (note the field attributes should be HW:RW, SW:R). All transactions for this channel uses the PC field for the protection context. Default Value: Undefined

2	B	Non-bufferable/bufferable access control: '0': non-bufferable. '1': bufferable. This field is used to indicate to an AMBA bridge that a write transaction can complete without waiting for the destination to accept the write transaction data. All transactions for this channel uses the B field for the non-bufferable/bufferable access control ("hprot[2]"). Default Value: Undefined
1	NS	Secure/on-secure access control: '0': secure. '1': non-secure. This field is set with the secure/ non-secure access control of the transaction that writes this register; i.e. the 'write data' is ignored and instead the access control is inherited from the write transaction (note the field attributes should be HW:RW, SW:R). All transactions for this channel use the NS field for the secure/non-secure access control ("hprot[4]"). Default Value: Undefined
0	P	User/privileged access control: '0': user mode. '1': privileged mode. This field is set with the user/privileged access control of the transaction that writes this register; i.e. the 'write data' is ignored and instead the access control is inherited from the write transaction (note the field attributes should be HW:RW, SW:R). All transactions for this channel use the P field for the user/privileged access control ("hprot[1]"). Default Value: Undefined

DW0_CH_STRUCT0_CH_STATUS

Channel status
Address: 0x40288004
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				INTR_CAUSE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	PENDING	None [30:24]						

Bits	Name	Description
31	PENDING	Specifies pending DW channels; i.e. enabled channels whose trigger got activated. This field includes all channels that are in the pending state (not scheduled) or active state (scheduled and performing data transfer(s)). Default Value: 0
3 : 0	INTR_CAUSE	Specifies the source of the interrupt cause: "0": No interrupt generated "1": Interrupt based on transfer complettion configuration based on INTR_TYPE "2": Source transfer bus error "3": Destination transfer bus error "4": Source address misalignment "5": Destination address misalignment "6": Current descriptor pointer is null "7": Active channel is disabled "8": Descriptor bus error "9"-"15": Not used. For error related interrupt causes (INTR_CAUSE is "2", "3", ..., "8"), the channel is disabled (HW sets CH_CTL.ENABLED to '0'). Default Value: Undefined

DW0_CH_STRUCT0_CH_IDX

Channel current indices
Address: 0x40288008
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	X_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	Y_IDX [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	Y_IDX	Specifies the Y loop index, with X_COUNT taken from the current descriptor. Note: HW sets this field to "0" when it updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor. Note: SW should set this field to "0" when it updates CH_CURR_PTR. Default Value: Undefined
7 : 0	X_IDX	Specifies the X loop index. In the range of [0, X_COUNT], with X_COUNT taken from the current descriptor. Note: HW sets this field to "0" when it updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor. Note: SW should set this field to "0" when it updates CH_CURR_PTR. Default Value: Undefined

DW0_CH_STRUCT0_CH_CURR_PTR

Channel current descriptor pointer
Address: 0x4028800C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	RW						None	
Name	ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 2	ADDR	Address of current descriptor. When this field is "0", there is no valid descriptor. Note: HW updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor. Note: Typically, when SW updates the current descriptor pointer CH_CURR_PTR, it also sets CH_IDX.X_IDX and CH_IDX.Y_IDX to "0". Default Value: Undefined

DW0_CH_STRUCT0_INTR

Interrupt
Address: 0x40288010
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							CH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CH	Set to '1', when event (as specified by CH_STATUS.INTR_CAUSE) is detected. Write INTR.CH field with '1', to clear bit. Write INTR_SET.CH field with '1', to set bit. Default Value: 0

DW0_CH_STRUCT0_INTR_SET

Interrupt set
Address: 0x40288014
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							CH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CH	Write INTR_SET field with '1' to set corresponding INTR.CH field (a write of '0' has no effect). Default Value: 0

DW0_CH_STRUCT0_INTR_MASK

Interrupt mask
Address: 0x40288018
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							CH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CH	Mask for corresponding field in INTR register. Default Value: 0

DW0_CH_STRUCT0_INTR_MASKED

Interrupt masked
Address: 0x4028801C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							CH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CH	Logical and of corresponding INTR and INTR_MASK fields. Default Value: 0

DW0_CH_STRUCT0_SRAM_DATA0

SRAM data 0
Address: 0x40288020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Default Value: Undefined

DW0_CH_STRUCT0_SRAM_DATA1

SRAM data 1
Address: 0x40288024
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Default Value: Undefined

DW0_CH_STRUCT0_TR_CMD

Channel software trigger
Address: 0x40288028
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							ACTIVATE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	ACTIVATE	Software trigger. When written with '1', a trigger is generated which sets 'trigger pending' (only if the channel is enabled). A read always returns a 0. Default Value: 0

DW1_STATUS0

Status
Address: 0x40290004
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None	R	R	R
HW Access	RW				None	RW	RW	RW
Name	PC [7:4]				None	B	NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	None	R	
HW Access	None				W	None	W	
Name	None [15:12]				PREEMPTABLE	None	PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		R					
HW Access	None		W					
Name	None [23:22]		CH_IDX [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	R	R			None			
HW Access	W	W			None			
Name	ACTIVE	STATE [30:28]			None [27:24]			

Bits	Name	Description
31	ACTIVE	Active channel present: '0': No. '1': Yes. Default Value: 0
30 : 28	STATE	State of the DW controller. "0": Default/inactive state. "1": Loading descriptor. "2": Loading data element from source location. "3": Storing data element to destination location. "4": CRC functionality (only used for CRC transfer descriptor type). "5": Update of active control information (e.g. source and destination addresses) and wait for trigger de-activation. "6": Error. Default Value: 0
21 : 16	CH_IDX	Active channel index. Default Value: Undefined
11	PREEMPTABLE	Active channel preemptable. Default Value: Undefined
9 : 8	PRIO	Active channel priority. Default Value: Undefined

7 : 4	PC	Active channel protection context. Default Value: Undefined
2	B	Active channel, non-bufferable/ bufferable access control: '0': non-bufferable '1': bufferable. Default Value: Undefined
1	NS	Active channel, secure/non-secure access control: '0': secure. '1': non-secure. Default Value: Undefined
0	P	Active channel, user/privileged access control: '0': user mode. '1': privileged mode. Default Value: Undefined

DMAC_CTL

Control

Address: 0x402A0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	IP enable: '0': Disabled. All non-retention registers (command and status registers) are reset to their default value when the IP is disabled. All retention registers retain their value when the IP is disabled. '1': Enabled. Default Value: 0
		0x0: DISABLED :
		0x1: ENABLED :

DMAC_ACTIVE

Active channels
Address: 0x402A0008
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				ACTIVE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	ACTIVE	Specifies active channels; i.e. enabled channels whose trigger got activated. Default Value: 0

DMAC_CH0_CTL

Channel control
Address: 0x402A1000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				None	RW	RW	RW
HW Access	R				None	R	R	R
Name	PC [7:4]				None	B	NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW1C	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	Channel enable: '0': Disabled. The channel's trigger is ignored and the channel cannot be made pending and therefore cannot be made active. If a pending channel is disabled, the channel is made non pending. If the activate channel is disabled, the channel is de-activated (bus transactions are completed). '1': Enabled. SW sets this field to '1' to enable a specific channel. HW sets this field to '0' when an error interrupt cause is activated. Default Value: 0

9 : 8	PRIO	Channel priority: "0": highest priority. "1" "2" "3": lowest priority. Channels with the same priority constitute a priority group and within this priority group, the following "roundrobin" arbitration is applied. A "round" consists of a contiguous sequence of channel activations, within this priority group, without any repetition. Within a round, higher priority is given to the lower channel indices. The notion of a round guarantees that within a group, higher channel indices do not yield to lower indices indefinitely. Default Value: 0
7 : 4	PC	Protection context. This field is set with the protection context of the transaction that writes this register; i.e. the context is inherited from the write transaction and not specified by the transaction write data. All transactions for this channel uses the PC field for the protection context. Default Value: 0
2	B	Non-bufferable/bufferable access control: '0': non-bufferable. '1': bufferable. This field is used to indicate to an AMBA bridge that a write transaction can complete without waiting for the destination to accept the write transaction data. All transactions for this channel uses the B field for the non-bufferable/bufferable access control. Default Value: 0
1	NS	Secure/on-secure access control: '0': secure. '1': non-secure. This field is set with the secure/non-secure access control of the transaction that writes this register; i.e. the access control is inherited from the write transaction and not specified by the transaction write data. All transactions for this channel use the NS field for the secure/non-secure access control. Default Value: 1

0	P	User/privileged access control: '0': user mode. '1': privileged mode. This field is set with the user/ privileged access control of the transaction that writes this register; i.e. the access control is inherited from the write transaction and not specified by the transaction write data. All transactions for this channel use the P field for the user/ privileged access control. Default Value: 0

DMAC_CH0_IDX

Channel current indices
Address: 0x402A1010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	X [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	X [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	Y [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	Y [31:24]							

Bits	Name	Description
31 : 16	Y	Specifies the Y loop index, with Y_COUNT taken from the current descriptor. Note: HW sets this field to "0" when it loads a descriptor.. Default Value: Undefined
15 : 0	X	Specifies the X loop index. In the range of [0, X_COUNT], with X_COUNT taken from the current descriptor. Note: HW sets this field to "0" when it loads a descriptor. Default Value: Undefined

DMAC_CH0_SRC

Channel current source address
Address: 0x402A1014
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Current address of source location. Default Value: Undefined

DMAC_CH0_DST

Channel current destination address
Address: 0x402A1018
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Current address of destination location. Default Value: Undefined

DMAC_CH0_CURR

Channel current descriptor pointer
Address: 0x402A1020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	RW						None	
Name	PTR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	PTR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	PTR [31:24]							

Bits	Name	Description
31 : 2	PTR	Address of current descriptor. When this field is "0", there is no valid descriptor. Note: HW updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor. Default Value: Undefined

DMAC_CH0_TR_CMD

Channle software trigger
Address: 0x402A1028
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							ACTIVATE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	ACTIVATE	Software trigger. When written with '1', a trigger is generated which sets 'trigger pending' (only if the channel is enabled). A read always returns a 0. Default Value: 0

DMAC_CH0_DESCR_STATUS

Channel descriptor status
Address: 0x402A1040
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	Indicates whether the descriptor information present in DESCR_CTL, DESCR_SRC, DESCR_DST, DESCR_X_SIZE, DESCR_X_INCR, DESCR_Y_SIZE, DESCR_Y_INCR, DESCR_NEXT status registers is valid or not. Default Value: 0

DMAC_CH0_DESCR_CTL

Channel descriptor control
Address: 0x402A1060
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R		R		R	
HW Access	W		W		W		W	
Name	TR_IN_TYPE [7:6]		TR_OUT_TYPE [5:4]		INTR_TYPE [3:2]		WAIT_FOR_DEACT [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							DATA_PREFETCH

Bits	23	22	21	20	19	18	17	16
SW Access	None						R	
HW Access	None						W	
Name	None [23:18]						DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None	R			R	R	None	R
HW Access	None	W			W	W	None	W
Name	None	DESCR_TYPE [30:28]			DST_TRANSFER_SIZE	SRC_TRANSFER_SIZE	None	CH_DISABLE

Bits	Name	Description

30 : 28	DESCR_TYPE	Specifies the descriptor type (not to be confused with the trigger type): "0": Single transfer. The DESCR_X_SIZE, DESCR_X_INCR, DESCR_Y_SIZE and DESCR_Y_INCR registers are NOT present. The DESCR_NEXT_PTR is at offset 0x0c. "1": 1D transfer. The DESCR_X_SIZE and DESCR_X_INCR registers are present, the DESCR_Y_SIZE and DESCR_Y_INCR are NOT present. A 1D transfer consists out of DESCR_X_SIZE.X_COUNT+1 single transfers. The DESCR_NEXT_PTR is at offset 0x14. "2": 2D transfer. The DESCR_X_SIZE, DESCR_X_INCR, DESCR_Y_SIZE and DESCR_Y_INCR registers are present. A 2D transfer consists of (DESCR_X_SIZE.X_COUNT+1)*(DESCR_Y_SIZE.Y_COUNT+1) single transfers. The DESCR_NEXT_PTR is at offset 0x1c. "3": Memory copy. The DESCR_X_SIZE register is present, the DESCR_X_INCR, DESCR_Y_SIZE and DESCR_Y_INCR are NOT present. A memory copy transfer copies DESCR_X_SIZE.X_COUNT+1 Bytes and may use Byte, halfword and word transfers. The DESCR_NEXT_PTR is at offset 0x10. "4": Scatter transfer. The DESCR_X_SIZE register is present, the DESCR_DST, DESCR_X_INCR, DESCR_Y_SIZE and DESCR_Y_INCR are NOT present. "5"-"7": Undefined. After the execution of the current descriptor, the DESCR_NEXT_PTR address is copied to the channel's CH_CURR_PTR address and CH_STATUS.X_IDX and CH_STATUS.Y_IDX are set to "0". Default Value: Undefined

27	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: '0': As specified by DATA_SIZE. '1': Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Note: this field is not used for a "memory copy" descriptor type. Note: this field must be set to '1' for a "scatter" descriptor type. Default Value: Undefined
26	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: '0': As specified by DATA_SIZE. '1': Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Note: this field is not used for a "memory copy" descriptor type. Note: this field must be set to '1' for a "scatter" descriptor type. Default Value: Undefined
24	CH_DISABLE	Specifies whether the channel is disabled or not after completion of the current descriptor (independent of the value of the DESCR_NEXT_PTR value): '0': Channel is not disabled. '1': Channel is disabled. Default Value: Undefined

17 : 16	DATA_SIZE	Specifies the data element size: "0": Byte (8 bits). "1": Halfword (16 bits). "2": Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit. - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit. - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made "0"). - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made "0"). - DATA is 16 bit, SRC is 16 bit, DST is 16 bit. - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit. - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made "0"). - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made "0"). - DATA is 32 bit, SRC is 32 bit, DST is 32 bit. Note: this field is not used for a "memory copy" descriptor type. Note: this field must be set to "2" for a "initialization" descriptor type. Default Value: Undefined
8	DATA_PREFETCH	Source data prefetch: '0': No source data prefetch. Source data transfers are only initiated AFTER the input trigger is activated. '1': Source data prefetch. Source data transfers are initiated as soon as the channel is enabled, the current descriptor pointer is NOT "0" and there is space available in the channel's data FIFO. When the input trigger is activated, the trigger can initiate destination data transfers with data that is already in the channel's data FIFO. This effectively shortens the initial delay of the data transfer. Note: data prefetch should be used with care, to ensure that data coherency is guaranteed and that prefetches do not cause undesired side effects. Default Value: Undefined

7 : 6	TR_IN_TYPE	Specifies the input trigger type (not to be confused with the descriptor type): "0": A trigger results in the execution of a single transfer. The descriptor type can be single, 1D or 2D. "1": A trigger results in the execution of a single 1D transfer. - If the descriptor type is "single", the trigger results in the execution of a single transfer. - If the descriptor type is "1D" or "2D", the trigger results in the execution of a 1D transfer. - If the descriptor type is "memory copy", the trigger results in the execution of a memory copy transfer. - If the descriptor type is "scatter", the trigger results in the execution of an scatter transfer. "2": A trigger results in the execution of the current descriptor. "3": A trigger results in the execution of the current descriptor and continues (without requiring another input trigger) with the execution of the next descriptor using the next descriptor's information. Default Value: Undefined
5 : 4	TR_OUT_TYPE	Specifies when an output trigger is generated: "0": An output trigger is generated after a single transfer. "1": An output trigger is generated after a single 1D transfer or a memory copy transfer. - If the descriptor type is "single", the output trigger is generated after a single transfer. - If the descriptor type is "1D" or "2D", the output trigger is generated after the execution of a 1D transfer. - If the descriptor type is "memory copy", the output trigger is generated after the execution of a memory copy transfer. - If the descriptor type is "scatter", the output trigger is generated after the execution of a scatter transfer. "2": An output trigger is generated after the execution of the current descriptor. "3": An output trigger is generated after the execution of a descriptor list: after the execution of the current descriptor AND the current descriptor's DESCR_NEXT_PTR.ADDR is "0'. Default Value: Undefined

3 : 2	INTR_TYPE	Specifies when a completion interrupt is generated (CH_STATUS.INTR_CAUSE is set to COMPLETION): "0": An interrupt is generated after a single transfer. "1": An interrupt is generated after a single 1D transfer or a memory copy transfer - If the descriptor type is "single", the interrupt is generated after a single transfer. - If the descriptor type is "1D" or "2D", the interrupt is generated after the execution of a 1D transfer. - If the descriptor type is "memory copy", the interrupt is generated after the execution of a memory copy transfer. - If the descriptor type is "scatter" the interrupt is generated after the execution of a scatter transfer. "2": An interrupt is generated after the execution of the current descriptor (independent of the value of DESCR_NEXT_PTR.ADDR of the current descriptor). "3": An interrupt is generated after the execution of the current descriptor and the current descriptor's DESCR_NEXT_PTR.ADDR is "0'. Default Value: Undefined

1 : 0	WAIT_FOR_DEACT	Specifies whether the controller should wait for the input trigger to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controller with the agent that generated the trigger. This field is ONLY used at the completion of the transfer as specified by TR_IN. E.g., a TX FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the controller AND received by the agent. Furthermore, the agent's trigger may be delayed by a few cycles before it reaches the controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW controller performance. "0": Do not wait for trigger de-activation (for pulse sensitive triggers). "1": Wait for up to 4 cycles. "2": Wait for up to 16 cycles. "3": Wait indefinitely. This option may result in controller lockup if the trigger is not de-activated. Default Value: Undefined

DMAC_CH0_DESCR_SRC

Channel descriptor source
Address: 0x402A1064
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. Default Value: Undefined

DMAC_CH0_DESCR_DST

Channel descriptor destination
Address: 0x402A1068
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. Default Value: Undefined

DMAC_CH0_DESCR_X_SIZE

Channel descriptor X size
Address: 0x402A106C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	X_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	X_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	X_COUNT	Number of iterations (minus 1) of the "X loop" (X_COUNT+1 is the number of single transfers in a 1D transfer). This field is an unsigned number in the range [0, 65535], representing 1 through 65536 iterations. For the "memory copy" descriptor type, (X_COUNT + 1) is the number of transferred Bytes. For the "scatter" descriptor type, ceiling(X_COUNT/2) is the number of (address, write data) initialization pairs processed. Default Value: Undefined

DMAC_CH0_DESCR_X_INCR

Channel descriptor X increment
Address: 0x402A1070
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SRC_X [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SRC_X [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DST_X [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DST_X [31:24]							

Bits	Name	Description
31 : 16	DST_X	Specifies increment of destination address for each X loop iteration (in multiples of DST_TRANSFER_SIZE). This field is a signed number (sign-magnitude format) in the range [-32768, 32767]. If this field is "0", the destination address is not incremented. This is useful for writing to TX FIFO structures. Default Value: Undefined
15 : 0	SRC_X	Specifies increment of source address for each X loop iteration (in multiples of SRC_TRANSFER_SIZE). This field is a signed number (sign-magnitude format) in the range [-32768, 32767]. If this field is "0", the source address is not incremented. This is useful for reading from RX FIFO structures. Default Value: Undefined

DMAC_CH0_DESCR_Y_SIZE

Channel descriptor Y size
Address: 0x402A1074
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	Y_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	Y_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	Y_COUNT	Number of iterations (minus 1) of the "Y loop" (X_COUNT+1)*(Y_COUNT+1) is the number of single transfers in a 2D transfer). This field is an unsigned number in the range [0, 65535], representing 1 through 65536 iterations. Default Value: Undefined

DMAC_CH0_DESCR_Y_INCR

Channel descriptor Y increment
Address: 0x402A1078
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SRC_Y [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SRC_Y [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DST_Y [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DST_Y [31:24]							

Bits	Name	Description
31 : 16	DST_Y	Specifies increment of destination address for each Y loop iteration (in multiples of DST_TRANSFER_SIZE). This field is a signed number in the range [-32768, 32767]. Default Value: Undefined
15 : 0	SRC_Y	Specifies increment of source address for each Y loop iteration (in multiples of SRC_TRANSFER_SIZE). This field is a signed number in the range [-32768, 32767]. Default Value: Undefined

DMAC_CH0_DESCR_NEXT

Channel descriptor next pointer
Address: 0x402A107C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	PTR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	PTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	PTR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	PTR [31:24]							

Bits	Name	Description
31 : 2	PTR	Address of next descriptor in descriptor list. When this field is "0", this is the last descriptor in the descriptor list. Default Value: Undefined

DMAC_CH0_INTR

Interrupt
Address: 0x402A1080
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	DESCR_BUS_ERROR	ACTIVE_CH_DISABLED	CURR_PTR_NULL	DST_MISAL	SRC_MISAL	DST_BUS_ERROR	SRC_BUS_ERROR	COMPLETION

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DESCR_BUS_ERROR	Activated (set to '1') on a bus error for a load of the descriptor. Default Value: 0
6	ACTIVE_CH_DISABLED	Activated (set to '1') if the channel is disabled by SW (accidentally/ incorrectly) when the data transfer engine is busy. Default Value: 0
5	CURR_PTR_NULL	Activated (set to '1') when the channel is enabled (CH_CTL.ENABLED is '1') and CH_CURR_PTR is "0". Default Value: 0
4	DST_MISAL	Activated (set to '1') on a misalignment of the destination address. Default Value: 0
3	SRC_MISAL	Activated (set to '1') on a misalignment of the source address. Default Value: 0

2	DST_BUS_ERROR	Activated (set to '1') on a bus error for a store to the destination. Default Value: 0
1	SRC_BUS_ERROR	Activated (set to '1') on a bus error for a load from the source. Default Value: 0
0	COMPLETION	Activated (set to '1') on completion of data transfer(s) as specified by the descriptor's CH_DESCR_CTL.INTR_TYPE. Default Value: 0

DMAC_CH0_INTR_SET

Interrupt set
Address: 0x402A1084
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	DESCR_BUS_ERROR	ACTIVE_CH_DISABLED	CURR_PTR_NULL	DST_MISAL	SRC_MISAL	DST_BUS_ERROR	SRC_BUS_ERROR	COMPLETION

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DESCR_BUS_ERROR	Write this field with '1' to set INTR.DESCR_BUS_ERROR field to '1' (a write of '0' has no effect). Default Value: 0
6	ACTIVE_CH_DISABLED	Write this field with '1' to set INTR.ACT_CH_DISABLED field to '1' (a write of '0' has no effect). Default Value: 0
5	CURR_PTR_NULL	Write this field with '1' to set INTR.CURR_PTR_NULL field to '1' (a write of '0' has no effect). Default Value: 0
4	DST_MISAL	Write this field with '1' to set INTR.DST_MISAL field to '1' (a write of '0' has no effect). Default Value: 0
3	SRC_MISAL	Write this field with '1' to set INTR.SRC_MISAL field to '1' (a write of '0' has no effect). Default Value: 0

2	DST_BUS_ERROR	Write this field with '1' to set INTR.DST_BUS_ERROR field to '1' (a write of '0' has no effect). Default Value: 0
1	SRC_BUS_ERROR	Write this field with '1' to set INTR.SRC_BUS_ERROR field to '1' (a write of '0' has no effect). Default Value: 0
0	COMPLETION	Write this field with '1' to set INTR.COMPLETION field to '1' (a write of '0' has no effect). Default Value: 0

DMAC_CH0_INTR_MASK

Interrupt mask
Address: 0x402A1088
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	DESCR_BUS_ERROR	ACTIVE_CH_DISABLED	CURR_PTR_NULL	DST_MISAL	SRC_MISAL	DST_BUS_ERROR	SRC_BUS_ERROR	COMPLETION

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DESCR_BUS_ERROR	Mask for INTR.DESCR_BUS_ERROR interrupt. Default Value: 0
6	ACTIVE_CH_DISABLED	Mask for INTR.ACTIVE_CH_DISABLED interrupt. Default Value: 0
5	CURR_PTR_NULL	Mask for INTR.CURR_PTR_NULL interrupt. Default Value: 0
4	DST_MISAL	Mask for INTR.DST_MISAL interrupt. Default Value: 0
3	SRC_MISAL	Mask for INTR.SRC_MISAL interrupt. Default Value: 0
2	DST_BUS_ERROR	Mask for INTR.DST_BUS_ERROR interrupt. Default Value: 0
1	SRC_BUS_ERROR	Mask for INTR.SRC_BUS_ERROR interrupt. Default Value: 0
0	COMPLETION	Mask for INTR.COMPLETION interrupt. Default Value: 0

DMAC_CH0_INTR_MASKED

Interrupt masked
Address: 0x402A108C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DESCR_BUS_ERROR	ACTIVE_CH_DISABLED	CURR_PTR_NULL	DST_MISAL	SRC_MISAL	DST_BUS_ERROR	SRC_BUS_ERROR	COMPLETION

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DESCR_BUS_ERROR	Logical and of corresponding INTR.DESCR_BUS_ERROR and INTR_MASK.DESCR_BUS_ERROR fields. Default Value: 0
6	ACTIVE_CH_DISABLED	Logical and of corresponding INTR.ACTIVE_CH_DISABLED and INTR_MASK.ACTIVE_CH_DISABLED fields. Default Value: 0
5	CURR_PTR_NULL	Logical and of corresponding INTR.CURR_PTR_NULL and INTR_MASK.CURR_PTR_NULL fields. Default Value: 0
4	DST_MISAL	Logical and of corresponding INTR.DST_MISAL and INTR_MASK.DST_MISAL fields. Default Value: 0
3	SRC_MISAL	Logical and of corresponding INTR.SRC_MISAL and INTR_MASK.SRC_MISAL fields. Default Value: 0

2	DST_BUS_ERROR	Logical and of corresponding INTR.DST_BUS_ERROR and INTR_MASK.DST_BUS_ERROR fields. Default Value: 0
1	SRC_BUS_ERROR	Logical and of corresponding INTR.SRC_BUS_ERROR and INTR_MASK.SRC_BUS_ERROR fields. Default Value: 0
0	COMPLETION	Logical and of corresponding INTR.COMPLETION and INTR_MASK.COMPLETION fields. Default Value: 0

5 FLASH

Register details

Register name	Address	Description
FLASHC_FLASH_CTL	0x40240000	Control
FLASHC_FLASH_PWR_CTL	0x40240004	Flash power control
FLASHC_FLASH_CMD	0x40240008	Command
FLASHC_ECC_CTL	0x402402A0	ECC control
FLASHC_FM_SRAM_ECC_CTL0	0x402402B0	eCT Flash SRAM ECC control 0
FLASHC_FM_SRAM_ECC_CTL1	0x402402B4	eCT Flash SRAM ECC control 1
FLASHC_FM_SRAM_ECC_CTL2	0x402402B8	eCT Flash SRAM ECC control 2
FLASHC_FM_SRAM_ECC_CTL3	0x402402BC	eCT Flash SRAM ECC control 3
FLASHC_CM0_CA_CTL0	0x40240400	CM0+ cache control
FLASHC_CM0_CA_CTL1	0x40240404	CM0+ cache control
FLASHC_CM0_CA_CTL2	0x40240408	CM0+ cache control
FLASHC_CM0_CA_STATUS0	0x40240440	CM0+ cache status 0
FLASHC_CM0_CA_STATUS1	0x40240444	CM0+ cache status 1
FLASHC_CM0_CA_STATUS2	0x40240448	CM0+ cache status 2
FLASHC_CM0_STATUS	0x40240460	CM0+ interface status
FLASHC_CM4_CA_CTL0	0x40240480	CM4 cache control
FLASHC_CM4_CA_CTL1	0x40240484	CM4 cache control
FLASHC_CM4_CA_CTL2	0x40240488	CM4 cache control
FLASHC_CM4_CA_STATUS0	0x402404C0	CM4 cache status 0
FLASHC_CM4_CA_STATUS1	0x402404C4	CM4 cache status 1
FLASHC_CM4_CA_STATUS2	0x402404C8	CM4 cache status 2
FLASHC_CM4_STATUS	0x402404E0	CM4 interface status
FLASHC_CRYPTO_BUFF_CTL	0x40240500	Cryptography buffer control
FLASHC_DW0_BUFF_CTL	0x40240580	Datawire 0 buffer control
FLASHC_DW1_BUFF_CTL	0x40240600	Datawire 1 buffer control
FLASHC_DMAC_BUFF_CTL	0x40240680	DMA controller buffer control
FLASHC_FM_CTL	0x4024F000	Flash Macro Control
FLASHC_FM_CODE_MARGIN	0x4024F004	Flash Macro Margin Mode on Code Flash
FLASHC_FM_ADDR	0x4024F008	Flash Macro Address
FLASHC_INTR	0x4024F020	Interrupt
FLASHC_INTR_SET	0x4024F024	Interrupt Set
FLASHC_INTR_MASK	0x4024F028	Interrupt Mask
FLASHC_INTR_MASKED	0x4024F02C	Interrupt Masked
FLASHC_ECC_OVERRIDE	0x4024F030	ECC Data In override information and control bits

Register name	Address	Description
FLASHC_FM_DATA	0x4024F040	Flash macro data_in[31 to 0] both Code and Work Flash
FLASHC_BOOKMARK	0x4024F064	Bookmark register - keeps the current FW HV seq
FLASHC_MAIN_FLASH_SAFETY	0x4024F400	Main (Code) Flash Security enable
FLASHC_STATUS	0x4024F404	Status read from Flash Macro
FLASHC_WORK_FLASH_SAFETY	0x4024F500	Work Flash Security enable

5.1 FLASH registers

FLASHC_FLASH_CTL

Control

Address: 0x40240000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				MAIN_WS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	None		RW	RW
HW Access	None		R	R	None		R	R
Name	None [15:14]		WORK_BANK_MODE	MAIN_BANK_MODE	None [11:10]		WORK_MAP	MAIN_MAP

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW	RW	RW	None	RW	RW	RW
HW Access	None	R	R	R	None	R	R	R
Name	None	WORK_ERR_SILENT	WORK_ECC_INJ_EN	WORK_ECC_EN	None	MAIN_ERR_SILENT	MAIN_ECC_INJ_EN	MAIN_ECC_EN

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

22	WORK_ERR_SILENT	Specifies bus transfer behavior for a non-recoverable error on the FLASH macro work interface (either a non-correctable ECC error, a FLASH macro work interface internal error, a FLASH macro work interface memory hole access): 0: Bus transfer has a bus error. 1: Bus transfer does NOT have a bus error; i.e. the error is "silent" In either case, the erroneous FLASH macro data is returned by the bus master interface. The erroneous data is NOT placed in a bus master interface's cache and/or buffer. This field is ONLY used by CPU (and debug i.e. SYS_AP/ CM0_AP/CM4_AP) bus transfers. Non-CPU bus transfers always have a bus transfer with a bus error, in case of a non-recoverable error. Note: All CPU bus masters have dedicated status registers (CM0_STATUS and CM4_STATUS) to register the occurrence of FLASH macro work interface internal errors (non-correctable ECC errors and memory hole errors are NOT registered). Note: fault reporting can be used to identify the error that occurred: - FLASH macro work interface internal error. - FLASH macro work interface non-recoverable ECC error. - FLASH macro work interface recoverable ECC error. - FLASH macro work interface memory hole error. Default Value: 0
21	WORK_ECC_INJ_EN	Enable error injection for FLASH work interface. When"1", the parity (ECC_CTL.PARITY[6:0]) is used for a load from the ECC_CTL.WORD_ADDR[23:0] word address. Default Value: 0
20	WORK_ECC_EN	Enable ECC checking for FLASH work interface: 0: Disabled. ECC checking/reporting on FLASH work interface is disabled. No correctable or non-correctable faults are reported. 1: Enabled. Default Value: 1

18	MAIN_ERR_SILENT	Specifies bus transfer behavior for a non-recoverable error on the FLASH macro main interface (either a non-correctable ECC error, a FLASH macro main interface internal error, a FLASH macro main interface memory hole access): 0: Bus transfer has a bus error. 1: Bus transfer does NOT have a bus error; i.e. the error is "silent" In either case, the erroneous FLASH macro data is returned by the bus master interface. The erroneous data is NOT placed in a bus master interface's cache and/or buffer. This field is ONLY used by CPU (and debug i.e. SYS_AP/ CM0_AP/CM4_AP) bus transfers. Non-CPU bus transfers always have a bus transfer with a bus error, in case of a non-recoverable error. Note: All CPU bus masters have dedicated status registers (CM0_STATUS and CM4_STATUS) to register the occurrence of FLASH macro main interface internal errors (non-correctable ECC errors and memory hole errors are NOT registered). Note: fault reporting can be used to identify the error that occurred: - FLASH macro main interface internal error. - FLASH macro main interface non-recoverable ECC error. - FLASH macro main interface recoverable ECC error. - FLASH macro main interface memory hole error. Default Value: 0
17	MAIN_ECC_INJ_EN	Enable error injection for FLASH main interface. When"1", the parity (ECC_CTL.PARITY[7:0]) is used for a load from the ECC_CTL.WORD_ADDR[23:0] word address. Default Value: 0
16	MAIN_ECC_EN	Enable ECC checking for FLASH main interface: 0: Disabled. ECC checking/reporting on FLASH main interface is disabled. No correctable or non-correctable faults are reported. 1: Enabled. Default Value: 1
13	WORK_BANK_MODE	Specifies bank mode of FLASH macro work array. 0: Single bank mode. 1: Dual bank mode. Default Value: 0

12	MAIN_BANK_MODE	Specifies bank mode of FLASH macro main array. 0: Single bank mode. 1: Dual bank mode. Default Value: 0
9	WORK_MAP	Specifies mapping of FLASH macro work array. 0: Mapping A. 1: Mapping B. This field is only used when WORK_BANK_MODE is "1" (dual bank mode). Default Value: 0
8	MAIN_MAP	Specifies mapping of FLASH macro main array. 0: Mapping A. 1: Mapping B. This field is only used when MAIN_BANK_MODE is "1" (dual bank mode). Default Value: 0
3 : 0	MAIN_WS	FLASH macro main interface wait states: "0": 0 wait states. ... "15": 15 wait states Default Value: 0

FLASHC_FLASH_PWR_CTL

Flash power control
Address: 0x40240004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						ENABLE_HV	ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	ENABLE_HV	Enables HV power to the flash memory Default Value: 1
0	ENABLE	Enables power to the flash memory Default Value: 1

FLASHC_FLASH_CMD

Command
Address: 0x40240008
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						RW1C	RW1C
Name	None [7:2]						BUFF_INV	INV

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	BUFF_INV	Invalidation of ALL buffers (does not invalidate the caches). SW writes a "1" to clear the buffers. HW sets this field to "0" when the operation is completed. The operation takes a maximum of three clock cycles on the slowest of the clk_slow and clk_fast clocks. Note: the caches only capture FLASH macro main array data. Therefore, invalidating just the buffers (BUFF_INV) does not invalidate captures main array data in the caches. Default Value: 0

0	INV	Invalidation of ALL caches (for CM0+ and CM4) and ALL buffers. SW writes a "1" to clear the caches. HW sets this field to "0" when the operation is completed. The operation takes a maximum of three clock cycles on the slowest of the clk_slow and clk_fast clocks. The caches' LRU structures are also reset to their default state. Default Value: 0

FLASHC_ECC_CTL

ECC control
Address: 0x402402A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WORD_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WORD_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	WORD_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	PARITY [31:24]							

Bits	Name	Description
31 : 24	PARITY	ECC parity to use for ECC error injection at address WORD_ADDR. - For cache SRAM ECC, the 7-bit parity PARITY[6:0] is for a 32-bit word. - For FLASH main interface ECC, the 8-bit parity PARITY[7:0] is for a 64-bit word. - For FLASH work interface ECC, the 7-bit parity PARITY[6:0] is for a 32-bit word. Default Value: 0

23 : 0	WORD_ADDR	Specifies the word address where an error will be injected. - For cache SRAM ECC, the word address WORD_ADDR[23:0] is device address A[25:2]. On a FLASH macro refill to this word address and when the corresponding CM0/4_CA_CTL.RAM_ECC_INJ_EN bit is "1", the parity (PARITY[6:0]) is injected and stored in the cache. - For FLASH main interface ECC, the word address WORD_ADDR[23:0] is device address A[26:3]. On a FLASH main interface read and when FLASH_CTL.MAIN_ECC_INJ_EN bit is "1", the parity (PARITY[7:0]) replaces the FLASH macro parity (FLASH main interface read path is manipulated). - For FLASH work interface ECC, the word address WORD_ADDR[23:0] is device address A[25:2]. On a FLASH work interface read and when FLASH_CTL.WORK_ECC_INJ_EN bit is "1", the parity (PARITY[6:0]) replaces the FLASH macro parity (FLASH work interface read path is manipulated). Default Value: 0

FLASHC_FM_SRAM_ECC_CTL0

eCT Flash SRAM ECC control 0
Address: 0x402402B0
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ECC_INJ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ECC_INJ_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ECC_INJ_DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ECC_INJ_DATA [31:24]							

Bits	Name	Description
31 : 0	ECC_INJ_DATA	32-bit data for ECC error injection test of eCT Flash SRAM ECC logic. Default Value: 0

FLASHC_FM_SRAM_ECC_CTL1

eCT Flash SRAM ECC control 1
Address: 0x402402B4
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	ECC_INJ_PARITY [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 0	ECC_INJ_PARITY	7-bit parity for ECC error injection test of eCT Flash SRAM ECC logic. Default Value: 0

FLASHC_FM_SRAM_ECC_CTL2

eCT Flash SRAM ECC control 2
Address: 0x402402B8
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CORRECTED_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CORRECTED_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	CORRECTED_DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	CORRECTED_DATA [31:24]							

Bits	Name	Description
31 : 0	CORRECTED_DATA	32-bit corrected data output of the ECC syndrome logic. Default Value: 0

FLASHC_FM_SRAM_ECC_CTL3

eCT Flash SRAM ECC control 3
Address: 0x402402BC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None			RW
HW Access	None			RW1C	None			R
Name	None [7:5]			ECC_INJ_EN	None [3:1]			ECC_ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							ECC_TEST_FAIL

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	ECC_TEST_FAIL	Status of ECC test. 1 : ECC test failed because eCT Flash macro is busy and using the SRAM. 0: ECC was performed. Default Value: 0
4	ECC_INJ_EN	eCT Flash SRAM ECC error injection test enable. Follow the steps below for ECC logic test: 1. Write corrupted or uncorrupted 39-bit data to FM_SRAM_ECC_CTL0/1 registers. 2. Set the ECC_INJ_EN bit to "1". 3. Confirm that the bit ECC_TEST_FAIL is "0". If this is not the case, start over at item 1 because the eCT Flash was not idle. 4. Check the corrected data in FM_SRAM_ECC_CTL2. 5. Confirm that fault was reported to fault structure, and check syndrome (only applicable if corrupted data was written in step 1). 6. If not finished, start over at 1 with different data. Default Value: 0

0	ECC_ENABLE	ECC generation/check enable for eCT Flash SRAM memory. Default Value: 1

FLASHC_CM0_CA_CTL0

CM0+ cache control
Address: 0x40240400
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						RAM_ECC_INJ_EN	RAM_ECC_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WAY [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None			RW		
HW Access	R	R	None			R		
Name	CA_EN	PREF_EN	None [29:27]			SET_ADDR [26:24]		

Bits	Name	Description
31	CA_EN	Cache enable: 0: Disabled. The cache tag valid bits are reset to "0"s and the cache LRU information is set to "1"s (making way 0 the LRU way and way 3 the MRU way). 1: Enabled. Default Value: 1
30	PREF_EN	Prefetch enable: 0: Disabled. 1: Enabled. Prefetching requires the cache to be enabled; i.e. ENABLED is "1". Default Value: 1
26 : 24	SET_ADDR	Specifies the cache set for which cache information is provided in CM0_CA_STATUS0/1/2. Default Value: 0
17 : 16	WAY	Specifies the cache way for which cache information is provided in CM0_CA_STATUS0/1/2. Default Value: 0

1	RAM_ECC_INJ_EN	Enable error injection for cache. When "1", the parity (ECC_CTL.PARITY[6:0]) is used when a refill is done from the FLASH macro to the ECC_CTL.WORD_ADDR[23:0] word address. Default Value: 0
0	RAM_ECC_EN	Enable ECC checking for cache accesses: 0: Disabled. 1: Enabled. Default Value: 1

FLASHC_CM0_CA_CTL1

CM0+ cache control
Address: 0x40240404
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VECTKEYSTAT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VECTKEYSTAT [31:24]							

Bits	Name	Description
31 : 16	VECTKEYSTAT	Register key (to prevent accidental writes). - Should be written with a 0x05fa key value for the write to take effect. - Always reads as 0xfa05. Note: Although the SW attribute for this field says ''R', SW need to write the key 0x05fa in this field for this register write to happen. This is a built in protection provided to prevent accidental writes from SW. Default Value: 0xFA05

1 : 0	PWR_MODE	Specifies power mode for CM0 cache. The following sequnece should be followed for turning OFF/ON the cache SRAM. Turn OFF sequence: a) Write CM0_CA_CTL0 to disable cache. b) Write CM0_CA_CTL1 to turn OFF cache SRAM. Turn ON sequence: a) Write CM0_CA_CTL1 to turn ON cache SRAM. b) Delay to allow power up of cache SRAM. Delay should be at a minimum of CM0_CA_CTL2.PWRUP_DELAY CLK_SLOW clock cycles. c) Write CM0_CA_CTL0 to enable cache. Default Value: 3
		0x0: OFF : Power OFF the CM0 cache, no retain
		0x1: RESERVED : Undefined
		0x2: RETAINED : Put the CM0 cache in retained mode
		0x3: ENABLED : Enable/Turn ON the CM0 cache SRAM.

FLASHC_CM0_CA_CTL2

CM0+ cache control
Address: 0x40240408
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PWRUP_DELAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PWRUP_DELAY [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	PWRUP_DELAY	Number clock cycles delay needed after power domain power up Default Value: 0x12C

FLASHC_CM0_CA_STATUS0

CM0+ cache status 0
Address: 0x40240440
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VALID32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	VALID32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	VALID32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	VALID32 [31:24]							

Bits	Name	Description
31 : 0	VALID32	Sixteen valid bits of the cache line specified by CM0_CA_CTL.WAY and CM0_CA_CTL.SET_ADDR. Default Value: 0

FLASHC_CM0_CA_STATUS1

CM0+ cache status 1
Address: 0x40240444
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	TAG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	TAG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	TAG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	TAG [31:24]							

Bits	Name	Description
31 : 0	TAG	Cache line address of the cache line specified by CM0_CA_CTL.WAY and CM0_CA_CTL.SET_ADDR. Default Value: Undefined

FLASHC_CM0_CA_STATUS2

CM0+ cache status 2
Address: 0x40240448
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		W					
Name	None [7:6]		LRU [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	LRU	Six bit LRU representation of the cache set specified by CM0_CA_CTL.SET_ADDR. The encoding of the field is as follows ("X_LRU_Y" indicates that way X is Less Recently Used than way Y): Bit 5: 0_LRU_1: way 0 less recently used than way 1. Bit 4: 0_LRU_2. Bit 3: 0_LRU_3. Bit 2: 1_LRU_2. Bit 1: 1_LRU_3. Bit 0: 2_LRU_3. Default Value: Undefined

FLASHC_CM0_STATUS

CM0+ interface status
Address: 0x40240460
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						W1S	W1S
Name	None [7:2]						WORK_INTERNAL_ERR	MAIN_INTERNAL_ERR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	WORK_INTERNAL_ERR	See CM0_STATUS.MAIN_INTERNAL_ERROR. Default Value: 0
0	MAIN_INTERNAL_ERR	Specifies/registers the occurrence of a FLASH macro main interface internal error (typically the result of a read access while a program erase operation is ongoing) as a result of a CM0+ access (or debug access via SYS_AP/CM0_AP). SW clears this field to "0". HW sets this field to "1" on a FLASH macro main interface internal error. Typically, SW reads this field after a code section to detect the occurrence of an error. Note: this field is independent of FLASH_CTL.MAIN_ERR_SILENT. Default Value: 0

FLASHC_CM4_CA_CTL0

CM4 cache control
Address: 0x40240480
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						RAM_ECC_INJ_EN	RAM_ECC_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WAY [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None			RW		
HW Access	R	R	None			R		
Name	CA_EN	PREF_EN	None [29:27]			SET_ADDR [26:24]		

Bits	Name	Description
31	CA_EN	Cache enable: 0: Disabled. The cache tag valid bits are reset to "0"s and the cache LRU information is set to "1"s (making way 0 the LRU way and way 3 the MRU way). 1: Enabled. Default Value: 1
30	PREF_EN	Prefetch enable: 0: Disabled. 1: Enabled. Prefetching requires the cache to be enabled; i.e. ENABLED is "1". Default Value: 1
26 : 24	SET_ADDR	Specifies the cache set for which cache information is provided in CM4_CA_STATUS0/1/2. Default Value: 0
17 : 16	WAY	Specifies the cache way for which cache information is provided in CM4_CA_STATUS0/1/2. Default Value: 0
1	RAM_ECC_INJ_EN	See CM0_CA_CTL. Default Value: 0
0	RAM_ECC_EN	See CM0_CA_CTL. Default Value: 1

FLASHC_CM4_CA_CTL1

CM4 cache control
Address: 0x40240484
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VECTKEYSTAT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VECTKEYSTAT [31:24]							

Bits	Name	Description
31 : 16	VECTKEYSTAT	Register key (to prevent accidental writes). - Should be written with a 0x05fa key value for the write to take effect. - Always reads as 0xfa05. Note: Although the SW attribute for this field says ''R', SW need to write the key 0x05fa in this field for this register write to happen. This is a built in protection provided to prevent accidental writes from SW. Default Value: 0xFA05

1 : 0	PWR_MODE	Specifies power mode for CM4 cache. The following sequnece should be followed for truning OFF/ON the cache SRAM. Turn OFF sequence: a) Write CM4_CA_CTL0 to disable cache. b) Write CM4_CA_CTL1 to turn OFF cache SRAM. Turn ON sequence: a) Write CM4_CA_CTL1 to turn ON cache SRAM. b) Delay to allow power up of cache SRAM. Delay should be at a minimum of CM4_CA_CTL2.PWRUP_DELAY CLK_SLOW clock cycles. c) Write CM4_CA_CTL0 to enable cache. Default Value: 3
		0x0: OFF : Power OFF the CM4 cache, not retained.
		0x1: RESERVED : Undefined
		0x2: RETAINED : Put the CM4 cache in retained mode.
		0x3: ENABLED : Enable/Turn ON the CM4 cache.

FLASHC_CM4_CA_CTL2

CM4 cache control
Address: 0x40240488
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PWRUP_DELAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PWRUP_DELAY [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	PWRUP_DELAY	Number clock cycles delay needed after power domain power up Default Value: 0x12C

FLASHC_CM4_CA_STATUS0

CM4 cache status 0
Address: 0x402404C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VALID32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	VALID32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	VALID32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	VALID32 [31:24]							

Bits	Name	Description
31 : 0	VALID32	See CM0_CA_STATUS0. Default Value: 0

FLASHC_CM4_CA_STATUS1

CM4 cache status 1
Address: 0x402404C4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	TAG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	TAG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	TAG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	TAG [31:24]							

Bits	Name	Description
31 : 0	TAG	See CM0_CA_STATUS1. Default Value: Undefined

FLASHC_CM4_CA_STATUS2

CM4 cache status 2
Address: 0x402404C8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		W					
Name	None [7:6]		LRU [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	LRU	See CM0_CA_STATUS2. Default Value: Undefined

FLASHC_CM4_STATUS

CM4 interface status
Address: 0x402404E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						W1S	W1S
Name	None [7:2]						WORK_INTERNAL_ERR	MAIN_INTERNAL_ERR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	WORK_INTERNAL_ERR	See CM4_STATUS.MAIN_INTERNAL_ERROR. Default Value: 0
0	MAIN_INTERNAL_ERR	Specifies/registers the occurrence of a FLASH macro main interface internal error (typically the result of a read access while a program erase operation is ongoing) as a result of a CM4 access (or debug access via SYS_AP/CM4_AP). SW clears this field to "0". HW sets this field to "1" on a FLASH macro main interface internal error. Typically, SW reads this field after a code section to detect the occurrence of an error. Note: this field is independent of FLASH_CTL.MAIN_ERR_SILENT. Default Value: 0

FLASHC_CRYPTO_BUFF_CTL

Cryptography buffer control
Address: 0x40240500
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW	None					
HW Access	None	R	None					
Name	None	PREF_EN	None [29:24]					

Bits	Name	Description
30	PREF_EN	Prefetch enable: 0: Disabled. 1: Enabled. A prefetch will be done when there is read "hit" on the last 32-bit word of the buffer. For eCT work Flash, prefetch will not be done. Default Value: 1

FLASHC_DW0_BUFF_CTL

Datawire 0 buffer control
Address: 0x40240580
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW	None					
HW Access	None	R	None					
Name	None	PREF_EN	None [29:24]					

Bits	Name	Description
30	PREF_EN	See CRYPTO_BUFF_CTL. Default Value: 1

FLASHC_DW1_BUFF_CTL

Datawire 1 buffer control
Address: 0x40240600
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW	None					
HW Access	None	R	None					
Name	None	PREF_EN	None [29:24]					

Bits	Name	Description
30	PREF_EN	See CRYPTO_BUFF_CTL. Default Value: 1

FLASHC_DMAC_BUFF_CTL

DMA controller buffer control
Address: 0x40240680
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW	None					
HW Access	None	R	None					
Name	None	PREF_EN	None [29:24]					

Bits	Name	Description
30	PREF_EN	See CRYPTO_BUFF_CTL. Default Value: 1

FLASHC_FM_CTL

Flash Macro Control
Address: 0x4024F000
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			FM_MODE [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	EMB_START	None [30:24]						

Bits	Name	Description
31	EMB_START	"0": not active "1": starts the actual embedded operation Default Value: 0

4 : 0	FM_MODE	Flash macro mode selection: d0: Read/Idle - Normal mode, read array enabled d1: Not Used - the 1st analog POR is done by enable/enable_hv d2 - POR FUR Download - Downloads critical Flash initialization data from OTP (BG, rd, redu, etc....) d3 - POR IRAM MMR Download - Downloads from OTP region the MMR / IRAM into to the 8051 RDL shadows d4 - POR SW Download - Downloads from OTP region the SW code into to the 8051 MCU SRAM d5 - POR Code_Work Prepare - Loads the Code and Work Flash MG's to be ready for user mode operation d6 - Not Used d7 - Program 32b (WORK) - Used as program confirm command for 32 (Work) bits program d8 - Program 64b (CODE) - Used as program confirm command for 64 (Code) bits program d9 - Program 256b (CODE) - Used as program confirm command for 256 (Code) bits program d10: Program Page (CODE) - Used as program confirm command for page program for Code flash d11: Not Used d12 - Sector Erase - Erase for all kinds of sectors (Code/Work/SMS) d13 - Blank check Entry (UBC) d14 - Blank Check Read 32bit (WORK) - Blank check mode d15 - Blank check Exit d16 - Not Used d17 - Erase Suspend - Suspend command to the Erase operation d18 - Erase Resume - Resume command to Erase suspended operation d19 - Not Used d20- Not Used d21- Not Used d22- Not Used d23- Not Used d24- Not Used d25- Not Used d26- Not Used d27- Not Used d28- Not Used d29- Not Used d30: Not Used d31: Not Used Default Value: 0

FLASHC_FM_CODE_MARGIN

Flash Macro Margin Mode on Code Flash
Address: 0x4024F004
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MARGIN_DCS_TRIM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW						RW	RW
HW Access	R						R	R
Name	MARGIN_RDREG_TRIM [15:10]						MARGIN_DCS_TRIM_EN	MARGIN_DCS_TRIM

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	None				
HW Access	R	R	R	None				
Name	MARGIN_MODE_EN	MARGIN_MODE_RDREG_CHNG_EN	MARGIN_PGM_ERS_B	None [28:24]				

Bits	Name	Description
31	MARGIN_MODE_EN	when set puts the s40ect Flash IP In Margin mode Default Value: 0
30	MARGIN_MODE_RDREG_CHNG_EN	when set will also use the MARGIN_RDREG_TRIM from above. Default is not to use Default Value: 0
29	MARGIN_PGM_ERS_B	0: ERS Margin is checked 1: PGM Margin is checked Default Value: 0
15 : 10	MARGIN_RDREG_TRIM	rdreg_c trim to be used in Margin mode if enabled by MARGIN_MODE_RDREG_CHNG_EN Default Value: 14
9	MARGIN_DCS_TRIM_EN	0: internal device defaults used from Margin reads reference current 1: MARGIN_DCS_TRIM configuration is used during Margin read Default Value: 0

8 : 0	MARGIN_DCS_TRIM	see above table to set the DCS reference current value to be used during Margin mode. (default set to 5uS = 0x143) which gives a Margin to the Erase side. 7uA would probably be used for Margin to the PGM side Default Value: 323

FLASHC_FM_ADDR

Flash Macro Address
Address: 0x4024F008
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	FM_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	FM_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	FM_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	FM_ADDR [31:24]							

Bits	Name	Description
31 : 0	FM_ADDR	Code or Work Flash Address to be used during write operations (PGM/ ERS) Default Value: 0

FLASHC_INTR

Interrupt
Address: 0x4024F020
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INTR	Set to "1", when event is detected. Write INTR field with "1", to clear bit. Write INTR_SET field with "1", to set bit. Default Value: 0

FLASHC_INTR_SET

Interrupt Set
Address: 0x4024F024
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							INTR_SET

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INTR_SET	Write INTR_SET field with "1" to set corresponding INTR field (a write of "0" has no effect). Default Value: 0

FLASHC_INTR_MASK

Interrupt Mask
Address: 0x4024F028
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							INTR_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INTR_MASK	Mask for corresponding field in the INTR register Default Value: 0

FLASHC_INTR_MASKED

Interrupt Masked
Address: 0x4024F02C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							INTR_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INTR_MASKED	Logical and of corresponding request and mask fields. Default Value: 0

FLASHC_ECC_OVERRIDE

ECC Data In override information and control bits
Address: 0x4024F030
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	ECC_OVERRIDE_SYNDROME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W	W	None					
HW Access	R	R	None					
Name	ECC_OVERRIDE_CODE	ECC_OVERRIDE_WORK	None [29:24]					

Bits	Name	Description
31	ECC_OVERRIDE_CODE	0: no override. Using internal ECC engine to calculate the ECC of the Code Flash Default Value: 0
30	ECC_OVERRIDE_WORK	0: no override. Using internal ECC engine to calculate the ECC of the Work Flash Default Value: 0
7 : 0	ECC_OVERRIDE_SYNDROME	The override syndrome itself to be used in case one of the enables are set. It will take [7:0] in the case of Code flash and [6:0] in the case of work flash, to bypass the internal generated syndrome Default Value: 0

FLASHC_FM_DATA

Flash macro data_in[31 to 0] both Code and Work Flash
Address: 0x4024F040
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	RW							
Name	FM_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	RW							
Name	FM_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	RW							
Name	FM_DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	RW							
Name	FM_DATA [31:24]							

Bits	Name	Description
31 : 0	FM_DATA	Pgm command data in going to the internal write buffer (WBUF). Default Value: 0

FLASHC_BOOKMARK

Bookmark register - keeps the current FW HV seq
Address: 0x4024F064
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BOOKMARK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	BOOKMARK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	BOOKMARK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	BOOKMARK [31:24]							

Bits	Name	Description
31 : 0	BOOKMARK	Used by FW. Keeps the Current HV cycle sequence Default Value: 0

FLASHC_MAIN_FLASH_SAFETY

Main (Code) Flash Security enable
Address: 0x4024F400
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							MainFlashWriteEnable

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	MainFlashWriteEnable	"0": Main Flash embedded operations are blocked "1": Main Flash embedded operations are enabled Default Value: 0

FLASHC_STATUS

Status read from Flash Macro
Address: 0x4024F404
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R	R	R	R	R	R	R
HW Access	None	W	W	W	W	W	W	W
Name	None	BLANK_CHCEK_PASS	BLANK_CHECK_WORK	ERS_SUSPEND	ERASE_WORK	ERASE_CODE	PGM_WORK	PGM_CODE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	R	R	None		
HW Access	W	W	W	W	W	None		
Name	BUSY	HANG	NATIVE_POR	POR_2b_ECC_ERROR	POR_1b_ECC_CORRECTED	None [26:24]		

Bits	Name	Description
31	BUSY	Whenever the device is in embedded mode the RDY goes low. Should be the same as c_interrupt pin of the IP (but inverted) 1: busy in embedded 0: rdy (high also in erase suspend) Default Value: 1
30	HANG	After embedded operation (pgm/erase) this flag will tell if it was successful or failed 0: PASS 1: FAIL Default Value: 0
29	NATIVE_POR	Indicates a Native Flash state (UV) or sorted one. Valid only after 2nd phase of POR (FUR DOWNLOAD). Comment: not a retained flop, therefore reset (rst_hf_act_n) puts it back to 0. If Set it is not cleaned till additional POR (rst_hf_ac_t) 0: SORTED DEVICE (Non - Native) 1: NATIVE Default Value: 0

28	POR_2b_ECC_ERROR	Indicates an internal ECC error of 2b while downloading info in POR from NVM to VM. Valid after 2nd, 3rd and 4th POR phases (FUR, IREM & MMR, SW DOWNLOAD). If Set it is not cleaned till additional POR (rst_hf_ac_t) 0: No error 1: ECC 2b Error in POR Default Value: 0
27	POR_1b_ECC_CORRECTED	Indicates internal ECC found 1b error while downloading info in POR from NVM to VM and fixed it. Valid after 2nd, 3rd and 4th POR phases (FUR, IREM & MMR, SW DOWNLOAD). If Set it is not cleaned till additional POR (rst_hf_ac_t) 0: No error 1: 1b ECC Error corrected in POR Default Value: 0
6	BLANK_CHCEK_PASS	Indicates the Blank check command result is PASS (Blank) 0: Not Blank 1: Blank (PASS) Default Value: 0
5	BLANK_CHECK_WORK	Indicates if Blank Check mode is currently running on the work flash 0: not running 1: running Default Value: 0
4	ERS_SUSPEND	Indicates if Erase operation (Code/ Work) is currently being suspended 0: not suspended 1: suspended Default Value: 0
3	ERASE_WORK	Indicates if active Erase operation to the Work flash is taking place 0: not running 1: running Default Value: 0
2	ERASE_CODE	Indicates if active Erase operation to the Code flash is taking place 0: not running 1: running Default Value: 0
1	PGM_WORK	Indicates if active PGM operation to the Work flash is taking place 0: not running 1: running Default Value: 0
0	PGM_CODE	Indicates if active PGM operation to the Code flash is taking place 0: not running 1: running Default Value: 0

FLASHC_WORK_FLASH_SAFETY

Work Flash Security enable
Address: 0x4024F500
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							WorkFlashWriteEnable

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	WorkFlashWriteEnable	0: Work Flash embedded operations are blocked 1: Work Flash embedded operations are enabled Default Value: 0

6 Supervisory Flash (SFLASH)

Register details

Register name	Address	Description
SFLASH_SI_REVISION_ID	0x17000001	Indicates Silicon Revision ID of the device
SFLASH_SILICON_ID	0x17000002	Indicates Silicon ID of the device
SFLASH_SFLASH_SVN	0x170000A8	SFLASH Subversion
SFLASH_FB_FLAGS	0x170001FC	Flash boot flags
SFLASH_EPASS_TEMP_TRIM_TEMP_ROOMSORT	0x1700064E	On Chip temperature measured using external currents and external ADC at ROOM
SFLASH_EPASS_TEMP_TRIM_DIODE_ROOMSORT	0x17000650	Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at ROOM
SFLASH_EPASS_TEMP_TRIM_VBG_ROOMSORT	0x17000652	Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at ROOM
SFLASH_EPASS_TEMP_TRIM_TEMP_COLDSORT	0x17000654	On Chip temperature measured using external currents and external ADC at COLD
SFLASH_EPASS_TEMP_TRIM_DIODE_COLDSORT	0x17000656	Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at COLD
SFLASH_EPASS_TEMP_TRIM_VBG_COLDSORT	0x17000658	Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at COLD
SFLASH_EPASS_TEMP_TRIM_TEMP_HOTCLASS	0x1700065A	On Chip temperature measured using external currents and external ADC at HOT
SFLASH_EPASS_TEMP_TRIM_DIODE_HOTCLASS	0x1700065C	Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at HOT
SFLASH_EPASS_TEMP_TRIM_VBG_HOTCLASS	0x1700065E	Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at HOT
SFLASH_EPASS_TEMP_TRIM_DIODE_ROOMSORT_5V	0x1700066A	Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at ROOM
SFLASH_EPASS_TEMP_TRIM_VBG_ROOMSORT_5V	0x1700066C	Temperature sensor calibration data for VDDA=5V, Bandgap voltage at ROOM
SFLASH_EPASS_TEMP_TRIM_DIODE_COLDSORT_5V	0x1700066E	Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at COLD
SFLASH_EPASS_TEMP_TRIM_VBG_COLDSORT_5V	0x17000670	Temperature sensor calibration data for VDDA=5V, Bandgap voltage at COLD
SFLASH_EPASS_TEMP_TRIM_DIODE_HOTCLASS_5V	0x17000672	Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at HOT
SFLASH_EPASS_TEMP_TRIM_VBG_HOTCLASS_5V	0x17000674	Temperature sensor calibration data for VDDA=5V, Bandgap voltage at HOT
SFLASH_SRSS_PWR_OFFSET	0x17000730	SRSS_PWR_OFFSET
SFLASH_USER_FREE_ROW00	0x17000800	USER_FREE_ROW0. This is the starting address of a register bank containing 128 registers (SFLASH_USER_FREE_ROW00 to SFLASH_USER_FREE_ROW0127).

Register name	Address	Description
SFLASH_USER_FREE_ROW10	0x17000A00	USER_FREE_ROW1. This is the starting address of a register bank containing 128 registers (SFLASH_USER_FREE_ROW10 to SFLASH_USER_FREE_ROW1127).
SFLASH_USER_FREE_ROW20	0x17000C00	USER_FREE_ROW2. This is the starting address of a register bank containing 128 registers (SFLASH_USER_FREE_ROW20 to SFLASH_USER_FREE_ROW2127).
SFLASH_USER_FREE_ROW30	0x17000E00	USER_FREE_ROW3. This is the starting address of a register bank containing 128 registers (SFLASH_USER_FREE_ROW30 to SFLASH_USER_FREE_ROW3127).
SFLASH_SFLASH_UPDATE_MARKER0	0x17001800	Markers for storing SFLASH programming states
SFLASH_SFLASH_UPDATE_MARKER1	0x17001804	Markers for storing SFLASH programming states. See SFLASH_SFLASH_UPDATE_MARKER0 for the details of bit fields.
SFLASH_FLASH_BOOT_OBJECT_SIZE	0x17002000	Flash Boot - Object Size
SFLASH_FLASH_BOOT_APP_ID	0x17002004	Flash Boot - Application ID/Version
SFLASH_FLASH_BOOT_VERSION_LOW	0x17002018	Flash Boot - Version Low
SFLASH_FLASH_BOOT_FAMILY_ID	0x1700201C	Flash Boot - Family ID
SFLASH_PUBLIC_KEY0	0x17006400	Public key for signature verification (max RSA key size 4096). This is the starting address of a register bank containing 3072 registers (SFLASH_PUBLIC_KEY0 to SFLASH_PUBLIC_KEY3071).
SFLASH_APP_PROT_SETTINGS0	0x17007600	Application protection settings (4*128=512 bytes). This is the starting address of a register bank containing 128 registers (SFLASH_APP_PROT_SETTINGS0 to SFLASH_APP_PROT_SETTINGS127).
SFLASH_TOC2_OBJECT_SIZE	0x17007C00	Object size in bytes for CRC calculation starting from offset 0x00
SFLASH_TOC2_MAGIC_NUMBER	0x17007C04	Magic number(0x01211220)
SFLASH_TOC2_SMIF_CFG_STRUCT_ADDR	0x17007C08	Null terminated table of pointers representing the SMIF configuration structure
SFLASH_TOC2_FIRST_USER_APP_ADDR	0x17007C0C	Address of First User Application Object
SFLASH_TOC2_FIRST_USER_APP_FORMAT	0x17007C10	Format of First User Application Object. 0 - Basic, 1 - Cypress standard & 2 - Simplified
SFLASH_TOC2_SECOND_USER_APP_ADDR	0x17007C14	Address of Second User Application Object
SFLASH_TOC2_SECOND_USER_APP_FORMAT	0x17007C18	Format of Second User Application Object. 0 - Basic, 1 - Cypress standard & 2 - Simplified
SFLASH_TOC2_FIRST_CMx_1_USER_APP_ADDR	0x17007C1C	Address of First CM4 or CM7 core1 User Application Object

Register name	Address	Description
SFLASH_TOC2_SECOND_CMx_1_USER_APP_ADDR	0x17007C20	Address of Second CM4 or CM7 core1 User Application Object
SFLASH_TOC2_FIRST_CMx_2_USER_APP_ADDR	0x17007C24	Address of First CM4 or CM7 core2 User Application Object
SFLASH_TOC2_SECOND_CMx_2_USER_APP_ADDR	0x17007C28	Address of Second CM4 or CM7 core2 User Application Object
SFLASH_TOC2_SECURITY_UPDATES_MARKER	0x17007CFC	Marker for Security Updates
SFLASH_TOC2_SHASH_OBJECTS	0x17007D00	Number of additional objects to be verified for SECURE_HASH
SFLASH_TOC2_SIGNATURE_VERIF_KEY	0x17007D04	Address of signature verification key (0 if none).The object is signature specific key. It is the public key in case of RSA
SFLASH_TOC2_APP_PROTECTION_ADDR	0x17007D08	Address of Application Protection
SFLASH_TOC2_REVISION	0x17007DF4	Indicates TOC2 Revision. It is not used now.
SFLASH_TOC2_FLAGS	0x17007DF8	Controls default configuration

6.1 SFLASH registers

SFLASH_SI_REVISION_ID

Indicates Silicon Revision ID of the device
Address: 0x17000001
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	SI_REVISION_ID [7:0]							

Bits	Name	Description
7 : 0	SI_REVISION_ID	Silicon Revision ID Default Value: X

SFLASH_SILICON_ID

Indicates Silicon ID of the device
Address: 0x17000002
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	ID [15:8]							

Bits	Name	Description
15 : 0	ID	Silicon ID Default Value: X

SFLASH_SFLASH_SVN

SFLASH Subversion
Address: 0x170000A8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	SFLASH Subversion Default Value: 0

SFLASH_FB_FLAGS

Flash boot flags
Address: 0x170001FC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None							
Name	None [7:6]		FB_RSA4K_CTL [5:4]		FB_RSA3K_CTL [3:2]		FB_PIN_CTL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	FB_RSA4K_CTL	Determines if RSA-4K is supported. 2 = RSA-4K is supported. RSA public key modulo length should be in range 512 to 4096 bit. RSA4K already includes RSA3K option. The field FB_RSA3K_CTL must be set to 0. Others = RSA-4K is not supported. Default Value: 1
3 : 2	FB_RSA3K_CTL	Determines if RSA-3K is supported. 2 = RSA-3K is supported. RSA public key modulo length should be in range 512 to 3072 bit. The field FB_RSA4K_CTL must be set to 0. Others = RSA-3K is not supported. RSA public key modulo length should be in range 512 to 2048 bit. Default Value: 1
1 : 0	FB_PIN_CTL	Determines toggling a GPIO pin at the start and end of Flash boot 2 = Enable toggling a GPIO pin at the start and end of Flash boot Others = Disable toggling a GPIO pin at the start and end of Flash boot Default Value: 1

SFLASH_EPASS_TEMP_TRIM_TEMP_ROOMSORT

On Chip temperature measured using external currents and external ADC at ROOM
Address: 0x1700064E
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA16 [15:8]							

Bits	Name	Description
15 : 0	DATA16	On Chip temperature measured using external currents and external ADC at ROOM Default Value: X

SFLASH_EPASS_TEMP_TRIM_DIODE_ROOMSORT

Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at ROOM
Address: 0x17000650
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA16 [15:8]							

Bits	Name	Description
15 : 0	DATA16	Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at ROOM Default Value: X

SFLASH_EPASS_TEMP_TRIM_VBG_ROOMSORT

Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at ROOM
Address: 0x17000652
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA16 [15:8]							

Bits	Name	Description
15 : 0	DATA16	Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at ROOM Default Value: X

SFLASH_EPASS_TEMP_TRIM_TEMP_COLDSORT

On Chip temperature measured using external currents and external ADC at COLD
Address: 0x17000654
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA16 [15:8]							

Bits	Name	Description
15 : 0	DATA16	On Chip temperature measured using external currents and external ADC at COLD Default Value: X

SFLASH_EPASS_TEMP_TRIM_DIODE_COLDSORT

Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at COLD
Address: 0x17000656
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA16 [15:8]							

Bits	Name	Description
15 : 0	DATA16	Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at COLD Default Value: X

SFLASH_EPASS_TEMP_TRIM_VBG_COLDSORT

Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at COLD
Address: 0x17000658
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA16 [15:8]							

Bits	Name	Description
15 : 0	DATA16	Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at COLD Default Value: X

SFLASH_EPASS_TEMP_TRIM_TEMP_HOTCLASS

On Chip temperature measured using external currents and external ADC at HOT
Address: 0x1700065A
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA16 [15:8]							

Bits	Name	Description
15 : 0	DATA16	On Chip temperature measured using external currents and external ADC at HOT Default Value: X

SFLASH_EPASS_TEMP_TRIM_DIODE_HOTCLASS

Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at HOT
Address: 0x1700065C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA16 [15:8]							

Bits	Name	Description
15 : 0	DATA16	Temperature sensor calibration data for VDDA=3.3V, Temperature sensor diode voltage at HOT Default Value: X

SFLASH_EPASS_TEMP_TRIM_VBG_HOTCLASS

Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at HOT
Address: 0x1700065E
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA16 [15:8]							

Bits	Name	Description
15 : 0	DATA16	Temperature sensor calibration data for VDDA=3.3V, Bandgap voltage at HOT Default Value: X

SFLASH_EPASS_TEMP_TRIM_DIODE_ROOMSORT_5V

Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at ROOM
Address: 0x1700066A
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA16 [15:8]							

Bits	Name	Description
15 : 0	DATA16	Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at ROOM Default Value: X

SFLASH_EPASS_TEMP_TRIM_VBG_ROOMSORT_5V

Temperature sensor calibration data for VDDA=5V, Bandgap voltage at ROOM
Address: 0x1700066C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA16 [15:8]							

Bits	Name	Description
15 : 0	DATA16	Temperature sensor calibration data for VDDA=5V, Bandgap voltage at ROOM Default Value: X

SFLASH_EPASS_TEMP_TRIM_DIODE_COLDSORT_5V

Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at COLD
Address: 0x1700066E
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA16 [15:8]							

Bits	Name	Description
15 : 0	DATA16	Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at COLD Default Value: X

SFLASH_EPASS_TEMP_TRIM_VBG_COLDSORT_5V

Temperature sensor calibration data for VDDA=5V, Bandgap voltage at COLD
Address: 0x17000670
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA16 [15:8]							

Bits	Name	Description
15 : 0	DATA16	Temperature sensor calibration data for VDDA=5V, Bandgap voltage at COLD Default Value: X

SFLASH_EPASS_TEMP_TRIM_DIODE_HOTCLASS_5V

Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at HOT
Address: 0x17000672
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA16 [15:8]							

Bits	Name	Description
15 : 0	DATA16	Temperature sensor calibration data for VDDA=5V, Temperature sensor diode voltage at HOT Default Value: X

SFLASH_EPASS_TEMP_TRIM_VBG_HOTCLASS_5V

Temperature sensor calibration data for VDDA=5V, Bandgap voltage at HOT
Address: 0x17000674
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA16 [15:8]							

Bits	Name	Description
15 : 0	DATA16	Temperature sensor calibration data for VDDA=5V, Bandgap voltage at HOT Default Value: X

SFLASH_SRSS_PWR_OFFSET

SRSS_PWR_OFFSET
Address: 0x17000730
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None							
Name	None [7:5]			PMIC_VADJ_OFFSET [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None							
Name	None [15:13]			REGHC_TRANS_VADJ_OFFSET [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12 : 8	REGHC_TRANS_VADJ_OFFSET	Die-specific offset for VADJ when using REGHC with external transistor Default Value: X
4 : 0	PMIC_VADJ_OFFSET	Die-specific offset for VADJ when using it for feedback to an external PMIC Default Value: X

SFLASH_USER_FREE_ROW00

USER_FREE_ROW0
Address: 0x17000800
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

SFLASH_USER_FREE_ROW10

USER_FREE_ROW1
Address: 0x17000A00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

SFLASH_USER_FREE_ROW20

USER_FREE_ROW2
Address: 0x17000C00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

SFLASH_USER_FREE_ROW30

USER_FREE_ROW3
Address: 0x17000E00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

SFLASH_SFLASH_UPDATE_MARKER0

Markers for storing SFLASH programming states
Address: 0x17001800
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Marker which indicates SFLASH programming state Default Value: X

SFLASH_FLASH_BOOT_OBJECT_SIZE

Flash Boot - Object Size
Address: 0x17002000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

SFLASH_FLASH_BOOT_APP_ID

Flash Boot - Application ID/Version
Address: 0x17002004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	APP_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	APP_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	MINOR_VERSION [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW			
HW Access	None							
Name	None [31:28]				MAJOR_VERSION [27:24]			

Bits	Name	Description
27 : 24	MAJOR_VERSION	Default Value: X
23 : 16	MINOR_VERSION	Default Value: X
15 : 0	APP_ID	Default Value: X

SFLASH_FLASH_BOOT_VERSION_LOW

Flash Boot - Version Low
Address: 0x17002018
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

SFLASH_FLASH_BOOT_FAMILY_ID

Flash Boot - Family ID
Address: 0x1700201C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

SFLASH_PUBLIC_KEY0

Public key for signature verification (max RSA key size 4096)
Address: 0x17006400
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA [7:0]							

Bits	Name	Description
7 : 0	DATA	Default Value: X

SFLASH_APP_PROT_SETTINGS0

Application protection settings (4*128=512 bytes)
Address: 0x17007600
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

SFLASH_TOC2_OBJECT_SIZE

Object size in bytes for CRC calculation starting from offset 0x00
Address: 0x17007C00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

SFLASH_TOC2_MAGIC_NUMBER

Magic number(0x01211220)
Address: 0x17007C04
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

SFLASH_TOC2_SMIF_CFG_STRUCT_ADDR

Null terminated table of pointers representing the SMIF configuration structure
Address: 0x17007C08
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

SFLASH_TOC2_FIRST_USER_APP_ADDR

Address of First User Application Object
Address: 0x17007C0C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

SFLASH_TOC2_FIRST_USER_APP_FORMAT

Format of First User Application Object. 0 - Basic, 1 - Cypress standard & 2 - Simplified
Address: 0x17007C10
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

SFLASH_TOC2_SECOND_USER_APP_ADDR

Address of Second User Application Object
Address: 0x17007C14
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

SFLASH_TOC2_SECOND_USER_APP_FORMAT

Format of Second User Application Object. 0 - Basic, 1 - Cypress standard & 2 - Simplified
Address: 0x17007C18
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

SFLASH_TOC2_FIRST_CMx_1_USER_APP_ADDR

Address of First CM4 or CM7 core1 User Application Object
Address: 0x17007C1C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address of First CM4 or CM7 core1 User Application Object Default Value: X

SFLASH_TOC2_SECOND_CMx_1_USER_APP_ADDR

Address of Second CM4 or CM7 core1 User Application Object
Address: 0x17007C20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

SFLASH_TOC2_FIRST_CMx_2_USER_APP_ADDR

Address of First CM4 or CM7 core2 User Application Object
Address: 0x17007C24
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

SFLASH_TOC2_SECOND_CMx_2_USER_APP_ADDR

Address of Second CM4 or CM7 core2 User Application Object
Address: 0x17007C28
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

SFLASH_TOC2_SECURITY_UPDATES_MARKER

Marker for Security Updates
Address: 0x17007CFC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	This field is valid in flash boot version 3.1.0.556 and later. When marker is set to 0xFEDEEDDF the following PPUs will be configured during boot: - PERI_MS_PPU_FX_PERI_GR2_GROUP (Fixed PPU) - read only for all PCs; - Programmable PPU#11 configured to allow full access for the following region 0x40201000 - 0x4020100C. The HSM may overwrite the default configuration and reconfigure the PPU. - Programmable PPU#12 configured to allow full access for the CPUSS_ECC_CTL register (0x402013C8). The HSM may overwrite the default configuration and reconfigure the PPU. - Programmable PPU#13 configured to allow full access for the following region 0x40201300 - 0x402013C8. The HSM may overwrite the default configuration and reconfigure the PPU. Default Value: X

SFLASH_TOC2_SHASH_OBJECTS

Number of additional objects to be verified for SECURE_HASH
Address: 0x17007D00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

SFLASH_TOC2_SIGNATURE_VERIF_KEY

Address of signature verification key (0 if none).The object is signature specific key. It is the public key in case of RSA

Address: 0x17007D04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

SFLASH_TOC2_APP_PROTECTION_ADDR

Address of Application Protection
Address: 0x17007D08
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

SFLASH_TOC2_REVISION

Indicates TOC2 Revision. It is not used now.
Address: 0x17007DF4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Indicate TOC2 Revision Value: 0x0000_0000 and 0xFFFF_FFFF - default. Default Value: X

SFLASH_TOC2_FLAGS

Controls default configuration
Address: 0x17007DF8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW		RW			RW	
HW Access								
Name	APP_AUTH_CTL	SWJ_PINS_CTL [6:5]		LISTEN_WINDOW [4:2]			CLOCK_CONFIG [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		RW
HW Access	None							
Name	None [15:11]					FB_BOOTLOADER_CTL [10:9]		APP_AUTH_CTL

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 9	FB_BOOTLOADER_CTL	Determine if the internal bootloader in Flash boot is disabled: 0 = Internal bootloader is disabled. 1 = Internal bootloader is launched if the other bootloader conditions are met (default). 2 = Internal bootloader is disabled. 3 = Internal bootloader is disabled. Default Value: 1
8 : 7	APP_AUTH_CTL	Determines if the application image digital signature verification (authentication) is performed: 0 = Authentication is enabled (default). 1 = Authentication is disabled. 2 = Authentication is enabled (recommended). 3 = Authentication is enabled. Default Value: 0

6 : 5	SWJ_PINS_CTL	Determines if SWJ pins are configured in SWJ mode by Flash boot. Note: SWJ pins may be enabled later in the user code. 0 = Do not enable SWJ pins in Flash boot. Listen window is skipped. 1 = Do not enable SWJ pins in Flash boot. Listen window is skipped. 2 = Enable SWJ pins in Flash boot (default). 3 = Do not enable SWJ pins in Flash boot. Listen window is skipped. Default Value: 2
4 : 2	LISTEN_WINDOW	Determines the Listen window to allow sufficient time to acquire debug port. When CLOCK_CONFIG is set to 3, these window times are calculated assuming ROM boot clock is at 100MHz. 0 = 20 ms (Default) 1 = 10 ms 2 = 1 ms 3 = 0 ms (No Listen window) 4 = 100 ms Default Value: 0
1 : 0	CLOCK_CONFIG	Indicates clock frequency configuration. The clock should stay the same after Flash Boot execution. 0 = 8 MHz, IMO, no FLL 1 = 25 MHz, IMO + FLL 2 = 50 MHz, IMO + FLL 3 = Use ROM boot clocks configuration (default) Note: the default value is 2 for Flash boot version earlier than 556. Default Value: 3

7 Fault subsystem

Register details

Register name	Address	Description
FAULT_STRUCT0_CTL	0x40210000	Fault control
FAULT_STRUCT0_STATUS	0x4021000C	Fault status
FAULT_STRUCT0_DATA0	0x40210010	Fault data
FAULT_STRUCT0_DATA1	0x40210014	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT0_DATA2	0x40210018	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT0_DATA3	0x4021001C	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT0_PENDING0	0x40210040	Fault pending 0
FAULT_STRUCT0_PENDING1	0x40210044	Fault pending 1
FAULT_STRUCT0_PENDING2	0x40210048	Fault pending 2
FAULT_STRUCT0_MASK0	0x40210050	Fault mask 0
FAULT_STRUCT0_MASK1	0x40210054	Fault mask 1
FAULT_STRUCT0_MASK2	0x40210058	Fault mask 2
FAULT_STRUCT0_INTR	0x402100C0	Interrupt
FAULT_STRUCT0_INTR_SET	0x402100C4	Interrupt set
FAULT_STRUCT0_INTR_MASK	0x402100C8	Interrupt mask
FAULT_STRUCT0_INTR_MASKED	0x402100CC	Interrupt masked
FAULT_STRUCT1_CTL	0x40210100	Fault control. See FAULT_STRUCT0_CTL for the details of bit fields.
FAULT_STRUCT1_STATUS	0x4021010C	Fault status. See FAULT_STRUCT0_STATUS for the details of bit fields.
FAULT_STRUCT1_DATA0	0x40210110	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT1_DATA1	0x40210114	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT1_DATA2	0x40210118	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT1_DATA3	0x4021011C	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT1_PENDING0	0x40210140	Fault pending 0. See FAULT_STRUCT0_PENDING0 for the details of bit fields.
FAULT_STRUCT1_PENDING1	0x40210144	Fault pending 1. See FAULT_STRUCT0_PENDING1 for the details of bit fields.
FAULT_STRUCT1_PENDING2	0x40210148	Fault pending 2. See FAULT_STRUCT0_PENDING2 for the details of bit fields.
FAULT_STRUCT1_MASK0	0x40210150	Fault mask 0. See FAULT_STRUCT0_MASK0 for the details of bit fields.

Register name	Address	Description
FAULT_STRUCT1_MASK1	0x40210154	Fault mask 1. See FAULT_STRUCT0_MASK1 for the details of bit fields.
FAULT_STRUCT1_MASK2	0x40210158	Fault mask 2. See FAULT_STRUCT0_MASK2 for the details of bit fields.
FAULT_STRUCT1_INTR	0x402101C0	Interrupt. See FAULT_STRUCT0_INTR for the details of bit fields.
FAULT_STRUCT1_INTR_SET	0x402101C4	Interrupt set. See FAULT_STRUCT0_INTR_SET for the details of bit fields.
FAULT_STRUCT1_INTR_MASK	0x402101C8	Interrupt mask. See FAULT_STRUCT0_INTR_MASK for the details of bit fields.
FAULT_STRUCT1_INTR_MASKED	0x402101CC	Interrupt masked. See FAULT_STRUCT0_INTR_MASKED for the details of bit fields.
FAULT_STRUCT2_CTL	0x40210200	Fault control. See FAULT_STRUCT0_CTL for the details of bit fields.
FAULT_STRUCT2_STATUS	0x4021020C	Fault status. See FAULT_STRUCT0_STATUS for the details of bit fields.
FAULT_STRUCT2_DATA0	0x40210210	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT2_DATA1	0x40210214	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT2_DATA2	0x40210218	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT2_DATA3	0x4021021C	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT2_PENDING0	0x40210240	Fault pending 0. See FAULT_STRUCT0_PENDING0 for the details of bit fields.
FAULT_STRUCT2_PENDING1	0x40210244	Fault pending 1. See FAULT_STRUCT0_PENDING1 for the details of bit fields.
FAULT_STRUCT2_PENDING2	0x40210248	Fault pending 2. See FAULT_STRUCT0_PENDING2 for the details of bit fields.
FAULT_STRUCT2_MASK0	0x40210250	Fault mask 0. See FAULT_STRUCT0_MASK0 for the details of bit fields.
FAULT_STRUCT2_MASK1	0x40210254	Fault mask 1. See FAULT_STRUCT0_MASK1 for the details of bit fields.
FAULT_STRUCT2_MASK2	0x40210258	Fault mask 2. See FAULT_STRUCT0_MASK2 for the details of bit fields.
FAULT_STRUCT2_INTR	0x402102C0	Interrupt. See FAULT_STRUCT0_INTR for the details of bit fields.
FAULT_STRUCT2_INTR_SET	0x402102C4	Interrupt set. See FAULT_STRUCT0_INTR_SET for the details of bit fields.
FAULT_STRUCT2_INTR_MASK	0x402102C8	Interrupt mask. See FAULT_STRUCT0_INTR_MASK for the details of bit fields.
FAULT_STRUCT2_INTR_MASKED	0x402102CC	Interrupt masked. See FAULT_STRUCT0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
FAULT_STRUCT3_CTL	0x40210300	Fault control. See FAULT_STRUCT0_CTL for the details of bit fields.
FAULT_STRUCT3_STATUS	0x4021030C	Fault status. See FAULT_STRUCT0_STATUS for the details of bit fields.
FAULT_STRUCT3_DATA0	0x40210310	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT3_DATA1	0x40210314	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT3_DATA2	0x40210318	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT3_DATA3	0x4021031C	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT3_PENDING0	0x40210340	Fault pending 0. See FAULT_STRUCT0_PENDING0 for the details of bit fields.
FAULT_STRUCT3_PENDING1	0x40210344	Fault pending 1. See FAULT_STRUCT0_PENDING1 for the details of bit fields.
FAULT_STRUCT3_PENDING2	0x40210348	Fault pending 2. See FAULT_STRUCT0_PENDING2 for the details of bit fields.
FAULT_STRUCT3_MASK0	0x40210350	Fault mask 0. See FAULT_STRUCT0_MASK0 for the details of bit fields.
FAULT_STRUCT3_MASK1	0x40210354	Fault mask 1. See FAULT_STRUCT0_MASK1 for the details of bit fields.
FAULT_STRUCT3_MASK2	0x40210358	Fault mask 2. See FAULT_STRUCT0_MASK2 for the details of bit fields.
FAULT_STRUCT3_INTR	0x402103C0	Interrupt. See FAULT_STRUCT0_INTR for the details of bit fields.
FAULT_STRUCT3_INTR_SET	0x402103C4	Interrupt set. See FAULT_STRUCT0_INTR_SET for the details of bit fields.
FAULT_STRUCT3_INTR_MASK	0x402103C8	Interrupt mask. See FAULT_STRUCT0_INTR_MASK for the details of bit fields.
FAULT_STRUCT3_INTR_MASKED	0x402103CC	Interrupt masked. See FAULT_STRUCT0_INTR_MASKED for the details of bit fields.

7.1 Fault subsystem registers

FAULT_STRUCT0_CTL

Fault control
Address: 0x40210000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					RESET_REQ_EN	OUT_EN	TR_EN
Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	RESET_REQ_EN	Reset request enable: '0': Disabled. '1': Enabled. The output reset request signal "fault_reset_req" reflects STATUS.VALID. This reset causes a warm/soft/core reset. This warm/soft/core reset does not affect the fault logic STATUS, DATA0, ..., DATA3 registers (allowing for post soft reset failure analysis). The "fault_reset_req" signals of the individual fault report structures are combined (logically OR'd) into a single SRSS "fault_reset_req" signal. Default Value: 0
1	OUT_EN	IO output signal enable: '0': Disabled. The IO output signal "fault_out" is '0'. The IO output enable signal "fault_out_en" is '0'. '1': Enabled. The IO output signal "fault_out" reflects STATUS.VALID. The IO output enable signal "fault_out_en" is '1'. Default Value: 0
0	TR_EN	Trigger output enable: '0': Disabled. The trigger output "tr_fault" is '0'. '1': Enabled. The trigger output "tr_fault" reflects STATUS.VALID. The trigger can be used to initiate a Datawire transfer of the FAULT data (FAULT_DATA0 through FAULT_DATA3). Default Value: 0

FAULT_STRUCT0_STATUS

Fault status
Address: 0x4021000C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	W						
Name	None	IDX [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW1S	None						
Name	VALID	None [30:24]						

Bits	Name	Description

31	VALID	Valid indication: '0': Invalid. '1': Valid. STATUS.IDX, DATA0, ..., DATA3 specify the fault. Note: Typically, HW sets this field to '1' (on an activated HW fault source that is "enabled" by the MASK registers) and SW clears this field to '0' (typically by boot code SW (after a warm system reset, when the fault is handled). In this typical use case scenario, the HW source fault data is simultaneously captured into DATA0, ..., DATA3 when the VALID field is set to '1'. An exceptional SW use case scenario is identified as well. In this scenario, SW sets this field to '1' with a fault source index different to one of the defined HW fault sources. SW update is not restricted by the MASK registers). In both use case scenarios, the following holds: - STATUS.IDX, DATA0, ..., DATA3 can only be written when STATUS.VALID is '0'; the fault structure is not in use yet. Writing STATUS.VALID to '1' effectively locks the fault structure (until SW clears STATUS.VALID to '0'). This restriction requires a SW update to sequentially update the DATA registers followed by an update of the STATUS register. Note: For the exceptional SW use case, sequential updates to the DATA and STATUS registers may be "interrupted" by a HW fault capture. In this case, the SW DATA register updates are overwritten by the HW update (and the STATUS.IDX field will reflect the HW capture) Default Value: 0
6 : 0	IDX	The fault source index for which fault information is captured in DATA0 through DATA3. The fault information is fault source specific and described below. Note: this register field (and associated fault source data in DATA0 through DATA3) should only be considered valid, when VALID is '1'. Default Value: Undefined

		0x0: MPU_0 : Bus master 0 MPU/SMPU. DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31]: '0' MPU violation; '1': SMPU violation.
		0x1: MPU_1 : Bus master 1 MPU. See MPU_0 description.
		0x2: MPU_2 : Bus master 2 MPU. See MPU_0 description.
		0x3: MPU_3 : Bus master 3 MPU. See MPU_0 description.
		0x4: MPU_4 : Bus master 4 MPU. See MPU_0 description.
		0x5: MPU_5 : Bus master 5 MPU. See MPU_0 description.
		0x6: MPU_6 : Bus master 6 MPU. See MPU_0 description.
		0x7: MPU_7 : Bus master 7 MPU. See MPU_0 description.
		0x8: MPU_8 : Bus master 8 MPU. See MPU_0 description.
		0x9: MPU_9 : Bus master 9 MPU. See MPU_0 description.
		0xa: MPU_10 : Bus master 10 MPU. See MPU_0 description.
		0xb: MPU_11 : Bus master 11 MPU. See MPU_0 description.
		0xc: MPU_12 : Bus master 12 MPU. See MPU_0 description.
		0xd: MPU_13 : Bus master 13 MPU. See MPU_0 description.
		0xe: MPU_14 : Bus master 14 MPU. See MPU_0 description.
		0xf: MPU_15 : Bus master 15 MPU. See MPU_0 description.
		0x10: CM4_SYS_MPU : CM4 system bus AHB-Lite interface MPU. See MPU_0 description.
		0x11: CM4_CODE_MPU : CM4 code bus AHB-Lite interface MPU for non flash controller accesses. See MPU_0 description.

		0x12: CM4_CODE_FLASHC_MPU : CM4 code bus AHB-Lite interface MPU for flash controller accesses. See MPU_0 description.
		0x19: MS_PPU_4 : Peripheral interconnect, master interface 4 PPU. See MS_PPU_0 description.
		0x1a: PERI_ECC : Peripheral interconnect, protection structures SRAM, correctable ECC error: DATA0[10:0]: Violating address. DATA1[7:0]: Syndrome of SRAM word.
		0x1b: PERI_NC_ECC : Peripheral interconnect, protection structures SRAM, non-correctable ECC error. See PERI_ECC description.
		0x1c: MS_PPU_0 : Peripheral interconnect, master interface 0 PPU. DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31:28]: "0": master interface, PPU violation, "1': timeout detected, "2": bus error, other: undefined.
		0x1d: MS_PPU_1 : Peripheral interconnect, master interface 1 PPU. See MS_PPU_0 description.
		0x1e: MS_PPU_2 : Peripheral interconnect, master interface 2 PPU. See MS_PPU_0 description.
		0x1f: MS_PPU_3 : Peripheral interconnect, master interface 3 PPU. See MS_PPU_0 description.

		0x20: GROUP_FAULT_0 : Peripheral group 0 fault detection. DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31:28]: "0": decoder or peripheral bus error, other: undefined.
		0x21: GROUP_FAULT_1 : Peripheral group 1 fault detection. See GROUP_FAULT_0 description.
		0x22: GROUP_FAULT_2 : Peripheral group 2 fault detection. See GROUP_FAULT_0 description.
		0x23: GROUP_FAULT_3 : Peripheral group 3 fault detection. See GROUP_FAULT_0 description.
		0x24: GROUP_FAULT_4 : Peripheral group 4 fault detection. See GROUP_FAULT_0 description.
		0x25: GROUP_FAULT_5 : Peripheral group 5 fault detection. See GROUP_FAULT_0 description.
		0x26: GROUP_FAULT_6 : Peripheral group 6 fault detection. See GROUP_FAULT_0 description.
		0x27: GROUP_FAULT_7 : Peripheral group 7 fault detection. See GROUP_FAULT_0 description.
		0x28: GROUP_FAULT_8 : Peripheral group 8 fault detection. See GROUP_FAULT_0 description.
		0x29: GROUP_FAULT_9 : Peripheral group 9 fault detection. See GROUP_FAULT_0 description.
		0x2a: GROUP_FAULT_10 : Peripheral group 10 fault detection. See GROUP_FAULT_0 description.
		0x2b: GROUP_FAULT_11 : Peripheral group 11 fault detection. See GROUP_FAULT_0 description.
		0x2c: GROUP_FAULT_12 : Peripheral group 12 fault detection. See GROUP_FAULT_0 description.

		0x2d: GROUP_FAULT_13 : Peripheral group 13 fault detection. See GROUP_FAULT_0 description.
		0x2e: GROUP_FAULT_14 : Peripheral group 14 fault detection. See GROUP_FAULT_0 description.
		0x2f: GROUP_FAULT_15 : Peripheral group 15 fault detection. See GROUP_FAULT_0 description.
		0x30: FLASHC_MAIN_BUS_ERROR : Flash controller, main interface, bus error: FAULT_DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. FAULT_DATA1[11:8]: Master identifier.
		0x31: FLASHC_MAIN_C_ECC : Flash controller, main interface, correctable ECC error: DATA[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. DATA1[7:0]: Syndrome of 64-bit word (at address offset 0x00). DATA1[15:8]: Syndrome of 64-bit word (at address offset 0x08). DATA1[23:16]: Syndrome of 64-bit word (at address offset 0x10). DATA1[31:24]: Syndrome of 64-bit word (at address offset 0x18).
		0x32: FLASHC_MAIN_NC_ECC : Flash controller, main interface, non-correctable ECC error. See FLASHC_MAIN_C_ECC description.
		0x33: FLASHC_WORK_BUS_ERROR : Flash controller, work interface, bus error. FAULT_DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. FAULT_DATA1[11:8]: Master identifier.
		0x34: FLASHC_WORK_C_ECC : Flash controller, work interface, correctable ECC error: DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. DATA1[6:0]: Syndrome of 32-bit word.

		0x35: FLASHC_WORK_NC_ECC : Flash controller, work interface, non-correctable ECC error. See FLASHC_WORK_C_ECC description.
		0x36: FLASHC_CM0_CA_C_ECC : Flash controller, CM0+ cache, correctable ECC error: DATA0[26:0]: Violating address. DATA1[6:0]: Syndrome of 32-bit SRAM word (at address offset 0x0). DATA1[14:8]: Syndrome of 32-bit SRAM word (at address offset 0x4). DATA1[22:16]: Syndrome of 32-bit SRAM word (at address offset 0x8). DATA1[30:24]: Syndrome of 32-bit SRAM word (at address offset 0xc).
		0x37: FLASHC_CM0_CA_NC_ECC : Flash controller, CM0+ cache, non-correctable ECC error. See FLASHC_CM0_CA_C_ECC description.
		0x38: FLASHC_CM4_CA_C_ECC : Flash controller, CM4 cache, correctable ECC error. See FLASHC_CM0_CA_C_ECC description.
		0x39: FLASHC_CM4_CA_NC_ECC : Flash controller, CM4 cache, non-correctable ECC error. See FLASHC_CM0_CA_C_ECC description.
		0x3a: RAMC0_C_ECC : System SRAM 0 correctable ECC error: DATA0[31:0]: Violating address. DATA1[6:0]: Syndrome of 32-bit SRAM code word.
		0x3b: RAMC0_NC_ECC : System SRAM 0 non-correctable ECC error. See RAMC0_C_ECC description.
		0x3c: RAMC1_C_ECC : System SRAM 1 correctable ECC error. See RAMC0_C_ECC description.
		0x3d: RAMC1_NC_ECC : System SRAM 1 non-correctable ECC error. See RAMC0_C_ECC description.
		0x3e: RAMC2_C_ECC : System SRAM 2 correctable ECC error. See RAMC0_C_ECC description.
		0x3f: RAMC2_NC_ECC : System SRAM 2 non-correctable ECC error. See RAMC0_C_ECC description.

		0x40: CRYPTO_C_ECC : Cryptography SRAM correctable ECC error. DATA0[31:0]: Violating address. DATA1[6:0]: Syndrome of Least Significant 32-bit SRAM. DATA1[14:8]: Syndrome of Most Significant 32-bit SRAM.
		0x41: CRYPTO_NC_ECC : Cryptography SRAM non-correctable ECC error. See CRYPTO_C_ECC description.
		0x46: DW0_C_ECC : DataWire 0 SRAM 1 correctable ECC error: DATA0[11:0]: Violating DW SRAM address (word address, assuming byte addressable). DATA1[6:0]: Syndrome of 32-bit SRAM code word.
		0x47: DW0_NC_ECC : DataWire 0 SRAM 1 non-correctable ECC error. See DW0_C_ECC description.
		0x48: DW1_C_ECC : DataWire 1 SRAM 1 correctable ECC error. See DW0_C_ECC description.
		0x49: DW1_NC_ECC : DataWire 1 SRAM 1 non-correctable ECC error. See DW0_C_ECC description.
		0x4a: FM_SRAM_C_ECC : eCT Flash SRAM (for embedded operations) correctable ECC error: DATA0[15:0]: Address location in the eCT Flash SRAM. DATA1[6:0]: Syndrome of 32-bit SRAM word.
		0x4b: FM_SRAM_NC_ECC : eCT Flash SRAM non-correctable ECC error: See FM_SRAM_C_ECC description.
		0x50: CAN0_C_ECC : CAN controller 0 MRAM correctable ECC error: DATA0[15:0]: Violating address. DATA0[22:16]: ECC violating data[38:32] from MRAM. DATA0[27:24]: Master ID: 0-7 = CAN channel ID within mxttcanfd cluster, 8 = AHB I/F DATA1[31:0]: ECC violating data[31:0] from MRAM.

		0x51: CAN0_NC_ECC : CAN controller 0 MRAM non-correctable ECC error: DATA0[15:0]: Violating address. DATA0[22:16]: ECC violating data[38:32] from MRAM (not for Address Error). DATA0[27:24]: Master ID: 0-7 = CAN channel ID within mxttcanfd cluster, 8 = AHB I/F DATA0[30]: Write access, only possible for Address Error DATA0[31]: Address Error: a CAN channel did an MRAM access above MRAM_SIZE DATA1[31:0]: ECC violating data[31:0] from MRAM (not for Address Error).
		0x52: CAN1_C_ECC : CAN controller 1 MRAM correctable ECC error. See CAN0_C_ECC description.
		0x53: CAN1_NC_ECC : CAN controller 1 MRAM non-correctable ECC error. See CAN0_NC_ECC description.
		0x54: CAN2_C_ECC : CAN controller 2 MRAM correctable ECC error. See CAN0_C_ECC description.
		0x55: CAN2_NC_ECC : CAN controller 2 MRAM non-correctable ECC error. See CAN0_NC_ECC description.
		0x5a: SRSS_CSV : SRSS Clock SuperVisor (CSV) violation detected. Multiple CSV can detect a violation at the same time. DATA0[15:0]: CSV violation occurred on corresponding clk_hf* root clock, each bit representing a clk_hf, say bit 0 for clk_hf0, bit 1 for clk_hf1, etc. DATA0[24]: CSV violation occurred on reference clock for clk_hf CSVs DATA0[25]: CSV violation occurred on clk_lf DATA0[26]: CSV violation occurred on clk_ilo0
		0x5b: SRSS_SSV : SRSS Supply SuperVisor (SSV) violation detected. Multiple SSV can detect a violation at the same time. DATA0[0]: BOD detected on VDDA DATA0[1]: OVD detected on VDDA DATA0[16]: violation detected on LVD/HVD #1 DATA0[17]: violation detected on LVD/HVD #2

		0x5c: SRSS_MCWDT0 : SRSS Multi-Counter Watch Dog Timer (MCWDT) #0 violation detected. Multiple counters can detect a violation at the same time. DATA0[0]: MCWDT subcounter 0 LOWER_LIMIT DATA0[1]: MCWDT subcounter 0 UPPER_LIMIT DATA0[2]: MCWDT subcounter 1 LOWER_LIMIT DATA0[3]: MCWDT subcounter 1 UPPER_LIMIT
		0x5d: SRSS_MCWDT1 : SRSS Multi-Counter Watch Dog Timer (MCWDT) #1 violation detected. See SRSS_MCWDT0 description.
		0x5e: SRSS_MCWDT2 : SRSS Multi-Counter Watch Dog Timer (MCWDT) #2 violation detected. See SRSS_MCWDT0 description.
		0x5f: SRSS_MCWDT3 : SRSS Multi-Counter Watch Dog Timer (MCWDT) #3 violation detected. See SRSS_MCWDT0 description.

FAULT_STRUCT0_DATA0

Fault data
Address: 0x40210010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Captured fault source data. Note: the DATA registers can only be written when STATUS.VALID is '0'. Note: the fault source index STATUS.IDX specifies the format of the DATA registers. Default Value: Undefined

FAULT_STRUCT0_PENDING0

Fault pending 0
Address: 0x40210040
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	This field specifies the following sources: Bit 0: CM0 MPU. Bit 1: CRYPTO MPU. Bit 2: DW 0 MPU. Bit 3: DW 1 MPU. Bit 4: DMA controller MPU. ... Bit 15: DAP MPU. Bit 16: CM4 system bus MPU. Bit 17: CM4 code bus MPU (for non FLASH controller accesses). Bit 18: CM4 code bus MPU (for FLASH controller accesses). Default Value: Undefined

FAULT_STRUCT0_PENDING1

Fault pending 1
Address: 0x40210044
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	This field specifies the following sources: Bit 0: Peripheral group 0 PPU. Bit 1: Peripheral group 1 PPU. Bit 2: Peripheral group 2 PPU. Bit 3: Peripheral group 3 PPU. Bit 4: Peripheral group 4 PPU. Bit 5: Peripheral group 5 PPU. Bit 6: Peripheral group 6 PPU. Bit 7: Peripheral group 7 PPU. ... Bit 15: Peripheral group 15 PPU. Bit 16 - 31: See STATUS register. Default Value: Undefined

FAULT_STRUCT0_PENDING2

Fault pending 2
Address: 0x40210048
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	This field specifies the following sources: Bit 0 - 31: See STATUS register. Default Value: Undefined

FAULT_STRUCT0_MASK0

Fault mask 0
Address: 0x40210050
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	Fault source enables: Bits 31-0: Fault sources 31 to 0. Default Value: 0

FAULT_STRUCT0_MASK1

Fault mask 1
Address: 0x40210054
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	Fault source enables: Bits 31-0: Fault sources 63 to 32. Default Value: 0

FAULT_STRUCT0_MASK2

Fault mask 2
Address: 0x40210058
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	Fault source enables: Bits 31-0: Fault sources 95 to 64. Default Value: 0

FAULT_STRUCT0_INTR

Interrupt
Address: 0x402100C0
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							FAULT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	FAULT	This interrupt cause field is activated (HW sets the field to '1') when an enabled (MASK0/MASK1/MASK2) pending fault source is captured: - STATUS.VALID is set to '1'. - STATUS.IDX specifies the fault source index. - DATA0 through DATA3 captures the fault source data. SW writes a '1' to this field to clear the interrupt cause to '0'. SW clear STATUS.VALID to '0' to enable capture of the next fault. Note that when there is an enabled pending fault source, the pending fault source is captured immediately and INTR.FAULT is immediately activated (set to '1'). Default Value: 0

FAULT_STRUCT0_INTR_SET

Interrupt set
Address: 0x402100C4
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							FAULT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	FAULT	SW writes a '1' to this field to set the corresponding field in the INTR register. Default Value: 0

FAULT_STRUCT0_INTR_MASK

Interrupt mask
Address: 0x402100C8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							FAULT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	FAULT	Mask bit for corresponding field in the INTR register. Default Value: 0

FAULT_STRUCT0_INTR_MASKED

Interrupt masked
Address: 0x402100CC
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							FAULT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	FAULT	Logical and of corresponding INTR and INTR_MASK fields. Default Value: 0

8 System resources subsystem (SRSS)

Register details

Register name	Address	Description
PWR_LVD_STATUS	0x40260040	High Voltage / Low Voltage Detector (HVLVD) Status Register
PWR_LVD_STATUS2	0x40260044	High Voltage / Low Voltage Detector (HVLVD) Status Register #2
CLK_DSI_SELECT0	0x40260100	Clock DSI Select Register
CLK_DSI_SELECT1	0x40260104	Clock DSI Select Register. See CLK_DSI_SELECT0 for the details of bit fields.
CLK_DSI_SELECT2	0x40260108	Clock DSI Select Register. See CLK_DSI_SELECT0 for the details of bit fields.
CLK_DSI_SELECT3	0x4026010C	Clock DSI Select Register. See CLK_DSI_SELECT0 for the details of bit fields.
CLK_OUTPUT_FAST	0x40260140	Fast Clock Output Select Register
CLK_OUTPUT_SLOW	0x40260144	Slow Clock Output Select Register
CLK_CAL_CNT1	0x40260148	Clock Calibration Counter 1
CLK_CAL_CNT2	0x4026014C	Clock Calibration Counter 2
SRSS_INTR	0x40260200	SRSS Interrupt Register
SRSS_INTR_SET	0x40260204	SRSS Interrupt Set Register
SRSS_INTR_MASK	0x40260208	SRSS Interrupt Mask Register
SRSS_INTR_MASKED	0x4026020C	SRSS Interrupt Masked Register
PWR_CTL	0x40261000	Power Mode Control
PWR_CTL2	0x40261004	Power Mode Control 2
PWR_HIBERNATE	0x40261008	HIBERNATE Mode Register
PWR_SSV_CTL	0x40261018	Supply Supervision Control Register
PWR_SSV_STATUS	0x4026101C	Supply Supervision Status Register
PWR_LVD_CTL	0x40261020	High Voltage / Low Voltage Detector (HVLVD) Configuration Register
PWR_LVD_CTL2	0x40261024	High Voltage / Low Voltage Detector (HVLVD) Configuration Register #2
PWR_HIB_DATA0	0x40261040	HIBERNATE Data Register
CLK_PATH_SELECT0	0x40261200	Clock Path Select Register
CLK_PATH_SELECT1	0x40261204	Clock Path Select Register. See CLK_PATH_SELECT0 for the details of bit fields.
CLK_PATH_SELECT2	0x40261208	Clock Path Select Register. See CLK_PATH_SELECT0 for the details of bit fields.
CLK_PATH_SELECT3	0x4026120C	Clock Path Select Register. See CLK_PATH_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT0	0x40261240	Clock Root Select Register

Register name	Address	Description
CLK_ROOT_SELECT1	0x40261244	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT2	0x40261248	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CSV_HF_CSV0_REF_CTL	0x40261400	Clock Supervision Reference Control
CSV_HF_CSV0_REF_LIMIT	0x40261404	Clock Supervision Reference Limits
CSV_HF_CSV0_MON_CTL	0x40261408	Clock Supervision Monitor Control
CSV_HF_CSV1_REF_CTL	0x40261410	Clock Supervision Reference Control. See CSV_HF_CSV0_REF_CTL for the details of bit fields.
CSV_HF_CSV1_REF_LIMIT	0x40261414	Clock Supervision Reference Limits. See CSV_HF_CSV0_REF_LIMIT for the details of bit fields.
CSV_HF_CSV1_MON_CTL	0x40261418	Clock Supervision Monitor Control. See CSV_HF_CSV0_MON_CTL for the details of bit fields.
CSV_HF_CSV2_REF_CTL	0x40261420	Clock Supervision Reference Control. See CSV_HF_CSV0_REF_CTL for the details of bit fields.
CSV_HF_CSV2_REF_LIMIT	0x40261424	Clock Supervision Reference Limits. See CSV_HF_CSV0_REF_LIMIT for the details of bit fields.
CSV_HF_CSV2_MON_CTL	0x40261428	Clock Supervision Monitor Control. See CSV_HF_CSV0_MON_CTL for the details of bit fields.
CLK_SELECT	0x40261500	Clock selection register
CLK_TIMER_CTL	0x40261504	Timer Clock Control Register
CLK_ILO0_CONFIG	0x40261508	ILO0 Configuration
CLK_ILO1_CONFIG	0x4026150C	ILO1 Configuration
CLK_IMO_CONFIG	0x40261518	IMO Configuration
CLK_ECO_CONFIG	0x4026151C	ECO Configuration Register
CLK_ECO_PRESCALE	0x40261520	ECO Prescaler Configuration Register
CLK_ECO_STATUS	0x40261524	ECO Status Register
CLK_FLL_CONFIG	0x40261530	FLL Configuration Register
CLK_FLL_CONFIG2	0x40261534	FLL Configuration Register 2
CLK_FLL_CONFIG3	0x40261538	FLL Configuration Register 3
CLK_FLL_CONFIG4	0x4026153C	FLL Configuration Register 4
CLK_FLL_STATUS	0x40261540	FLL Status Register
CLK_ECO_CONFIG2	0x40261544	ECO Configuration Register 2
CLK_PLL_CONFIG0	0x40261600	PLL Configuration Register
CLK_PLL_STATUS0	0x40261640	PLL Status Register
CSV_REF_SEL	0x40261700	Select CSV Reference clock for Active domain
CSV_REF_CSV_REF_CTL	0x40261710	Clock Supervision Reference Control. See CSV_HF_CSV0_REF_CTL for the details of bit fields.
CSV_REF_CSV_REF_LIMIT	0x40261714	Clock Supervision Reference Limits. See CSV_HF_CSV0_REF_LIMIT for the details of bit fields.

Register name	Address	Description
CSV_REF_CSV_MON_CTL	0x40261718	Clock Supervision Monitor Control. See CSV_HF_CSV0_MON_CTL for the details of bit fields.
CSV_LF_CSV_REF_CTL	0x40261720	Clock Supervision Reference Control
CSV_LF_CSV_REF_LIMIT	0x40261724	Clock Supervision Reference Limits
CSV_LF_CSV_MON_CTL	0x40261728	Clock Supervision Monitor Control
CSV_ILO_CSV_REF_CTL	0x40261730	Clock Supervision Reference Control. See CSV_LF_CSV_REF_CTL for the details of bit fields.
CSV_ILO_CSV_REF_LIMIT	0x40261734	Clock Supervision Reference Limits. See CSV_LF_CSV_REF_LIMIT for the details of bit fields.
CSV_ILO_CSV_MON_CTL	0x40261738	Clock Supervision Monitor Control. See CSV_LF_CSV_MON_CTL for the details of bit fields.
RES_CAUSE	0x40261800	Reset Cause Observation Register
RES_CAUSE2	0x40261804	Reset Cause Observation Register 2
CLK_TRIM_ILO0_CTL	0x40263014	ILO0 Trim Register
CLK_TRIM_ILO1_CTL	0x40263220	ILO1 Trim Register
MCWDT0_CTR0_CTL	0x40268000	MCWDT Subcounter Control Register
MCWDT0_CTR0_LOWER_LIMIT	0x40268004	MCWDT Subcounter Lower Limit Register
MCWDT0_CTR0_UPPER_LIMIT	0x40268008	MCWDT Subcounter Upper Limit Register
MCWDT0_CTR0_WARN_LIMIT	0x4026800C	MCWDT Subcounter Warn Limit Register
MCWDT0_CTR0_CONFIG	0x40268010	MCWDT Subcounter Configuration Register
MCWDT0_CTR0_CNT	0x40268014	MCWDT Subcounter Count Register
MCWDT0_CTR1_CTL	0x40268020	MCWDT Subcounter Control Register. See MCWDT0_CTR0_CTL for the details of bit fields.
MCWDT0_CTR1_LOWER_LIMIT	0x40268024	MCWDT Subcounter Lower Limit Register. See MCWDT0_CTR0_LOWER_LIMIT for the details of bit fields.
MCWDT0_CTR1_UPPER_LIMIT	0x40268028	MCWDT Subcounter Upper Limit Register. See MCWDT0_CTR0_UPPER_LIMIT for the details of bit fields.
MCWDT0_CTR1_WARN_LIMIT	0x4026802C	MCWDT Subcounter Warn Limit Register. See MCWDT0_CTR0_WARN_LIMIT for the details of bit fields.
MCWDT0_CTR1_CONFIG	0x40268030	MCWDT Subcounter Configuration Register. See MCWDT0_CTR0_CONFIG for the details of bit fields.
MCWDT0_CTR1_CNT	0x40268034	MCWDT Subcounter Count Register. See MCWDT0_CTR0_CNT for the details of bit fields.
MCWDT0_CPU_SELECT	0x40268040	MCWDT CPU selection register
MCWDT0_CTR2_CTL	0x40268080	MCWDT Subcounter 2 Control register
MCWDT0_CTR2_CONFIG	0x40268084	MCWDT Subcounter 2 Configuration register
MCWDT0_CTR2_CNT	0x40268088	MCWDT Subcounter 2 Count Register
MCWDT0_LOCK	0x40268090	MCWDT Lock Register
MCWDT0_SERVICE	0x40268094	MCWDT Service Register

Register name	Address	Description
MCWDT0_INTR	0x402680A0	MCWDT Interrupt Register
MCWDT0_INTR_SET	0x402680A4	MCWDT Interrupt Set Register
MCWDT0_INTR_MASK	0x402680A8	MCWDT Interrupt Mask Register
MCWDT0_INTR_MASKED	0x402680AC	MCWDT Interrupt Masked Register
MCWDT1_CTR0_CTL	0x40268100	MCWDT Subcounter Control Register. See MCWDT0_CTR0_CTL for the details of bit fields.
MCWDT1_CTR0_LOWER_LIMIT	0x40268104	MCWDT Subcounter Lower Limit Register. See MCWDT0_CTR0_LOWER_LIMIT for the details of bit fields.
MCWDT1_CTR0_UPPER_LIMIT	0x40268108	MCWDT Subcounter Upper Limit Register. See MCWDT0_CTR0_UPPER_LIMIT for the details of bit fields.
MCWDT1_CTR0_WARN_LIMIT	0x4026810C	MCWDT Subcounter Warn Limit Register. See MCWDT0_CTR0_WARN_LIMIT for the details of bit fields.
MCWDT1_CTR0_CONFIG	0x40268110	MCWDT Subcounter Configuration Register. See MCWDT0_CTR0_CONFIG for the details of bit fields.
MCWDT1_CTR0_CNT	0x40268114	MCWDT Subcounter Count Register. See MCWDT0_CTR0_CNT for the details of bit fields.
MCWDT1_CTR1_CTL	0x40268120	MCWDT Subcounter Control Register. See MCWDT0_CTR0_CTL for the details of bit fields.
MCWDT1_CTR1_LOWER_LIMIT	0x40268124	MCWDT Subcounter Lower Limit Register. See MCWDT0_CTR0_LOWER_LIMIT for the details of bit fields.
MCWDT1_CTR1_UPPER_LIMIT	0x40268128	MCWDT Subcounter Upper Limit Register. See MCWDT0_CTR0_UPPER_LIMIT for the details of bit fields.
MCWDT1_CTR1_WARN_LIMIT	0x4026812C	MCWDT Subcounter Warn Limit Register. See MCWDT0_CTR0_WARN_LIMIT for the details of bit fields.
MCWDT1_CTR1_CONFIG	0x40268130	MCWDT Subcounter Configuration Register. See MCWDT0_CTR0_CONFIG for the details of bit fields.
MCWDT1_CTR1_CNT	0x40268134	MCWDT Subcounter Count Register. See MCWDT0_CTR0_CNT for the details of bit fields.
MCWDT1_CPU_SELECT	0x40268140	MCWDT CPU selection register. See MCWDT0_CPU_SELECT for the details of bit fields.
MCWDT1_CTR2_CTL	0x40268180	MCWDT Subcounter 2 Control register. See MCWDT0_CTR2_CTL for the details of bit fields.
MCWDT1_CTR2_CONFIG	0x40268184	MCWDT Subcounter 2 Configuration register. See MCWDT0_CTR2_CONFIG for the details of bit fields.
MCWDT1_CTR2_CNT	0x40268188	MCWDT Subcounter 2 Count Register. See MCWDT0_CTR2_CNT for the details of bit fields.
MCWDT1_LOCK	0x40268190	MCWDT Lock Register. See MCWDT0_LOCK for the details of bit fields.
MCWDT1_SERVICE	0x40268194	MCWDT Service Register. See MCWDT0_SERVICE for the details of bit fields.

Register name	Address	Description
MCWDT1_INTR	0x402681A0	MCWDT Interrupt Register. See MCWDT0_INTR for the details of bit fields.
MCWDT1_INTR_SET	0x402681A4	MCWDT Interrupt Set Register. See MCWDT0_INTR_SET for the details of bit fields.
MCWDT1_INTR_MASK	0x402681A8	MCWDT Interrupt Mask Register. See MCWDT0_INTR_MASK for the details of bit fields.
MCWDT1_INTR_MASKED	0x402681AC	MCWDT Interrupt Masked Register. See MCWDT0_INTR_MASKED for the details of bit fields.
WDT_CTL	0x4026C000	WDT Control Register
WDT_LOWER_LIMIT	0x4026C004	WDT Lower Limit Register
WDT_UPPER_LIMIT	0x4026C008	WDT Upper Limit Register
WDT_WARN_LIMIT	0x4026C00C	WDT Warn Limit Register
WDT_CONFIG	0x4026C010	WDT Configuration Register
WDT_CNT	0x4026C014	WDT Count Register
WDT_LOCK	0x4026C040	WDT Lock register
WDT_SERVICE	0x4026C044	WDT Service register
WDT_INTR	0x4026C050	WDT Interrupt Register
WDT_INTR_SET	0x4026C054	WDT Interrupt Set Register
WDT_INTR_MASK	0x4026C058	WDT Interrupt Mask Register
WDT_INTR_MASKED	0x4026C05C	WDT Interrupt Masked Register

8.1 SRSS registers

PWR_LVD_STATUS

High Voltage / Low Voltage Detector (HVLVD) Status Register
Address: 0x40260040
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							HVLVD1_OUT
Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	None							
HW Access	None							
Name	None [15:8]							
Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None							
HW Access	None							

Bits	23	22	21	20	19	18	17	16
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	HVLVD1_OUT	HVLVD1 output. 0: below voltage threshold 1: above voltage threshold Default Value: 0

PWR_LVD_STATUS2

High Voltage / Low Voltage Detector (HVLVD) Status Register #2
Address: 0x40260044
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							HVLVD2_OUT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	HVLVD2_OUT	HVLVD2 output. 0: below voltage threshold 1: above voltage threshold Default Value: 0

CLK_DSI_SELECT0

Clock DSI Select Register
Address: 0x40260100
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			DSI_MUX [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	DSI_MUX	Selects a DSI source or low frequency clock for use in a clock path. The output of this mux can be selected for clock PATH<i> using CLK_PATH_SELECT register. Using the output of this mux as HFCLK source will result in undefined behavior. It can be used to clocks to DSI or as reference inputs for the FLL/PLL, subject to the frequency limits of those circuits. This mux is not glitch free, so do not change the selection while it is an actively selected clock. Default Value: 0
		0x0: DSI_OUT0 : DSI0 - dsi_out[0]
		0x1: DSI_OUT1 : DSI1 - dsi_out[1]
		0x2: DSI_OUT2 : DSI2 - dsi_out[2]
		0x3: DSI_OUT3 : DSI3 - dsi_out[3]
		0x4: DSI_OUT4 : DSI4 - dsi_out[4]
		0x5: DSI_OUT5 : DSI5 - dsi_out[5]
		0x6: DSI_OUT6 : DSI6 - dsi_out[6]

		0x7: DSI_OUT7 : DSI7 - dsi_out[7]
		0x8: DSI_OUT8 : DSI8 - dsi_out[8]
		0x9: DSI_OUT9 : DSI9 - dsi_out[9]
		0xa: DSI_OUT10 : DSI10 - dsi_out[10]
		0xb: DSI_OUT11 : DSI11 - dsi_out[11]
		0xc: DSI_OUT12 : DSI12 - dsi_out[12]
		0xd: DSI_OUT13 : DSI13 - dsi_out[13]
		0xe: DSI_OUT14 : DSI14 - dsi_out[14]
		0xf: DSI_OUT15 : DSI15 - dsi_out[15]
		0x10: ILO0 : ILO0 - Internal Low-speed Oscillator #0
		0x11: WCO : WCO - Watch-Crystal Oscillator
		0x12: ALTLF : ALTLF - Alternate Low-Frequency Clock
		0x13: PILO : PILO - Precision Internal Low-speed Oscillator
		0x14: ILO1 : ILO1 - Internal Low-speed Oscillator #1, if present.

CLK_OUTPUT_FAST

Fast Clock Output Select Register
Address: 0x40260140
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PATH_SEL0 [7:4]				FAST_SEL0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				HFCLK_SEL0 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	PATH_SEL1 [23:20]				FAST_SEL1 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW			
HW Access	None				R			
Name	None [31:28]				HFCLK_SEL1 [27:24]			

Bits	Name	Description
27 : 24	HFCLK_SEL1	Selects a HFCLK tree for use in fast clock output #1 logic Default Value: 0
23 : 20	PATH_SEL1	Selects a clock path to use in fast clock output #1 logic. 0: FLL output 1-15: PLL output on path1-path15 (if available) Default Value: 0
19 : 16	FAST_SEL1	Select signal for fast clock output #1 Default Value: 0
		0x0: NC : Disabled - output is 0. For power savings, clocks are blocked before entering any muxes, including PATH_SEL1 and HFCLK_SEL1.
		0x1: ECO : External Crystal Oscillator (ECO)
		0x2: EXTCLK : External clock input (EXTCLK)
		0x3: ALTHF : Alternate High-Frequency (ALTHF) clock input to SRSS

		0x4: TIMERCLK : Timer clock. It is grouped with the fast clocks because it may be a gated version of a fast clock, and therefore may have a short high pulse.
		0x5: PATH_SEL1 : Selects the clock path chosen by PATH_SEL1 field
		0x6: HFCLK_SEL1 : Selects the output of the HFCLK_SEL1 mux
		0x7: SLOW_SEL1 : Selects the output of CLK_OUTPUT_SLOW.SLOW_SEL1
11 : 8	HFCLK_SEL0	Selects a HFCLK tree for use in fast clock output #0 Default Value: 0
7 : 4	PATH_SEL0	Selects a clock path to use in fast clock output #0 logic. 0: FLL output 1-15: PLL output on path1-path15 (if available) Default Value: 0
3 : 0	FAST_SEL0	Select signal for fast clock output #0 Default Value: 0
		0x0: NC : Disabled - output is 0. For power savings, clocks are blocked before entering any muxes, including PATH_SEL0 and HFCLK_SEL0.
		0x1: ECO : External Crystal Oscillator (ECO)
		0x2: EXTCLK : External clock input (EXTCLK)
		0x3: ALTHF : Alternate High-Frequency (ALTHF) clock input to SRSS
		0x4: TIMERCLK : Timer clock. It is grouped with the fast clocks because it may be a gated version of a fast clock, and therefore may have a short high pulse.
		0x5: PATH_SEL0 : Selects the clock path chosen by PATH_SEL0 field
		0x6: HFCLK_SEL0 : Selects the output of the HFCLK_SEL0 mux
		0x7: SLOW_SEL0 : Selects the output of CLK_OUTPUT_SLOW.SLOW_SEL0

CLK_OUTPUT_SLOW

Slow Clock Output Select Register
Address: 0x40260144
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	SLOW_SEL1 [7:4]				SLOW_SEL0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	SLOW_SEL1	Select signal for slow clock output #1 Default Value: 0
		0x0: NC : Disabled - output is 0. For power savings, clocks are blocked before entering any muxes.
		0x1: ILO0 : Internal Low Speed Oscillator (ILO)
		0x2: WCO : Watch-Crystal Oscillator (WCO)
		0x3: BAK : Root of the Backup domain clock tree (BAK)
		0x4: ALTLF : Alternate low-frequency clock input to SRSS (ALTLF)
		0x5: LFCLK : Root of the low-speed clock tree (LFCLK)
		0x6: IMO : Internal Main Oscillator (IMO). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit.

		0x7: SLPCTRL : Sleep Controller clock (SLPCTRL). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/ exit.
		0x8: PILO : Precision Internal Low Speed Oscillator (PILO)
		0x9: ILO1 : Internal Low Speed Oscillator (ILO1), if present on the product.
		0xa: ECO_PRESCALER : ECO Prescaler (ECO_PRESCALER)
3 : 0	SLOW_SEL0	Select signal for slow clock output #0 Default Value: 0
		0x0: NC : Disabled - output is 0. For power savings, clocks are blocked before entering any muxes.
		0x1: ILO0 : Internal Low Speed Oscillator (ILO0)
		0x2: WCO : Watch-Crystal Oscillator (WCO)
		0x3: BAK : Root of the Backup domain clock tree (BAK)
		0x4: ALTLF : Alternate low-frequency clock input to SRSS (ALTLF)
		0x5: LFCLK : Root of the low-speed clock tree (LFCLK)
		0x6: IMO : Internal Main Oscillator (IMO). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit.
		0x7: SLPCTRL : Sleep Controller clock (SLPCTRL). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/ exit.
		0x8: PILO : Precision Internal Low Speed Oscillator (PILO)
		0x9: ILO1 : Internal Low Speed Oscillator (ILO1), if present on the product.
		0xa: ECO_PRESCALER : ECO Prescaler (ECO_PRESCALER)

CLK_CAL_CNT1

Clock Calibration Counter 1
Address: 0x40260148
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	CAL_COUNTER1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	CAL_COUNTER1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	CAL_COUNTER1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CAL_COUNTER_DONE	None [30:24]						

Bits	Name	Description
31	CAL_COUNTER_DONE	Status bit indicating that the internal counter #1 is finished counting and CLK_CAL_CNT2.COUNTER stopped counting up Default Value: 1

23 : 0	CAL_COUNTER1	Down-counter clocked on fast clock output #0 (see CLK_OUTPUT_FAST). This register always reads as zero. Counting starts internally when this register is written with a nonzero value. CAL_COUNTER_DONE goes immediately low to indicate that the counter has started and will be asserted when the counters are done. Do not write this field unless CAL_COUNTER_DONE==1. Both clocks must be running or the measurement will not complete. A stalled counter can be recovered by selecting valid clocks, waiting until the measurement completes, and discarding the first result. Default Value: 0

CLK_CAL_CNT2

Clock Calibration Counter 2
Address: 0x4026014C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CAL_COUNTER2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CAL_COUNTER2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	CAL_COUNTER2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	CAL_COUNTER2	Up-counter clocked on fast clock output #1 (see CLK_OUTPUT_FAST). When CLK_CAL_CNT1.CAL_COUNTER_DONE==1, the counter is stopped and can be read by SW. Do not read this value unless CAL_COUNTER_DONE==1. The expected final value is related to the ratio of clock frequencies used for the two counters and the value loaded into counter 1: CLK_CAL_CNT2.COUNTER=(F_cnt2/F_cnt1)*(CLK_CAL_CNT1.COUNTER) Default Value: 0

SRSS_INTR

SRSS Interrupt Register
Address: 0x40260200
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1C	None		RW1C	RW1C	None
HW Access	None		A	None		A	A	None
Name	None [7:6]		CLK_CAL	None [4:3]		HVLVD2	HVLVD1	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	CLK_CAL	Clock calibration counter is done. This field is reset during DEEPSLEEP mode. Default Value: 0
2	HVLVD2	Interrupt for low voltage detector HVLVD2 Default Value: 0
1	HVLVD1	Interrupt for low voltage detector HVLVD1 Default Value: 0

SRSS_INTR_SET

SRSS Interrupt Set Register
Address: 0x40260204
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1S	None		RW1S	RW1S	None
HW Access	None		A	None		A	A	None
Name	None [7:6]		CLK_CAL	None [4:3]		HVLVD2	HVLVD1	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	CLK_CAL	Set interrupt for clock calibration counter done. This field is reset during DEEPSLEEP mode. Default Value: 0
2	HVLVD2	Set interrupt for low voltage detector HVLVD2 Default Value: 0
1	HVLVD1	Set interrupt for low voltage detector HVLVD1 Default Value: 0

SRSS_INTR_MASK

SRSS Interrupt Mask Register
Address: 0x40260208
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	None		RW	RW	None
HW Access	None		R	None		R	R	None
Name	None [7:6]		CLK_CAL	None [4:3]		HVLVD2	HVLVD1	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	CLK_CAL	Mask for clock calibration done Default Value: 0
2	HVLVD2	Mask for low voltage detector HVLVD2 Default Value: 0
1	HVLVD1	Mask for low voltage detector HVLVD1 Default Value: 0

SRSS_INTR_MASKED

SRSS Interrupt Masked Register
Address: 0x4026020C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	None		R	R	None
HW Access	None		RW	None		RW	RW	None
Name	None [7:6]		CLK_CAL	None [4:3]		HVLVD2	HVLVD1	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	CLK_CAL	Logical and of corresponding request and mask bits. Default Value: 0
2	HVLVD2	Logical and of corresponding request and mask bits. Default Value: 0
1	HVLVD1	Logical and of corresponding request and mask bits. Default Value: 0

PWR_CTL

Power Mode Control
Address: 0x40261000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None		R	
HW Access	None		RW	RW	None		RW	
Name	None [7:6]		LPM_READY	DEBUG_SESSION	None [3:2]		POWER_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	LPM_READY	Indicates whether certain low power functions are ready. The low current circuits take longer to startup after XRES, HIBERNATE wakeup, or supply supervision reset than the normal mode circuits. HIBERNATE mode may be entered regardless of this bit. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. 0: If a low power circuit operation is requested, it will stay in its normal operating mode until it is ready. If DEEPSLEEP is requested by all processors WFI/WFE, the device will instead enter SLEEP. When low power circuits are ready, device will automatically enter the originally requested mode. 1: Normal operation. DEEPSLEEP and low power circuits operate as requested in other registers. Default Value: 0

4	DEBUG_SESSION	Indicates whether a debug session is active (CDBGPWRUPREQ signal is 1) Default Value: 0
		0x0: NO_SESSION : No debug session active
		0x1: SESSION_ACTIVE : Debug session is active. Power modes behave differently to keep the debug session active.
1 : 0	POWER_MODE	Current power mode of the device. Note that this field cannot be read in all power modes on actual silicon. Default Value: 0
		0x0: RESET : System is resetting.
		0x1: ACTIVE : At least one CPU is running.
		0x2: SLEEP : No CPUs are running. Peripherals may be running.
		0x3: DEEPSLEEP : Main high-frequency clock is off; low speed clocks are available. Communication interface clocks may be present.

PWR_CTL2

Power Mode Control 2
Address: 0x40261004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		R	RW
HW Access	None			A	None		RW	A
Name	None [7:5]			DPSLP_REG_DIS	None [3:2]		LINREG_OK	LINREG_DIS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		R	RW	None			RW
HW Access	None		RW	A	None			A
Name	None [23:22]		REFVBUF_OK	REFVBUF_DIS	None [19:17]			REFV_DIS

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None		RW	None		R	RW
HW Access	R	None		A	None		RW	A
Name	PLL_LS_BYPASS	None [30:29]		BGREF_LPMODE	None [27:26]		REFI_OK	REFI_DIS

Bits	Name	Description
31	PLL_LS_BYPASS	Bypass level shifter inside the PLL. Unused, if no PLL is present in the product. 0: Do not bypass the level shifter. This setting is ok for all operational modes and vccd target voltage. 1: Bypass the level shifter. This may reduce jitter on the PLL output clock, but can only be used when vccd is targeted to 1.1V nominal. Otherwise, it can result in clock degradation and static current. Default Value: 0

28	BGREF_LPMODE	Current is reduced using a sample&hold feature. This requires ILO0 to be operating properly. This register will not set unless CLK_ILO0_CONFIG.ILO0_ENABLE==1. When changing back to continuous operation, keep ILO0 enabled for at least 5 cycles after clearing this bit to allow for internal synchronization. 0: Bandgap Reference circuits operate in higher current mode. 1: Bandgap Reference circuits operate in low power (see above for tradeoffs). Default Value: 0
25	REFI_OK	Indicates that the current reference is ready. Due to synchronization delays, it may take two IMO clock cycles for hardware to clear this bit after asserting REFI_DIS=1. Default Value: 0
24	REFI_DIS	Reserved. Write zero. Default Value: 0
21	REFVBUF_OK	Indicates that the voltage reference buffer is ready. Due to synchronization delays, it may take two IMO clock cycles for hardware to clear this bit after asserting REFVBUF_DIS=1. Default Value: 0
20	REFVBUF_DIS	Disable the voltage reference buffer. Firmware should only disable the buffer when there is no connected circuit that is using it. SRSS circuits that require it are the PLL and ECO. A particular product may have circuits outside the SRSS that use the buffer. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. Default Value: 0
16	REFV_DIS	Reserved. Write zero. Default Value: 0
4	DPSLP_REG_DIS	Reserved. Must be kept zero. Default Value: 0
1	LINREG_OK	Status of the linear Core Regulator. Default Value: 0

0	LINREG_DIS	Explicitly disable the linear Core Regulator. Write zero for XMC5000 devices. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. 0: Linear Core Regulator is not explicitly disabled. Hardware disables it automatically for internal sequences, including for DEEPSLEEP, HIBERNATE, and XRES low power modes. 1: Linear Core Regulator is explicitly disabled. Only use this for special cases when another source supplies vccd during ACTIVE and SLEEP modes. This setting is only legal when another source supplies vccd, but there is no special hardware protection for this case. Default Value: 0

PWR_HIBERNATE

HIBERNATE Mode Register
Address: 0x40261008
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	TOKEN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	UNLOCK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW	RW	RW	None
HW Access	A				A	A	A	None
Name	POLARITY_HIBPIN [23:20]				MASK_HIBWDT	MASK_HIBALARM	FREEZE	None

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW1S	None		RW			
HW Access	A	R	None		A			
Name	HIBERNATE	HIBERNATE_DISABLE	None [29:28]		MASK_HIBPIN [27:24]			

Bits	Name	Description
31	HIBERNATE	Firmware sets this bit to enter HIBERNATE mode. The system will enter HIBERNATE mode immediately after writing to this bit and will wakeup only in response to XRES or WAKEUP event. Both UNLOCK and FREEZE must have been set correctly in a previous write operations. Otherwise, it will not enter HIBERNATE. External supplies must have been stable for 250us before entering HIBERNATE mode. Default Value: 0

30	HIBERNATE_DISABLE	Hibernate disable bit. 0: Normal operation, HIBERNATE works as described 1: Further writes to this register are ignored Note: This bit is a write-once bit until the next reset. Avoid changing any other bits in this register while disabling HIBERNATE mode. Also, it is recommended to clear the UNLOCK code, if it was previously written.. Default Value: 0
27 : 24	MASK_HIBPIN	When set, HIBERNATE will wakeup if the corresponding pin input matches the POLARITY_HIBPIN setting. Each bit corresponds to one of the wakeup pins. Default Value: 0
23 : 20	POLARITY_HIBPIN	Each bit sets the active polarity of the corresponding wakeup pin. 0: Pin input of 0 will wakeup the part from HIBERNATE 1: Pin input of 1 will wakeup the part from HIBERNATE Default Value: 0
19	MASK_HIBWDT	When set, HIBERNATE will wakeup for WDT interrupt Default Value: 0
18	MASK_HIBALARM	When set, HIBERNATE will wakeup for a RTC interrupt Default Value: 0
17	FREEZE	Firmware sets this bit to freeze the configuration, mode and state of all GPIOs and SIOs in the system. When entering HIBERNATE mode, the first write instructs DEEPSLEEP peripherals that they cannot ignore the upcoming freeze command. This occurs even in the illegal condition where UNLOCK is not set. If UNLOCK and HIBERNATE are properly set, the IOs actually freeze on the second write. Supply supervision is disabled during HIBERNATE mode. HIBERNATE peripherals ignore resets (excluding XRES) while FREEZE==1. Default Value: 0
15 : 8	UNLOCK	This byte must be set to 0x3A for FREEZE or HIBERNATE fields to operate. Any other value in this register will cause FREEZE/ HIBERNATE to have no effect, except as noted in the FREEZE description. Default Value: 0

7 : 0	TOKEN	Contains a 8-bit token that is retained through a HIBERNATE/ WAKEUP sequence that can be used by firmware to differentiate WAKEUP from a general RESET event. Note that waking up from HIBERNATE using XRES will reset this register. Default Value: 0

PWR_SSV_CTL

Supply Supervision Control Register
Address: 0x40261018
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None	RW	RW	None		RW
HW Access	R		None	R	A	None		R
Name	BODVDDA_ACTION [7:6]		None	BODVDDA_VSEL	BODVDDD_ENABLE	None [2:1]		BODVDDD_VSEL

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	None		RW
HW Access	None				A	None		A
Name	None [15:12]				BODVCCD_ENABLE	None [10:9]		BODVDDA_ENABLE

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None	RW	RW	None		RW
HW Access	R		None	R	A	None		R
Name	OVDVDDA_ACTION [23:22]		None	OVDVDDA_VSEL	OVDVDDD_ENABLE	None [18:17]		OVDVDDD_VSEL

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW	None		RW
HW Access	None				A	None		A
Name	None [31:28]				OVDVCCD_ENABLE	None [26:25]		OVDVDDA_ENABLE

Bits	Name	Description
27	OVDVCCD_ENABLE	Enable for OVD on vccd. This cannot be disabled during normal operation. Default Value: 1
24	OVDVDDA_ENABLE	Enable for OVD on vdda. Default Value: 0
23 : 22	OVDVDDA_ACTION	Action taken when the OVD on vdda triggers. Default Value: 0
		0x0: NOTHING : No action
		0x1: FAULT : Generate a fault
		0x2: RESET : Reset the chip
20	OVDVDDA_VSEL	Selects the voltage threshold for OVD on vdda. Ensure OVDVDDA_ENABLE==0 before changing this setting to prevent false triggers 0: vddd>5.5V 1: vddd>5.0V Default Value: 0

19	OVDVDDD_ENABLE	Enable for OVD on vddd. This cannot be disabled during normal operation. Default Value: 1
16	OVDVDDD_VSEL	Selects the voltage threshold for OVD on vddd. The OVD does not reliably monitor the supply during the transition. 0: vddd>5.5V 1: vddd>5.0V Default Value: 0
11	BODVCCD_ENABLE	Enable for BOD on vccd. This cannot be disabled during normal operation. Default Value: 1
8	BODVDDA_ENABLE	Enable for BOD on vdda. BODVDDA_ACTION will be triggered when the BOD is disabled. If no action is desired when disabling, firmware must first write BODVDDA_ACTION=NOTHING in a separate write cycle. Default Value: 0
7 : 6	BODVDDA_ACTION	Action taken when the BOD on vdda triggers. Default Value: 0
		0x0: NOTHING : No action
		0x1: FAULT : Generate a fault
		0x2: RESET : Reset the chip
4	BODVDDA_VSEL	Selects the voltage threshold for BOD on vdda. Ensure BODVDDA_ENABLE==0 before changing this setting to prevent false triggers. 0: vdda<2.7V 1: vdda<3.0V Default Value: 0
3	BODVDDD_ENABLE	Enable for BOD on vddd. This cannot be disabled during normal operation. Default Value: 1
0	BODVDDD_VSEL	Selects the voltage threshold for BOD on vddd. The BOD does not reliably monitor the supply during the transition. 0: vddd<2.7V 1: vddd<3.0V Default Value: 0

PWR_SSV_STATUS

Supply Supervision Status Register
Address: 0x4026101C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					RW	RW	RW
Name	None [7:3]					BODVCCD_OK	BODVDDA_OK	BODVDDD_OK

Bits	15	14	13	12	11	10	9	8
SW Access	None					R	R	R
HW Access	None					RW	RW	RW
Name	None [15:11]					OVDVCCD_OK	OVDVDDA_OK	OVDVDDD_OK

Bits	23	22	21	20	19	18	17	16
SW Access	None						R	R
HW Access	None						RW	RW
Name	None [23:18]						OCD_DPSLP_REG_OK	OCD_ACT_LINREG_OK

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	OCD_DPSLP_REG_OK	OCD indicates the current drawn from the linear DeepSleep Regulator is ok. This will always read 1, because a detected over-current condition will reset the chip. Default Value: 1
16	OCD_ACT_LINREG_OK	OCD indicates the current drawn from the linear Active Regulator is ok. This will always read 1, because a detected over-current condition will reset the chip. Default Value: 1
10	OVDVCCD_OK	OVD indicates vccd is ok. This will always read 1, because a detected over-over-voltage condition will reset the chip. Default Value: 1
9	OVDVDDA_OK	OVD indicates vdda is ok. Default Value: 0

8	OVDVDDD_OK	OVD indicates vddd is ok. This will always read 1, because a detected over-voltage condition will reset the chip. Default Value: 1
2	BODVCCD_OK	BOD indicates vccd is ok. This will always read 1, because a detected brownout will reset the chip. Default Value: 1
1	BODVDDA_OK	BOD indicates vdda is ok. Default Value: 0
0	BODVDDD_OK	BOD indicates vddd is ok. This will always read 1, because a detected brownout will reset the chip. Default Value: 1

PWR_LVD_CTL

High Voltage / Low Voltage Detector (HVLVD) Configuration Register
Address: 0x40261020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	None	RW				
HW Access	R	R	None	R				
Name	HVLVD1_EN_HT	HVLVD1_DPSLP_EN_HT	None	HVLVD1_TRIPSEL_HT [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW	RW	
HW Access	None					R	R	
Name	None [23:19]					HVLVD1_ACTION	HVLVD1_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18	HVLVD1_ACTION	Action taken when the threshold is crossed in the programmed directions(s) Default Value: 0
		0x0: INTERRUPT : Generate an interrupt
		0x1: FAULT : Generate a fault
17 : 16	HVLVD1_EDGE_SEL	Sets which edge(s) will trigger an action when the threshold is crossed. Default Value: 0
		0x0: DISABLE : Disabled
		0x1: RISING : Rising edge
		0x2: FALLING : Falling edge
		0x3: BOTH : Both rising and falling edges

15	HVLVD1_EN_HT	Enable HVLVD1 voltage monitor. This detector monitors vddd only. Do not change other HVLVD1 settings when enabled. Default Value: 0
14	HVLVD1_DPSLP_EN_HT	Keep HVLVD1 voltage monitor enabled during DEEPSLEEP mode. This field is only used when HVLVD1_EN_HT==1. Default Value: 0
12 : 8	HVLVD1_TRIPSEL_HT	Threshold selection for HVLVD1 for HT products. Detector accuracy is +/-4% of the nominal values listed below. Disable the detector (HVLVD1_EN=0) before changing the threshold. NOTE: When increasing the trip selection bits, the user must increase by one binary unit in 10us cycle, otherwise there is the potential to generate an HV OVD reset. 0: rise 2.825V (nom), fall=2.8V (nom) 1: rise 2.925V (nom), fall=2.9V (nom) 2: rise 3.025V (nom), fall=3.0V (nom) 3: rise 3.125V (nom), fall=3.1V (nom) 4: rise 3.225V (nom), fall=3.2V (nom) 5: rise 3.325V (nom), fall=3.3V (nom) 6: rise 3.425V (nom), fall=3.4V (nom) 7: rise 3.525V (nom), fall=3.5V (nom) 8: rise 3.625V (nom), fall=3.6V (nom) 9: rise 3.725V (nom), fall=3.7V (nom) 10: rise 3.825V (nom), fall=3.8V (nom) 11: rise 3.925V (nom), fall=3.9V (nom) 12: rise 4.025V (nom), fall=4.0V (nom) 13: rise 4.125V (nom), fall=4.1V (nom) 14: rise 4.225V (nom), fall=4.2V (nom) 15: rise 4.325V (nom), fall=4.3V (nom) 16: rise 4.425V (nom), fall=4.4V (nom) 17: rise 4.525V (nom), fall=4.5V (nom) 18: rise 4.625V (nom), fall=4.6V (nom) 19: rise 4.725V (nom), fall=4.7V (nom) 20: rise 4.825V (nom), fall=4.8V (nom) 21: rise 4.925V (nom), fall=4.9V (nom) 22: rise 5.025V (nom), fall=5.0V (nom) 23: rise 5.125V (nom), fall=5.1V (nom) 24: rise 5.225V (nom), fall=5.2V (nom) 25: rise 5.325V (nom), fall=5.3V (nom) others: reserved Default Value: 0

PWR_LVD_CTL2

High Voltage / Low Voltage Detector (HVLVD) Configuration Register #2
Address: 0x40261024
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	None	RW				
HW Access	R	R	None	R				
Name	HVLVD2_EN_HT	HVLVD2_DPSLP_EN_HT	None	HVLVD2_TRIPSEL_HT [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW	RW	
HW Access	None					R	R	
Name	None [23:19]					HVLVD2_ACTION	HVLVD2_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18	HVLVD2_ACTION	Action taken when the threshold is crossed in the programmed directions(s) Default Value: 0
		0x0: INTERRUPT : Generate an interrupt
		0x1: FAULT : Generate a fault
17 : 16	HVLVD2_EDGE_SEL	Sets which edge(s) will trigger an action when the threshold is crossed. Default Value: 0
		0x0: DISABLE : Disabled
		0x1: RISING : Rising edge
		0x2: FALLING : Falling edge
		0x3: BOTH : Both rising and falling edges

15	HVLVD2_EN_HT	Enable HVLVD2 voltage monitor. This detector monitors vddd only. Do not change other HVLVD2 settings when enabled. Default Value: 0
14	HVLVD2_DPSLP_EN_HT	Keep HVLVD2 voltage monitor enabled during DEEPSLEEP mode. This field is only used when HVLVD1_EN_HT==1. Default Value: 0
12 : 8	HVLVD2_TRIPSEL_HT	Threshold selection for HVLVD2 for HT products. Detector accuracy is +/-4% of the nominal values listed below. Disable the detector (HVLVD1_EN=0) before changing the threshold. NOTE: When increasing the trip selection bits, the user must increase by one binary unit in 10us cycle, otherwise there is the potential to generate an HV OVD reset. 0: rise 2.825V (nom), fall=2.8V (nom) 1: rise 2.925V (nom), fall=2.9V (nom) 2: rise 3.025V (nom), fall=3.0V (nom) 3: rise 3.125V (nom), fall=3.1V (nom) 4: rise 3.225V (nom), fall=3.2V (nom) 5: rise 3.325V (nom), fall=3.3V (nom) 6: rise 3.425V (nom), fall=3.4V (nom) 7: rise 3.525V (nom), fall=3.5V (nom) 8: rise 3.625V (nom), fall=3.6V (nom) 9: rise 3.725V (nom), fall=3.7V (nom) 10: rise 3.825V (nom), fall=3.8V (nom) 11: rise 3.925V (nom), fall=3.9V (nom) 12: rise 4.025V (nom), fall=4.0V (nom) 13: rise 4.125V (nom), fall=4.1V (nom) 14: rise 4.225V (nom), fall=4.2V (nom) 15: rise 4.325V (nom), fall=4.3V (nom) 16: rise 4.425V (nom), fall=4.4V (nom) 17: rise 4.525V (nom), fall=4.5V (nom) 18: rise 4.625V (nom), fall=4.6V (nom) 19: rise 4.725V (nom), fall=4.7V (nom) 20: rise 4.825V (nom), fall=4.8V (nom) 21: rise 4.925V (nom), fall=4.9V (nom) 22: rise 5.025V (nom), fall=5.0V (nom) 23: rise 5.125V (nom), fall=5.1V (nom) 24: rise 5.225V (nom), fall=5.2V (nom) 25: rise 5.325V (nom), fall=5.3V (nom) others: reserved Default Value: 0

PWR_HIB_DATA0

HIBERNATE Data Register
Address: 0x40261040
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	HIB_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	HIB_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	HIB_DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	HIB_DATA [31:24]							

Bits	Name	Description
31 : 0	HIB_DATA	Additional data that is retained through a HIBERNATE/WAKEUP sequence that can be used by firmware for any application-specific purpose. Note that waking up from HIBERNATE using XRES will reset this register. Default Value: 0

CLK_PATH_SELECT0

Clock Path Select Register
Address: 0x40261200
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					PATH_MUX [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	PATH_MUX	Selects a source for clock PATH<i>. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. Default Value: 0
		0x0: IMO : IMO - Internal R/C Oscillator
		0x1: EXTCLK : EXTCLK - External Clock Pin
		0x2: ECO : ECO - External-Crystal Oscillator
		0x3: ALTHF : ALTHF - Alternate High-Frequency clock input (product-specific clock)
		0x4: DSI_MUX : DSI_MUX - Output of DSI mux for this path. Using a DSI source directly as root of HFCLK will result in undefined behavior.

		0x5: LPECO : Reserved. Do not use.

CLK_ROOT_SELECT0

Clock Root Select Register
Address: 0x40261240
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW			
HW Access	None		R		R			
Name	None [7:6]		ROOT_DIV [5:4]		ROOT_MUX [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	A	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Enable for this clock root. All clock roots default to disabled (ENABLE==0) except HFCLK0, which cannot be disabled. Default Value: 0
5 : 4	ROOT_DIV	Selects predivider value for this clock root and DSI input. Default Value: 0
		0x0: NO_DIV : Transparent mode, feed through selected clock source w/o dividing.
		0x1: DIV_BY_2 : Divide selected clock source by 2
		0x2: DIV_BY_4 : Divide selected clock source by 4
		0x3: DIV_BY_8 : Divide selected clock source by 8

3 : 0	ROOT_MUX	Selects a clock path as the root of HFCLK<k> and for SRSS DSI input <k>. Use CLK_PATH_SELECT[i] to configure the desired path. Some paths may have FLL or PLL available (product-specific), and the control and bypass mux selections of these are in other registers. Configure the FLL using CLK_FLL_CONFIG register. Configure a PLL using the related CLK_PLL_CONFIG[k] register. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. Default Value: 0
		0x0: PATH0 : Select PATH0 (can be configured for FLL)
		0x1: PATH1 : Select PATH1 (can be configured for PLL0, if available in the product)
		0x2: PATH2 : Select PATH2 (can be configured for PLL1, if available in the product)
		0x3: PATH3 : Select PATH3 (can be configured for PLL2, if available in the product)
		0x4: PATH4 : Select PATH4 (can be configured for PLL3, if available in the product)
		0x5: PATH5 : Select PATH5 (can be configured for PLL4, if available in the product)
		0x6: PATH6 : Select PATH6 (can be configured for PLL5, if available in the product)
		0x7: PATH7 : Select PATH7 (can be configured for PLL6, if available in the product)
		0x8: PATH8 : Select PATH8 (can be configured for PLL7, if available in the product)
		0x9: PATH9 : Select PATH9 (can be configured for PLL8, if available in the product)
		0xa: PATH10 : Select PATH10 (can be configured for PLL9, if available in the product)

		0xb: PATH11 : Select PATH11 (can be configured for PLL10, if available in the product)
		0xc: PATH12 : Select PATH12 (can be configured for PLL11, if available in the product)
		0xd: PATH13 : Select PATH13 (can be configured for PLL12, if available in the product)
		0xe: PATH14 : Select PATH14 (can be configured for PLL13, if available in the product)
		0xf: PATH15 : Select PATH15 (can be configured for PLL14, if available in the product)

CSV_HF_CSV0_REF_CTL

Clock Supervision Reference Control
Address: 0x40261400
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	STARTUP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	STARTUP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	CSV_EN	CSV_ACTION	None [29:24]					

Bits	Name	Description
31	CSV_EN	Enables clock supervision, both frequency and loss. CSV in Active domain: Clock supervision is reset during DeepSleep and Hibernate modes. When enabled it begins operating automatically after a DeepSleep wakeup, but it must be reconfigured after Hibernate wakeup. CSV in DeepSleep domain: Clock supervision is reset during Hibernate mode. It must be reconfigured after Hibernate wakeup. A CSV error detection is reported to the Fault structure, or instead it can generate a power reset. Default Value: 0
30	CSV_ACTION	Specifies the action taken when an anomaly is detected on the monitored clock. CSV in DeepSleep domain always do a Fault report (which also wakes up the system). Default Value: 0
		0x0: FAULT : Do a Fault report.

		0x1: RESET : Cause a power reset. This should only be used for clk_hf0.
15 : 0	STARTUP	Startup delay time -1 (in reference clock cycles), after enable or DeepSleep wakeup, from reference clock start to monitored clock start. At a minimum (both clocks running): STARTUP >= (PERIOD +3) * FREQ_RATIO - UPPER, with FREQ_RATIO = (Reference frequency / Monitored frequency) On top of that the actual clock startup delay and the margin for accuracy of both clocks must be added. Default Value: 0

CSV_HF_CSV0_REF_LIMIT

Clock Supervision Reference Limits
Address: 0x40261404
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LOWER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	LOWER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	UPPER [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	UPPER [31:24]							

Bits	Name	Description
31 : 16	UPPER	Cycle time upper limit. Set the upper limit -1, in reference clock cycles, before (or same time) the next monitored clock event must happen. If a monitored clock event does not happen before this limit is reached, or does not happen at all (clock loss), a CSV error is detected. Default Value: 0
15 : 0	LOWER	Cycle time lower limit. Set the lower limit -1, in reference clock cycles, before the next monitored clock event is allowed to happen. If a monitored clock event happens before this limit is reached a CSV error is detected. LOWER must be at least 1 less than UPPER. In case the clocks are asynchronous LOWER must be at least 3 less than UPPER. Default Value: 0

CSV_HF_CSV0_MON_CTL

Clock Supervision Monitor Control
Address: 0x40261408
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period time. Set the Period -1, in monitored clock cycles, before the next monitored clock event happens. PERIOD <= (UPPER+1) / FREQ_RATIO -1, with FREQ_RATIO = (Reference frequency / Monitored frequency) In case the clocks are asynchronous: PERIOD <= UPPER / FREQ_RATIO -1 Additionally margin must be added for accuracy of both clocks. Default Value: 0

CLK_SELECT

Clock selection register
Address: 0x40261500
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					A		
Name	None [7:3]					LFCLK_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	PUMP_ENABLE	PUMP_DIV [14:12]			PUMP_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	PUMP_ENABLE	Reserved. Not used in the product. Default Value: 0
14 : 12	PUMP_DIV	Reserved. Not used in the product. Default Value: 0
		0x0: NO_DIV : Reserved. Not used in the product.
		0x1: DIV_BY_2 : Reserved. Not used in the product.
		0x2: DIV_BY_4 : Reserved. Not used in the product.
		0x3: DIV_BY_8 : Reserved. Not used in the product.
		0x4: DIV_BY_16 : Reserved. Not used in the product.
11 : 8	PUMP_SEL	Reserved. Not used the product. Default Value: 0

2 : 0	LFCLK_SEL	Select source for LFCLK. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. Default Value: 0
		0x0: ILO0 : ILO0 - Internal Low-speed Oscillator #0.
		0x1: WCO : WCO - Watch-Crystal Oscillator. Requires Backup domain to be present and properly configured (including external watch crystal, if used).
		0x2: ALTLF : ALTLF - Alternate Low-Frequency Clock. Capability is product-specific
		0x3: PILO : PILO - Precision ILO. If present, it works in DEEPSLEEP and higher modes. Does not work in HIBERNATE mode.
		0x4: ILO1 : ILO1 - Internal Low-speed Oscillator #1, if present.
		0x5: ECO_PRESCALE : ECO_PRESCALE - External-Crystal Oscillator after prescaling in CLK_ECO_PRESCALE. Does not work in DEEPSLEEP or HIBERNATE modes. Intended for applications that operate in ACTIVE/SLEEP modes only. This option is only valid when an ECO present in the product.

CLK_TIMER_CTL

Timer Clock Control Register
Address: 0x40261504
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TIMER_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						TIMER_HF0_DIV [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TIMER_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Enable for TIMERCLK. 0: TIMERCLK is off 1: TIMERCLK is enabled Default Value: 0
23 : 16	TIMER_DIV	Divide selected timer clock source by (1+TIMER_DIV). The output of this divider is TIMERCLK Allows for integer divisions in the range [1, 256]. Do not change this setting while the timer is enabled. Default Value: 7
9 : 8	TIMER_HF0_DIV	Predivider used when HF0_DIV is selected in TIMER_SEL. If HFCLK0 frequency is less than 100MHz and has approximately 50% duty cycle, then no division is required (NO_DIV). Otherwise, select a divide ratio of 2, 4, or 8 before selected HF0_DIV as the timer clock. Default Value: 0

		0x0: NO_DIV : Transparent mode, feed through selected clock source w/o dividing or correcting duty cycle.
		0x1: DIV_BY_2 : Divide HFCLK0 by 2.
		0x2: DIV_BY_4 : Divide HFCLK0 by 4.
		0x3: DIV_BY_8 : Divide HFCLK0 by 8.
0	TIMER_SEL	Select source for TIMERCLK. The output of this mux can be further divided using TIMER_DIV. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. Default Value: 0
		0x0: IMO : IMO - Internal Main Oscillator
		0x1: HF0_DIV : Select the output of the predivider configured by TIMER_HF0_DIV.

CLK_ILO0_CONFIG

ILO0 Configuration
Address: 0x40261508
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							A
Name	None [7:1]							ILO0_BACKUP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	A	A	None					
Name	ENABLE	ILO0_MON_ENABLE	None [29:24]					

Bits	Name	Description
31	ENABLE	Master enable for ILO. Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. HT-variant: This register will not clear unless PWR_CTL2.BGREF_LPMODE==0. After enabling, the first ILO0 cycle occurs within 12us and is +/-10% accuracy. Thereafter, ILO0 is +/-5% accurate. Default Value: 1
30	ILO0_MON_ENABLE	Reserved. Always write a zero. Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. Default Value: 0

0	ILO0_BACKUP	This register indicates that ILO0 should stay enabled during XRES and HIBERNATE modes. If backup voltage domain is implemented on the product, this bit also indicates if ILO0 should stay enabled through power-related resets on other supplies, e.g.. BOD on VDDD/VCCD. Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. This register is reset when the backup logic resets. 0: ILO0 turns off during XRES, HIBERNATE, and power-related resets. ILO0 configuration and trims are reset by these events. 1: ILO0 stays enabled, as described above. ILO0 configuration and trims are not reset by these events. Default Value: 0

CLK_ILO1_CONFIG

ILO1 Configuration
Address: 0x4026150C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	ENABLE	ILO1_MON_ENABLE	None [29:24]					

Bits	Name	Description
31	ENABLE	Master enable for ILO1. HT-variant: After enabling, the first ILO1 cycle occurs within 12us and is +/-10% accuracy. Thereafter, ILO1 is +/-5% accurate. Default Value: 0
30	ILO1_MON_ENABLE	Reserved. Always write a zero. Default Value: 0

CLK_IMO_CONFIG

IMO Configuration
Address: 0x40261518
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Master enable for IMO oscillator. This bit must be high at all times for all functions to work properly. Hardware will automatically disable the IMO during DEEPSLEEP, HIBERNATE, and XRES. Default Value: 1

CLK_ECO_CONFIG

ECO Configuration Register
Address: 0x4026151C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	None
HW Access	None						R	None
Name	None [7:2]						AGC_EN	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None		RW	RW	None		
HW Access	R	None		RW1C	RW1C	None		
Name	ECO_EN	None [30:29]		ECO_DIV_ENABLE	ECO_DIV_DISABLE	None [26:24]		

Bits	Name	Description
31	ECO_EN	Master enable for ECO oscillator. Default Value: 0

28	ECO_DIV_ENABLE	ECO prescaler enable command (mutually exclusive with ECO_DIV_DISABLE). ECO Prescaler only works in ACTIVE and SLEEP modes. SW sets this field to '1' to enable the divider and HW sets this field to '0' to indicate that divider enabling has completed. When the divider is enabled, its integer and fractional counters are initialized to "0". If a divider is to be re-enabled using different integer and fractional divider values, the SW should follow these steps: 0: Disable the divider using the ECO_DIV_DISABLE field. 1: Configure CLK_ECO_PRESCALE registers. 2: Enable the divider using the ECO_DIV_ENABLE field. HW sets the ECO_DIV_ENABLE field to '0' when the enabling is performed and HW set CLK_ECO_PRESCALER.ENABLED to '1' when the enabling is performed. Default Value: 0
27	ECO_DIV_DISABLE	ECO prescaler disable command (mutually exclusive with ECO_DIV_ENABLE). SW sets this field to '1' and HW sets this field to '0'. HW sets ECO_DIV_DISABLE field to '0' immediately and HW sets CLK_ECO_PRESCALE.ECO_DIV_EN field to '0' immediately. Default Value: 0
1	AGC_EN	Automatic Gain Control (AGC) enable. When set, the oscillation amplitude is controlled to the level selected by CLK_ECO_CONFIG2.ATRIM. When low, the amplitude is not explicitly controlled and can be as high as the vddd supply. WARNING: use care when disabling AGC because driving a crystal beyond its rated limit can permanently damage the crystal. Default Value: 1

CLK_ECO_PRESCALE

ECO Prescaler Configuration Register
Address: 0x40261520
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							ECO_DIV_ENABLED

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ECO_FRAC_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ECO_INT_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						ECO_INT_DIV [25:24]	

Bits	Name	Description
25 : 16	ECO_INT_DIV	10-bit integer value allows for ECO frequencies up to 33.55MHz. Subtract one from the desired divide value when writing this field. For example, to divide by 1, write ECO_INT_DIV=0. Do not change this setting when ECO Prescaler is enabled. Default Value: 0
15 : 8	ECO_FRAC_DIV	8-bit fractional value, sufficient to get prescaler output within the +/-65ppm calibration range. Do not change this setting when ECO Prescaler is enabled. Default Value: 0
0	ECO_DIV_ENABLED	ECO prescaler enabled. HW sets this field to '1' as a result of an CLK_ECO_CONFIG.ECO_DIV_ENABLE command. HW sets this field to '0' as a result on a CLK_ECO_CONFIG.ECO_DIV_DISABLE command. Default Value: 0

CLK_ECO_STATUS

ECO Status Register
Address: 0x40261524
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						ECO_READY	ECO_OK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	ECO_READY	Indicates the ECO internal oscillator circuit has had enough time to fully stabilize. This is the output of a counter since ECO was enabled, and it does not check the ECO output. It is recommended to also confirm ECO_OK==1. Default Value: 0
0	ECO_OK	Indicates the ECO internal oscillator circuit has sufficient amplitude. It may not meet the PPM accuracy or duty cycle spec. Default Value: 0

CLK_FLL_CONFIG

FLL Configuration Register
Address: 0x40261530
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FLL_MULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FLL_MULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						FLL_MULT [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						RW
HW Access	R	None						R
Name	FLL_ENABLE	None [30:25]						FLL_OUTPUT_DIV

Bits	Name	Description

31	FLL_ENABLE	Master enable for FLL. The FLL requires firmware sequencing when enabling and disabling. Hardware handles sequencing automatically when entering/ exiting DEEPSLEEP. To enable the FLL, use the following sequence: 1) Configure FLL and CCO settings. Do not modify CLK_FLL_CONFIG3.BYPASS_SEL (must be AUTO) or CLK_FLL_CONFIG.FLL_ENABLE (must be 0). 2) Enable the CCO by writing CLK_FLL_CONFIG4.CCO_ENABLE=1 3) Wait until CLK_FLL_STATUS.CCO_READY==1. 4) Ensure the reference clock has stabilized. 5) Write FLL_ENABLE=1. 6) Optionally wait until CLK_FLL_STATUS.LOCKED==1. The hardware automatically changes to the FLL output when LOCKED==1. To disable the FLL, use the following sequence: 1) Write CLK_FLL_CONFIG3.BYPASS_SEL=FLL_REF. 2) Read CLK_FLL_CONFIG3.BYPASS_SEL to ensure the write completes (read is not optional). 3) Wait at least ten cycles of either FLL reference clock or FLL output clock, whichever is slower. It is recommended to use a HW counter (e.g. clock calibration counter, event generator) running on the slower clock. 4) Disable FLL with FLL_ENABLE=0. 5) Disable the CCO by writing CLK_FLL_CONFIG4.CCO_ENABLE=0. 6) Write CLK_FLL_CONFIG3.BYPASS_SEL=AUTO. 7) Read CLK_FLL_CONFIG3.BYPASS_SEL to ensure the write completes (read is not optional). 8) Wait three cycles of FLL reference clock. It is recommended to use a HW counter (e.g. clock calibration counter, event generator) running on the reference clock. 0: Block is powered off 1: Block is powered on Default Value: 0
24	FLL_OUTPUT_DIV	Control bits for Output divider. Set the divide value before enabling the FLL, and do not change it while FLL is enabled. 0: no division 1: divide by 2 Default Value: 1

17 : 0	FLL_MULT	Multiplier to determine CCO frequency in multiples of the frequency of the selected reference clock (Fref). Ffll = (FLL_MULT) * (Fref / REFERENCE_DIV) / (OUTPUT_DIV+1) Default Value: 0

CLK_FLL_CONFIG2

FLL Configuration Register 2
Address: 0x40261534
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FLL_REF_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			FLL_REF_DIV [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LOCK_TOL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	UPDATE_TOL [31:24]							

Bits	Name	Description
31 : 24	UPDATE_TOL	Update tolerance sets the error threshold for when the FLL will update the CCO frequency settings. The update tolerance is the allowed difference between the count value for the ideal formula and the measured value. UPDATE_TOL should be less than LOCK_TOL. Default Value: 0
23 : 16	LOCK_TOL	Lock tolerance sets the error threshold for when the FLL output is considered locked to the reference input. A high tolerance can be used to lock more quickly or allow less accuracy. The tolerance is the allowed difference between the count value for the ideal formula and the measured value. 0: tolerate error of 1 count value 1: tolerate error of 2 count values ... 255: tolerate error of 256 count values Default Value: 2

12 : 0	FLL_REF_DIV	Control bits for reference divider. Set the divide value before enabling the FLL, and do not change it while FLL is enabled. 0: illegal (undefined behavior) 1: divide by 1 ... 8191: divide by 8191 Default Value: 1

CLK_FLL_CONFIG3

FLL Configuration Register 3
Address: 0x40261538
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	FLL_LF_PGAIN [7:4]				FLL_LF_IGAIN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SETTLING_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			SETTLING_COUNT [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None			
HW Access	None		R		None			
Name	None [31:30]		BYPASS_SEL [29:28]		None [27:24]			

Bits	Name	Description
29 : 28	BYPASS_SEL	Bypass mux located just after FLL output. This register can be written while the FLL is enabled. When changing BYPASS_SEL, do not turn off the reference clock or CCO clock for five cycles (whichever is slower). In case of disabling FLL(FLL_ENABLE=0), additional five cycles are required. Refer to FLL disable sequence for more details in CLK_FLL_CONFIG->FLL_ENABLE. Whenever BYPASS_SEL is changed, it is required to read CLK_FLL_CONFIG3 to ensure the change takes effect. Default Value: 0

		0x0: AUTO : Automatic using lock indicator. When unlocked, automatically selects FLL reference input (bypass mode). When locked, automatically selects FLL output. This can allow some processing to occur while the FLL is locking, such as after DEEPSLEEP wakeup. It is incompatible with clock supervision, because the frequency changes based on the lock signal.
		0x1: LOCKED_OR_NOTHING : Similar to AUTO, except the clock is gated off when unlocked. This is compatible with clock supervision, because the supervisors allow no clock during startup (until a timeout occurs), and the clock targets the proper frequency whenever it is running.
		0x2: FLL_REF : Select FLL reference input (bypass mode). Ignores lock indicator
		0x3: FLL_OUT : Select FLL output. Ignores lock indicator.
20 : 8	SETTLING_COUNT	Number of undivided reference clock cycles to wait after changing the CCO trim until the loop measurement restarts. A delay allows the CCO output to settle and gives a more accurate measurement. The default is tuned to an 8MHz reference clock since the IMO is expected to be the most common use case. 0: no settling time 1: wait one reference clock cycle ... 8191: wait 8191 reference clock cycles Default Value: 40
7 : 4	FLL_LF_PGAIN	FLL Loop Filter Gain Setting #2. The proportional gain is the sum of FLL_LF_IGAIN and FLL_LF_PGAIN. 0: 1/256 1: 1/128 2: 1/64 3: 1/32 4: 1/16 5: 1/8 6: 1/4 7: 1/2 8: 1.0 9: 2.0 10: 4.0 11: 8.0 >=12: illegal Default Value: 0
3 : 0	FLL_LF_IGAIN	FLL Loop Filter Gain Setting #1. The proportional gain is the sum of FLL_LF_IGAIN and FLL_LF_PGAIN. 0: 1/256 1: 1/128 2: 1/64 3: 1/32 4: 1/16 5: 1/8 6: 1/4 7: 1/2 8: 1.0 9: 2.0 10: 4.0 11: 8.0 >=12: illegal Default Value: 0

CLK_FLL_CONFIG4

FLL Configuration Register 4
Address: 0x4026153C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CCO_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					CCO_RANGE [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	CCO_FREQ [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					RW
HW Access	R	R	None					RW
Name	CCO_ENABLE	CCO_HW_UPDATE_DIS	None [29:25]					CCO_FREQ

Bits	Name	Description
31	CCO_ENABLE	Enable the CCO. It is required to enable the CCO before using the FLL. 0: Block is powered off 1: Block is powered on Default Value: 0
30	CCO_HW_UPDATE_DIS	Disable CCO frequency update by FLL hardware 0: Hardware update of CCO settings is allowed. Use this setting for normal FLL operation. 1: Hardware update of CCO settings is disabled. Use this setting for open-loop FLL operation. Default Value: 0
24 : 16	CCO_FREQ	CCO frequency code. This is updated by HW when the FLL is enabled. It can be manually updated to use the CCO in an open loop configuration. The meaning of each frequency code depends on the range. Default Value: 0
10 : 8	CCO_RANGE	Frequency range of CCO Default Value: 0

		0x0: RANGE0 : Target frequency is in range [48, 64) MHz
		0x1: RANGE1 : Target frequency is in range [64, 85) MHz
		0x2: RANGE2 : Target frequency is in range [85, 113) MHz
		0x3: RANGE3 : Target frequency is in range [113, 150) MHz
		0x4: RANGE4 : Target frequency is in range [150, 200] MHz
7 : 0	CCO_LIMIT	Maximum CCO offset allowed (used to prevent FLL dynamics from selecting an CCO frequency that the logic cannot support) Default Value: 0xFF

CLK_FLL_STATUS

FLL Status Register
Address: 0x40261540
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	RW1C	R
HW Access	None					RW	A	W
Name	None [7:3]					CCO_READY	UNLOCK_OCCURRED	LOCKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CCO_READY	This indicates that the CCO is internally settled and ready to use. Default Value: 0
1	UNLOCK_OCCURRED	This bit sets whenever the FLL is enabled and goes out of lock. This bit stays set until cleared by firmware. Default Value: 0
0	LOCKED	FLL Lock Indicator Default Value: 0

CLK_ECO_CONFIG2

ECO Configuration Register 2
Address: 0x40261544
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				None	RW		
HW Access	R				None	R		
Name	ATRIM [7:4]				None	WDTRIM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW			RW		RW	
HW Access	None	R			R		R	
Name	None	GTRIM [14:12]			RTRIM [11:10]		FTRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14 : 12	GTRIM	Gain Trim - Startup time. Default Value: 0
11 : 10	RTRIM	Feedback resistor Trim Default Value: 0
9 : 8	FTRIM	Filter Trim - 3rd harmonic oscillation Default Value: 0

7 : 4	ATRIM	Amplitude trim. Sets maximum oscillation amplitude (Vp) to set the crystal drive level when ECO_CONFIG.AGC_EN=1. When AGC_EN=0, most values of this register are unused, except as noted. WARNING: use care when setting this field because driving a crystal beyond its rated limit can permanently damage the crystal. 0x0: Vp < 0.35V 0x1: Vp < 0.40V 0x2: Vp < 0.45V 0x3: Vp < 0.50V 0x4: Vp < 0.55V 0x5: Vp < 0.60V 0x6: Vp < 0.65V 0x7: Vp < 0.70V 0x8: Vp < 0.75V 0x9: Vp < 0.80V 0xA: Vp < 0.85V 0xB: Vp < 0.90V 0xC: Vp < 0.95V 0xD: Vp < 1.00V 0xE: Vp < 1.05V 0xF: Vp < 1.10V when AGC_EN=1. When AGC_EN=0, this setting enables maximum swing between vddd and vssd. Default Value: 0
2 : 0	WDTRIM	Watch Dog Trim. Sets the minimum oscillation amplitude (Vp) for the crystal drive level. The minimum amplitude detector output is readable in CLK_ECO_STATUS.ECO_OK. 0x0: Vp > 0.05V 0x1: Vp > 0.10V 0x2: Vp > 0.15V 0x3: Vp > 0.20V 0x4: Vp > 0.25V 0x5: Vp > 0.30V 0x6: Vp > 0.35V 0x7: Vp > 0.40V Default Value: 3

CLK_PLL_CONFIG0

PLL Configuration Register
Address: 0x40261600
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	FEEDBACK_DIV [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			REFERENCE_DIV [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			OUTPUT_DIV [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None	RW		RW	RW		None
HW Access	R	None	R		R	R		None
Name	ENABLE	None	BYPASS_SEL [29:28]		PLL_LF_MODE	LOCK_DELAY [26:25]		None

Bits	Name	Description
31	ENABLE	Master enable for PLL. Setup FEEDBACK_DIV, REFERENCE_DIV, and OUTPUT_DIV at least one cycle before setting ENABLE=1. Fpll = (FEEDBACK_DIV) * (Fref / REFERENCE_DIV) / (OUTPUT_DIV) 0: Block is disabled. When the PLL disables, hardware controls the bypass mux as described in BYPASS_SEL, before disabling the PLL circuit. 1: Block is enabled Default Value: 0
29 : 28	BYPASS_SEL	Bypass mux located just after PLL output. This selection is glitch-free and can be changed while the PLL is running. When changing BYPASS_SEL, do not turn off the reference clock or PLL clock for five cycles (whichever is slower). Default Value: 0

		0x0: AUTO : Automatic using lock indicator. When unlocked, automatically selects PLL reference input (bypass mode). When locked, automatically selects PLL output. If ENABLE=0, automatically selects PLL reference input.
		0x1: LOCKED_OR_NOTHING : Similar to AUTO, except the clock is gated off when unlocked. This is compatible with clock supervision, because the supervisors allow no clock during startup (until a timeout occurs), and the clock targets the proper frequency whenever it is running. If ENABLE=0, no clock is output.
		0x2: PLL_REF : Select PLL reference input (bypass mode). Ignores lock indicator
		0x3: PLL_OUT : Select PLL output. Ignores lock indicator. If ENABLE=0, no clock is output.
27	PLL_LF_MODE	VCO frequency range selection. Configure this bit according to the targeted VCO frequency. Do not change this setting while the PLL is enabled. 0: VCO frequency is [200MHz, 400MHz] 1: VCO frequency is [170MHz, 200MHz) Default Value: 0
26 : 25	LOCK_DELAY	Configures the sensitivity of the lock detection logic. 0: normal operation 1: reduced sensitivity to allow tracking a modulating reference clock. When this option is selected, configure Fvco=320MHz. The PLL can track the a reference clock frequency that modulates within +/-4% at a rate of Fref/1000 MHz. 2,3: reserved (do not use) Default Value: 0
20 : 16	OUTPUT_DIV	Control bits for Output divider. Set the divide value before enabling the PLL, and do not change it while PLL is enabled. 0: illegal (undefined behavior) 1: illegal (undefined behavior) 2: divide by 2. Suitable for direct usage as HFCLK source. ... 16: divide by 16. Suitable for direct usage as HFCLK source. >16: illegal (undefined behavior) Default Value: 2

12 : 8	REFERENCE_DIV	Control bits for reference divider. Set the divide value before enabling the PLL, and do not change it while PLL is enabled. 0: illegal (undefined behavior) 1: divide by 1 ... 20: divide by 20 others: illegal (undefined behavior) Default Value: 1
6 : 0	FEEDBACK_DIV	Control bits for feedback divider. Set the divide value before enabling the PLL, and do not change it while PLL is enabled. 0-21: illegal (undefined behavior) 22: divide by 22 ... 112: divide by 112 >112: illegal (undefined behavior) Default Value: 22

CLK_PLL_STATUS0

PLL Status Register
Address: 0x40261640
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	R
HW Access	None						A	W
Name	None [7:2]						UNLOCK_OCCURRED	LOCKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	UNLOCK_OCCURRED	This bit sets whenever the PLL Lock bit goes low, and stays set until cleared by firmware. Default Value: 0
0	LOCKED	PLL Lock Indicator Default Value: 0

CSV_REF_SEL

Select CSV Reference clock for Active domain
Address: 0x40261700
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					REF_MUX [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	REF_MUX	Selects a source for clock clk_ref_hf. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. Default Value: 0
		0x0: IMO : IMO - Internal R/C Oscillator
		0x1: EXTCLK : EXTCLK - External Clock Pin
		0x2: ECO : ECO - External-Crystal Oscillator
		0x3: ALTHF : ALTHF - Alternate High-Frequency clock input (product-specific clock)

CSV_LF_CSV_REF_CTL

Clock Supervision Reference Control
Address: 0x40261720
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	STARTUP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	CSV_EN	None [30:24]						

Bits	Name	Description
31	CSV_EN	Enables clock supervision, both frequency and loss. CSV in Active domain: Clock supervision is reset during DeepSleep and Hibernate modes. When enabled it begins operating automatically after a DeepSleep wakeup, but it must be reconfigured after Hibernate wakeup. CSV in DeepSleep domain: Clock supervision is reset during Hibernate mode. It must be reconfigured after Hibernate wakeup. CSV in Backup domain: Clock supervision operates during Hibernate mode, can be configured to wake from Hibernate, and continues operating during reboot. A CSV error detection is reported to the Fault structure. Default Value: 0

7 : 0	STARTUP	Startup delay time -1 (in reference clock cycles), after enable, from reference clock start to monitored clock start. At a minimum (both clocks running): STARTUP >= (PERIOD +3) * FREQ_RATIO - UPPER, with FREQ_RATIO = (Reference frequency / Monitored frequency) On top of that the actual clock startup delay and the margin for accuracy of both clocks must be added. Default Value: 0

CSV_LF_CSV_REF_LIMIT

Clock Supervision Reference Limits
Address: 0x40261724
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LOWER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	UPPER [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	UPPER	Cycle time upper limit. Set the upper limit -1, in reference clock cycles, before (or same time) the next monitored clock event must happen. If a monitored clock event does not happen before this limit is reached, or does not happen at all (clock loss), a CSV error is detected. Default Value: 0
7 : 0	LOWER	Cycle time lower limit. Set the lower limit -1, in reference clock cycles, before the next monitored clock event is allowed to happen. If a monitored clock event happens before this limit is reached a CSV error is detected. LOWER must be at least 1 less than UPPER. In case the clocks are asynchronous LOWER must be at least 3 less than UPPER. Default Value: 0

CSV_LF_CSV_MON_CTL

Clock Supervision Monitor Control
Address: 0x40261728
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PERIOD	Period time. Set the Period -1, in monitored clock cycles, before the next monitored clock event happens. PERIOD <= (UPPER+1) / FREQ_RATIO -1, with FREQ_RATIO = (Reference frequency / Monitored frequency) In case the clocks are asynchronous: PERIOD <= UPPER / FREQ_RATIO -1 Additionally margin must be added for accuracy of both clocks. Default Value: 0

RES_CAUSE

Reset Cause Observation Register
Address: 0x40261800
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	RESET_MCWDT2	RESET_MCWDT1	RESET_MCWDT0	RESET_SOFT	RESET_TC_DBGRESET	RESET_DPSLP_FAULT	RESET_ACT_FAULT	RESET_WDT

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							RESET_MCWDT3

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	RESET_OCD_ACT_LINREG	RESET_OVDVCCD	RESET_OVDVDDA	RESET_OVDVDDD	RESET_BODVCCD	RESET_BODVDDA	RESET_BODVDDD	RESET_XRES

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW1C	RW1C	RW1C	None			RW1C
HW Access	None	A	A	A	None			A
Name	None	RESET_PORVDDD	RESET_STRUCT_XRES	RESET_PXRES	None [27:25]			RESET_OCD_DPSLP_LINREG

Bits	Name	Description
30	RESET_PORVDDD	Indicator that a POR occurred. This is a high-voltage cause bit, and hardware clears the other bits when this one is set. It does not block further recording of other high-voltage causes. Default Value: 1
29	RESET_STRUCT_XRES	Structural reset was asserted. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. This bit is not blocked by other HV cause bits. Default Value: 0

28	RESET_PXRES	PXRES triggered. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. This bit is not blocked by other HV cause bits. Default Value: 0
24	RESET_OCD_DPSLP_LINREG	Overcurrent detection on the internal VCCD supply when supplied by the DEEPSLEEP power mode linear regulator. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. Default Value: 0
23	RESET_OCD_ACT_LINREG	Overcurrent detection on the internal VCCD supply when supplied by the ACTIVE power mode linear regulator. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. Default Value: 0
22	RESET_OVDVCCD	Overvoltage detection on the internal core VCCD supply. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. Default Value: 0
21	RESET_OVDVDDA	Overvoltage detection on the external VDDA supply. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. Default Value: 0
20	RESET_OVDVDDD	Overvoltage detection on the external VDDD supply. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. Default Value: 0

19	RESET_BODVCCD	Internal VCCD core supply crossed the brown-out limit. Note that this detector will detect gross issues with the internal core supply, but may not catch all brown-out conditions. Functional and timing supervision (CSV, WDT) is provided to create fully failsafe internal crash detection. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. Default Value: 0
18	RESET_BODVDDA	External VDDA supply crossed the brown-out limit. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. Default Value: 0
17	RESET_BODVDDD	External VDDD supply crossed brown-out limit. Note that this cause will only be observable as long as the VDDD supply does not go below the POR (power on reset) detection limit. Below this limit it is not possible to reliably retain information in the device. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. Default Value: 0
16	RESET_XRES	External XRES pin was asserted. This is a high-voltage cause bit that blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. This bit is not blocked by other HV cause bits. Default Value: 0
8	RESET_MCWDT3	Multi-Counter Watchdog timer reset #3. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). Default Value: 0
7	RESET_MCWDT2	Multi-Counter Watchdog timer reset #2. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). Default Value: 0

6	RESET_MCWDT1	Multi-Counter Watchdog timer reset #1. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). Default Value: 0
5	RESET_MCWDT0	Multi-Counter Watchdog timer reset #0. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). Default Value: 0
4	RESET_SOFT	A CPU requested a system reset through it's SYSRESETREQ. This can be done via a debugger probe or in firmware. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). Default Value: 0
3	RESET_TC_DBGRESET	Test controller or debugger asserted reset. Only resets debug domain. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). Default Value: 0
2	RESET_DPSLP_FAULT	Fault logging system requested a reset from its DeepSleep logic. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). Default Value: 0
1	RESET_ACT_FAULT	Fault logging system requested a reset from its Active logic. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). Default Value: 0
0	RESET_WDT	A basic WatchDog Timer (WDT) reset has occurred since last power cycle. ULP products: This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). For products that support high-voltage cause detection, this bit blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. This bit is not blocked by other HV cause bits. Default Value: 0

RES_CAUSE2

Reset Cause Observation Register 2
Address: 0x40261804
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	A							
Name	RESET_CSV_HF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	A							
Name	RESET_CSV_HF [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW1C
HW Access	None							A
Name	None [23:17]							RESET_CSV_REF

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	RESET_CSV_REF	Clock supervision logic requested a reset due to loss or frequency violation of the reference clock source that is used to monitor the other HF clock sources. Default Value: 0
15 : 0	RESET_CSV_HF	Clock supervision logic requested a reset due to loss or frequency violation of a high-frequency clock. Each bit index K corresponds to a HFCLK<K>. Unimplemented clock bits return zero. Default Value: 0

CLK_TRIM_ILO0_CTL

ILO0 Trim Register
Address: 0x40263014
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		A					
Name	None [7:6]		ILO0_FTRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				A			
Name	None [15:12]				ILO0_MONTRIM [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 8	ILO0_MONTRIM	ILO0 internal monitor trim. Default Value: 0x5
5 : 0	ILO0_FTRIM	ILO0 frequency trims. LSB step size is 1.5% (typical) of the frequency. Default Value: 0x2C

CLK_TRIM_ILO1_CTL

ILO1 Trim Register
Address: 0x40263220
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		ILO1_FTRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				ILO1_MONTRIM [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 8	ILO1_MONTRIM	ILO1 internal monitor trim. Default Value: 0x5
5 : 0	ILO1_FTRIM	ILO1 frequency trims. LSB step size is 1.5% (typical) of the frequency. Default Value: 0x2C

MCWDT0_CTR0_CTL

MCWDT Subcounter Control Register
Address: 0x40268000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							ENABLED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Enable subcounter. May take up to 2 clk_lf cycles to take effect. When ENABLE changes from 1->0, the counter is cleared. 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Default Value: 0
0	ENABLED	Indicates actual state of this subcounter. May lag ENABLE by up to two clk_lf cycles. Default Value: 0

MCWDT0_CTR0_LOWER_LIMIT

MCWDT Subcounter Lower Limit Register
Address: 0x40268004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LOWER_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	LOWER_LIMIT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	LOWER_LIMIT	Lower limit for this MCWDT subcounter. See LOWER_ACTION. Default Value: 0

MCWDT0_CTR0_UPPER_LIMIT

MCWDT Subcounter Upper Limit Register
Address: 0x40268008
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	UPPER_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	UPPER_LIMIT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	UPPER_LIMIT	Upper limit for this MCWDT subcounter. See UPPER_ACTION. Default Value: 0

MCWDT0_CTR0_WARN_LIMIT

MCWDT Subcounter Warn Limit Register
Address: 0x4026800C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WARN_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WARN_LIMIT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	WARN_LIMIT	Warn limit for this MCWDT subcounter. See WARN_ACTION. Default Value: 0

MCWDT0_CTR0_CONFIG

MCWDT Subcounter Configuration Register
Address: 0x40268010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		None		RW	
HW Access	None		R		None		R	
Name	None [7:6]		UPPER_ACTION [5:4]		None [3:2]		LOWER_ACTION [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None			RW
HW Access	None			R	None			R
Name	None [15:13]			AUTO_SERVICE	None [11:9]			WARN_ACTION

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	RW	None			
HW Access	R	R	None	R	None			
Name	DEBUG_RUN	SLEEPDEEP_PAUSE	None	DEBUG_TRIGGER_EN	None [27:24]			

Bits	Name	Description

31	DEBUG_RUN	Pauses/runs this counter while a debugger is connected. Other behaviors are unchanged during debugging, including service, configuration updates and enable/disable. Note it may take up to two clk_lf cycles for the counter to pause, due to internal synchronization. When (DEBUG_RUN==1 or DEBUG_TRIGGER_EN==0) and the debugger is connected for at least two clk_lf cycles, the LOWER_ACTION is ignored until after the first service after the debugger is disconnected. After the debugger is disconnected, the LOWER_ACTION is ignored until after the first service. This prevents an unintentional trigger of the LOWER_ACTION before the firmware realigns the servicing period. After the first service, LOWER_ACTION behaves as configured. If the debugger is disconnected before two clk_lf cycles, the LOWER_ACTION may or may not be ignored. 0: When debugger connected, counter pauses incrementing as configured in DEBUG_TRIGGER_EN. 1: When debugger connected, counter increments normally, but reset generation is blocked. To block LOWER_ACTION fault generation, write DEBUG_TRIGGER_EN==0. Default Value: 0
30	SLEEPDEEP_PAUSE	Pauses/runs this counter when the corresponding processor is in SLEEPDEEP. Note it may take up to two clk_lf cycles for the counter to pause and up to two clk_lf cycles for it to unpause, due to internal synchronization. After wakeup, the LOWER_ACTION is ignored until after the first service. This prevents an unintentional trigger of the LOWER_ACTION before the firmware realigns the servicing period. After the first service, LOWER_ACTION behaves as configured. 0: Counter runs normally regardless of processor mode. 1: Counter pauses when corresponding processor is in SLEEPDEEP. Default Value: 0

28	DEBUG_TRIGGER_EN	Enables the trigger input for this MCWDT to pause the counter during debug mode. To pause at a breakpoint while debugging, configure the trigger matrix to connect the related CPU halted signal to the trigger input for this MCWDT, and then set this bit. It takes up to two clk_lf cycles for the trigger signal to be processed. Triggers that are less than two clk_lf cycles may be missed. Synchronization errors can accumulate each time it is halted. 0: Pauses the counter whenever a debug probe is connected. 1: Pauses the counter whenever a debug probe is connected and the trigger input is high. Default Value: 0
12	AUTO_SERVICE	Automatically service when the count value reaches WARN_LIMIT. This allows creation of a periodic interrupt if this counter is not needed as a watchdog. This field is ignored when LOWER_ACTION<>NOTHING or when UPPER_ACTION<>NOTHING. Default Value: 0
8	WARN_ACTION	Action taken when the count value reaches WARN_LIMIT. The minimum setting to achieve a periodic interrupt is WARN_LIMIT==1. A setting of zero will trigger once but not periodically. For WARN_LIMIT >= 2: The action is triggered on same edge when it meets this condition. For WARN_LIMIT == [0,1] : The action may take up to one extra clk_lf cycle to trigger. Default Value: 0
		0x0: NOTHING : Do nothing
		0x1: INT : Trigger an interrupt.
5 : 4	UPPER_ACTION	Action taken if this watchdog is not serviced before UPPER_LIMIT is reached. The counter stops counting when UPPER_LIMIT is reached, regardless of UPPER_ACTION setting. UPPER_ACTION is ignored (i.e. treated as NOTHING) when a debugger is connected. Default Value: 0

		0x0: NOTHING : Do nothing
		0x1: FAULT : Trigger a fault. For UPPER_LIMIT >= 2: The action is triggered on same edge when it meets this condition. For UPPER_LIMIT < 2: The action may take up to one extra clk_lf cycle to trigger.
		0x2: FAULT_THEN_RESET : Trigger a fault. Further, trigger a system-wide reset if the fault is not serviced and the watchdog is not cleared within 6 clk_lf cycles. It can take up to 3 clk_lf cycles for the fault to be transferred to the fault manager, which gives at least 3 clk_lf cycles for software to respond. For UPPER_LIMIT >= 2: The action is triggered on same edge when it meets this condition. For UPPER_LIMIT < 2: The action may take up to one extra clk_lf cycle to trigger.
1 : 0	LOWER_ACTION	Action taken if this watchdog is serviced before LOWER_LIMIT is reached. LOWER_ACTION is ignored (i.e. treated as NOTHING) when a debugger is connected and/or when the corresponding processor is in SLEEPDEEP. Default Value: 0
		0x0: NOTHING : Do nothing
		0x1: FAULT : Trigger a fault. It can take up to 3 clk_lf cycles for the fault to be transferred to the fault manager. For LOWER_LIMIT >= 1: The action is triggered on same edge when it meets this condition. For LOWER_LIMIT == 0: No action is triggered.
		0x2: FAULT_THEN_RESET : Trigger a fault. Further, trigger a system-wide reset if the fault is not serviced and the watchdog is not cleared within 6 clk_lf cycles. It can take up to 3 clk_lf cycles for the fault to be transferred to the fault manager, which gives at least 3 clk_lf cycles for software to respond. For LOWER_LIMIT >= 1: The action is triggered on same edge when it meets this condition. For LOWER_LIMIT == 0: No action is triggered.

MCWDT0_CTR0_CNT

MCWDT Subcounter Count Register
Address: 0x40268014
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	CNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	CNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CNT	Current value of subcounter for this MCWDT. This field may lag the actual count value by up to one clk_lf cycle, due to internal synchronization. When this subcounter is disabled and unlocked, the count value can be written for verification and debugging purposes. Software writes are always ignored when the subcounter is enabled. This register retains information during DeepSleep mode if SLEEPDEEP_PAUSE == 1. Default Value: 0

MCWDT0_CPU_SELECT

MCWDT CPU selection register
Address: 0x40268040
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						CPU_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	CPU_SEL	Assigns this MCWDT to a CPU. This selects which CPU SLEEPDEEP signal is used for SLEEPDEEP_PAUSE. Default Value: 0

MCWDT0_CTR2_CTL

MCWDT Subcounter 2 Control register
Address: 0x40268080
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							ENABLED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Enable subcounter. May take up to 2 clk_lf cycles to take effect. When ENABLE changes from 1->0, the counter is cleared. 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Default Value: 0
0	ENABLED	Indicates actual state of this subcounter. May lag ENABLE by up to two clk_lf cycles. Default Value: 0

MCWDT0_CTR2_CONFIG

MCWDT Subcounter 2 Configuration register
Address: 0x40268084
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							ACTION

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			BITS [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	RW	None			
HW Access	R	R	None	R	None			
Name	DEBUG_RUN	SLEEPDEEP_PAUSE	None	DEBUG_TRIGGER_EN	None [27:24]			

Bits	Name	Description
31	DEBUG_RUN	Pauses/runs this counter while a debugger is connected. Other behaviors are unchanged during debugging, including service, configuration updates and enable/disable. Note it may take up to two clk_lf cycles for the counter to pause and another two cycles to unpause, due to internal synchronization. 0: When debugger connected, counter pauses incrementing as configured in DEBUG_TRIGGER_EN. 1: When debugger connected, counter increments normally, but reset generation is blocked. Default Value: 0

30	SLEEPDEEP_PAUSE	Pauses/runs this counter when the corresponding processor is in SLEEPDEEP. Note it may take up to two clk_lf cycles for the counter to pause and up to two clk_lf cycles for it to unpause, due to internal synchronization. 0: Counter runs normally regardless of processor mode. 1: Counter pauses when corresponding processor is in SLEEPDEEP. Default Value: 0
28	DEBUG_TRIGGER_EN	Enables the trigger input for this MCWDT to pause the counter during debug mode. To pause at a breakpoint while debugging, configure the trigger matrix to connect the related CPU halted signal to the trigger input for this MCWDT, and then set this bit. It takes up to two clk_lf cycles for the trigger signal to be processed. Triggers that are less than two clk_lf cycles may be missed. Synchronization errors can accumulate each time it is halted. 0: Pauses the counter whenever a debug probe is connected. 1: Pauses the counter whenever a debug probe is connected and the trigger input is high. Default Value: 0
20 : 16	BITS	Bit to observe for a toggle: 0: Do ACTION after CNT[0] toggles (i.e. every tick) . 31: Do ACTION after CNT[31] toggles (i.e. every 2^31 ticks) Default Value: 0
0	ACTION	Action taken when the specified BIT toggles. Action will be triggered on the same edge where BITS to observe toggle. Default Value: 0
		0x0: NOTHING : Do nothing
		0x1: INT : Trigger an interrupt

MCWDT0_CTR2_CNT

MCWDT Subcounter 2 Count Register
Address: 0x40268088
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	CNT2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	CNT2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	CNT2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	CNT2 [31:24]							

Bits	Name	Description
31 : 0	CNT2	Current value of subcounter 2 for this MCWDT. This field may lag the actual count value by up to one clk_lf cycle, due to internal synchronization. When this subcounter is disabled and unlocked, the count value can be written for verification and debugging purposes. Software writes are always ignored when the subcounter is enabled. This register retains information during DeepSleep mode if SLEEPDEEP_PAUSE == 1. Default Value: 0

MCWDT0_LOCK

MCWDT Lock Register
Address: 0x40268090
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						A	
Name	None [7:2]						MCWDT_LOCK [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	MCWDT_LOCK	Prohibits writing control and configuration registers related to this MCWDT when not equal 0 (as specified in the other register descriptions). Requires at least two different writes to unlock. Note that this field is 2 bits to force multiple writes only. Each MCWDT has a separate local lock. Default Value: 0
		0x0: NO_CHG : No effect
		0x1: CLR0 : Clears bit 0
		0x2: CLR1 : Clears bit 1
		0x3: SET01 : Sets both bits 0 and 1

MCWDT0_SERVICE

MCWDT Service Register
Address: 0x40268094
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						RW1C	RW1C
Name	None [7:2]						CTR1_SERVICE	CTR0_SERVICE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CTR1_SERVICE	Services subcounter 1. This resets the count value for subcounter 1 to zero. This may take up to three clk_lf cycles to take effect. Hardware clears this bit, after necessary synchronization. To ensure a pending CTR1_SERVICE write is reflected, firmware should wait until this bit reads low before attempting to write CTR1_SERVICE=1. If subcounter 1 is disabled, CTR1_SERVICE will not trigger a LOWER_ACTION and will not clear a preloaded count value. Default Value: 0

0	CTR0_SERVICE	Services subcounter 0. This resets the count value for subcounter 0 to zero. This may take up to three clk_lf cycles to take effect. Hardware clears this bit, after necessary synchronization. To ensure a pending CTR0_SERVICE write is reflected, firmware should wait until this bit reads low before attempting to write CTR0_SERVICE=1. If subcounter 0 is disabled, CTR0_SERVICE will not trigger a LOWER_ACTION and will not clear a preloaded count value. Default Value: 0

MCWDT0_INTR

MCWDT Interrupt Register
Address: 0x402680A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					A	A	A
Name	None [7:3]					CTR2_INT	CTR1_INT	CTR0_INT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CTR2_INT	MCWDT Interrupt Request for sub-counter 2. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Default Value: 0
1	CTR1_INT	MCWDT Interrupt Request for sub-counter 1. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Default Value: 0
0	CTR0_INT	MCWDT Interrupt Request for sub-counter 0. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Default Value: 0

MCWDT0_INTR_SET

MCWDT Interrupt Set Register
Address: 0x402680A4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [7:3]					CTR2_INT	CTR1_INT	CTR0_INT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CTR2_INT	Set interrupt for MCWDT_INT2 Default Value: 0
1	CTR1_INT	Set interrupt for MCWDT_INT1 Default Value: 0
0	CTR0_INT	Set interrupt for MCWDT_INT0 Default Value: 0

MCWDT0_INTR_MASK

MCWDT Interrupt Mask Register
Address: 0x402680A8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					CTR2_INT	CTR1_INT	CTR0_INT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CTR2_INT	Interrupt Mask for sub-counter 2. The bit controls if the interrupt is forwarded to the CPU. The interrupt is blocked when the value of the bit is 0. The interrupt is forwarded if the value of the bit is 1. Default Value: 0
1	CTR1_INT	Interrupt Mask for sub-counter 1 for warning interrupt. The bit controls if the interrupt is forwarded to the CPU. The interrupt is blocked when the value of the bit is 0. The interrupt is forwarded if the value of the bit is 1. Default Value: 0
0	CTR0_INT	Interrupt Mask for sub-counter 0 for warning interrupt. The bit controls if the interrupt is forwarded to the CPU. The interrupt is blocked when the value of the bit is 0. The interrupt is forwarded if the value of the bit is 1. Default Value: 0

MCWDT0_INTR_MASKED

MCWDT Interrupt Masked Register
Address: 0x402680AC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					RW	RW	RW
Name	None [7:3]					CTR2_INT	CTR1_INT	CTR0_INT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CTR2_INT	Logical and of corresponding request and mask bits. Default Value: 0
1	CTR1_INT	Logical and of corresponding request and mask bits. Default Value: 0
0	CTR0_INT	Logical and of corresponding request and mask bits. Default Value: 0

WDT_CTL

WDT Control Register
Address: 0x4026C000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							ENABLED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	A	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Enable watchdog. May take up to three clk_ilo0 cycles to take effect. When ENABLE changes from 1->0, the counter is cleared. Do not enter DEEPSLEEP or HIBERNATE mode if ENABLE<>ENABLED. This can be done by waiting until ENABLE==ENABLED whenever ENABLE is changed. 0: Counter is disabled (not clocked). 1: Counter is enabled (counting up) Default Value: 1
0	ENABLED	Indicates actual state of watchdog. May lag ENABLE by up to three clk_ilo0 cycles. Default Value: 1

WDT_LOWER_LIMIT

WDT Lower Limit Register
Address: 0x4026C004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	LOWER_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	LOWER_LIMIT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	LOWER_LIMIT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	LOWER_LIMIT [31:24]							

Bits	Name	Description
31 : 0	LOWER_LIMIT	Lower limit for watchdog. See LOWER_ACTION. Default Value: 0

WDT_UPPER_LIMIT

WDT Upper Limit Register
Address: 0x4026C008
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	UPPER_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	UPPER_LIMIT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	UPPER_LIMIT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	UPPER_LIMIT [31:24]							

Bits	Name	Description
31 : 0	UPPER_LIMIT	Upper limit for watchdog. See UPPER_ACTION. Default Value: 0x8000

WDT_WARN_LIMIT

WDT Warn Limit Register
Address: 0x4026C00C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	WARN_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	WARN_LIMIT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	WARN_LIMIT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	WARN_LIMIT [31:24]							

Bits	Name	Description
31 : 0	WARN_LIMIT	Warn limit for watchdog. See WARN_ACTION. Default Value: 0

WDT_CONFIG

WDT Configuration Register
Address: 0x4026C010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None			RW
HW Access	None			A	None			A
Name	None [7:5]			UPPER_ACTION	None [3:1]			LOWER_ACTION

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None			RW
HW Access	None			A	None			A
Name	None [15:13]			AUTO_SERVICE	None [11:9]			WARN_ACTION

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	None			
HW Access	A	A	A	A	None			
Name	DEBUG_RUN	HIB_PAUSE	DPSLP_PAUSE	DEBUG_TRIGGER_EN	None [27:24]			

Bits	Name	Description

31	DEBUG_RUN	Pauses/runs this counter while a debugger is connected. Other behaviors are unchanged during debugging, including service, configuration updates and enable/disable. Note it may take up to two clk_ilo0 cycles for the counter to pause and another two cycles to unpause, due to internal synchronization. If the debugger is connected for at least two clk_ilo0 cycles, the LOWER_ACTION is ignored until after the first service after the debugger is disconnected. This prevents an unintentional trigger of the LOWER_ACTION before the firmware realigns the servicing period. After the first service, LOWER_ACTION behaves as configured. If the debugger is disconnected before two clk_ilo0 cycles, the LOWER_ACTION may or may not be ignored. 0: When debugger connected, counter pauses incrementing as configured in DEBUG_TRIGGER_EN. 1: When debugger connected, counter increments normally, but reset generation is blocked. Default Value: 0
30	HIB_PAUSE	Pauses/runs this counter when the system is in HIBERNATE. Note it may take up to two clk_ilo0 cycles for the counter to pause, due to internal synchronization. After wakeup, the LOWER_ACTION is ignored until after the first service. This prevents an unintentional trigger of the LOWER_ACTION before the firmware realigns the servicing period. After the first service, LOWER_ACTION behaves as configured. 0: Counter behaves normally during HIBERNATE. 1: Counter pauses during HIBERNATE. Default Value: 0

29	DPSLP_PAUSE	Pauses/runs this counter when the system is in DEEPSLEEP. Note it may take up to two clk_ilo0 cycles for the counter to pause, due to internal synchronization. During DEEPSLEEP wakeup, the pause request is removed when clk_hf0 starts clocking, and then it may take up to two clk_ilo0 cycles for the counter to start. After wakeup, the LOWER_ACTION is ignored until after the first service. This prevents an unintentional trigger of the LOWER_ACTION before the firmware realigns the servicing period. After the first service, LOWER_ACTION behaves as configured. 0: Counter behaves normally during DEEPSLEEP. 1: Counter pauses during DEEPSLEEP. Default Value: 0
28	DEBUG_TRIGGER_EN	Enables the trigger input for WDT to pause the counter during debug mode. To pause at a breakpoint while debugging, configure the trigger matrix to connect the related CPU halted signal to the trigger input for this WDT, and then set this bit. It takes up to two clk_ilo0 cycles for the trigger signal to be processed. Triggers that are less than two clk_ilo0 cycles may be missed. Synchronization error can accumulate each time it is halted. 0: Pauses the counter whenever a debug probe is connected. 1: Pauses the counter whenever a debug probe is connected and the trigger input is high. Default Value: 0
12	AUTO_SERVICE	Automatically service when the count value reaches WARN_LIMIT. This allows creation of a periodic interrupt if this counter is not needed as a watchdog. This field is ignored when LOWER_ACTION<>NOTHING or when UPPER_ACTION<>NOTHING. Default Value: 0

8	WARN_ACTION	Action taken when the count value reaches WARN_LIMIT. The minimum setting to achieve a periodic interrupt is WARN_LIMIT==1. A setting of zero will trigger once but not periodically. For WARN_LIMIT >= 2: The action is triggered on same edge when it meets this condition. For WARN_LIMIT < 2 : The action may take up to one extra clk_ilo0 cycle to trigger. Default Value: 0
		0x0: NOTHING : Do nothing
		0x1: INT : Trigger an interrupt.
4	UPPER_ACTION	Action taken if this watchdog is not serviced before UPPER_LIMIT is reached. The counter stops counting when UPPER_LIMIT is reached, regardless of UPPER_ACTION setting. UPPER_ACTION is ignored (i.e. treated as NOTHING) when a debugger is connected. For UPPER_LIMIT >= 2: The action is triggered on same edge when it meets this condition. For UPPER_LIMIT < 2: The action may take up to one extra clk_ilo0 cycle to trigger. Default Value: 1
		0x0: NOTHING : Do nothing
		0x1: RESET : Trigger a reset.
0	LOWER_ACTION	Action taken if this watchdog is serviced before LOWER_LIMIT is reached. LOWER_ACTION is ignored (i.e. treated as NOTHING) when a debugger is connected and/or when the chip is in DEEPSLEEP/HIBERNATE modes. For LOWER_LIMIT >= 1: The action is triggered on same edge when it meets this condition. For LOWER_LIMIT == 0: No action is triggered. Default Value: 0
		0x0: NOTHING : Do nothing
		0x1: RESET : Trigger a reset.

WDT_CNT

WDT Count Register
Address: 0x4026C014
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	CNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	CNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	CNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	CNT [31:24]							

Bits	Name	Description
31 : 0	CNT	Current value of subcounter for this WDT. This field may lag the actual count value by up to one clk_ilo0 cycle, due to internal synchronization. When this subcounter is disabled and unlocked, the count value can be written for verification and debugging purposes. Software writes are always ignored when the subcounter is enabled. This register retains information during DeepSleep or Hiberbate mode if DPSLP_PAUSE == 1 or HIB_PAUSE == 1. Default Value: 0

WDT_LOCK

WDT Lock register
Address: 0x4026C040
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						A	
Name	None [7:2]						WDT_LOCK [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	WDT_LOCK	Prohibits writing control and configuration registers related to this WDT when not equal 0 (as specified in the other register descriptions). Requires at least two different writes to unlock. Note that this field is 2 bits to force multiple writes only. This register also locks the clk_ilo0 settings. Default Value: 3
		0x0: NO_CHG : No effect
		0x1: CLR0 : Clears bit 0
		0x2: CLR1 : Clears bit 1
		0x3: SET01 : Sets both bits 0 and 1

WDT_SERVICE

WDT Service register
Address: 0x4026C044
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							SERVICE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	SERVICE	Services the watchdog. This resets the count value to zero. This may take up to three clk_ilo0 cycle to take effect. Hardware clears this bit, after necessary synchronization. To ensure a pending SERVICE write is reflected, firmware should wait until this bit reads low before attempting to write SERVICE=1. If WDT is disabled, SERVICE will not trigger a LOWER_ACTION and will not clear a preloaded count value. Default Value: 0

WDT_INTR

WDT Interrupt Register
Address: 0x4026C050
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							A
Name	None [7:1]							WDT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	WDT	WDT Interrupt Request. This bit is set as configured by WDT action and limits. Due to internal synchronization, it takes up to 8 SYSCLK cycles to update after a W1C or reading this register and during this time AHB bus is stalled. Default Value: 0

WDT_INTR_SET

WDT Interrupt Set Register
Address: 0x4026C054
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							WDT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	WDT	Set interrupt. Due to internal synchronization, it takes up to 8 SYSCLK cycles to update after a W1S or reading from this register and during this time AHB bus is stalled. Default Value: 0

WDT_INTR_MASK

WDT Interrupt Mask Register
Address: 0x4026C058
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							WDT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	WDT	Mask for watchdog timer. Clearing this bit will not forward the interrupt to the CPU. Default Value: 0

WDT_INTR_MASKED

WDT Interrupt Masked Register
Address: 0x4026C05C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							WDT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	WDT	Logical and of corresponding request and mask bits. Due to internal synchronization, it takes up to 8 SYSCLK cycles to read from this register. During this time AHB bus is stalled. Default Value: 0

9 Peripheral

Register details

Register name	Address	Description
PERI_TIMEOUT_CTL	0x40000200	Timeout control
PERI_TR_CMD	0x40000220	Trigger command
PERI_DIV_CMD	0x40000400	Divider command
PERI_CLOCK_CTL0	0x40000C00	Clock control. This is the starting address of a register bank containing 110 registers (PERI_CLOCK_CTL0 to PERI_CLOCK_CTL109).
PERI_DIV_8_CTL0	0x40001000	Divider control (for 8.0 divider). This is the starting address of a register bank containing 32 registers (PERI_DIV_8_CTL0 to PERI_DIV_8_CTL31).
PERI_DIV_16_CTL0	0x40001400	Divider control (for 16.0 divider)
PERI_DIV_16_CTL1	0x40001404	Divider control (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL2	0x40001408	Divider control (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL3	0x4000140C	Divider control (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL4	0x40001410	Divider control (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL5	0x40001414	Divider control (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL6	0x40001418	Divider control (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL7	0x4000141C	Divider control (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL8	0x40001420	Divider control (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL9	0x40001424	Divider control (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL10	0x40001428	Divider control (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL11	0x4000142C	Divider control (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL12	0x40001430	Divider control (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL13	0x40001434	Divider control (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL14	0x40001438	Divider control (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL15	0x4000143C	Divider control (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_24_5_CTL0	0x40001C00	Divider control (for 24.5 divider)

Register name	Address	Description
PERI_DIV_24_5_CTL1	0x40001C04	Divider control (for 24.5 divider). See PERI_DIV_24_5_CTL0 for the details of bit fields.
PERI_DIV_24_5_CTL2	0x40001C08	Divider control (for 24.5 divider). See PERI_DIV_24_5_CTL0 for the details of bit fields.
PERI_DIV_24_5_CTL3	0x40001C0C	Divider control (for 24.5 divider). See PERI_DIV_24_5_CTL0 for the details of bit fields.
PERI_DIV_24_5_CTL4	0x40001C10	Divider control (for 24.5 divider). See PERI_DIV_24_5_CTL0 for the details of bit fields.
PERI_DIV_24_5_CTL5	0x40001C14	Divider control (for 24.5 divider). See PERI_DIV_24_5_CTL0 for the details of bit fields.
PERI_DIV_24_5_CTL6	0x40001C18	Divider control (for 24.5 divider). See PERI_DIV_24_5_CTL0 for the details of bit fields.
PERI_DIV_24_5_CTL7	0x40001C1C	Divider control (for 24.5 divider). See PERI_DIV_24_5_CTL0 for the details of bit fields.
PERI_ECC_CTL	0x40002000	ECC control
PERI_GR0_SL_CTL	0x40004010	Slave control
PERI_GR1_SL_CTL	0x40004030	Slave control
PERI_GR2_SL_CTL	0x40004050	Slave control
PERI_GR3_CLOCK_CTL	0x40004060	Clock control
PERI_GR3_SL_CTL	0x40004070	Slave control
PERI_GR5_CLOCK_CTL	0x400040A0	Clock control. See PERI_GR3_CLOCK_CTL for the details of bit fields.
PERI_GR5_SL_CTL	0x400040B0	Slave control
PERI_GR6_CLOCK_CTL	0x400040C0	Clock control. See PERI_GR3_CLOCK_CTL for the details of bit fields.
PERI_GR6_SL_CTL	0x400040D0	Slave control
PERI_GR9_CLOCK_CTL	0x40004120	Clock control. See PERI_GR3_CLOCK_CTL for the details of bit fields.
PERI_GR9_SL_CTL	0x40004130	Slave control. See PERI_GR1_SL_CTL for the details of bit fields.
PERI_TR_GR0_TR_CTL0	0x40008000	Trigger control register
PERI_TR_GR0_TR_CTL1	0x40008004	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR0_TR_CTL2	0x40008008	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR0_TR_CTL3	0x4000800C	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR0_TR_CTL4	0x40008010	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR0_TR_CTL5	0x40008014	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR0_TR_CTL6	0x40008018	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.

Register name	Address	Description
PERI_TR_GR0_TR_CTL7	0x4000801C	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_CTL0	0x40008400	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_CTL1	0x40008404	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_CTL2	0x40008408	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_CTL3	0x4000840C	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_CTL4	0x40008410	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_CTL5	0x40008414	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_CTL6	0x40008418	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_CTL7	0x4000841C	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_CTL0	0x40008800	Trigger control register
PERI_TR_GR2_TR_CTL1	0x40008804	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_CTL2	0x40008808	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_CTL3	0x4000880C	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_CTL0	0x40008C00	Trigger control register
PERI_TR_GR3_TR_CTL1	0x40008C04	Trigger control register. See PERI_TR_GR3_TR_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_CTL2	0x40008C08	Trigger control register. See PERI_TR_GR3_TR_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_CTL3	0x40008C0C	Trigger control register. See PERI_TR_GR3_TR_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_CTL4	0x40008C10	Trigger control register. See PERI_TR_GR3_TR_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_CTL5	0x40008C14	Trigger control register. See PERI_TR_GR3_TR_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_CTL6	0x40008C18	Trigger control register. See PERI_TR_GR3_TR_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_CTL7	0x40008C1C	Trigger control register. See PERI_TR_GR3_TR_CTL0 for the details of bit fields.
PERI_TR_GR4_TR_CTL0	0x40009000	Trigger control register
PERI_TR_GR4_TR_CTL1	0x40009004	Trigger control register. See PERI_TR_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_GR4_TR_CTL2	0x40009008	Trigger control register. See PERI_TR_GR4_TR_CTL0 for the details of bit fields.

Register name	Address	Description
PERI_TR_GR4_TR_CTL3	0x4000900C	Trigger control register. See PERI_TR_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_GR4_TR_CTL4	0x40009010	Trigger control register. See PERI_TR_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_GR4_TR_CTL5	0x40009014	Trigger control register. See PERI_TR_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_GR4_TR_CTL6	0x40009018	Trigger control register. See PERI_TR_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_GR4_TR_CTL7	0x4000901C	Trigger control register. See PERI_TR_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_GR4_TR_CTL8	0x40009020	Trigger control register. See PERI_TR_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_GR4_TR_CTL9	0x40009024	Trigger control register. See PERI_TR_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_GR4_TR_CTL10	0x40009028	Trigger control register. See PERI_TR_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_GR4_TR_CTL11	0x4000902C	Trigger control register. See PERI_TR_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_GR4_TR_CTL12	0x40009030	Trigger control register. See PERI_TR_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_GR4_TR_CTL13	0x40009034	Trigger control register. See PERI_TR_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_GR4_TR_CTL14	0x40009038	Trigger control register. See PERI_TR_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_GR4_TR_CTL15	0x4000903C	Trigger control register. See PERI_TR_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_GR5_TR_CTL0	0x40009400	Trigger control register
PERI_TR_GR5_TR_CTL1	0x40009404	Trigger control register. See PERI_TR_GR5_TR_CTL0 for the details of bit fields.
PERI_TR_GR5_TR_CTL2	0x40009408	Trigger control register. See PERI_TR_GR5_TR_CTL0 for the details of bit fields.
PERI_TR_GR5_TR_CTL3	0x4000940C	Trigger control register. See PERI_TR_GR5_TR_CTL0 for the details of bit fields.
PERI_TR_GR5_TR_CTL4	0x40009410	Trigger control register. See PERI_TR_GR5_TR_CTL0 for the details of bit fields.
PERI_TR_GR5_TR_CTL5	0x40009414	Trigger control register. See PERI_TR_GR5_TR_CTL0 for the details of bit fields.
PERI_TR_GR5_TR_CTL6	0x40009418	Trigger control register. See PERI_TR_GR5_TR_CTL0 for the details of bit fields.
PERI_TR_GR5_TR_CTL7	0x4000941C	Trigger control register. See PERI_TR_GR5_TR_CTL0 for the details of bit fields.
PERI_TR_GR5_TR_CTL8	0x40009420	Trigger control register. See PERI_TR_GR5_TR_CTL0 for the details of bit fields.
PERI_TR_GR5_TR_CTL9	0x40009424	Trigger control register. See PERI_TR_GR5_TR_CTL0 for the details of bit fields.

Register name	Address	Description
PERI_TR_GR5_TR_CTL10	0x40009428	Trigger control register. See PERI_TR_GR5_TR_CTL0 for the details of bit fields.
PERI_TR_GR6_TR_CTL0	0x40009800	Trigger control register
PERI_TR_GR6_TR_CTL1	0x40009804	Trigger control register. See PERI_TR_GR6_TR_CTL0 for the details of bit fields.
PERI_TR_GR6_TR_CTL2	0x40009808	Trigger control register. See PERI_TR_GR6_TR_CTL0 for the details of bit fields.
PERI_TR_GR6_TR_CTL3	0x4000980C	Trigger control register. See PERI_TR_GR6_TR_CTL0 for the details of bit fields.
PERI_TR_GR6_TR_CTL4	0x40009810	Trigger control register. See PERI_TR_GR6_TR_CTL0 for the details of bit fields.
PERI_TR_GR6_TR_CTL5	0x40009814	Trigger control register. See PERI_TR_GR6_TR_CTL0 for the details of bit fields.
PERI_TR_GR6_TR_CTL6	0x40009818	Trigger control register. See PERI_TR_GR6_TR_CTL0 for the details of bit fields.
PERI_TR_GR6_TR_CTL7	0x4000981C	Trigger control register. See PERI_TR_GR6_TR_CTL0 for the details of bit fields.
PERI_TR_GR6_TR_CTL8	0x40009820	Trigger control register. See PERI_TR_GR6_TR_CTL0 for the details of bit fields.
PERI_TR_GR6_TR_CTL9	0x40009824	Trigger control register. See PERI_TR_GR6_TR_CTL0 for the details of bit fields.
PERI_TR_GR6_TR_CTL10	0x40009828	Trigger control register. See PERI_TR_GR6_TR_CTL0 for the details of bit fields.
PERI_TR_GR6_TR_CTL11	0x4000982C	Trigger control register. See PERI_TR_GR6_TR_CTL0 for the details of bit fields.
PERI_TR_GR7_TR_CTL0	0x40009C00	Trigger control register
PERI_TR_GR7_TR_CTL1	0x40009C04	Trigger control register. See PERI_TR_GR7_TR_CTL0 for the details of bit fields.
PERI_TR_GR7_TR_CTL2	0x40009C08	Trigger control register. See PERI_TR_GR7_TR_CTL0 for the details of bit fields.
PERI_TR_GR7_TR_CTL3	0x40009C0C	Trigger control register. See PERI_TR_GR7_TR_CTL0 for the details of bit fields.
PERI_TR_GR7_TR_CTL4	0x40009C10	Trigger control register. See PERI_TR_GR7_TR_CTL0 for the details of bit fields.
PERI_TR_GR7_TR_CTL5	0x40009C14	Trigger control register. See PERI_TR_GR7_TR_CTL0 for the details of bit fields.
PERI_TR_GR8_TR_CTL0	0x4000A000	Trigger control register
PERI_TR_GR8_TR_CTL1	0x4000A004	Trigger control register. See PERI_TR_GR8_TR_CTL0 for the details of bit fields.
PERI_TR_GR8_TR_CTL2	0x4000A008	Trigger control register. See PERI_TR_GR8_TR_CTL0 for the details of bit fields.
PERI_TR_GR8_TR_CTL3	0x4000A00C	Trigger control register. See PERI_TR_GR8_TR_CTL0 for the details of bit fields.
PERI_TR_GR8_TR_CTL4	0x4000A010	Trigger control register. See PERI_TR_GR8_TR_CTL0 for the details of bit fields.

Register name	Address	Description
PERI_TR_GR8_TR_CTL5	0x4000A014	Trigger control register. See PERI_TR_GR8_TR_CTL0 for the details of bit fields.
PERI_TR_GR8_TR_CTL6	0x4000A018	Trigger control register. See PERI_TR_GR8_TR_CTL0 for the details of bit fields.
PERI_TR_GR8_TR_CTL7	0x4000A01C	Trigger control register. See PERI_TR_GR8_TR_CTL0 for the details of bit fields.
PERI_TR_GR8_TR_CTL8	0x4000A020	Trigger control register. See PERI_TR_GR8_TR_CTL0 for the details of bit fields.
PERI_TR_GR8_TR_CTL9	0x4000A024	Trigger control register. See PERI_TR_GR8_TR_CTL0 for the details of bit fields.
PERI_TR_GR9_TR_CTL0	0x4000A400	Trigger control register
PERI_TR_GR9_TR_CTL1	0x4000A404	Trigger control register. See PERI_TR_GR9_TR_CTL0 for the details of bit fields.
PERI_TR_GR9_TR_CTL2	0x4000A408	Trigger control register. See PERI_TR_GR9_TR_CTL0 for the details of bit fields.
PERI_TR_GR9_TR_CTL3	0x4000A40C	Trigger control register. See PERI_TR_GR9_TR_CTL0 for the details of bit fields.
PERI_TR_GR9_TR_CTL4	0x4000A410	Trigger control register. See PERI_TR_GR9_TR_CTL0 for the details of bit fields.
PERI_TR_GR10_TR_CTL0	0x4000A800	Trigger control register. See PERI_TR_GR9_TR_CTL0 for the details of bit fields.
PERI_TR_GR10_TR_CTL1	0x4000A804	Trigger control register. See PERI_TR_GR9_TR_CTL0 for the details of bit fields.
PERI_TR_GR10_TR_CTL2	0x4000A808	Trigger control register. See PERI_TR_GR9_TR_CTL0 for the details of bit fields.
PERI_TR_GR10_TR_CTL3	0x4000A80C	Trigger control register. See PERI_TR_GR9_TR_CTL0 for the details of bit fields.
PERI_TR_GR10_TR_CTL4	0x4000A810	Trigger control register. See PERI_TR_GR9_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR0_TR_CTL0	0x4000C000	Trigger control register
PERI_TR_1TO1_GR0_TR_CTL1	0x4000C004	Trigger control register. See PERI_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR0_TR_CTL2	0x4000C008	Trigger control register. See PERI_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR0_TR_CTL3	0x4000C00C	Trigger control register. See PERI_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR0_TR_CTL4	0x4000C010	Trigger control register. See PERI_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR0_TR_CTL5	0x4000C014	Trigger control register. See PERI_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.

Register name	Address	Description
PERI_TR_1TO1_GR0_TR_CTL6	0x4000C018	Trigger control register. See PERI_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR0_TR_CTL7	0x4000C01C	Trigger control register. See PERI_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR1_TR_CTL0	0x4000C400	Trigger control register. This is the starting address of a register bank containing 64 registers (PERI_TR_1TO1_GR1_TR_CTL0 to PERI_TR_1TO1_GR1_TR_CTL63).
PERI_TR_1TO1_GR2_TR_CTL0	0x4000C800	Trigger control register. This is the starting address of a register bank containing 64 registers (PERI_TR_1TO1_GR2_TR_CTL0 to PERI_TR_1TO1_GR2_TR_CTL63). See PERI_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR3_TR_CTL0	0x4000CC00	Trigger control register. This is the starting address of a register bank containing 64 registers (PERI_TR_1TO1_GR3_TR_CTL0 to PERI_TR_1TO1_GR3_TR_CTL63). See PERI_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR4_TR_CTL0	0x4000D000	Trigger control register
PERI_TR_1TO1_GR4_TR_CTL1	0x4000D004	Trigger control register. See PERI_TR_1TO1_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR4_TR_CTL2	0x4000D008	Trigger control register. See PERI_TR_1TO1_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR4_TR_CTL3	0x4000D00C	Trigger control register. See PERI_TR_1TO1_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR4_TR_CTL4	0x4000D010	Trigger control register. See PERI_TR_1TO1_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR4_TR_CTL5	0x4000D014	Trigger control register. See PERI_TR_1TO1_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR4_TR_CTL6	0x4000D018	Trigger control register. See PERI_TR_1TO1_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR4_TR_CTL7	0x4000D01C	Trigger control register. See PERI_TR_1TO1_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR4_TR_CTL8	0x4000D020	Trigger control register. See PERI_TR_1TO1_GR4_TR_CTL0 for the details of bit fields.

Register name	Address	Description
PERI_TR_1TO1_GR5_TR_CTL0	0x4000D400	Trigger control register. See PERI_TR_1TO1_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR5_TR_CTL1	0x4000D404	Trigger control register. See PERI_TR_1TO1_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR5_TR_CTL2	0x4000D408	Trigger control register. See PERI_TR_1TO1_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR5_TR_CTL3	0x4000D40C	Trigger control register. See PERI_TR_1TO1_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR5_TR_CTL4	0x4000D410	Trigger control register. See PERI_TR_1TO1_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR5_TR_CTL5	0x4000D414	Trigger control register. See PERI_TR_1TO1_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR5_TR_CTL6	0x4000D418	Trigger control register. See PERI_TR_1TO1_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR5_TR_CTL7	0x4000D41C	Trigger control register. See PERI_TR_1TO1_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR5_TR_CTL8	0x4000D420	Trigger control register. See PERI_TR_1TO1_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR6_TR_CTL0	0x4000D800	Trigger control register
PERI_TR_1TO1_GR6_TR_CTL1	0x4000D804	Trigger control register. See PERI_TR_1TO1_GR6_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR6_TR_CTL2	0x4000D808	Trigger control register. See PERI_TR_1TO1_GR6_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR7_TR_CTL0	0x4000DC00	Trigger control register. See PERI_TR_1TO1_GR6_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR7_TR_CTL1	0x4000DC04	Trigger control register. See PERI_TR_1TO1_GR6_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR7_TR_CTL2	0x4000DC08	Trigger control register. See PERI_TR_1TO1_GR6_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR8_TR_CTL0	0x4000E000	Trigger control register
PERI_TR_1TO1_GR8_TR_CTL1	0x4000E004	Trigger control register. See PERI_TR_1TO1_GR8_TR_CTL0 for the details of bit fields.

Register name	Address	Description
PERI_TR_1TO1_GR8_TR_CTL2	0x4000E008	Trigger control register. See PERI_TR_1TO1_GR8_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR8_TR_CTL3	0x4000E00C	Trigger control register. See PERI_TR_1TO1_GR8_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR8_TR_CTL4	0x4000E010	Trigger control register. See PERI_TR_1TO1_GR8_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR8_TR_CTL5	0x4000E014	Trigger control register. See PERI_TR_1TO1_GR8_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR8_TR_CTL6	0x4000E018	Trigger control register. See PERI_TR_1TO1_GR8_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR8_TR_CTL7	0x4000E01C	Trigger control register. See PERI_TR_1TO1_GR8_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR8_TR_CTL8	0x4000E020	Trigger control register. See PERI_TR_1TO1_GR8_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR8_TR_CTL9	0x4000E024	Trigger control register. See PERI_TR_1TO1_GR8_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR8_TR_CTL10	0x4000E028	Trigger control register. See PERI_TR_1TO1_GR8_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR8_TR_CTL11	0x4000E02C	Trigger control register. See PERI_TR_1TO1_GR8_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR8_TR_CTL12	0x4000E030	Trigger control register. See PERI_TR_1TO1_GR8_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR8_TR_CTL13	0x4000E034	Trigger control register. See PERI_TR_1TO1_GR8_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR8_TR_CTL14	0x4000E038	Trigger control register. See PERI_TR_1TO1_GR8_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR8_TR_CTL15	0x4000E03C	Trigger control register. See PERI_TR_1TO1_GR8_TR_CTL0 for the details of bit fields.
PERI_MS_PPU_PR0_SL_ADDR	0x40010000	Slave region, base address
PERI_MS_PPU_PR0_SL_SIZE	0x40010004	Slave region, size
PERI_MS_PPU_PR0_SL_ATT0	0x40010010	Slave attributes 0
PERI_MS_PPU_PR0_SL_ATT1	0x40010014	Slave attributes 1
PERI_MS_PPU_PR0_SL_ATT2	0x40010018	Slave attributes 2

Register name	Address	Description
PERI_MS_PPU_PR0_SL_ATT3	0x4001001C	Slave attributes 3
PERI_MS_PPU_PR0_MS_ADDR	0x40010020	Master region, base address
PERI_MS_PPU_PR0_MS_SIZE	0x40010024	Master region, size
PERI_MS_PPU_PR0_MS_ATT0	0x40010030	Master attributes 0
PERI_MS_PPU_PR0_MS_ATT1	0x40010034	Master attributes 1
PERI_MS_PPU_PR0_MS_ATT2	0x40010038	Master attributes 2
PERI_MS_PPU_PR0_MS_ATT3	0x4001003C	Master attributes 3
PERI_MS_PPU_PR1_SL_ADDR	0x40010040	Slave region, base address. See PERI_MS_PPU_PR0_SL_ADDR for the details of bit fields.
PERI_MS_PPU_PR1_SL_SIZE	0x40010044	Slave region, size. See PERI_MS_PPU_PR0_SL_SIZE for the details of bit fields.
PERI_MS_PPU_PR1_SL_ATT0	0x40010050	Slave attributes 0. See PERI_MS_PPU_PR0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_PR1_SL_ATT1	0x40010054	Slave attributes 1. See PERI_MS_PPU_PR0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_PR1_SL_ATT2	0x40010058	Slave attributes 2. See PERI_MS_PPU_PR0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_PR1_SL_ATT3	0x4001005C	Slave attributes 3. See PERI_MS_PPU_PR0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_PR1_MS_ADDR	0x40010060	Master region, base address
PERI_MS_PPU_PR1_MS_SIZE	0x40010064	Master region, size. See PERI_MS_PPU_PR0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_PR1_MS_ATT0	0x40010070	Master attributes 0. See PERI_MS_PPU_PR0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_PR1_MS_ATT1	0x40010074	Master attributes 1. See PERI_MS_PPU_PR0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_PR1_MS_ATT2	0x40010078	Master attributes 2. See PERI_MS_PPU_PR0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_PR1_MS_ATT3	0x4001007C	Master attributes 3. See PERI_MS_PPU_PR0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_PR2_SL_ADDR	0x40010080	Slave region, base address. See PERI_MS_PPU_PR0_SL_ADDR for the details of bit fields.
PERI_MS_PPU_PR2_SL_SIZE	0x40010084	Slave region, size. See PERI_MS_PPU_PR0_SL_SIZE for the details of bit fields.
PERI_MS_PPU_PR2_SL_ATT0	0x40010090	Slave attributes 0. See PERI_MS_PPU_PR0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_PR2_SL_ATT1	0x40010094	Slave attributes 1. See PERI_MS_PPU_PR0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_PR2_SL_ATT2	0x40010098	Slave attributes 2. See PERI_MS_PPU_PR0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_PR2_SL_ATT3	0x4001009C	Slave attributes 3. See PERI_MS_PPU_PR0_SL_ATT3 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_PR2_MS_ADDR	0x400100A0	Master region, base address
PERI_MS_PPU_PR2_MS_SIZE	0x400100A4	Master region, size. See PERI_MS_PPU_PR0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_PR2_MS_ATT0	0x400100B0	Master attributes 0. See PERI_MS_PPU_PR0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_PR2_MS_ATT1	0x400100B4	Master attributes 1. See PERI_MS_PPU_PR0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_PR2_MS_ATT2	0x400100B8	Master attributes 2. See PERI_MS_PPU_PR0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_PR2_MS_ATT3	0x400100BC	Master attributes 3. See PERI_MS_PPU_PR0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_PR3_SL_ADDR	0x400100C0	Slave region, base address. See PERI_MS_PPU_PR0_SL_ADDR for the details of bit fields.
PERI_MS_PPU_PR3_SL_SIZE	0x400100C4	Slave region, size. See PERI_MS_PPU_PR0_SL_SIZE for the details of bit fields.
PERI_MS_PPU_PR3_SL_ATT0	0x400100D0	Slave attributes 0. See PERI_MS_PPU_PR0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_PR3_SL_ATT1	0x400100D4	Slave attributes 1. See PERI_MS_PPU_PR0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_PR3_SL_ATT2	0x400100D8	Slave attributes 2. See PERI_MS_PPU_PR0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_PR3_SL_ATT3	0x400100DC	Slave attributes 3. See PERI_MS_PPU_PR0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_PR3_MS_ADDR	0x400100E0	Master region, base address
PERI_MS_PPU_PR3_MS_SIZE	0x400100E4	Master region, size. See PERI_MS_PPU_PR0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_PR3_MS_ATT0	0x400100F0	Master attributes 0. See PERI_MS_PPU_PR0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_PR3_MS_ATT1	0x400100F4	Master attributes 1. See PERI_MS_PPU_PR0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_PR3_MS_ATT2	0x400100F8	Master attributes 2. See PERI_MS_PPU_PR0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_PR3_MS_ATT3	0x400100FC	Master attributes 3. See PERI_MS_PPU_PR0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_PR4_SL_ADDR	0x40010100	Slave region, base address. See PERI_MS_PPU_PR0_SL_ADDR for the details of bit fields.
PERI_MS_PPU_PR4_SL_SIZE	0x40010104	Slave region, size. See PERI_MS_PPU_PR0_SL_SIZE for the details of bit fields.
PERI_MS_PPU_PR4_SL_ATT0	0x40010110	Slave attributes 0. See PERI_MS_PPU_PR0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_PR4_SL_ATT1	0x40010114	Slave attributes 1. See PERI_MS_PPU_PR0_SL_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_PR4_SL_ATT2	0x40010118	Slave attributes 2. See PERI_MS_PPU_PR0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_PR4_SL_ATT3	0x4001011C	Slave attributes 3. See PERI_MS_PPU_PR0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_PR4_MS_ADDR	0x40010120	Master region, base address
PERI_MS_PPU_PR4_MS_SIZE	0x40010124	Master region, size. See PERI_MS_PPU_PR0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_PR4_MS_ATT0	0x40010130	Master attributes 0. See PERI_MS_PPU_PR0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_PR4_MS_ATT1	0x40010134	Master attributes 1. See PERI_MS_PPU_PR0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_PR4_MS_ATT2	0x40010138	Master attributes 2. See PERI_MS_PPU_PR0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_PR4_MS_ATT3	0x4001013C	Master attributes 3. See PERI_MS_PPU_PR0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_PR5_SL_ADDR	0x40010140	Slave region, base address. See PERI_MS_PPU_PR0_SL_ADDR for the details of bit fields.
PERI_MS_PPU_PR5_SL_SIZE	0x40010144	Slave region, size. See PERI_MS_PPU_PR0_SL_SIZE for the details of bit fields.
PERI_MS_PPU_PR5_SL_ATT0	0x40010150	Slave attributes 0. See PERI_MS_PPU_PR0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_PR5_SL_ATT1	0x40010154	Slave attributes 1. See PERI_MS_PPU_PR0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_PR5_SL_ATT2	0x40010158	Slave attributes 2. See PERI_MS_PPU_PR0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_PR5_SL_ATT3	0x4001015C	Slave attributes 3. See PERI_MS_PPU_PR0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_PR5_MS_ADDR	0x40010160	Master region, base address
PERI_MS_PPU_PR5_MS_SIZE	0x40010164	Master region, size. See PERI_MS_PPU_PR0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_PR5_MS_ATT0	0x40010170	Master attributes 0. See PERI_MS_PPU_PR0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_PR5_MS_ATT1	0x40010174	Master attributes 1. See PERI_MS_PPU_PR0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_PR5_MS_ATT2	0x40010178	Master attributes 2. See PERI_MS_PPU_PR0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_PR5_MS_ATT3	0x4001017C	Master attributes 3. See PERI_MS_PPU_PR0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_PR6_SL_ADDR	0x40010180	Slave region, base address. See PERI_MS_PPU_PR0_SL_ADDR for the details of bit fields.
PERI_MS_PPU_PR6_SL_SIZE	0x40010184	Slave region, size. See PERI_MS_PPU_PR0_SL_SIZE for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_PR6_SL_ATT0	0x40010190	Slave attributes 0. See PERI_MS_PPU_PR0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_PR6_SL_ATT1	0x40010194	Slave attributes 1. See PERI_MS_PPU_PR0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_PR6_SL_ATT2	0x40010198	Slave attributes 2. See PERI_MS_PPU_PR0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_PR6_SL_ATT3	0x4001019C	Slave attributes 3. See PERI_MS_PPU_PR0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_PR6_MS_ADDR	0x400101A0	Master region, base address
PERI_MS_PPU_PR6_MS_SIZE	0x400101A4	Master region, size. See PERI_MS_PPU_PR0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_PR6_MS_ATT0	0x400101B0	Master attributes 0. See PERI_MS_PPU_PR0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_PR6_MS_ATT1	0x400101B4	Master attributes 1. See PERI_MS_PPU_PR0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_PR6_MS_ATT2	0x400101B8	Master attributes 2. See PERI_MS_PPU_PR0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_PR6_MS_ATT3	0x400101BC	Master attributes 3. See PERI_MS_PPU_PR0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_PR7_SL_ADDR	0x400101C0	Slave region, base address. See PERI_MS_PPU_PR0_SL_ADDR for the details of bit fields.
PERI_MS_PPU_PR7_SL_SIZE	0x400101C4	Slave region, size. See PERI_MS_PPU_PR0_SL_SIZE for the details of bit fields.
PERI_MS_PPU_PR7_SL_ATT0	0x400101D0	Slave attributes 0. See PERI_MS_PPU_PR0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_PR7_SL_ATT1	0x400101D4	Slave attributes 1. See PERI_MS_PPU_PR0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_PR7_SL_ATT2	0x400101D8	Slave attributes 2. See PERI_MS_PPU_PR0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_PR7_SL_ATT3	0x400101DC	Slave attributes 3. See PERI_MS_PPU_PR0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_PR7_MS_ADDR	0x400101E0	Master region, base address
PERI_MS_PPU_PR7_MS_SIZE	0x400101E4	Master region, size. See PERI_MS_PPU_PR0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_PR7_MS_ATT0	0x400101F0	Master attributes 0. See PERI_MS_PPU_PR0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_PR7_MS_ATT1	0x400101F4	Master attributes 1. See PERI_MS_PPU_PR0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_PR7_MS_ATT2	0x400101F8	Master attributes 2. See PERI_MS_PPU_PR0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_PR7_MS_ATT3	0x400101FC	Master attributes 3. See PERI_MS_PPU_PR0_MS_ATT3 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_PR8_SL_ADDR	0x40010200	Slave region, base address. See PERI_MS_PPU_PR0_SL_ADDR for the details of bit fields.
PERI_MS_PPU_PR8_SL_SIZE	0x40010204	Slave region, size. See PERI_MS_PPU_PR0_SL_SIZE for the details of bit fields.
PERI_MS_PPU_PR8_SL_ATT0	0x40010210	Slave attributes 0. See PERI_MS_PPU_PR0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_PR8_SL_ATT1	0x40010214	Slave attributes 1. See PERI_MS_PPU_PR0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_PR8_SL_ATT2	0x40010218	Slave attributes 2. See PERI_MS_PPU_PR0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_PR8_SL_ATT3	0x4001021C	Slave attributes 3. See PERI_MS_PPU_PR0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_PR8_MS_ADDR	0x40010220	Master region, base address
PERI_MS_PPU_PR8_MS_SIZE	0x40010224	Master region, size. See PERI_MS_PPU_PR0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_PR8_MS_ATT0	0x40010230	Master attributes 0. See PERI_MS_PPU_PR0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_PR8_MS_ATT1	0x40010234	Master attributes 1. See PERI_MS_PPU_PR0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_PR8_MS_ATT2	0x40010238	Master attributes 2. See PERI_MS_PPU_PR0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_PR8_MS_ATT3	0x4001023C	Master attributes 3. See PERI_MS_PPU_PR0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_PR9_SL_ADDR	0x40010240	Slave region, base address. See PERI_MS_PPU_PR0_SL_ADDR for the details of bit fields.
PERI_MS_PPU_PR9_SL_SIZE	0x40010244	Slave region, size. See PERI_MS_PPU_PR0_SL_SIZE for the details of bit fields.
PERI_MS_PPU_PR9_SL_ATT0	0x40010250	Slave attributes 0. See PERI_MS_PPU_PR0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_PR9_SL_ATT1	0x40010254	Slave attributes 1. See PERI_MS_PPU_PR0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_PR9_SL_ATT2	0x40010258	Slave attributes 2. See PERI_MS_PPU_PR0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_PR9_SL_ATT3	0x4001025C	Slave attributes 3. See PERI_MS_PPU_PR0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_PR9_MS_ADDR	0x40010260	Master region, base address
PERI_MS_PPU_PR9_MS_SIZE	0x40010264	Master region, size. See PERI_MS_PPU_PR0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_PR9_MS_ATT0	0x40010270	Master attributes 0. See PERI_MS_PPU_PR0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_PR9_MS_ATT1	0x40010274	Master attributes 1. See PERI_MS_PPU_PR0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_PR9_MS_ATT2	0x40010278	Master attributes 2. See PERI_MS_PPU_PR0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_PR9_MS_ATT3	0x4001027C	Master attributes 3. See PERI_MS_PPU_PR0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_PR10_SL_ADDR	0x40010280	Slave region, base address. See PERI_MS_PPU_PR0_SL_ADDR for the details of bit fields.
PERI_MS_PPU_PR10_SL_SIZE	0x40010284	Slave region, size. See PERI_MS_PPU_PR0_SL_SIZE for the details of bit fields.
PERI_MS_PPU_PR10_SL_ATT0	0x40010290	Slave attributes 0. See PERI_MS_PPU_PR0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_PR10_SL_ATT1	0x40010294	Slave attributes 1. See PERI_MS_PPU_PR0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_PR10_SL_ATT2	0x40010298	Slave attributes 2. See PERI_MS_PPU_PR0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_PR10_SL_ATT3	0x4001029C	Slave attributes 3. See PERI_MS_PPU_PR0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_PR10_MS_ADDR	0x400102A0	Master region, base address
PERI_MS_PPU_PR10_MS_SIZE	0x400102A4	Master region, size. See PERI_MS_PPU_PR0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_PR10_MS_ATT0	0x400102B0	Master attributes 0. See PERI_MS_PPU_PR0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_PR10_MS_ATT1	0x400102B4	Master attributes 1. See PERI_MS_PPU_PR0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_PR10_MS_ATT2	0x400102B8	Master attributes 2. See PERI_MS_PPU_PR0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_PR10_MS_ATT3	0x400102BC	Master attributes 3. See PERI_MS_PPU_PR0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_PR11_SL_ADDR	0x400102C0	Slave region, base address. See PERI_MS_PPU_PR0_SL_ADDR for the details of bit fields.
PERI_MS_PPU_PR11_SL_SIZE	0x400102C4	Slave region, size. See PERI_MS_PPU_PR0_SL_SIZE for the details of bit fields.
PERI_MS_PPU_PR11_SL_ATT0	0x400102D0	Slave attributes 0. See PERI_MS_PPU_PR0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_PR11_SL_ATT1	0x400102D4	Slave attributes 1. See PERI_MS_PPU_PR0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_PR11_SL_ATT2	0x400102D8	Slave attributes 2. See PERI_MS_PPU_PR0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_PR11_SL_ATT3	0x400102DC	Slave attributes 3. See PERI_MS_PPU_PR0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_PR11_MS_ADDR	0x400102E0	Master region, base address
PERI_MS_PPU_PR11_MS_SIZE	0x400102E4	Master region, size. See PERI_MS_PPU_PR0_MS_SIZE for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_PR11_MS_ATT0	0x400102F0	Master attributes 0. See PERI_MS_PPU_PR0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_PR11_MS_ATT1	0x400102F4	Master attributes 1. See PERI_MS_PPU_PR0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_PR11_MS_ATT2	0x400102F8	Master attributes 2. See PERI_MS_PPU_PR0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_PR11_MS_ATT3	0x400102FC	Master attributes 3. See PERI_MS_PPU_PR0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_PR12_SL_ADDR	0x40010300	Slave region, base address. See PERI_MS_PPU_PR0_SL_ADDR for the details of bit fields.
PERI_MS_PPU_PR12_SL_SIZE	0x40010304	Slave region, size. See PERI_MS_PPU_PR0_SL_SIZE for the details of bit fields.
PERI_MS_PPU_PR12_SL_ATT0	0x40010310	Slave attributes 0. See PERI_MS_PPU_PR0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_PR12_SL_ATT1	0x40010314	Slave attributes 1. See PERI_MS_PPU_PR0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_PR12_SL_ATT2	0x40010318	Slave attributes 2. See PERI_MS_PPU_PR0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_PR12_SL_ATT3	0x4001031C	Slave attributes 3. See PERI_MS_PPU_PR0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_PR12_MS_ADDR	0x40010320	Master region, base address
PERI_MS_PPU_PR12_MS_SIZE	0x40010324	Master region, size. See PERI_MS_PPU_PR0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_PR12_MS_ATT0	0x40010330	Master attributes 0. See PERI_MS_PPU_PR0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_PR12_MS_ATT1	0x40010334	Master attributes 1. See PERI_MS_PPU_PR0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_PR12_MS_ATT2	0x40010338	Master attributes 2. See PERI_MS_PPU_PR0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_PR12_MS_ATT3	0x4001033C	Master attributes 3. See PERI_MS_PPU_PR0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_PR13_SL_ADDR	0x40010340	Slave region, base address. See PERI_MS_PPU_PR0_SL_ADDR for the details of bit fields.
PERI_MS_PPU_PR13_SL_SIZE	0x40010344	Slave region, size. See PERI_MS_PPU_PR0_SL_SIZE for the details of bit fields.
PERI_MS_PPU_PR13_SL_ATT0	0x40010350	Slave attributes 0. See PERI_MS_PPU_PR0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_PR13_SL_ATT1	0x40010354	Slave attributes 1. See PERI_MS_PPU_PR0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_PR13_SL_ATT2	0x40010358	Slave attributes 2. See PERI_MS_PPU_PR0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_PR13_SL_ATT3	0x4001035C	Slave attributes 3. See PERI_MS_PPU_PR0_SL_ATT3 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_PR13_MS_ADDR	0x40010360	Master region, base address
PERI_MS_PPU_PR13_MS_SIZE	0x40010364	Master region, size. See PERI_MS_PPU_PR0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_PR13_MS_ATT0	0x40010370	Master attributes 0. See PERI_MS_PPU_PR0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_PR13_MS_ATT1	0x40010374	Master attributes 1. See PERI_MS_PPU_PR0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_PR13_MS_ATT2	0x40010378	Master attributes 2. See PERI_MS_PPU_PR0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_PR13_MS_ATT3	0x4001037C	Master attributes 3. See PERI_MS_PPU_PR0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_PR14_SL_ADDR	0x40010380	Slave region, base address. See PERI_MS_PPU_PR0_SL_ADDR for the details of bit fields.
PERI_MS_PPU_PR14_SL_SIZE	0x40010384	Slave region, size. See PERI_MS_PPU_PR0_SL_SIZE for the details of bit fields.
PERI_MS_PPU_PR14_SL_ATT0	0x40010390	Slave attributes 0. See PERI_MS_PPU_PR0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_PR14_SL_ATT1	0x40010394	Slave attributes 1. See PERI_MS_PPU_PR0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_PR14_SL_ATT2	0x40010398	Slave attributes 2. See PERI_MS_PPU_PR0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_PR14_SL_ATT3	0x4001039C	Slave attributes 3. See PERI_MS_PPU_PR0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_PR14_MS_ADDR	0x400103A0	Master region, base address
PERI_MS_PPU_PR14_MS_SIZE	0x400103A4	Master region, size. See PERI_MS_PPU_PR0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_PR14_MS_ATT0	0x400103B0	Master attributes 0. See PERI_MS_PPU_PR0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_PR14_MS_ATT1	0x400103B4	Master attributes 1. See PERI_MS_PPU_PR0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_PR14_MS_ATT2	0x400103B8	Master attributes 2. See PERI_MS_PPU_PR0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_PR14_MS_ATT3	0x400103BC	Master attributes 3. See PERI_MS_PPU_PR0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_PR15_SL_ADDR	0x400103C0	Slave region, base address. See PERI_MS_PPU_PR0_SL_ADDR for the details of bit fields.
PERI_MS_PPU_PR15_SL_SIZE	0x400103C4	Slave region, size. See PERI_MS_PPU_PR0_SL_SIZE for the details of bit fields.
PERI_MS_PPU_PR15_SL_ATT0	0x400103D0	Slave attributes 0. See PERI_MS_PPU_PR0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_PR15_SL_ATT1	0x400103D4	Slave attributes 1. See PERI_MS_PPU_PR0_SL_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_PR15_SL_ATT2	0x400103D8	Slave attributes 2. See PERI_MS_PPU_PR0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_PR15_SL_ATT3	0x400103DC	Slave attributes 3. See PERI_MS_PPU_PR0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_PR15_MS_ADDR	0x400103E0	Master region, base address
PERI_MS_PPU_PR15_MS_SIZE	0x400103E4	Master region, size. See PERI_MS_PPU_PR0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_PR15_MS_ATT0	0x400103F0	Master attributes 0. See PERI_MS_PPU_PR0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_PR15_MS_ATT1	0x400103F4	Master attributes 1. See PERI_MS_PPU_PR0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_PR15_MS_ATT2	0x400103F8	Master attributes 2. See PERI_MS_PPU_PR0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_PR15_MS_ATT3	0x400103FC	Master attributes 3. See PERI_MS_PPU_PR0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX0_SL_ADDR	0x40010800	Slave region, base address
PERI_MS_PPU_FX0_SL_SIZE	0x40010804	Slave region, size
PERI_MS_PPU_FX0_SL_ATT0	0x40010810	Slave attributes 0
PERI_MS_PPU_FX0_SL_ATT1	0x40010814	Slave attributes 1
PERI_MS_PPU_FX0_SL_ATT2	0x40010818	Slave attributes 2
PERI_MS_PPU_FX0_SL_ATT3	0x4001081C	Slave attributes 3
PERI_MS_PPU_FX0_MS_ADDR	0x40010820	Master region, base address
PERI_MS_PPU_FX0_MS_SIZE	0x40010824	Master region, size
PERI_MS_PPU_FX0_MS_ATT0	0x40010830	Master attributes 0
PERI_MS_PPU_FX0_MS_ATT1	0x40010834	Master attributes 1
PERI_MS_PPU_FX0_MS_ATT2	0x40010838	Master attributes 2
PERI_MS_PPU_FX0_MS_ATT3	0x4001083C	Master attributes 3
PERI_MS_PPU_FX1_SL_ADDR	0x40010840	Slave region, base address
PERI_MS_PPU_FX1_SL_SIZE	0x40010844	Slave region, size
PERI_MS_PPU_FX1_SL_ATT0	0x40010850	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX1_SL_ATT1	0x40010854	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX1_SL_ATT2	0x40010858	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX1_SL_ATT3	0x4001085C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX1_MS_ADDR	0x40010860	Master region, base address
PERI_MS_PPU_FX1_MS_SIZE	0x40010864	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX1_MS_ATT0	0x40010870	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX1_MS_ATT1	0x40010874	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX1_MS_ATT2	0x40010878	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX1_MS_ATT3	0x4001087C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX2_SL_ADDR	0x40010880	Slave region, base address
PERI_MS_PPU_FX2_SL_SIZE	0x40010884	Slave region, size. See PERI_MS_PPU_FX1_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX2_SL_ATT0	0x40010890	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX2_SL_ATT1	0x40010894	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX2_SL_ATT2	0x40010898	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX2_SL_ATT3	0x4001089C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX2_MS_ADDR	0x400108A0	Master region, base address
PERI_MS_PPU_FX2_MS_SIZE	0x400108A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX2_MS_ATT0	0x400108B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX2_MS_ATT1	0x400108B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX2_MS_ATT2	0x400108B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX2_MS_ATT3	0x400108BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX3_SL_ADDR	0x400108C0	Slave region, base address
PERI_MS_PPU_FX3_SL_SIZE	0x400108C4	Slave region, size. See PERI_MS_PPU_FX1_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX3_SL_ATT0	0x400108D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX3_SL_ATT1	0x400108D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX3_SL_ATT2	0x400108D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX3_SL_ATT3	0x400108DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX3_MS_ADDR	0x400108E0	Master region, base address
PERI_MS_PPU_FX3_MS_SIZE	0x400108E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX3_MS_ATT0	0x400108F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX3_MS_ATT1	0x400108F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX3_MS_ATT2	0x400108F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX3_MS_ATT3	0x400108FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX4_SL_ADDR	0x40010900	Slave region, base address
PERI_MS_PPU_FX4_SL_SIZE	0x40010904	Slave region, size. See PERI_MS_PPU_FX1_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX4_SL_ATT0	0x40010910	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX4_SL_ATT1	0x40010914	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX4_SL_ATT2	0x40010918	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX4_SL_ATT3	0x4001091C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX4_MS_ADDR	0x40010920	Master region, base address
PERI_MS_PPU_FX4_MS_SIZE	0x40010924	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX4_MS_ATT0	0x40010930	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX4_MS_ATT1	0x40010934	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX4_MS_ATT2	0x40010938	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX4_MS_ATT3	0x4001093C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX5_SL_ADDR	0x40010940	Slave region, base address
PERI_MS_PPU_FX5_SL_SIZE	0x40010944	Slave region, size
PERI_MS_PPU_FX5_SL_ATT0	0x40010950	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX5_SL_ATT1	0x40010954	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX5_SL_ATT2	0x40010958	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX5_SL_ATT3	0x4001095C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX5_MS_ADDR	0x40010960	Master region, base address
PERI_MS_PPU_FX5_MS_SIZE	0x40010964	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX5_MS_ATT0	0x40010970	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX5_MS_ATT1	0x40010974	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX5_MS_ATT2	0x40010978	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX5_MS_ATT3	0x4001097C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX6_SL_ADDR	0x40010980	Slave region, base address
PERI_MS_PPU_FX6_SL_SIZE	0x40010984	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX6_SL_ATT0	0x40010990	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX6_SL_ATT1	0x40010994	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX6_SL_ATT2	0x40010998	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX6_SL_ATT3	0x4001099C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX6_MS_ADDR	0x400109A0	Master region, base address
PERI_MS_PPU_FX6_MS_SIZE	0x400109A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX6_MS_ATT0	0x400109B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX6_MS_ATT1	0x400109B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX6_MS_ATT2	0x400109B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX6_MS_ATT3	0x400109BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX7_SL_ADDR	0x400109C0	Slave region, base address
PERI_MS_PPU_FX7_SL_SIZE	0x400109C4	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX7_SL_ATT0	0x400109D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX7_SL_ATT1	0x400109D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX7_SL_ATT2	0x400109D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX7_SL_ATT3	0x400109DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX7_MS_ADDR	0x400109E0	Master region, base address
PERI_MS_PPU_FX7_MS_SIZE	0x400109E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX7_MS_ATT0	0x400109F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX7_MS_ATT1	0x400109F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX7_MS_ATT2	0x400109F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX7_MS_ATT3	0x400109FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX8_SL_ADDR	0x40010A00	Slave region, base address
PERI_MS_PPU_FX8_SL_SIZE	0x40010A04	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX8_SL_ATT0	0x40010A10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX8_SL_ATT1	0x40010A14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX8_SL_ATT2	0x40010A18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX8_SL_ATT3	0x40010A1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX8_MS_ADDR	0x40010A20	Master region, base address
PERI_MS_PPU_FX8_MS_SIZE	0x40010A24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX8_MS_ATT0	0x40010A30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX8_MS_ATT1	0x40010A34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX8_MS_ATT2	0x40010A38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX8_MS_ATT3	0x40010A3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX9_SL_ADDR	0x40010A40	Slave region, base address
PERI_MS_PPU_FX9_SL_SIZE	0x40010A44	Slave region, size
PERI_MS_PPU_FX9_SL_ATT0	0x40010A50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX9_SL_ATT1	0x40010A54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX9_SL_ATT2	0x40010A58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX9_SL_ATT3	0x40010A5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX9_MS_ADDR	0x40010A60	Master region, base address
PERI_MS_PPU_FX9_MS_SIZE	0x40010A64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX9_MS_ATT0	0x40010A70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX9_MS_ATT1	0x40010A74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX9_MS_ATT2	0x40010A78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX9_MS_ATT3	0x40010A7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX10_SL_ADDR	0x40010A80	Slave region, base address
PERI_MS_PPU_FX10_SL_SIZE	0x40010A84	Slave region, size
PERI_MS_PPU_FX10_SL_ATT0	0x40010A90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX10_SL_ATT1	0x40010A94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX10_SL_ATT2	0x40010A98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX10_SL_ATT3	0x40010A9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX10_MS_ADDR	0x40010AA0	Master region, base address
PERI_MS_PPU_FX10_MS_SIZE	0x40010AA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX10_MS_ATT0	0x40010AB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX10_MS_ATT1	0x40010AB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX10_MS_ATT2	0x40010AB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX10_MS_ATT3	0x40010ABC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX11_SL_ADDR	0x40010AC0	Slave region, base address
PERI_MS_PPU_FX11_SL_SIZE	0x40010AC4	Slave region, size
PERI_MS_PPU_FX11_SL_ATT0	0x40010AD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX11_SL_ATT1	0x40010AD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX11_SL_ATT2	0x40010AD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX11_SL_ATT3	0x40010ADC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX11_MS_ADDR	0x40010AE0	Master region, base address
PERI_MS_PPU_FX11_MS_SIZE	0x40010AE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX11_MS_ATT0	0x40010AF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX11_MS_ATT1	0x40010AF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX11_MS_ATT2	0x40010AF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX11_MS_ATT3	0x40010AFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX12_SL_ADDR	0x40010B00	Slave region, base address
PERI_MS_PPU_FX12_SL_SIZE	0x40010B04	Slave region, size
PERI_MS_PPU_FX12_SL_ATT0	0x40010B10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX12_SL_ATT1	0x40010B14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX12_SL_ATT2	0x40010B18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX12_SL_ATT3	0x40010B1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX12_MS_ADDR	0x40010B20	Master region, base address
PERI_MS_PPU_FX12_MS_SIZE	0x40010B24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX12_MS_ATT0	0x40010B30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX12_MS_ATT1	0x40010B34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX12_MS_ATT2	0x40010B38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX12_MS_ATT3	0x40010B3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX13_SL_ADDR	0x40010B40	Slave region, base address
PERI_MS_PPU_FX13_SL_SIZE	0x40010B44	Slave region, size. See PERI_MS_PPU_FX1_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX13_SL_ATT0	0x40010B50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX13_SL_ATT1	0x40010B54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX13_SL_ATT2	0x40010B58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX13_SL_ATT3	0x40010B5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX13_MS_ADDR	0x40010B60	Master region, base address
PERI_MS_PPU_FX13_MS_SIZE	0x40010B64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX13_MS_ATT0	0x40010B70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX13_MS_ATT1	0x40010B74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX13_MS_ATT2	0x40010B78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX13_MS_ATT3	0x40010B7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX14_SL_ADDR	0x40010B80	Slave region, base address
PERI_MS_PPU_FX14_SL_SIZE	0x40010B84	Slave region, size. See PERI_MS_PPU_FX1_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX14_SL_ATT0	0x40010B90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX14_SL_ATT1	0x40010B94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX14_SL_ATT2	0x40010B98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX14_SL_ATT3	0x40010B9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX14_MS_ADDR	0x40010BA0	Master region, base address
PERI_MS_PPU_FX14_MS_SIZE	0x40010BA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX14_MS_ATT0	0x40010BB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX14_MS_ATT1	0x40010BB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX14_MS_ATT2	0x40010BB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX14_MS_ATT3	0x40010BBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX15_SL_ADDR	0x40010BC0	Slave region, base address
PERI_MS_PPU_FX15_SL_SIZE	0x40010BC4	Slave region, size. See PERI_MS_PPU_FX0_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX15_SL_ATT0	0x40010BD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX15_SL_ATT1	0x40010BD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX15_SL_ATT2	0x40010BD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX15_SL_ATT3	0x40010BDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX15_MS_ADDR	0x40010BE0	Master region, base address
PERI_MS_PPU_FX15_MS_SIZE	0x40010BE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX15_MS_ATT0	0x40010BF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX15_MS_ATT1	0x40010BF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX15_MS_ATT2	0x40010BF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX15_MS_ATT3	0x40010BFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX16_SL_ADDR	0x40010C00	Slave region, base address
PERI_MS_PPU_FX16_SL_SIZE	0x40010C04	Slave region, size. See PERI_MS_PPU_FX10_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX16_SL_ATT0	0x40010C10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX16_SL_ATT1	0x40010C14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX16_SL_ATT2	0x40010C18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX16_SL_ATT3	0x40010C1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX16_MS_ADDR	0x40010C20	Master region, base address
PERI_MS_PPU_FX16_MS_SIZE	0x40010C24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX16_MS_ATT0	0x40010C30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX16_MS_ATT1	0x40010C34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX16_MS_ATT2	0x40010C38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX16_MS_ATT3	0x40010C3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX17_SL_ADDR	0x40010C40	Slave region, base address
PERI_MS_PPU_FX17_SL_SIZE	0x40010C44	Slave region, size
PERI_MS_PPU_FX17_SL_ATT0	0x40010C50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX17_SL_ATT1	0x40010C54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX17_SL_ATT2	0x40010C58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX17_SL_ATT3	0x40010C5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX17_MS_ADDR	0x40010C60	Master region, base address
PERI_MS_PPU_FX17_MS_SIZE	0x40010C64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX17_MS_ATT0	0x40010C70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX17_MS_ATT1	0x40010C74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX17_MS_ATT2	0x40010C78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX17_MS_ATT3	0x40010C7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX18_SL_ADDR	0x40010C80	Slave region, base address
PERI_MS_PPU_FX18_SL_SIZE	0x40010C84	Slave region, size
PERI_MS_PPU_FX18_SL_ATT0	0x40010C90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX18_SL_ATT1	0x40010C94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX18_SL_ATT2	0x40010C98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX18_SL_ATT3	0x40010C9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX18_MS_ADDR	0x40010CA0	Master region, base address
PERI_MS_PPU_FX18_MS_SIZE	0x40010CA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX18_MS_ATT0	0x40010CB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX18_MS_ATT1	0x40010CB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX18_MS_ATT2	0x40010CB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX18_MS_ATT3	0x40010CBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX19_SL_ADDR	0x40010CC0	Slave region, base address
PERI_MS_PPU_FX19_SL_SIZE	0x40010CC4	Slave region, size. See PERI_MS_PPU_FX11_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX19_SL_ATT0	0x40010CD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX19_SL_ATT1	0x40010CD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX19_SL_ATT2	0x40010CD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX19_SL_ATT3	0x40010CDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX19_MS_ADDR	0x40010CE0	Master region, base address
PERI_MS_PPU_FX19_MS_SIZE	0x40010CE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX19_MS_ATT0	0x40010CF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX19_MS_ATT1	0x40010CF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX19_MS_ATT2	0x40010CF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX19_MS_ATT3	0x40010CFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX20_SL_ADDR	0x40010D00	Slave region, base address
PERI_MS_PPU_FX20_SL_SIZE	0x40010D04	Slave region, size. See PERI_MS_PPU_FX11_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX20_SL_ATT0	0x40010D10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX20_SL_ATT1	0x40010D14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX20_SL_ATT2	0x40010D18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX20_SL_ATT3	0x40010D1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX20_MS_ADDR	0x40010D20	Master region, base address
PERI_MS_PPU_FX20_MS_SIZE	0x40010D24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX20_MS_ATT0	0x40010D30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX20_MS_ATT1	0x40010D34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX20_MS_ATT2	0x40010D38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX20_MS_ATT3	0x40010D3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX21_SL_ADDR	0x40010D40	Slave region, base address
PERI_MS_PPU_FX21_SL_SIZE	0x40010D44	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX21_SL_ATT0	0x40010D50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX21_SL_ATT1	0x40010D54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX21_SL_ATT2	0x40010D58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX21_SL_ATT3	0x40010D5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX21_MS_ADDR	0x40010D60	Master region, base address
PERI_MS_PPU_FX21_MS_SIZE	0x40010D64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX21_MS_ATT0	0x40010D70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX21_MS_ATT1	0x40010D74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX21_MS_ATT2	0x40010D78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX21_MS_ATT3	0x40010D7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX22_SL_ADDR	0x40010D80	Slave region, base address
PERI_MS_PPU_FX22_SL_SIZE	0x40010D84	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX22_SL_ATT0	0x40010D90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX22_SL_ATT1	0x40010D94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX22_SL_ATT2	0x40010D98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX22_SL_ATT3	0x40010D9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX22_MS_ADDR	0x40010DA0	Master region, base address
PERI_MS_PPU_FX22_MS_SIZE	0x40010DA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX22_MS_ATT0	0x40010DB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX22_MS_ATT1	0x40010DB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX22_MS_ATT2	0x40010DB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX22_MS_ATT3	0x40010DBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX23_SL_ADDR	0x40010DC0	Slave region, base address
PERI_MS_PPU_FX23_SL_SIZE	0x40010DC4	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX23_SL_ATT0	0x40010DD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX23_SL_ATT1	0x40010DD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX23_SL_ATT2	0x40010DD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX23_SL_ATT3	0x40010DDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX23_MS_ADDR	0x40010DE0	Master region, base address
PERI_MS_PPU_FX23_MS_SIZE	0x40010DE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX23_MS_ATT0	0x40010DF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX23_MS_ATT1	0x40010DF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX23_MS_ATT2	0x40010DF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX23_MS_ATT3	0x40010DFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX24_SL_ADDR	0x40010E00	Slave region, base address
PERI_MS_PPU_FX24_SL_SIZE	0x40010E04	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX24_SL_ATT0	0x40010E10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX24_SL_ATT1	0x40010E14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX24_SL_ATT2	0x40010E18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX24_SL_ATT3	0x40010E1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX24_MS_ADDR	0x40010E20	Master region, base address
PERI_MS_PPU_FX24_MS_SIZE	0x40010E24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX24_MS_ATT0	0x40010E30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX24_MS_ATT1	0x40010E34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX24_MS_ATT2	0x40010E38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX24_MS_ATT3	0x40010E3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX25_SL_ADDR	0x40010E40	Slave region, base address
PERI_MS_PPU_FX25_SL_SIZE	0x40010E44	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX25_SL_ATT0	0x40010E50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX25_SL_ATT1	0x40010E54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX25_SL_ATT2	0x40010E58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX25_SL_ATT3	0x40010E5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX25_MS_ADDR	0x40010E60	Master region, base address
PERI_MS_PPU_FX25_MS_SIZE	0x40010E64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX25_MS_ATT0	0x40010E70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX25_MS_ATT1	0x40010E74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX25_MS_ATT2	0x40010E78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX25_MS_ATT3	0x40010E7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX26_SL_ADDR	0x40010E80	Slave region, base address
PERI_MS_PPU_FX26_SL_SIZE	0x40010E84	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX26_SL_ATT0	0x40010E90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX26_SL_ATT1	0x40010E94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX26_SL_ATT2	0x40010E98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX26_SL_ATT3	0x40010E9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX26_MS_ADDR	0x40010EA0	Master region, base address
PERI_MS_PPU_FX26_MS_SIZE	0x40010EA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX26_MS_ATT0	0x40010EB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX26_MS_ATT1	0x40010EB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX26_MS_ATT2	0x40010EB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX26_MS_ATT3	0x40010EBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX27_SL_ADDR	0x40010EC0	Slave region, base address
PERI_MS_PPU_FX27_SL_SIZE	0x40010EC4	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX27_SL_ATT0	0x40010ED0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX27_SL_ATT1	0x40010ED4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX27_SL_ATT2	0x40010ED8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX27_SL_ATT3	0x40010EDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX27_MS_ADDR	0x40010EE0	Master region, base address
PERI_MS_PPU_FX27_MS_SIZE	0x40010EE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX27_MS_ATT0	0x40010EF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX27_MS_ATT1	0x40010EF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX27_MS_ATT2	0x40010EF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX27_MS_ATT3	0x40010EFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX28_SL_ADDR	0x40010F00	Slave region, base address
PERI_MS_PPU_FX28_SL_SIZE	0x40010F04	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX28_SL_ATT0	0x40010F10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX28_SL_ATT1	0x40010F14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX28_SL_ATT2	0x40010F18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX28_SL_ATT3	0x40010F1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX28_MS_ADDR	0x40010F20	Master region, base address
PERI_MS_PPU_FX28_MS_SIZE	0x40010F24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX28_MS_ATT0	0x40010F30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX28_MS_ATT1	0x40010F34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX28_MS_ATT2	0x40010F38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX28_MS_ATT3	0x40010F3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX29_SL_ADDR	0x40010F40	Slave region, base address
PERI_MS_PPU_FX29_SL_SIZE	0x40010F44	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX29_SL_ATT0	0x40010F50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX29_SL_ATT1	0x40010F54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX29_SL_ATT2	0x40010F58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX29_SL_ATT3	0x40010F5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX29_MS_ADDR	0x40010F60	Master region, base address
PERI_MS_PPU_FX29_MS_SIZE	0x40010F64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX29_MS_ATT0	0x40010F70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX29_MS_ATT1	0x40010F74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX29_MS_ATT2	0x40010F78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX29_MS_ATT3	0x40010F7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX30_SL_ADDR	0x40010F80	Slave region, base address
PERI_MS_PPU_FX30_SL_SIZE	0x40010F84	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX30_SL_ATT0	0x40010F90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX30_SL_ATT1	0x40010F94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX30_SL_ATT2	0x40010F98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX30_SL_ATT3	0x40010F9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX30_MS_ADDR	0x40010FA0	Master region, base address
PERI_MS_PPU_FX30_MS_SIZE	0x40010FA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX30_MS_ATT0	0x40010FB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX30_MS_ATT1	0x40010FB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX30_MS_ATT2	0x40010FB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX30_MS_ATT3	0x40010FBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX31_SL_ADDR	0x40010FC0	Slave region, base address
PERI_MS_PPU_FX31_SL_SIZE	0x40010FC4	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX31_SL_ATT0	0x40010FD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX31_SL_ATT1	0x40010FD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX31_SL_ATT2	0x40010FD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX31_SL_ATT3	0x40010FDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX31_MS_ADDR	0x40010FE0	Master region, base address
PERI_MS_PPU_FX31_MS_SIZE	0x40010FE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX31_MS_ATT0	0x40010FF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX31_MS_ATT1	0x40010FF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX31_MS_ATT2	0x40010FF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX31_MS_ATT3	0x40010FFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX32_SL_ADDR	0x40011000	Slave region, base address
PERI_MS_PPU_FX32_SL_SIZE	0x40011004	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX32_SL_ATT0	0x40011010	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX32_SL_ATT1	0x40011014	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX32_SL_ATT2	0x40011018	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX32_SL_ATT3	0x4001101C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX32_MS_ADDR	0x40011020	Master region, base address
PERI_MS_PPU_FX32_MS_SIZE	0x40011024	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX32_MS_ATT0	0x40011030	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX32_MS_ATT1	0x40011034	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX32_MS_ATT2	0x40011038	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX32_MS_ATT3	0x4001103C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX33_SL_ADDR	0x40011040	Slave region, base address
PERI_MS_PPU_FX33_SL_SIZE	0x40011044	Slave region, size
PERI_MS_PPU_FX33_SL_ATT0	0x40011050	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX33_SL_ATT1	0x40011054	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX33_SL_ATT2	0x40011058	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX33_SL_ATT3	0x4001105C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX33_MS_ADDR	0x40011060	Master region, base address
PERI_MS_PPU_FX33_MS_SIZE	0x40011064	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX33_MS_ATT0	0x40011070	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX33_MS_ATT1	0x40011074	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX33_MS_ATT2	0x40011078	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX33_MS_ATT3	0x4001107C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX34_SL_ADDR	0x40011080	Slave region, base address
PERI_MS_PPU_FX34_SL_SIZE	0x40011084	Slave region, size. See PERI_MS_PPU_FX33_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX34_SL_ATT0	0x40011090	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX34_SL_ATT1	0x40011094	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX34_SL_ATT2	0x40011098	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX34_SL_ATT3	0x4001109C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX34_MS_ADDR	0x400110A0	Master region, base address
PERI_MS_PPU_FX34_MS_SIZE	0x400110A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX34_MS_ATT0	0x400110B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX34_MS_ATT1	0x400110B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX34_MS_ATT2	0x400110B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX34_MS_ATT3	0x400110BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX35_SL_ADDR	0x400110C0	Slave region, base address
PERI_MS_PPU_FX35_SL_SIZE	0x400110C4	Slave region, size. See PERI_MS_PPU_FX33_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX35_SL_ATT0	0x400110D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX35_SL_ATT1	0x400110D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX35_SL_ATT2	0x400110D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX35_SL_ATT3	0x400110DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX35_MS_ADDR	0x400110E0	Master region, base address
PERI_MS_PPU_FX35_MS_SIZE	0x400110E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX35_MS_ATT0	0x400110F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX35_MS_ATT1	0x400110F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX35_MS_ATT2	0x400110F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX35_MS_ATT3	0x400110FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX36_SL_ADDR	0x40011100	Slave region, base address
PERI_MS_PPU_FX36_SL_SIZE	0x40011104	Slave region, size. See PERI_MS_PPU_FX33_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX36_SL_ATT0	0x40011110	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX36_SL_ATT1	0x40011114	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX36_SL_ATT2	0x40011118	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX36_SL_ATT3	0x4001111C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX36_MS_ADDR	0x40011120	Master region, base address
PERI_MS_PPU_FX36_MS_SIZE	0x40011124	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX36_MS_ATT0	0x40011130	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX36_MS_ATT1	0x40011134	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX36_MS_ATT2	0x40011138	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX36_MS_ATT3	0x4001113C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX37_SL_ADDR	0x40011140	Slave region, base address
PERI_MS_PPU_FX37_SL_SIZE	0x40011144	Slave region, size. See PERI_MS_PPU_FX33_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX37_SL_ATT0	0x40011150	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX37_SL_ATT1	0x40011154	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX37_SL_ATT2	0x40011158	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX37_SL_ATT3	0x4001115C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX37_MS_ADDR	0x40011160	Master region, base address
PERI_MS_PPU_FX37_MS_SIZE	0x40011164	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX37_MS_ATT0	0x40011170	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX37_MS_ATT1	0x40011174	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX37_MS_ATT2	0x40011178	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX37_MS_ATT3	0x4001117C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX38_SL_ADDR	0x40011180	Slave region, base address
PERI_MS_PPU_FX38_SL_SIZE	0x40011184	Slave region, size. See PERI_MS_PPU_FX33_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX38_SL_ATT0	0x40011190	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX38_SL_ATT1	0x40011194	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX38_SL_ATT2	0x40011198	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX38_SL_ATT3	0x4001119C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX38_MS_ADDR	0x400111A0	Master region, base address
PERI_MS_PPU_FX38_MS_SIZE	0x400111A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX38_MS_ATT0	0x400111B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX38_MS_ATT1	0x400111B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX38_MS_ATT2	0x400111B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX38_MS_ATT3	0x400111BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX39_SL_ADDR	0x400111C0	Slave region, base address
PERI_MS_PPU_FX39_SL_SIZE	0x400111C4	Slave region, size. See PERI_MS_PPU_FX33_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX39_SL_ATT0	0x400111D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX39_SL_ATT1	0x400111D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX39_SL_ATT2	0x400111D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX39_SL_ATT3	0x400111DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX39_MS_ADDR	0x400111E0	Master region, base address
PERI_MS_PPU_FX39_MS_SIZE	0x400111E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX39_MS_ATT0	0x400111F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX39_MS_ATT1	0x400111F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX39_MS_ATT2	0x400111F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX39_MS_ATT3	0x400111FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX40_SL_ADDR	0x40011200	Slave region, base address
PERI_MS_PPU_FX40_SL_SIZE	0x40011204	Slave region, size. See PERI_MS_PPU_FX33_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX40_SL_ATT0	0x40011210	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX40_SL_ATT1	0x40011214	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX40_SL_ATT2	0x40011218	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX40_SL_ATT3	0x4001121C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX40_MS_ADDR	0x40011220	Master region, base address
PERI_MS_PPU_FX40_MS_SIZE	0x40011224	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX40_MS_ATT0	0x40011230	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX40_MS_ATT1	0x40011234	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX40_MS_ATT2	0x40011238	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX40_MS_ATT3	0x4001123C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX41_SL_ADDR	0x40011240	Slave region, base address
PERI_MS_PPU_FX41_SL_SIZE	0x40011244	Slave region, size
PERI_MS_PPU_FX41_SL_ATT0	0x40011250	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX41_SL_ATT1	0x40011254	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX41_SL_ATT2	0x40011258	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX41_SL_ATT3	0x4001125C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX41_MS_ADDR	0x40011260	Master region, base address
PERI_MS_PPU_FX41_MS_SIZE	0x40011264	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX41_MS_ATT0	0x40011270	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX41_MS_ATT1	0x40011274	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX41_MS_ATT2	0x40011278	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX41_MS_ATT3	0x4001127C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX42_SL_ADDR	0x40011280	Slave region, base address
PERI_MS_PPU_FX42_SL_SIZE	0x40011284	Slave region, size. See PERI_MS_PPU_FX1_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX42_SL_ATT0	0x40011290	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX42_SL_ATT1	0x40011294	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX42_SL_ATT2	0x40011298	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX42_SL_ATT3	0x4001129C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX42_MS_ADDR	0x400112A0	Master region, base address
PERI_MS_PPU_FX42_MS_SIZE	0x400112A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX42_MS_ATT0	0x400112B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX42_MS_ATT1	0x400112B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX42_MS_ATT2	0x400112B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX42_MS_ATT3	0x400112BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX43_SL_ADDR	0x400112C0	Slave region, base address
PERI_MS_PPU_FX43_SL_SIZE	0x400112C4	Slave region, size. See PERI_MS_PPU_FX1_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX43_SL_ATT0	0x400112D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX43_SL_ATT1	0x400112D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX43_SL_ATT2	0x400112D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX43_SL_ATT3	0x400112DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX43_MS_ADDR	0x400112E0	Master region, base address
PERI_MS_PPU_FX43_MS_SIZE	0x400112E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX43_MS_ATT0	0x400112F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX43_MS_ATT1	0x400112F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX43_MS_ATT2	0x400112F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX43_MS_ATT3	0x400112FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX44_SL_ADDR	0x40011300	Slave region, base address
PERI_MS_PPU_FX44_SL_SIZE	0x40011304	Slave region, size. See PERI_MS_PPU_FX10_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX44_SL_ATT0	0x40011310	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX44_SL_ATT1	0x40011314	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX44_SL_ATT2	0x40011318	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX44_SL_ATT3	0x4001131C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX44_MS_ADDR	0x40011320	Master region, base address
PERI_MS_PPU_FX44_MS_SIZE	0x40011324	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX44_MS_ATT0	0x40011330	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX44_MS_ATT1	0x40011334	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX44_MS_ATT2	0x40011338	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX44_MS_ATT3	0x4001133C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX45_SL_ADDR	0x40011340	Slave region, base address
PERI_MS_PPU_FX45_SL_SIZE	0x40011344	Slave region, size
PERI_MS_PPU_FX45_SL_ATT0	0x40011350	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX45_SL_ATT1	0x40011354	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX45_SL_ATT2	0x40011358	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX45_SL_ATT3	0x4001135C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX45_MS_ADDR	0x40011360	Master region, base address
PERI_MS_PPU_FX45_MS_SIZE	0x40011364	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX45_MS_ATT0	0x40011370	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX45_MS_ATT1	0x40011374	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX45_MS_ATT2	0x40011378	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX45_MS_ATT3	0x4001137C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX46_SL_ADDR	0x40011380	Slave region, base address
PERI_MS_PPU_FX46_SL_SIZE	0x40011384	Slave region, size. See PERI_MS_PPU_FX1_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX46_SL_ATT0	0x40011390	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX46_SL_ATT1	0x40011394	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX46_SL_ATT2	0x40011398	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX46_SL_ATT3	0x4001139C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX46_MS_ADDR	0x400113A0	Master region, base address
PERI_MS_PPU_FX46_MS_SIZE	0x400113A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX46_MS_ATT0	0x400113B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX46_MS_ATT1	0x400113B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX46_MS_ATT2	0x400113B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX46_MS_ATT3	0x400113BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX47_SL_ADDR	0x400113C0	Slave region, base address
PERI_MS_PPU_FX47_SL_SIZE	0x400113C4	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX47_SL_ATT0	0x400113D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX47_SL_ATT1	0x400113D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX47_SL_ATT2	0x400113D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX47_SL_ATT3	0x400113DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX47_MS_ADDR	0x400113E0	Master region, base address
PERI_MS_PPU_FX47_MS_SIZE	0x400113E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX47_MS_ATT0	0x400113F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX47_MS_ATT1	0x400113F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX47_MS_ATT2	0x400113F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX47_MS_ATT3	0x400113FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX48_SL_ADDR	0x40011400	Slave region, base address
PERI_MS_PPU_FX48_SL_SIZE	0x40011404	Slave region, size
PERI_MS_PPU_FX48_SL_ATT0	0x40011410	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX48_SL_ATT1	0x40011414	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX48_SL_ATT2	0x40011418	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX48_SL_ATT3	0x4001141C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX48_MS_ADDR	0x40011420	Master region, base address
PERI_MS_PPU_FX48_MS_SIZE	0x40011424	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX48_MS_ATT0	0x40011430	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX48_MS_ATT1	0x40011434	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX48_MS_ATT2	0x40011438	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX48_MS_ATT3	0x4001143C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX49_SL_ADDR	0x40011440	Slave region, base address
PERI_MS_PPU_FX49_SL_SIZE	0x40011444	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX49_SL_ATT0	0x40011450	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX49_SL_ATT1	0x40011454	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX49_SL_ATT2	0x40011458	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX49_SL_ATT3	0x4001145C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX49_MS_ADDR	0x40011460	Master region, base address
PERI_MS_PPU_FX49_MS_SIZE	0x40011464	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX49_MS_ATT0	0x40011470	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX49_MS_ATT1	0x40011474	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX49_MS_ATT2	0x40011478	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX49_MS_ATT3	0x4001147C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX50_SL_ADDR	0x40011480	Slave region, base address
PERI_MS_PPU_FX50_SL_SIZE	0x40011484	Slave region, size. See PERI_MS_PPU_FX1_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX50_SL_ATT0	0x40011490	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX50_SL_ATT1	0x40011494	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX50_SL_ATT2	0x40011498	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX50_SL_ATT3	0x4001149C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX50_MS_ADDR	0x400114A0	Master region, base address
PERI_MS_PPU_FX50_MS_SIZE	0x400114A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX50_MS_ATT0	0x400114B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX50_MS_ATT1	0x400114B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX50_MS_ATT2	0x400114B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX50_MS_ATT3	0x400114BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX51_SL_ADDR	0x400114C0	Slave region, base address
PERI_MS_PPU_FX51_SL_SIZE	0x400114C4	Slave region, size. See PERI_MS_PPU_FX1_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX51_SL_ATT0	0x400114D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX51_SL_ATT1	0x400114D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX51_SL_ATT2	0x400114D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX51_SL_ATT3	0x400114DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX51_MS_ADDR	0x400114E0	Master region, base address
PERI_MS_PPU_FX51_MS_SIZE	0x400114E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX51_MS_ATT0	0x400114F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX51_MS_ATT1	0x400114F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX51_MS_ATT2	0x400114F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX51_MS_ATT3	0x400114FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX52_SL_ADDR	0x40011500	Slave region, base address
PERI_MS_PPU_FX52_SL_SIZE	0x40011504	Slave region, size. See PERI_MS_PPU_FX1_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX52_SL_ATT0	0x40011510	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX52_SL_ATT1	0x40011514	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX52_SL_ATT2	0x40011518	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX52_SL_ATT3	0x4001151C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX52_MS_ADDR	0x40011520	Master region, base address
PERI_MS_PPU_FX52_MS_SIZE	0x40011524	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX52_MS_ATT0	0x40011530	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX52_MS_ATT1	0x40011534	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX52_MS_ATT2	0x40011538	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX52_MS_ATT3	0x4001153C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX53_SL_ADDR	0x40011540	Slave region, base address
PERI_MS_PPU_FX53_SL_SIZE	0x40011544	Slave region, size. See PERI_MS_PPU_FX1_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX53_SL_ATT0	0x40011550	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX53_SL_ATT1	0x40011554	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX53_SL_ATT2	0x40011558	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX53_SL_ATT3	0x4001155C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX53_MS_ADDR	0x40011560	Master region, base address
PERI_MS_PPU_FX53_MS_SIZE	0x40011564	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX53_MS_ATT0	0x40011570	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX53_MS_ATT1	0x40011574	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX53_MS_ATT2	0x40011578	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX53_MS_ATT3	0x4001157C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX54_SL_ADDR	0x40011580	Slave region, base address
PERI_MS_PPU_FX54_SL_SIZE	0x40011584	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX54_SL_ATT0	0x40011590	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX54_SL_ATT1	0x40011594	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX54_SL_ATT2	0x40011598	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX54_SL_ATT3	0x4001159C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX54_MS_ADDR	0x400115A0	Master region, base address
PERI_MS_PPU_FX54_MS_SIZE	0x400115A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX54_MS_ATT0	0x400115B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX54_MS_ATT1	0x400115B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX54_MS_ATT2	0x400115B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX54_MS_ATT3	0x400115BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX55_SL_ADDR	0x400115C0	Slave region, base address
PERI_MS_PPU_FX55_SL_SIZE	0x400115C4	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX55_SL_ATT0	0x400115D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX55_SL_ATT1	0x400115D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX55_SL_ATT2	0x400115D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX55_SL_ATT3	0x400115DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX55_MS_ADDR	0x400115E0	Master region, base address
PERI_MS_PPU_FX55_MS_SIZE	0x400115E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX55_MS_ATT0	0x400115F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX55_MS_ATT1	0x400115F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX55_MS_ATT2	0x400115F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX55_MS_ATT3	0x400115FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX56_SL_ADDR	0x40011600	Slave region, base address
PERI_MS_PPU_FX56_SL_SIZE	0x40011604	Slave region, size. See PERI_MS_PPU_FX1_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX56_SL_ATT0	0x40011610	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX56_SL_ATT1	0x40011614	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX56_SL_ATT2	0x40011618	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX56_SL_ATT3	0x4001161C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX56_MS_ADDR	0x40011620	Master region, base address
PERI_MS_PPU_FX56_MS_SIZE	0x40011624	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX56_MS_ATT0	0x40011630	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX56_MS_ATT1	0x40011634	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX56_MS_ATT2	0x40011638	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX56_MS_ATT3	0x4001163C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX57_SL_ADDR	0x40011640	Slave region, base address
PERI_MS_PPU_FX57_SL_SIZE	0x40011644	Slave region, size. See PERI_MS_PPU_FX10_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX57_SL_ATT0	0x40011650	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX57_SL_ATT1	0x40011654	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX57_SL_ATT2	0x40011658	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX57_SL_ATT3	0x4001165C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX57_MS_ADDR	0x40011660	Master region, base address
PERI_MS_PPU_FX57_MS_SIZE	0x40011664	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX57_MS_ATT0	0x40011670	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX57_MS_ATT1	0x40011674	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX57_MS_ATT2	0x40011678	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX57_MS_ATT3	0x4001167C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX58_SL_ADDR	0x40011680	Slave region, base address
PERI_MS_PPU_FX58_SL_SIZE	0x40011684	Slave region, size. See PERI_MS_PPU_FX17_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX58_SL_ATT0	0x40011690	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX58_SL_ATT1	0x40011694	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX58_SL_ATT2	0x40011698	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX58_SL_ATT3	0x4001169C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX58_MS_ADDR	0x400116A0	Master region, base address
PERI_MS_PPU_FX58_MS_SIZE	0x400116A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX58_MS_ATT0	0x400116B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX58_MS_ATT1	0x400116B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX58_MS_ATT2	0x400116B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX58_MS_ATT3	0x400116BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX59_SL_ADDR	0x400116C0	Slave region, base address
PERI_MS_PPU_FX59_SL_SIZE	0x400116C4	Slave region, size. See PERI_MS_PPU_FX0_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX59_SL_ATT0	0x400116D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX59_SL_ATT1	0x400116D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX59_SL_ATT2	0x400116D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX59_SL_ATT3	0x400116DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX59_MS_ADDR	0x400116E0	Master region, base address
PERI_MS_PPU_FX59_MS_SIZE	0x400116E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX59_MS_ATT0	0x400116F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX59_MS_ATT1	0x400116F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX59_MS_ATT2	0x400116F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX59_MS_ATT3	0x400116FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX60_SL_ADDR	0x40011700	Slave region, base address
PERI_MS_PPU_FX60_SL_SIZE	0x40011704	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX60_SL_ATT0	0x40011710	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX60_SL_ATT1	0x40011714	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX60_SL_ATT2	0x40011718	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX60_SL_ATT3	0x4001171C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX60_MS_ADDR	0x40011720	Master region, base address
PERI_MS_PPU_FX60_MS_SIZE	0x40011724	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX60_MS_ATT0	0x40011730	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX60_MS_ATT1	0x40011734	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX60_MS_ATT2	0x40011738	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX60_MS_ATT3	0x4001173C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX61_SL_ADDR	0x40011740	Slave region, base address
PERI_MS_PPU_FX61_SL_SIZE	0x40011744	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX61_SL_ATT0	0x40011750	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX61_SL_ATT1	0x40011754	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX61_SL_ATT2	0x40011758	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX61_SL_ATT3	0x4001175C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX61_MS_ADDR	0x40011760	Master region, base address
PERI_MS_PPU_FX61_MS_SIZE	0x40011764	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX61_MS_ATT0	0x40011770	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX61_MS_ATT1	0x40011774	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX61_MS_ATT2	0x40011778	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX61_MS_ATT3	0x4001177C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX62_SL_ADDR	0x40011780	Slave region, base address
PERI_MS_PPU_FX62_SL_SIZE	0x40011784	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX62_SL_ATT0	0x40011790	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX62_SL_ATT1	0x40011794	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX62_SL_ATT2	0x40011798	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX62_SL_ATT3	0x4001179C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX62_MS_ADDR	0x400117A0	Master region, base address
PERI_MS_PPU_FX62_MS_SIZE	0x400117A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX62_MS_ATT0	0x400117B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX62_MS_ATT1	0x400117B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX62_MS_ATT2	0x400117B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX62_MS_ATT3	0x400117BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX63_SL_ADDR	0x400117C0	Slave region, base address
PERI_MS_PPU_FX63_SL_SIZE	0x400117C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX63_SL_ATT0	0x400117D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX63_SL_ATT1	0x400117D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX63_SL_ATT2	0x400117D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX63_SL_ATT3	0x400117DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX63_MS_ADDR	0x400117E0	Master region, base address
PERI_MS_PPU_FX63_MS_SIZE	0x400117E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX63_MS_ATT0	0x400117F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX63_MS_ATT1	0x400117F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX63_MS_ATT2	0x400117F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX63_MS_ATT3	0x400117FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX64_SL_ADDR	0x40011800	Slave region, base address
PERI_MS_PPU_FX64_SL_SIZE	0x40011804	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX64_SL_ATT0	0x40011810	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX64_SL_ATT1	0x40011814	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX64_SL_ATT2	0x40011818	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX64_SL_ATT3	0x4001181C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX64_MS_ADDR	0x40011820	Master region, base address
PERI_MS_PPU_FX64_MS_SIZE	0x40011824	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX64_MS_ATT0	0x40011830	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX64_MS_ATT1	0x40011834	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX64_MS_ATT2	0x40011838	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX64_MS_ATT3	0x4001183C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX65_SL_ADDR	0x40011840	Slave region, base address
PERI_MS_PPU_FX65_SL_SIZE	0x40011844	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX65_SL_ATT0	0x40011850	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX65_SL_ATT1	0x40011854	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX65_SL_ATT2	0x40011858	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX65_SL_ATT3	0x4001185C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX65_MS_ADDR	0x40011860	Master region, base address
PERI_MS_PPU_FX65_MS_SIZE	0x40011864	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX65_MS_ATT0	0x40011870	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX65_MS_ATT1	0x40011874	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX65_MS_ATT2	0x40011878	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX65_MS_ATT3	0x4001187C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX66_SL_ADDR	0x40011880	Slave region, base address
PERI_MS_PPU_FX66_SL_SIZE	0x40011884	Slave region, size
PERI_MS_PPU_FX66_SL_ATT0	0x40011890	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX66_SL_ATT1	0x40011894	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX66_SL_ATT2	0x40011898	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX66_SL_ATT3	0x4001189C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX66_MS_ADDR	0x400118A0	Master region, base address
PERI_MS_PPU_FX66_MS_SIZE	0x400118A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX66_MS_ATT0	0x400118B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX66_MS_ATT1	0x400118B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX66_MS_ATT2	0x400118B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX66_MS_ATT3	0x400118BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX67_SL_ADDR	0x400118C0	Slave region, base address
PERI_MS_PPU_FX67_SL_SIZE	0x400118C4	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX67_SL_ATT0	0x400118D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX67_SL_ATT1	0x400118D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX67_SL_ATT2	0x400118D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX67_SL_ATT3	0x400118DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX67_MS_ADDR	0x400118E0	Master region, base address
PERI_MS_PPU_FX67_MS_SIZE	0x400118E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX67_MS_ATT0	0x400118F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX67_MS_ATT1	0x400118F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX67_MS_ATT2	0x400118F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX67_MS_ATT3	0x400118FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX68_SL_ADDR	0x40011900	Slave region, base address
PERI_MS_PPU_FX68_SL_SIZE	0x40011904	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX68_SL_ATT0	0x40011910	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX68_SL_ATT1	0x40011914	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX68_SL_ATT2	0x40011918	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX68_SL_ATT3	0x4001191C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX68_MS_ADDR	0x40011920	Master region, base address
PERI_MS_PPU_FX68_MS_SIZE	0x40011924	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX68_MS_ATT0	0x40011930	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX68_MS_ATT1	0x40011934	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX68_MS_ATT2	0x40011938	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX68_MS_ATT3	0x4001193C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX69_SL_ADDR	0x40011940	Slave region, base address
PERI_MS_PPU_FX69_SL_SIZE	0x40011944	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX69_SL_ATT0	0x40011950	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX69_SL_ATT1	0x40011954	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX69_SL_ATT2	0x40011958	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX69_SL_ATT3	0x4001195C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX69_MS_ADDR	0x40011960	Master region, base address
PERI_MS_PPU_FX69_MS_SIZE	0x40011964	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX69_MS_ATT0	0x40011970	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX69_MS_ATT1	0x40011974	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX69_MS_ATT2	0x40011978	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX69_MS_ATT3	0x4001197C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX70_SL_ADDR	0x40011980	Slave region, base address
PERI_MS_PPU_FX70_SL_SIZE	0x40011984	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX70_SL_ATT0	0x40011990	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX70_SL_ATT1	0x40011994	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX70_SL_ATT2	0x40011998	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX70_SL_ATT3	0x4001199C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX70_MS_ADDR	0x400119A0	Master region, base address
PERI_MS_PPU_FX70_MS_SIZE	0x400119A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX70_MS_ATT0	0x400119B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX70_MS_ATT1	0x400119B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX70_MS_ATT2	0x400119B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX70_MS_ATT3	0x400119BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX71_SL_ADDR	0x400119C0	Slave region, base address
PERI_MS_PPU_FX71_SL_SIZE	0x400119C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX71_SL_ATT0	0x400119D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX71_SL_ATT1	0x400119D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX71_SL_ATT2	0x400119D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX71_SL_ATT3	0x400119DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX71_MS_ADDR	0x400119E0	Master region, base address
PERI_MS_PPU_FX71_MS_SIZE	0x400119E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX71_MS_ATT0	0x400119F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX71_MS_ATT1	0x400119F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX71_MS_ATT2	0x400119F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX71_MS_ATT3	0x400119FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX72_SL_ADDR	0x40011A00	Slave region, base address
PERI_MS_PPU_FX72_SL_SIZE	0x40011A04	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX72_SL_ATT0	0x40011A10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX72_SL_ATT1	0x40011A14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX72_SL_ATT2	0x40011A18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX72_SL_ATT3	0x40011A1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX72_MS_ADDR	0x40011A20	Master region, base address
PERI_MS_PPU_FX72_MS_SIZE	0x40011A24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX72_MS_ATT0	0x40011A30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX72_MS_ATT1	0x40011A34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX72_MS_ATT2	0x40011A38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX72_MS_ATT3	0x40011A3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX73_SL_ADDR	0x40011A40	Slave region, base address
PERI_MS_PPU_FX73_SL_SIZE	0x40011A44	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX73_SL_ATT0	0x40011A50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX73_SL_ATT1	0x40011A54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX73_SL_ATT2	0x40011A58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX73_SL_ATT3	0x40011A5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX73_MS_ADDR	0x40011A60	Master region, base address
PERI_MS_PPU_FX73_MS_SIZE	0x40011A64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX73_MS_ATT0	0x40011A70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX73_MS_ATT1	0x40011A74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX73_MS_ATT2	0x40011A78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX73_MS_ATT3	0x40011A7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX74_SL_ADDR	0x40011A80	Slave region, base address
PERI_MS_PPU_FX74_SL_SIZE	0x40011A84	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX74_SL_ATT0	0x40011A90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX74_SL_ATT1	0x40011A94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX74_SL_ATT2	0x40011A98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX74_SL_ATT3	0x40011A9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX74_MS_ADDR	0x40011AA0	Master region, base address
PERI_MS_PPU_FX74_MS_SIZE	0x40011AA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX74_MS_ATT0	0x40011AB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX74_MS_ATT1	0x40011AB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX74_MS_ATT2	0x40011AB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX74_MS_ATT3	0x40011ABC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX75_SL_ADDR	0x40011AC0	Slave region, base address
PERI_MS_PPU_FX75_SL_SIZE	0x40011AC4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX75_SL_ATT0	0x40011AD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX75_SL_ATT1	0x40011AD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX75_SL_ATT2	0x40011AD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX75_SL_ATT3	0x40011ADC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX75_MS_ADDR	0x40011AE0	Master region, base address
PERI_MS_PPU_FX75_MS_SIZE	0x40011AE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX75_MS_ATT0	0x40011AF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX75_MS_ATT1	0x40011AF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX75_MS_ATT2	0x40011AF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX75_MS_ATT3	0x40011AFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX76_SL_ADDR	0x40011B00	Slave region, base address
PERI_MS_PPU_FX76_SL_SIZE	0x40011B04	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX76_SL_ATT0	0x40011B10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX76_SL_ATT1	0x40011B14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX76_SL_ATT2	0x40011B18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX76_SL_ATT3	0x40011B1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX76_MS_ADDR	0x40011B20	Master region, base address
PERI_MS_PPU_FX76_MS_SIZE	0x40011B24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX76_MS_ATT0	0x40011B30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX76_MS_ATT1	0x40011B34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX76_MS_ATT2	0x40011B38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX76_MS_ATT3	0x40011B3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX77_SL_ADDR	0x40011B40	Slave region, base address
PERI_MS_PPU_FX77_SL_SIZE	0x40011B44	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX77_SL_ATT0	0x40011B50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX77_SL_ATT1	0x40011B54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX77_SL_ATT2	0x40011B58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX77_SL_ATT3	0x40011B5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX77_MS_ADDR	0x40011B60	Master region, base address
PERI_MS_PPU_FX77_MS_SIZE	0x40011B64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX77_MS_ATT0	0x40011B70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX77_MS_ATT1	0x40011B74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX77_MS_ATT2	0x40011B78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX77_MS_ATT3	0x40011B7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX78_SL_ADDR	0x40011B80	Slave region, base address
PERI_MS_PPU_FX78_SL_SIZE	0x40011B84	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX78_SL_ATT0	0x40011B90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX78_SL_ATT1	0x40011B94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX78_SL_ATT2	0x40011B98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX78_SL_ATT3	0x40011B9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX78_MS_ADDR	0x40011BA0	Master region, base address
PERI_MS_PPU_FX78_MS_SIZE	0x40011BA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX78_MS_ATT0	0x40011BB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX78_MS_ATT1	0x40011BB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX78_MS_ATT2	0x40011BB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX78_MS_ATT3	0x40011BBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX79_SL_ADDR	0x40011BC0	Slave region, base address
PERI_MS_PPU_FX79_SL_SIZE	0x40011BC4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX79_SL_ATT0	0x40011BD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX79_SL_ATT1	0x40011BD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX79_SL_ATT2	0x40011BD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX79_SL_ATT3	0x40011BDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX79_MS_ADDR	0x40011BE0	Master region, base address
PERI_MS_PPU_FX79_MS_SIZE	0x40011BE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX79_MS_ATT0	0x40011BF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX79_MS_ATT1	0x40011BF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX79_MS_ATT2	0x40011BF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX79_MS_ATT3	0x40011BFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX80_SL_ADDR	0x40011C00	Slave region, base address
PERI_MS_PPU_FX80_SL_SIZE	0x40011C04	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX80_SL_ATT0	0x40011C10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX80_SL_ATT1	0x40011C14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX80_SL_ATT2	0x40011C18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX80_SL_ATT3	0x40011C1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX80_MS_ADDR	0x40011C20	Master region, base address
PERI_MS_PPU_FX80_MS_SIZE	0x40011C24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX80_MS_ATT0	0x40011C30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX80_MS_ATT1	0x40011C34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX80_MS_ATT2	0x40011C38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX80_MS_ATT3	0x40011C3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX81_SL_ADDR	0x40011C40	Slave region, base address
PERI_MS_PPU_FX81_SL_SIZE	0x40011C44	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX81_SL_ATT0	0x40011C50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX81_SL_ATT1	0x40011C54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX81_SL_ATT2	0x40011C58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX81_SL_ATT3	0x40011C5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX81_MS_ADDR	0x40011C60	Master region, base address
PERI_MS_PPU_FX81_MS_SIZE	0x40011C64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX81_MS_ATT0	0x40011C70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX81_MS_ATT1	0x40011C74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX81_MS_ATT2	0x40011C78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX81_MS_ATT3	0x40011C7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX82_SL_ADDR	0x40011C80	Slave region, base address
PERI_MS_PPU_FX82_SL_SIZE	0x40011C84	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX82_SL_ATT0	0x40011C90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX82_SL_ATT1	0x40011C94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX82_SL_ATT2	0x40011C98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX82_SL_ATT3	0x40011C9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX82_MS_ADDR	0x40011CA0	Master region, base address
PERI_MS_PPU_FX82_MS_SIZE	0x40011CA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX82_MS_ATT0	0x40011CB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX82_MS_ATT1	0x40011CB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX82_MS_ATT2	0x40011CB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX82_MS_ATT3	0x40011CBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX83_SL_ADDR	0x40011CC0	Slave region, base address
PERI_MS_PPU_FX83_SL_SIZE	0x40011CC4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX83_SL_ATT0	0x40011CD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX83_SL_ATT1	0x40011CD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX83_SL_ATT2	0x40011CD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX83_SL_ATT3	0x40011CDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX83_MS_ADDR	0x40011CE0	Master region, base address
PERI_MS_PPU_FX83_MS_SIZE	0x40011CE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX83_MS_ATT0	0x40011CF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX83_MS_ATT1	0x40011CF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX83_MS_ATT2	0x40011CF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX83_MS_ATT3	0x40011CFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX84_SL_ADDR	0x40011D00	Slave region, base address
PERI_MS_PPU_FX84_SL_SIZE	0x40011D04	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX84_SL_ATT0	0x40011D10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX84_SL_ATT1	0x40011D14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX84_SL_ATT2	0x40011D18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX84_SL_ATT3	0x40011D1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX84_MS_ADDR	0x40011D20	Master region, base address
PERI_MS_PPU_FX84_MS_SIZE	0x40011D24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX84_MS_ATT0	0x40011D30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX84_MS_ATT1	0x40011D34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX84_MS_ATT2	0x40011D38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX84_MS_ATT3	0x40011D3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX85_SL_ADDR	0x40011D40	Slave region, base address
PERI_MS_PPU_FX85_SL_SIZE	0x40011D44	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX85_SL_ATT0	0x40011D50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX85_SL_ATT1	0x40011D54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX85_SL_ATT2	0x40011D58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX85_SL_ATT3	0x40011D5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX85_MS_ADDR	0x40011D60	Master region, base address
PERI_MS_PPU_FX85_MS_SIZE	0x40011D64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX85_MS_ATT0	0x40011D70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX85_MS_ATT1	0x40011D74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX85_MS_ATT2	0x40011D78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX85_MS_ATT3	0x40011D7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX86_SL_ADDR	0x40011D80	Slave region, base address
PERI_MS_PPU_FX86_SL_SIZE	0x40011D84	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX86_SL_ATT0	0x40011D90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX86_SL_ATT1	0x40011D94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX86_SL_ATT2	0x40011D98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX86_SL_ATT3	0x40011D9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX86_MS_ADDR	0x40011DA0	Master region, base address
PERI_MS_PPU_FX86_MS_SIZE	0x40011DA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX86_MS_ATT0	0x40011DB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX86_MS_ATT1	0x40011DB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX86_MS_ATT2	0x40011DB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX86_MS_ATT3	0x40011DBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX87_SL_ADDR	0x40011DC0	Slave region, base address
PERI_MS_PPU_FX87_SL_SIZE	0x40011DC4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX87_SL_ATT0	0x40011DD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX87_SL_ATT1	0x40011DD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX87_SL_ATT2	0x40011DD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX87_SL_ATT3	0x40011DDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX87_MS_ADDR	0x40011DE0	Master region, base address
PERI_MS_PPU_FX87_MS_SIZE	0x40011DE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX87_MS_ATT0	0x40011DF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX87_MS_ATT1	0x40011DF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX87_MS_ATT2	0x40011DF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX87_MS_ATT3	0x40011DFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX88_SL_ADDR	0x40011E00	Slave region, base address
PERI_MS_PPU_FX88_SL_SIZE	0x40011E04	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX88_SL_ATT0	0x40011E10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX88_SL_ATT1	0x40011E14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX88_SL_ATT2	0x40011E18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX88_SL_ATT3	0x40011E1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX88_MS_ADDR	0x40011E20	Master region, base address
PERI_MS_PPU_FX88_MS_SIZE	0x40011E24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX88_MS_ATT0	0x40011E30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX88_MS_ATT1	0x40011E34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX88_MS_ATT2	0x40011E38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX88_MS_ATT3	0x40011E3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX89_SL_ADDR	0x40011E40	Slave region, base address
PERI_MS_PPU_FX89_SL_SIZE	0x40011E44	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX89_SL_ATT0	0x40011E50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX89_SL_ATT1	0x40011E54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX89_SL_ATT2	0x40011E58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX89_SL_ATT3	0x40011E5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX89_MS_ADDR	0x40011E60	Master region, base address
PERI_MS_PPU_FX89_MS_SIZE	0x40011E64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX89_MS_ATT0	0x40011E70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX89_MS_ATT1	0x40011E74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX89_MS_ATT2	0x40011E78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX89_MS_ATT3	0x40011E7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX90_SL_ADDR	0x40011E80	Slave region, base address
PERI_MS_PPU_FX90_SL_SIZE	0x40011E84	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX90_SL_ATT0	0x40011E90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX90_SL_ATT1	0x40011E94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX90_SL_ATT2	0x40011E98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX90_SL_ATT3	0x40011E9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX90_MS_ADDR	0x40011EA0	Master region, base address
PERI_MS_PPU_FX90_MS_SIZE	0x40011EA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX90_MS_ATT0	0x40011EB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX90_MS_ATT1	0x40011EB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX90_MS_ATT2	0x40011EB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX90_MS_ATT3	0x40011EBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX91_SL_ADDR	0x40011EC0	Slave region, base address
PERI_MS_PPU_FX91_SL_SIZE	0x40011EC4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX91_SL_ATT0	0x40011ED0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX91_SL_ATT1	0x40011ED4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX91_SL_ATT2	0x40011ED8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX91_SL_ATT3	0x40011EDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX91_MS_ADDR	0x40011EE0	Master region, base address
PERI_MS_PPU_FX91_MS_SIZE	0x40011EE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX91_MS_ATT0	0x40011EF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX91_MS_ATT1	0x40011EF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX91_MS_ATT2	0x40011EF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX91_MS_ATT3	0x40011EFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX92_SL_ADDR	0x40011F00	Slave region, base address
PERI_MS_PPU_FX92_SL_SIZE	0x40011F04	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX92_SL_ATT0	0x40011F10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX92_SL_ATT1	0x40011F14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX92_SL_ATT2	0x40011F18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX92_SL_ATT3	0x40011F1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX92_MS_ADDR	0x40011F20	Master region, base address
PERI_MS_PPU_FX92_MS_SIZE	0x40011F24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX92_MS_ATT0	0x40011F30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX92_MS_ATT1	0x40011F34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX92_MS_ATT2	0x40011F38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX92_MS_ATT3	0x40011F3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX93_SL_ADDR	0x40011F40	Slave region, base address
PERI_MS_PPU_FX93_SL_SIZE	0x40011F44	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX93_SL_ATT0	0x40011F50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX93_SL_ATT1	0x40011F54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX93_SL_ATT2	0x40011F58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX93_SL_ATT3	0x40011F5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX93_MS_ADDR	0x40011F60	Master region, base address
PERI_MS_PPU_FX93_MS_SIZE	0x40011F64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX93_MS_ATT0	0x40011F70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX93_MS_ATT1	0x40011F74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX93_MS_ATT2	0x40011F78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX93_MS_ATT3	0x40011F7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX94_SL_ADDR	0x40011F80	Slave region, base address
PERI_MS_PPU_FX94_SL_SIZE	0x40011F84	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX94_SL_ATT0	0x40011F90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX94_SL_ATT1	0x40011F94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX94_SL_ATT2	0x40011F98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX94_SL_ATT3	0x40011F9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX94_MS_ADDR	0x40011FA0	Master region, base address
PERI_MS_PPU_FX94_MS_SIZE	0x40011FA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX94_MS_ATT0	0x40011FB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX94_MS_ATT1	0x40011FB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX94_MS_ATT2	0x40011FB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX94_MS_ATT3	0x40011FBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX95_SL_ADDR	0x40011FC0	Slave region, base address
PERI_MS_PPU_FX95_SL_SIZE	0x40011FC4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX95_SL_ATT0	0x40011FD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX95_SL_ATT1	0x40011FD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX95_SL_ATT2	0x40011FD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX95_SL_ATT3	0x40011FDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX95_MS_ADDR	0x40011FE0	Master region, base address
PERI_MS_PPU_FX95_MS_SIZE	0x40011FE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX95_MS_ATT0	0x40011FF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX95_MS_ATT1	0x40011FF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX95_MS_ATT2	0x40011FF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX95_MS_ATT3	0x40011FFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX96_SL_ADDR	0x40012000	Slave region, base address
PERI_MS_PPU_FX96_SL_SIZE	0x40012004	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX96_SL_ATT0	0x40012010	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX96_SL_ATT1	0x40012014	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX96_SL_ATT2	0x40012018	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX96_SL_ATT3	0x4001201C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX96_MS_ADDR	0x40012020	Master region, base address
PERI_MS_PPU_FX96_MS_SIZE	0x40012024	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX96_MS_ATT0	0x40012030	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX96_MS_ATT1	0x40012034	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX96_MS_ATT2	0x40012038	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX96_MS_ATT3	0x4001203C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX97_SL_ADDR	0x40012040	Slave region, base address
PERI_MS_PPU_FX97_SL_SIZE	0x40012044	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX97_SL_ATT0	0x40012050	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX97_SL_ATT1	0x40012054	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX97_SL_ATT2	0x40012058	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX97_SL_ATT3	0x4001205C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX97_MS_ADDR	0x40012060	Master region, base address
PERI_MS_PPU_FX97_MS_SIZE	0x40012064	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX97_MS_ATT0	0x40012070	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX97_MS_ATT1	0x40012074	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX97_MS_ATT2	0x40012078	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX97_MS_ATT3	0x4001207C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX98_SL_ADDR	0x40012080	Slave region, base address
PERI_MS_PPU_FX98_SL_SIZE	0x40012084	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX98_SL_ATT0	0x40012090	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX98_SL_ATT1	0x40012094	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX98_SL_ATT2	0x40012098	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX98_SL_ATT3	0x4001209C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX98_MS_ADDR	0x400120A0	Master region, base address
PERI_MS_PPU_FX98_MS_SIZE	0x400120A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX98_MS_ATT0	0x400120B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX98_MS_ATT1	0x400120B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX98_MS_ATT2	0x400120B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX98_MS_ATT3	0x400120BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX99_SL_ADDR	0x400120C0	Slave region, base address
PERI_MS_PPU_FX99_SL_SIZE	0x400120C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX99_SL_ATT0	0x400120D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX99_SL_ATT1	0x400120D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX99_SL_ATT2	0x400120D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX99_SL_ATT3	0x400120DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX99_MS_ADDR	0x400120E0	Master region, base address
PERI_MS_PPU_FX99_MS_SIZE	0x400120E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX99_MS_ATT0	0x400120F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX99_MS_ATT1	0x400120F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX99_MS_ATT2	0x400120F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX99_MS_ATT3	0x400120FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX100_SL_ADDR	0x40012100	Slave region, base address
PERI_MS_PPU_FX100_SL_SIZE	0x40012104	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX100_SL_ATT0	0x40012110	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX100_SL_ATT1	0x40012114	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX100_SL_ATT2	0x40012118	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX100_SL_ATT3	0x4001211C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX100_MS_ADDR	0x40012120	Master region, base address
PERI_MS_PPU_FX100_MS_SIZE	0x40012124	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX100_MS_ATT0	0x40012130	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX100_MS_ATT1	0x40012134	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX100_MS_ATT2	0x40012138	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX100_MS_ATT3	0x4001213C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX101_SL_ADDR	0x40012140	Slave region, base address
PERI_MS_PPU_FX101_SL_SIZE	0x40012144	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX101_SL_ATT0	0x40012150	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX101_SL_ATT1	0x40012154	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX101_SL_ATT2	0x40012158	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX101_SL_ATT3	0x4001215C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX101_MS_ADDR	0x40012160	Master region, base address
PERI_MS_PPU_FX101_MS_SIZE	0x40012164	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX101_MS_ATT0	0x40012170	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX101_MS_ATT1	0x40012174	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX101_MS_ATT2	0x40012178	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX101_MS_ATT3	0x4001217C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX102_SL_ADDR	0x40012180	Slave region, base address
PERI_MS_PPU_FX102_SL_SIZE	0x40012184	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX102_SL_ATT0	0x40012190	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX102_SL_ATT1	0x40012194	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX102_SL_ATT2	0x40012198	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX102_SL_ATT3	0x4001219C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX102_MS_ADDR	0x400121A0	Master region, base address
PERI_MS_PPU_FX102_MS_SIZE	0x400121A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX102_MS_ATT0	0x400121B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX102_MS_ATT1	0x400121B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX102_MS_ATT2	0x400121B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX102_MS_ATT3	0x400121BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX103_SL_ADDR	0x400121C0	Slave region, base address
PERI_MS_PPU_FX103_SL_SIZE	0x400121C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX103_SL_ATT0	0x400121D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX103_SL_ATT1	0x400121D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX103_SL_ATT2	0x400121D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX103_SL_ATT3	0x400121DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX103_MS_ADDR	0x400121E0	Master region, base address
PERI_MS_PPU_FX103_MS_SIZE	0x400121E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX103_MS_ATT0	0x400121F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX103_MS_ATT1	0x400121F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX103_MS_ATT2	0x400121F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX103_MS_ATT3	0x400121FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX104_SL_ADDR	0x40012200	Slave region, base address
PERI_MS_PPU_FX104_SL_SIZE	0x40012204	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX104_SL_ATT0	0x40012210	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX104_SL_ATT1	0x40012214	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX104_SL_ATT2	0x40012218	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX104_SL_ATT3	0x4001221C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX104_MS_ADDR	0x40012220	Master region, base address
PERI_MS_PPU_FX104_MS_SIZE	0x40012224	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX104_MS_ATT0	0x40012230	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX104_MS_ATT1	0x40012234	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX104_MS_ATT2	0x40012238	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX104_MS_ATT3	0x4001223C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX105_SL_ADDR	0x40012240	Slave region, base address
PERI_MS_PPU_FX105_SL_SIZE	0x40012244	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX105_SL_ATT0	0x40012250	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX105_SL_ATT1	0x40012254	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX105_SL_ATT2	0x40012258	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX105_SL_ATT3	0x4001225C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX105_MS_ADDR	0x40012260	Master region, base address
PERI_MS_PPU_FX105_MS_SIZE	0x40012264	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX105_MS_ATT0	0x40012270	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX105_MS_ATT1	0x40012274	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX105_MS_ATT2	0x40012278	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX105_MS_ATT3	0x4001227C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX106_SL_ADDR	0x40012280	Slave region, base address
PERI_MS_PPU_FX106_SL_SIZE	0x40012284	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX106_SL_ATT0	0x40012290	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX106_SL_ATT1	0x40012294	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX106_SL_ATT2	0x40012298	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX106_SL_ATT3	0x4001229C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX106_MS_ADDR	0x400122A0	Master region, base address
PERI_MS_PPU_FX106_MS_SIZE	0x400122A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX106_MS_ATT0	0x400122B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX106_MS_ATT1	0x400122B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX106_MS_ATT2	0x400122B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX106_MS_ATT3	0x400122BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX107_SL_ADDR	0x400122C0	Slave region, base address
PERI_MS_PPU_FX107_SL_SIZE	0x400122C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX107_SL_ATT0	0x400122D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX107_SL_ATT1	0x400122D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX107_SL_ATT2	0x400122D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX107_SL_ATT3	0x400122DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX107_MS_ADDR	0x400122E0	Master region, base address
PERI_MS_PPU_FX107_MS_SIZE	0x400122E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX107_MS_ATT0	0x400122F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX107_MS_ATT1	0x400122F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX107_MS_ATT2	0x400122F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX107_MS_ATT3	0x400122FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX108_SL_ADDR	0x40012300	Slave region, base address
PERI_MS_PPU_FX108_SL_SIZE	0x40012304	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX108_SL_ATT0	0x40012310	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX108_SL_ATT1	0x40012314	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX108_SL_ATT2	0x40012318	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX108_SL_ATT3	0x4001231C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX108_MS_ADDR	0x40012320	Master region, base address
PERI_MS_PPU_FX108_MS_SIZE	0x40012324	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX108_MS_ATT0	0x40012330	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX108_MS_ATT1	0x40012334	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX108_MS_ATT2	0x40012338	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX108_MS_ATT3	0x4001233C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX109_SL_ADDR	0x40012340	Slave region, base address
PERI_MS_PPU_FX109_SL_SIZE	0x40012344	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX109_SL_ATT0	0x40012350	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX109_SL_ATT1	0x40012354	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX109_SL_ATT2	0x40012358	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX109_SL_ATT3	0x4001235C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX109_MS_ADDR	0x40012360	Master region, base address
PERI_MS_PPU_FX109_MS_SIZE	0x40012364	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX109_MS_ATT0	0x40012370	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX109_MS_ATT1	0x40012374	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX109_MS_ATT2	0x40012378	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX109_MS_ATT3	0x4001237C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX110_SL_ADDR	0x40012380	Slave region, base address
PERI_MS_PPU_FX110_SL_SIZE	0x40012384	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX110_SL_ATT0	0x40012390	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX110_SL_ATT1	0x40012394	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX110_SL_ATT2	0x40012398	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX110_SL_ATT3	0x4001239C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX110_MS_ADDR	0x400123A0	Master region, base address
PERI_MS_PPU_FX110_MS_SIZE	0x400123A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX110_MS_ATT0	0x400123B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX110_MS_ATT1	0x400123B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX110_MS_ATT2	0x400123B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX110_MS_ATT3	0x400123BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX111_SL_ADDR	0x400123C0	Slave region, base address
PERI_MS_PPU_FX111_SL_SIZE	0x400123C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX111_SL_ATT0	0x400123D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX111_SL_ATT1	0x400123D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX111_SL_ATT2	0x400123D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX111_SL_ATT3	0x400123DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX111_MS_ADDR	0x400123E0	Master region, base address
PERI_MS_PPU_FX111_MS_SIZE	0x400123E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX111_MS_ATT0	0x400123F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX111_MS_ATT1	0x400123F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX111_MS_ATT2	0x400123F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX111_MS_ATT3	0x400123FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX112_SL_ADDR	0x40012400	Slave region, base address
PERI_MS_PPU_FX112_SL_SIZE	0x40012404	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX112_SL_ATT0	0x40012410	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX112_SL_ATT1	0x40012414	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX112_SL_ATT2	0x40012418	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX112_SL_ATT3	0x4001241C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX112_MS_ADDR	0x40012420	Master region, base address
PERI_MS_PPU_FX112_MS_SIZE	0x40012424	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX112_MS_ATT0	0x40012430	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX112_MS_ATT1	0x40012434	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX112_MS_ATT2	0x40012438	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX112_MS_ATT3	0x4001243C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX113_SL_ADDR	0x40012440	Slave region, base address
PERI_MS_PPU_FX113_SL_SIZE	0x40012444	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX113_SL_ATT0	0x40012450	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX113_SL_ATT1	0x40012454	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX113_SL_ATT2	0x40012458	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX113_SL_ATT3	0x4001245C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX113_MS_ADDR	0x40012460	Master region, base address
PERI_MS_PPU_FX113_MS_SIZE	0x40012464	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX113_MS_ATT0	0x40012470	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX113_MS_ATT1	0x40012474	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX113_MS_ATT2	0x40012478	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX113_MS_ATT3	0x4001247C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX114_SL_ADDR	0x40012480	Slave region, base address
PERI_MS_PPU_FX114_SL_SIZE	0x40012484	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX114_SL_ATT0	0x40012490	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX114_SL_ATT1	0x40012494	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX114_SL_ATT2	0x40012498	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX114_SL_ATT3	0x4001249C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX114_MS_ADDR	0x400124A0	Master region, base address
PERI_MS_PPU_FX114_MS_SIZE	0x400124A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX114_MS_ATT0	0x400124B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX114_MS_ATT1	0x400124B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX114_MS_ATT2	0x400124B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX114_MS_ATT3	0x400124BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX115_SL_ADDR	0x400124C0	Slave region, base address
PERI_MS_PPU_FX115_SL_SIZE	0x400124C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX115_SL_ATT0	0x400124D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX115_SL_ATT1	0x400124D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX115_SL_ATT2	0x400124D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX115_SL_ATT3	0x400124DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX115_MS_ADDR	0x400124E0	Master region, base address
PERI_MS_PPU_FX115_MS_SIZE	0x400124E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX115_MS_ATT0	0x400124F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX115_MS_ATT1	0x400124F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX115_MS_ATT2	0x400124F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX115_MS_ATT3	0x400124FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX116_SL_ADDR	0x40012500	Slave region, base address
PERI_MS_PPU_FX116_SL_SIZE	0x40012504	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX116_SL_ATT0	0x40012510	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX116_SL_ATT1	0x40012514	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX116_SL_ATT2	0x40012518	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX116_SL_ATT3	0x4001251C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX116_MS_ADDR	0x40012520	Master region, base address
PERI_MS_PPU_FX116_MS_SIZE	0x40012524	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX116_MS_ATT0	0x40012530	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX116_MS_ATT1	0x40012534	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX116_MS_ATT2	0x40012538	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX116_MS_ATT3	0x4001253C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX117_SL_ADDR	0x40012540	Slave region, base address
PERI_MS_PPU_FX117_SL_SIZE	0x40012544	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX117_SL_ATT0	0x40012550	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX117_SL_ATT1	0x40012554	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX117_SL_ATT2	0x40012558	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX117_SL_ATT3	0x4001255C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX117_MS_ADDR	0x40012560	Master region, base address
PERI_MS_PPU_FX117_MS_SIZE	0x40012564	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX117_MS_ATT0	0x40012570	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX117_MS_ATT1	0x40012574	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX117_MS_ATT2	0x40012578	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX117_MS_ATT3	0x4001257C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX118_SL_ADDR	0x40012580	Slave region, base address
PERI_MS_PPU_FX118_SL_SIZE	0x40012584	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX118_SL_ATT0	0x40012590	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX118_SL_ATT1	0x40012594	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX118_SL_ATT2	0x40012598	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX118_SL_ATT3	0x4001259C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX118_MS_ADDR	0x400125A0	Master region, base address
PERI_MS_PPU_FX118_MS_SIZE	0x400125A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX118_MS_ATT0	0x400125B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX118_MS_ATT1	0x400125B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX118_MS_ATT2	0x400125B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX118_MS_ATT3	0x400125BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX119_SL_ADDR	0x400125C0	Slave region, base address
PERI_MS_PPU_FX119_SL_SIZE	0x400125C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX119_SL_ATT0	0x400125D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX119_SL_ATT1	0x400125D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX119_SL_ATT2	0x400125D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX119_SL_ATT3	0x400125DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX119_MS_ADDR	0x400125E0	Master region, base address
PERI_MS_PPU_FX119_MS_SIZE	0x400125E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX119_MS_ATT0	0x400125F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX119_MS_ATT1	0x400125F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX119_MS_ATT2	0x400125F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX119_MS_ATT3	0x400125FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX120_SL_ADDR	0x40012600	Slave region, base address
PERI_MS_PPU_FX120_SL_SIZE	0x40012604	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX120_SL_ATT0	0x40012610	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX120_SL_ATT1	0x40012614	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX120_SL_ATT2	0x40012618	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX120_SL_ATT3	0x4001261C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX120_MS_ADDR	0x40012620	Master region, base address
PERI_MS_PPU_FX120_MS_SIZE	0x40012624	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX120_MS_ATT0	0x40012630	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX120_MS_ATT1	0x40012634	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX120_MS_ATT2	0x40012638	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX120_MS_ATT3	0x4001263C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX121_SL_ADDR	0x40012640	Slave region, base address
PERI_MS_PPU_FX121_SL_SIZE	0x40012644	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX121_SL_ATT0	0x40012650	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX121_SL_ATT1	0x40012654	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX121_SL_ATT2	0x40012658	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX121_SL_ATT3	0x4001265C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX121_MS_ADDR	0x40012660	Master region, base address
PERI_MS_PPU_FX121_MS_SIZE	0x40012664	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX121_MS_ATT0	0x40012670	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX121_MS_ATT1	0x40012674	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX121_MS_ATT2	0x40012678	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX121_MS_ATT3	0x4001267C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX122_SL_ADDR	0x40012680	Slave region, base address
PERI_MS_PPU_FX122_SL_SIZE	0x40012684	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX122_SL_ATT0	0x40012690	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX122_SL_ATT1	0x40012694	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX122_SL_ATT2	0x40012698	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX122_SL_ATT3	0x4001269C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX122_MS_ADDR	0x400126A0	Master region, base address
PERI_MS_PPU_FX122_MS_SIZE	0x400126A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX122_MS_ATT0	0x400126B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX122_MS_ATT1	0x400126B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX122_MS_ATT2	0x400126B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX122_MS_ATT3	0x400126BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX123_SL_ADDR	0x400126C0	Slave region, base address
PERI_MS_PPU_FX123_SL_SIZE	0x400126C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX123_SL_ATT0	0x400126D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX123_SL_ATT1	0x400126D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX123_SL_ATT2	0x400126D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX123_SL_ATT3	0x400126DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX123_MS_ADDR	0x400126E0	Master region, base address
PERI_MS_PPU_FX123_MS_SIZE	0x400126E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX123_MS_ATT0	0x400126F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX123_MS_ATT1	0x400126F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX123_MS_ATT2	0x400126F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX123_MS_ATT3	0x400126FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX124_SL_ADDR	0x40012700	Slave region, base address
PERI_MS_PPU_FX124_SL_SIZE	0x40012704	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX124_SL_ATT0	0x40012710	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX124_SL_ATT1	0x40012714	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX124_SL_ATT2	0x40012718	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX124_SL_ATT3	0x4001271C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX124_MS_ADDR	0x40012720	Master region, base address
PERI_MS_PPU_FX124_MS_SIZE	0x40012724	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX124_MS_ATT0	0x40012730	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX124_MS_ATT1	0x40012734	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX124_MS_ATT2	0x40012738	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX124_MS_ATT3	0x4001273C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX125_SL_ADDR	0x40012740	Slave region, base address
PERI_MS_PPU_FX125_SL_SIZE	0x40012744	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX125_SL_ATT0	0x40012750	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX125_SL_ATT1	0x40012754	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX125_SL_ATT2	0x40012758	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX125_SL_ATT3	0x4001275C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX125_MS_ADDR	0x40012760	Master region, base address
PERI_MS_PPU_FX125_MS_SIZE	0x40012764	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX125_MS_ATT0	0x40012770	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX125_MS_ATT1	0x40012774	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX125_MS_ATT2	0x40012778	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX125_MS_ATT3	0x4001277C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX126_SL_ADDR	0x40012780	Slave region, base address
PERI_MS_PPU_FX126_SL_SIZE	0x40012784	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX126_SL_ATT0	0x40012790	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX126_SL_ATT1	0x40012794	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX126_SL_ATT2	0x40012798	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX126_SL_ATT3	0x4001279C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX126_MS_ADDR	0x400127A0	Master region, base address
PERI_MS_PPU_FX126_MS_SIZE	0x400127A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX126_MS_ATT0	0x400127B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX126_MS_ATT1	0x400127B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX126_MS_ATT2	0x400127B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX126_MS_ATT3	0x400127BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX127_SL_ADDR	0x400127C0	Slave region, base address
PERI_MS_PPU_FX127_SL_SIZE	0x400127C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX127_SL_ATT0	0x400127D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX127_SL_ATT1	0x400127D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX127_SL_ATT2	0x400127D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX127_SL_ATT3	0x400127DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX127_MS_ADDR	0x400127E0	Master region, base address
PERI_MS_PPU_FX127_MS_SIZE	0x400127E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX127_MS_ATT0	0x400127F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX127_MS_ATT1	0x400127F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX127_MS_ATT2	0x400127F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX127_MS_ATT3	0x400127FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX128_SL_ADDR	0x40012800	Slave region, base address
PERI_MS_PPU_FX128_SL_SIZE	0x40012804	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX128_SL_ATT0	0x40012810	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX128_SL_ATT1	0x40012814	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX128_SL_ATT2	0x40012818	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX128_SL_ATT3	0x4001281C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX128_MS_ADDR	0x40012820	Master region, base address
PERI_MS_PPU_FX128_MS_SIZE	0x40012824	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX128_MS_ATT0	0x40012830	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX128_MS_ATT1	0x40012834	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX128_MS_ATT2	0x40012838	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX128_MS_ATT3	0x4001283C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX129_SL_ADDR	0x40012840	Slave region, base address
PERI_MS_PPU_FX129_SL_SIZE	0x40012844	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX129_SL_ATT0	0x40012850	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX129_SL_ATT1	0x40012854	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX129_SL_ATT2	0x40012858	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX129_SL_ATT3	0x4001285C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX129_MS_ADDR	0x40012860	Master region, base address
PERI_MS_PPU_FX129_MS_SIZE	0x40012864	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX129_MS_ATT0	0x40012870	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX129_MS_ATT1	0x40012874	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX129_MS_ATT2	0x40012878	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX129_MS_ATT3	0x4001287C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX130_SL_ADDR	0x40012880	Slave region, base address
PERI_MS_PPU_FX130_SL_SIZE	0x40012884	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX130_SL_ATT0	0x40012890	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX130_SL_ATT1	0x40012894	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX130_SL_ATT2	0x40012898	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX130_SL_ATT3	0x4001289C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX130_MS_ADDR	0x400128A0	Master region, base address
PERI_MS_PPU_FX130_MS_SIZE	0x400128A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX130_MS_ATT0	0x400128B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX130_MS_ATT1	0x400128B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX130_MS_ATT2	0x400128B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX130_MS_ATT3	0x400128BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX131_SL_ADDR	0x400128C0	Slave region, base address
PERI_MS_PPU_FX131_SL_SIZE	0x400128C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX131_SL_ATT0	0x400128D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX131_SL_ATT1	0x400128D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX131_SL_ATT2	0x400128D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX131_SL_ATT3	0x400128DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX131_MS_ADDR	0x400128E0	Master region, base address
PERI_MS_PPU_FX131_MS_SIZE	0x400128E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX131_MS_ATT0	0x400128F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX131_MS_ATT1	0x400128F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX131_MS_ATT2	0x400128F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX131_MS_ATT3	0x400128FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX132_SL_ADDR	0x40012900	Slave region, base address
PERI_MS_PPU_FX132_SL_SIZE	0x40012904	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX132_SL_ATT0	0x40012910	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX132_SL_ATT1	0x40012914	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX132_SL_ATT2	0x40012918	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX132_SL_ATT3	0x4001291C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX132_MS_ADDR	0x40012920	Master region, base address
PERI_MS_PPU_FX132_MS_SIZE	0x40012924	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX132_MS_ATT0	0x40012930	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX132_MS_ATT1	0x40012934	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX132_MS_ATT2	0x40012938	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX132_MS_ATT3	0x4001293C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX133_SL_ADDR	0x40012940	Slave region, base address
PERI_MS_PPU_FX133_SL_SIZE	0x40012944	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX133_SL_ATT0	0x40012950	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX133_SL_ATT1	0x40012954	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX133_SL_ATT2	0x40012958	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX133_SL_ATT3	0x4001295C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX133_MS_ADDR	0x40012960	Master region, base address
PERI_MS_PPU_FX133_MS_SIZE	0x40012964	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX133_MS_ATT0	0x40012970	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX133_MS_ATT1	0x40012974	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX133_MS_ATT2	0x40012978	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX133_MS_ATT3	0x4001297C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX134_SL_ADDR	0x40012980	Slave region, base address
PERI_MS_PPU_FX134_SL_SIZE	0x40012984	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX134_SL_ATT0	0x40012990	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX134_SL_ATT1	0x40012994	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX134_SL_ATT2	0x40012998	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX134_SL_ATT3	0x4001299C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX134_MS_ADDR	0x400129A0	Master region, base address
PERI_MS_PPU_FX134_MS_SIZE	0x400129A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX134_MS_ATT0	0x400129B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX134_MS_ATT1	0x400129B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX134_MS_ATT2	0x400129B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX134_MS_ATT3	0x400129BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX135_SL_ADDR	0x400129C0	Slave region, base address
PERI_MS_PPU_FX135_SL_SIZE	0x400129C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX135_SL_ATT0	0x400129D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX135_SL_ATT1	0x400129D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX135_SL_ATT2	0x400129D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX135_SL_ATT3	0x400129DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX135_MS_ADDR	0x400129E0	Master region, base address
PERI_MS_PPU_FX135_MS_SIZE	0x400129E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX135_MS_ATT0	0x400129F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX135_MS_ATT1	0x400129F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX135_MS_ATT2	0x400129F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX135_MS_ATT3	0x400129FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX136_SL_ADDR	0x40012A00	Slave region, base address
PERI_MS_PPU_FX136_SL_SIZE	0x40012A04	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX136_SL_ATT0	0x40012A10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX136_SL_ATT1	0x40012A14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX136_SL_ATT2	0x40012A18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX136_SL_ATT3	0x40012A1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX136_MS_ADDR	0x40012A20	Master region, base address
PERI_MS_PPU_FX136_MS_SIZE	0x40012A24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX136_MS_ATT0	0x40012A30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX136_MS_ATT1	0x40012A34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX136_MS_ATT2	0x40012A38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX136_MS_ATT3	0x40012A3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX137_SL_ADDR	0x40012A40	Slave region, base address
PERI_MS_PPU_FX137_SL_SIZE	0x40012A44	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX137_SL_ATT0	0x40012A50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX137_SL_ATT1	0x40012A54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX137_SL_ATT2	0x40012A58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX137_SL_ATT3	0x40012A5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX137_MS_ADDR	0x40012A60	Master region, base address
PERI_MS_PPU_FX137_MS_SIZE	0x40012A64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX137_MS_ATT0	0x40012A70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX137_MS_ATT1	0x40012A74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX137_MS_ATT2	0x40012A78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX137_MS_ATT3	0x40012A7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX138_SL_ADDR	0x40012A80	Slave region, base address
PERI_MS_PPU_FX138_SL_SIZE	0x40012A84	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX138_SL_ATT0	0x40012A90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX138_SL_ATT1	0x40012A94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX138_SL_ATT2	0x40012A98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX138_SL_ATT3	0x40012A9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX138_MS_ADDR	0x40012AA0	Master region, base address
PERI_MS_PPU_FX138_MS_SIZE	0x40012AA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX138_MS_ATT0	0x40012AB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX138_MS_ATT1	0x40012AB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX138_MS_ATT2	0x40012AB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX138_MS_ATT3	0x40012ABC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX139_SL_ADDR	0x40012AC0	Slave region, base address
PERI_MS_PPU_FX139_SL_SIZE	0x40012AC4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX139_SL_ATT0	0x40012AD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX139_SL_ATT1	0x40012AD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX139_SL_ATT2	0x40012AD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX139_SL_ATT3	0x40012ADC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX139_MS_ADDR	0x40012AE0	Master region, base address
PERI_MS_PPU_FX139_MS_SIZE	0x40012AE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX139_MS_ATT0	0x40012AF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX139_MS_ATT1	0x40012AF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX139_MS_ATT2	0x40012AF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX139_MS_ATT3	0x40012AFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX140_SL_ADDR	0x40012B00	Slave region, base address
PERI_MS_PPU_FX140_SL_SIZE	0x40012B04	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX140_SL_ATT0	0x40012B10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX140_SL_ATT1	0x40012B14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX140_SL_ATT2	0x40012B18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX140_SL_ATT3	0x40012B1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX140_MS_ADDR	0x40012B20	Master region, base address
PERI_MS_PPU_FX140_MS_SIZE	0x40012B24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX140_MS_ATT0	0x40012B30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX140_MS_ATT1	0x40012B34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX140_MS_ATT2	0x40012B38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX140_MS_ATT3	0x40012B3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX141_SL_ADDR	0x40012B40	Slave region, base address
PERI_MS_PPU_FX141_SL_SIZE	0x40012B44	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX141_SL_ATT0	0x40012B50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX141_SL_ATT1	0x40012B54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX141_SL_ATT2	0x40012B58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX141_SL_ATT3	0x40012B5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX141_MS_ADDR	0x40012B60	Master region, base address
PERI_MS_PPU_FX141_MS_SIZE	0x40012B64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX141_MS_ATT0	0x40012B70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX141_MS_ATT1	0x40012B74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX141_MS_ATT2	0x40012B78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX141_MS_ATT3	0x40012B7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX142_SL_ADDR	0x40012B80	Slave region, base address
PERI_MS_PPU_FX142_SL_SIZE	0x40012B84	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX142_SL_ATT0	0x40012B90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX142_SL_ATT1	0x40012B94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX142_SL_ATT2	0x40012B98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX142_SL_ATT3	0x40012B9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX142_MS_ADDR	0x40012BA0	Master region, base address
PERI_MS_PPU_FX142_MS_SIZE	0x40012BA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX142_MS_ATT0	0x40012BB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX142_MS_ATT1	0x40012BB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX142_MS_ATT2	0x40012BB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX142_MS_ATT3	0x40012BBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX143_SL_ADDR	0x40012BC0	Slave region, base address
PERI_MS_PPU_FX143_SL_SIZE	0x40012BC4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX143_SL_ATT0	0x40012BD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX143_SL_ATT1	0x40012BD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX143_SL_ATT2	0x40012BD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX143_SL_ATT3	0x40012BDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX143_MS_ADDR	0x40012BE0	Master region, base address
PERI_MS_PPU_FX143_MS_SIZE	0x40012BE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX143_MS_ATT0	0x40012BF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX143_MS_ATT1	0x40012BF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX143_MS_ATT2	0x40012BF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX143_MS_ATT3	0x40012BFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX144_SL_ADDR	0x40012C00	Slave region, base address
PERI_MS_PPU_FX144_SL_SIZE	0x40012C04	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX144_SL_ATT0	0x40012C10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX144_SL_ATT1	0x40012C14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX144_SL_ATT2	0x40012C18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX144_SL_ATT3	0x40012C1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX144_MS_ADDR	0x40012C20	Master region, base address
PERI_MS_PPU_FX144_MS_SIZE	0x40012C24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX144_MS_ATT0	0x40012C30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX144_MS_ATT1	0x40012C34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX144_MS_ATT2	0x40012C38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX144_MS_ATT3	0x40012C3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX145_SL_ADDR	0x40012C40	Slave region, base address
PERI_MS_PPU_FX145_SL_SIZE	0x40012C44	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX145_SL_ATT0	0x40012C50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX145_SL_ATT1	0x40012C54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX145_SL_ATT2	0x40012C58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX145_SL_ATT3	0x40012C5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX145_MS_ADDR	0x40012C60	Master region, base address
PERI_MS_PPU_FX145_MS_SIZE	0x40012C64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX145_MS_ATT0	0x40012C70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX145_MS_ATT1	0x40012C74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX145_MS_ATT2	0x40012C78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX145_MS_ATT3	0x40012C7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX146_SL_ADDR	0x40012C80	Slave region, base address
PERI_MS_PPU_FX146_SL_SIZE	0x40012C84	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX146_SL_ATT0	0x40012C90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX146_SL_ATT1	0x40012C94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX146_SL_ATT2	0x40012C98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX146_SL_ATT3	0x40012C9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX146_MS_ADDR	0x40012CA0	Master region, base address
PERI_MS_PPU_FX146_MS_SIZE	0x40012CA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX146_MS_ATT0	0x40012CB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX146_MS_ATT1	0x40012CB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX146_MS_ATT2	0x40012CB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX146_MS_ATT3	0x40012CBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX147_SL_ADDR	0x40012CC0	Slave region, base address
PERI_MS_PPU_FX147_SL_SIZE	0x40012CC4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX147_SL_ATT0	0x40012CD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX147_SL_ATT1	0x40012CD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX147_SL_ATT2	0x40012CD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX147_SL_ATT3	0x40012CDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX147_MS_ADDR	0x40012CE0	Master region, base address
PERI_MS_PPU_FX147_MS_SIZE	0x40012CE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX147_MS_ATT0	0x40012CF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX147_MS_ATT1	0x40012CF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX147_MS_ATT2	0x40012CF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX147_MS_ATT3	0x40012CFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX148_SL_ADDR	0x40012D00	Slave region, base address
PERI_MS_PPU_FX148_SL_SIZE	0x40012D04	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX148_SL_ATT0	0x40012D10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX148_SL_ATT1	0x40012D14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX148_SL_ATT2	0x40012D18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX148_SL_ATT3	0x40012D1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX148_MS_ADDR	0x40012D20	Master region, base address
PERI_MS_PPU_FX148_MS_SIZE	0x40012D24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX148_MS_ATT0	0x40012D30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX148_MS_ATT1	0x40012D34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX148_MS_ATT2	0x40012D38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX148_MS_ATT3	0x40012D3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX149_SL_ADDR	0x40012D40	Slave region, base address
PERI_MS_PPU_FX149_SL_SIZE	0x40012D44	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX149_SL_ATT0	0x40012D50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX149_SL_ATT1	0x40012D54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX149_SL_ATT2	0x40012D58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX149_SL_ATT3	0x40012D5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX149_MS_ADDR	0x40012D60	Master region, base address
PERI_MS_PPU_FX149_MS_SIZE	0x40012D64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX149_MS_ATT0	0x40012D70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX149_MS_ATT1	0x40012D74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX149_MS_ATT2	0x40012D78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX149_MS_ATT3	0x40012D7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX150_SL_ADDR	0x40012D80	Slave region, base address
PERI_MS_PPU_FX150_SL_SIZE	0x40012D84	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX150_SL_ATT0	0x40012D90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX150_SL_ATT1	0x40012D94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX150_SL_ATT2	0x40012D98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX150_SL_ATT3	0x40012D9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX150_MS_ADDR	0x40012DA0	Master region, base address
PERI_MS_PPU_FX150_MS_SIZE	0x40012DA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX150_MS_ATT0	0x40012DB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX150_MS_ATT1	0x40012DB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX150_MS_ATT2	0x40012DB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX150_MS_ATT3	0x40012DBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX151_SL_ADDR	0x40012DC0	Slave region, base address
PERI_MS_PPU_FX151_SL_SIZE	0x40012DC4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX151_SL_ATT0	0x40012DD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX151_SL_ATT1	0x40012DD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX151_SL_ATT2	0x40012DD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX151_SL_ATT3	0x40012DDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX151_MS_ADDR	0x40012DE0	Master region, base address
PERI_MS_PPU_FX151_MS_SIZE	0x40012DE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX151_MS_ATT0	0x40012DF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX151_MS_ATT1	0x40012DF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX151_MS_ATT2	0x40012DF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX151_MS_ATT3	0x40012DFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX152_SL_ADDR	0x40012E00	Slave region, base address
PERI_MS_PPU_FX152_SL_SIZE	0x40012E04	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX152_SL_ATT0	0x40012E10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX152_SL_ATT1	0x40012E14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX152_SL_ATT2	0x40012E18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX152_SL_ATT3	0x40012E1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX152_MS_ADDR	0x40012E20	Master region, base address
PERI_MS_PPU_FX152_MS_SIZE	0x40012E24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX152_MS_ATT0	0x40012E30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX152_MS_ATT1	0x40012E34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX152_MS_ATT2	0x40012E38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX152_MS_ATT3	0x40012E3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX153_SL_ADDR	0x40012E40	Slave region, base address
PERI_MS_PPU_FX153_SL_SIZE	0x40012E44	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX153_SL_ATT0	0x40012E50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX153_SL_ATT1	0x40012E54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX153_SL_ATT2	0x40012E58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX153_SL_ATT3	0x40012E5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX153_MS_ADDR	0x40012E60	Master region, base address
PERI_MS_PPU_FX153_MS_SIZE	0x40012E64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX153_MS_ATT0	0x40012E70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX153_MS_ATT1	0x40012E74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX153_MS_ATT2	0x40012E78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX153_MS_ATT3	0x40012E7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX154_SL_ADDR	0x40012E80	Slave region, base address
PERI_MS_PPU_FX154_SL_SIZE	0x40012E84	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX154_SL_ATT0	0x40012E90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX154_SL_ATT1	0x40012E94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX154_SL_ATT2	0x40012E98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX154_SL_ATT3	0x40012E9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX154_MS_ADDR	0x40012EA0	Master region, base address
PERI_MS_PPU_FX154_MS_SIZE	0x40012EA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX154_MS_ATT0	0x40012EB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX154_MS_ATT1	0x40012EB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX154_MS_ATT2	0x40012EB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX154_MS_ATT3	0x40012EBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX155_SL_ADDR	0x40012EC0	Slave region, base address
PERI_MS_PPU_FX155_SL_SIZE	0x40012EC4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX155_SL_ATT0	0x40012ED0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX155_SL_ATT1	0x40012ED4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX155_SL_ATT2	0x40012ED8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX155_SL_ATT3	0x40012EDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX155_MS_ADDR	0x40012EE0	Master region, base address
PERI_MS_PPU_FX155_MS_SIZE	0x40012EE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX155_MS_ATT0	0x40012EF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX155_MS_ATT1	0x40012EF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX155_MS_ATT2	0x40012EF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX155_MS_ATT3	0x40012EFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX156_SL_ADDR	0x40012F00	Slave region, base address
PERI_MS_PPU_FX156_SL_SIZE	0x40012F04	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX156_SL_ATT0	0x40012F10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX156_SL_ATT1	0x40012F14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX156_SL_ATT2	0x40012F18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX156_SL_ATT3	0x40012F1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX156_MS_ADDR	0x40012F20	Master region, base address
PERI_MS_PPU_FX156_MS_SIZE	0x40012F24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX156_MS_ATT0	0x40012F30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX156_MS_ATT1	0x40012F34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX156_MS_ATT2	0x40012F38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX156_MS_ATT3	0x40012F3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX157_SL_ADDR	0x40012F40	Slave region, base address
PERI_MS_PPU_FX157_SL_SIZE	0x40012F44	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX157_SL_ATT0	0x40012F50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX157_SL_ATT1	0x40012F54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX157_SL_ATT2	0x40012F58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX157_SL_ATT3	0x40012F5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX157_MS_ADDR	0x40012F60	Master region, base address
PERI_MS_PPU_FX157_MS_SIZE	0x40012F64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX157_MS_ATT0	0x40012F70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX157_MS_ATT1	0x40012F74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX157_MS_ATT2	0x40012F78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX157_MS_ATT3	0x40012F7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX158_SL_ADDR	0x40012F80	Slave region, base address
PERI_MS_PPU_FX158_SL_SIZE	0x40012F84	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX158_SL_ATT0	0x40012F90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX158_SL_ATT1	0x40012F94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX158_SL_ATT2	0x40012F98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX158_SL_ATT3	0x40012F9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX158_MS_ADDR	0x40012FA0	Master region, base address
PERI_MS_PPU_FX158_MS_SIZE	0x40012FA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX158_MS_ATT0	0x40012FB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX158_MS_ATT1	0x40012FB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX158_MS_ATT2	0x40012FB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX158_MS_ATT3	0x40012FBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX159_SL_ADDR	0x40012FC0	Slave region, base address
PERI_MS_PPU_FX159_SL_SIZE	0x40012FC4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX159_SL_ATT0	0x40012FD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX159_SL_ATT1	0x40012FD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX159_SL_ATT2	0x40012FD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX159_SL_ATT3	0x40012FDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX159_MS_ADDR	0x40012FE0	Master region, base address
PERI_MS_PPU_FX159_MS_SIZE	0x40012FE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX159_MS_ATT0	0x40012FF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX159_MS_ATT1	0x40012FF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX159_MS_ATT2	0x40012FF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX159_MS_ATT3	0x40012FFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX160_SL_ADDR	0x40013000	Slave region, base address
PERI_MS_PPU_FX160_SL_SIZE	0x40013004	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX160_SL_ATT0	0x40013010	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX160_SL_ATT1	0x40013014	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX160_SL_ATT2	0x40013018	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX160_SL_ATT3	0x4001301C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX160_MS_ADDR	0x40013020	Master region, base address
PERI_MS_PPU_FX160_MS_SIZE	0x40013024	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX160_MS_ATT0	0x40013030	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX160_MS_ATT1	0x40013034	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX160_MS_ATT2	0x40013038	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX160_MS_ATT3	0x4001303C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX161_SL_ADDR	0x40013040	Slave region, base address
PERI_MS_PPU_FX161_SL_SIZE	0x40013044	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX161_SL_ATT0	0x40013050	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX161_SL_ATT1	0x40013054	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX161_SL_ATT2	0x40013058	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX161_SL_ATT3	0x4001305C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX161_MS_ADDR	0x40013060	Master region, base address
PERI_MS_PPU_FX161_MS_SIZE	0x40013064	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX161_MS_ATT0	0x40013070	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX161_MS_ATT1	0x40013074	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX161_MS_ATT2	0x40013078	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX161_MS_ATT3	0x4001307C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX162_SL_ADDR	0x40013080	Slave region, base address
PERI_MS_PPU_FX162_SL_SIZE	0x40013084	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX162_SL_ATT0	0x40013090	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX162_SL_ATT1	0x40013094	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX162_SL_ATT2	0x40013098	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX162_SL_ATT3	0x4001309C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX162_MS_ADDR	0x400130A0	Master region, base address
PERI_MS_PPU_FX162_MS_SIZE	0x400130A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX162_MS_ATT0	0x400130B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX162_MS_ATT1	0x400130B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX162_MS_ATT2	0x400130B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX162_MS_ATT3	0x400130BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX163_SL_ADDR	0x400130C0	Slave region, base address
PERI_MS_PPU_FX163_SL_SIZE	0x400130C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX163_SL_ATT0	0x400130D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX163_SL_ATT1	0x400130D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX163_SL_ATT2	0x400130D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX163_SL_ATT3	0x400130DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX163_MS_ADDR	0x400130E0	Master region, base address
PERI_MS_PPU_FX163_MS_SIZE	0x400130E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX163_MS_ATT0	0x400130F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX163_MS_ATT1	0x400130F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX163_MS_ATT2	0x400130F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX163_MS_ATT3	0x400130FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX164_SL_ADDR	0x40013100	Slave region, base address
PERI_MS_PPU_FX164_SL_SIZE	0x40013104	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX164_SL_ATT0	0x40013110	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX164_SL_ATT1	0x40013114	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX164_SL_ATT2	0x40013118	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX164_SL_ATT3	0x4001311C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX164_MS_ADDR	0x40013120	Master region, base address
PERI_MS_PPU_FX164_MS_SIZE	0x40013124	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX164_MS_ATT0	0x40013130	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX164_MS_ATT1	0x40013134	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX164_MS_ATT2	0x40013138	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX164_MS_ATT3	0x4001313C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX165_SL_ADDR	0x40013140	Slave region, base address
PERI_MS_PPU_FX165_SL_SIZE	0x40013144	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX165_SL_ATT0	0x40013150	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX165_SL_ATT1	0x40013154	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX165_SL_ATT2	0x40013158	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX165_SL_ATT3	0x4001315C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX165_MS_ADDR	0x40013160	Master region, base address
PERI_MS_PPU_FX165_MS_SIZE	0x40013164	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX165_MS_ATT0	0x40013170	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX165_MS_ATT1	0x40013174	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX165_MS_ATT2	0x40013178	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX165_MS_ATT3	0x4001317C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX166_SL_ADDR	0x40013180	Slave region, base address
PERI_MS_PPU_FX166_SL_SIZE	0x40013184	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX166_SL_ATT0	0x40013190	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX166_SL_ATT1	0x40013194	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX166_SL_ATT2	0x40013198	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX166_SL_ATT3	0x4001319C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX166_MS_ADDR	0x400131A0	Master region, base address
PERI_MS_PPU_FX166_MS_SIZE	0x400131A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX166_MS_ATT0	0x400131B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX166_MS_ATT1	0x400131B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX166_MS_ATT2	0x400131B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX166_MS_ATT3	0x400131BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX167_SL_ADDR	0x400131C0	Slave region, base address
PERI_MS_PPU_FX167_SL_SIZE	0x400131C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX167_SL_ATT0	0x400131D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX167_SL_ATT1	0x400131D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX167_SL_ATT2	0x400131D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX167_SL_ATT3	0x400131DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX167_MS_ADDR	0x400131E0	Master region, base address
PERI_MS_PPU_FX167_MS_SIZE	0x400131E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX167_MS_ATT0	0x400131F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX167_MS_ATT1	0x400131F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX167_MS_ATT2	0x400131F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX167_MS_ATT3	0x400131FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX168_SL_ADDR	0x40013200	Slave region, base address
PERI_MS_PPU_FX168_SL_SIZE	0x40013204	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX168_SL_ATT0	0x40013210	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX168_SL_ATT1	0x40013214	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX168_SL_ATT2	0x40013218	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX168_SL_ATT3	0x4001321C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX168_MS_ADDR	0x40013220	Master region, base address
PERI_MS_PPU_FX168_MS_SIZE	0x40013224	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX168_MS_ATT0	0x40013230	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX168_MS_ATT1	0x40013234	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX168_MS_ATT2	0x40013238	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX168_MS_ATT3	0x4001323C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX169_SL_ADDR	0x40013240	Slave region, base address
PERI_MS_PPU_FX169_SL_SIZE	0x40013244	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX169_SL_ATT0	0x40013250	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX169_SL_ATT1	0x40013254	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX169_SL_ATT2	0x40013258	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX169_SL_ATT3	0x4001325C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX169_MS_ADDR	0x40013260	Master region, base address
PERI_MS_PPU_FX169_MS_SIZE	0x40013264	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX169_MS_ATT0	0x40013270	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX169_MS_ATT1	0x40013274	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX169_MS_ATT2	0x40013278	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX169_MS_ATT3	0x4001327C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX170_SL_ADDR	0x40013280	Slave region, base address
PERI_MS_PPU_FX170_SL_SIZE	0x40013284	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX170_SL_ATT0	0x40013290	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX170_SL_ATT1	0x40013294	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX170_SL_ATT2	0x40013298	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX170_SL_ATT3	0x4001329C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX170_MS_ADDR	0x400132A0	Master region, base address
PERI_MS_PPU_FX170_MS_SIZE	0x400132A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX170_MS_ATT0	0x400132B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX170_MS_ATT1	0x400132B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX170_MS_ATT2	0x400132B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX170_MS_ATT3	0x400132BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX171_SL_ADDR	0x400132C0	Slave region, base address
PERI_MS_PPU_FX171_SL_SIZE	0x400132C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX171_SL_ATT0	0x400132D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX171_SL_ATT1	0x400132D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX171_SL_ATT2	0x400132D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX171_SL_ATT3	0x400132DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX171_MS_ADDR	0x400132E0	Master region, base address
PERI_MS_PPU_FX171_MS_SIZE	0x400132E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX171_MS_ATT0	0x400132F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX171_MS_ATT1	0x400132F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX171_MS_ATT2	0x400132F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX171_MS_ATT3	0x400132FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX172_SL_ADDR	0x40013300	Slave region, base address
PERI_MS_PPU_FX172_SL_SIZE	0x40013304	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX172_SL_ATT0	0x40013310	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX172_SL_ATT1	0x40013314	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX172_SL_ATT2	0x40013318	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX172_SL_ATT3	0x4001331C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX172_MS_ADDR	0x40013320	Master region, base address
PERI_MS_PPU_FX172_MS_SIZE	0x40013324	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX172_MS_ATT0	0x40013330	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX172_MS_ATT1	0x40013334	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX172_MS_ATT2	0x40013338	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX172_MS_ATT3	0x4001333C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX173_SL_ADDR	0x40013340	Slave region, base address
PERI_MS_PPU_FX173_SL_SIZE	0x40013344	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX173_SL_ATT0	0x40013350	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX173_SL_ATT1	0x40013354	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX173_SL_ATT2	0x40013358	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX173_SL_ATT3	0x4001335C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX173_MS_ADDR	0x40013360	Master region, base address
PERI_MS_PPU_FX173_MS_SIZE	0x40013364	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX173_MS_ATT0	0x40013370	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX173_MS_ATT1	0x40013374	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX173_MS_ATT2	0x40013378	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX173_MS_ATT3	0x4001337C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX174_SL_ADDR	0x40013380	Slave region, base address
PERI_MS_PPU_FX174_SL_SIZE	0x40013384	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX174_SL_ATT0	0x40013390	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX174_SL_ATT1	0x40013394	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX174_SL_ATT2	0x40013398	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX174_SL_ATT3	0x4001339C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX174_MS_ADDR	0x400133A0	Master region, base address
PERI_MS_PPU_FX174_MS_SIZE	0x400133A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX174_MS_ATT0	0x400133B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX174_MS_ATT1	0x400133B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX174_MS_ATT2	0x400133B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX174_MS_ATT3	0x400133BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX175_SL_ADDR	0x400133C0	Slave region, base address
PERI_MS_PPU_FX175_SL_SIZE	0x400133C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX175_SL_ATT0	0x400133D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX175_SL_ATT1	0x400133D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX175_SL_ATT2	0x400133D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX175_SL_ATT3	0x400133DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX175_MS_ADDR	0x400133E0	Master region, base address
PERI_MS_PPU_FX175_MS_SIZE	0x400133E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX175_MS_ATT0	0x400133F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX175_MS_ATT1	0x400133F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX175_MS_ATT2	0x400133F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX175_MS_ATT3	0x400133FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX176_SL_ADDR	0x40013400	Slave region, base address
PERI_MS_PPU_FX176_SL_SIZE	0x40013404	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX176_SL_ATT0	0x40013410	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX176_SL_ATT1	0x40013414	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX176_SL_ATT2	0x40013418	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX176_SL_ATT3	0x4001341C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX176_MS_ADDR	0x40013420	Master region, base address
PERI_MS_PPU_FX176_MS_SIZE	0x40013424	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX176_MS_ATT0	0x40013430	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX176_MS_ATT1	0x40013434	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX176_MS_ATT2	0x40013438	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX176_MS_ATT3	0x4001343C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX177_SL_ADDR	0x40013440	Slave region, base address
PERI_MS_PPU_FX177_SL_SIZE	0x40013444	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX177_SL_ATT0	0x40013450	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX177_SL_ATT1	0x40013454	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX177_SL_ATT2	0x40013458	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX177_SL_ATT3	0x4001345C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX177_MS_ADDR	0x40013460	Master region, base address
PERI_MS_PPU_FX177_MS_SIZE	0x40013464	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX177_MS_ATT0	0x40013470	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX177_MS_ATT1	0x40013474	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX177_MS_ATT2	0x40013478	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX177_MS_ATT3	0x4001347C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX178_SL_ADDR	0x40013480	Slave region, base address
PERI_MS_PPU_FX178_SL_SIZE	0x40013484	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX178_SL_ATT0	0x40013490	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX178_SL_ATT1	0x40013494	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX178_SL_ATT2	0x40013498	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX178_SL_ATT3	0x4001349C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX178_MS_ADDR	0x400134A0	Master region, base address
PERI_MS_PPU_FX178_MS_SIZE	0x400134A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX178_MS_ATT0	0x400134B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX178_MS_ATT1	0x400134B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX178_MS_ATT2	0x400134B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX178_MS_ATT3	0x400134BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX179_SL_ADDR	0x400134C0	Slave region, base address
PERI_MS_PPU_FX179_SL_SIZE	0x400134C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX179_SL_ATT0	0x400134D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX179_SL_ATT1	0x400134D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX179_SL_ATT2	0x400134D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX179_SL_ATT3	0x400134DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX179_MS_ADDR	0x400134E0	Master region, base address
PERI_MS_PPU_FX179_MS_SIZE	0x400134E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX179_MS_ATT0	0x400134F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX179_MS_ATT1	0x400134F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX179_MS_ATT2	0x400134F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX179_MS_ATT3	0x400134FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX180_SL_ADDR	0x40013500	Slave region, base address
PERI_MS_PPU_FX180_SL_SIZE	0x40013504	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX180_SL_ATT0	0x40013510	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX180_SL_ATT1	0x40013514	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX180_SL_ATT2	0x40013518	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX180_SL_ATT3	0x4001351C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX180_MS_ADDR	0x40013520	Master region, base address
PERI_MS_PPU_FX180_MS_SIZE	0x40013524	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX180_MS_ATT0	0x40013530	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX180_MS_ATT1	0x40013534	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX180_MS_ATT2	0x40013538	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX180_MS_ATT3	0x4001353C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX181_SL_ADDR	0x40013540	Slave region, base address
PERI_MS_PPU_FX181_SL_SIZE	0x40013544	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX181_SL_ATT0	0x40013550	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX181_SL_ATT1	0x40013554	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX181_SL_ATT2	0x40013558	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX181_SL_ATT3	0x4001355C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX181_MS_ADDR	0x40013560	Master region, base address
PERI_MS_PPU_FX181_MS_SIZE	0x40013564	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX181_MS_ATT0	0x40013570	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX181_MS_ATT1	0x40013574	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX181_MS_ATT2	0x40013578	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX181_MS_ATT3	0x4001357C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX182_SL_ADDR	0x40013580	Slave region, base address
PERI_MS_PPU_FX182_SL_SIZE	0x40013584	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX182_SL_ATT0	0x40013590	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX182_SL_ATT1	0x40013594	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX182_SL_ATT2	0x40013598	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX182_SL_ATT3	0x4001359C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX182_MS_ADDR	0x400135A0	Master region, base address
PERI_MS_PPU_FX182_MS_SIZE	0x400135A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX182_MS_ATT0	0x400135B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX182_MS_ATT1	0x400135B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX182_MS_ATT2	0x400135B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX182_MS_ATT3	0x400135BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX183_SL_ADDR	0x400135C0	Slave region, base address
PERI_MS_PPU_FX183_SL_SIZE	0x400135C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX183_SL_ATT0	0x400135D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX183_SL_ATT1	0x400135D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX183_SL_ATT2	0x400135D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX183_SL_ATT3	0x400135DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX183_MS_ADDR	0x400135E0	Master region, base address
PERI_MS_PPU_FX183_MS_SIZE	0x400135E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX183_MS_ATT0	0x400135F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX183_MS_ATT1	0x400135F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX183_MS_ATT2	0x400135F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX183_MS_ATT3	0x400135FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX184_SL_ADDR	0x40013600	Slave region, base address
PERI_MS_PPU_FX184_SL_SIZE	0x40013604	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX184_SL_ATT0	0x40013610	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX184_SL_ATT1	0x40013614	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX184_SL_ATT2	0x40013618	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX184_SL_ATT3	0x4001361C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX184_MS_ADDR	0x40013620	Master region, base address
PERI_MS_PPU_FX184_MS_SIZE	0x40013624	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX184_MS_ATT0	0x40013630	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX184_MS_ATT1	0x40013634	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX184_MS_ATT2	0x40013638	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX184_MS_ATT3	0x4001363C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX185_SL_ADDR	0x40013640	Slave region, base address
PERI_MS_PPU_FX185_SL_SIZE	0x40013644	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX185_SL_ATT0	0x40013650	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX185_SL_ATT1	0x40013654	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX185_SL_ATT2	0x40013658	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX185_SL_ATT3	0x4001365C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX185_MS_ADDR	0x40013660	Master region, base address
PERI_MS_PPU_FX185_MS_SIZE	0x40013664	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX185_MS_ATT0	0x40013670	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX185_MS_ATT1	0x40013674	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX185_MS_ATT2	0x40013678	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX185_MS_ATT3	0x4001367C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX186_SL_ADDR	0x40013680	Slave region, base address
PERI_MS_PPU_FX186_SL_SIZE	0x40013684	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX186_SL_ATT0	0x40013690	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX186_SL_ATT1	0x40013694	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX186_SL_ATT2	0x40013698	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX186_SL_ATT3	0x4001369C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX186_MS_ADDR	0x400136A0	Master region, base address
PERI_MS_PPU_FX186_MS_SIZE	0x400136A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX186_MS_ATT0	0x400136B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX186_MS_ATT1	0x400136B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX186_MS_ATT2	0x400136B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX186_MS_ATT3	0x400136BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX187_SL_ADDR	0x400136C0	Slave region, base address
PERI_MS_PPU_FX187_SL_SIZE	0x400136C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX187_SL_ATT0	0x400136D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX187_SL_ATT1	0x400136D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX187_SL_ATT2	0x400136D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX187_SL_ATT3	0x400136DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX187_MS_ADDR	0x400136E0	Master region, base address
PERI_MS_PPU_FX187_MS_SIZE	0x400136E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX187_MS_ATT0	0x400136F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX187_MS_ATT1	0x400136F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX187_MS_ATT2	0x400136F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX187_MS_ATT3	0x400136FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX188_SL_ADDR	0x40013700	Slave region, base address
PERI_MS_PPU_FX188_SL_SIZE	0x40013704	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX188_SL_ATT0	0x40013710	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX188_SL_ATT1	0x40013714	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX188_SL_ATT2	0x40013718	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX188_SL_ATT3	0x4001371C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX188_MS_ADDR	0x40013720	Master region, base address
PERI_MS_PPU_FX188_MS_SIZE	0x40013724	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX188_MS_ATT0	0x40013730	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX188_MS_ATT1	0x40013734	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX188_MS_ATT2	0x40013738	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX188_MS_ATT3	0x4001373C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX189_SL_ADDR	0x40013740	Slave region, base address
PERI_MS_PPU_FX189_SL_SIZE	0x40013744	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX189_SL_ATT0	0x40013750	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX189_SL_ATT1	0x40013754	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX189_SL_ATT2	0x40013758	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX189_SL_ATT3	0x4001375C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX189_MS_ADDR	0x40013760	Master region, base address
PERI_MS_PPU_FX189_MS_SIZE	0x40013764	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX189_MS_ATT0	0x40013770	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX189_MS_ATT1	0x40013774	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX189_MS_ATT2	0x40013778	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX189_MS_ATT3	0x4001377C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX190_SL_ADDR	0x40013780	Slave region, base address
PERI_MS_PPU_FX190_SL_SIZE	0x40013784	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX190_SL_ATT0	0x40013790	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX190_SL_ATT1	0x40013794	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX190_SL_ATT2	0x40013798	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX190_SL_ATT3	0x4001379C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX190_MS_ADDR	0x400137A0	Master region, base address
PERI_MS_PPU_FX190_MS_SIZE	0x400137A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX190_MS_ATT0	0x400137B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX190_MS_ATT1	0x400137B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX190_MS_ATT2	0x400137B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX190_MS_ATT3	0x400137BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX191_SL_ADDR	0x400137C0	Slave region, base address
PERI_MS_PPU_FX191_SL_SIZE	0x400137C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX191_SL_ATT0	0x400137D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX191_SL_ATT1	0x400137D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX191_SL_ATT2	0x400137D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX191_SL_ATT3	0x400137DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX191_MS_ADDR	0x400137E0	Master region, base address
PERI_MS_PPU_FX191_MS_SIZE	0x400137E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX191_MS_ATT0	0x400137F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX191_MS_ATT1	0x400137F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX191_MS_ATT2	0x400137F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX191_MS_ATT3	0x400137FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX192_SL_ADDR	0x40013800	Slave region, base address
PERI_MS_PPU_FX192_SL_SIZE	0x40013804	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX192_SL_ATT0	0x40013810	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX192_SL_ATT1	0x40013814	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX192_SL_ATT2	0x40013818	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX192_SL_ATT3	0x4001381C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX192_MS_ADDR	0x40013820	Master region, base address
PERI_MS_PPU_FX192_MS_SIZE	0x40013824	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX192_MS_ATT0	0x40013830	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX192_MS_ATT1	0x40013834	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX192_MS_ATT2	0x40013838	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX192_MS_ATT3	0x4001383C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX193_SL_ADDR	0x40013840	Slave region, base address
PERI_MS_PPU_FX193_SL_SIZE	0x40013844	Slave region, size. See PERI_MS_PPU_FX33_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX193_SL_ATT0	0x40013850	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX193_SL_ATT1	0x40013854	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX193_SL_ATT2	0x40013858	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX193_SL_ATT3	0x4001385C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX193_MS_ADDR	0x40013860	Master region, base address
PERI_MS_PPU_FX193_MS_SIZE	0x40013864	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX193_MS_ATT0	0x40013870	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX193_MS_ATT1	0x40013874	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX193_MS_ATT2	0x40013878	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX193_MS_ATT3	0x4001387C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX194_SL_ADDR	0x40013880	Slave region, base address
PERI_MS_PPU_FX194_SL_SIZE	0x40013884	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX194_SL_ATT0	0x40013890	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX194_SL_ATT1	0x40013894	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX194_SL_ATT2	0x40013898	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX194_SL_ATT3	0x4001389C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX194_MS_ADDR	0x400138A0	Master region, base address
PERI_MS_PPU_FX194_MS_SIZE	0x400138A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX194_MS_ATT0	0x400138B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX194_MS_ATT1	0x400138B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX194_MS_ATT2	0x400138B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX194_MS_ATT3	0x400138BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX195_SL_ADDR	0x400138C0	Slave region, base address
PERI_MS_PPU_FX195_SL_SIZE	0x400138C4	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX195_SL_ATT0	0x400138D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX195_SL_ATT1	0x400138D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX195_SL_ATT2	0x400138D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX195_SL_ATT3	0x400138DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX195_MS_ADDR	0x400138E0	Master region, base address
PERI_MS_PPU_FX195_MS_SIZE	0x400138E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX195_MS_ATT0	0x400138F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX195_MS_ATT1	0x400138F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX195_MS_ATT2	0x400138F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX195_MS_ATT3	0x400138FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX196_SL_ADDR	0x40013900	Slave region, base address
PERI_MS_PPU_FX196_SL_SIZE	0x40013904	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX196_SL_ATT0	0x40013910	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX196_SL_ATT1	0x40013914	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX196_SL_ATT2	0x40013918	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX196_SL_ATT3	0x4001391C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX196_MS_ADDR	0x40013920	Master region, base address
PERI_MS_PPU_FX196_MS_SIZE	0x40013924	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX196_MS_ATT0	0x40013930	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX196_MS_ATT1	0x40013934	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX196_MS_ATT2	0x40013938	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX196_MS_ATT3	0x4001393C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX197_SL_ADDR	0x40013940	Slave region, base address
PERI_MS_PPU_FX197_SL_SIZE	0x40013944	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX197_SL_ATT0	0x40013950	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX197_SL_ATT1	0x40013954	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX197_SL_ATT2	0x40013958	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX197_SL_ATT3	0x4001395C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX197_MS_ADDR	0x40013960	Master region, base address
PERI_MS_PPU_FX197_MS_SIZE	0x40013964	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX197_MS_ATT0	0x40013970	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX197_MS_ATT1	0x40013974	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX197_MS_ATT2	0x40013978	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX197_MS_ATT3	0x4001397C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX198_SL_ADDR	0x40013980	Slave region, base address
PERI_MS_PPU_FX198_SL_SIZE	0x40013984	Slave region, size. See PERI_MS_PPU_FX18_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX198_SL_ATT0	0x40013990	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX198_SL_ATT1	0x40013994	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX198_SL_ATT2	0x40013998	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX198_SL_ATT3	0x4001399C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX198_MS_ADDR	0x400139A0	Master region, base address
PERI_MS_PPU_FX198_MS_SIZE	0x400139A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX198_MS_ATT0	0x400139B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX198_MS_ATT1	0x400139B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX198_MS_ATT2	0x400139B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX198_MS_ATT3	0x400139BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX199_SL_ADDR	0x400139C0	Slave region, base address
PERI_MS_PPU_FX199_SL_SIZE	0x400139C4	Slave region, size. See PERI_MS_PPU_FX18_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX199_SL_ATT0	0x400139D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX199_SL_ATT1	0x400139D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX199_SL_ATT2	0x400139D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX199_SL_ATT3	0x400139DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX199_MS_ADDR	0x400139E0	Master region, base address
PERI_MS_PPU_FX199_MS_SIZE	0x400139E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX199_MS_ATT0	0x400139F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX199_MS_ATT1	0x400139F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX199_MS_ATT2	0x400139F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX199_MS_ATT3	0x400139FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX200_SL_ADDR	0x40013A00	Slave region, base address
PERI_MS_PPU_FX200_SL_SIZE	0x40013A04	Slave region, size. See PERI_MS_PPU_FX17_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX200_SL_ATT0	0x40013A10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX200_SL_ATT1	0x40013A14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX200_SL_ATT2	0x40013A18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX200_SL_ATT3	0x40013A1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX200_MS_ADDR	0x40013A20	Master region, base address
PERI_MS_PPU_FX200_MS_SIZE	0x40013A24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX200_MS_ATT0	0x40013A30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX200_MS_ATT1	0x40013A34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX200_MS_ATT2	0x40013A38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX200_MS_ATT3	0x40013A3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX201_SL_ADDR	0x40013A40	Slave region, base address
PERI_MS_PPU_FX201_SL_SIZE	0x40013A44	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX201_SL_ATT0	0x40013A50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX201_SL_ATT1	0x40013A54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX201_SL_ATT2	0x40013A58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX201_SL_ATT3	0x40013A5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX201_MS_ADDR	0x40013A60	Master region, base address
PERI_MS_PPU_FX201_MS_SIZE	0x40013A64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX201_MS_ATT0	0x40013A70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX201_MS_ATT1	0x40013A74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX201_MS_ATT2	0x40013A78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX201_MS_ATT3	0x40013A7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX202_SL_ADDR	0x40013A80	Slave region, base address
PERI_MS_PPU_FX202_SL_SIZE	0x40013A84	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX202_SL_ATT0	0x40013A90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX202_SL_ATT1	0x40013A94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX202_SL_ATT2	0x40013A98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX202_SL_ATT3	0x40013A9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX202_MS_ADDR	0x40013AA0	Master region, base address
PERI_MS_PPU_FX202_MS_SIZE	0x40013AA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX202_MS_ATT0	0x40013AB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX202_MS_ATT1	0x40013AB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX202_MS_ATT2	0x40013AB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX202_MS_ATT3	0x40013ABC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX203_SL_ADDR	0x40013AC0	Slave region, base address
PERI_MS_PPU_FX203_SL_SIZE	0x40013AC4	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX203_SL_ATT0	0x40013AD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX203_SL_ATT1	0x40013AD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX203_SL_ATT2	0x40013AD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX203_SL_ATT3	0x40013ADC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX203_MS_ADDR	0x40013AE0	Master region, base address
PERI_MS_PPU_FX203_MS_SIZE	0x40013AE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX203_MS_ATT0	0x40013AF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX203_MS_ATT1	0x40013AF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX203_MS_ATT2	0x40013AF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX203_MS_ATT3	0x40013AFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX204_SL_ADDR	0x40013B00	Slave region, base address
PERI_MS_PPU_FX204_SL_SIZE	0x40013B04	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX204_SL_ATT0	0x40013B10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX204_SL_ATT1	0x40013B14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX204_SL_ATT2	0x40013B18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX204_SL_ATT3	0x40013B1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX204_MS_ADDR	0x40013B20	Master region, base address
PERI_MS_PPU_FX204_MS_SIZE	0x40013B24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX204_MS_ATT0	0x40013B30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX204_MS_ATT1	0x40013B34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX204_MS_ATT2	0x40013B38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX204_MS_ATT3	0x40013B3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX205_SL_ADDR	0x40013B40	Slave region, base address
PERI_MS_PPU_FX205_SL_SIZE	0x40013B44	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX205_SL_ATT0	0x40013B50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX205_SL_ATT1	0x40013B54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX205_SL_ATT2	0x40013B58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX205_SL_ATT3	0x40013B5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX205_MS_ADDR	0x40013B60	Master region, base address
PERI_MS_PPU_FX205_MS_SIZE	0x40013B64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX205_MS_ATT0	0x40013B70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX205_MS_ATT1	0x40013B74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX205_MS_ATT2	0x40013B78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX205_MS_ATT3	0x40013B7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX206_SL_ADDR	0x40013B80	Slave region, base address
PERI_MS_PPU_FX206_SL_SIZE	0x40013B84	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX206_SL_ATT0	0x40013B90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX206_SL_ATT1	0x40013B94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX206_SL_ATT2	0x40013B98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX206_SL_ATT3	0x40013B9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX206_MS_ADDR	0x40013BA0	Master region, base address
PERI_MS_PPU_FX206_MS_SIZE	0x40013BA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX206_MS_ATT0	0x40013BB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX206_MS_ATT1	0x40013BB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX206_MS_ATT2	0x40013BB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX206_MS_ATT3	0x40013BBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX207_SL_ADDR	0x40013BC0	Slave region, base address
PERI_MS_PPU_FX207_SL_SIZE	0x40013BC4	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX207_SL_ATT0	0x40013BD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX207_SL_ATT1	0x40013BD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX207_SL_ATT2	0x40013BD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX207_SL_ATT3	0x40013BDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX207_MS_ADDR	0x40013BE0	Master region, base address
PERI_MS_PPU_FX207_MS_SIZE	0x40013BE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX207_MS_ATT0	0x40013BF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX207_MS_ATT1	0x40013BF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX207_MS_ATT2	0x40013BF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX207_MS_ATT3	0x40013BFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX208_SL_ADDR	0x40013C00	Slave region, base address
PERI_MS_PPU_FX208_SL_SIZE	0x40013C04	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX208_SL_ATT0	0x40013C10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX208_SL_ATT1	0x40013C14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX208_SL_ATT2	0x40013C18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX208_SL_ATT3	0x40013C1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX208_MS_ADDR	0x40013C20	Master region, base address
PERI_MS_PPU_FX208_MS_SIZE	0x40013C24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX208_MS_ATT0	0x40013C30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX208_MS_ATT1	0x40013C34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX208_MS_ATT2	0x40013C38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX208_MS_ATT3	0x40013C3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX209_SL_ADDR	0x40013C40	Slave region, base address
PERI_MS_PPU_FX209_SL_SIZE	0x40013C44	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX209_SL_ATT0	0x40013C50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX209_SL_ATT1	0x40013C54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX209_SL_ATT2	0x40013C58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX209_SL_ATT3	0x40013C5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX209_MS_ADDR	0x40013C60	Master region, base address
PERI_MS_PPU_FX209_MS_SIZE	0x40013C64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX209_MS_ATT0	0x40013C70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX209_MS_ATT1	0x40013C74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX209_MS_ATT2	0x40013C78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX209_MS_ATT3	0x40013C7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX210_SL_ADDR	0x40013C80	Slave region, base address
PERI_MS_PPU_FX210_SL_SIZE	0x40013C84	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX210_SL_ATT0	0x40013C90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX210_SL_ATT1	0x40013C94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX210_SL_ATT2	0x40013C98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX210_SL_ATT3	0x40013C9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX210_MS_ADDR	0x40013CA0	Master region, base address
PERI_MS_PPU_FX210_MS_SIZE	0x40013CA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX210_MS_ATT0	0x40013CB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX210_MS_ATT1	0x40013CB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX210_MS_ATT2	0x40013CB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX210_MS_ATT3	0x40013CBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX211_SL_ADDR	0x40013CC0	Slave region, base address
PERI_MS_PPU_FX211_SL_SIZE	0x40013CC4	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX211_SL_ATT0	0x40013CD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX211_SL_ATT1	0x40013CD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX211_SL_ATT2	0x40013CD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX211_SL_ATT3	0x40013CDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX211_MS_ADDR	0x40013CE0	Master region, base address
PERI_MS_PPU_FX211_MS_SIZE	0x40013CE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX211_MS_ATT0	0x40013CF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX211_MS_ATT1	0x40013CF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX211_MS_ATT2	0x40013CF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX211_MS_ATT3	0x40013CFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX212_SL_ADDR	0x40013D00	Slave region, base address
PERI_MS_PPU_FX212_SL_SIZE	0x40013D04	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX212_SL_ATT0	0x40013D10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX212_SL_ATT1	0x40013D14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX212_SL_ATT2	0x40013D18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX212_SL_ATT3	0x40013D1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX212_MS_ADDR	0x40013D20	Master region, base address
PERI_MS_PPU_FX212_MS_SIZE	0x40013D24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX212_MS_ATT0	0x40013D30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX212_MS_ATT1	0x40013D34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX212_MS_ATT2	0x40013D38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX212_MS_ATT3	0x40013D3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX213_SL_ADDR	0x40013D40	Slave region, base address
PERI_MS_PPU_FX213_SL_SIZE	0x40013D44	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX213_SL_ATT0	0x40013D50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX213_SL_ATT1	0x40013D54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX213_SL_ATT2	0x40013D58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX213_SL_ATT3	0x40013D5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX213_MS_ADDR	0x40013D60	Master region, base address
PERI_MS_PPU_FX213_MS_SIZE	0x40013D64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX213_MS_ATT0	0x40013D70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX213_MS_ATT1	0x40013D74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX213_MS_ATT2	0x40013D78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX213_MS_ATT3	0x40013D7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX214_SL_ADDR	0x40013D80	Slave region, base address
PERI_MS_PPU_FX214_SL_SIZE	0x40013D84	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX214_SL_ATT0	0x40013D90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX214_SL_ATT1	0x40013D94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX214_SL_ATT2	0x40013D98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX214_SL_ATT3	0x40013D9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX214_MS_ADDR	0x40013DA0	Master region, base address
PERI_MS_PPU_FX214_MS_SIZE	0x40013DA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX214_MS_ATT0	0x40013DB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX214_MS_ATT1	0x40013DB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX214_MS_ATT2	0x40013DB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX214_MS_ATT3	0x40013DBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX215_SL_ADDR	0x40013DC0	Slave region, base address
PERI_MS_PPU_FX215_SL_SIZE	0x40013DC4	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX215_SL_ATT0	0x40013DD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX215_SL_ATT1	0x40013DD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX215_SL_ATT2	0x40013DD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX215_SL_ATT3	0x40013DDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX215_MS_ADDR	0x40013DE0	Master region, base address
PERI_MS_PPU_FX215_MS_SIZE	0x40013DE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX215_MS_ATT0	0x40013DF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX215_MS_ATT1	0x40013DF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX215_MS_ATT2	0x40013DF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX215_MS_ATT3	0x40013DFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX216_SL_ADDR	0x40013E00	Slave region, base address
PERI_MS_PPU_FX216_SL_SIZE	0x40013E04	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX216_SL_ATT0	0x40013E10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX216_SL_ATT1	0x40013E14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX216_SL_ATT2	0x40013E18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX216_SL_ATT3	0x40013E1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX216_MS_ADDR	0x40013E20	Master region, base address
PERI_MS_PPU_FX216_MS_SIZE	0x40013E24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX216_MS_ATT0	0x40013E30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX216_MS_ATT1	0x40013E34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX216_MS_ATT2	0x40013E38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX216_MS_ATT3	0x40013E3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX217_SL_ADDR	0x40013E40	Slave region, base address
PERI_MS_PPU_FX217_SL_SIZE	0x40013E44	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX217_SL_ATT0	0x40013E50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX217_SL_ATT1	0x40013E54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX217_SL_ATT2	0x40013E58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX217_SL_ATT3	0x40013E5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX217_MS_ADDR	0x40013E60	Master region, base address
PERI_MS_PPU_FX217_MS_SIZE	0x40013E64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX217_MS_ATT0	0x40013E70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX217_MS_ATT1	0x40013E74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX217_MS_ATT2	0x40013E78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX217_MS_ATT3	0x40013E7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX218_SL_ADDR	0x40013E80	Slave region, base address
PERI_MS_PPU_FX218_SL_SIZE	0x40013E84	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX218_SL_ATT0	0x40013E90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX218_SL_ATT1	0x40013E94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX218_SL_ATT2	0x40013E98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX218_SL_ATT3	0x40013E9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX218_MS_ADDR	0x40013EA0	Master region, base address
PERI_MS_PPU_FX218_MS_SIZE	0x40013EA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX218_MS_ATT0	0x40013EB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX218_MS_ATT1	0x40013EB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX218_MS_ATT2	0x40013EB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX218_MS_ATT3	0x40013EBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX219_SL_ADDR	0x40013EC0	Slave region, base address
PERI_MS_PPU_FX219_SL_SIZE	0x40013EC4	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX219_SL_ATT0	0x40013ED0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX219_SL_ATT1	0x40013ED4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX219_SL_ATT2	0x40013ED8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX219_SL_ATT3	0x40013EDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX219_MS_ADDR	0x40013EE0	Master region, base address
PERI_MS_PPU_FX219_MS_SIZE	0x40013EE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX219_MS_ATT0	0x40013EF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX219_MS_ATT1	0x40013EF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX219_MS_ATT2	0x40013EF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX219_MS_ATT3	0x40013EFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX220_SL_ADDR	0x40013F00	Slave region, base address
PERI_MS_PPU_FX220_SL_SIZE	0x40013F04	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX220_SL_ATT0	0x40013F10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX220_SL_ATT1	0x40013F14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX220_SL_ATT2	0x40013F18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX220_SL_ATT3	0x40013F1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX220_MS_ADDR	0x40013F20	Master region, base address
PERI_MS_PPU_FX220_MS_SIZE	0x40013F24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX220_MS_ATT0	0x40013F30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX220_MS_ATT1	0x40013F34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX220_MS_ATT2	0x40013F38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX220_MS_ATT3	0x40013F3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX221_SL_ADDR	0x40013F40	Slave region, base address
PERI_MS_PPU_FX221_SL_SIZE	0x40013F44	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX221_SL_ATT0	0x40013F50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX221_SL_ATT1	0x40013F54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX221_SL_ATT2	0x40013F58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX221_SL_ATT3	0x40013F5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX221_MS_ADDR	0x40013F60	Master region, base address
PERI_MS_PPU_FX221_MS_SIZE	0x40013F64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX221_MS_ATT0	0x40013F70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX221_MS_ATT1	0x40013F74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX221_MS_ATT2	0x40013F78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX221_MS_ATT3	0x40013F7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX222_SL_ADDR	0x40013F80	Slave region, base address
PERI_MS_PPU_FX222_SL_SIZE	0x40013F84	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX222_SL_ATT0	0x40013F90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX222_SL_ATT1	0x40013F94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX222_SL_ATT2	0x40013F98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX222_SL_ATT3	0x40013F9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX222_MS_ADDR	0x40013FA0	Master region, base address
PERI_MS_PPU_FX222_MS_SIZE	0x40013FA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX222_MS_ATT0	0x40013FB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX222_MS_ATT1	0x40013FB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX222_MS_ATT2	0x40013FB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX222_MS_ATT3	0x40013FBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX223_SL_ADDR	0x40013FC0	Slave region, base address
PERI_MS_PPU_FX223_SL_SIZE	0x40013FC4	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX223_SL_ATT0	0x40013FD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX223_SL_ATT1	0x40013FD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX223_SL_ATT2	0x40013FD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX223_SL_ATT3	0x40013FDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX223_MS_ADDR	0x40013FE0	Master region, base address
PERI_MS_PPU_FX223_MS_SIZE	0x40013FE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX223_MS_ATT0	0x40013FF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX223_MS_ATT1	0x40013FF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX223_MS_ATT2	0x40013FF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX223_MS_ATT3	0x40013FFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX224_SL_ADDR	0x40014000	Slave region, base address
PERI_MS_PPU_FX224_SL_SIZE	0x40014004	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX224_SL_ATT0	0x40014010	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX224_SL_ATT1	0x40014014	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX224_SL_ATT2	0x40014018	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX224_SL_ATT3	0x4001401C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX224_MS_ADDR	0x40014020	Master region, base address
PERI_MS_PPU_FX224_MS_SIZE	0x40014024	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX224_MS_ATT0	0x40014030	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX224_MS_ATT1	0x40014034	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX224_MS_ATT2	0x40014038	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX224_MS_ATT3	0x4001403C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX225_SL_ADDR	0x40014040	Slave region, base address
PERI_MS_PPU_FX225_SL_SIZE	0x40014044	Slave region, size. See PERI_MS_PPU_FX33_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX225_SL_ATT0	0x40014050	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX225_SL_ATT1	0x40014054	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX225_SL_ATT2	0x40014058	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX225_SL_ATT3	0x4001405C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX225_MS_ADDR	0x40014060	Master region, base address
PERI_MS_PPU_FX225_MS_SIZE	0x40014064	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX225_MS_ATT0	0x40014070	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX225_MS_ATT1	0x40014074	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX225_MS_ATT2	0x40014078	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX225_MS_ATT3	0x4001407C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX226_SL_ADDR	0x40014080	Slave region, base address
PERI_MS_PPU_FX226_SL_SIZE	0x40014084	Slave region, size. See PERI_MS_PPU_FX33_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX226_SL_ATT0	0x40014090	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX226_SL_ATT1	0x40014094	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX226_SL_ATT2	0x40014098	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX226_SL_ATT3	0x4001409C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX226_MS_ADDR	0x400140A0	Master region, base address
PERI_MS_PPU_FX226_MS_SIZE	0x400140A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX226_MS_ATT0	0x400140B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX226_MS_ATT1	0x400140B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX226_MS_ATT2	0x400140B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX226_MS_ATT3	0x400140BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX227_SL_ADDR	0x400140C0	Slave region, base address
PERI_MS_PPU_FX227_SL_SIZE	0x400140C4	Slave region, size. See PERI_MS_PPU_FX1_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX227_SL_ATT0	0x400140D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX227_SL_ATT1	0x400140D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX227_SL_ATT2	0x400140D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX227_SL_ATT3	0x400140DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX227_MS_ADDR	0x400140E0	Master region, base address
PERI_MS_PPU_FX227_MS_SIZE	0x400140E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX227_MS_ATT0	0x400140F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX227_MS_ATT1	0x400140F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX227_MS_ATT2	0x400140F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX227_MS_ATT3	0x400140FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX228_SL_ADDR	0x40014100	Slave region, base address
PERI_MS_PPU_FX228_SL_SIZE	0x40014104	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX228_SL_ATT0	0x40014110	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX228_SL_ATT1	0x40014114	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX228_SL_ATT2	0x40014118	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX228_SL_ATT3	0x4001411C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX228_MS_ADDR	0x40014120	Master region, base address
PERI_MS_PPU_FX228_MS_SIZE	0x40014124	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX228_MS_ATT0	0x40014130	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX228_MS_ATT1	0x40014134	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX228_MS_ATT2	0x40014138	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX228_MS_ATT3	0x4001413C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX229_SL_ADDR	0x40014140	Slave region, base address
PERI_MS_PPU_FX229_SL_SIZE	0x40014144	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX229_SL_ATT0	0x40014150	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX229_SL_ATT1	0x40014154	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX229_SL_ATT2	0x40014158	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX229_SL_ATT3	0x4001415C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX229_MS_ADDR	0x40014160	Master region, base address
PERI_MS_PPU_FX229_MS_SIZE	0x40014164	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX229_MS_ATT0	0x40014170	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX229_MS_ATT1	0x40014174	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX229_MS_ATT2	0x40014178	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX229_MS_ATT3	0x4001417C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX230_SL_ADDR	0x40014180	Slave region, base address
PERI_MS_PPU_FX230_SL_SIZE	0x40014184	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX230_SL_ATT0	0x40014190	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX230_SL_ATT1	0x40014194	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX230_SL_ATT2	0x40014198	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX230_SL_ATT3	0x4001419C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX230_MS_ADDR	0x400141A0	Master region, base address
PERI_MS_PPU_FX230_MS_SIZE	0x400141A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX230_MS_ATT0	0x400141B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX230_MS_ATT1	0x400141B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX230_MS_ATT2	0x400141B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX230_MS_ATT3	0x400141BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX231_SL_ADDR	0x400141C0	Slave region, base address
PERI_MS_PPU_FX231_SL_SIZE	0x400141C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX231_SL_ATT0	0x400141D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX231_SL_ATT1	0x400141D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX231_SL_ATT2	0x400141D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX231_SL_ATT3	0x400141DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX231_MS_ADDR	0x400141E0	Master region, base address
PERI_MS_PPU_FX231_MS_SIZE	0x400141E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX231_MS_ATT0	0x400141F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX231_MS_ATT1	0x400141F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX231_MS_ATT2	0x400141F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX231_MS_ATT3	0x400141FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX232_SL_ADDR	0x40014200	Slave region, base address
PERI_MS_PPU_FX232_SL_SIZE	0x40014204	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX232_SL_ATT0	0x40014210	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX232_SL_ATT1	0x40014214	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX232_SL_ATT2	0x40014218	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX232_SL_ATT3	0x4001421C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX232_MS_ADDR	0x40014220	Master region, base address
PERI_MS_PPU_FX232_MS_SIZE	0x40014224	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX232_MS_ATT0	0x40014230	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX232_MS_ATT1	0x40014234	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX232_MS_ATT2	0x40014238	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX232_MS_ATT3	0x4001423C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX233_SL_ADDR	0x40014240	Slave region, base address
PERI_MS_PPU_FX233_SL_SIZE	0x40014244	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX233_SL_ATT0	0x40014250	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX233_SL_ATT1	0x40014254	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX233_SL_ATT2	0x40014258	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX233_SL_ATT3	0x4001425C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX233_MS_ADDR	0x40014260	Master region, base address
PERI_MS_PPU_FX233_MS_SIZE	0x40014264	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX233_MS_ATT0	0x40014270	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX233_MS_ATT1	0x40014274	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX233_MS_ATT2	0x40014278	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX233_MS_ATT3	0x4001427C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX234_SL_ADDR	0x40014280	Slave region, base address
PERI_MS_PPU_FX234_SL_SIZE	0x40014284	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX234_SL_ATT0	0x40014290	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX234_SL_ATT1	0x40014294	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX234_SL_ATT2	0x40014298	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX234_SL_ATT3	0x4001429C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX234_MS_ADDR	0x400142A0	Master region, base address
PERI_MS_PPU_FX234_MS_SIZE	0x400142A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX234_MS_ATT0	0x400142B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX234_MS_ATT1	0x400142B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX234_MS_ATT2	0x400142B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX234_MS_ATT3	0x400142BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX235_SL_ADDR	0x400142C0	Slave region, base address
PERI_MS_PPU_FX235_SL_SIZE	0x400142C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX235_SL_ATT0	0x400142D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX235_SL_ATT1	0x400142D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX235_SL_ATT2	0x400142D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX235_SL_ATT3	0x400142DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX235_MS_ADDR	0x400142E0	Master region, base address
PERI_MS_PPU_FX235_MS_SIZE	0x400142E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX235_MS_ATT0	0x400142F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX235_MS_ATT1	0x400142F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX235_MS_ATT2	0x400142F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX235_MS_ATT3	0x400142FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX236_SL_ADDR	0x40014300	Slave region, base address
PERI_MS_PPU_FX236_SL_SIZE	0x40014304	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX236_SL_ATT0	0x40014310	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX236_SL_ATT1	0x40014314	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX236_SL_ATT2	0x40014318	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX236_SL_ATT3	0x4001431C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX236_MS_ADDR	0x40014320	Master region, base address
PERI_MS_PPU_FX236_MS_SIZE	0x40014324	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX236_MS_ATT0	0x40014330	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX236_MS_ATT1	0x40014334	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX236_MS_ATT2	0x40014338	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX236_MS_ATT3	0x4001433C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX237_SL_ADDR	0x40014340	Slave region, base address
PERI_MS_PPU_FX237_SL_SIZE	0x40014344	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX237_SL_ATT0	0x40014350	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX237_SL_ATT1	0x40014354	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX237_SL_ATT2	0x40014358	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX237_SL_ATT3	0x4001435C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX237_MS_ADDR	0x40014360	Master region, base address
PERI_MS_PPU_FX237_MS_SIZE	0x40014364	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX237_MS_ATT0	0x40014370	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX237_MS_ATT1	0x40014374	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX237_MS_ATT2	0x40014378	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX237_MS_ATT3	0x4001437C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX238_SL_ADDR	0x40014380	Slave region, base address
PERI_MS_PPU_FX238_SL_SIZE	0x40014384	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX238_SL_ATT0	0x40014390	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX238_SL_ATT1	0x40014394	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX238_SL_ATT2	0x40014398	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX238_SL_ATT3	0x4001439C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX238_MS_ADDR	0x400143A0	Master region, base address
PERI_MS_PPU_FX238_MS_SIZE	0x400143A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX238_MS_ATT0	0x400143B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX238_MS_ATT1	0x400143B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX238_MS_ATT2	0x400143B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX238_MS_ATT3	0x400143BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX239_SL_ADDR	0x400143C0	Slave region, base address
PERI_MS_PPU_FX239_SL_SIZE	0x400143C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX239_SL_ATT0	0x400143D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX239_SL_ATT1	0x400143D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX239_SL_ATT2	0x400143D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX239_SL_ATT3	0x400143DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX239_MS_ADDR	0x400143E0	Master region, base address
PERI_MS_PPU_FX239_MS_SIZE	0x400143E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX239_MS_ATT0	0x400143F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX239_MS_ATT1	0x400143F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX239_MS_ATT2	0x400143F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX239_MS_ATT3	0x400143FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX240_SL_ADDR	0x40014400	Slave region, base address
PERI_MS_PPU_FX240_SL_SIZE	0x40014404	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX240_SL_ATT0	0x40014410	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX240_SL_ATT1	0x40014414	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX240_SL_ATT2	0x40014418	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX240_SL_ATT3	0x4001441C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX240_MS_ADDR	0x40014420	Master region, base address
PERI_MS_PPU_FX240_MS_SIZE	0x40014424	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX240_MS_ATT0	0x40014430	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX240_MS_ATT1	0x40014434	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX240_MS_ATT2	0x40014438	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX240_MS_ATT3	0x4001443C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX241_SL_ADDR	0x40014440	Slave region, base address
PERI_MS_PPU_FX241_SL_SIZE	0x40014444	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX241_SL_ATT0	0x40014450	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX241_SL_ATT1	0x40014454	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX241_SL_ATT2	0x40014458	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX241_SL_ATT3	0x4001445C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX241_MS_ADDR	0x40014460	Master region, base address
PERI_MS_PPU_FX241_MS_SIZE	0x40014464	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX241_MS_ATT0	0x40014470	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX241_MS_ATT1	0x40014474	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX241_MS_ATT2	0x40014478	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX241_MS_ATT3	0x4001447C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX242_SL_ADDR	0x40014480	Slave region, base address
PERI_MS_PPU_FX242_SL_SIZE	0x40014484	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX242_SL_ATT0	0x40014490	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX242_SL_ATT1	0x40014494	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX242_SL_ATT2	0x40014498	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX242_SL_ATT3	0x4001449C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX242_MS_ADDR	0x400144A0	Master region, base address
PERI_MS_PPU_FX242_MS_SIZE	0x400144A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX242_MS_ATT0	0x400144B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX242_MS_ATT1	0x400144B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX242_MS_ATT2	0x400144B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX242_MS_ATT3	0x400144BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX243_SL_ADDR	0x400144C0	Slave region, base address
PERI_MS_PPU_FX243_SL_SIZE	0x400144C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX243_SL_ATT0	0x400144D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX243_SL_ATT1	0x400144D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX243_SL_ATT2	0x400144D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX243_SL_ATT3	0x400144DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX243_MS_ADDR	0x400144E0	Master region, base address
PERI_MS_PPU_FX243_MS_SIZE	0x400144E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX243_MS_ATT0	0x400144F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX243_MS_ATT1	0x400144F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX243_MS_ATT2	0x400144F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX243_MS_ATT3	0x400144FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX244_SL_ADDR	0x40014500	Slave region, base address
PERI_MS_PPU_FX244_SL_SIZE	0x40014504	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX244_SL_ATT0	0x40014510	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX244_SL_ATT1	0x40014514	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX244_SL_ATT2	0x40014518	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX244_SL_ATT3	0x4001451C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX244_MS_ADDR	0x40014520	Master region, base address
PERI_MS_PPU_FX244_MS_SIZE	0x40014524	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX244_MS_ATT0	0x40014530	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX244_MS_ATT1	0x40014534	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX244_MS_ATT2	0x40014538	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX244_MS_ATT3	0x4001453C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX245_SL_ADDR	0x40014540	Slave region, base address
PERI_MS_PPU_FX245_SL_SIZE	0x40014544	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX245_SL_ATT0	0x40014550	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX245_SL_ATT1	0x40014554	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX245_SL_ATT2	0x40014558	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX245_SL_ATT3	0x4001455C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX245_MS_ADDR	0x40014560	Master region, base address
PERI_MS_PPU_FX245_MS_SIZE	0x40014564	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX245_MS_ATT0	0x40014570	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX245_MS_ATT1	0x40014574	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX245_MS_ATT2	0x40014578	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX245_MS_ATT3	0x4001457C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX246_SL_ADDR	0x40014580	Slave region, base address
PERI_MS_PPU_FX246_SL_SIZE	0x40014584	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX246_SL_ATT0	0x40014590	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX246_SL_ATT1	0x40014594	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX246_SL_ATT2	0x40014598	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX246_SL_ATT3	0x4001459C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX246_MS_ADDR	0x400145A0	Master region, base address
PERI_MS_PPU_FX246_MS_SIZE	0x400145A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX246_MS_ATT0	0x400145B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX246_MS_ATT1	0x400145B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX246_MS_ATT2	0x400145B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX246_MS_ATT3	0x400145BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX247_SL_ADDR	0x400145C0	Slave region, base address
PERI_MS_PPU_FX247_SL_SIZE	0x400145C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX247_SL_ATT0	0x400145D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX247_SL_ATT1	0x400145D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX247_SL_ATT2	0x400145D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX247_SL_ATT3	0x400145DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX247_MS_ADDR	0x400145E0	Master region, base address
PERI_MS_PPU_FX247_MS_SIZE	0x400145E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX247_MS_ATT0	0x400145F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX247_MS_ATT1	0x400145F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX247_MS_ATT2	0x400145F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX247_MS_ATT3	0x400145FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX248_SL_ADDR	0x40014600	Slave region, base address
PERI_MS_PPU_FX248_SL_SIZE	0x40014604	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX248_SL_ATT0	0x40014610	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX248_SL_ATT1	0x40014614	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX248_SL_ATT2	0x40014618	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX248_SL_ATT3	0x4001461C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX248_MS_ADDR	0x40014620	Master region, base address
PERI_MS_PPU_FX248_MS_SIZE	0x40014624	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX248_MS_ATT0	0x40014630	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX248_MS_ATT1	0x40014634	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX248_MS_ATT2	0x40014638	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX248_MS_ATT3	0x4001463C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX249_SL_ADDR	0x40014640	Slave region, base address
PERI_MS_PPU_FX249_SL_SIZE	0x40014644	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX249_SL_ATT0	0x40014650	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX249_SL_ATT1	0x40014654	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX249_SL_ATT2	0x40014658	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX249_SL_ATT3	0x4001465C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX249_MS_ADDR	0x40014660	Master region, base address
PERI_MS_PPU_FX249_MS_SIZE	0x40014664	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX249_MS_ATT0	0x40014670	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX249_MS_ATT1	0x40014674	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX249_MS_ATT2	0x40014678	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX249_MS_ATT3	0x4001467C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX250_SL_ADDR	0x40014680	Slave region, base address
PERI_MS_PPU_FX250_SL_SIZE	0x40014684	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX250_SL_ATT0	0x40014690	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX250_SL_ATT1	0x40014694	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX250_SL_ATT2	0x40014698	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX250_SL_ATT3	0x4001469C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX250_MS_ADDR	0x400146A0	Master region, base address
PERI_MS_PPU_FX250_MS_SIZE	0x400146A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX250_MS_ATT0	0x400146B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX250_MS_ATT1	0x400146B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX250_MS_ATT2	0x400146B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX250_MS_ATT3	0x400146BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX251_SL_ADDR	0x400146C0	Slave region, base address
PERI_MS_PPU_FX251_SL_SIZE	0x400146C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX251_SL_ATT0	0x400146D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX251_SL_ATT1	0x400146D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX251_SL_ATT2	0x400146D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX251_SL_ATT3	0x400146DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX251_MS_ADDR	0x400146E0	Master region, base address
PERI_MS_PPU_FX251_MS_SIZE	0x400146E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX251_MS_ATT0	0x400146F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX251_MS_ATT1	0x400146F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX251_MS_ATT2	0x400146F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX251_MS_ATT3	0x400146FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX252_SL_ADDR	0x40014700	Slave region, base address
PERI_MS_PPU_FX252_SL_SIZE	0x40014704	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX252_SL_ATT0	0x40014710	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX252_SL_ATT1	0x40014714	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX252_SL_ATT2	0x40014718	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX252_SL_ATT3	0x4001471C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX252_MS_ADDR	0x40014720	Master region, base address
PERI_MS_PPU_FX252_MS_SIZE	0x40014724	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX252_MS_ATT0	0x40014730	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX252_MS_ATT1	0x40014734	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX252_MS_ATT2	0x40014738	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX252_MS_ATT3	0x4001473C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX253_SL_ADDR	0x40014740	Slave region, base address
PERI_MS_PPU_FX253_SL_SIZE	0x40014744	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX253_SL_ATT0	0x40014750	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX253_SL_ATT1	0x40014754	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX253_SL_ATT2	0x40014758	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX253_SL_ATT3	0x4001475C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX253_MS_ADDR	0x40014760	Master region, base address
PERI_MS_PPU_FX253_MS_SIZE	0x40014764	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX253_MS_ATT0	0x40014770	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX253_MS_ATT1	0x40014774	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX253_MS_ATT2	0x40014778	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX253_MS_ATT3	0x4001477C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX254_SL_ADDR	0x40014780	Slave region, base address
PERI_MS_PPU_FX254_SL_SIZE	0x40014784	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX254_SL_ATT0	0x40014790	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX254_SL_ATT1	0x40014794	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX254_SL_ATT2	0x40014798	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX254_SL_ATT3	0x4001479C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX254_MS_ADDR	0x400147A0	Master region, base address
PERI_MS_PPU_FX254_MS_SIZE	0x400147A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX254_MS_ATT0	0x400147B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX254_MS_ATT1	0x400147B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX254_MS_ATT2	0x400147B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX254_MS_ATT3	0x400147BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX255_SL_ADDR	0x400147C0	Slave region, base address
PERI_MS_PPU_FX255_SL_SIZE	0x400147C4	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX255_SL_ATT0	0x400147D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX255_SL_ATT1	0x400147D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX255_SL_ATT2	0x400147D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX255_SL_ATT3	0x400147DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX255_MS_ADDR	0x400147E0	Master region, base address
PERI_MS_PPU_FX255_MS_SIZE	0x400147E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX255_MS_ATT0	0x400147F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX255_MS_ATT1	0x400147F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX255_MS_ATT2	0x400147F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX255_MS_ATT3	0x400147FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX256_SL_ADDR	0x40014800	Slave region, base address
PERI_MS_PPU_FX256_SL_SIZE	0x40014804	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX256_SL_ATT0	0x40014810	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX256_SL_ATT1	0x40014814	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX256_SL_ATT2	0x40014818	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX256_SL_ATT3	0x4001481C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX256_MS_ADDR	0x40014820	Master region, base address
PERI_MS_PPU_FX256_MS_SIZE	0x40014824	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX256_MS_ATT0	0x40014830	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX256_MS_ATT1	0x40014834	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX256_MS_ATT2	0x40014838	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX256_MS_ATT3	0x4001483C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX257_SL_ADDR	0x40014840	Slave region, base address
PERI_MS_PPU_FX257_SL_SIZE	0x40014844	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX257_SL_ATT0	0x40014850	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX257_SL_ATT1	0x40014854	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX257_SL_ATT2	0x40014858	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX257_SL_ATT3	0x4001485C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX257_MS_ADDR	0x40014860	Master region, base address
PERI_MS_PPU_FX257_MS_SIZE	0x40014864	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX257_MS_ATT0	0x40014870	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX257_MS_ATT1	0x40014874	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX257_MS_ATT2	0x40014878	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX257_MS_ATT3	0x4001487C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX258_SL_ADDR	0x40014880	Slave region, base address
PERI_MS_PPU_FX258_SL_SIZE	0x40014884	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX258_SL_ATT0	0x40014890	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX258_SL_ATT1	0x40014894	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX258_SL_ATT2	0x40014898	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX258_SL_ATT3	0x4001489C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX258_MS_ADDR	0x400148A0	Master region, base address
PERI_MS_PPU_FX258_MS_SIZE	0x400148A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX258_MS_ATT0	0x400148B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX258_MS_ATT1	0x400148B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX258_MS_ATT2	0x400148B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX258_MS_ATT3	0x400148BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX259_SL_ADDR	0x400148C0	Slave region, base address
PERI_MS_PPU_FX259_SL_SIZE	0x400148C4	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX259_SL_ATT0	0x400148D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX259_SL_ATT1	0x400148D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX259_SL_ATT2	0x400148D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX259_SL_ATT3	0x400148DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX259_MS_ADDR	0x400148E0	Master region, base address
PERI_MS_PPU_FX259_MS_SIZE	0x400148E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX259_MS_ATT0	0x400148F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX259_MS_ATT1	0x400148F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX259_MS_ATT2	0x400148F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX259_MS_ATT3	0x400148FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX260_SL_ADDR	0x40014900	Slave region, base address
PERI_MS_PPU_FX260_SL_SIZE	0x40014904	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX260_SL_ATT0	0x40014910	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX260_SL_ATT1	0x40014914	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX260_SL_ATT2	0x40014918	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX260_SL_ATT3	0x4001491C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX260_MS_ADDR	0x40014920	Master region, base address
PERI_MS_PPU_FX260_MS_SIZE	0x40014924	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX260_MS_ATT0	0x40014930	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX260_MS_ATT1	0x40014934	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX260_MS_ATT2	0x40014938	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX260_MS_ATT3	0x4001493C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX261_SL_ADDR	0x40014940	Slave region, base address
PERI_MS_PPU_FX261_SL_SIZE	0x40014944	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX261_SL_ATT0	0x40014950	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX261_SL_ATT1	0x40014954	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX261_SL_ATT2	0x40014958	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX261_SL_ATT3	0x4001495C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX261_MS_ADDR	0x40014960	Master region, base address
PERI_MS_PPU_FX261_MS_SIZE	0x40014964	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX261_MS_ATT0	0x40014970	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX261_MS_ATT1	0x40014974	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX261_MS_ATT2	0x40014978	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX261_MS_ATT3	0x4001497C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX262_SL_ADDR	0x40014980	Slave region, base address
PERI_MS_PPU_FX262_SL_SIZE	0x40014984	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX262_SL_ATT0	0x40014990	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX262_SL_ATT1	0x40014994	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX262_SL_ATT2	0x40014998	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX262_SL_ATT3	0x4001499C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX262_MS_ADDR	0x400149A0	Master region, base address
PERI_MS_PPU_FX262_MS_SIZE	0x400149A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX262_MS_ATT0	0x400149B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX262_MS_ATT1	0x400149B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX262_MS_ATT2	0x400149B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX262_MS_ATT3	0x400149BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX263_SL_ADDR	0x400149C0	Slave region, base address
PERI_MS_PPU_FX263_SL_SIZE	0x400149C4	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX263_SL_ATT0	0x400149D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX263_SL_ATT1	0x400149D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX263_SL_ATT2	0x400149D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX263_SL_ATT3	0x400149DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX263_MS_ADDR	0x400149E0	Master region, base address
PERI_MS_PPU_FX263_MS_SIZE	0x400149E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX263_MS_ATT0	0x400149F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX263_MS_ATT1	0x400149F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX263_MS_ATT2	0x400149F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX263_MS_ATT3	0x400149FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX264_SL_ADDR	0x40014A00	Slave region, base address
PERI_MS_PPU_FX264_SL_SIZE	0x40014A04	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX264_SL_ATT0	0x40014A10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX264_SL_ATT1	0x40014A14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX264_SL_ATT2	0x40014A18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX264_SL_ATT3	0x40014A1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX264_MS_ADDR	0x40014A20	Master region, base address
PERI_MS_PPU_FX264_MS_SIZE	0x40014A24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX264_MS_ATT0	0x40014A30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX264_MS_ATT1	0x40014A34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX264_MS_ATT2	0x40014A38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX264_MS_ATT3	0x40014A3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX265_SL_ADDR	0x40014A40	Slave region, base address
PERI_MS_PPU_FX265_SL_SIZE	0x40014A44	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX265_SL_ATT0	0x40014A50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX265_SL_ATT1	0x40014A54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX265_SL_ATT2	0x40014A58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX265_SL_ATT3	0x40014A5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX265_MS_ADDR	0x40014A60	Master region, base address
PERI_MS_PPU_FX265_MS_SIZE	0x40014A64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX265_MS_ATT0	0x40014A70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX265_MS_ATT1	0x40014A74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX265_MS_ATT2	0x40014A78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX265_MS_ATT3	0x40014A7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX266_SL_ADDR	0x40014A80	Slave region, base address
PERI_MS_PPU_FX266_SL_SIZE	0x40014A84	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX266_SL_ATT0	0x40014A90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX266_SL_ATT1	0x40014A94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX266_SL_ATT2	0x40014A98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX266_SL_ATT3	0x40014A9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX266_MS_ADDR	0x40014AA0	Master region, base address
PERI_MS_PPU_FX266_MS_SIZE	0x40014AA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX266_MS_ATT0	0x40014AB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX266_MS_ATT1	0x40014AB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX266_MS_ATT2	0x40014AB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX266_MS_ATT3	0x40014ABC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX267_SL_ADDR	0x40014AC0	Slave region, base address
PERI_MS_PPU_FX267_SL_SIZE	0x40014AC4	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX267_SL_ATT0	0x40014AD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX267_SL_ATT1	0x40014AD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX267_SL_ATT2	0x40014AD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX267_SL_ATT3	0x40014ADC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX267_MS_ADDR	0x40014AE0	Master region, base address
PERI_MS_PPU_FX267_MS_SIZE	0x40014AE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX267_MS_ATT0	0x40014AF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX267_MS_ATT1	0x40014AF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX267_MS_ATT2	0x40014AF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX267_MS_ATT3	0x40014AFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX268_SL_ADDR	0x40014B00	Slave region, base address
PERI_MS_PPU_FX268_SL_SIZE	0x40014B04	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX268_SL_ATT0	0x40014B10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX268_SL_ATT1	0x40014B14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX268_SL_ATT2	0x40014B18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX268_SL_ATT3	0x40014B1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX268_MS_ADDR	0x40014B20	Master region, base address
PERI_MS_PPU_FX268_MS_SIZE	0x40014B24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX268_MS_ATT0	0x40014B30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX268_MS_ATT1	0x40014B34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX268_MS_ATT2	0x40014B38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX268_MS_ATT3	0x40014B3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX269_SL_ADDR	0x40014B40	Slave region, base address
PERI_MS_PPU_FX269_SL_SIZE	0x40014B44	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX269_SL_ATT0	0x40014B50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX269_SL_ATT1	0x40014B54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX269_SL_ATT2	0x40014B58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX269_SL_ATT3	0x40014B5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX269_MS_ADDR	0x40014B60	Master region, base address
PERI_MS_PPU_FX269_MS_SIZE	0x40014B64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX269_MS_ATT0	0x40014B70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX269_MS_ATT1	0x40014B74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX269_MS_ATT2	0x40014B78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX269_MS_ATT3	0x40014B7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX270_SL_ADDR	0x40014B80	Slave region, base address
PERI_MS_PPU_FX270_SL_SIZE	0x40014B84	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX270_SL_ATT0	0x40014B90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX270_SL_ATT1	0x40014B94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX270_SL_ATT2	0x40014B98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX270_SL_ATT3	0x40014B9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX270_MS_ADDR	0x40014BA0	Master region, base address
PERI_MS_PPU_FX270_MS_SIZE	0x40014BA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX270_MS_ATT0	0x40014BB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX270_MS_ATT1	0x40014BB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX270_MS_ATT2	0x40014BB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX270_MS_ATT3	0x40014BBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX271_SL_ADDR	0x40014BC0	Slave region, base address
PERI_MS_PPU_FX271_SL_SIZE	0x40014BC4	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX271_SL_ATT0	0x40014BD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX271_SL_ATT1	0x40014BD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX271_SL_ATT2	0x40014BD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX271_SL_ATT3	0x40014BDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX271_MS_ADDR	0x40014BE0	Master region, base address
PERI_MS_PPU_FX271_MS_SIZE	0x40014BE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX271_MS_ATT0	0x40014BF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX271_MS_ATT1	0x40014BF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX271_MS_ATT2	0x40014BF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX271_MS_ATT3	0x40014BFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX272_SL_ADDR	0x40014C00	Slave region, base address
PERI_MS_PPU_FX272_SL_SIZE	0x40014C04	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX272_SL_ATT0	0x40014C10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX272_SL_ATT1	0x40014C14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX272_SL_ATT2	0x40014C18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX272_SL_ATT3	0x40014C1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX272_MS_ADDR	0x40014C20	Master region, base address
PERI_MS_PPU_FX272_MS_SIZE	0x40014C24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX272_MS_ATT0	0x40014C30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX272_MS_ATT1	0x40014C34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX272_MS_ATT2	0x40014C38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX272_MS_ATT3	0x40014C3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX273_SL_ADDR	0x40014C40	Slave region, base address
PERI_MS_PPU_FX273_SL_SIZE	0x40014C44	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX273_SL_ATT0	0x40014C50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX273_SL_ATT1	0x40014C54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX273_SL_ATT2	0x40014C58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX273_SL_ATT3	0x40014C5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX273_MS_ADDR	0x40014C60	Master region, base address
PERI_MS_PPU_FX273_MS_SIZE	0x40014C64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX273_MS_ATT0	0x40014C70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX273_MS_ATT1	0x40014C74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX273_MS_ATT2	0x40014C78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX273_MS_ATT3	0x40014C7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX274_SL_ADDR	0x40014C80	Slave region, base address
PERI_MS_PPU_FX274_SL_SIZE	0x40014C84	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX274_SL_ATT0	0x40014C90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX274_SL_ATT1	0x40014C94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX274_SL_ATT2	0x40014C98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX274_SL_ATT3	0x40014C9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX274_MS_ADDR	0x40014CA0	Master region, base address
PERI_MS_PPU_FX274_MS_SIZE	0x40014CA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX274_MS_ATT0	0x40014CB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX274_MS_ATT1	0x40014CB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX274_MS_ATT2	0x40014CB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX274_MS_ATT3	0x40014CBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX275_SL_ADDR	0x40014CC0	Slave region, base address
PERI_MS_PPU_FX275_SL_SIZE	0x40014CC4	Slave region, size. See PERI_MS_PPU_FX5_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX275_SL_ATT0	0x40014CD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX275_SL_ATT1	0x40014CD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX275_SL_ATT2	0x40014CD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX275_SL_ATT3	0x40014CDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX275_MS_ADDR	0x40014CE0	Master region, base address
PERI_MS_PPU_FX275_MS_SIZE	0x40014CE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX275_MS_ATT0	0x40014CF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX275_MS_ATT1	0x40014CF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX275_MS_ATT2	0x40014CF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX275_MS_ATT3	0x40014CFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX276_SL_ADDR	0x40014D00	Slave region, base address
PERI_MS_PPU_FX276_SL_SIZE	0x40014D04	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX276_SL_ATT0	0x40014D10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX276_SL_ATT1	0x40014D14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX276_SL_ATT2	0x40014D18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX276_SL_ATT3	0x40014D1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX276_MS_ADDR	0x40014D20	Master region, base address
PERI_MS_PPU_FX276_MS_SIZE	0x40014D24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX276_MS_ATT0	0x40014D30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX276_MS_ATT1	0x40014D34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX276_MS_ATT2	0x40014D38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX276_MS_ATT3	0x40014D3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX277_SL_ADDR	0x40014D40	Slave region, base address
PERI_MS_PPU_FX277_SL_SIZE	0x40014D44	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX277_SL_ATT0	0x40014D50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX277_SL_ATT1	0x40014D54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX277_SL_ATT2	0x40014D58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX277_SL_ATT3	0x40014D5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX277_MS_ADDR	0x40014D60	Master region, base address
PERI_MS_PPU_FX277_MS_SIZE	0x40014D64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX277_MS_ATT0	0x40014D70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX277_MS_ATT1	0x40014D74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX277_MS_ATT2	0x40014D78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX277_MS_ATT3	0x40014D7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX278_SL_ADDR	0x40014D80	Slave region, base address
PERI_MS_PPU_FX278_SL_SIZE	0x40014D84	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX278_SL_ATT0	0x40014D90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX278_SL_ATT1	0x40014D94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX278_SL_ATT2	0x40014D98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX278_SL_ATT3	0x40014D9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX278_MS_ADDR	0x40014DA0	Master region, base address
PERI_MS_PPU_FX278_MS_SIZE	0x40014DA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX278_MS_ATT0	0x40014DB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX278_MS_ATT1	0x40014DB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX278_MS_ATT2	0x40014DB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX278_MS_ATT3	0x40014DBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX279_SL_ADDR	0x40014DC0	Slave region, base address
PERI_MS_PPU_FX279_SL_SIZE	0x40014DC4	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX279_SL_ATT0	0x40014DD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX279_SL_ATT1	0x40014DD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX279_SL_ATT2	0x40014DD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX279_SL_ATT3	0x40014DDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX279_MS_ADDR	0x40014DE0	Master region, base address
PERI_MS_PPU_FX279_MS_SIZE	0x40014DE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX279_MS_ATT0	0x40014DF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX279_MS_ATT1	0x40014DF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX279_MS_ATT2	0x40014DF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX279_MS_ATT3	0x40014DFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX280_SL_ADDR	0x40014E00	Slave region, base address
PERI_MS_PPU_FX280_SL_SIZE	0x40014E04	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX280_SL_ATT0	0x40014E10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX280_SL_ATT1	0x40014E14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX280_SL_ATT2	0x40014E18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX280_SL_ATT3	0x40014E1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX280_MS_ADDR	0x40014E20	Master region, base address
PERI_MS_PPU_FX280_MS_SIZE	0x40014E24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX280_MS_ATT0	0x40014E30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX280_MS_ATT1	0x40014E34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX280_MS_ATT2	0x40014E38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX280_MS_ATT3	0x40014E3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX281_SL_ADDR	0x40014E40	Slave region, base address
PERI_MS_PPU_FX281_SL_SIZE	0x40014E44	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX281_SL_ATT0	0x40014E50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX281_SL_ATT1	0x40014E54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX281_SL_ATT2	0x40014E58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX281_SL_ATT3	0x40014E5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX281_MS_ADDR	0x40014E60	Master region, base address
PERI_MS_PPU_FX281_MS_SIZE	0x40014E64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX281_MS_ATT0	0x40014E70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX281_MS_ATT1	0x40014E74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX281_MS_ATT2	0x40014E78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX281_MS_ATT3	0x40014E7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX282_SL_ADDR	0x40014E80	Slave region, base address
PERI_MS_PPU_FX282_SL_SIZE	0x40014E84	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX282_SL_ATT0	0x40014E90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX282_SL_ATT1	0x40014E94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX282_SL_ATT2	0x40014E98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX282_SL_ATT3	0x40014E9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX282_MS_ADDR	0x40014EA0	Master region, base address
PERI_MS_PPU_FX282_MS_SIZE	0x40014EA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX282_MS_ATT0	0x40014EB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX282_MS_ATT1	0x40014EB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX282_MS_ATT2	0x40014EB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX282_MS_ATT3	0x40014EBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX283_SL_ADDR	0x40014EC0	Slave region, base address
PERI_MS_PPU_FX283_SL_SIZE	0x40014EC4	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX283_SL_ATT0	0x40014ED0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX283_SL_ATT1	0x40014ED4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX283_SL_ATT2	0x40014ED8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX283_SL_ATT3	0x40014EDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX283_MS_ADDR	0x40014EE0	Master region, base address
PERI_MS_PPU_FX283_MS_SIZE	0x40014EE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX283_MS_ATT0	0x40014EF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX283_MS_ATT1	0x40014EF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX283_MS_ATT2	0x40014EF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX283_MS_ATT3	0x40014EFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX284_SL_ADDR	0x40014F00	Slave region, base address
PERI_MS_PPU_FX284_SL_SIZE	0x40014F04	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX284_SL_ATT0	0x40014F10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX284_SL_ATT1	0x40014F14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX284_SL_ATT2	0x40014F18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX284_SL_ATT3	0x40014F1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX284_MS_ADDR	0x40014F20	Master region, base address
PERI_MS_PPU_FX284_MS_SIZE	0x40014F24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX284_MS_ATT0	0x40014F30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX284_MS_ATT1	0x40014F34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX284_MS_ATT2	0x40014F38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX284_MS_ATT3	0x40014F3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX285_SL_ADDR	0x40014F40	Slave region, base address
PERI_MS_PPU_FX285_SL_SIZE	0x40014F44	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX285_SL_ATT0	0x40014F50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX285_SL_ATT1	0x40014F54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX285_SL_ATT2	0x40014F58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX285_SL_ATT3	0x40014F5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX285_MS_ADDR	0x40014F60	Master region, base address
PERI_MS_PPU_FX285_MS_SIZE	0x40014F64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX285_MS_ATT0	0x40014F70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX285_MS_ATT1	0x40014F74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX285_MS_ATT2	0x40014F78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX285_MS_ATT3	0x40014F7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX286_SL_ADDR	0x40014F80	Slave region, base address
PERI_MS_PPU_FX286_SL_SIZE	0x40014F84	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX286_SL_ATT0	0x40014F90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX286_SL_ATT1	0x40014F94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX286_SL_ATT2	0x40014F98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX286_SL_ATT3	0x40014F9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX286_MS_ADDR	0x40014FA0	Master region, base address
PERI_MS_PPU_FX286_MS_SIZE	0x40014FA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX286_MS_ATT0	0x40014FB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX286_MS_ATT1	0x40014FB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX286_MS_ATT2	0x40014FB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX286_MS_ATT3	0x40014FBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX287_SL_ADDR	0x40014FC0	Slave region, base address
PERI_MS_PPU_FX287_SL_SIZE	0x40014FC4	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX287_SL_ATT0	0x40014FD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX287_SL_ATT1	0x40014FD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX287_SL_ATT2	0x40014FD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX287_SL_ATT3	0x40014FDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX287_MS_ADDR	0x40014FE0	Master region, base address
PERI_MS_PPU_FX287_MS_SIZE	0x40014FE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX287_MS_ATT0	0x40014FF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX287_MS_ATT1	0x40014FF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX287_MS_ATT2	0x40014FF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX287_MS_ATT3	0x40014FFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX288_SL_ADDR	0x40015000	Slave region, base address
PERI_MS_PPU_FX288_SL_SIZE	0x40015004	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX288_SL_ATT0	0x40015010	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX288_SL_ATT1	0x40015014	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX288_SL_ATT2	0x40015018	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX288_SL_ATT3	0x4001501C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX288_MS_ADDR	0x40015020	Master region, base address
PERI_MS_PPU_FX288_MS_SIZE	0x40015024	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX288_MS_ATT0	0x40015030	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX288_MS_ATT1	0x40015034	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX288_MS_ATT2	0x40015038	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX288_MS_ATT3	0x4001503C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX289_SL_ADDR	0x40015040	Slave region, base address
PERI_MS_PPU_FX289_SL_SIZE	0x40015044	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX289_SL_ATT0	0x40015050	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX289_SL_ATT1	0x40015054	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX289_SL_ATT2	0x40015058	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX289_SL_ATT3	0x4001505C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX289_MS_ADDR	0x40015060	Master region, base address
PERI_MS_PPU_FX289_MS_SIZE	0x40015064	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX289_MS_ATT0	0x40015070	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX289_MS_ATT1	0x40015074	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX289_MS_ATT2	0x40015078	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX289_MS_ATT3	0x4001507C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX290_SL_ADDR	0x40015080	Slave region, base address
PERI_MS_PPU_FX290_SL_SIZE	0x40015084	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX290_SL_ATT0	0x40015090	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX290_SL_ATT1	0x40015094	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX290_SL_ATT2	0x40015098	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX290_SL_ATT3	0x4001509C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX290_MS_ADDR	0x400150A0	Master region, base address
PERI_MS_PPU_FX290_MS_SIZE	0x400150A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX290_MS_ATT0	0x400150B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX290_MS_ATT1	0x400150B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX290_MS_ATT2	0x400150B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX290_MS_ATT3	0x400150BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX291_SL_ADDR	0x400150C0	Slave region, base address
PERI_MS_PPU_FX291_SL_SIZE	0x400150C4	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX291_SL_ATT0	0x400150D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX291_SL_ATT1	0x400150D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX291_SL_ATT2	0x400150D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX291_SL_ATT3	0x400150DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX291_MS_ADDR	0x400150E0	Master region, base address
PERI_MS_PPU_FX291_MS_SIZE	0x400150E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX291_MS_ATT0	0x400150F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX291_MS_ATT1	0x400150F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX291_MS_ATT2	0x400150F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX291_MS_ATT3	0x400150FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX292_SL_ADDR	0x40015100	Slave region, base address
PERI_MS_PPU_FX292_SL_SIZE	0x40015104	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX292_SL_ATT0	0x40015110	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX292_SL_ATT1	0x40015114	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX292_SL_ATT2	0x40015118	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX292_SL_ATT3	0x4001511C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX292_MS_ADDR	0x40015120	Master region, base address
PERI_MS_PPU_FX292_MS_SIZE	0x40015124	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX292_MS_ATT0	0x40015130	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX292_MS_ATT1	0x40015134	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX292_MS_ATT2	0x40015138	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX292_MS_ATT3	0x4001513C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX293_SL_ADDR	0x40015140	Slave region, base address
PERI_MS_PPU_FX293_SL_SIZE	0x40015144	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX293_SL_ATT0	0x40015150	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX293_SL_ATT1	0x40015154	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX293_SL_ATT2	0x40015158	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX293_SL_ATT3	0x4001515C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX293_MS_ADDR	0x40015160	Master region, base address
PERI_MS_PPU_FX293_MS_SIZE	0x40015164	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX293_MS_ATT0	0x40015170	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX293_MS_ATT1	0x40015174	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX293_MS_ATT2	0x40015178	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX293_MS_ATT3	0x4001517C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX294_SL_ADDR	0x40015180	Slave region, base address
PERI_MS_PPU_FX294_SL_SIZE	0x40015184	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX294_SL_ATT0	0x40015190	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX294_SL_ATT1	0x40015194	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX294_SL_ATT2	0x40015198	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX294_SL_ATT3	0x4001519C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX294_MS_ADDR	0x400151A0	Master region, base address
PERI_MS_PPU_FX294_MS_SIZE	0x400151A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX294_MS_ATT0	0x400151B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX294_MS_ATT1	0x400151B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX294_MS_ATT2	0x400151B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX294_MS_ATT3	0x400151BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX295_SL_ADDR	0x400151C0	Slave region, base address
PERI_MS_PPU_FX295_SL_SIZE	0x400151C4	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX295_SL_ATT0	0x400151D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX295_SL_ATT1	0x400151D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX295_SL_ATT2	0x400151D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX295_SL_ATT3	0x400151DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX295_MS_ADDR	0x400151E0	Master region, base address
PERI_MS_PPU_FX295_MS_SIZE	0x400151E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX295_MS_ATT0	0x400151F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX295_MS_ATT1	0x400151F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX295_MS_ATT2	0x400151F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX295_MS_ATT3	0x400151FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX296_SL_ADDR	0x40015200	Slave region, base address
PERI_MS_PPU_FX296_SL_SIZE	0x40015204	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX296_SL_ATT0	0x40015210	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX296_SL_ATT1	0x40015214	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX296_SL_ATT2	0x40015218	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX296_SL_ATT3	0x4001521C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX296_MS_ADDR	0x40015220	Master region, base address
PERI_MS_PPU_FX296_MS_SIZE	0x40015224	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX296_MS_ATT0	0x40015230	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX296_MS_ATT1	0x40015234	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX296_MS_ATT2	0x40015238	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX296_MS_ATT3	0x4001523C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX297_SL_ADDR	0x40015240	Slave region, base address
PERI_MS_PPU_FX297_SL_SIZE	0x40015244	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX297_SL_ATT0	0x40015250	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX297_SL_ATT1	0x40015254	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX297_SL_ATT2	0x40015258	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX297_SL_ATT3	0x4001525C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX297_MS_ADDR	0x40015260	Master region, base address
PERI_MS_PPU_FX297_MS_SIZE	0x40015264	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX297_MS_ATT0	0x40015270	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX297_MS_ATT1	0x40015274	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX297_MS_ATT2	0x40015278	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX297_MS_ATT3	0x4001527C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX298_SL_ADDR	0x40015280	Slave region, base address
PERI_MS_PPU_FX298_SL_SIZE	0x40015284	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX298_SL_ATT0	0x40015290	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX298_SL_ATT1	0x40015294	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX298_SL_ATT2	0x40015298	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX298_SL_ATT3	0x4001529C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX298_MS_ADDR	0x400152A0	Master region, base address
PERI_MS_PPU_FX298_MS_SIZE	0x400152A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX298_MS_ATT0	0x400152B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX298_MS_ATT1	0x400152B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX298_MS_ATT2	0x400152B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX298_MS_ATT3	0x400152BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX299_SL_ADDR	0x400152C0	Slave region, base address
PERI_MS_PPU_FX299_SL_SIZE	0x400152C4	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX299_SL_ATT0	0x400152D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX299_SL_ATT1	0x400152D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX299_SL_ATT2	0x400152D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX299_SL_ATT3	0x400152DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX299_MS_ADDR	0x400152E0	Master region, base address
PERI_MS_PPU_FX299_MS_SIZE	0x400152E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX299_MS_ATT0	0x400152F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX299_MS_ATT1	0x400152F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX299_MS_ATT2	0x400152F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX299_MS_ATT3	0x400152FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX300_SL_ADDR	0x40015300	Slave region, base address
PERI_MS_PPU_FX300_SL_SIZE	0x40015304	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX300_SL_ATT0	0x40015310	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX300_SL_ATT1	0x40015314	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX300_SL_ATT2	0x40015318	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX300_SL_ATT3	0x4001531C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX300_MS_ADDR	0x40015320	Master region, base address
PERI_MS_PPU_FX300_MS_SIZE	0x40015324	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX300_MS_ATT0	0x40015330	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX300_MS_ATT1	0x40015334	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX300_MS_ATT2	0x40015338	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX300_MS_ATT3	0x4001533C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX301_SL_ADDR	0x40015340	Slave region, base address
PERI_MS_PPU_FX301_SL_SIZE	0x40015344	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX301_SL_ATT0	0x40015350	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX301_SL_ATT1	0x40015354	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX301_SL_ATT2	0x40015358	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX301_SL_ATT3	0x4001535C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX301_MS_ADDR	0x40015360	Master region, base address
PERI_MS_PPU_FX301_MS_SIZE	0x40015364	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX301_MS_ATT0	0x40015370	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX301_MS_ATT1	0x40015374	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX301_MS_ATT2	0x40015378	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX301_MS_ATT3	0x4001537C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX302_SL_ADDR	0x40015380	Slave region, base address
PERI_MS_PPU_FX302_SL_SIZE	0x40015384	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX302_SL_ATT0	0x40015390	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX302_SL_ATT1	0x40015394	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX302_SL_ATT2	0x40015398	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX302_SL_ATT3	0x4001539C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX302_MS_ADDR	0x400153A0	Master region, base address
PERI_MS_PPU_FX302_MS_SIZE	0x400153A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX302_MS_ATT0	0x400153B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX302_MS_ATT1	0x400153B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX302_MS_ATT2	0x400153B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX302_MS_ATT3	0x400153BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX303_SL_ADDR	0x400153C0	Slave region, base address
PERI_MS_PPU_FX303_SL_SIZE	0x400153C4	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX303_SL_ATT0	0x400153D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX303_SL_ATT1	0x400153D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX303_SL_ATT2	0x400153D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX303_SL_ATT3	0x400153DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX303_MS_ADDR	0x400153E0	Master region, base address
PERI_MS_PPU_FX303_MS_SIZE	0x400153E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX303_MS_ATT0	0x400153F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX303_MS_ATT1	0x400153F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX303_MS_ATT2	0x400153F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX303_MS_ATT3	0x400153FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX304_SL_ADDR	0x40015400	Slave region, base address
PERI_MS_PPU_FX304_SL_SIZE	0x40015404	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX304_SL_ATT0	0x40015410	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX304_SL_ATT1	0x40015414	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX304_SL_ATT2	0x40015418	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX304_SL_ATT3	0x4001541C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX304_MS_ADDR	0x40015420	Master region, base address
PERI_MS_PPU_FX304_MS_SIZE	0x40015424	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX304_MS_ATT0	0x40015430	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX304_MS_ATT1	0x40015434	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX304_MS_ATT2	0x40015438	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX304_MS_ATT3	0x4001543C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX305_SL_ADDR	0x40015440	Slave region, base address
PERI_MS_PPU_FX305_SL_SIZE	0x40015444	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX305_SL_ATT0	0x40015450	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX305_SL_ATT1	0x40015454	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX305_SL_ATT2	0x40015458	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX305_SL_ATT3	0x4001545C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX305_MS_ADDR	0x40015460	Master region, base address
PERI_MS_PPU_FX305_MS_SIZE	0x40015464	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX305_MS_ATT0	0x40015470	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX305_MS_ATT1	0x40015474	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX305_MS_ATT2	0x40015478	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX305_MS_ATT3	0x4001547C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX306_SL_ADDR	0x40015480	Slave region, base address
PERI_MS_PPU_FX306_SL_SIZE	0x40015484	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX306_SL_ATT0	0x40015490	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX306_SL_ATT1	0x40015494	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX306_SL_ATT2	0x40015498	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX306_SL_ATT3	0x4001549C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX306_MS_ADDR	0x400154A0	Master region, base address
PERI_MS_PPU_FX306_MS_SIZE	0x400154A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX306_MS_ATT0	0x400154B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX306_MS_ATT1	0x400154B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX306_MS_ATT2	0x400154B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX306_MS_ATT3	0x400154BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX307_SL_ADDR	0x400154C0	Slave region, base address
PERI_MS_PPU_FX307_SL_SIZE	0x400154C4	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX307_SL_ATT0	0x400154D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX307_SL_ATT1	0x400154D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX307_SL_ATT2	0x400154D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX307_SL_ATT3	0x400154DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX307_MS_ADDR	0x400154E0	Master region, base address
PERI_MS_PPU_FX307_MS_SIZE	0x400154E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX307_MS_ATT0	0x400154F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX307_MS_ATT1	0x400154F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX307_MS_ATT2	0x400154F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX307_MS_ATT3	0x400154FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX308_SL_ADDR	0x40015500	Slave region, base address
PERI_MS_PPU_FX308_SL_SIZE	0x40015504	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX308_SL_ATT0	0x40015510	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX308_SL_ATT1	0x40015514	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX308_SL_ATT2	0x40015518	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX308_SL_ATT3	0x4001551C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX308_MS_ADDR	0x40015520	Master region, base address
PERI_MS_PPU_FX308_MS_SIZE	0x40015524	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX308_MS_ATT0	0x40015530	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX308_MS_ATT1	0x40015534	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX308_MS_ATT2	0x40015538	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX308_MS_ATT3	0x4001553C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX309_SL_ADDR	0x40015540	Slave region, base address
PERI_MS_PPU_FX309_SL_SIZE	0x40015544	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX309_SL_ATT0	0x40015550	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX309_SL_ATT1	0x40015554	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX309_SL_ATT2	0x40015558	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX309_SL_ATT3	0x4001555C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX309_MS_ADDR	0x40015560	Master region, base address
PERI_MS_PPU_FX309_MS_SIZE	0x40015564	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX309_MS_ATT0	0x40015570	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX309_MS_ATT1	0x40015574	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX309_MS_ATT2	0x40015578	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX309_MS_ATT3	0x4001557C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX310_SL_ADDR	0x40015580	Slave region, base address
PERI_MS_PPU_FX310_SL_SIZE	0x40015584	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX310_SL_ATT0	0x40015590	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX310_SL_ATT1	0x40015594	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX310_SL_ATT2	0x40015598	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX310_SL_ATT3	0x4001559C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX310_MS_ADDR	0x400155A0	Master region, base address
PERI_MS_PPU_FX310_MS_SIZE	0x400155A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX310_MS_ATT0	0x400155B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX310_MS_ATT1	0x400155B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX310_MS_ATT2	0x400155B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX310_MS_ATT3	0x400155BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX311_SL_ADDR	0x400155C0	Slave region, base address
PERI_MS_PPU_FX311_SL_SIZE	0x400155C4	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX311_SL_ATT0	0x400155D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX311_SL_ATT1	0x400155D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX311_SL_ATT2	0x400155D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX311_SL_ATT3	0x400155DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX311_MS_ADDR	0x400155E0	Master region, base address
PERI_MS_PPU_FX311_MS_SIZE	0x400155E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX311_MS_ATT0	0x400155F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX311_MS_ATT1	0x400155F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX311_MS_ATT2	0x400155F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX311_MS_ATT3	0x400155FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX312_SL_ADDR	0x40015600	Slave region, base address
PERI_MS_PPU_FX312_SL_SIZE	0x40015604	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX312_SL_ATT0	0x40015610	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX312_SL_ATT1	0x40015614	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX312_SL_ATT2	0x40015618	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX312_SL_ATT3	0x4001561C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX312_MS_ADDR	0x40015620	Master region, base address
PERI_MS_PPU_FX312_MS_SIZE	0x40015624	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX312_MS_ATT0	0x40015630	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX312_MS_ATT1	0x40015634	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX312_MS_ATT2	0x40015638	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX312_MS_ATT3	0x4001563C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX313_SL_ADDR	0x40015640	Slave region, base address
PERI_MS_PPU_FX313_SL_SIZE	0x40015644	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX313_SL_ATT0	0x40015650	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX313_SL_ATT1	0x40015654	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX313_SL_ATT2	0x40015658	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX313_SL_ATT3	0x4001565C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX313_MS_ADDR	0x40015660	Master region, base address
PERI_MS_PPU_FX313_MS_SIZE	0x40015664	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX313_MS_ATT0	0x40015670	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX313_MS_ATT1	0x40015674	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX313_MS_ATT2	0x40015678	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX313_MS_ATT3	0x4001567C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX314_SL_ADDR	0x40015680	Slave region, base address
PERI_MS_PPU_FX314_SL_SIZE	0x40015684	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX314_SL_ATT0	0x40015690	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX314_SL_ATT1	0x40015694	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX314_SL_ATT2	0x40015698	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX314_SL_ATT3	0x4001569C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX314_MS_ADDR	0x400156A0	Master region, base address
PERI_MS_PPU_FX314_MS_SIZE	0x400156A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX314_MS_ATT0	0x400156B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX314_MS_ATT1	0x400156B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX314_MS_ATT2	0x400156B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX314_MS_ATT3	0x400156BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX315_SL_ADDR	0x400156C0	Slave region, base address
PERI_MS_PPU_FX315_SL_SIZE	0x400156C4	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX315_SL_ATT0	0x400156D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX315_SL_ATT1	0x400156D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX315_SL_ATT2	0x400156D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX315_SL_ATT3	0x400156DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX315_MS_ADDR	0x400156E0	Master region, base address
PERI_MS_PPU_FX315_MS_SIZE	0x400156E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX315_MS_ATT0	0x400156F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX315_MS_ATT1	0x400156F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX315_MS_ATT2	0x400156F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX315_MS_ATT3	0x400156FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX316_SL_ADDR	0x40015700	Slave region, base address
PERI_MS_PPU_FX316_SL_SIZE	0x40015704	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX316_SL_ATT0	0x40015710	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX316_SL_ATT1	0x40015714	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX316_SL_ATT2	0x40015718	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX316_SL_ATT3	0x4001571C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX316_MS_ADDR	0x40015720	Master region, base address
PERI_MS_PPU_FX316_MS_SIZE	0x40015724	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX316_MS_ATT0	0x40015730	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX316_MS_ATT1	0x40015734	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX316_MS_ATT2	0x40015738	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX316_MS_ATT3	0x4001573C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX317_SL_ADDR	0x40015740	Slave region, base address
PERI_MS_PPU_FX317_SL_SIZE	0x40015744	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX317_SL_ATT0	0x40015750	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX317_SL_ATT1	0x40015754	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX317_SL_ATT2	0x40015758	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX317_SL_ATT3	0x4001575C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX317_MS_ADDR	0x40015760	Master region, base address
PERI_MS_PPU_FX317_MS_SIZE	0x40015764	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX317_MS_ATT0	0x40015770	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX317_MS_ATT1	0x40015774	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX317_MS_ATT2	0x40015778	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX317_MS_ATT3	0x4001577C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX318_SL_ADDR	0x40015780	Slave region, base address
PERI_MS_PPU_FX318_SL_SIZE	0x40015784	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX318_SL_ATT0	0x40015790	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX318_SL_ATT1	0x40015794	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX318_SL_ATT2	0x40015798	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX318_SL_ATT3	0x4001579C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX318_MS_ADDR	0x400157A0	Master region, base address
PERI_MS_PPU_FX318_MS_SIZE	0x400157A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX318_MS_ATT0	0x400157B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX318_MS_ATT1	0x400157B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX318_MS_ATT2	0x400157B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX318_MS_ATT3	0x400157BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX319_SL_ADDR	0x400157C0	Slave region, base address
PERI_MS_PPU_FX319_SL_SIZE	0x400157C4	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX319_SL_ATT0	0x400157D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX319_SL_ATT1	0x400157D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX319_SL_ATT2	0x400157D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX319_SL_ATT3	0x400157DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX319_MS_ADDR	0x400157E0	Master region, base address
PERI_MS_PPU_FX319_MS_SIZE	0x400157E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX319_MS_ATT0	0x400157F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX319_MS_ATT1	0x400157F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX319_MS_ATT2	0x400157F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX319_MS_ATT3	0x400157FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX320_SL_ADDR	0x40015800	Slave region, base address
PERI_MS_PPU_FX320_SL_SIZE	0x40015804	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX320_SL_ATT0	0x40015810	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX320_SL_ATT1	0x40015814	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX320_SL_ATT2	0x40015818	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX320_SL_ATT3	0x4001581C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX320_MS_ADDR	0x40015820	Master region, base address
PERI_MS_PPU_FX320_MS_SIZE	0x40015824	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX320_MS_ATT0	0x40015830	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX320_MS_ATT1	0x40015834	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX320_MS_ATT2	0x40015838	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX320_MS_ATT3	0x4001583C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX321_SL_ADDR	0x40015840	Slave region, base address
PERI_MS_PPU_FX321_SL_SIZE	0x40015844	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX321_SL_ATT0	0x40015850	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX321_SL_ATT1	0x40015854	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX321_SL_ATT2	0x40015858	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX321_SL_ATT3	0x4001585C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX321_MS_ADDR	0x40015860	Master region, base address
PERI_MS_PPU_FX321_MS_SIZE	0x40015864	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX321_MS_ATT0	0x40015870	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX321_MS_ATT1	0x40015874	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX321_MS_ATT2	0x40015878	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX321_MS_ATT3	0x4001587C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX322_SL_ADDR	0x40015880	Slave region, base address
PERI_MS_PPU_FX322_SL_SIZE	0x40015884	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX322_SL_ATT0	0x40015890	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX322_SL_ATT1	0x40015894	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX322_SL_ATT2	0x40015898	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX322_SL_ATT3	0x4001589C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX322_MS_ADDR	0x400158A0	Master region, base address
PERI_MS_PPU_FX322_MS_SIZE	0x400158A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX322_MS_ATT0	0x400158B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX322_MS_ATT1	0x400158B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX322_MS_ATT2	0x400158B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX322_MS_ATT3	0x400158BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX323_SL_ADDR	0x400158C0	Slave region, base address
PERI_MS_PPU_FX323_SL_SIZE	0x400158C4	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX323_SL_ATT0	0x400158D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX323_SL_ATT1	0x400158D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX323_SL_ATT2	0x400158D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX323_SL_ATT3	0x400158DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX323_MS_ADDR	0x400158E0	Master region, base address
PERI_MS_PPU_FX323_MS_SIZE	0x400158E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX323_MS_ATT0	0x400158F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX323_MS_ATT1	0x400158F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX323_MS_ATT2	0x400158F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX323_MS_ATT3	0x400158FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX324_SL_ADDR	0x40015900	Slave region, base address
PERI_MS_PPU_FX324_SL_SIZE	0x40015904	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX324_SL_ATT0	0x40015910	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX324_SL_ATT1	0x40015914	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX324_SL_ATT2	0x40015918	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX324_SL_ATT3	0x4001591C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX324_MS_ADDR	0x40015920	Master region, base address
PERI_MS_PPU_FX324_MS_SIZE	0x40015924	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX324_MS_ATT0	0x40015930	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX324_MS_ATT1	0x40015934	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX324_MS_ATT2	0x40015938	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX324_MS_ATT3	0x4001593C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX325_SL_ADDR	0x40015940	Slave region, base address
PERI_MS_PPU_FX325_SL_SIZE	0x40015944	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX325_SL_ATT0	0x40015950	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX325_SL_ATT1	0x40015954	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX325_SL_ATT2	0x40015958	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX325_SL_ATT3	0x4001595C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX325_MS_ADDR	0x40015960	Master region, base address
PERI_MS_PPU_FX325_MS_SIZE	0x40015964	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX325_MS_ATT0	0x40015970	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX325_MS_ATT1	0x40015974	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX325_MS_ATT2	0x40015978	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX325_MS_ATT3	0x4001597C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX326_SL_ADDR	0x40015980	Slave region, base address
PERI_MS_PPU_FX326_SL_SIZE	0x40015984	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX326_SL_ATT0	0x40015990	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX326_SL_ATT1	0x40015994	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX326_SL_ATT2	0x40015998	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX326_SL_ATT3	0x4001599C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX326_MS_ADDR	0x400159A0	Master region, base address
PERI_MS_PPU_FX326_MS_SIZE	0x400159A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX326_MS_ATT0	0x400159B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX326_MS_ATT1	0x400159B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX326_MS_ATT2	0x400159B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX326_MS_ATT3	0x400159BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX327_SL_ADDR	0x400159C0	Slave region, base address
PERI_MS_PPU_FX327_SL_SIZE	0x400159C4	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX327_SL_ATT0	0x400159D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX327_SL_ATT1	0x400159D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX327_SL_ATT2	0x400159D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX327_SL_ATT3	0x400159DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX327_MS_ADDR	0x400159E0	Master region, base address
PERI_MS_PPU_FX327_MS_SIZE	0x400159E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX327_MS_ATT0	0x400159F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX327_MS_ATT1	0x400159F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX327_MS_ATT2	0x400159F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX327_MS_ATT3	0x400159FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX328_SL_ADDR	0x40015A00	Slave region, base address
PERI_MS_PPU_FX328_SL_SIZE	0x40015A04	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX328_SL_ATT0	0x40015A10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX328_SL_ATT1	0x40015A14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX328_SL_ATT2	0x40015A18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX328_SL_ATT3	0x40015A1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX328_MS_ADDR	0x40015A20	Master region, base address
PERI_MS_PPU_FX328_MS_SIZE	0x40015A24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX328_MS_ATT0	0x40015A30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX328_MS_ATT1	0x40015A34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX328_MS_ATT2	0x40015A38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX328_MS_ATT3	0x40015A3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX329_SL_ADDR	0x40015A40	Slave region, base address
PERI_MS_PPU_FX329_SL_SIZE	0x40015A44	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX329_SL_ATT0	0x40015A50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX329_SL_ATT1	0x40015A54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX329_SL_ATT2	0x40015A58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX329_SL_ATT3	0x40015A5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX329_MS_ADDR	0x40015A60	Master region, base address
PERI_MS_PPU_FX329_MS_SIZE	0x40015A64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX329_MS_ATT0	0x40015A70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX329_MS_ATT1	0x40015A74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX329_MS_ATT2	0x40015A78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX329_MS_ATT3	0x40015A7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX330_SL_ADDR	0x40015A80	Slave region, base address
PERI_MS_PPU_FX330_SL_SIZE	0x40015A84	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX330_SL_ATT0	0x40015A90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX330_SL_ATT1	0x40015A94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX330_SL_ATT2	0x40015A98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX330_SL_ATT3	0x40015A9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX330_MS_ADDR	0x40015AA0	Master region, base address
PERI_MS_PPU_FX330_MS_SIZE	0x40015AA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX330_MS_ATT0	0x40015AB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX330_MS_ATT1	0x40015AB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX330_MS_ATT2	0x40015AB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX330_MS_ATT3	0x40015ABC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX331_SL_ADDR	0x40015AC0	Slave region, base address
PERI_MS_PPU_FX331_SL_SIZE	0x40015AC4	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX331_SL_ATT0	0x40015AD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX331_SL_ATT1	0x40015AD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX331_SL_ATT2	0x40015AD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX331_SL_ATT3	0x40015ADC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX331_MS_ADDR	0x40015AE0	Master region, base address
PERI_MS_PPU_FX331_MS_SIZE	0x40015AE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX331_MS_ATT0	0x40015AF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX331_MS_ATT1	0x40015AF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX331_MS_ATT2	0x40015AF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX331_MS_ATT3	0x40015AFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX332_SL_ADDR	0x40015B00	Slave region, base address
PERI_MS_PPU_FX332_SL_SIZE	0x40015B04	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX332_SL_ATT0	0x40015B10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX332_SL_ATT1	0x40015B14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX332_SL_ATT2	0x40015B18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX332_SL_ATT3	0x40015B1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX332_MS_ADDR	0x40015B20	Master region, base address
PERI_MS_PPU_FX332_MS_SIZE	0x40015B24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX332_MS_ATT0	0x40015B30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX332_MS_ATT1	0x40015B34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX332_MS_ATT2	0x40015B38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX332_MS_ATT3	0x40015B3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX333_SL_ADDR	0x40015B40	Slave region, base address
PERI_MS_PPU_FX333_SL_SIZE	0x40015B44	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX333_SL_ATT0	0x40015B50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX333_SL_ATT1	0x40015B54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX333_SL_ATT2	0x40015B58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX333_SL_ATT3	0x40015B5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX333_MS_ADDR	0x40015B60	Master region, base address
PERI_MS_PPU_FX333_MS_SIZE	0x40015B64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX333_MS_ATT0	0x40015B70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX333_MS_ATT1	0x40015B74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX333_MS_ATT2	0x40015B78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX333_MS_ATT3	0x40015B7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX334_SL_ADDR	0x40015B80	Slave region, base address
PERI_MS_PPU_FX334_SL_SIZE	0x40015B84	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX334_SL_ATT0	0x40015B90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX334_SL_ATT1	0x40015B94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX334_SL_ATT2	0x40015B98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX334_SL_ATT3	0x40015B9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX334_MS_ADDR	0x40015BA0	Master region, base address
PERI_MS_PPU_FX334_MS_SIZE	0x40015BA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX334_MS_ATT0	0x40015BB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX334_MS_ATT1	0x40015BB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX334_MS_ATT2	0x40015BB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX334_MS_ATT3	0x40015BBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX335_SL_ADDR	0x40015BC0	Slave region, base address
PERI_MS_PPU_FX335_SL_SIZE	0x40015BC4	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX335_SL_ATT0	0x40015BD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX335_SL_ATT1	0x40015BD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX335_SL_ATT2	0x40015BD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX335_SL_ATT3	0x40015BDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX335_MS_ADDR	0x40015BE0	Master region, base address
PERI_MS_PPU_FX335_MS_SIZE	0x40015BE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX335_MS_ATT0	0x40015BF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX335_MS_ATT1	0x40015BF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX335_MS_ATT2	0x40015BF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX335_MS_ATT3	0x40015BFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX336_SL_ADDR	0x40015C00	Slave region, base address
PERI_MS_PPU_FX336_SL_SIZE	0x40015C04	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX336_SL_ATT0	0x40015C10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX336_SL_ATT1	0x40015C14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX336_SL_ATT2	0x40015C18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX336_SL_ATT3	0x40015C1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX336_MS_ADDR	0x40015C20	Master region, base address
PERI_MS_PPU_FX336_MS_SIZE	0x40015C24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX336_MS_ATT0	0x40015C30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX336_MS_ATT1	0x40015C34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX336_MS_ATT2	0x40015C38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX336_MS_ATT3	0x40015C3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX337_SL_ADDR	0x40015C40	Slave region, base address
PERI_MS_PPU_FX337_SL_SIZE	0x40015C44	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX337_SL_ATT0	0x40015C50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX337_SL_ATT1	0x40015C54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX337_SL_ATT2	0x40015C58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX337_SL_ATT3	0x40015C5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX337_MS_ADDR	0x40015C60	Master region, base address
PERI_MS_PPU_FX337_MS_SIZE	0x40015C64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX337_MS_ATT0	0x40015C70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX337_MS_ATT1	0x40015C74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX337_MS_ATT2	0x40015C78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX337_MS_ATT3	0x40015C7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX338_SL_ADDR	0x40015C80	Slave region, base address
PERI_MS_PPU_FX338_SL_SIZE	0x40015C84	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX338_SL_ATT0	0x40015C90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX338_SL_ATT1	0x40015C94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX338_SL_ATT2	0x40015C98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX338_SL_ATT3	0x40015C9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX338_MS_ADDR	0x40015CA0	Master region, base address
PERI_MS_PPU_FX338_MS_SIZE	0x40015CA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX338_MS_ATT0	0x40015CB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX338_MS_ATT1	0x40015CB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX338_MS_ATT2	0x40015CB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX338_MS_ATT3	0x40015CBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX339_SL_ADDR	0x40015CC0	Slave region, base address
PERI_MS_PPU_FX339_SL_SIZE	0x40015CC4	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX339_SL_ATT0	0x40015CD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX339_SL_ATT1	0x40015CD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX339_SL_ATT2	0x40015CD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX339_SL_ATT3	0x40015CDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX339_MS_ADDR	0x40015CE0	Master region, base address
PERI_MS_PPU_FX339_MS_SIZE	0x40015CE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX339_MS_ATT0	0x40015CF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX339_MS_ATT1	0x40015CF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX339_MS_ATT2	0x40015CF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX339_MS_ATT3	0x40015CFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX340_SL_ADDR	0x40015D00	Slave region, base address
PERI_MS_PPU_FX340_SL_SIZE	0x40015D04	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX340_SL_ATT0	0x40015D10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX340_SL_ATT1	0x40015D14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX340_SL_ATT2	0x40015D18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX340_SL_ATT3	0x40015D1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX340_MS_ADDR	0x40015D20	Master region, base address
PERI_MS_PPU_FX340_MS_SIZE	0x40015D24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX340_MS_ATT0	0x40015D30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX340_MS_ATT1	0x40015D34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX340_MS_ATT2	0x40015D38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX340_MS_ATT3	0x40015D3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX341_SL_ADDR	0x40015D40	Slave region, base address
PERI_MS_PPU_FX341_SL_SIZE	0x40015D44	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX341_SL_ATT0	0x40015D50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX341_SL_ATT1	0x40015D54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX341_SL_ATT2	0x40015D58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX341_SL_ATT3	0x40015D5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX341_MS_ADDR	0x40015D60	Master region, base address
PERI_MS_PPU_FX341_MS_SIZE	0x40015D64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX341_MS_ATT0	0x40015D70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX341_MS_ATT1	0x40015D74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX341_MS_ATT2	0x40015D78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX341_MS_ATT3	0x40015D7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX342_SL_ADDR	0x40015D80	Slave region, base address
PERI_MS_PPU_FX342_SL_SIZE	0x40015D84	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX342_SL_ATT0	0x40015D90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX342_SL_ATT1	0x40015D94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX342_SL_ATT2	0x40015D98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX342_SL_ATT3	0x40015D9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX342_MS_ADDR	0x40015DA0	Master region, base address
PERI_MS_PPU_FX342_MS_SIZE	0x40015DA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX342_MS_ATT0	0x40015DB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX342_MS_ATT1	0x40015DB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX342_MS_ATT2	0x40015DB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX342_MS_ATT3	0x40015DBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX343_SL_ADDR	0x40015DC0	Slave region, base address
PERI_MS_PPU_FX343_SL_SIZE	0x40015DC4	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX343_SL_ATT0	0x40015DD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX343_SL_ATT1	0x40015DD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX343_SL_ATT2	0x40015DD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX343_SL_ATT3	0x40015DDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX343_MS_ADDR	0x40015DE0	Master region, base address
PERI_MS_PPU_FX343_MS_SIZE	0x40015DE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX343_MS_ATT0	0x40015DF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX343_MS_ATT1	0x40015DF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX343_MS_ATT2	0x40015DF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX343_MS_ATT3	0x40015DFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX344_SL_ADDR	0x40015E00	Slave region, base address
PERI_MS_PPU_FX344_SL_SIZE	0x40015E04	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX344_SL_ATT0	0x40015E10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX344_SL_ATT1	0x40015E14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX344_SL_ATT2	0x40015E18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX344_SL_ATT3	0x40015E1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX344_MS_ADDR	0x40015E20	Master region, base address
PERI_MS_PPU_FX344_MS_SIZE	0x40015E24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX344_MS_ATT0	0x40015E30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX344_MS_ATT1	0x40015E34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX344_MS_ATT2	0x40015E38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX344_MS_ATT3	0x40015E3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX345_SL_ADDR	0x40015E40	Slave region, base address
PERI_MS_PPU_FX345_SL_SIZE	0x40015E44	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX345_SL_ATT0	0x40015E50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX345_SL_ATT1	0x40015E54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX345_SL_ATT2	0x40015E58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX345_SL_ATT3	0x40015E5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX345_MS_ADDR	0x40015E60	Master region, base address
PERI_MS_PPU_FX345_MS_SIZE	0x40015E64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX345_MS_ATT0	0x40015E70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX345_MS_ATT1	0x40015E74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX345_MS_ATT2	0x40015E78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX345_MS_ATT3	0x40015E7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX346_SL_ADDR	0x40015E80	Slave region, base address
PERI_MS_PPU_FX346_SL_SIZE	0x40015E84	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX346_SL_ATT0	0x40015E90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX346_SL_ATT1	0x40015E94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX346_SL_ATT2	0x40015E98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX346_SL_ATT3	0x40015E9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX346_MS_ADDR	0x40015EA0	Master region, base address
PERI_MS_PPU_FX346_MS_SIZE	0x40015EA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX346_MS_ATT0	0x40015EB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX346_MS_ATT1	0x40015EB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX346_MS_ATT2	0x40015EB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX346_MS_ATT3	0x40015EBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX347_SL_ADDR	0x40015EC0	Slave region, base address
PERI_MS_PPU_FX347_SL_SIZE	0x40015EC4	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX347_SL_ATT0	0x40015ED0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX347_SL_ATT1	0x40015ED4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX347_SL_ATT2	0x40015ED8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX347_SL_ATT3	0x40015EDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX347_MS_ADDR	0x40015EE0	Master region, base address
PERI_MS_PPU_FX347_MS_SIZE	0x40015EE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX347_MS_ATT0	0x40015EF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX347_MS_ATT1	0x40015EF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX347_MS_ATT2	0x40015EF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX347_MS_ATT3	0x40015EFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX348_SL_ADDR	0x40015F00	Slave region, base address
PERI_MS_PPU_FX348_SL_SIZE	0x40015F04	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX348_SL_ATT0	0x40015F10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX348_SL_ATT1	0x40015F14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX348_SL_ATT2	0x40015F18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX348_SL_ATT3	0x40015F1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX348_MS_ADDR	0x40015F20	Master region, base address
PERI_MS_PPU_FX348_MS_SIZE	0x40015F24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX348_MS_ATT0	0x40015F30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX348_MS_ATT1	0x40015F34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX348_MS_ATT2	0x40015F38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX348_MS_ATT3	0x40015F3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX349_SL_ADDR	0x40015F40	Slave region, base address
PERI_MS_PPU_FX349_SL_SIZE	0x40015F44	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX349_SL_ATT0	0x40015F50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX349_SL_ATT1	0x40015F54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX349_SL_ATT2	0x40015F58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX349_SL_ATT3	0x40015F5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX349_MS_ADDR	0x40015F60	Master region, base address
PERI_MS_PPU_FX349_MS_SIZE	0x40015F64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX349_MS_ATT0	0x40015F70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX349_MS_ATT1	0x40015F74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX349_MS_ATT2	0x40015F78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX349_MS_ATT3	0x40015F7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX350_SL_ADDR	0x40015F80	Slave region, base address
PERI_MS_PPU_FX350_SL_SIZE	0x40015F84	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX350_SL_ATT0	0x40015F90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX350_SL_ATT1	0x40015F94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX350_SL_ATT2	0x40015F98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX350_SL_ATT3	0x40015F9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX350_MS_ADDR	0x40015FA0	Master region, base address
PERI_MS_PPU_FX350_MS_SIZE	0x40015FA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX350_MS_ATT0	0x40015FB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX350_MS_ATT1	0x40015FB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX350_MS_ATT2	0x40015FB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX350_MS_ATT3	0x40015FBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX351_SL_ADDR	0x40015FC0	Slave region, base address
PERI_MS_PPU_FX351_SL_SIZE	0x40015FC4	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX351_SL_ATT0	0x40015FD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX351_SL_ATT1	0x40015FD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX351_SL_ATT2	0x40015FD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX351_SL_ATT3	0x40015FDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX351_MS_ADDR	0x40015FE0	Master region, base address
PERI_MS_PPU_FX351_MS_SIZE	0x40015FE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX351_MS_ATT0	0x40015FF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX351_MS_ATT1	0x40015FF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX351_MS_ATT2	0x40015FF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX351_MS_ATT3	0x40015FFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX352_SL_ADDR	0x40016000	Slave region, base address
PERI_MS_PPU_FX352_SL_SIZE	0x40016004	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX352_SL_ATT0	0x40016010	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX352_SL_ATT1	0x40016014	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX352_SL_ATT2	0x40016018	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX352_SL_ATT3	0x4001601C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX352_MS_ADDR	0x40016020	Master region, base address
PERI_MS_PPU_FX352_MS_SIZE	0x40016024	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX352_MS_ATT0	0x40016030	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX352_MS_ATT1	0x40016034	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX352_MS_ATT2	0x40016038	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX352_MS_ATT3	0x4001603C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX353_SL_ADDR	0x40016040	Slave region, base address
PERI_MS_PPU_FX353_SL_SIZE	0x40016044	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX353_SL_ATT0	0x40016050	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX353_SL_ATT1	0x40016054	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX353_SL_ATT2	0x40016058	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX353_SL_ATT3	0x4001605C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX353_MS_ADDR	0x40016060	Master region, base address
PERI_MS_PPU_FX353_MS_SIZE	0x40016064	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX353_MS_ATT0	0x40016070	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX353_MS_ATT1	0x40016074	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX353_MS_ATT2	0x40016078	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX353_MS_ATT3	0x4001607C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX354_SL_ADDR	0x40016080	Slave region, base address
PERI_MS_PPU_FX354_SL_SIZE	0x40016084	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX354_SL_ATT0	0x40016090	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX354_SL_ATT1	0x40016094	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX354_SL_ATT2	0x40016098	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX354_SL_ATT3	0x4001609C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX354_MS_ADDR	0x400160A0	Master region, base address
PERI_MS_PPU_FX354_MS_SIZE	0x400160A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX354_MS_ATT0	0x400160B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX354_MS_ATT1	0x400160B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX354_MS_ATT2	0x400160B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX354_MS_ATT3	0x400160BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX355_SL_ADDR	0x400160C0	Slave region, base address
PERI_MS_PPU_FX355_SL_SIZE	0x400160C4	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX355_SL_ATT0	0x400160D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX355_SL_ATT1	0x400160D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX355_SL_ATT2	0x400160D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX355_SL_ATT3	0x400160DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX355_MS_ADDR	0x400160E0	Master region, base address
PERI_MS_PPU_FX355_MS_SIZE	0x400160E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX355_MS_ATT0	0x400160F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX355_MS_ATT1	0x400160F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX355_MS_ATT2	0x400160F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX355_MS_ATT3	0x400160FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX356_SL_ADDR	0x40016100	Slave region, base address
PERI_MS_PPU_FX356_SL_SIZE	0x40016104	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX356_SL_ATT0	0x40016110	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX356_SL_ATT1	0x40016114	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX356_SL_ATT2	0x40016118	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX356_SL_ATT3	0x4001611C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX356_MS_ADDR	0x40016120	Master region, base address
PERI_MS_PPU_FX356_MS_SIZE	0x40016124	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX356_MS_ATT0	0x40016130	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX356_MS_ATT1	0x40016134	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX356_MS_ATT2	0x40016138	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX356_MS_ATT3	0x4001613C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX357_SL_ADDR	0x40016140	Slave region, base address
PERI_MS_PPU_FX357_SL_SIZE	0x40016144	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX357_SL_ATT0	0x40016150	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX357_SL_ATT1	0x40016154	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX357_SL_ATT2	0x40016158	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX357_SL_ATT3	0x4001615C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX357_MS_ADDR	0x40016160	Master region, base address
PERI_MS_PPU_FX357_MS_SIZE	0x40016164	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX357_MS_ATT0	0x40016170	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX357_MS_ATT1	0x40016174	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX357_MS_ATT2	0x40016178	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX357_MS_ATT3	0x4001617C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX358_SL_ADDR	0x40016180	Slave region, base address
PERI_MS_PPU_FX358_SL_SIZE	0x40016184	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX358_SL_ATT0	0x40016190	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX358_SL_ATT1	0x40016194	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX358_SL_ATT2	0x40016198	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX358_SL_ATT3	0x4001619C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX358_MS_ADDR	0x400161A0	Master region, base address
PERI_MS_PPU_FX358_MS_SIZE	0x400161A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX358_MS_ATT0	0x400161B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX358_MS_ATT1	0x400161B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX358_MS_ATT2	0x400161B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX358_MS_ATT3	0x400161BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX359_SL_ADDR	0x400161C0	Slave region, base address
PERI_MS_PPU_FX359_SL_SIZE	0x400161C4	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX359_SL_ATT0	0x400161D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX359_SL_ATT1	0x400161D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX359_SL_ATT2	0x400161D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX359_SL_ATT3	0x400161DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX359_MS_ADDR	0x400161E0	Master region, base address
PERI_MS_PPU_FX359_MS_SIZE	0x400161E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX359_MS_ATT0	0x400161F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX359_MS_ATT1	0x400161F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX359_MS_ATT2	0x400161F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX359_MS_ATT3	0x400161FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX360_SL_ADDR	0x40016200	Slave region, base address
PERI_MS_PPU_FX360_SL_SIZE	0x40016204	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX360_SL_ATT0	0x40016210	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX360_SL_ATT1	0x40016214	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX360_SL_ATT2	0x40016218	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX360_SL_ATT3	0x4001621C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX360_MS_ADDR	0x40016220	Master region, base address
PERI_MS_PPU_FX360_MS_SIZE	0x40016224	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX360_MS_ATT0	0x40016230	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX360_MS_ATT1	0x40016234	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX360_MS_ATT2	0x40016238	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX360_MS_ATT3	0x4001623C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX361_SL_ADDR	0x40016240	Slave region, base address
PERI_MS_PPU_FX361_SL_SIZE	0x40016244	Slave region, size. See PERI_MS_PPU_FX48_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX361_SL_ATT0	0x40016250	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX361_SL_ATT1	0x40016254	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX361_SL_ATT2	0x40016258	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX361_SL_ATT3	0x4001625C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX361_MS_ADDR	0x40016260	Master region, base address
PERI_MS_PPU_FX361_MS_SIZE	0x40016264	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX361_MS_ATT0	0x40016270	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX361_MS_ATT1	0x40016274	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX361_MS_ATT2	0x40016278	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX361_MS_ATT3	0x4001627C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX362_SL_ADDR	0x40016280	Slave region, base address
PERI_MS_PPU_FX362_SL_SIZE	0x40016284	Slave region, size. See PERI_MS_PPU_FX17_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX362_SL_ATT0	0x40016290	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX362_SL_ATT1	0x40016294	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX362_SL_ATT2	0x40016298	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX362_SL_ATT3	0x4001629C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX362_MS_ADDR	0x400162A0	Master region, base address
PERI_MS_PPU_FX362_MS_SIZE	0x400162A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX362_MS_ATT0	0x400162B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX362_MS_ATT1	0x400162B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX362_MS_ATT2	0x400162B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX362_MS_ATT3	0x400162BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX363_SL_ADDR	0x400162C0	Slave region, base address
PERI_MS_PPU_FX363_SL_SIZE	0x400162C4	Slave region, size. See PERI_MS_PPU_FX45_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX363_SL_ATT0	0x400162D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX363_SL_ATT1	0x400162D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX363_SL_ATT2	0x400162D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX363_SL_ATT3	0x400162DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX363_MS_ADDR	0x400162E0	Master region, base address
PERI_MS_PPU_FX363_MS_SIZE	0x400162E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX363_MS_ATT0	0x400162F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX363_MS_ATT1	0x400162F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX363_MS_ATT2	0x400162F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX363_MS_ATT3	0x400162FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX364_SL_ADDR	0x40016300	Slave region, base address
PERI_MS_PPU_FX364_SL_SIZE	0x40016304	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX364_SL_ATT0	0x40016310	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX364_SL_ATT1	0x40016314	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX364_SL_ATT2	0x40016318	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX364_SL_ATT3	0x4001631C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX364_MS_ADDR	0x40016320	Master region, base address
PERI_MS_PPU_FX364_MS_SIZE	0x40016324	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX364_MS_ATT0	0x40016330	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX364_MS_ATT1	0x40016334	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX364_MS_ATT2	0x40016338	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX364_MS_ATT3	0x4001633C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX365_SL_ADDR	0x40016340	Slave region, base address
PERI_MS_PPU_FX365_SL_SIZE	0x40016344	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX365_SL_ATT0	0x40016350	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX365_SL_ATT1	0x40016354	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX365_SL_ATT2	0x40016358	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX365_SL_ATT3	0x4001635C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX365_MS_ADDR	0x40016360	Master region, base address
PERI_MS_PPU_FX365_MS_SIZE	0x40016364	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX365_MS_ATT0	0x40016370	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX365_MS_ATT1	0x40016374	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX365_MS_ATT2	0x40016378	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX365_MS_ATT3	0x4001637C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX366_SL_ADDR	0x40016380	Slave region, base address
PERI_MS_PPU_FX366_SL_SIZE	0x40016384	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX366_SL_ATT0	0x40016390	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX366_SL_ATT1	0x40016394	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX366_SL_ATT2	0x40016398	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX366_SL_ATT3	0x4001639C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX366_MS_ADDR	0x400163A0	Master region, base address
PERI_MS_PPU_FX366_MS_SIZE	0x400163A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX366_MS_ATT0	0x400163B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX366_MS_ATT1	0x400163B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX366_MS_ATT2	0x400163B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX366_MS_ATT3	0x400163BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX367_SL_ADDR	0x400163C0	Slave region, base address
PERI_MS_PPU_FX367_SL_SIZE	0x400163C4	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX367_SL_ATT0	0x400163D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX367_SL_ATT1	0x400163D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX367_SL_ATT2	0x400163D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX367_SL_ATT3	0x400163DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX367_MS_ADDR	0x400163E0	Master region, base address
PERI_MS_PPU_FX367_MS_SIZE	0x400163E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX367_MS_ATT0	0x400163F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX367_MS_ATT1	0x400163F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX367_MS_ATT2	0x400163F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX367_MS_ATT3	0x400163FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX368_SL_ADDR	0x40016400	Slave region, base address
PERI_MS_PPU_FX368_SL_SIZE	0x40016404	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX368_SL_ATT0	0x40016410	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX368_SL_ATT1	0x40016414	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX368_SL_ATT2	0x40016418	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX368_SL_ATT3	0x4001641C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX368_MS_ADDR	0x40016420	Master region, base address
PERI_MS_PPU_FX368_MS_SIZE	0x40016424	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX368_MS_ATT0	0x40016430	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX368_MS_ATT1	0x40016434	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX368_MS_ATT2	0x40016438	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX368_MS_ATT3	0x4001643C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX369_SL_ADDR	0x40016440	Slave region, base address
PERI_MS_PPU_FX369_SL_SIZE	0x40016444	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX369_SL_ATT0	0x40016450	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX369_SL_ATT1	0x40016454	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX369_SL_ATT2	0x40016458	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX369_SL_ATT3	0x4001645C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX369_MS_ADDR	0x40016460	Master region, base address
PERI_MS_PPU_FX369_MS_SIZE	0x40016464	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX369_MS_ATT0	0x40016470	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX369_MS_ATT1	0x40016474	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX369_MS_ATT2	0x40016478	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX369_MS_ATT3	0x4001647C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX370_SL_ADDR	0x40016480	Slave region, base address
PERI_MS_PPU_FX370_SL_SIZE	0x40016484	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX370_SL_ATT0	0x40016490	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX370_SL_ATT1	0x40016494	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX370_SL_ATT2	0x40016498	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX370_SL_ATT3	0x4001649C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX370_MS_ADDR	0x400164A0	Master region, base address
PERI_MS_PPU_FX370_MS_SIZE	0x400164A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX370_MS_ATT0	0x400164B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX370_MS_ATT1	0x400164B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX370_MS_ATT2	0x400164B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX370_MS_ATT3	0x400164BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX371_SL_ADDR	0x400164C0	Slave region, base address
PERI_MS_PPU_FX371_SL_SIZE	0x400164C4	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX371_SL_ATT0	0x400164D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX371_SL_ATT1	0x400164D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX371_SL_ATT2	0x400164D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX371_SL_ATT3	0x400164DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX371_MS_ADDR	0x400164E0	Master region, base address
PERI_MS_PPU_FX371_MS_SIZE	0x400164E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX371_MS_ATT0	0x400164F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX371_MS_ATT1	0x400164F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX371_MS_ATT2	0x400164F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX371_MS_ATT3	0x400164FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX372_SL_ADDR	0x40016500	Slave region, base address
PERI_MS_PPU_FX372_SL_SIZE	0x40016504	Slave region, size. See PERI_MS_PPU_FX18_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX372_SL_ATT0	0x40016510	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX372_SL_ATT1	0x40016514	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX372_SL_ATT2	0x40016518	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX372_SL_ATT3	0x4001651C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX372_MS_ADDR	0x40016520	Master region, base address
PERI_MS_PPU_FX372_MS_SIZE	0x40016524	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX372_MS_ATT0	0x40016530	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX372_MS_ATT1	0x40016534	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX372_MS_ATT2	0x40016538	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX372_MS_ATT3	0x4001653C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX373_SL_ADDR	0x40016540	Slave region, base address
PERI_MS_PPU_FX373_SL_SIZE	0x40016544	Slave region, size. See PERI_MS_PPU_FX18_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX373_SL_ATT0	0x40016550	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX373_SL_ATT1	0x40016554	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX373_SL_ATT2	0x40016558	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX373_SL_ATT3	0x4001655C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX373_MS_ADDR	0x40016560	Master region, base address
PERI_MS_PPU_FX373_MS_SIZE	0x40016564	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX373_MS_ATT0	0x40016570	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX373_MS_ATT1	0x40016574	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX373_MS_ATT2	0x40016578	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX373_MS_ATT3	0x4001657C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX374_SL_ADDR	0x40016580	Slave region, base address
PERI_MS_PPU_FX374_SL_SIZE	0x40016584	Slave region, size. See PERI_MS_PPU_FX18_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX374_SL_ATT0	0x40016590	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX374_SL_ATT1	0x40016594	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX374_SL_ATT2	0x40016598	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX374_SL_ATT3	0x4001659C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX374_MS_ADDR	0x400165A0	Master region, base address
PERI_MS_PPU_FX374_MS_SIZE	0x400165A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX374_MS_ATT0	0x400165B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX374_MS_ATT1	0x400165B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX374_MS_ATT2	0x400165B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX374_MS_ATT3	0x400165BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX375_SL_ADDR	0x400165C0	Slave region, base address
PERI_MS_PPU_FX375_SL_SIZE	0x400165C4	Slave region, size. See PERI_MS_PPU_FX18_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX375_SL_ATT0	0x400165D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX375_SL_ATT1	0x400165D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX375_SL_ATT2	0x400165D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX375_SL_ATT3	0x400165DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX375_MS_ADDR	0x400165E0	Master region, base address
PERI_MS_PPU_FX375_MS_SIZE	0x400165E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX375_MS_ATT0	0x400165F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX375_MS_ATT1	0x400165F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX375_MS_ATT2	0x400165F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX375_MS_ATT3	0x400165FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX376_SL_ADDR	0x40016600	Slave region, base address
PERI_MS_PPU_FX376_SL_SIZE	0x40016604	Slave region, size. See PERI_MS_PPU_FX18_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX376_SL_ATT0	0x40016610	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX376_SL_ATT1	0x40016614	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX376_SL_ATT2	0x40016618	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX376_SL_ATT3	0x4001661C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX376_MS_ADDR	0x40016620	Master region, base address
PERI_MS_PPU_FX376_MS_SIZE	0x40016624	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX376_MS_ATT0	0x40016630	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX376_MS_ATT1	0x40016634	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX376_MS_ATT2	0x40016638	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX376_MS_ATT3	0x4001663C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX377_SL_ADDR	0x40016640	Slave region, base address
PERI_MS_PPU_FX377_SL_SIZE	0x40016644	Slave region, size. See PERI_MS_PPU_FX18_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX377_SL_ATT0	0x40016650	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX377_SL_ATT1	0x40016654	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX377_SL_ATT2	0x40016658	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX377_SL_ATT3	0x4001665C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX377_MS_ADDR	0x40016660	Master region, base address
PERI_MS_PPU_FX377_MS_SIZE	0x40016664	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX377_MS_ATT0	0x40016670	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX377_MS_ATT1	0x40016674	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX377_MS_ATT2	0x40016678	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX377_MS_ATT3	0x4001667C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX378_SL_ADDR	0x40016680	Slave region, base address
PERI_MS_PPU_FX378_SL_SIZE	0x40016684	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX378_SL_ATT0	0x40016690	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX378_SL_ATT1	0x40016694	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX378_SL_ATT2	0x40016698	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX378_SL_ATT3	0x4001669C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX378_MS_ADDR	0x400166A0	Master region, base address
PERI_MS_PPU_FX378_MS_SIZE	0x400166A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX378_MS_ATT0	0x400166B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX378_MS_ATT1	0x400166B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX378_MS_ATT2	0x400166B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX378_MS_ATT3	0x400166BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX379_SL_ADDR	0x400166C0	Slave region, base address
PERI_MS_PPU_FX379_SL_SIZE	0x400166C4	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX379_SL_ATT0	0x400166D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX379_SL_ATT1	0x400166D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX379_SL_ATT2	0x400166D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX379_SL_ATT3	0x400166DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX379_MS_ADDR	0x400166E0	Master region, base address
PERI_MS_PPU_FX379_MS_SIZE	0x400166E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX379_MS_ATT0	0x400166F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX379_MS_ATT1	0x400166F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX379_MS_ATT2	0x400166F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX379_MS_ATT3	0x400166FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX380_SL_ADDR	0x40016700	Slave region, base address
PERI_MS_PPU_FX380_SL_SIZE	0x40016704	Slave region, size. See PERI_MS_PPU_FX66_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX380_SL_ATT0	0x40016710	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX380_SL_ATT1	0x40016714	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX380_SL_ATT2	0x40016718	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX380_SL_ATT3	0x4001671C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX380_MS_ADDR	0x40016720	Master region, base address
PERI_MS_PPU_FX380_MS_SIZE	0x40016724	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX380_MS_ATT0	0x40016730	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX380_MS_ATT1	0x40016734	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX380_MS_ATT2	0x40016738	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX380_MS_ATT3	0x4001673C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX381_SL_ADDR	0x40016740	Slave region, base address
PERI_MS_PPU_FX381_SL_SIZE	0x40016744	Slave region, size. See PERI_MS_PPU_FX66_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX381_SL_ATT0	0x40016750	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX381_SL_ATT1	0x40016754	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX381_SL_ATT2	0x40016758	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX381_SL_ATT3	0x4001675C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX381_MS_ADDR	0x40016760	Master region, base address
PERI_MS_PPU_FX381_MS_SIZE	0x40016764	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX381_MS_ATT0	0x40016770	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX381_MS_ATT1	0x40016774	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX381_MS_ATT2	0x40016778	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX381_MS_ATT3	0x4001677C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX382_SL_ADDR	0x40016780	Slave region, base address
PERI_MS_PPU_FX382_SL_SIZE	0x40016784	Slave region, size. See PERI_MS_PPU_FX66_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX382_SL_ATT0	0x40016790	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX382_SL_ATT1	0x40016794	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX382_SL_ATT2	0x40016798	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX382_SL_ATT3	0x4001679C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX382_MS_ADDR	0x400167A0	Master region, base address
PERI_MS_PPU_FX382_MS_SIZE	0x400167A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX382_MS_ATT0	0x400167B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX382_MS_ATT1	0x400167B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX382_MS_ATT2	0x400167B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX382_MS_ATT3	0x400167BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX383_SL_ADDR	0x400167C0	Slave region, base address
PERI_MS_PPU_FX383_SL_SIZE	0x400167C4	Slave region, size. See PERI_MS_PPU_FX66_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX383_SL_ATT0	0x400167D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX383_SL_ATT1	0x400167D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX383_SL_ATT2	0x400167D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX383_SL_ATT3	0x400167DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX383_MS_ADDR	0x400167E0	Master region, base address
PERI_MS_PPU_FX383_MS_SIZE	0x400167E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX383_MS_ATT0	0x400167F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX383_MS_ATT1	0x400167F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX383_MS_ATT2	0x400167F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX383_MS_ATT3	0x400167FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX384_SL_ADDR	0x40016800	Slave region, base address
PERI_MS_PPU_FX384_SL_SIZE	0x40016804	Slave region, size. See PERI_MS_PPU_FX66_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX384_SL_ATT0	0x40016810	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX384_SL_ATT1	0x40016814	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX384_SL_ATT2	0x40016818	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX384_SL_ATT3	0x4001681C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX384_MS_ADDR	0x40016820	Master region, base address
PERI_MS_PPU_FX384_MS_SIZE	0x40016824	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX384_MS_ATT0	0x40016830	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX384_MS_ATT1	0x40016834	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX384_MS_ATT2	0x40016838	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX384_MS_ATT3	0x4001683C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX385_SL_ADDR	0x40016840	Slave region, base address
PERI_MS_PPU_FX385_SL_SIZE	0x40016844	Slave region, size. See PERI_MS_PPU_FX66_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX385_SL_ATT0	0x40016850	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX385_SL_ATT1	0x40016854	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX385_SL_ATT2	0x40016858	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX385_SL_ATT3	0x4001685C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX385_MS_ADDR	0x40016860	Master region, base address
PERI_MS_PPU_FX385_MS_SIZE	0x40016864	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX385_MS_ATT0	0x40016870	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX385_MS_ATT1	0x40016874	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX385_MS_ATT2	0x40016878	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX385_MS_ATT3	0x4001687C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX386_SL_ADDR	0x40016880	Slave region, base address
PERI_MS_PPU_FX386_SL_SIZE	0x40016884	Slave region, size. See PERI_MS_PPU_FX66_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX386_SL_ATT0	0x40016890	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX386_SL_ATT1	0x40016894	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX386_SL_ATT2	0x40016898	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX386_SL_ATT3	0x4001689C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX386_MS_ADDR	0x400168A0	Master region, base address
PERI_MS_PPU_FX386_MS_SIZE	0x400168A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX386_MS_ATT0	0x400168B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX386_MS_ATT1	0x400168B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX386_MS_ATT2	0x400168B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX386_MS_ATT3	0x400168BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX387_SL_ADDR	0x400168C0	Slave region, base address
PERI_MS_PPU_FX387_SL_SIZE	0x400168C4	Slave region, size. See PERI_MS_PPU_FX66_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX387_SL_ATT0	0x400168D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX387_SL_ATT1	0x400168D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX387_SL_ATT2	0x400168D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX387_SL_ATT3	0x400168DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX387_MS_ADDR	0x400168E0	Master region, base address
PERI_MS_PPU_FX387_MS_SIZE	0x400168E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX387_MS_ATT0	0x400168F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX387_MS_ATT1	0x400168F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX387_MS_ATT2	0x400168F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX387_MS_ATT3	0x400168FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX388_SL_ADDR	0x40016900	Slave region, base address
PERI_MS_PPU_FX388_SL_SIZE	0x40016904	Slave region, size. See PERI_MS_PPU_FX66_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX388_SL_ATT0	0x40016910	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX388_SL_ATT1	0x40016914	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX388_SL_ATT2	0x40016918	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX388_SL_ATT3	0x4001691C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX388_MS_ADDR	0x40016920	Master region, base address
PERI_MS_PPU_FX388_MS_SIZE	0x40016924	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX388_MS_ATT0	0x40016930	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX388_MS_ATT1	0x40016934	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX388_MS_ATT2	0x40016938	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX388_MS_ATT3	0x4001693C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX389_SL_ADDR	0x40016940	Slave region, base address
PERI_MS_PPU_FX389_SL_SIZE	0x40016944	Slave region, size. See PERI_MS_PPU_FX66_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX389_SL_ATT0	0x40016950	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX389_SL_ATT1	0x40016954	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX389_SL_ATT2	0x40016958	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX389_SL_ATT3	0x4001695C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX389_MS_ADDR	0x40016960	Master region, base address
PERI_MS_PPU_FX389_MS_SIZE	0x40016964	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX389_MS_ATT0	0x40016970	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX389_MS_ATT1	0x40016974	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX389_MS_ATT2	0x40016978	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX389_MS_ATT3	0x4001697C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX390_SL_ADDR	0x40016980	Slave region, base address
PERI_MS_PPU_FX390_SL_SIZE	0x40016984	Slave region, size. See PERI_MS_PPU_FX10_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX390_SL_ATT0	0x40016990	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX390_SL_ATT1	0x40016994	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX390_SL_ATT2	0x40016998	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX390_SL_ATT3	0x4001699C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX390_MS_ADDR	0x400169A0	Master region, base address
PERI_MS_PPU_FX390_MS_SIZE	0x400169A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX390_MS_ATT0	0x400169B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX390_MS_ATT1	0x400169B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX390_MS_ATT2	0x400169B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX390_MS_ATT3	0x400169BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX391_SL_ADDR	0x400169C0	Slave region, base address
PERI_MS_PPU_FX391_SL_SIZE	0x400169C4	Slave region, size. See PERI_MS_PPU_FX10_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX391_SL_ATT0	0x400169D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX391_SL_ATT1	0x400169D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX391_SL_ATT2	0x400169D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX391_SL_ATT3	0x400169DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX391_MS_ADDR	0x400169E0	Master region, base address
PERI_MS_PPU_FX391_MS_SIZE	0x400169E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX391_MS_ATT0	0x400169F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX391_MS_ATT1	0x400169F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX391_MS_ATT2	0x400169F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX391_MS_ATT3	0x400169FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX392_SL_ADDR	0x40016A00	Slave region, base address
PERI_MS_PPU_FX392_SL_SIZE	0x40016A04	Slave region, size. See PERI_MS_PPU_FX10_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX392_SL_ATT0	0x40016A10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX392_SL_ATT1	0x40016A14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX392_SL_ATT2	0x40016A18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX392_SL_ATT3	0x40016A1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX392_MS_ADDR	0x40016A20	Master region, base address
PERI_MS_PPU_FX392_MS_SIZE	0x40016A24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX392_MS_ATT0	0x40016A30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX392_MS_ATT1	0x40016A34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX392_MS_ATT2	0x40016A38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX392_MS_ATT3	0x40016A3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX393_SL_ADDR	0x40016A40	Slave region, base address
PERI_MS_PPU_FX393_SL_SIZE	0x40016A44	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX393_SL_ATT0	0x40016A50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX393_SL_ATT1	0x40016A54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX393_SL_ATT2	0x40016A58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX393_SL_ATT3	0x40016A5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX393_MS_ADDR	0x40016A60	Master region, base address
PERI_MS_PPU_FX393_MS_SIZE	0x40016A64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX393_MS_ATT0	0x40016A70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX393_MS_ATT1	0x40016A74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX393_MS_ATT2	0x40016A78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX393_MS_ATT3	0x40016A7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX394_SL_ADDR	0x40016A80	Slave region, base address
PERI_MS_PPU_FX394_SL_SIZE	0x40016A84	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX394_SL_ATT0	0x40016A90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX394_SL_ATT1	0x40016A94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX394_SL_ATT2	0x40016A98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX394_SL_ATT3	0x40016A9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX394_MS_ADDR	0x40016AA0	Master region, base address
PERI_MS_PPU_FX394_MS_SIZE	0x40016AA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX394_MS_ATT0	0x40016AB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX394_MS_ATT1	0x40016AB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX394_MS_ATT2	0x40016AB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX394_MS_ATT3	0x40016ABC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX395_SL_ADDR	0x40016AC0	Slave region, base address
PERI_MS_PPU_FX395_SL_SIZE	0x40016AC4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX395_SL_ATT0	0x40016AD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX395_SL_ATT1	0x40016AD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX395_SL_ATT2	0x40016AD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX395_SL_ATT3	0x40016ADC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX395_MS_ADDR	0x40016AE0	Master region, base address
PERI_MS_PPU_FX395_MS_SIZE	0x40016AE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX395_MS_ATT0	0x40016AF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX395_MS_ATT1	0x40016AF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX395_MS_ATT2	0x40016AF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX395_MS_ATT3	0x40016AFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX396_SL_ADDR	0x40016B00	Slave region, base address
PERI_MS_PPU_FX396_SL_SIZE	0x40016B04	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX396_SL_ATT0	0x40016B10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX396_SL_ATT1	0x40016B14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX396_SL_ATT2	0x40016B18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX396_SL_ATT3	0x40016B1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX396_MS_ADDR	0x40016B20	Master region, base address
PERI_MS_PPU_FX396_MS_SIZE	0x40016B24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX396_MS_ATT0	0x40016B30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX396_MS_ATT1	0x40016B34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX396_MS_ATT2	0x40016B38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX396_MS_ATT3	0x40016B3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX397_SL_ADDR	0x40016B40	Slave region, base address
PERI_MS_PPU_FX397_SL_SIZE	0x40016B44	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX397_SL_ATT0	0x40016B50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX397_SL_ATT1	0x40016B54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX397_SL_ATT2	0x40016B58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX397_SL_ATT3	0x40016B5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX397_MS_ADDR	0x40016B60	Master region, base address
PERI_MS_PPU_FX397_MS_SIZE	0x40016B64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX397_MS_ATT0	0x40016B70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX397_MS_ATT1	0x40016B74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX397_MS_ATT2	0x40016B78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX397_MS_ATT3	0x40016B7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX398_SL_ADDR	0x40016B80	Slave region, base address
PERI_MS_PPU_FX398_SL_SIZE	0x40016B84	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX398_SL_ATT0	0x40016B90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX398_SL_ATT1	0x40016B94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX398_SL_ATT2	0x40016B98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX398_SL_ATT3	0x40016B9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX398_MS_ADDR	0x40016BA0	Master region, base address
PERI_MS_PPU_FX398_MS_SIZE	0x40016BA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX398_MS_ATT0	0x40016BB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX398_MS_ATT1	0x40016BB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX398_MS_ATT2	0x40016BB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX398_MS_ATT3	0x40016BBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX399_SL_ADDR	0x40016BC0	Slave region, base address
PERI_MS_PPU_FX399_SL_SIZE	0x40016BC4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX399_SL_ATT0	0x40016BD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX399_SL_ATT1	0x40016BD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX399_SL_ATT2	0x40016BD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX399_SL_ATT3	0x40016BDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX399_MS_ADDR	0x40016BE0	Master region, base address
PERI_MS_PPU_FX399_MS_SIZE	0x40016BE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX399_MS_ATT0	0x40016BF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX399_MS_ATT1	0x40016BF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX399_MS_ATT2	0x40016BF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX399_MS_ATT3	0x40016BFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX400_SL_ADDR	0x40016C00	Slave region, base address
PERI_MS_PPU_FX400_SL_SIZE	0x40016C04	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX400_SL_ATT0	0x40016C10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX400_SL_ATT1	0x40016C14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX400_SL_ATT2	0x40016C18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX400_SL_ATT3	0x40016C1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX400_MS_ADDR	0x40016C20	Master region, base address
PERI_MS_PPU_FX400_MS_SIZE	0x40016C24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX400_MS_ATT0	0x40016C30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX400_MS_ATT1	0x40016C34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX400_MS_ATT2	0x40016C38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX400_MS_ATT3	0x40016C3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX401_SL_ADDR	0x40016C40	Slave region, base address
PERI_MS_PPU_FX401_SL_SIZE	0x40016C44	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX401_SL_ATT0	0x40016C50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX401_SL_ATT1	0x40016C54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX401_SL_ATT2	0x40016C58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX401_SL_ATT3	0x40016C5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX401_MS_ADDR	0x40016C60	Master region, base address
PERI_MS_PPU_FX401_MS_SIZE	0x40016C64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX401_MS_ATT0	0x40016C70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX401_MS_ATT1	0x40016C74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX401_MS_ATT2	0x40016C78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX401_MS_ATT3	0x40016C7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX402_SL_ADDR	0x40016C80	Slave region, base address
PERI_MS_PPU_FX402_SL_SIZE	0x40016C84	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX402_SL_ATT0	0x40016C90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX402_SL_ATT1	0x40016C94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX402_SL_ATT2	0x40016C98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX402_SL_ATT3	0x40016C9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX402_MS_ADDR	0x40016CA0	Master region, base address
PERI_MS_PPU_FX402_MS_SIZE	0x40016CA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX402_MS_ATT0	0x40016CB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX402_MS_ATT1	0x40016CB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX402_MS_ATT2	0x40016CB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX402_MS_ATT3	0x40016CBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX403_SL_ADDR	0x40016CC0	Slave region, base address
PERI_MS_PPU_FX403_SL_SIZE	0x40016CC4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX403_SL_ATT0	0x40016CD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX403_SL_ATT1	0x40016CD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX403_SL_ATT2	0x40016CD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX403_SL_ATT3	0x40016CDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX403_MS_ADDR	0x40016CE0	Master region, base address
PERI_MS_PPU_FX403_MS_SIZE	0x40016CE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX403_MS_ATT0	0x40016CF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX403_MS_ATT1	0x40016CF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX403_MS_ATT2	0x40016CF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX403_MS_ATT3	0x40016CFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX404_SL_ADDR	0x40016D00	Slave region, base address
PERI_MS_PPU_FX404_SL_SIZE	0x40016D04	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX404_SL_ATT0	0x40016D10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX404_SL_ATT1	0x40016D14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX404_SL_ATT2	0x40016D18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX404_SL_ATT3	0x40016D1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX404_MS_ADDR	0x40016D20	Master region, base address
PERI_MS_PPU_FX404_MS_SIZE	0x40016D24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX404_MS_ATT0	0x40016D30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX404_MS_ATT1	0x40016D34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX404_MS_ATT2	0x40016D38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX404_MS_ATT3	0x40016D3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX405_SL_ADDR	0x40016D40	Slave region, base address
PERI_MS_PPU_FX405_SL_SIZE	0x40016D44	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX405_SL_ATT0	0x40016D50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX405_SL_ATT1	0x40016D54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX405_SL_ATT2	0x40016D58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX405_SL_ATT3	0x40016D5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX405_MS_ADDR	0x40016D60	Master region, base address
PERI_MS_PPU_FX405_MS_SIZE	0x40016D64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX405_MS_ATT0	0x40016D70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX405_MS_ATT1	0x40016D74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX405_MS_ATT2	0x40016D78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX405_MS_ATT3	0x40016D7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX406_SL_ADDR	0x40016D80	Slave region, base address
PERI_MS_PPU_FX406_SL_SIZE	0x40016D84	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX406_SL_ATT0	0x40016D90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX406_SL_ATT1	0x40016D94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX406_SL_ATT2	0x40016D98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX406_SL_ATT3	0x40016D9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX406_MS_ADDR	0x40016DA0	Master region, base address
PERI_MS_PPU_FX406_MS_SIZE	0x40016DA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX406_MS_ATT0	0x40016DB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX406_MS_ATT1	0x40016DB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX406_MS_ATT2	0x40016DB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX406_MS_ATT3	0x40016DBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX407_SL_ADDR	0x40016DC0	Slave region, base address
PERI_MS_PPU_FX407_SL_SIZE	0x40016DC4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX407_SL_ATT0	0x40016DD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX407_SL_ATT1	0x40016DD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX407_SL_ATT2	0x40016DD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX407_SL_ATT3	0x40016DDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX407_MS_ADDR	0x40016DE0	Master region, base address
PERI_MS_PPU_FX407_MS_SIZE	0x40016DE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX407_MS_ATT0	0x40016DF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX407_MS_ATT1	0x40016DF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX407_MS_ATT2	0x40016DF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX407_MS_ATT3	0x40016DFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX408_SL_ADDR	0x40016E00	Slave region, base address
PERI_MS_PPU_FX408_SL_SIZE	0x40016E04	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX408_SL_ATT0	0x40016E10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX408_SL_ATT1	0x40016E14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX408_SL_ATT2	0x40016E18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX408_SL_ATT3	0x40016E1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX408_MS_ADDR	0x40016E20	Master region, base address
PERI_MS_PPU_FX408_MS_SIZE	0x40016E24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX408_MS_ATT0	0x40016E30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX408_MS_ATT1	0x40016E34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX408_MS_ATT2	0x40016E38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX408_MS_ATT3	0x40016E3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX409_SL_ADDR	0x40016E40	Slave region, base address
PERI_MS_PPU_FX409_SL_SIZE	0x40016E44	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX409_SL_ATT0	0x40016E50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX409_SL_ATT1	0x40016E54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX409_SL_ATT2	0x40016E58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX409_SL_ATT3	0x40016E5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX409_MS_ADDR	0x40016E60	Master region, base address
PERI_MS_PPU_FX409_MS_SIZE	0x40016E64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX409_MS_ATT0	0x40016E70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX409_MS_ATT1	0x40016E74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX409_MS_ATT2	0x40016E78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX409_MS_ATT3	0x40016E7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX410_SL_ADDR	0x40016E80	Slave region, base address
PERI_MS_PPU_FX410_SL_SIZE	0x40016E84	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX410_SL_ATT0	0x40016E90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX410_SL_ATT1	0x40016E94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX410_SL_ATT2	0x40016E98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX410_SL_ATT3	0x40016E9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX410_MS_ADDR	0x40016EA0	Master region, base address
PERI_MS_PPU_FX410_MS_SIZE	0x40016EA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX410_MS_ATT0	0x40016EB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX410_MS_ATT1	0x40016EB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX410_MS_ATT2	0x40016EB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX410_MS_ATT3	0x40016EBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX411_SL_ADDR	0x40016EC0	Slave region, base address
PERI_MS_PPU_FX411_SL_SIZE	0x40016EC4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX411_SL_ATT0	0x40016ED0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX411_SL_ATT1	0x40016ED4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX411_SL_ATT2	0x40016ED8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX411_SL_ATT3	0x40016EDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX411_MS_ADDR	0x40016EE0	Master region, base address
PERI_MS_PPU_FX411_MS_SIZE	0x40016EE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX411_MS_ATT0	0x40016EF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX411_MS_ATT1	0x40016EF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX411_MS_ATT2	0x40016EF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX411_MS_ATT3	0x40016EFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX412_SL_ADDR	0x40016F00	Slave region, base address
PERI_MS_PPU_FX412_SL_SIZE	0x40016F04	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX412_SL_ATT0	0x40016F10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX412_SL_ATT1	0x40016F14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX412_SL_ATT2	0x40016F18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX412_SL_ATT3	0x40016F1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX412_MS_ADDR	0x40016F20	Master region, base address
PERI_MS_PPU_FX412_MS_SIZE	0x40016F24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX412_MS_ATT0	0x40016F30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX412_MS_ATT1	0x40016F34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX412_MS_ATT2	0x40016F38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX412_MS_ATT3	0x40016F3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX413_SL_ADDR	0x40016F40	Slave region, base address
PERI_MS_PPU_FX413_SL_SIZE	0x40016F44	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX413_SL_ATT0	0x40016F50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX413_SL_ATT1	0x40016F54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX413_SL_ATT2	0x40016F58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX413_SL_ATT3	0x40016F5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX413_MS_ADDR	0x40016F60	Master region, base address
PERI_MS_PPU_FX413_MS_SIZE	0x40016F64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX413_MS_ATT0	0x40016F70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX413_MS_ATT1	0x40016F74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX413_MS_ATT2	0x40016F78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX413_MS_ATT3	0x40016F7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX414_SL_ADDR	0x40016F80	Slave region, base address
PERI_MS_PPU_FX414_SL_SIZE	0x40016F84	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX414_SL_ATT0	0x40016F90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX414_SL_ATT1	0x40016F94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX414_SL_ATT2	0x40016F98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX414_SL_ATT3	0x40016F9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX414_MS_ADDR	0x40016FA0	Master region, base address
PERI_MS_PPU_FX414_MS_SIZE	0x40016FA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX414_MS_ATT0	0x40016FB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX414_MS_ATT1	0x40016FB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX414_MS_ATT2	0x40016FB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX414_MS_ATT3	0x40016FBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX415_SL_ADDR	0x40016FC0	Slave region, base address
PERI_MS_PPU_FX415_SL_SIZE	0x40016FC4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX415_SL_ATT0	0x40016FD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX415_SL_ATT1	0x40016FD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX415_SL_ATT2	0x40016FD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX415_SL_ATT3	0x40016FDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX415_MS_ADDR	0x40016FE0	Master region, base address
PERI_MS_PPU_FX415_MS_SIZE	0x40016FE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX415_MS_ATT0	0x40016FF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX415_MS_ATT1	0x40016FF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX415_MS_ATT2	0x40016FF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX415_MS_ATT3	0x40016FFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX416_SL_ADDR	0x40017000	Slave region, base address
PERI_MS_PPU_FX416_SL_SIZE	0x40017004	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX416_SL_ATT0	0x40017010	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX416_SL_ATT1	0x40017014	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX416_SL_ATT2	0x40017018	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX416_SL_ATT3	0x4001701C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX416_MS_ADDR	0x40017020	Master region, base address
PERI_MS_PPU_FX416_MS_SIZE	0x40017024	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX416_MS_ATT0	0x40017030	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX416_MS_ATT1	0x40017034	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX416_MS_ATT2	0x40017038	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX416_MS_ATT3	0x4001703C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX417_SL_ADDR	0x40017040	Slave region, base address
PERI_MS_PPU_FX417_SL_SIZE	0x40017044	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX417_SL_ATT0	0x40017050	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX417_SL_ATT1	0x40017054	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX417_SL_ATT2	0x40017058	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX417_SL_ATT3	0x4001705C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX417_MS_ADDR	0x40017060	Master region, base address
PERI_MS_PPU_FX417_MS_SIZE	0x40017064	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX417_MS_ATT0	0x40017070	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX417_MS_ATT1	0x40017074	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX417_MS_ATT2	0x40017078	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX417_MS_ATT3	0x4001707C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX418_SL_ADDR	0x40017080	Slave region, base address
PERI_MS_PPU_FX418_SL_SIZE	0x40017084	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX418_SL_ATT0	0x40017090	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX418_SL_ATT1	0x40017094	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX418_SL_ATT2	0x40017098	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX418_SL_ATT3	0x4001709C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX418_MS_ADDR	0x400170A0	Master region, base address
PERI_MS_PPU_FX418_MS_SIZE	0x400170A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX418_MS_ATT0	0x400170B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX418_MS_ATT1	0x400170B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX418_MS_ATT2	0x400170B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX418_MS_ATT3	0x400170BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX419_SL_ADDR	0x400170C0	Slave region, base address
PERI_MS_PPU_FX419_SL_SIZE	0x400170C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX419_SL_ATT0	0x400170D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX419_SL_ATT1	0x400170D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX419_SL_ATT2	0x400170D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX419_SL_ATT3	0x400170DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX419_MS_ADDR	0x400170E0	Master region, base address
PERI_MS_PPU_FX419_MS_SIZE	0x400170E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX419_MS_ATT0	0x400170F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX419_MS_ATT1	0x400170F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX419_MS_ATT2	0x400170F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX419_MS_ATT3	0x400170FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX420_SL_ADDR	0x40017100	Slave region, base address
PERI_MS_PPU_FX420_SL_SIZE	0x40017104	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX420_SL_ATT0	0x40017110	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX420_SL_ATT1	0x40017114	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX420_SL_ATT2	0x40017118	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX420_SL_ATT3	0x4001711C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX420_MS_ADDR	0x40017120	Master region, base address
PERI_MS_PPU_FX420_MS_SIZE	0x40017124	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX420_MS_ATT0	0x40017130	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX420_MS_ATT1	0x40017134	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX420_MS_ATT2	0x40017138	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX420_MS_ATT3	0x4001713C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX421_SL_ADDR	0x40017140	Slave region, base address
PERI_MS_PPU_FX421_SL_SIZE	0x40017144	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX421_SL_ATT0	0x40017150	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX421_SL_ATT1	0x40017154	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX421_SL_ATT2	0x40017158	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX421_SL_ATT3	0x4001715C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX421_MS_ADDR	0x40017160	Master region, base address
PERI_MS_PPU_FX421_MS_SIZE	0x40017164	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX421_MS_ATT0	0x40017170	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX421_MS_ATT1	0x40017174	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX421_MS_ATT2	0x40017178	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX421_MS_ATT3	0x4001717C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX422_SL_ADDR	0x40017180	Slave region, base address
PERI_MS_PPU_FX422_SL_SIZE	0x40017184	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX422_SL_ATT0	0x40017190	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX422_SL_ATT1	0x40017194	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX422_SL_ATT2	0x40017198	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX422_SL_ATT3	0x4001719C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX422_MS_ADDR	0x400171A0	Master region, base address
PERI_MS_PPU_FX422_MS_SIZE	0x400171A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX422_MS_ATT0	0x400171B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX422_MS_ATT1	0x400171B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX422_MS_ATT2	0x400171B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX422_MS_ATT3	0x400171BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX423_SL_ADDR	0x400171C0	Slave region, base address
PERI_MS_PPU_FX423_SL_SIZE	0x400171C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX423_SL_ATT0	0x400171D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX423_SL_ATT1	0x400171D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX423_SL_ATT2	0x400171D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX423_SL_ATT3	0x400171DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX423_MS_ADDR	0x400171E0	Master region, base address
PERI_MS_PPU_FX423_MS_SIZE	0x400171E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX423_MS_ATT0	0x400171F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX423_MS_ATT1	0x400171F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX423_MS_ATT2	0x400171F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX423_MS_ATT3	0x400171FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX424_SL_ADDR	0x40017200	Slave region, base address
PERI_MS_PPU_FX424_SL_SIZE	0x40017204	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX424_SL_ATT0	0x40017210	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX424_SL_ATT1	0x40017214	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX424_SL_ATT2	0x40017218	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX424_SL_ATT3	0x4001721C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX424_MS_ADDR	0x40017220	Master region, base address
PERI_MS_PPU_FX424_MS_SIZE	0x40017224	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX424_MS_ATT0	0x40017230	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX424_MS_ATT1	0x40017234	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX424_MS_ATT2	0x40017238	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX424_MS_ATT3	0x4001723C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX425_SL_ADDR	0x40017240	Slave region, base address
PERI_MS_PPU_FX425_SL_SIZE	0x40017244	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX425_SL_ATT0	0x40017250	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX425_SL_ATT1	0x40017254	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX425_SL_ATT2	0x40017258	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX425_SL_ATT3	0x4001725C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX425_MS_ADDR	0x40017260	Master region, base address
PERI_MS_PPU_FX425_MS_SIZE	0x40017264	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX425_MS_ATT0	0x40017270	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX425_MS_ATT1	0x40017274	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX425_MS_ATT2	0x40017278	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX425_MS_ATT3	0x4001727C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX426_SL_ADDR	0x40017280	Slave region, base address
PERI_MS_PPU_FX426_SL_SIZE	0x40017284	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX426_SL_ATT0	0x40017290	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX426_SL_ATT1	0x40017294	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX426_SL_ATT2	0x40017298	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX426_SL_ATT3	0x4001729C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX426_MS_ADDR	0x400172A0	Master region, base address
PERI_MS_PPU_FX426_MS_SIZE	0x400172A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX426_MS_ATT0	0x400172B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX426_MS_ATT1	0x400172B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX426_MS_ATT2	0x400172B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX426_MS_ATT3	0x400172BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX427_SL_ADDR	0x400172C0	Slave region, base address
PERI_MS_PPU_FX427_SL_SIZE	0x400172C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX427_SL_ATT0	0x400172D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX427_SL_ATT1	0x400172D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX427_SL_ATT2	0x400172D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX427_SL_ATT3	0x400172DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX427_MS_ADDR	0x400172E0	Master region, base address
PERI_MS_PPU_FX427_MS_SIZE	0x400172E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX427_MS_ATT0	0x400172F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX427_MS_ATT1	0x400172F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX427_MS_ATT2	0x400172F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX427_MS_ATT3	0x400172FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX428_SL_ADDR	0x40017300	Slave region, base address
PERI_MS_PPU_FX428_SL_SIZE	0x40017304	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX428_SL_ATT0	0x40017310	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX428_SL_ATT1	0x40017314	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX428_SL_ATT2	0x40017318	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX428_SL_ATT3	0x4001731C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX428_MS_ADDR	0x40017320	Master region, base address
PERI_MS_PPU_FX428_MS_SIZE	0x40017324	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX428_MS_ATT0	0x40017330	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX428_MS_ATT1	0x40017334	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX428_MS_ATT2	0x40017338	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX428_MS_ATT3	0x4001733C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX429_SL_ADDR	0x40017340	Slave region, base address
PERI_MS_PPU_FX429_SL_SIZE	0x40017344	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX429_SL_ATT0	0x40017350	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX429_SL_ATT1	0x40017354	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX429_SL_ATT2	0x40017358	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX429_SL_ATT3	0x4001735C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX429_MS_ADDR	0x40017360	Master region, base address
PERI_MS_PPU_FX429_MS_SIZE	0x40017364	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX429_MS_ATT0	0x40017370	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX429_MS_ATT1	0x40017374	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX429_MS_ATT2	0x40017378	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX429_MS_ATT3	0x4001737C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX430_SL_ADDR	0x40017380	Slave region, base address
PERI_MS_PPU_FX430_SL_SIZE	0x40017384	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX430_SL_ATT0	0x40017390	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX430_SL_ATT1	0x40017394	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX430_SL_ATT2	0x40017398	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX430_SL_ATT3	0x4001739C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX430_MS_ADDR	0x400173A0	Master region, base address
PERI_MS_PPU_FX430_MS_SIZE	0x400173A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX430_MS_ATT0	0x400173B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX430_MS_ATT1	0x400173B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX430_MS_ATT2	0x400173B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX430_MS_ATT3	0x400173BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX431_SL_ADDR	0x400173C0	Slave region, base address
PERI_MS_PPU_FX431_SL_SIZE	0x400173C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX431_SL_ATT0	0x400173D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX431_SL_ATT1	0x400173D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX431_SL_ATT2	0x400173D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX431_SL_ATT3	0x400173DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX431_MS_ADDR	0x400173E0	Master region, base address
PERI_MS_PPU_FX431_MS_SIZE	0x400173E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX431_MS_ATT0	0x400173F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX431_MS_ATT1	0x400173F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX431_MS_ATT2	0x400173F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX431_MS_ATT3	0x400173FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX432_SL_ADDR	0x40017400	Slave region, base address
PERI_MS_PPU_FX432_SL_SIZE	0x40017404	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX432_SL_ATT0	0x40017410	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX432_SL_ATT1	0x40017414	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX432_SL_ATT2	0x40017418	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX432_SL_ATT3	0x4001741C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX432_MS_ADDR	0x40017420	Master region, base address
PERI_MS_PPU_FX432_MS_SIZE	0x40017424	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX432_MS_ATT0	0x40017430	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX432_MS_ATT1	0x40017434	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX432_MS_ATT2	0x40017438	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX432_MS_ATT3	0x4001743C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX433_SL_ADDR	0x40017440	Slave region, base address
PERI_MS_PPU_FX433_SL_SIZE	0x40017444	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX433_SL_ATT0	0x40017450	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX433_SL_ATT1	0x40017454	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX433_SL_ATT2	0x40017458	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX433_SL_ATT3	0x4001745C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX433_MS_ADDR	0x40017460	Master region, base address
PERI_MS_PPU_FX433_MS_SIZE	0x40017464	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX433_MS_ATT0	0x40017470	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX433_MS_ATT1	0x40017474	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX433_MS_ATT2	0x40017478	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX433_MS_ATT3	0x4001747C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX434_SL_ADDR	0x40017480	Slave region, base address
PERI_MS_PPU_FX434_SL_SIZE	0x40017484	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX434_SL_ATT0	0x40017490	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX434_SL_ATT1	0x40017494	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX434_SL_ATT2	0x40017498	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX434_SL_ATT3	0x4001749C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX434_MS_ADDR	0x400174A0	Master region, base address
PERI_MS_PPU_FX434_MS_SIZE	0x400174A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX434_MS_ATT0	0x400174B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX434_MS_ATT1	0x400174B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX434_MS_ATT2	0x400174B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX434_MS_ATT3	0x400174BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX435_SL_ADDR	0x400174C0	Slave region, base address
PERI_MS_PPU_FX435_SL_SIZE	0x400174C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX435_SL_ATT0	0x400174D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX435_SL_ATT1	0x400174D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX435_SL_ATT2	0x400174D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX435_SL_ATT3	0x400174DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX435_MS_ADDR	0x400174E0	Master region, base address
PERI_MS_PPU_FX435_MS_SIZE	0x400174E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX435_MS_ATT0	0x400174F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX435_MS_ATT1	0x400174F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX435_MS_ATT2	0x400174F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX435_MS_ATT3	0x400174FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX436_SL_ADDR	0x40017500	Slave region, base address
PERI_MS_PPU_FX436_SL_SIZE	0x40017504	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX436_SL_ATT0	0x40017510	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX436_SL_ATT1	0x40017514	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX436_SL_ATT2	0x40017518	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX436_SL_ATT3	0x4001751C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX436_MS_ADDR	0x40017520	Master region, base address
PERI_MS_PPU_FX436_MS_SIZE	0x40017524	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX436_MS_ATT0	0x40017530	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX436_MS_ATT1	0x40017534	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX436_MS_ATT2	0x40017538	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX436_MS_ATT3	0x4001753C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX437_SL_ADDR	0x40017540	Slave region, base address
PERI_MS_PPU_FX437_SL_SIZE	0x40017544	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX437_SL_ATT0	0x40017550	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX437_SL_ATT1	0x40017554	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX437_SL_ATT2	0x40017558	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX437_SL_ATT3	0x4001755C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX437_MS_ADDR	0x40017560	Master region, base address
PERI_MS_PPU_FX437_MS_SIZE	0x40017564	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX437_MS_ATT0	0x40017570	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX437_MS_ATT1	0x40017574	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX437_MS_ATT2	0x40017578	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX437_MS_ATT3	0x4001757C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX438_SL_ADDR	0x40017580	Slave region, base address
PERI_MS_PPU_FX438_SL_SIZE	0x40017584	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX438_SL_ATT0	0x40017590	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX438_SL_ATT1	0x40017594	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX438_SL_ATT2	0x40017598	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX438_SL_ATT3	0x4001759C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX438_MS_ADDR	0x400175A0	Master region, base address
PERI_MS_PPU_FX438_MS_SIZE	0x400175A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX438_MS_ATT0	0x400175B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX438_MS_ATT1	0x400175B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX438_MS_ATT2	0x400175B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX438_MS_ATT3	0x400175BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX439_SL_ADDR	0x400175C0	Slave region, base address
PERI_MS_PPU_FX439_SL_SIZE	0x400175C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX439_SL_ATT0	0x400175D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX439_SL_ATT1	0x400175D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX439_SL_ATT2	0x400175D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX439_SL_ATT3	0x400175DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX439_MS_ADDR	0x400175E0	Master region, base address
PERI_MS_PPU_FX439_MS_SIZE	0x400175E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX439_MS_ATT0	0x400175F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX439_MS_ATT1	0x400175F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX439_MS_ATT2	0x400175F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX439_MS_ATT3	0x400175FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX440_SL_ADDR	0x40017600	Slave region, base address
PERI_MS_PPU_FX440_SL_SIZE	0x40017604	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX440_SL_ATT0	0x40017610	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX440_SL_ATT1	0x40017614	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX440_SL_ATT2	0x40017618	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX440_SL_ATT3	0x4001761C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX440_MS_ADDR	0x40017620	Master region, base address
PERI_MS_PPU_FX440_MS_SIZE	0x40017624	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX440_MS_ATT0	0x40017630	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX440_MS_ATT1	0x40017634	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX440_MS_ATT2	0x40017638	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX440_MS_ATT3	0x4001763C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX441_SL_ADDR	0x40017640	Slave region, base address
PERI_MS_PPU_FX441_SL_SIZE	0x40017644	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX441_SL_ATT0	0x40017650	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX441_SL_ATT1	0x40017654	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX441_SL_ATT2	0x40017658	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX441_SL_ATT3	0x4001765C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX441_MS_ADDR	0x40017660	Master region, base address
PERI_MS_PPU_FX441_MS_SIZE	0x40017664	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX441_MS_ATT0	0x40017670	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX441_MS_ATT1	0x40017674	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX441_MS_ATT2	0x40017678	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX441_MS_ATT3	0x4001767C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX442_SL_ADDR	0x40017680	Slave region, base address
PERI_MS_PPU_FX442_SL_SIZE	0x40017684	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX442_SL_ATT0	0x40017690	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX442_SL_ATT1	0x40017694	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX442_SL_ATT2	0x40017698	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX442_SL_ATT3	0x4001769C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX442_MS_ADDR	0x400176A0	Master region, base address
PERI_MS_PPU_FX442_MS_SIZE	0x400176A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX442_MS_ATT0	0x400176B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX442_MS_ATT1	0x400176B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX442_MS_ATT2	0x400176B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX442_MS_ATT3	0x400176BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX443_SL_ADDR	0x400176C0	Slave region, base address
PERI_MS_PPU_FX443_SL_SIZE	0x400176C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX443_SL_ATT0	0x400176D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX443_SL_ATT1	0x400176D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX443_SL_ATT2	0x400176D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX443_SL_ATT3	0x400176DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX443_MS_ADDR	0x400176E0	Master region, base address
PERI_MS_PPU_FX443_MS_SIZE	0x400176E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX443_MS_ATT0	0x400176F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX443_MS_ATT1	0x400176F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX443_MS_ATT2	0x400176F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX443_MS_ATT3	0x400176FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX444_SL_ADDR	0x40017700	Slave region, base address
PERI_MS_PPU_FX444_SL_SIZE	0x40017704	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX444_SL_ATT0	0x40017710	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX444_SL_ATT1	0x40017714	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX444_SL_ATT2	0x40017718	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX444_SL_ATT3	0x4001771C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX444_MS_ADDR	0x40017720	Master region, base address
PERI_MS_PPU_FX444_MS_SIZE	0x40017724	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX444_MS_ATT0	0x40017730	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX444_MS_ATT1	0x40017734	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX444_MS_ATT2	0x40017738	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX444_MS_ATT3	0x4001773C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX445_SL_ADDR	0x40017740	Slave region, base address
PERI_MS_PPU_FX445_SL_SIZE	0x40017744	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX445_SL_ATT0	0x40017750	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX445_SL_ATT1	0x40017754	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX445_SL_ATT2	0x40017758	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX445_SL_ATT3	0x4001775C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX445_MS_ADDR	0x40017760	Master region, base address
PERI_MS_PPU_FX445_MS_SIZE	0x40017764	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX445_MS_ATT0	0x40017770	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX445_MS_ATT1	0x40017774	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX445_MS_ATT2	0x40017778	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX445_MS_ATT3	0x4001777C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX446_SL_ADDR	0x40017780	Slave region, base address
PERI_MS_PPU_FX446_SL_SIZE	0x40017784	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX446_SL_ATT0	0x40017790	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX446_SL_ATT1	0x40017794	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX446_SL_ATT2	0x40017798	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX446_SL_ATT3	0x4001779C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX446_MS_ADDR	0x400177A0	Master region, base address
PERI_MS_PPU_FX446_MS_SIZE	0x400177A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX446_MS_ATT0	0x400177B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX446_MS_ATT1	0x400177B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX446_MS_ATT2	0x400177B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX446_MS_ATT3	0x400177BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX447_SL_ADDR	0x400177C0	Slave region, base address
PERI_MS_PPU_FX447_SL_SIZE	0x400177C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX447_SL_ATT0	0x400177D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX447_SL_ATT1	0x400177D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX447_SL_ATT2	0x400177D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX447_SL_ATT3	0x400177DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX447_MS_ADDR	0x400177E0	Master region, base address
PERI_MS_PPU_FX447_MS_SIZE	0x400177E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX447_MS_ATT0	0x400177F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX447_MS_ATT1	0x400177F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX447_MS_ATT2	0x400177F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX447_MS_ATT3	0x400177FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX448_SL_ADDR	0x40017800	Slave region, base address
PERI_MS_PPU_FX448_SL_SIZE	0x40017804	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX448_SL_ATT0	0x40017810	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX448_SL_ATT1	0x40017814	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX448_SL_ATT2	0x40017818	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX448_SL_ATT3	0x4001781C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX448_MS_ADDR	0x40017820	Master region, base address
PERI_MS_PPU_FX448_MS_SIZE	0x40017824	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX448_MS_ATT0	0x40017830	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX448_MS_ATT1	0x40017834	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX448_MS_ATT2	0x40017838	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX448_MS_ATT3	0x4001783C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX449_SL_ADDR	0x40017840	Slave region, base address
PERI_MS_PPU_FX449_SL_SIZE	0x40017844	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX449_SL_ATT0	0x40017850	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX449_SL_ATT1	0x40017854	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX449_SL_ATT2	0x40017858	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX449_SL_ATT3	0x4001785C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX449_MS_ADDR	0x40017860	Master region, base address
PERI_MS_PPU_FX449_MS_SIZE	0x40017864	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX449_MS_ATT0	0x40017870	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX449_MS_ATT1	0x40017874	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX449_MS_ATT2	0x40017878	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX449_MS_ATT3	0x4001787C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX450_SL_ADDR	0x40017880	Slave region, base address
PERI_MS_PPU_FX450_SL_SIZE	0x40017884	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX450_SL_ATT0	0x40017890	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX450_SL_ATT1	0x40017894	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX450_SL_ATT2	0x40017898	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX450_SL_ATT3	0x4001789C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX450_MS_ADDR	0x400178A0	Master region, base address
PERI_MS_PPU_FX450_MS_SIZE	0x400178A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX450_MS_ATT0	0x400178B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX450_MS_ATT1	0x400178B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX450_MS_ATT2	0x400178B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX450_MS_ATT3	0x400178BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX451_SL_ADDR	0x400178C0	Slave region, base address
PERI_MS_PPU_FX451_SL_SIZE	0x400178C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX451_SL_ATT0	0x400178D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX451_SL_ATT1	0x400178D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX451_SL_ATT2	0x400178D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX451_SL_ATT3	0x400178DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX451_MS_ADDR	0x400178E0	Master region, base address
PERI_MS_PPU_FX451_MS_SIZE	0x400178E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX451_MS_ATT0	0x400178F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX451_MS_ATT1	0x400178F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX451_MS_ATT2	0x400178F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX451_MS_ATT3	0x400178FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX452_SL_ADDR	0x40017900	Slave region, base address
PERI_MS_PPU_FX452_SL_SIZE	0x40017904	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX452_SL_ATT0	0x40017910	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX452_SL_ATT1	0x40017914	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX452_SL_ATT2	0x40017918	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX452_SL_ATT3	0x4001791C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX452_MS_ADDR	0x40017920	Master region, base address
PERI_MS_PPU_FX452_MS_SIZE	0x40017924	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX452_MS_ATT0	0x40017930	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX452_MS_ATT1	0x40017934	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX452_MS_ATT2	0x40017938	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX452_MS_ATT3	0x4001793C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX453_SL_ADDR	0x40017940	Slave region, base address
PERI_MS_PPU_FX453_SL_SIZE	0x40017944	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX453_SL_ATT0	0x40017950	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX453_SL_ATT1	0x40017954	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX453_SL_ATT2	0x40017958	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX453_SL_ATT3	0x4001795C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX453_MS_ADDR	0x40017960	Master region, base address
PERI_MS_PPU_FX453_MS_SIZE	0x40017964	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX453_MS_ATT0	0x40017970	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX453_MS_ATT1	0x40017974	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX453_MS_ATT2	0x40017978	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX453_MS_ATT3	0x4001797C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX454_SL_ADDR	0x40017980	Slave region, base address
PERI_MS_PPU_FX454_SL_SIZE	0x40017984	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX454_SL_ATT0	0x40017990	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX454_SL_ATT1	0x40017994	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX454_SL_ATT2	0x40017998	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX454_SL_ATT3	0x4001799C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX454_MS_ADDR	0x400179A0	Master region, base address
PERI_MS_PPU_FX454_MS_SIZE	0x400179A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX454_MS_ATT0	0x400179B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX454_MS_ATT1	0x400179B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX454_MS_ATT2	0x400179B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX454_MS_ATT3	0x400179BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX455_SL_ADDR	0x400179C0	Slave region, base address
PERI_MS_PPU_FX455_SL_SIZE	0x400179C4	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX455_SL_ATT0	0x400179D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX455_SL_ATT1	0x400179D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX455_SL_ATT2	0x400179D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX455_SL_ATT3	0x400179DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX455_MS_ADDR	0x400179E0	Master region, base address
PERI_MS_PPU_FX455_MS_SIZE	0x400179E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX455_MS_ATT0	0x400179F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX455_MS_ATT1	0x400179F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX455_MS_ATT2	0x400179F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX455_MS_ATT3	0x400179FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX456_SL_ADDR	0x40017A00	Slave region, base address
PERI_MS_PPU_FX456_SL_SIZE	0x40017A04	Slave region, size. See PERI_MS_PPU_FX41_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX456_SL_ATT0	0x40017A10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX456_SL_ATT1	0x40017A14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX456_SL_ATT2	0x40017A18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX456_SL_ATT3	0x40017A1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX456_MS_ADDR	0x40017A20	Master region, base address
PERI_MS_PPU_FX456_MS_SIZE	0x40017A24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX456_MS_ATT0	0x40017A30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX456_MS_ATT1	0x40017A34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX456_MS_ATT2	0x40017A38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX456_MS_ATT3	0x40017A3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX457_SL_ADDR	0x40017A40	Slave region, base address
PERI_MS_PPU_FX457_SL_SIZE	0x40017A44	Slave region, size. See PERI_MS_PPU_FX17_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX457_SL_ATT0	0x40017A50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX457_SL_ATT1	0x40017A54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX457_SL_ATT2	0x40017A58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX457_SL_ATT3	0x40017A5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX457_MS_ADDR	0x40017A60	Master region, base address
PERI_MS_PPU_FX457_MS_SIZE	0x40017A64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX457_MS_ATT0	0x40017A70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX457_MS_ATT1	0x40017A74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.

Register name	Address	Description
PERI_MS_PPU_FX457_MS_ATT2	0x40017A78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX457_MS_ATT3	0x40017A7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.

9.1 Peripheral registers

PERI_TIMEOUT_CTL

Timeout control
Address: 0x40000200
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TIMEOUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TIMEOUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

15 : 0	TIMEOUT	This field specifies a number of clock cycles (clk_slow). If an AHB-Lite bus transfer takes more than the specified number of cycles (timeout detection), the bus transfer is terminated with an AHB-Lite bus error and a fault is generated (and possibly recorded in the fault report structure(s)). "0x0000"-"0xfffe": Number of clock cycles. "0xffff": This value is the default/reset value and specifies that no timeout detection is performed: a bus transfer will never be terminated and a fault will never be generated. Default Value: 0xFFFF

PERI_TR_CMD

Trigger command
Address: 0x40000220
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TR_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			GROUP_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	None				
HW Access	RW1C	R	R	None				
Name	ACTIVATE	OUT_SEL	TR_EDGE	None [28:24]				

Bits	Name	Description
31	ACTIVATE	SW sets this field to '1' to activate (set to '1') a trigger as identified by TR_SEL, TR_EDGE and OUT_SEL. HW sets this field to '0' for edge sensitive triggers AFTER the selected trigger is activated for two clk_peri cycles. Note: when ACTIVATE is '1', SW should not modify the other register fields. SW MUST NOT set ACTIVATE bit to '1' while updating the other register bits simultaneously. At first the SW MUST update the other register bits as needed, and then set ACTIVATE to '1' with a new register write. Default Value: 0

30	OUT_SEL	Specifies whether trigger activation is for a specific input or output trigger of the trigger multiplexer. Activation of a specific input trigger, will result in activation of all output triggers that have the specific input trigger selected through their TR_OUT_CTL.TR_SEL field. Activation of a specific output trigger, will result in activation of the specified TR_SEL output trigger only. '0': TR_SEL selection and trigger activation is for an input trigger to the trigger multiplexer. '1': TR_SEL selection and trigger activation is for an output trigger from the trigger multiplexer. Note: this field is not used for trigger 1-to-1 groups. Default Value: 0
29	TR_EDGE	Specifies if the activated trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. The trigger reflects TR_CMD.ACTIVATE. '1': edge sensitive trigger. The trigger is activated for two clk_peri cycles. Default Value: 0
12 : 8	GROUP_SEL	Specifies the trigger group: "0"-"15": trigger multiplexer groups. "16"-"31": trigger 1-to-1 groups. Default Value: 0
7 : 0	TR_SEL	Specifies the activated trigger when ACTIVATE is '1'. If the specified trigger is not present, the trigger activation has no effect. Default Value: 0

PERI_DIV_CMD

Divider command
Address: 0x40000400
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DIV_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						TYPE_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	PA_DIV_SEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None				RW	
HW Access	RW1C	RW1C	None				R	
Name	ENABLE	DISABLE	None [29:26]				PA_TYPE_SEL [25:24]	

Bits	Name	Description

31	ENABLE	Clock divider enable command (mutually exclusive with DISABLE). Typically, SW sets this field to '1' to enable a divider and HW sets this field to '0' to indicate that divider enabling has completed. When a divider is enabled, its integer and fractional (if present) counters are initialized to "0". If a divider is to be re-enabled using different integer and fractional divider values, the SW should follow these steps: 0: Disable the divider using the DIV_CMD.DISABLE field. 1: Configure the divider's DIV_XXX_CTL register. 2: Enable the divider using the DIV_CMD_ENABLE field. The DIV_SEL and TYPE_SEL fields specify which divider is to be enabled. The enabled divider may be phase aligned to either "clk_peri" (typical usage) or to ANY enabled divider. The PA_DIV_SEL and PA_TYPE_SEL fields specify the reference divider. The HW sets the ENABLE field to '0' when the enabling is performed and the HW set the DIV_XXX_CTL.EN field of the divider to '1' when the enabling is performed. Note that enabling with phase alignment to a low frequency divider takes time. E.g. To align to a divider that generates a clock of "clk_peri"/n (with n being the integer divider value INT_DIV+1), up to n cycles may be required to perform alignment. Phase alignment to "clk_peri" takes affect immediately. SW can set this field to '0' during phase alignment to abort the enabling process. Default Value: 0
30	DISABLE	Clock divider disable command (mutually exclusive with ENABLE). SW sets this field to '1' and HW sets this field to '0'. The DIV_SEL and TYPE_SEL fields specify which divider is to be disabled. The HW sets the DISABLE field to '0' immediately and the HW sets the DIV_XXX_CTL.EN field of the divider to '0' immediately. Default Value: 0

25 : 24	PA_TYPE_SEL	Specifies the divider type of the divider to which phase alignment is performed for the clock enable command: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
23 : 16	PA_DIV_SEL	(PA_TYPE_SEL, PA_DIV_SEL) specifies the divider to which phase alignment is performed for the clock enable command. Any enabled divider can be used as reference. This allows all dividers to be aligned with each other, even when they are enabled at different times. If PA_DIV_SEL is "255" and PA_TYPE_SEL is "3", "clk_peri" is used as reference. Default Value: 255
9 : 8	TYPE_SEL	Specifies the divider type of the divider on which the command is performed: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
7 : 0	DIV_SEL	(TYPE_SEL, DIV_SEL) specifies the divider on which the command (DISABLE/ENABLE) is performed. If DIV_SEL is "255" and TYPE_SEL is "3" (default/reset value), no divider is specified and no clock signal(s) are generated. Default Value: 255

PERI_CLOCK_CTL0

Clock control
Address: 0x40000C00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			DIV_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						TYPE_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	TYPE_SEL	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3

4 : 0	DIV_SEL	Specifies one of the dividers of the divider type specified by TYPE_SEL. If DIV_SEL is "255" and TYPE_SEL is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out-of-phase dividers, spurious clock control signals may be generated for one "clk_peri" cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (DIV_SEL is "255" and TYPE_SEL is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 31

PERI_DIV_8_CTL0

Divider control (for 8.0 divider)
Address: 0x40001000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT8_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	INT8_DIV	Integer division by (1+INT8_DIV). Allows for integer divisions in the range [1, 256]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 256]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 256]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

PERI_DIV_16_CTL0

Divider control (for 16.0 divider)
Address: 0x40001400
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

PERI_DIV_24_5_CTL0

Divider control (for 24.5 divider)
Address: 0x40001C00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		R
HW Access	R					None		RW
Name	FRAC5_DIV [7:3]					None [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT24_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT24_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	INT24_DIV [31:24]							

Bits	Name	Description
31 : 8	INT24_DIV	Integer division by (1+INT24_DIV). Allows for integer divisions in the range [1, 16,777,216]. Note: combined with fractional division, this divider type allows for a division in the range [1, 16,777,216 31/32] in 1/32 increments. For the generation of a divided clock, the integer division range is restricted to [2, 16,777,216 31/32]. For the generation of a 50/50% duty cycle divided clock, the division range is restricted to [2, 16,777,216]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

7 : 3	FRAC5_DIV	Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 "clk_peri" cycle longer than other clock periods. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

PERI_ECC_CTL

ECC control
Address: 0x40002000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WORD_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					WORD_ADDR [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW	None	RW
HW Access	None					R	None	R
Name	None [23:19]					ECC_INJ_EN	None	ECC_EN

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	PARITY [31:24]							

Bits	Name	Description
31 : 24	PARITY	ECC parity to use for ECC error injection at address WORD_ADDR. Default Value: 0
18	ECC_INJ_EN	Enable error injection for PERI protection structure SRAM. When '1', the parity (PARITY) is used when a write is done to the WORD_ADDR word address of the SRAM. Default Value: 0
16	ECC_EN	Enable ECC checking: '0': Disabled. '1': Enabled. Default Value: 1
10 : 0	WORD_ADDR	Specifies the word address where the parity is injected. - On a 32-bit write access to this SRAM address and when ECC_INJ_EN bit is '1', the parity (PARITY) is injected. Default Value: 0

PERI_GR0_SL_CTL

Slave control
Address: 0x40004010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						ENABLED_1	ENABLED_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW1S	RW1S
HW Access	None						R	R
Name	None [23:18]						DISABLED_1	DISABLED_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	DISABLED_1	Default Value: 0
16	DISABLED_0	Peripheral group, slave 0 permanent disable. Setting this bit to 1 has the same effect as setting ENABLED_0 to 0. However, once set to 1, this bit cannot be changed back to 0 anymore. Default Value: 0
1	ENABLED_1	Peripheral group, slave 1 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect, master interface MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1

0	ENABLED_0	Peripheral group, slave 0 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1

PERI_GR1_SL_CTL

Slave control
Address: 0x40004030
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							ENABLED_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW1S
HW Access	None							R
Name	None [23:17]							DISABLED_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	DISABLED_0	Peripheral group, slave 0 permanent disable. Setting this bit to 1 has the same effect as setting ENABLED_0 to 0. However, once set to 1, this bit cannot be changed back to 0 anymore. Default Value: 0
0	ENABLED_0	Peripheral group, slave 0 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1

PERI_GR2_SL_CTL

Slave control
Address: 0x40004050
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	ENABLED_7	ENABLED_6	ENABLED_5	ENABLED_4	ENABLED_3	ENABLED_2	ENABLED_1	ENABLED_0

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				ENABLED_11	ENABLED_10	ENABLED_9	ENABLED_8

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	R	R	R	R	R	R	R	R
Name	DISABLED_7	DISABLED_6	DISABLED_5	DISABLED_4	DISABLED_3	DISABLED_2	DISABLED_1	DISABLED_0

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				R	R	R	R
Name	None [31:28]				DISABLED_11	DISABLED_10	DISABLED_9	DISABLED_8

Bits	Name	Description
27	DISABLED_11	Default Value: 0
26	DISABLED_10	Default Value: 0
25	DISABLED_9	Default Value: 0
24	DISABLED_8	Default Value: 0
23	DISABLED_7	Default Value: 0
22	DISABLED_6	Default Value: 0
21	DISABLED_5	Default Value: 0
20	DISABLED_4	Default Value: 0
19	DISABLED_3	Default Value: 0
18	DISABLED_2	Default Value: 0
17	DISABLED_1	Default Value: 0

16	DISABLED_0	Peripheral group, slave 0 permanent disable. Setting this bit to 1 has the same effect as setting ENABLED_0 to 0. However, once set to 1, this bit cannot be changed back to 0 anymore. Default Value: 0
11	ENABLED_11	Default Value: 1
10	ENABLED_10	Default Value: 1
9	ENABLED_9	Default Value: 1
8	ENABLED_8	Default Value: 1
7	ENABLED_7	Default Value: 1
6	ENABLED_6	Default Value: 1
5	ENABLED_5	Default Value: 1
4	ENABLED_4	Default Value: 1
3	ENABLED_3	Default Value: 1
2	ENABLED_2	Default Value: 1
1	ENABLED_1	Peripheral group, slave 1 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect, master interface MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1
0	ENABLED_0	Peripheral group, slave 0 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1

PERI_GR3_CLOCK_CTL

Clock control
Address: 0x40004060
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT8_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	INT8_DIV	Specifies a group clock divider (from the peripheral clock "clk_peri" to the group clock "clk_group[3/4/5/...15]"). Integer division by (1+INT8_DIV). Allows for integer divisions in the range [1, 256]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

PERI_GR3_SL_CTL

Slave control
Address: 0x40004070
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			ENABLED_4	ENABLED_3	ENABLED_2	ENABLED_1	ENABLED_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	None			R	R	R	R	R
Name	None [23:21]			DISABLED_4	DISABLED_3	DISABLED_2	DISABLED_1	DISABLED_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20	DISABLED_4	Default Value: 0
19	DISABLED_3	Default Value: 0
18	DISABLED_2	Default Value: 0
17	DISABLED_1	Default Value: 0
16	DISABLED_0	Peripheral group, slave 0 permanent disable. Setting this bit to 1 has the same effect as setting ENABLED_0 to 0. However, once set to 1, this bit cannot be changed back to 0 anymore. Default Value: 0
4	ENABLED_4	Default Value: 1
3	ENABLED_3	Default Value: 1
2	ENABLED_2	Default Value: 1

1	ENABLED_1	Peripheral group, slave 1 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect, master interface MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1
0	ENABLED_0	Peripheral group, slave 0 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1

PERI_GR5_SL_CTL

Slave control
Address: 0x400040B0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					ENABLED_2	ENABLED_1	ENABLED_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					R	R	R
Name	None [23:19]					DISABLED_2	DISABLED_1	DISABLED_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18	DISABLED_2	Default Value: 0
17	DISABLED_1	Default Value: 0
16	DISABLED_0	Peripheral group, slave 0 permanent disable. Setting this bit to 1 has the same effect as setting ENABLED_0 to 0. However, once set to 1, this bit cannot be changed back to 0 anymore. Default Value: 0
2	ENABLED_2	Default Value: 1
1	ENABLED_1	Peripheral group, slave 1 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect, master interface MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1

0	ENABLED_0	Peripheral group, slave 0 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1

PERI_GR6_SL_CTL

Slave control
Address: 0x400040D0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	ENABLED_7	ENABLED_6	ENABLED_5	ENABLED_4	ENABLED_3	ENABLED_2	ENABLED_1	ENABLED_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	R	R	R	R	R	R	R	R
Name	DISABLED_7	DISABLED_6	DISABLED_5	DISABLED_4	DISABLED_3	DISABLED_2	DISABLED_1	DISABLED_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	DISABLED_7	Default Value: 0
22	DISABLED_6	Default Value: 0
21	DISABLED_5	Default Value: 0
20	DISABLED_4	Default Value: 0
19	DISABLED_3	Default Value: 0
18	DISABLED_2	Default Value: 0
17	DISABLED_1	Default Value: 0
16	DISABLED_0	Peripheral group, slave 0 permanent disable. Setting this bit to 1 has the same effect as setting ENABLED_0 to 0. However, once set to 1, this bit cannot be changed back to 0 anymore. Default Value: 0
7	ENABLED_7	Default Value: 1
6	ENABLED_6	Default Value: 1
5	ENABLED_5	Default Value: 1
4	ENABLED_4	Default Value: 1

3	ENABLED_3	Default Value: 1
2	ENABLED_2	Default Value: 1
1	ENABLED_1	Peripheral group, slave 1 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect, master interface MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1
0	ENABLED_0	Peripheral group, slave 0 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1

PERI_TR_GR0_TR_CTL0

Trigger control register
Address: 0x40008000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		TR_SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0

5 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

PERI_TR_GR2_TR_CTL0

Trigger control register
Address: 0x40008800
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					TR_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0

2 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

PERI_TR_GR3_TR_CTL0

Trigger control register
Address: 0x40008C00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TR_SEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0

6 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

PERI_TR_GR4_TR_CTL0

Trigger control register
Address: 0x40009000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TR_SEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0

6 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

PERI_TR_GR5_TR_CTL0

Trigger control register
Address: 0x40009400
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TR_SEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0

6 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

PERI_TR_GR6_TR_CTL0

Trigger control register
Address: 0x40009800
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TR_SEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0

6 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

PERI_TR_GR7_TR_CTL0

Trigger control register
Address: 0x40009C00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					TR_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0

2 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

PERI_TR_GR8_TR_CTL0

Trigger control register
Address: 0x4000A000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TR_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0

3 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

PERI_TR_GR9_TR_CTL0

Trigger control register
Address: 0x4000A400
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TR_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None			
HW Access	None			R	None			
Name	None [15:13]			DBG_FREEZE_EN	None [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
7 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

PERI_TR_1TO1_GR0_TR_CTL0

Trigger control register
Address: 0x4000C000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TR_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
0	TR_SEL	Specifies input trigger: '0'': constant signal level '0'. '1': input trigger. Default Value: 0

PERI_TR_1TO1_GR1_TR_CTL0

Trigger control register
Address: 0x4000C400
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TR_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
0	TR_SEL	Specifies input trigger: '0'': constant signal level '0'. '1': input trigger. Default Value: 0

PERI_TR_1TO1_GR4_TR_CTL0

Trigger control register
Address: 0x4000D000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TR_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
0	TR_SEL	Specifies input trigger: '0'': constant signal level '0'. '1': input trigger. Default Value: 0

PERI_TR_1TO1_GR6_TR_CTL0

Trigger control register
Address: 0x4000D800
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TR_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
0	TR_SEL	Specifies input trigger: '0'': constant signal level '0'. '1': input trigger. Default Value: 0

PERI_TR_1TO1_GR8_TR_CTL0

Trigger control register
Address: 0x4000E000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TR_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
0	TR_SEL	Specifies input trigger: '0'': constant signal level '0'. '1': input trigger. Default Value: 0

PERI_MS_PPU_PR0_SL_ADDR

Slave region, base address
Address: 0x40010000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: Undefined

PERI_MS_PPU_PR0_SL_SIZE

Slave region, size
Address: 0x40010004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None		RW				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 0
28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: Undefined

PERI_MS_PPU_PR0_SL_ATT0

Slave attributes 0
Address: 0x40010010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	R	R	R	R
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC0_NS	PC0_PW	PC0_PR	PC0_UW	PC0_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC1_NS	PC1_PW	PC1_PR	PC1_UW	PC1_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC2_NS	PC2_PW	PC2_PR	PC2_UW	PC2_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC3_NS	PC3_PW	PC3_PR	PC3_UW	PC3_UR

Bits	Name	Description
28	PC3_NS	Protection context 3, non-secure. Default Value: 1
27	PC3_PW	Protection context 3, privileged write enable. Default Value: 1
26	PC3_PR	Protection context 3, privileged read enable. Default Value: 1
25	PC3_UW	Protection context 3, user write enable. Default Value: 1
24	PC3_UR	Protection context 3, user read enable. Default Value: 1
20	PC2_NS	Protection context 2, non-secure. Default Value: 1
19	PC2_PW	Protection context 2, privileged write enable. Default Value: 1
18	PC2_PR	Protection context 2, privileged read enable. Default Value: 1
17	PC2_UW	Protection context 2, user write enable. Default Value: 1
16	PC2_UR	Protection context 2, user read enable. Default Value: 1

12	PC1_NS	Protection context 1, non-secure. Default Value: 1
11	PC1_PW	Protection context 1, privileged write enable. Default Value: 1
10	PC1_PR	Protection context 1, privileged read enable. Default Value: 1
9	PC1_UW	Protection context 1, user write enable. Default Value: 1
8	PC1_UR	Protection context 1, user read enable. Default Value: 1
4	PC0_NS	Protection context 0, non-secure: '0': Secure (secure accesses allowed, non-secure access NOT allowed). '1': Non-secure (both secure and non-secure accesses allowed). Default Value: 1
3	PC0_PW	Protection context 0, privileged write enable: '0': Disabled (privileged, write accesses are NOT allowed). '1': Enabled (privileged, write accesses are allowed). Default Value: 1
2	PC0_PR	Protection context 0, privileged read enable: '0': Disabled (privileged, read accesses are NOT allowed). '1': Enabled (privileged, read accesses are allowed). Default Value: 1
1	PC0_UW	Protection context 0, user write enable: '0': Disabled (user, write accesses are NOT allowed). '1': Enabled (user, write accesses are allowed). Default Value: 1
0	PC0_UR	Protection context 0, user read enable: '0': Disabled (user, read accesses are NOT allowed). '1': Enabled (user, read accesses are allowed). Default Value: 1

PERI_MS_PPU_PR0_SL_ATT1

Slave attributes 1
Address: 0x40010014
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC4_NS	PC4_PW	PC4_PR	PC4_UW	PC4_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC5_NS	PC5_PW	PC5_PR	PC5_UW	PC5_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC6_NS	PC6_PW	PC6_PR	PC6_UW	PC6_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC7_NS	PC7_PW	PC7_PR	PC7_UW	PC7_UR

Bits	Name	Description
28	PC7_NS	Protection context 7, non-secure. Default Value: 1
27	PC7_PW	Protection context 7, privileged write enable. Default Value: 1
26	PC7_PR	Protection context 7, privileged read enable. Default Value: 1
25	PC7_UW	Protection context 7, user write enable. Default Value: 1
24	PC7_UR	Protection context 7, user read enable. Default Value: 1
20	PC6_NS	Protection context 6, non-secure. Default Value: 1
19	PC6_PW	Protection context 6, privileged write enable. Default Value: 1
18	PC6_PR	Protection context 6, privileged read enable. Default Value: 1
17	PC6_UW	Protection context 6, user write enable. Default Value: 1
16	PC6_UR	Protection context 6, user read enable. Default Value: 1

12	PC5_NS	Protection context 5, non-secure. Default Value: 1
11	PC5_PW	Protection context 5, privileged write enable. Default Value: 1
10	PC5_PR	Protection context 5, privileged read enable. Default Value: 1
9	PC5_UW	Protection context 5, user write enable. Default Value: 1
8	PC5_UR	Protection context 5, user read enable. Default Value: 1
4	PC4_NS	Protection context 4, non-secure. Default Value: 1
3	PC4_PW	Protection context 4, privileged write enable. Default Value: 1
2	PC4_PR	Protection context 4, privileged read enable. Default Value: 1
1	PC4_UW	Protection context 4, user write enable. Default Value: 1
0	PC4_UR	Protection context 4, user read enable. Default Value: 1

PERI_MS_PPU_PR0_SL_ATT2

Slave attributes 2
Address: 0x40010018
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC8_NS	PC8_PW	PC8_PR	PC8_UW	PC8_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC9_NS	PC9_PW	PC9_PR	PC9_UW	PC9_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC10_NS	PC10_PW	PC10_PR	PC10_UW	PC10_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC11_NS	PC11_PW	PC11_PR	PC11_UW	PC11_UR

Bits	Name	Description
28	PC11_NS	Protection context 11, non-secure. Default Value: 1
27	PC11_PW	Protection context 11, privileged write enable. Default Value: 1
26	PC11_PR	Protection context 11, privileged read enable. Default Value: 1
25	PC11_UW	Protection context 11, user write enable. Default Value: 1
24	PC11_UR	Protection context 11, user read enable. Default Value: 1
20	PC10_NS	Protection context 10, non-secure. Default Value: 1
19	PC10_PW	Protection context 10, privileged write enable. Default Value: 1
18	PC10_PR	Protection context 10, privileged read enable. Default Value: 1
17	PC10_UW	Protection context 10, user write enable. Default Value: 1
16	PC10_UR	Protection context 10, user read enable. Default Value: 1

12	PC9_NS	Protection context 9, non-secure. Default Value: 1
11	PC9_PW	Protection context 9, privileged write enable. Default Value: 1
10	PC9_PR	Protection context 9, privileged read enable. Default Value: 1
9	PC9_UW	Protection context 9, user write enable. Default Value: 1
8	PC9_UR	Protection context 9, user read enable. Default Value: 1
4	PC8_NS	Protection context 8, non-secure. Default Value: 1
3	PC8_PW	Protection context 8, privileged write enable. Default Value: 1
2	PC8_PR	Protection context 8, privileged read enable. Default Value: 1
1	PC8_UW	Protection context 8, user write enable. Default Value: 1
0	PC8_UR	Protection context 8, user read enable. Default Value: 1

PERI_MS_PPU_PR0_SL_ATT3

Slave attributes 3
Address: 0x4001001C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC12_NS	PC12_PW	PC12_PR	PC12_UW	PC12_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC13_NS	PC13_PW	PC13_PR	PC13_UW	PC13_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC14_NS	PC14_PW	PC14_PR	PC14_UW	PC14_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC15_NS	PC15_PW	PC15_PR	PC15_UW	PC15_UR

Bits	Name	Description
28	PC15_NS	Protection context 15, non-secure. Default Value: 1
27	PC15_PW	Protection context 15, privileged write enable. Default Value: 1
26	PC15_PR	Protection context 15, privileged read enable. Default Value: 1
25	PC15_UW	Protection context 15, user write enable. Default Value: 1
24	PC15_UR	Protection context 15, user read enable. Default Value: 1
20	PC14_NS	Protection context 14, non-secure. Default Value: 1
19	PC14_PW	Protection context 14, privileged write enable. Default Value: 1
18	PC14_PR	Protection context 14, privileged read enable. Default Value: 1
17	PC14_UW	Protection context 14, user write enable. Default Value: 1
16	PC14_UR	Protection context 14, user read enable. Default Value: 1

12	PC13_NS	Protection context 13, non-secure. Default Value: 1
11	PC13_PW	Protection context 13, privileged write enable. Default Value: 1
10	PC13_PR	Protection context 13, privileged read enable. Default Value: 1
9	PC13_UW	Protection context 13, user write enable. Default Value: 1
8	PC13_UR	Protection context 13, user read enable. Default Value: 1
4	PC12_NS	Protection context 12, non-secure. Default Value: 1
3	PC12_PW	Protection context 12, privileged write enable. Default Value: 1
2	PC12_PR	Protection context 12, privileged read enable. Default Value: 1
1	PC12_UW	Protection context 12, user write enable. Default Value: 1
0	PC12_UR	Protection context 12, user read enable. Default Value: 1

PERI_MS_PPU_PR0_MS_ADDR

Master region, base address
Address: 0x40010020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778240

PERI_MS_PPU_PR0_MS_SIZE

Master region, size
Address: 0x40010024
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Master region enable: '1': Enabled. Default Value: 1
28 : 24	REGION_SIZE	This field specifies the size of the master region: "5": 64 B region The master region includes the SL_ADDR, SL_SIZE, SL_ATT0, ..., SL_ATT3, MS_ADDR, MS_SIZE, MS_ATT0, ..., MS_ATT3 registers. Therefore, the access privileges for all these registers is determined by MS_ATT0, ..., MS_ATT3. Default Value: 0x05

PERI_MS_PPU_PR0_MS_ATT0

Master attributes 0
Address: 0x40010030
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	R	R	R	R
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC0_NS	PC0_PW	PC0_PR	PC0_UW	PC0_UR
Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC1_NS	PC1_PW	PC1_PR	PC1_UW	PC1_UR
Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC2_NS	PC2_PW	PC2_PR	PC2_UW	PC2_UR
Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC3_NS	PC3_PW	PC3_PR	PC3_UW	PC3_UR

Bits	Name	Description
28	PC3_NS	Protection context 3, non-secure. Default Value: 1
27	PC3_PW	Protection context 3, privileged write enable. Default Value: 1
26	PC3_PR	Protection context 3, privileged read enable. Default Value: 1
25	PC3_UW	Protection context 3, user write enable. Default Value: 1
24	PC3_UR	Protection context 3, user read enable. Default Value: 1
20	PC2_NS	Protection context 2, non-secure. Default Value: 1
19	PC2_PW	Protection context 2, privileged write enable. Default Value: 1
18	PC2_PR	Protection context 2, privileged read enable. Default Value: 1
17	PC2_UW	Protection context 2, user write enable. Default Value: 1
16	PC2_UR	Protection context 2, user read enable. Default Value: 1

12	PC1_NS	Protection context 1, non-secure. Default Value: 1
11	PC1_PW	Protection context 1, privileged write enable. Default Value: 1
10	PC1_PR	Protection context 1, privileged read enable. Default Value: 1
9	PC1_UW	Protection context 1, user write enable. Default Value: 1
8	PC1_UR	Protection context 1, user read enable. Default Value: 1
4	PC0_NS	Protection context 0, non-secure: '0': Secure (secure accesses allowed, non-secure access NOT allowed). '1': Non-secure (both secure and non-secure accesses allowed). Default Value: 1
3	PC0_PW	Protection context 0, privileged write enable: '0': Disabled (privileged, write accesses are NOT allowed). '1': Enabled (privileged, write accesses are allowed). Default Value: 1
2	PC0_PR	Protection context 0, privileged read enable: '0': Disabled (privileged, read accesses are NOT allowed). '1': Enabled (privileged, read accesses are allowed). Default Value: 1
1	PC0_UW	Protection context 0, user write enable: '0': Disabled (user, write accesses are NOT allowed). '1': Enabled (user, write accesses are allowed). Default Value: 1
0	PC0_UR	Protection context 0, user read enable: '0': Disabled (user, read accesses are NOT allowed). '1': Enabled (user, read accesses are allowed). Default Value: 1

PERI_MS_PPU_PR0_MS_ATT1

Master attributes 1
Address: 0x40010034
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC4_NS	PC4_PW	PC4_PR	PC4_UW	PC4_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC5_NS	PC5_PW	PC5_PR	PC5_UW	PC5_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC6_NS	PC6_PW	PC6_PR	PC6_UW	PC6_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC7_NS	PC7_PW	PC7_PR	PC7_UW	PC7_UR

Bits	Name	Description
28	PC7_NS	Protection context 7, non-secure. Default Value: 1
27	PC7_PW	Protection context 7, privileged write enable. Default Value: 1
26	PC7_PR	Protection context 7, privileged read enable. Default Value: 1
25	PC7_UW	Protection context 7, user write enable. Default Value: 1
24	PC7_UR	Protection context 7, user read enable. Default Value: 1
20	PC6_NS	Protection context 6, non-secure. Default Value: 1
19	PC6_PW	Protection context 6, privileged write enable. Default Value: 1
18	PC6_PR	Protection context 6, privileged read enable. Default Value: 1
17	PC6_UW	Protection context 6, user write enable. Default Value: 1
16	PC6_UR	Protection context 6, user read enable. Default Value: 1

12	PC5_NS	Protection context 5, non-secure. Default Value: 1
11	PC5_PW	Protection context 5, privileged write enable. Default Value: 1
10	PC5_PR	Protection context 5, privileged read enable. Default Value: 1
9	PC5_UW	Protection context 5, user write enable. Default Value: 1
8	PC5_UR	Protection context 5, user read enable. Default Value: 1
4	PC4_NS	Protection context 4, non-secure. Default Value: 1
3	PC4_PW	Protection context 4, privileged write enable. Default Value: 1
2	PC4_PR	Protection context 4, privileged read enable. Default Value: 1
1	PC4_UW	Protection context 4, user write enable. Default Value: 1
0	PC4_UR	Protection context 4, user read enable. Default Value: 1

PERI_MS_PPU_PR0_MS_ATT2

Master attributes 2
Address: 0x40010038
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC8_NS	PC8_PW	PC8_PR	PC8_UW	PC8_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC9_NS	PC9_PW	PC9_PR	PC9_UW	PC9_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC10_NS	PC10_PW	PC10_PR	PC10_UW	PC10_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC11_NS	PC11_PW	PC11_PR	PC11_UW	PC11_UR

Bits	Name	Description
28	PC11_NS	Protection context 11, non-secure. Default Value: 1
27	PC11_PW	Protection context 11, privileged write enable. Default Value: 1
26	PC11_PR	Protection context 11, privileged read enable. Default Value: 1
25	PC11_UW	Protection context 11, user write enable. Default Value: 1
24	PC11_UR	Protection context 11, user read enable. Default Value: 1
20	PC10_NS	Protection context 10, non-secure. Default Value: 1
19	PC10_PW	Protection context 10, privileged write enable. Default Value: 1
18	PC10_PR	Protection context 10, privileged read enable. Default Value: 1
17	PC10_UW	Protection context 10, user write enable. Default Value: 1
16	PC10_UR	Protection context 10, user read enable. Default Value: 1

12	PC9_NS	Protection context 9, non-secure. Default Value: 1
11	PC9_PW	Protection context 9, privileged write enable. Default Value: 1
10	PC9_PR	Protection context 9, privileged read enable. Default Value: 1
9	PC9_UW	Protection context 9, user write enable. Default Value: 1
8	PC9_UR	Protection context 9, user read enable. Default Value: 1
4	PC8_NS	Protection context 8, non-secure. Default Value: 1
3	PC8_PW	Protection context 8, privileged write enable. Default Value: 1
2	PC8_PR	Protection context 8, privileged read enable. Default Value: 1
1	PC8_UW	Protection context 8, user write enable. Default Value: 1
0	PC8_UR	Protection context 8, user read enable. Default Value: 1

PERI_MS_PPU_PR0_MS_ATT3

Master attributes 3
Address: 0x4001003C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC12_NS	PC12_PW	PC12_PR	PC12_UW	PC12_UR
Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC13_NS	PC13_PW	PC13_PR	PC13_UW	PC13_UR
Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC14_NS	PC14_PW	PC14_PR	PC14_UW	PC14_UR
Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC15_NS	PC15_PW	PC15_PR	PC15_UW	PC15_UR

Bits	Name	Description
28	PC15_NS	Protection context 15, non-secure. Default Value: 1
27	PC15_PW	Protection context 15, privileged write enable. Default Value: 1
26	PC15_PR	Protection context 15, privileged read enable. Default Value: 1
25	PC15_UW	Protection context 15, user write enable. Default Value: 1
24	PC15_UR	Protection context 15, user read enable. Default Value: 1
20	PC14_NS	Protection context 14, non-secure. Default Value: 1
19	PC14_PW	Protection context 14, privileged write enable. Default Value: 1
18	PC14_PR	Protection context 14, privileged read enable. Default Value: 1
17	PC14_UW	Protection context 14, user write enable. Default Value: 1
16	PC14_UR	Protection context 14, user read enable. Default Value: 1

12	PC13_NS	Protection context 13, non-secure. Default Value: 1
11	PC13_PW	Protection context 13, privileged write enable. Default Value: 1
10	PC13_PR	Protection context 13, privileged read enable. Default Value: 1
9	PC13_UW	Protection context 13, user write enable. Default Value: 1
8	PC13_UR	Protection context 13, user read enable. Default Value: 1
4	PC12_NS	Protection context 12, non-secure. Default Value: 1
3	PC12_PW	Protection context 12, privileged write enable. Default Value: 1
2	PC12_PR	Protection context 12, privileged read enable. Default Value: 1
1	PC12_UW	Protection context 12, user write enable. Default Value: 1
0	PC12_UR	Protection context 12, user read enable. Default Value: 1

PERI_MS_PPU_PR1_MS_ADDR

Master region, base address
Address: 0x40010060
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778241

PERI_MS_PPU_PR2_MS_ADDR

Master region, base address
Address: 0x400100A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778242

PERI_MS_PPU_PR3_MS_ADDR

Master region, base address
Address: 0x400100E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778243

PERI_MS_PPU_PR4_MS_ADDR

Master region, base address
Address: 0x40010120
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778244

PERI_MS_PPU_PR5_MS_ADDR

Master region, base address
Address: 0x40010160
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778245

PERI_MS_PPU_PR6_MS_ADDR

Master region, base address
Address: 0x400101A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778246

PERI_MS_PPU_PR7_MS_ADDR

Master region, base address
Address: 0x400101E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778247

PERI_MS_PPU_PR8_MS_ADDR

Master region, base address
Address: 0x40010220
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778248

PERI_MS_PPU_PR9_MS_ADDR

Master region, base address
Address: 0x40010260
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778249

PERI_MS_PPU_PR10_MS_ADDR

Master region, base address
Address: 0x400102A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778250

PERI_MS_PPU_PR11_MS_ADDR

Master region, base address
Address: 0x400102E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778251

PERI_MS_PPU_PR12_MS_ADDR

Master region, base address
Address: 0x40010320
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778252

PERI_MS_PPU_PR13_MS_ADDR

Master region, base address
Address: 0x40010360
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778253

PERI_MS_PPU_PR14_MS_ADDR

Master region, base address
Address: 0x400103A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778254

PERI_MS_PPU_PR15_MS_ADDR

Master region, base address
Address: 0x400103E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778255

PERI_MS_PPU_FX0_SL_ADDR

Slave region, base address
Address: 0x40010800
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268435456

PERI_MS_PPU_FX0_SL_SIZE

Slave region, size
Address: 0x40010804
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1
28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 12

PERI_MS_PPU_FX0_SL_ATT0

Slave attributes 0
Address: 0x40010810
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	R	R	R	R
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC0_NS	PC0_PW	PC0_PR	PC0_UW	PC0_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC1_NS	PC1_PW	PC1_PR	PC1_UW	PC1_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC2_NS	PC2_PW	PC2_PR	PC2_UW	PC2_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC3_NS	PC3_PW	PC3_PR	PC3_UW	PC3_UR

Bits	Name	Description
28	PC3_NS	Protection context 3, non-secure. Default Value: 1
27	PC3_PW	Protection context 3, privileged write enable. Default Value: 1
26	PC3_PR	Protection context 3, privileged read enable. Default Value: 1
25	PC3_UW	Protection context 3, user write enable. Default Value: 1
24	PC3_UR	Protection context 3, user read enable. Default Value: 1
20	PC2_NS	Protection context 2, non-secure. Default Value: 1
19	PC2_PW	Protection context 2, privileged write enable. Default Value: 1
18	PC2_PR	Protection context 2, privileged read enable. Default Value: 1
17	PC2_UW	Protection context 2, user write enable. Default Value: 1
16	PC2_UR	Protection context 2, user read enable. Default Value: 1

12	PC1_NS	Protection context 1, non-secure. Default Value: 1
11	PC1_PW	Protection context 1, privileged write enable. Default Value: 1
10	PC1_PR	Protection context 1, privileged read enable. Default Value: 1
9	PC1_UW	Protection context 1, user write enable. Default Value: 1
8	PC1_UR	Protection context 1, user read enable. Default Value: 1
4	PC0_NS	Protection context 0, non-secure: '0': Secure (secure accesses allowed, non-secure access NOT allowed). '1': Non-secure (both secure and non-secure accesses allowed). Default Value: 1
3	PC0_PW	Protection context 0, privileged write enable: '0': Disabled (privileged, write accesses are NOT allowed). '1': Enabled (privileged, write accesses are allowed). Default Value: 1
2	PC0_PR	Protection context 0, privileged read enable: '0': Disabled (privileged, read accesses are NOT allowed). '1': Enabled (privileged, read accesses are allowed). Default Value: 1
1	PC0_UW	Protection context 0, user write enable: '0': Disabled (user, write accesses are NOT allowed). '1': Enabled (user, write accesses are allowed). Default Value: 1
0	PC0_UR	Protection context 0, user read enable: '0': Disabled (user, read accesses are NOT allowed). '1': Enabled (user, read accesses are allowed). Default Value: 1

PERI_MS_PPU_FX0_SL_ATT1

Slave attributes 1
Address: 0x40010814
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC4_NS	PC4_PW	PC4_PR	PC4_UW	PC4_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC5_NS	PC5_PW	PC5_PR	PC5_UW	PC5_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC6_NS	PC6_PW	PC6_PR	PC6_UW	PC6_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC7_NS	PC7_PW	PC7_PR	PC7_UW	PC7_UR

Bits	Name	Description
28	PC7_NS	Protection context 7, non-secure. Default Value: 1
27	PC7_PW	Protection context 7, privileged write enable. Default Value: 1
26	PC7_PR	Protection context 7, privileged read enable. Default Value: 1
25	PC7_UW	Protection context 7, user write enable. Default Value: 1
24	PC7_UR	Protection context 7, user read enable. Default Value: 1
20	PC6_NS	Protection context 6, non-secure. Default Value: 1
19	PC6_PW	Protection context 6, privileged write enable. Default Value: 1
18	PC6_PR	Protection context 6, privileged read enable. Default Value: 1
17	PC6_UW	Protection context 6, user write enable. Default Value: 1
16	PC6_UR	Protection context 6, user read enable. Default Value: 1

12	PC5_NS	Protection context 5, non-secure. Default Value: 1
11	PC5_PW	Protection context 5, privileged write enable. Default Value: 1
10	PC5_PR	Protection context 5, privileged read enable. Default Value: 1
9	PC5_UW	Protection context 5, user write enable. Default Value: 1
8	PC5_UR	Protection context 5, user read enable. Default Value: 1
4	PC4_NS	Protection context 4, non-secure. Default Value: 1
3	PC4_PW	Protection context 4, privileged write enable. Default Value: 1
2	PC4_PR	Protection context 4, privileged read enable. Default Value: 1
1	PC4_UW	Protection context 4, user write enable. Default Value: 1
0	PC4_UR	Protection context 4, user read enable. Default Value: 1

PERI_MS_PPU_FX0_SL_ATT2

Slave attributes 2
Address: 0x40010818
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC8_NS	PC8_PW	PC8_PR	PC8_UW	PC8_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC9_NS	PC9_PW	PC9_PR	PC9_UW	PC9_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC10_NS	PC10_PW	PC10_PR	PC10_UW	PC10_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC11_NS	PC11_PW	PC11_PR	PC11_UW	PC11_UR

Bits	Name	Description
28	PC11_NS	Protection context 11, non-secure. Default Value: 1
27	PC11_PW	Protection context 11, privileged write enable. Default Value: 1
26	PC11_PR	Protection context 11, privileged read enable. Default Value: 1
25	PC11_UW	Protection context 11, user write enable. Default Value: 1
24	PC11_UR	Protection context 11, user read enable. Default Value: 1
20	PC10_NS	Protection context 10, non-secure. Default Value: 1
19	PC10_PW	Protection context 10, privileged write enable. Default Value: 1
18	PC10_PR	Protection context 10, privileged read enable. Default Value: 1
17	PC10_UW	Protection context 10, user write enable. Default Value: 1
16	PC10_UR	Protection context 10, user read enable. Default Value: 1

12	PC9_NS	Protection context 9, non-secure. Default Value: 1
11	PC9_PW	Protection context 9, privileged write enable. Default Value: 1
10	PC9_PR	Protection context 9, privileged read enable. Default Value: 1
9	PC9_UW	Protection context 9, user write enable. Default Value: 1
8	PC9_UR	Protection context 9, user read enable. Default Value: 1
4	PC8_NS	Protection context 8, non-secure. Default Value: 1
3	PC8_PW	Protection context 8, privileged write enable. Default Value: 1
2	PC8_PR	Protection context 8, privileged read enable. Default Value: 1
1	PC8_UW	Protection context 8, user write enable. Default Value: 1
0	PC8_UR	Protection context 8, user read enable. Default Value: 1

PERI_MS_PPU_FX0_SL_ATT3

Slave attributes 3
Address: 0x4001081C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC12_NS	PC12_PW	PC12_PR	PC12_UW	PC12_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC13_NS	PC13_PW	PC13_PR	PC13_UW	PC13_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC14_NS	PC14_PW	PC14_PR	PC14_UW	PC14_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC15_NS	PC15_PW	PC15_PR	PC15_UW	PC15_UR

Bits	Name	Description
28	PC15_NS	Protection context 15, non-secure. Default Value: 1
27	PC15_PW	Protection context 15, privileged write enable. Default Value: 1
26	PC15_PR	Protection context 15, privileged read enable. Default Value: 1
25	PC15_UW	Protection context 15, user write enable. Default Value: 1
24	PC15_UR	Protection context 15, user read enable. Default Value: 1
20	PC14_NS	Protection context 14, non-secure. Default Value: 1
19	PC14_PW	Protection context 14, privileged write enable. Default Value: 1
18	PC14_PR	Protection context 14, privileged read enable. Default Value: 1
17	PC14_UW	Protection context 14, user write enable. Default Value: 1
16	PC14_UR	Protection context 14, user read enable. Default Value: 1

12	PC13_NS	Protection context 13, non-secure. Default Value: 1
11	PC13_PW	Protection context 13, privileged write enable. Default Value: 1
10	PC13_PR	Protection context 13, privileged read enable. Default Value: 1
9	PC13_UW	Protection context 13, user write enable. Default Value: 1
8	PC13_UR	Protection context 13, user read enable. Default Value: 1
4	PC12_NS	Protection context 12, non-secure. Default Value: 1
3	PC12_PW	Protection context 12, privileged write enable. Default Value: 1
2	PC12_PR	Protection context 12, privileged read enable. Default Value: 1
1	PC12_UW	Protection context 12, user write enable. Default Value: 1
0	PC12_UR	Protection context 12, user read enable. Default Value: 1

PERI_MS_PPU_FX0_MS_ADDR

Master region, base address
Address: 0x40010820
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778272

PERI_MS_PPU_FX0_MS_SIZE

Master region, size
Address: 0x40010824
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Master region enable: '1': Enabled. Default Value: 1
28 : 24	REGION_SIZE	This field specifies the size of the master region: "5": 64 B region The master region includes the SL_ADDR, SL_SIZE, SL_ATT0, ..., SL_ATT3, MS_ADDR, MS_SIZE, MS_ATT0, ..., MS_ATT3 registers. Therefore, the access privileges for all these registers is determined by MS_ATT0, ..., MS_ATT3. Default Value: 0x05

PERI_MS_PPU_FX0_MS_ATT0

Master attributes 0
Address: 0x40010830
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	R	R	R	R
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC0_NS	PC0_PW	PC0_PR	PC0_UW	PC0_UR
Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC1_NS	PC1_PW	PC1_PR	PC1_UW	PC1_UR
Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC2_NS	PC2_PW	PC2_PR	PC2_UW	PC2_UR
Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC3_NS	PC3_PW	PC3_PR	PC3_UW	PC3_UR

Bits	Name	Description
28	PC3_NS	Protection context 3, non-secure. Default Value: 1
27	PC3_PW	Protection context 3, privileged write enable. Default Value: 1
26	PC3_PR	Protection context 3, privileged read enable. Default Value: 1
25	PC3_UW	Protection context 3, user write enable. Default Value: 1
24	PC3_UR	Protection context 3, user read enable. Default Value: 1
20	PC2_NS	Protection context 2, non-secure. Default Value: 1
19	PC2_PW	Protection context 2, privileged write enable. Default Value: 1
18	PC2_PR	Protection context 2, privileged read enable. Default Value: 1
17	PC2_UW	Protection context 2, user write enable. Default Value: 1
16	PC2_UR	Protection context 2, user read enable. Default Value: 1

12	PC1_NS	Protection context 1, non-secure. Default Value: 1
11	PC1_PW	Protection context 1, privileged write enable. Default Value: 1
10	PC1_PR	Protection context 1, privileged read enable. Default Value: 1
9	PC1_UW	Protection context 1, user write enable. Default Value: 1
8	PC1_UR	Protection context 1, user read enable. Default Value: 1
4	PC0_NS	Protection context 0, non-secure: '0': Secure (secure accesses allowed, non-secure access NOT allowed). '1': Non-secure (both secure and non-secure accesses allowed). Default Value: 1
3	PC0_PW	Protection context 0, privileged write enable: '0': Disabled (privileged, write accesses are NOT allowed). '1': Enabled (privileged, write accesses are allowed). Default Value: 1
2	PC0_PR	Protection context 0, privileged read enable: '0': Disabled (privileged, read accesses are NOT allowed). '1': Enabled (privileged, read accesses are allowed). Default Value: 1
1	PC0_UW	Protection context 0, user write enable: '0': Disabled (user, write accesses are NOT allowed). '1': Enabled (user, write accesses are allowed). Default Value: 1
0	PC0_UR	Protection context 0, user read enable: '0': Disabled (user, read accesses are NOT allowed). '1': Enabled (user, read accesses are allowed). Default Value: 1

PERI_MS_PPU_FX0_MS_ATT1

Master attributes 1
Address: 0x40010834
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC4_NS	PC4_PW	PC4_PR	PC4_UW	PC4_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC5_NS	PC5_PW	PC5_PR	PC5_UW	PC5_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC6_NS	PC6_PW	PC6_PR	PC6_UW	PC6_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC7_NS	PC7_PW	PC7_PR	PC7_UW	PC7_UR

Bits	Name	Description
28	PC7_NS	Protection context 7, non-secure. Default Value: 1
27	PC7_PW	Protection context 7, privileged write enable. Default Value: 1
26	PC7_PR	Protection context 7, privileged read enable. Default Value: 1
25	PC7_UW	Protection context 7, user write enable. Default Value: 1
24	PC7_UR	Protection context 7, user read enable. Default Value: 1
20	PC6_NS	Protection context 6, non-secure. Default Value: 1
19	PC6_PW	Protection context 6, privileged write enable. Default Value: 1
18	PC6_PR	Protection context 6, privileged read enable. Default Value: 1
17	PC6_UW	Protection context 6, user write enable. Default Value: 1
16	PC6_UR	Protection context 6, user read enable. Default Value: 1

12	PC5_NS	Protection context 5, non-secure. Default Value: 1
11	PC5_PW	Protection context 5, privileged write enable. Default Value: 1
10	PC5_PR	Protection context 5, privileged read enable. Default Value: 1
9	PC5_UW	Protection context 5, user write enable. Default Value: 1
8	PC5_UR	Protection context 5, user read enable. Default Value: 1
4	PC4_NS	Protection context 4, non-secure. Default Value: 1
3	PC4_PW	Protection context 4, privileged write enable. Default Value: 1
2	PC4_PR	Protection context 4, privileged read enable. Default Value: 1
1	PC4_UW	Protection context 4, user write enable. Default Value: 1
0	PC4_UR	Protection context 4, user read enable. Default Value: 1

PERI_MS_PPU_FX0_MS_ATT2

Master attributes 2
Address: 0x40010838
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC8_NS	PC8_PW	PC8_PR	PC8_UW	PC8_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC9_NS	PC9_PW	PC9_PR	PC9_UW	PC9_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC10_NS	PC10_PW	PC10_PR	PC10_UW	PC10_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC11_NS	PC11_PW	PC11_PR	PC11_UW	PC11_UR

Bits	Name	Description
28	PC11_NS	Protection context 11, non-secure. Default Value: 1
27	PC11_PW	Protection context 11, privileged write enable. Default Value: 1
26	PC11_PR	Protection context 11, privileged read enable. Default Value: 1
25	PC11_UW	Protection context 11, user write enable. Default Value: 1
24	PC11_UR	Protection context 11, user read enable. Default Value: 1
20	PC10_NS	Protection context 10, non-secure. Default Value: 1
19	PC10_PW	Protection context 10, privileged write enable. Default Value: 1
18	PC10_PR	Protection context 10, privileged read enable. Default Value: 1
17	PC10_UW	Protection context 10, user write enable. Default Value: 1
16	PC10_UR	Protection context 10, user read enable. Default Value: 1

12	PC9_NS	Protection context 9, non-secure. Default Value: 1
11	PC9_PW	Protection context 9, privileged write enable. Default Value: 1
10	PC9_PR	Protection context 9, privileged read enable. Default Value: 1
9	PC9_UW	Protection context 9, user write enable. Default Value: 1
8	PC9_UR	Protection context 9, user read enable. Default Value: 1
4	PC8_NS	Protection context 8, non-secure. Default Value: 1
3	PC8_PW	Protection context 8, privileged write enable. Default Value: 1
2	PC8_PR	Protection context 8, privileged read enable. Default Value: 1
1	PC8_UW	Protection context 8, user write enable. Default Value: 1
0	PC8_UR	Protection context 8, user read enable. Default Value: 1

PERI_MS_PPU_FX0_MS_ATT3

Master attributes 3
Address: 0x4001083C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC12_NS	PC12_PW	PC12_PR	PC12_UW	PC12_UR
Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC13_NS	PC13_PW	PC13_PR	PC13_UW	PC13_UR
Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC14_NS	PC14_PW	PC14_PR	PC14_UW	PC14_UR
Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC15_NS	PC15_PW	PC15_PR	PC15_UW	PC15_UR

Bits	Name	Description
28	PC15_NS	Protection context 15, non-secure. Default Value: 1
27	PC15_PW	Protection context 15, privileged write enable. Default Value: 1
26	PC15_PR	Protection context 15, privileged read enable. Default Value: 1
25	PC15_UW	Protection context 15, user write enable. Default Value: 1
24	PC15_UR	Protection context 15, user read enable. Default Value: 1
20	PC14_NS	Protection context 14, non-secure. Default Value: 1
19	PC14_PW	Protection context 14, privileged write enable. Default Value: 1
18	PC14_PR	Protection context 14, privileged read enable. Default Value: 1
17	PC14_UW	Protection context 14, user write enable. Default Value: 1
16	PC14_UR	Protection context 14, user read enable. Default Value: 1

12	PC13_NS	Protection context 13, non-secure. Default Value: 1
11	PC13_PW	Protection context 13, privileged write enable. Default Value: 1
10	PC13_PR	Protection context 13, privileged read enable. Default Value: 1
9	PC13_UW	Protection context 13, user write enable. Default Value: 1
8	PC13_UR	Protection context 13, user read enable. Default Value: 1
4	PC12_NS	Protection context 12, non-secure. Default Value: 1
3	PC12_PW	Protection context 12, privileged write enable. Default Value: 1
2	PC12_PR	Protection context 12, privileged read enable. Default Value: 1
1	PC12_UW	Protection context 12, user write enable. Default Value: 1
0	PC12_UR	Protection context 12, user read enable. Default Value: 1

PERI_MS_PPU_FX1_SL_ADDR

Slave region, base address
Address: 0x40010840
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268437504

PERI_MS_PPU_FX1_SL_SIZE

Slave region, size
Address: 0x40010844
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1
28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 1

PERI_MS_PPU_FX1_MS_ADDR

Master region, base address
Address: 0x40010860
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778273

PERI_MS_PPU_FX2_SL_ADDR

Slave region, base address
Address: 0x40010880
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268439556

PERI_MS_PPU_FX2_MS_ADDR

Master region, base address
Address: 0x400108A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778274

PERI_MS_PPU_FX3_SL_ADDR

Slave region, base address
Address: 0x400108C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268439564

PERI_MS_PPU_FX3_MS_ADDR

Master region, base address
Address: 0x400108E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778275

PERI_MS_PPU_FX4_SL_ADDR

Slave region, base address
Address: 0x40010900
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268439572

PERI_MS_PPU_FX4_MS_ADDR

Master region, base address
Address: 0x40010920
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778276

PERI_MS_PPU_FX5_SL_ADDR

Slave region, base address
Address: 0x40010940
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268439576

PERI_MS_PPU_FX5_SL_SIZE

Slave region, size
Address: 0x40010944
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1
28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 4

PERI_MS_PPU_FX5_MS_ADDR

Master region, base address
Address: 0x40010960
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778277

PERI_MS_PPU_FX6_SL_ADDR

Slave region, base address
Address: 0x40010980
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268439592

PERI_MS_PPU_FX6_MS_ADDR

Master region, base address
Address: 0x400109A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778278

PERI_MS_PPU_FX7_SL_ADDR

Slave region, base address
Address: 0x400109C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268439600

PERI_MS_PPU_FX7_MS_ADDR

Master region, base address
Address: 0x400109E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778279

PERI_MS_PPU_FX8_SL_ADDR

Slave region, base address
Address: 0x40010A00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268439624

PERI_MS_PPU_FX8_MS_ADDR

Master region, base address
Address: 0x40010A20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778280

PERI_MS_PPU_FX9_SL_ADDR

Slave region, base address
Address: 0x40010A40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268443648

PERI_MS_PPU_FX9_SL_SIZE

Slave region, size
Address: 0x40010A44
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1
28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 14

PERI_MS_PPU_FX9_MS_ADDR

Master region, base address
Address: 0x40010A60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778281

PERI_MS_PPU_FX10_SL_ADDR

Slave region, base address
Address: 0x40010A80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268697600

PERI_MS_PPU_FX10_SL_SIZE

Slave region, size
Address: 0x40010A84
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1
28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 9

PERI_MS_PPU_FX10_MS_ADDR

Master region, base address
Address: 0x40010AA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778282

PERI_MS_PPU_FX11_SL_ADDR

Slave region, base address
Address: 0x40010AC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268698624

PERI_MS_PPU_FX11_SL_SIZE

Slave region, size
Address: 0x40010AC4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1
28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 10

PERI_MS_PPU_FX11_MS_ADDR

Master region, base address
Address: 0x40010AE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778283

PERI_MS_PPU_FX12_SL_ADDR

Slave region, base address
Address: 0x40010B00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268699648

PERI_MS_PPU_FX12_SL_SIZE

Slave region, size
Address: 0x40010B04
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1
28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 7

PERI_MS_PPU_FX12_MS_ADDR

Master region, base address
Address: 0x40010B20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778284

PERI_MS_PPU_FX13_SL_ADDR

Slave region, base address
Address: 0x40010B40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268699712

PERI_MS_PPU_FX13_MS_ADDR

Master region, base address
Address: 0x40010B60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778285

PERI_MS_PPU_FX14_SL_ADDR

Slave region, base address
Address: 0x40010B80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268699720

PERI_MS_PPU_FX14_MS_ADDR

Master region, base address
Address: 0x40010BA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778286

PERI_MS_PPU_FX15_SL_ADDR

Slave region, base address
Address: 0x40010BC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268705792

PERI_MS_PPU_FX15_MS_ADDR

Master region, base address
Address: 0x40010BE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778287

PERI_MS_PPU_FX16_SL_ADDR

Slave region, base address
Address: 0x40010C00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268959744

PERI_MS_PPU_FX16_MS_ADDR

Master region, base address
Address: 0x40010C20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778288

PERI_MS_PPU_FX17_SL_ADDR

Slave region, base address
Address: 0x40010C40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268960768

PERI_MS_PPU_FX17_SL_SIZE

Slave region, size
Address: 0x40010C44
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1
28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 11

PERI_MS_PPU_FX17_MS_ADDR

Master region, base address
Address: 0x40010C60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778289

PERI_MS_PPU_FX18_SL_ADDR

Slave region, base address
Address: 0x40010C80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268961792

PERI_MS_PPU_FX18_SL_SIZE

Slave region, size
Address: 0x40010C84
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1
28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 8

PERI_MS_PPU_FX18_MS_ADDR

Master region, base address
Address: 0x40010CA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778290

PERI_MS_PPU_FX19_SL_ADDR

Slave region, base address
Address: 0x40010CC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268967936

PERI_MS_PPU_FX19_MS_ADDR

Master region, base address
Address: 0x40010CE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778291

PERI_MS_PPU_FX20_SL_ADDR

Slave region, base address
Address: 0x40010D00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268969984

PERI_MS_PPU_FX20_MS_ADDR

Master region, base address
Address: 0x40010D20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778292

PERI_MS_PPU_FX21_SL_ADDR

Slave region, base address
Address: 0x40010D40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268976128

PERI_MS_PPU_FX21_MS_ADDR

Master region, base address
Address: 0x40010D60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778293

PERI_MS_PPU_FX22_SL_ADDR

Slave region, base address
Address: 0x40010D80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268976192

PERI_MS_PPU_FX22_MS_ADDR

Master region, base address
Address: 0x40010DA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778294

PERI_MS_PPU_FX23_SL_ADDR

Slave region, base address
Address: 0x40010DC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268976256

PERI_MS_PPU_FX23_MS_ADDR

Master region, base address
Address: 0x40010DE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778295

PERI_MS_PPU_FX24_SL_ADDR

Slave region, base address
Address: 0x40010E00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268976320

PERI_MS_PPU_FX24_MS_ADDR

Master region, base address
Address: 0x40010E20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778296

PERI_MS_PPU_FX25_SL_ADDR

Slave region, base address
Address: 0x40010E40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268992512

PERI_MS_PPU_FX25_MS_ADDR

Master region, base address
Address: 0x40010E60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778297

PERI_MS_PPU_FX26_SL_ADDR

Slave region, base address
Address: 0x40010E80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268992520

PERI_MS_PPU_FX26_MS_ADDR

Master region, base address
Address: 0x40010EA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778298

PERI_MS_PPU_FX27_SL_ADDR

Slave region, base address
Address: 0x40010EC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268992528

PERI_MS_PPU_FX27_MS_ADDR

Master region, base address
Address: 0x40010EE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778299

PERI_MS_PPU_FX28_SL_ADDR

Slave region, base address
Address: 0x40010F00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268992536

PERI_MS_PPU_FX28_MS_ADDR

Master region, base address
Address: 0x40010F20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778300

PERI_MS_PPU_FX29_SL_ADDR

Slave region, base address
Address: 0x40010F40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268992544

PERI_MS_PPU_FX29_MS_ADDR

Master region, base address
Address: 0x40010F60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778301

PERI_MS_PPU_FX30_SL_ADDR

Slave region, base address
Address: 0x40010F80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268992552

PERI_MS_PPU_FX30_MS_ADDR

Master region, base address
Address: 0x40010FA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778302

PERI_MS_PPU_FX31_SL_ADDR

Slave region, base address
Address: 0x40010FC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268992560

PERI_MS_PPU_FX31_MS_ADDR

Master region, base address
Address: 0x40010FE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778303

PERI_MS_PPU_FX32_SL_ADDR

Slave region, base address
Address: 0x40011000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268992568

PERI_MS_PPU_FX32_MS_ADDR

Master region, base address
Address: 0x40011020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778304

PERI_MS_PPU_FX33_SL_ADDR

Slave region, base address
Address: 0x40011040
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268993536

PERI_MS_PPU_FX33_SL_SIZE

Slave region, size
Address: 0x40011044
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1
28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 3

PERI_MS_PPU_FX33_MS_ADDR

Master region, base address
Address: 0x40011060
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778305

PERI_MS_PPU_FX34_SL_ADDR

Slave region, base address
Address: 0x40011080
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268993544

PERI_MS_PPU_FX34_MS_ADDR

Master region, base address
Address: 0x400110A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778306

PERI_MS_PPU_FX35_SL_ADDR

Slave region, base address
Address: 0x400110C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268993552

PERI_MS_PPU_FX35_MS_ADDR

Master region, base address
Address: 0x400110E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778307

PERI_MS_PPU_FX36_SL_ADDR

Slave region, base address
Address: 0x40011100
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268993560

PERI_MS_PPU_FX36_MS_ADDR

Master region, base address
Address: 0x40011120
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778308

PERI_MS_PPU_FX37_SL_ADDR

Slave region, base address
Address: 0x40011140
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268993568

PERI_MS_PPU_FX37_MS_ADDR

Master region, base address
Address: 0x40011160
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778309

PERI_MS_PPU_FX38_SL_ADDR

Slave region, base address
Address: 0x40011180
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268993576

PERI_MS_PPU_FX38_MS_ADDR

Master region, base address
Address: 0x400111A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778310

PERI_MS_PPU_FX39_SL_ADDR

Slave region, base address
Address: 0x400111C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268993584

PERI_MS_PPU_FX39_MS_ADDR

Master region, base address
Address: 0x400111E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778311

PERI_MS_PPU_FX40_SL_ADDR

Slave region, base address
Address: 0x40011200
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268993592

PERI_MS_PPU_FX40_MS_ADDR

Master region, base address
Address: 0x40011220
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778312

PERI_MS_PPU_FX41_SL_ADDR

Slave region, base address
Address: 0x40011240
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269008896

PERI_MS_PPU_FX41_SL_SIZE

Slave region, size
Address: 0x40011244
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1
28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 5

PERI_MS_PPU_FX41_MS_ADDR

Master region, base address
Address: 0x40011260
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778313

PERI_MS_PPU_FX42_SL_ADDR

Slave region, base address
Address: 0x40011280
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269012992

PERI_MS_PPU_FX42_MS_ADDR

Master region, base address
Address: 0x400112A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778314

PERI_MS_PPU_FX43_SL_ADDR

Slave region, base address
Address: 0x400112C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269016576

PERI_MS_PPU_FX43_MS_ADDR

Master region, base address
Address: 0x400112E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778315

PERI_MS_PPU_FX44_SL_ADDR

Slave region, base address
Address: 0x40011300
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269016832

PERI_MS_PPU_FX44_MS_ADDR

Master region, base address
Address: 0x40011320
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778316

PERI_MS_PPU_FX45_SL_ADDR

Slave region, base address
Address: 0x40011340
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269025280

PERI_MS_PPU_FX45_SL_SIZE

Slave region, size
Address: 0x40011344
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1
28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 2

PERI_MS_PPU_FX45_MS_ADDR

Master region, base address
Address: 0x40011360
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778317

PERI_MS_PPU_FX46_SL_ADDR

Slave region, base address
Address: 0x40011380
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269025282

PERI_MS_PPU_FX46_MS_ADDR

Master region, base address
Address: 0x400113A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778318

PERI_MS_PPU_FX47_SL_ADDR

Slave region, base address
Address: 0x400113C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269025408

PERI_MS_PPU_FX47_MS_ADDR

Master region, base address
Address: 0x400113E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778319

PERI_MS_PPU_FX48_SL_ADDR

Slave region, base address
Address: 0x40011400
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269025536

PERI_MS_PPU_FX48_SL_SIZE

Slave region, size
Address: 0x40011404
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1
28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 6

PERI_MS_PPU_FX48_MS_ADDR

Master region, base address
Address: 0x40011420
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778320

PERI_MS_PPU_FX49_SL_ADDR

Slave region, base address
Address: 0x40011440
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269025568

PERI_MS_PPU_FX49_MS_ADDR

Master region, base address
Address: 0x40011460
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778321

PERI_MS_PPU_FX50_SL_ADDR

Slave region, base address
Address: 0x40011480
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269025600

PERI_MS_PPU_FX50_MS_ADDR

Master region, base address
Address: 0x400114A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778322

PERI_MS_PPU_FX51_SL_ADDR

Slave region, base address
Address: 0x400114C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269025632

PERI_MS_PPU_FX51_MS_ADDR

Master region, base address
Address: 0x400114E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778323

PERI_MS_PPU_FX52_SL_ADDR

Slave region, base address
Address: 0x40011500
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269025664

PERI_MS_PPU_FX52_MS_ADDR

Master region, base address
Address: 0x40011520
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778324

PERI_MS_PPU_FX53_SL_ADDR

Slave region, base address
Address: 0x40011540
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269025696

PERI_MS_PPU_FX53_MS_ADDR

Master region, base address
Address: 0x40011560
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778325

PERI_MS_PPU_FX54_SL_ADDR

Slave region, base address
Address: 0x40011580
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269040640

PERI_MS_PPU_FX54_MS_ADDR

Master region, base address
Address: 0x400115A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778326

PERI_MS_PPU_FX55_SL_ADDR

Slave region, base address
Address: 0x400115C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269040896

PERI_MS_PPU_FX55_MS_ADDR

Master region, base address
Address: 0x400115E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778327

PERI_MS_PPU_FX56_SL_ADDR

Slave region, base address
Address: 0x40011600
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269040960

PERI_MS_PPU_FX56_MS_ADDR

Master region, base address
Address: 0x40011620
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778328

PERI_MS_PPU_FX57_SL_ADDR

Slave region, base address
Address: 0x40011640
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269058048

PERI_MS_PPU_FX57_MS_ADDR

Master region, base address
Address: 0x40011660
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778329

PERI_MS_PPU_FX58_SL_ADDR

Slave region, base address
Address: 0x40011680
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269059072

PERI_MS_PPU_FX58_MS_ADDR

Master region, base address
Address: 0x400116A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778330

PERI_MS_PPU_FX59_SL_ADDR

Slave region, base address
Address: 0x400116C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269060096

PERI_MS_PPU_FX59_MS_ADDR

Master region, base address
Address: 0x400116E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778331

PERI_MS_PPU_FX60_SL_ADDR

Slave region, base address
Address: 0x40011700
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269066240

PERI_MS_PPU_FX60_MS_ADDR

Master region, base address
Address: 0x40011720
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778332

PERI_MS_PPU_FX61_SL_ADDR

Slave region, base address
Address: 0x40011740
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269066304

PERI_MS_PPU_FX61_MS_ADDR

Master region, base address
Address: 0x40011760
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778333

PERI_MS_PPU_FX62_SL_ADDR

Slave region, base address
Address: 0x40011780
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269066272

PERI_MS_PPU_FX62_MS_ADDR

Master region, base address
Address: 0x400117A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778334

PERI_MS_PPU_FX63_SL_ADDR

Slave region, base address
Address: 0x400117C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269066336

PERI_MS_PPU_FX63_MS_ADDR

Master region, base address
Address: 0x400117E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778335

PERI_MS_PPU_FX64_SL_ADDR

Slave region, base address
Address: 0x40011800
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269070336

PERI_MS_PPU_FX64_MS_ADDR

Master region, base address
Address: 0x40011820
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778336

PERI_MS_PPU_FX65_SL_ADDR

Slave region, base address
Address: 0x40011840
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269070352

PERI_MS_PPU_FX65_MS_ADDR

Master region, base address
Address: 0x40011860
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778337

PERI_MS_PPU_FX66_SL_ADDR

Slave region, base address
Address: 0x40011880
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269074432

PERI_MS_PPU_FX66_SL_SIZE

Slave region, size
Address: 0x40011884
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1
28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 15

PERI_MS_PPU_FX66_MS_ADDR

Master region, base address
Address: 0x400118A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778338

PERI_MS_PPU_FX67_SL_ADDR

Slave region, base address
Address: 0x400118C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269090816

PERI_MS_PPU_FX67_MS_ADDR

Master region, base address
Address: 0x400118E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778339

PERI_MS_PPU_FX68_SL_ADDR

Slave region, base address
Address: 0x40011900
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269107200

PERI_MS_PPU_FX68_MS_ADDR

Master region, base address
Address: 0x40011920
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778340

PERI_MS_PPU_FX69_SL_ADDR

Slave region, base address
Address: 0x40011940
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269090880

PERI_MS_PPU_FX69_MS_ADDR

Master region, base address
Address: 0x40011960
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778341

PERI_MS_PPU_FX70_SL_ADDR

Slave region, base address
Address: 0x40011980
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269107264

PERI_MS_PPU_FX70_MS_ADDR

Master region, base address
Address: 0x400119A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778342

PERI_MS_PPU_FX71_SL_ADDR

Slave region, base address
Address: 0x400119C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099008

PERI_MS_PPU_FX71_MS_ADDR

Master region, base address
Address: 0x400119E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778343

PERI_MS_PPU_FX72_SL_ADDR

Slave region, base address
Address: 0x40011A00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099024

PERI_MS_PPU_FX72_MS_ADDR

Master region, base address
Address: 0x40011A20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778344

PERI_MS_PPU_FX73_SL_ADDR

Slave region, base address
Address: 0x40011A40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099040

PERI_MS_PPU_FX73_MS_ADDR

Master region, base address
Address: 0x40011A60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778345

PERI_MS_PPU_FX74_SL_ADDR

Slave region, base address
Address: 0x40011A80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099056

PERI_MS_PPU_FX74_MS_ADDR

Master region, base address
Address: 0x40011AA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778346

PERI_MS_PPU_FX75_SL_ADDR

Slave region, base address
Address: 0x40011AC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099072

PERI_MS_PPU_FX75_MS_ADDR

Master region, base address
Address: 0x40011AE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778347

PERI_MS_PPU_FX76_SL_ADDR

Slave region, base address
Address: 0x40011B00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099088

PERI_MS_PPU_FX76_MS_ADDR

Master region, base address
Address: 0x40011B20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778348

PERI_MS_PPU_FX77_SL_ADDR

Slave region, base address
Address: 0x40011B40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099104

PERI_MS_PPU_FX77_MS_ADDR

Master region, base address
Address: 0x40011B60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778349

PERI_MS_PPU_FX78_SL_ADDR

Slave region, base address
Address: 0x40011B80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099120

PERI_MS_PPU_FX78_MS_ADDR

Master region, base address
Address: 0x40011BA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778350

PERI_MS_PPU_FX79_SL_ADDR

Slave region, base address
Address: 0x40011BC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099136

PERI_MS_PPU_FX79_MS_ADDR

Master region, base address
Address: 0x40011BE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778351

PERI_MS_PPU_FX80_SL_ADDR

Slave region, base address
Address: 0x40011C00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099152

PERI_MS_PPU_FX80_MS_ADDR

Master region, base address
Address: 0x40011C20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778352

PERI_MS_PPU_FX81_SL_ADDR

Slave region, base address
Address: 0x40011C40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099168

PERI_MS_PPU_FX81_MS_ADDR

Master region, base address
Address: 0x40011C60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778353

PERI_MS_PPU_FX82_SL_ADDR

Slave region, base address
Address: 0x40011C80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099184

PERI_MS_PPU_FX82_MS_ADDR

Master region, base address
Address: 0x40011CA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778354

PERI_MS_PPU_FX83_SL_ADDR

Slave region, base address
Address: 0x40011CC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099200

PERI_MS_PPU_FX83_MS_ADDR

Master region, base address
Address: 0x40011CE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778355

PERI_MS_PPU_FX84_SL_ADDR

Slave region, base address
Address: 0x40011D00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099216

PERI_MS_PPU_FX84_MS_ADDR

Master region, base address
Address: 0x40011D20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778356

PERI_MS_PPU_FX85_SL_ADDR

Slave region, base address
Address: 0x40011D40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099232

PERI_MS_PPU_FX85_MS_ADDR

Master region, base address
Address: 0x40011D60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778357

PERI_MS_PPU_FX86_SL_ADDR

Slave region, base address
Address: 0x40011D80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099248

PERI_MS_PPU_FX86_MS_ADDR

Master region, base address
Address: 0x40011DA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778358

PERI_MS_PPU_FX87_SL_ADDR

Slave region, base address
Address: 0x40011DC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099264

PERI_MS_PPU_FX87_MS_ADDR

Master region, base address
Address: 0x40011DE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778359

PERI_MS_PPU_FX88_SL_ADDR

Slave region, base address
Address: 0x40011E00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099280

PERI_MS_PPU_FX88_MS_ADDR

Master region, base address
Address: 0x40011E20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778360

PERI_MS_PPU_FX89_SL_ADDR

Slave region, base address
Address: 0x40011E40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099296

PERI_MS_PPU_FX89_MS_ADDR

Master region, base address
Address: 0x40011E60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778361

PERI_MS_PPU_FX90_SL_ADDR

Slave region, base address
Address: 0x40011E80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099312

PERI_MS_PPU_FX90_MS_ADDR

Master region, base address
Address: 0x40011EA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778362

PERI_MS_PPU_FX91_SL_ADDR

Slave region, base address
Address: 0x40011EC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099328

PERI_MS_PPU_FX91_MS_ADDR

Master region, base address
Address: 0x40011EE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778363

PERI_MS_PPU_FX92_SL_ADDR

Slave region, base address
Address: 0x40011F00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099344

PERI_MS_PPU_FX92_MS_ADDR

Master region, base address
Address: 0x40011F20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778364

PERI_MS_PPU_FX93_SL_ADDR

Slave region, base address
Address: 0x40011F40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099360

PERI_MS_PPU_FX93_MS_ADDR

Master region, base address
Address: 0x40011F60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778365

PERI_MS_PPU_FX94_SL_ADDR

Slave region, base address
Address: 0x40011F80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099376

PERI_MS_PPU_FX94_MS_ADDR

Master region, base address
Address: 0x40011FA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778366

PERI_MS_PPU_FX95_SL_ADDR

Slave region, base address
Address: 0x40011FC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099392

PERI_MS_PPU_FX95_MS_ADDR

Master region, base address
Address: 0x40011FE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778367

PERI_MS_PPU_FX96_SL_ADDR

Slave region, base address
Address: 0x40012000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099408

PERI_MS_PPU_FX96_MS_ADDR

Master region, base address
Address: 0x40012020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778368

PERI_MS_PPU_FX97_SL_ADDR

Slave region, base address
Address: 0x40012040
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099424

PERI_MS_PPU_FX97_MS_ADDR

Master region, base address
Address: 0x40012060
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778369

PERI_MS_PPU_FX98_SL_ADDR

Slave region, base address
Address: 0x40012080
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099440

PERI_MS_PPU_FX98_MS_ADDR

Master region, base address
Address: 0x400120A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778370

PERI_MS_PPU_FX99_SL_ADDR

Slave region, base address
Address: 0x400120C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099456

PERI_MS_PPU_FX99_MS_ADDR

Master region, base address
Address: 0x400120E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778371

PERI_MS_PPU_FX100_SL_ADDR

Slave region, base address
Address: 0x40012100
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099472

PERI_MS_PPU_FX100_MS_ADDR

Master region, base address
Address: 0x40012120
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778372

PERI_MS_PPU_FX101_SL_ADDR

Slave region, base address
Address: 0x40012140
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099488

PERI_MS_PPU_FX101_MS_ADDR

Master region, base address
Address: 0x40012160
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778373

PERI_MS_PPU_FX102_SL_ADDR

Slave region, base address
Address: 0x40012180
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099504

PERI_MS_PPU_FX102_MS_ADDR

Master region, base address
Address: 0x400121A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778374

PERI_MS_PPU_FX103_SL_ADDR

Slave region, base address
Address: 0x400121C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099520

PERI_MS_PPU_FX103_MS_ADDR

Master region, base address
Address: 0x400121E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778375

PERI_MS_PPU_FX104_SL_ADDR

Slave region, base address
Address: 0x40012200
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099536

PERI_MS_PPU_FX104_MS_ADDR

Master region, base address
Address: 0x40012220
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778376

PERI_MS_PPU_FX105_SL_ADDR

Slave region, base address
Address: 0x40012240
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099552

PERI_MS_PPU_FX105_MS_ADDR

Master region, base address
Address: 0x40012260
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778377

PERI_MS_PPU_FX106_SL_ADDR

Slave region, base address
Address: 0x40012280
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099568

PERI_MS_PPU_FX106_MS_ADDR

Master region, base address
Address: 0x400122A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778378

PERI_MS_PPU_FX107_SL_ADDR

Slave region, base address
Address: 0x400122C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099584

PERI_MS_PPU_FX107_MS_ADDR

Master region, base address
Address: 0x400122E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778379

PERI_MS_PPU_FX108_SL_ADDR

Slave region, base address
Address: 0x40012300
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099600

PERI_MS_PPU_FX108_MS_ADDR

Master region, base address
Address: 0x40012320
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778380

PERI_MS_PPU_FX109_SL_ADDR

Slave region, base address
Address: 0x40012340
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099616

PERI_MS_PPU_FX109_MS_ADDR

Master region, base address
Address: 0x40012360
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778381

PERI_MS_PPU_FX110_SL_ADDR

Slave region, base address
Address: 0x40012380
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099632

PERI_MS_PPU_FX110_MS_ADDR

Master region, base address
Address: 0x400123A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778382

PERI_MS_PPU_FX111_SL_ADDR

Slave region, base address
Address: 0x400123C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099648

PERI_MS_PPU_FX111_MS_ADDR

Master region, base address
Address: 0x400123E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778383

PERI_MS_PPU_FX112_SL_ADDR

Slave region, base address
Address: 0x40012400
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099664

PERI_MS_PPU_FX112_MS_ADDR

Master region, base address
Address: 0x40012420
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778384

PERI_MS_PPU_FX113_SL_ADDR

Slave region, base address
Address: 0x40012440
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099680

PERI_MS_PPU_FX113_MS_ADDR

Master region, base address
Address: 0x40012460
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778385

PERI_MS_PPU_FX114_SL_ADDR

Slave region, base address
Address: 0x40012480
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099696

PERI_MS_PPU_FX114_MS_ADDR

Master region, base address
Address: 0x400124A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778386

PERI_MS_PPU_FX115_SL_ADDR

Slave region, base address
Address: 0x400124C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099712

PERI_MS_PPU_FX115_MS_ADDR

Master region, base address
Address: 0x400124E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778387

PERI_MS_PPU_FX116_SL_ADDR

Slave region, base address
Address: 0x40012500
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099728

PERI_MS_PPU_FX116_MS_ADDR

Master region, base address
Address: 0x40012520
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778388

PERI_MS_PPU_FX117_SL_ADDR

Slave region, base address
Address: 0x40012540
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099744

PERI_MS_PPU_FX117_MS_ADDR

Master region, base address
Address: 0x40012560
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778389

PERI_MS_PPU_FX118_SL_ADDR

Slave region, base address
Address: 0x40012580
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099760

PERI_MS_PPU_FX118_MS_ADDR

Master region, base address
Address: 0x400125A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778390

PERI_MS_PPU_FX119_SL_ADDR

Slave region, base address
Address: 0x400125C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099776

PERI_MS_PPU_FX119_MS_ADDR

Master region, base address
Address: 0x400125E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778391

PERI_MS_PPU_FX120_SL_ADDR

Slave region, base address
Address: 0x40012600
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099792

PERI_MS_PPU_FX120_MS_ADDR

Master region, base address
Address: 0x40012620
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778392

PERI_MS_PPU_FX121_SL_ADDR

Slave region, base address
Address: 0x40012640
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099808

PERI_MS_PPU_FX121_MS_ADDR

Master region, base address
Address: 0x40012660
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778393

PERI_MS_PPU_FX122_SL_ADDR

Slave region, base address
Address: 0x40012680
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099824

PERI_MS_PPU_FX122_MS_ADDR

Master region, base address
Address: 0x400126A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778394

PERI_MS_PPU_FX123_SL_ADDR

Slave region, base address
Address: 0x400126C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099840

PERI_MS_PPU_FX123_MS_ADDR

Master region, base address
Address: 0x400126E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778395

PERI_MS_PPU_FX124_SL_ADDR

Slave region, base address
Address: 0x40012700
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099856

PERI_MS_PPU_FX124_MS_ADDR

Master region, base address
Address: 0x40012720
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778396

PERI_MS_PPU_FX125_SL_ADDR

Slave region, base address
Address: 0x40012740
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099872

PERI_MS_PPU_FX125_MS_ADDR

Master region, base address
Address: 0x40012760
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778397

PERI_MS_PPU_FX126_SL_ADDR

Slave region, base address
Address: 0x40012780
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099888

PERI_MS_PPU_FX126_MS_ADDR

Master region, base address
Address: 0x400127A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778398

PERI_MS_PPU_FX127_SL_ADDR

Slave region, base address
Address: 0x400127C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099904

PERI_MS_PPU_FX127_MS_ADDR

Master region, base address
Address: 0x400127E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778399

PERI_MS_PPU_FX128_SL_ADDR

Slave region, base address
Address: 0x40012800
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099920

PERI_MS_PPU_FX128_MS_ADDR

Master region, base address
Address: 0x40012820
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778400

PERI_MS_PPU_FX129_SL_ADDR

Slave region, base address
Address: 0x40012840
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099936

PERI_MS_PPU_FX129_MS_ADDR

Master region, base address
Address: 0x40012860
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778401

PERI_MS_PPU_FX130_SL_ADDR

Slave region, base address
Address: 0x40012880
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099952

PERI_MS_PPU_FX130_MS_ADDR

Master region, base address
Address: 0x400128A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778402

PERI_MS_PPU_FX131_SL_ADDR

Slave region, base address
Address: 0x400128C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099968

PERI_MS_PPU_FX131_MS_ADDR

Master region, base address
Address: 0x400128E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778403

PERI_MS_PPU_FX132_SL_ADDR

Slave region, base address
Address: 0x40012900
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099984

PERI_MS_PPU_FX132_MS_ADDR

Master region, base address
Address: 0x40012920
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778404

PERI_MS_PPU_FX133_SL_ADDR

Slave region, base address
Address: 0x40012940
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100000

PERI_MS_PPU_FX133_MS_ADDR

Master region, base address
Address: 0x40012960
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778405

PERI_MS_PPU_FX134_SL_ADDR

Slave region, base address
Address: 0x40012980
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100016

PERI_MS_PPU_FX134_MS_ADDR

Master region, base address
Address: 0x400129A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778406

PERI_MS_PPU_FX135_SL_ADDR

Slave region, base address
Address: 0x400129C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100032

PERI_MS_PPU_FX135_MS_ADDR

Master region, base address
Address: 0x400129E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778407

PERI_MS_PPU_FX136_SL_ADDR

Slave region, base address
Address: 0x40012A00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100048

PERI_MS_PPU_FX136_MS_ADDR

Master region, base address
Address: 0x40012A20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778408

PERI_MS_PPU_FX137_SL_ADDR

Slave region, base address
Address: 0x40012A40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100064

PERI_MS_PPU_FX137_MS_ADDR

Master region, base address
Address: 0x40012A60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778409

PERI_MS_PPU_FX138_SL_ADDR

Slave region, base address
Address: 0x40012A80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100080

PERI_MS_PPU_FX138_MS_ADDR

Master region, base address
Address: 0x40012AA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778410

PERI_MS_PPU_FX139_SL_ADDR

Slave region, base address
Address: 0x40012AC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100096

PERI_MS_PPU_FX139_MS_ADDR

Master region, base address
Address: 0x40012AE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778411

PERI_MS_PPU_FX140_SL_ADDR

Slave region, base address
Address: 0x40012B00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100112

PERI_MS_PPU_FX140_MS_ADDR

Master region, base address
Address: 0x40012B20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778412

PERI_MS_PPU_FX141_SL_ADDR

Slave region, base address
Address: 0x40012B40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100128

PERI_MS_PPU_FX141_MS_ADDR

Master region, base address
Address: 0x40012B60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778413

PERI_MS_PPU_FX142_SL_ADDR

Slave region, base address
Address: 0x40012B80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100144

PERI_MS_PPU_FX142_MS_ADDR

Master region, base address
Address: 0x40012BA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778414

PERI_MS_PPU_FX143_SL_ADDR

Slave region, base address
Address: 0x40012BC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100160

PERI_MS_PPU_FX143_MS_ADDR

Master region, base address
Address: 0x40012BE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778415

PERI_MS_PPU_FX144_SL_ADDR

Slave region, base address
Address: 0x40012C00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100176

PERI_MS_PPU_FX144_MS_ADDR

Master region, base address
Address: 0x40012C20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778416

PERI_MS_PPU_FX145_SL_ADDR

Slave region, base address
Address: 0x40012C40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100192

PERI_MS_PPU_FX145_MS_ADDR

Master region, base address
Address: 0x40012C60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778417

PERI_MS_PPU_FX146_SL_ADDR

Slave region, base address
Address: 0x40012C80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100208

PERI_MS_PPU_FX146_MS_ADDR

Master region, base address
Address: 0x40012CA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778418

PERI_MS_PPU_FX147_SL_ADDR

Slave region, base address
Address: 0x40012CC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100224

PERI_MS_PPU_FX147_MS_ADDR

Master region, base address
Address: 0x40012CE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778419

PERI_MS_PPU_FX148_SL_ADDR

Slave region, base address
Address: 0x40012D00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100240

PERI_MS_PPU_FX148_MS_ADDR

Master region, base address
Address: 0x40012D20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778420

PERI_MS_PPU_FX149_SL_ADDR

Slave region, base address
Address: 0x40012D40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100256

PERI_MS_PPU_FX149_MS_ADDR

Master region, base address
Address: 0x40012D60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778421

PERI_MS_PPU_FX150_SL_ADDR

Slave region, base address
Address: 0x40012D80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100272

PERI_MS_PPU_FX150_MS_ADDR

Master region, base address
Address: 0x40012DA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778422

PERI_MS_PPU_FX151_SL_ADDR

Slave region, base address
Address: 0x40012DC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100288

PERI_MS_PPU_FX151_MS_ADDR

Master region, base address
Address: 0x40012DE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778423

PERI_MS_PPU_FX152_SL_ADDR

Slave region, base address
Address: 0x40012E00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100304

PERI_MS_PPU_FX152_MS_ADDR

Master region, base address
Address: 0x40012E20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778424

PERI_MS_PPU_FX153_SL_ADDR

Slave region, base address
Address: 0x40012E40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100320

PERI_MS_PPU_FX153_MS_ADDR

Master region, base address
Address: 0x40012E60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778425

PERI_MS_PPU_FX154_SL_ADDR

Slave region, base address
Address: 0x40012E80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100336

PERI_MS_PPU_FX154_MS_ADDR

Master region, base address
Address: 0x40012EA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778426

PERI_MS_PPU_FX155_SL_ADDR

Slave region, base address
Address: 0x40012EC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100352

PERI_MS_PPU_FX155_MS_ADDR

Master region, base address
Address: 0x40012EE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778427

PERI_MS_PPU_FX156_SL_ADDR

Slave region, base address
Address: 0x40012F00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100368

PERI_MS_PPU_FX156_MS_ADDR

Master region, base address
Address: 0x40012F20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778428

PERI_MS_PPU_FX157_SL_ADDR

Slave region, base address
Address: 0x40012F40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100384

PERI_MS_PPU_FX157_MS_ADDR

Master region, base address
Address: 0x40012F60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778429

PERI_MS_PPU_FX158_SL_ADDR

Slave region, base address
Address: 0x40012F80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100400

PERI_MS_PPU_FX158_MS_ADDR

Master region, base address
Address: 0x40012FA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778430

PERI_MS_PPU_FX159_SL_ADDR

Slave region, base address
Address: 0x40012FC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269100416

PERI_MS_PPU_FX159_MS_ADDR

Master region, base address
Address: 0x40012FE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778431

PERI_MS_PPU_FX160_SL_ADDR

Slave region, base address
Address: 0x40013000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115392

PERI_MS_PPU_FX160_MS_ADDR

Master region, base address
Address: 0x40013020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778432

PERI_MS_PPU_FX161_SL_ADDR

Slave region, base address
Address: 0x40013040
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115408

PERI_MS_PPU_FX161_MS_ADDR

Master region, base address
Address: 0x40013060
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778433

PERI_MS_PPU_FX162_SL_ADDR

Slave region, base address
Address: 0x40013080
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115424

PERI_MS_PPU_FX162_MS_ADDR

Master region, base address
Address: 0x400130A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778434

PERI_MS_PPU_FX163_SL_ADDR

Slave region, base address
Address: 0x400130C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115440

PERI_MS_PPU_FX163_MS_ADDR

Master region, base address
Address: 0x400130E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778435

PERI_MS_PPU_FX164_SL_ADDR

Slave region, base address
Address: 0x40013100
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115456

PERI_MS_PPU_FX164_MS_ADDR

Master region, base address
Address: 0x40013120
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778436

PERI_MS_PPU_FX165_SL_ADDR

Slave region, base address
Address: 0x40013140
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115472

PERI_MS_PPU_FX165_MS_ADDR

Master region, base address
Address: 0x40013160
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778437

PERI_MS_PPU_FX166_SL_ADDR

Slave region, base address
Address: 0x40013180
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115488

PERI_MS_PPU_FX166_MS_ADDR

Master region, base address
Address: 0x400131A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778438

PERI_MS_PPU_FX167_SL_ADDR

Slave region, base address
Address: 0x400131C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115504

PERI_MS_PPU_FX167_MS_ADDR

Master region, base address
Address: 0x400131E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778439

PERI_MS_PPU_FX168_SL_ADDR

Slave region, base address
Address: 0x40013200
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115520

PERI_MS_PPU_FX168_MS_ADDR

Master region, base address
Address: 0x40013220
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778440

PERI_MS_PPU_FX169_SL_ADDR

Slave region, base address
Address: 0x40013240
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115536

PERI_MS_PPU_FX169_MS_ADDR

Master region, base address
Address: 0x40013260
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778441

PERI_MS_PPU_FX170_SL_ADDR

Slave region, base address
Address: 0x40013280
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115552

PERI_MS_PPU_FX170_MS_ADDR

Master region, base address
Address: 0x400132A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778442

PERI_MS_PPU_FX171_SL_ADDR

Slave region, base address
Address: 0x400132C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115568

PERI_MS_PPU_FX171_MS_ADDR

Master region, base address
Address: 0x400132E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778443

PERI_MS_PPU_FX172_SL_ADDR

Slave region, base address
Address: 0x40013300
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115584

PERI_MS_PPU_FX172_MS_ADDR

Master region, base address
Address: 0x40013320
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778444

PERI_MS_PPU_FX173_SL_ADDR

Slave region, base address
Address: 0x40013340
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115600

PERI_MS_PPU_FX173_MS_ADDR

Master region, base address
Address: 0x40013360
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778445

PERI_MS_PPU_FX174_SL_ADDR

Slave region, base address
Address: 0x40013380
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115616

PERI_MS_PPU_FX174_MS_ADDR

Master region, base address
Address: 0x400133A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778446

PERI_MS_PPU_FX175_SL_ADDR

Slave region, base address
Address: 0x400133C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115632

PERI_MS_PPU_FX175_MS_ADDR

Master region, base address
Address: 0x400133E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778447

PERI_MS_PPU_FX176_SL_ADDR

Slave region, base address
Address: 0x40013400
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115648

PERI_MS_PPU_FX176_MS_ADDR

Master region, base address
Address: 0x40013420
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778448

PERI_MS_PPU_FX177_SL_ADDR

Slave region, base address
Address: 0x40013440
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115664

PERI_MS_PPU_FX177_MS_ADDR

Master region, base address
Address: 0x40013460
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778449

PERI_MS_PPU_FX178_SL_ADDR

Slave region, base address
Address: 0x40013480
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115680

PERI_MS_PPU_FX178_MS_ADDR

Master region, base address
Address: 0x400134A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778450

PERI_MS_PPU_FX179_SL_ADDR

Slave region, base address
Address: 0x400134C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115696

PERI_MS_PPU_FX179_MS_ADDR

Master region, base address
Address: 0x400134E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778451

PERI_MS_PPU_FX180_SL_ADDR

Slave region, base address
Address: 0x40013500
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115712

PERI_MS_PPU_FX180_MS_ADDR

Master region, base address
Address: 0x40013520
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778452

PERI_MS_PPU_FX181_SL_ADDR

Slave region, base address
Address: 0x40013540
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115728

PERI_MS_PPU_FX181_MS_ADDR

Master region, base address
Address: 0x40013560
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778453

PERI_MS_PPU_FX182_SL_ADDR

Slave region, base address
Address: 0x40013580
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115744

PERI_MS_PPU_FX182_MS_ADDR

Master region, base address
Address: 0x400135A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778454

PERI_MS_PPU_FX183_SL_ADDR

Slave region, base address
Address: 0x400135C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115760

PERI_MS_PPU_FX183_MS_ADDR

Master region, base address
Address: 0x400135E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778455

PERI_MS_PPU_FX184_SL_ADDR

Slave region, base address
Address: 0x40013600
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115776

PERI_MS_PPU_FX184_MS_ADDR

Master region, base address
Address: 0x40013620
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778456

PERI_MS_PPU_FX185_SL_ADDR

Slave region, base address
Address: 0x40013640
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115792

PERI_MS_PPU_FX185_MS_ADDR

Master region, base address
Address: 0x40013660
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778457

PERI_MS_PPU_FX186_SL_ADDR

Slave region, base address
Address: 0x40013680
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115808

PERI_MS_PPU_FX186_MS_ADDR

Master region, base address
Address: 0x400136A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778458

PERI_MS_PPU_FX187_SL_ADDR

Slave region, base address
Address: 0x400136C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115824

PERI_MS_PPU_FX187_MS_ADDR

Master region, base address
Address: 0x400136E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778459

PERI_MS_PPU_FX188_SL_ADDR

Slave region, base address
Address: 0x40013700
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115840

PERI_MS_PPU_FX188_MS_ADDR

Master region, base address
Address: 0x40013720
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778460

PERI_MS_PPU_FX189_SL_ADDR

Slave region, base address
Address: 0x40013740
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115856

PERI_MS_PPU_FX189_MS_ADDR

Master region, base address
Address: 0x40013760
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778461

PERI_MS_PPU_FX190_SL_ADDR

Slave region, base address
Address: 0x40013780
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115872

PERI_MS_PPU_FX190_MS_ADDR

Master region, base address
Address: 0x400137A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778462

PERI_MS_PPU_FX191_SL_ADDR

Slave region, base address
Address: 0x400137C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115888

PERI_MS_PPU_FX191_MS_ADDR

Master region, base address
Address: 0x400137E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778463

PERI_MS_PPU_FX192_SL_ADDR

Slave region, base address
Address: 0x40013800
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115904

PERI_MS_PPU_FX192_MS_ADDR

Master region, base address
Address: 0x40013820
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778464

PERI_MS_PPU_FX193_SL_ADDR

Slave region, base address
Address: 0x40013840
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269123584

PERI_MS_PPU_FX193_MS_ADDR

Master region, base address
Address: 0x40013860
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778465

PERI_MS_PPU_FX194_SL_ADDR

Slave region, base address
Address: 0x40013880
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269124608

PERI_MS_PPU_FX194_MS_ADDR

Master region, base address
Address: 0x400138A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778466

PERI_MS_PPU_FX195_SL_ADDR

Slave region, base address
Address: 0x400138C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269124672

PERI_MS_PPU_FX195_MS_ADDR

Master region, base address
Address: 0x400138E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778467

PERI_MS_PPU_FX196_SL_ADDR

Slave region, base address
Address: 0x40013900
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269124736

PERI_MS_PPU_FX196_MS_ADDR

Master region, base address
Address: 0x40013920
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778468

PERI_MS_PPU_FX197_SL_ADDR

Slave region, base address
Address: 0x40013940
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269124800

PERI_MS_PPU_FX197_MS_ADDR

Master region, base address
Address: 0x40013960
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778469

PERI_MS_PPU_FX198_SL_ADDR

Slave region, base address
Address: 0x40013980
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269156352

PERI_MS_PPU_FX198_MS_ADDR

Master region, base address
Address: 0x400139A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778470

PERI_MS_PPU_FX199_SL_ADDR

Slave region, base address
Address: 0x400139C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269156864

PERI_MS_PPU_FX199_MS_ADDR

Master region, base address
Address: 0x400139E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778471

PERI_MS_PPU_FX200_SL_ADDR

Slave region, base address
Address: 0x40013A00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269205504

PERI_MS_PPU_FX200_MS_ADDR

Master region, base address
Address: 0x40013A20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778472

PERI_MS_PPU_FX201_SL_ADDR

Slave region, base address
Address: 0x40013A40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221888

PERI_MS_PPU_FX201_MS_ADDR

Master region, base address
Address: 0x40013A60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778473

PERI_MS_PPU_FX202_SL_ADDR

Slave region, base address
Address: 0x40013A80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221892

PERI_MS_PPU_FX202_MS_ADDR

Master region, base address
Address: 0x40013AA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778474

PERI_MS_PPU_FX203_SL_ADDR

Slave region, base address
Address: 0x40013AC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221896

PERI_MS_PPU_FX203_MS_ADDR

Master region, base address
Address: 0x40013AE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778475

PERI_MS_PPU_FX204_SL_ADDR

Slave region, base address
Address: 0x40013B00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221900

PERI_MS_PPU_FX204_MS_ADDR

Master region, base address
Address: 0x40013B20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778476

PERI_MS_PPU_FX205_SL_ADDR

Slave region, base address
Address: 0x40013B40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221904

PERI_MS_PPU_FX205_MS_ADDR

Master region, base address
Address: 0x40013B60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778477

PERI_MS_PPU_FX206_SL_ADDR

Slave region, base address
Address: 0x40013B80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221908

PERI_MS_PPU_FX206_MS_ADDR

Master region, base address
Address: 0x40013BA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778478

PERI_MS_PPU_FX207_SL_ADDR

Slave region, base address
Address: 0x40013BC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221912

PERI_MS_PPU_FX207_MS_ADDR

Master region, base address
Address: 0x40013BE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778479

PERI_MS_PPU_FX208_SL_ADDR

Slave region, base address
Address: 0x40013C00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221916

PERI_MS_PPU_FX208_MS_ADDR

Master region, base address
Address: 0x40013C20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778480

PERI_MS_PPU_FX209_SL_ADDR

Slave region, base address
Address: 0x40013C40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221920

PERI_MS_PPU_FX209_MS_ADDR

Master region, base address
Address: 0x40013C60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778481

PERI_MS_PPU_FX210_SL_ADDR

Slave region, base address
Address: 0x40013C80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221924

PERI_MS_PPU_FX210_MS_ADDR

Master region, base address
Address: 0x40013CA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778482

PERI_MS_PPU_FX211_SL_ADDR

Slave region, base address
Address: 0x40013CC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221928

PERI_MS_PPU_FX211_MS_ADDR

Master region, base address
Address: 0x40013CE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778483

PERI_MS_PPU_FX212_SL_ADDR

Slave region, base address
Address: 0x40013D00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221932

PERI_MS_PPU_FX212_MS_ADDR

Master region, base address
Address: 0x40013D20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778484

PERI_MS_PPU_FX213_SL_ADDR

Slave region, base address
Address: 0x40013D40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221936

PERI_MS_PPU_FX213_MS_ADDR

Master region, base address
Address: 0x40013D60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778485

PERI_MS_PPU_FX214_SL_ADDR

Slave region, base address
Address: 0x40013D80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221940

PERI_MS_PPU_FX214_MS_ADDR

Master region, base address
Address: 0x40013DA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778486

PERI_MS_PPU_FX215_SL_ADDR

Slave region, base address
Address: 0x40013DC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221944

PERI_MS_PPU_FX215_MS_ADDR

Master region, base address
Address: 0x40013DE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778487

PERI_MS_PPU_FX216_SL_ADDR

Slave region, base address
Address: 0x40013E00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221948

PERI_MS_PPU_FX216_MS_ADDR

Master region, base address
Address: 0x40013E20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778488

PERI_MS_PPU_FX217_SL_ADDR

Slave region, base address
Address: 0x40013E40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221952

PERI_MS_PPU_FX217_MS_ADDR

Master region, base address
Address: 0x40013E60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778489

PERI_MS_PPU_FX218_SL_ADDR

Slave region, base address
Address: 0x40013E80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221956

PERI_MS_PPU_FX218_MS_ADDR

Master region, base address
Address: 0x40013EA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778490

PERI_MS_PPU_FX219_SL_ADDR

Slave region, base address
Address: 0x40013EC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221960

PERI_MS_PPU_FX219_MS_ADDR

Master region, base address
Address: 0x40013EE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778491

PERI_MS_PPU_FX220_SL_ADDR

Slave region, base address
Address: 0x40013F00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221964

PERI_MS_PPU_FX220_MS_ADDR

Master region, base address
Address: 0x40013F20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778492

PERI_MS_PPU_FX221_SL_ADDR

Slave region, base address
Address: 0x40013F40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221968

PERI_MS_PPU_FX221_MS_ADDR

Master region, base address
Address: 0x40013F60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778493

PERI_MS_PPU_FX222_SL_ADDR

Slave region, base address
Address: 0x40013F80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221972

PERI_MS_PPU_FX222_MS_ADDR

Master region, base address
Address: 0x40013FA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778494

PERI_MS_PPU_FX223_SL_ADDR

Slave region, base address
Address: 0x40013FC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221976

PERI_MS_PPU_FX223_MS_ADDR

Master region, base address
Address: 0x40013FE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778495

PERI_MS_PPU_FX224_SL_ADDR

Slave region, base address
Address: 0x40014000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221980

PERI_MS_PPU_FX224_MS_ADDR

Master region, base address
Address: 0x40014020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778496

PERI_MS_PPU_FX225_SL_ADDR

Slave region, base address
Address: 0x40014040
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269223936

PERI_MS_PPU_FX225_MS_ADDR

Master region, base address
Address: 0x40014060
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778497

PERI_MS_PPU_FX226_SL_ADDR

Slave region, base address
Address: 0x40014080
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269224064

PERI_MS_PPU_FX226_MS_ADDR

Master region, base address
Address: 0x400140A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778498

PERI_MS_PPU_FX227_SL_ADDR

Slave region, base address
Address: 0x400140C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269224080

PERI_MS_PPU_FX227_MS_ADDR

Master region, base address
Address: 0x400140E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778499

PERI_MS_PPU_FX228_SL_ADDR

Slave region, base address
Address: 0x40014100
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238272

PERI_MS_PPU_FX228_MS_ADDR

Master region, base address
Address: 0x40014120
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778500

PERI_MS_PPU_FX229_SL_ADDR

Slave region, base address
Address: 0x40014140
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238304

PERI_MS_PPU_FX229_MS_ADDR

Master region, base address
Address: 0x40014160
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778501

PERI_MS_PPU_FX230_SL_ADDR

Slave region, base address
Address: 0x40014180
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238336

PERI_MS_PPU_FX230_MS_ADDR

Master region, base address
Address: 0x400141A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778502

PERI_MS_PPU_FX231_SL_ADDR

Slave region, base address
Address: 0x400141C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238368

PERI_MS_PPU_FX231_MS_ADDR

Master region, base address
Address: 0x400141E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778503

PERI_MS_PPU_FX232_SL_ADDR

Slave region, base address
Address: 0x40014200
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238400

PERI_MS_PPU_FX232_MS_ADDR

Master region, base address
Address: 0x40014220
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778504

PERI_MS_PPU_FX233_SL_ADDR

Slave region, base address
Address: 0x40014240
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238432

PERI_MS_PPU_FX233_MS_ADDR

Master region, base address
Address: 0x40014260
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778505

PERI_MS_PPU_FX234_SL_ADDR

Slave region, base address
Address: 0x40014280
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238464

PERI_MS_PPU_FX234_MS_ADDR

Master region, base address
Address: 0x400142A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778506

PERI_MS_PPU_FX235_SL_ADDR

Slave region, base address
Address: 0x400142C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238496

PERI_MS_PPU_FX235_MS_ADDR

Master region, base address
Address: 0x400142E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778507

PERI_MS_PPU_FX236_SL_ADDR

Slave region, base address
Address: 0x40014300
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238528

PERI_MS_PPU_FX236_MS_ADDR

Master region, base address
Address: 0x40014320
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778508

PERI_MS_PPU_FX237_SL_ADDR

Slave region, base address
Address: 0x40014340
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238560

PERI_MS_PPU_FX237_MS_ADDR

Master region, base address
Address: 0x40014360
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778509

PERI_MS_PPU_FX238_SL_ADDR

Slave region, base address
Address: 0x40014380
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238592

PERI_MS_PPU_FX238_MS_ADDR

Master region, base address
Address: 0x400143A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778510

PERI_MS_PPU_FX239_SL_ADDR

Slave region, base address
Address: 0x400143C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238624

PERI_MS_PPU_FX239_MS_ADDR

Master region, base address
Address: 0x400143E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778511

PERI_MS_PPU_FX240_SL_ADDR

Slave region, base address
Address: 0x40014400
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238656

PERI_MS_PPU_FX240_MS_ADDR

Master region, base address
Address: 0x40014420
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778512

PERI_MS_PPU_FX241_SL_ADDR

Slave region, base address
Address: 0x40014440
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238688

PERI_MS_PPU_FX241_MS_ADDR

Master region, base address
Address: 0x40014460
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778513

PERI_MS_PPU_FX242_SL_ADDR

Slave region, base address
Address: 0x40014480
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238720

PERI_MS_PPU_FX242_MS_ADDR

Master region, base address
Address: 0x400144A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778514

PERI_MS_PPU_FX243_SL_ADDR

Slave region, base address
Address: 0x400144C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238752

PERI_MS_PPU_FX243_MS_ADDR

Master region, base address
Address: 0x400144E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778515

PERI_MS_PPU_FX244_SL_ADDR

Slave region, base address
Address: 0x40014500
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238784

PERI_MS_PPU_FX244_MS_ADDR

Master region, base address
Address: 0x40014520
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778516

PERI_MS_PPU_FX245_SL_ADDR

Slave region, base address
Address: 0x40014540
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238816

PERI_MS_PPU_FX245_MS_ADDR

Master region, base address
Address: 0x40014560
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778517

PERI_MS_PPU_FX246_SL_ADDR

Slave region, base address
Address: 0x40014580
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238848

PERI_MS_PPU_FX246_MS_ADDR

Master region, base address
Address: 0x400145A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778518

PERI_MS_PPU_FX247_SL_ADDR

Slave region, base address
Address: 0x400145C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238880

PERI_MS_PPU_FX247_MS_ADDR

Master region, base address
Address: 0x400145E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778519

PERI_MS_PPU_FX248_SL_ADDR

Slave region, base address
Address: 0x40014600
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238912

PERI_MS_PPU_FX248_MS_ADDR

Master region, base address
Address: 0x40014620
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778520

PERI_MS_PPU_FX249_SL_ADDR

Slave region, base address
Address: 0x40014640
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238944

PERI_MS_PPU_FX249_MS_ADDR

Master region, base address
Address: 0x40014660
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778521

PERI_MS_PPU_FX250_SL_ADDR

Slave region, base address
Address: 0x40014680
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238976

PERI_MS_PPU_FX250_MS_ADDR

Master region, base address
Address: 0x400146A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778522

PERI_MS_PPU_FX251_SL_ADDR

Slave region, base address
Address: 0x400146C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269239008

PERI_MS_PPU_FX251_MS_ADDR

Master region, base address
Address: 0x400146E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778523

PERI_MS_PPU_FX252_SL_ADDR

Slave region, base address
Address: 0x40014700
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238288

PERI_MS_PPU_FX252_MS_ADDR

Master region, base address
Address: 0x40014720
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778524

PERI_MS_PPU_FX253_SL_ADDR

Slave region, base address
Address: 0x40014740
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238320

PERI_MS_PPU_FX253_MS_ADDR

Master region, base address
Address: 0x40014760
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778525

PERI_MS_PPU_FX254_SL_ADDR

Slave region, base address
Address: 0x40014780
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238352

PERI_MS_PPU_FX254_MS_ADDR

Master region, base address
Address: 0x400147A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778526

PERI_MS_PPU_FX255_SL_ADDR

Slave region, base address
Address: 0x400147C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238384

PERI_MS_PPU_FX255_MS_ADDR

Master region, base address
Address: 0x400147E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778527

PERI_MS_PPU_FX256_SL_ADDR

Slave region, base address
Address: 0x40014800
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238416

PERI_MS_PPU_FX256_MS_ADDR

Master region, base address
Address: 0x40014820
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778528

PERI_MS_PPU_FX257_SL_ADDR

Slave region, base address
Address: 0x40014840
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238448

PERI_MS_PPU_FX257_MS_ADDR

Master region, base address
Address: 0x40014860
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778529

PERI_MS_PPU_FX258_SL_ADDR

Slave region, base address
Address: 0x40014880
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238480

PERI_MS_PPU_FX258_MS_ADDR

Master region, base address
Address: 0x400148A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778530

PERI_MS_PPU_FX259_SL_ADDR

Slave region, base address
Address: 0x400148C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238512

PERI_MS_PPU_FX259_MS_ADDR

Master region, base address
Address: 0x400148E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778531

PERI_MS_PPU_FX260_SL_ADDR

Slave region, base address
Address: 0x40014900
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238544

PERI_MS_PPU_FX260_MS_ADDR

Master region, base address
Address: 0x40014920
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778532

PERI_MS_PPU_FX261_SL_ADDR

Slave region, base address
Address: 0x40014940
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238576

PERI_MS_PPU_FX261_MS_ADDR

Master region, base address
Address: 0x40014960
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778533

PERI_MS_PPU_FX262_SL_ADDR

Slave region, base address
Address: 0x40014980
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238608

PERI_MS_PPU_FX262_MS_ADDR

Master region, base address
Address: 0x400149A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778534

PERI_MS_PPU_FX263_SL_ADDR

Slave region, base address
Address: 0x400149C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238640

PERI_MS_PPU_FX263_MS_ADDR

Master region, base address
Address: 0x400149E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778535

PERI_MS_PPU_FX264_SL_ADDR

Slave region, base address
Address: 0x40014A00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238672

PERI_MS_PPU_FX264_MS_ADDR

Master region, base address
Address: 0x40014A20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778536

PERI_MS_PPU_FX265_SL_ADDR

Slave region, base address
Address: 0x40014A40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238704

PERI_MS_PPU_FX265_MS_ADDR

Master region, base address
Address: 0x40014A60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778537

PERI_MS_PPU_FX266_SL_ADDR

Slave region, base address
Address: 0x40014A80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238736

PERI_MS_PPU_FX266_MS_ADDR

Master region, base address
Address: 0x40014AA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778538

PERI_MS_PPU_FX267_SL_ADDR

Slave region, base address
Address: 0x40014AC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238768

PERI_MS_PPU_FX267_MS_ADDR

Master region, base address
Address: 0x40014AE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778539

PERI_MS_PPU_FX268_SL_ADDR

Slave region, base address
Address: 0x40014B00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238800

PERI_MS_PPU_FX268_MS_ADDR

Master region, base address
Address: 0x40014B20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778540

PERI_MS_PPU_FX269_SL_ADDR

Slave region, base address
Address: 0x40014B40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238832

PERI_MS_PPU_FX269_MS_ADDR

Master region, base address
Address: 0x40014B60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778541

PERI_MS_PPU_FX270_SL_ADDR

Slave region, base address
Address: 0x40014B80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238864

PERI_MS_PPU_FX270_MS_ADDR

Master region, base address
Address: 0x40014BA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778542

PERI_MS_PPU_FX271_SL_ADDR

Slave region, base address
Address: 0x40014BC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238896

PERI_MS_PPU_FX271_MS_ADDR

Master region, base address
Address: 0x40014BE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778543

PERI_MS_PPU_FX272_SL_ADDR

Slave region, base address
Address: 0x40014C00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238928

PERI_MS_PPU_FX272_MS_ADDR

Master region, base address
Address: 0x40014C20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778544

PERI_MS_PPU_FX273_SL_ADDR

Slave region, base address
Address: 0x40014C40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238960

PERI_MS_PPU_FX273_MS_ADDR

Master region, base address
Address: 0x40014C60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778545

PERI_MS_PPU_FX274_SL_ADDR

Slave region, base address
Address: 0x40014C80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238992

PERI_MS_PPU_FX274_MS_ADDR

Master region, base address
Address: 0x40014CA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778546

PERI_MS_PPU_FX275_SL_ADDR

Slave region, base address
Address: 0x40014CC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269239024

PERI_MS_PPU_FX275_MS_ADDR

Master region, base address
Address: 0x40014CE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778547

PERI_MS_PPU_FX276_SL_ADDR

Slave region, base address
Address: 0x40014D00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269242368

PERI_MS_PPU_FX276_MS_ADDR

Master region, base address
Address: 0x40014D20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778548

PERI_MS_PPU_FX277_SL_ADDR

Slave region, base address
Address: 0x40014D40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269243392

PERI_MS_PPU_FX277_MS_ADDR

Master region, base address
Address: 0x40014D60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778549

PERI_MS_PPU_FX278_SL_ADDR

Slave region, base address
Address: 0x40014D80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269255424

PERI_MS_PPU_FX278_MS_ADDR

Master region, base address
Address: 0x40014DA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778550

PERI_MS_PPU_FX279_SL_ADDR

Slave region, base address
Address: 0x40014DC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269255488

PERI_MS_PPU_FX279_MS_ADDR

Master region, base address
Address: 0x40014DE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778551

PERI_MS_PPU_FX280_SL_ADDR

Slave region, base address
Address: 0x40014E00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269255552

PERI_MS_PPU_FX280_MS_ADDR

Master region, base address
Address: 0x40014E20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778552

PERI_MS_PPU_FX281_SL_ADDR

Slave region, base address
Address: 0x40014E40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269255616

PERI_MS_PPU_FX281_MS_ADDR

Master region, base address
Address: 0x40014E60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778553

PERI_MS_PPU_FX282_SL_ADDR

Slave region, base address
Address: 0x40014E80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269255744

PERI_MS_PPU_FX282_MS_ADDR

Master region, base address
Address: 0x40014EA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778554

PERI_MS_PPU_FX283_SL_ADDR

Slave region, base address
Address: 0x40014EC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269352960

PERI_MS_PPU_FX283_MS_ADDR

Master region, base address
Address: 0x40014EE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778555

PERI_MS_PPU_FX284_SL_ADDR

Slave region, base address
Address: 0x40014F00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269352992

PERI_MS_PPU_FX284_MS_ADDR

Master region, base address
Address: 0x40014F20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778556

PERI_MS_PPU_FX285_SL_ADDR

Slave region, base address
Address: 0x40014F40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353024

PERI_MS_PPU_FX285_MS_ADDR

Master region, base address
Address: 0x40014F60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778557

PERI_MS_PPU_FX286_SL_ADDR

Slave region, base address
Address: 0x40014F80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353056

PERI_MS_PPU_FX286_MS_ADDR

Master region, base address
Address: 0x40014FA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778558

PERI_MS_PPU_FX287_SL_ADDR

Slave region, base address
Address: 0x40014FC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353088

PERI_MS_PPU_FX287_MS_ADDR

Master region, base address
Address: 0x40014FE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778559

PERI_MS_PPU_FX288_SL_ADDR

Slave region, base address
Address: 0x40015000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353120

PERI_MS_PPU_FX288_MS_ADDR

Master region, base address
Address: 0x40015020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778560

PERI_MS_PPU_FX289_SL_ADDR

Slave region, base address
Address: 0x40015040
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353152

PERI_MS_PPU_FX289_MS_ADDR

Master region, base address
Address: 0x40015060
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778561

PERI_MS_PPU_FX290_SL_ADDR

Slave region, base address
Address: 0x40015080
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353184

PERI_MS_PPU_FX290_MS_ADDR

Master region, base address
Address: 0x400150A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778562

PERI_MS_PPU_FX291_SL_ADDR

Slave region, base address
Address: 0x400150C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353216

PERI_MS_PPU_FX291_MS_ADDR

Master region, base address
Address: 0x400150E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778563

PERI_MS_PPU_FX292_SL_ADDR

Slave region, base address
Address: 0x40015100
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353248

PERI_MS_PPU_FX292_MS_ADDR

Master region, base address
Address: 0x40015120
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778564

PERI_MS_PPU_FX293_SL_ADDR

Slave region, base address
Address: 0x40015140
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353280

PERI_MS_PPU_FX293_MS_ADDR

Master region, base address
Address: 0x40015160
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778565

PERI_MS_PPU_FX294_SL_ADDR

Slave region, base address
Address: 0x40015180
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353312

PERI_MS_PPU_FX294_MS_ADDR

Master region, base address
Address: 0x400151A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778566

PERI_MS_PPU_FX295_SL_ADDR

Slave region, base address
Address: 0x400151C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353344

PERI_MS_PPU_FX295_MS_ADDR

Master region, base address
Address: 0x400151E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778567

PERI_MS_PPU_FX296_SL_ADDR

Slave region, base address
Address: 0x40015200
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353376

PERI_MS_PPU_FX296_MS_ADDR

Master region, base address
Address: 0x40015220
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778568

PERI_MS_PPU_FX297_SL_ADDR

Slave region, base address
Address: 0x40015240
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353408

PERI_MS_PPU_FX297_MS_ADDR

Master region, base address
Address: 0x40015260
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778569

PERI_MS_PPU_FX298_SL_ADDR

Slave region, base address
Address: 0x40015280
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353440

PERI_MS_PPU_FX298_MS_ADDR

Master region, base address
Address: 0x400152A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778570

PERI_MS_PPU_FX299_SL_ADDR

Slave region, base address
Address: 0x400152C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353472

PERI_MS_PPU_FX299_MS_ADDR

Master region, base address
Address: 0x400152E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778571

PERI_MS_PPU_FX300_SL_ADDR

Slave region, base address
Address: 0x40015300
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353504

PERI_MS_PPU_FX300_MS_ADDR

Master region, base address
Address: 0x40015320
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778572

PERI_MS_PPU_FX301_SL_ADDR

Slave region, base address
Address: 0x40015340
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353536

PERI_MS_PPU_FX301_MS_ADDR

Master region, base address
Address: 0x40015360
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778573

PERI_MS_PPU_FX302_SL_ADDR

Slave region, base address
Address: 0x40015380
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353568

PERI_MS_PPU_FX302_MS_ADDR

Master region, base address
Address: 0x400153A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778574

PERI_MS_PPU_FX303_SL_ADDR

Slave region, base address
Address: 0x400153C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353600

PERI_MS_PPU_FX303_MS_ADDR

Master region, base address
Address: 0x400153E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778575

PERI_MS_PPU_FX304_SL_ADDR

Slave region, base address
Address: 0x40015400
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353632

PERI_MS_PPU_FX304_MS_ADDR

Master region, base address
Address: 0x40015420
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778576

PERI_MS_PPU_FX305_SL_ADDR

Slave region, base address
Address: 0x40015440
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353664

PERI_MS_PPU_FX305_MS_ADDR

Master region, base address
Address: 0x40015460
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778577

PERI_MS_PPU_FX306_SL_ADDR

Slave region, base address
Address: 0x40015480
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353696

PERI_MS_PPU_FX306_MS_ADDR

Master region, base address
Address: 0x400154A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778578

PERI_MS_PPU_FX307_SL_ADDR

Slave region, base address
Address: 0x400154C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353728

PERI_MS_PPU_FX307_MS_ADDR

Master region, base address
Address: 0x400154E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778579

PERI_MS_PPU_FX308_SL_ADDR

Slave region, base address
Address: 0x40015500
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353760

PERI_MS_PPU_FX308_MS_ADDR

Master region, base address
Address: 0x40015520
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778580

PERI_MS_PPU_FX309_SL_ADDR

Slave region, base address
Address: 0x40015540
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353792

PERI_MS_PPU_FX309_MS_ADDR

Master region, base address
Address: 0x40015560
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778581

PERI_MS_PPU_FX310_SL_ADDR

Slave region, base address
Address: 0x40015580
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353824

PERI_MS_PPU_FX310_MS_ADDR

Master region, base address
Address: 0x400155A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778582

PERI_MS_PPU_FX311_SL_ADDR

Slave region, base address
Address: 0x400155C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353856

PERI_MS_PPU_FX311_MS_ADDR

Master region, base address
Address: 0x400155E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778583

PERI_MS_PPU_FX312_SL_ADDR

Slave region, base address
Address: 0x40015600
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353888

PERI_MS_PPU_FX312_MS_ADDR

Master region, base address
Address: 0x40015620
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778584

PERI_MS_PPU_FX313_SL_ADDR

Slave region, base address
Address: 0x40015640
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353920

PERI_MS_PPU_FX313_MS_ADDR

Master region, base address
Address: 0x40015660
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778585

PERI_MS_PPU_FX314_SL_ADDR

Slave region, base address
Address: 0x40015680
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353952

PERI_MS_PPU_FX314_MS_ADDR

Master region, base address
Address: 0x400156A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778586

PERI_MS_PPU_FX315_SL_ADDR

Slave region, base address
Address: 0x400156C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353984

PERI_MS_PPU_FX315_MS_ADDR

Master region, base address
Address: 0x400156E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778587

PERI_MS_PPU_FX316_SL_ADDR

Slave region, base address
Address: 0x40015700
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354016

PERI_MS_PPU_FX316_MS_ADDR

Master region, base address
Address: 0x40015720
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778588

PERI_MS_PPU_FX317_SL_ADDR

Slave region, base address
Address: 0x40015740
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354048

PERI_MS_PPU_FX317_MS_ADDR

Master region, base address
Address: 0x40015760
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778589

PERI_MS_PPU_FX318_SL_ADDR

Slave region, base address
Address: 0x40015780
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354080

PERI_MS_PPU_FX318_MS_ADDR

Master region, base address
Address: 0x400157A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778590

PERI_MS_PPU_FX319_SL_ADDR

Slave region, base address
Address: 0x400157C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354112

PERI_MS_PPU_FX319_MS_ADDR

Master region, base address
Address: 0x400157E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778591

PERI_MS_PPU_FX320_SL_ADDR

Slave region, base address
Address: 0x40015800
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354144

PERI_MS_PPU_FX320_MS_ADDR

Master region, base address
Address: 0x40015820
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778592

PERI_MS_PPU_FX321_SL_ADDR

Slave region, base address
Address: 0x40015840
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354176

PERI_MS_PPU_FX321_MS_ADDR

Master region, base address
Address: 0x40015860
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778593

PERI_MS_PPU_FX322_SL_ADDR

Slave region, base address
Address: 0x40015880
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354208

PERI_MS_PPU_FX322_MS_ADDR

Master region, base address
Address: 0x400158A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778594

PERI_MS_PPU_FX323_SL_ADDR

Slave region, base address
Address: 0x400158C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354240

PERI_MS_PPU_FX323_MS_ADDR

Master region, base address
Address: 0x400158E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778595

PERI_MS_PPU_FX324_SL_ADDR

Slave region, base address
Address: 0x40015900
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354272

PERI_MS_PPU_FX324_MS_ADDR

Master region, base address
Address: 0x40015920
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778596

PERI_MS_PPU_FX325_SL_ADDR

Slave region, base address
Address: 0x40015940
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354304

PERI_MS_PPU_FX325_MS_ADDR

Master region, base address
Address: 0x40015960
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778597

PERI_MS_PPU_FX326_SL_ADDR

Slave region, base address
Address: 0x40015980
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354336

PERI_MS_PPU_FX326_MS_ADDR

Master region, base address
Address: 0x400159A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778598

PERI_MS_PPU_FX327_SL_ADDR

Slave region, base address
Address: 0x400159C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354368

PERI_MS_PPU_FX327_MS_ADDR

Master region, base address
Address: 0x400159E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778599

PERI_MS_PPU_FX328_SL_ADDR

Slave region, base address
Address: 0x40015A00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354400

PERI_MS_PPU_FX328_MS_ADDR

Master region, base address
Address: 0x40015A20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778600

PERI_MS_PPU_FX329_SL_ADDR

Slave region, base address
Address: 0x40015A40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354432

PERI_MS_PPU_FX329_MS_ADDR

Master region, base address
Address: 0x40015A60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778601

PERI_MS_PPU_FX330_SL_ADDR

Slave region, base address
Address: 0x40015A80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354464

PERI_MS_PPU_FX330_MS_ADDR

Master region, base address
Address: 0x40015AA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778602

PERI_MS_PPU_FX331_SL_ADDR

Slave region, base address
Address: 0x40015AC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354496

PERI_MS_PPU_FX331_MS_ADDR

Master region, base address
Address: 0x40015AE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778603

PERI_MS_PPU_FX332_SL_ADDR

Slave region, base address
Address: 0x40015B00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354528

PERI_MS_PPU_FX332_MS_ADDR

Master region, base address
Address: 0x40015B20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778604

PERI_MS_PPU_FX333_SL_ADDR

Slave region, base address
Address: 0x40015B40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354560

PERI_MS_PPU_FX333_MS_ADDR

Master region, base address
Address: 0x40015B60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778605

PERI_MS_PPU_FX334_SL_ADDR

Slave region, base address
Address: 0x40015B80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354592

PERI_MS_PPU_FX334_MS_ADDR

Master region, base address
Address: 0x40015BA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778606

PERI_MS_PPU_FX335_SL_ADDR

Slave region, base address
Address: 0x40015BC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354624

PERI_MS_PPU_FX335_MS_ADDR

Master region, base address
Address: 0x40015BE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778607

PERI_MS_PPU_FX336_SL_ADDR

Slave region, base address
Address: 0x40015C00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354656

PERI_MS_PPU_FX336_MS_ADDR

Master region, base address
Address: 0x40015C20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778608

PERI_MS_PPU_FX337_SL_ADDR

Slave region, base address
Address: 0x40015C40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354688

PERI_MS_PPU_FX337_MS_ADDR

Master region, base address
Address: 0x40015C60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778609

PERI_MS_PPU_FX338_SL_ADDR

Slave region, base address
Address: 0x40015C80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354720

PERI_MS_PPU_FX338_MS_ADDR

Master region, base address
Address: 0x40015CA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778610

PERI_MS_PPU_FX339_SL_ADDR

Slave region, base address
Address: 0x40015CC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354752

PERI_MS_PPU_FX339_MS_ADDR

Master region, base address
Address: 0x40015CE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778611

PERI_MS_PPU_FX340_SL_ADDR

Slave region, base address
Address: 0x40015D00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354784

PERI_MS_PPU_FX340_MS_ADDR

Master region, base address
Address: 0x40015D20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778612

PERI_MS_PPU_FX341_SL_ADDR

Slave region, base address
Address: 0x40015D40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354816

PERI_MS_PPU_FX341_MS_ADDR

Master region, base address
Address: 0x40015D60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778613

PERI_MS_PPU_FX342_SL_ADDR

Slave region, base address
Address: 0x40015D80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354848

PERI_MS_PPU_FX342_MS_ADDR

Master region, base address
Address: 0x40015DA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778614

PERI_MS_PPU_FX343_SL_ADDR

Slave region, base address
Address: 0x40015DC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354880

PERI_MS_PPU_FX343_MS_ADDR

Master region, base address
Address: 0x40015DE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778615

PERI_MS_PPU_FX344_SL_ADDR

Slave region, base address
Address: 0x40015E00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354912

PERI_MS_PPU_FX344_MS_ADDR

Master region, base address
Address: 0x40015E20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778616

PERI_MS_PPU_FX345_SL_ADDR

Slave region, base address
Address: 0x40015E40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269354944

PERI_MS_PPU_FX345_MS_ADDR

Master region, base address
Address: 0x40015E60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778617

PERI_MS_PPU_FX346_SL_ADDR

Slave region, base address
Address: 0x40015E80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269361152

PERI_MS_PPU_FX346_MS_ADDR

Master region, base address
Address: 0x40015EA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778618

PERI_MS_PPU_FX347_SL_ADDR

Slave region, base address
Address: 0x40015EC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269361184

PERI_MS_PPU_FX347_MS_ADDR

Master region, base address
Address: 0x40015EE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778619

PERI_MS_PPU_FX348_SL_ADDR

Slave region, base address
Address: 0x40015F00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269361216

PERI_MS_PPU_FX348_MS_ADDR

Master region, base address
Address: 0x40015F20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778620

PERI_MS_PPU_FX349_SL_ADDR

Slave region, base address
Address: 0x40015F40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269361248

PERI_MS_PPU_FX349_MS_ADDR

Master region, base address
Address: 0x40015F60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778621

PERI_MS_PPU_FX350_SL_ADDR

Slave region, base address
Address: 0x40015F80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269361280

PERI_MS_PPU_FX350_MS_ADDR

Master region, base address
Address: 0x40015FA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778622

PERI_MS_PPU_FX351_SL_ADDR

Slave region, base address
Address: 0x40015FC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269361312

PERI_MS_PPU_FX351_MS_ADDR

Master region, base address
Address: 0x40015FE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778623

PERI_MS_PPU_FX352_SL_ADDR

Slave region, base address
Address: 0x40016000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269361344

PERI_MS_PPU_FX352_MS_ADDR

Master region, base address
Address: 0x40016020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778624

PERI_MS_PPU_FX353_SL_ADDR

Slave region, base address
Address: 0x40016040
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269361376

PERI_MS_PPU_FX353_MS_ADDR

Master region, base address
Address: 0x40016060
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778625

PERI_MS_PPU_FX354_SL_ADDR

Slave region, base address
Address: 0x40016080
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269361408

PERI_MS_PPU_FX354_MS_ADDR

Master region, base address
Address: 0x400160A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778626

PERI_MS_PPU_FX355_SL_ADDR

Slave region, base address
Address: 0x400160C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269361440

PERI_MS_PPU_FX355_MS_ADDR

Master region, base address
Address: 0x400160E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778627

PERI_MS_PPU_FX356_SL_ADDR

Slave region, base address
Address: 0x40016100
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269361472

PERI_MS_PPU_FX356_MS_ADDR

Master region, base address
Address: 0x40016120
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778628

PERI_MS_PPU_FX357_SL_ADDR

Slave region, base address
Address: 0x40016140
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269361504

PERI_MS_PPU_FX357_MS_ADDR

Master region, base address
Address: 0x40016160
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778629

PERI_MS_PPU_FX358_SL_ADDR

Slave region, base address
Address: 0x40016180
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269369344

PERI_MS_PPU_FX358_MS_ADDR

Master region, base address
Address: 0x400161A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778630

PERI_MS_PPU_FX359_SL_ADDR

Slave region, base address
Address: 0x400161C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269369376

PERI_MS_PPU_FX359_MS_ADDR

Master region, base address
Address: 0x400161E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778631

PERI_MS_PPU_FX360_SL_ADDR

Slave region, base address
Address: 0x40016200
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269369408

PERI_MS_PPU_FX360_MS_ADDR

Master region, base address
Address: 0x40016220
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778632

PERI_MS_PPU_FX361_SL_ADDR

Slave region, base address
Address: 0x40016240
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269369440

PERI_MS_PPU_FX361_MS_ADDR

Master region, base address
Address: 0x40016260
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778633

PERI_MS_PPU_FX362_SL_ADDR

Slave region, base address
Address: 0x40016280
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269467648

PERI_MS_PPU_FX362_MS_ADDR

Master region, base address
Address: 0x400162A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778634

PERI_MS_PPU_FX363_SL_ADDR

Slave region, base address
Address: 0x400162C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269746176

PERI_MS_PPU_FX363_MS_ADDR

Master region, base address
Address: 0x400162E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778635

PERI_MS_PPU_FX364_SL_ADDR

Slave region, base address
Address: 0x40016300
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269754368

PERI_MS_PPU_FX364_MS_ADDR

Master region, base address
Address: 0x40016320
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778636

PERI_MS_PPU_FX365_SL_ADDR

Slave region, base address
Address: 0x40016340
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269754432

PERI_MS_PPU_FX365_MS_ADDR

Master region, base address
Address: 0x40016360
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778637

PERI_MS_PPU_FX366_SL_ADDR

Slave region, base address
Address: 0x40016380
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269754496

PERI_MS_PPU_FX366_MS_ADDR

Master region, base address
Address: 0x400163A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778638

PERI_MS_PPU_FX367_SL_ADDR

Slave region, base address
Address: 0x400163C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269754560

PERI_MS_PPU_FX367_MS_ADDR

Master region, base address
Address: 0x400163E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778639

PERI_MS_PPU_FX368_SL_ADDR

Slave region, base address
Address: 0x40016400
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269754624

PERI_MS_PPU_FX368_MS_ADDR

Master region, base address
Address: 0x40016420
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778640

PERI_MS_PPU_FX369_SL_ADDR

Slave region, base address
Address: 0x40016440
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269754688

PERI_MS_PPU_FX369_MS_ADDR

Master region, base address
Address: 0x40016460
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778641

PERI_MS_PPU_FX370_SL_ADDR

Slave region, base address
Address: 0x40016480
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269754752

PERI_MS_PPU_FX370_MS_ADDR

Master region, base address
Address: 0x400164A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778642

PERI_MS_PPU_FX371_SL_ADDR

Slave region, base address
Address: 0x400164C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269754816

PERI_MS_PPU_FX371_MS_ADDR

Master region, base address
Address: 0x400164E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778643

PERI_MS_PPU_FX372_SL_ADDR

Slave region, base address
Address: 0x40016500
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269778944

PERI_MS_PPU_FX372_MS_ADDR

Master region, base address
Address: 0x40016520
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778644

PERI_MS_PPU_FX373_SL_ADDR

Slave region, base address
Address: 0x40016540
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269779072

PERI_MS_PPU_FX373_MS_ADDR

Master region, base address
Address: 0x40016560
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778645

PERI_MS_PPU_FX374_SL_ADDR

Slave region, base address
Address: 0x40016580
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269779200

PERI_MS_PPU_FX374_MS_ADDR

Master region, base address
Address: 0x400165A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778646

PERI_MS_PPU_FX375_SL_ADDR

Slave region, base address
Address: 0x400165C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269811712

PERI_MS_PPU_FX375_MS_ADDR

Master region, base address
Address: 0x400165E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778647

PERI_MS_PPU_FX376_SL_ADDR

Slave region, base address
Address: 0x40016600
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269811840

PERI_MS_PPU_FX376_MS_ADDR

Master region, base address
Address: 0x40016620
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778648

PERI_MS_PPU_FX377_SL_ADDR

Slave region, base address
Address: 0x40016640
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269811968

PERI_MS_PPU_FX377_MS_ADDR

Master region, base address
Address: 0x40016660
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778649

PERI_MS_PPU_FX378_SL_ADDR

Slave region, base address
Address: 0x40016680
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269779968

PERI_MS_PPU_FX378_MS_ADDR

Master region, base address
Address: 0x400166A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778650

PERI_MS_PPU_FX379_SL_ADDR

Slave region, base address
Address: 0x400166C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269812736

PERI_MS_PPU_FX379_MS_ADDR

Master region, base address
Address: 0x400166E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778651

PERI_MS_PPU_FX380_SL_ADDR

Slave region, base address
Address: 0x40016700
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269795328

PERI_MS_PPU_FX380_MS_ADDR

Master region, base address
Address: 0x40016720
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778652

PERI_MS_PPU_FX381_SL_ADDR

Slave region, base address
Address: 0x40016740
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269828096

PERI_MS_PPU_FX381_MS_ADDR

Master region, base address
Address: 0x40016760
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778653

PERI_MS_PPU_FX382_SL_ADDR

Slave region, base address
Address: 0x40016780
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270008320

PERI_MS_PPU_FX382_MS_ADDR

Master region, base address
Address: 0x400167A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778654

PERI_MS_PPU_FX383_SL_ADDR

Slave region, base address
Address: 0x400167C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270024704

PERI_MS_PPU_FX383_MS_ADDR

Master region, base address
Address: 0x400167E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778655

PERI_MS_PPU_FX384_SL_ADDR

Slave region, base address
Address: 0x40016800
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270041088

PERI_MS_PPU_FX384_MS_ADDR

Master region, base address
Address: 0x40016820
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778656

PERI_MS_PPU_FX385_SL_ADDR

Slave region, base address
Address: 0x40016840
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270057472

PERI_MS_PPU_FX385_MS_ADDR

Master region, base address
Address: 0x40016860
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778657

PERI_MS_PPU_FX386_SL_ADDR

Slave region, base address
Address: 0x40016880
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270073856

PERI_MS_PPU_FX386_MS_ADDR

Master region, base address
Address: 0x400168A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778658

PERI_MS_PPU_FX387_SL_ADDR

Slave region, base address
Address: 0x400168C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270090240

PERI_MS_PPU_FX387_MS_ADDR

Master region, base address
Address: 0x400168E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778659

PERI_MS_PPU_FX388_SL_ADDR

Slave region, base address
Address: 0x40016900
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270106624

PERI_MS_PPU_FX388_MS_ADDR

Master region, base address
Address: 0x40016920
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778660

PERI_MS_PPU_FX389_SL_ADDR

Slave region, base address
Address: 0x40016940
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270123008

PERI_MS_PPU_FX389_MS_ADDR

Master region, base address
Address: 0x40016960
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778661

PERI_MS_PPU_FX390_SL_ADDR

Slave region, base address
Address: 0x40016980
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270794752

PERI_MS_PPU_FX390_MS_ADDR

Master region, base address
Address: 0x400169A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778662

PERI_MS_PPU_FX391_SL_ADDR

Slave region, base address
Address: 0x400169C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270795776

PERI_MS_PPU_FX391_MS_ADDR

Master region, base address
Address: 0x400169E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778663

PERI_MS_PPU_FX392_SL_ADDR

Slave region, base address
Address: 0x40016A00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796800

PERI_MS_PPU_FX392_MS_ADDR

Master region, base address
Address: 0x40016A20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778664

PERI_MS_PPU_FX393_SL_ADDR

Slave region, base address
Address: 0x40016A40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270795264

PERI_MS_PPU_FX393_MS_ADDR

Master region, base address
Address: 0x40016A60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778665

PERI_MS_PPU_FX394_SL_ADDR

Slave region, base address
Address: 0x40016A80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270795280

PERI_MS_PPU_FX394_MS_ADDR

Master region, base address
Address: 0x40016AA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778666

PERI_MS_PPU_FX395_SL_ADDR

Slave region, base address
Address: 0x40016AC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270795296

PERI_MS_PPU_FX395_MS_ADDR

Master region, base address
Address: 0x40016AE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778667

PERI_MS_PPU_FX396_SL_ADDR

Slave region, base address
Address: 0x40016B00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270795312

PERI_MS_PPU_FX396_MS_ADDR

Master region, base address
Address: 0x40016B20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778668

PERI_MS_PPU_FX397_SL_ADDR

Slave region, base address
Address: 0x40016B40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270795328

PERI_MS_PPU_FX397_MS_ADDR

Master region, base address
Address: 0x40016B60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778669

PERI_MS_PPU_FX398_SL_ADDR

Slave region, base address
Address: 0x40016B80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270795344

PERI_MS_PPU_FX398_MS_ADDR

Master region, base address
Address: 0x40016BA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778670

PERI_MS_PPU_FX399_SL_ADDR

Slave region, base address
Address: 0x40016BC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270795360

PERI_MS_PPU_FX399_MS_ADDR

Master region, base address
Address: 0x40016BE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778671

PERI_MS_PPU_FX400_SL_ADDR

Slave region, base address
Address: 0x40016C00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270795376

PERI_MS_PPU_FX400_MS_ADDR

Master region, base address
Address: 0x40016C20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778672

PERI_MS_PPU_FX401_SL_ADDR

Slave region, base address
Address: 0x40016C40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270795392

PERI_MS_PPU_FX401_MS_ADDR

Master region, base address
Address: 0x40016C60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778673

PERI_MS_PPU_FX402_SL_ADDR

Slave region, base address
Address: 0x40016C80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270795408

PERI_MS_PPU_FX402_MS_ADDR

Master region, base address
Address: 0x40016CA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778674

PERI_MS_PPU_FX403_SL_ADDR

Slave region, base address
Address: 0x40016CC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270795424

PERI_MS_PPU_FX403_MS_ADDR

Master region, base address
Address: 0x40016CE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778675

PERI_MS_PPU_FX404_SL_ADDR

Slave region, base address
Address: 0x40016D00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270795440

PERI_MS_PPU_FX404_MS_ADDR

Master region, base address
Address: 0x40016D20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778676

PERI_MS_PPU_FX405_SL_ADDR

Slave region, base address
Address: 0x40016D40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270795456

PERI_MS_PPU_FX405_MS_ADDR

Master region, base address
Address: 0x40016D60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778677

PERI_MS_PPU_FX406_SL_ADDR

Slave region, base address
Address: 0x40016D80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270795472

PERI_MS_PPU_FX406_MS_ADDR

Master region, base address
Address: 0x40016DA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778678

PERI_MS_PPU_FX407_SL_ADDR

Slave region, base address
Address: 0x40016DC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270795488

PERI_MS_PPU_FX407_MS_ADDR

Master region, base address
Address: 0x40016DE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778679

PERI_MS_PPU_FX408_SL_ADDR

Slave region, base address
Address: 0x40016E00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270795504

PERI_MS_PPU_FX408_MS_ADDR

Master region, base address
Address: 0x40016E20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778680

PERI_MS_PPU_FX409_SL_ADDR

Slave region, base address
Address: 0x40016E40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270795520

PERI_MS_PPU_FX409_MS_ADDR

Master region, base address
Address: 0x40016E60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778681

PERI_MS_PPU_FX410_SL_ADDR

Slave region, base address
Address: 0x40016E80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270795536

PERI_MS_PPU_FX410_MS_ADDR

Master region, base address
Address: 0x40016EA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778682

PERI_MS_PPU_FX411_SL_ADDR

Slave region, base address
Address: 0x40016EC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270795552

PERI_MS_PPU_FX411_MS_ADDR

Master region, base address
Address: 0x40016EE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778683

PERI_MS_PPU_FX412_SL_ADDR

Slave region, base address
Address: 0x40016F00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270795568

PERI_MS_PPU_FX412_MS_ADDR

Master region, base address
Address: 0x40016F20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778684

PERI_MS_PPU_FX413_SL_ADDR

Slave region, base address
Address: 0x40016F40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270795584

PERI_MS_PPU_FX413_MS_ADDR

Master region, base address
Address: 0x40016F60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778685

PERI_MS_PPU_FX414_SL_ADDR

Slave region, base address
Address: 0x40016F80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270795600

PERI_MS_PPU_FX414_MS_ADDR

Master region, base address
Address: 0x40016FA0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778686

PERI_MS_PPU_FX415_SL_ADDR

Slave region, base address
Address: 0x40016FC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270795616

PERI_MS_PPU_FX415_MS_ADDR

Master region, base address
Address: 0x40016FE0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778687

PERI_MS_PPU_FX416_SL_ADDR

Slave region, base address
Address: 0x40017000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270795632

PERI_MS_PPU_FX416_MS_ADDR

Master region, base address
Address: 0x40017020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778688

PERI_MS_PPU_FX417_SL_ADDR

Slave region, base address
Address: 0x40017040
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796288

PERI_MS_PPU_FX417_MS_ADDR

Master region, base address
Address: 0x40017060
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778689

PERI_MS_PPU_FX418_SL_ADDR

Slave region, base address
Address: 0x40017080
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796304

PERI_MS_PPU_FX418_MS_ADDR

Master region, base address
Address: 0x400170A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778690

PERI_MS_PPU_FX419_SL_ADDR

Slave region, base address
Address: 0x400170C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796320

PERI_MS_PPU_FX419_MS_ADDR

Master region, base address
Address: 0x400170E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778691

PERI_MS_PPU_FX420_SL_ADDR

Slave region, base address
Address: 0x40017100
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796336

PERI_MS_PPU_FX420_MS_ADDR

Master region, base address
Address: 0x40017120
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778692

PERI_MS_PPU_FX421_SL_ADDR

Slave region, base address
Address: 0x40017140
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796352

PERI_MS_PPU_FX421_MS_ADDR

Master region, base address
Address: 0x40017160
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778693

PERI_MS_PPU_FX422_SL_ADDR

Slave region, base address
Address: 0x40017180
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796368

PERI_MS_PPU_FX422_MS_ADDR

Master region, base address
Address: 0x400171A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778694

PERI_MS_PPU_FX423_SL_ADDR

Slave region, base address
Address: 0x400171C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796384

PERI_MS_PPU_FX423_MS_ADDR

Master region, base address
Address: 0x400171E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778695

PERI_MS_PPU_FX424_SL_ADDR

Slave region, base address
Address: 0x40017200
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796400

PERI_MS_PPU_FX424_MS_ADDR

Master region, base address
Address: 0x40017220
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778696

PERI_MS_PPU_FX425_SL_ADDR

Slave region, base address
Address: 0x40017240
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796416

PERI_MS_PPU_FX425_MS_ADDR

Master region, base address
Address: 0x40017260
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778697

PERI_MS_PPU_FX426_SL_ADDR

Slave region, base address
Address: 0x40017280
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796432

PERI_MS_PPU_FX426_MS_ADDR

Master region, base address
Address: 0x400172A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778698

PERI_MS_PPU_FX427_SL_ADDR

Slave region, base address
Address: 0x400172C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796448

PERI_MS_PPU_FX427_MS_ADDR

Master region, base address
Address: 0x400172E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778699

PERI_MS_PPU_FX428_SL_ADDR

Slave region, base address
Address: 0x40017300
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796464

PERI_MS_PPU_FX428_MS_ADDR

Master region, base address
Address: 0x40017320
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778700

PERI_MS_PPU_FX429_SL_ADDR

Slave region, base address
Address: 0x40017340
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796480

PERI_MS_PPU_FX429_MS_ADDR

Master region, base address
Address: 0x40017360
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778701

PERI_MS_PPU_FX430_SL_ADDR

Slave region, base address
Address: 0x40017380
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796496

PERI_MS_PPU_FX430_MS_ADDR

Master region, base address
Address: 0x400173A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778702

PERI_MS_PPU_FX431_SL_ADDR

Slave region, base address
Address: 0x400173C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796512

PERI_MS_PPU_FX431_MS_ADDR

Master region, base address
Address: 0x400173E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778703

PERI_MS_PPU_FX432_SL_ADDR

Slave region, base address
Address: 0x40017400
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796528

PERI_MS_PPU_FX432_MS_ADDR

Master region, base address
Address: 0x40017420
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778704

PERI_MS_PPU_FX433_SL_ADDR

Slave region, base address
Address: 0x40017440
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796544

PERI_MS_PPU_FX433_MS_ADDR

Master region, base address
Address: 0x40017460
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778705

PERI_MS_PPU_FX434_SL_ADDR

Slave region, base address
Address: 0x40017480
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796560

PERI_MS_PPU_FX434_MS_ADDR

Master region, base address
Address: 0x400174A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778706

PERI_MS_PPU_FX435_SL_ADDR

Slave region, base address
Address: 0x400174C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796576

PERI_MS_PPU_FX435_MS_ADDR

Master region, base address
Address: 0x400174E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778707

PERI_MS_PPU_FX436_SL_ADDR

Slave region, base address
Address: 0x40017500
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796592

PERI_MS_PPU_FX436_MS_ADDR

Master region, base address
Address: 0x40017520
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778708

PERI_MS_PPU_FX437_SL_ADDR

Slave region, base address
Address: 0x40017540
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796608

PERI_MS_PPU_FX437_MS_ADDR

Master region, base address
Address: 0x40017560
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778709

PERI_MS_PPU_FX438_SL_ADDR

Slave region, base address
Address: 0x40017580
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796624

PERI_MS_PPU_FX438_MS_ADDR

Master region, base address
Address: 0x400175A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778710

PERI_MS_PPU_FX439_SL_ADDR

Slave region, base address
Address: 0x400175C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796640

PERI_MS_PPU_FX439_MS_ADDR

Master region, base address
Address: 0x400175E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778711

PERI_MS_PPU_FX440_SL_ADDR

Slave region, base address
Address: 0x40017600
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796656

PERI_MS_PPU_FX440_MS_ADDR

Master region, base address
Address: 0x40017620
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778712

PERI_MS_PPU_FX441_SL_ADDR

Slave region, base address
Address: 0x40017640
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796672

PERI_MS_PPU_FX441_MS_ADDR

Master region, base address
Address: 0x40017660
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778713

PERI_MS_PPU_FX442_SL_ADDR

Slave region, base address
Address: 0x40017680
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796688

PERI_MS_PPU_FX442_MS_ADDR

Master region, base address
Address: 0x400176A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778714

PERI_MS_PPU_FX443_SL_ADDR

Slave region, base address
Address: 0x400176C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796704

PERI_MS_PPU_FX443_MS_ADDR

Master region, base address
Address: 0x400176E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778715

PERI_MS_PPU_FX444_SL_ADDR

Slave region, base address
Address: 0x40017700
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796720

PERI_MS_PPU_FX444_MS_ADDR

Master region, base address
Address: 0x40017720
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778716

PERI_MS_PPU_FX445_SL_ADDR

Slave region, base address
Address: 0x40017740
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796736

PERI_MS_PPU_FX445_MS_ADDR

Master region, base address
Address: 0x40017760
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778717

PERI_MS_PPU_FX446_SL_ADDR

Slave region, base address
Address: 0x40017780
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796752

PERI_MS_PPU_FX446_MS_ADDR

Master region, base address
Address: 0x400177A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778718

PERI_MS_PPU_FX447_SL_ADDR

Slave region, base address
Address: 0x400177C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796768

PERI_MS_PPU_FX447_MS_ADDR

Master region, base address
Address: 0x400177E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778719

PERI_MS_PPU_FX448_SL_ADDR

Slave region, base address
Address: 0x40017800
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270796784

PERI_MS_PPU_FX448_MS_ADDR

Master region, base address
Address: 0x40017820
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778720

PERI_MS_PPU_FX449_SL_ADDR

Slave region, base address
Address: 0x40017840
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270797312

PERI_MS_PPU_FX449_MS_ADDR

Master region, base address
Address: 0x40017860
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778721

PERI_MS_PPU_FX450_SL_ADDR

Slave region, base address
Address: 0x40017880
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270797328

PERI_MS_PPU_FX450_MS_ADDR

Master region, base address
Address: 0x400178A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778722

PERI_MS_PPU_FX451_SL_ADDR

Slave region, base address
Address: 0x400178C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270797344

PERI_MS_PPU_FX451_MS_ADDR

Master region, base address
Address: 0x400178E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778723

PERI_MS_PPU_FX452_SL_ADDR

Slave region, base address
Address: 0x40017900
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270797360

PERI_MS_PPU_FX452_MS_ADDR

Master region, base address
Address: 0x40017920
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778724

PERI_MS_PPU_FX453_SL_ADDR

Slave region, base address
Address: 0x40017940
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270797376

PERI_MS_PPU_FX453_MS_ADDR

Master region, base address
Address: 0x40017960
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778725

PERI_MS_PPU_FX454_SL_ADDR

Slave region, base address
Address: 0x40017980
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270797392

PERI_MS_PPU_FX454_MS_ADDR

Master region, base address
Address: 0x400179A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778726

PERI_MS_PPU_FX455_SL_ADDR

Slave region, base address
Address: 0x400179C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270797408

PERI_MS_PPU_FX455_MS_ADDR

Master region, base address
Address: 0x400179E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778727

PERI_MS_PPU_FX456_SL_ADDR

Slave region, base address
Address: 0x40017A00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270797424

PERI_MS_PPU_FX456_MS_ADDR

Master region, base address
Address: 0x40017A20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778728

PERI_MS_PPU_FX457_SL_ADDR

Slave region, base address
Address: 0x40017A40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 271040512

PERI_MS_PPU_FX457_MS_ADDR

Master region, base address
Address: 0x40017A60
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778729

10 BACKUP

Register details

Register name	Address	Description
BACKUP_CTL	0x40270000	Control
BACKUP_RTC_RW	0x40270008	RTC Read Write register
BACKUP_CAL_CTL	0x4027000C	Oscillator calibration for absolute frequency
BACKUP_STATUS	0x40270010	Status
BACKUP_RTC_TIME	0x40270014	Calendar Seconds, Minutes, Hours, Day of Week
BACKUP_RTC_DATE	0x40270018	Calendar Day of Month, Month, Year
BACKUP_ALM1_TIME	0x4027001C	Alarm 1 Seconds, Minute, Hours, Day of Week
BACKUP_ALM1_DATE	0x40270020	Alarm 1 Day of Month, Month
BACKUP_ALM2_TIME	0x40270024	Alarm 2 Seconds, Minute, Hours, Day of Week
BACKUP_ALM2_DATE	0x40270028	Alarm 2 Day of Month, Month
BACKUP_INTR	0x4027002C	Interrupt request register
BACKUP_INTR_SET	0x40270030	Interrupt set request register
BACKUP_INTR_MASK	0x40270034	Interrupt mask register
BACKUP_INTR_MASKED	0x40270038	Interrupt masked request register
BACKUP_RESET	0x40270048	Backup reset register
BACKUP_BREG0	0x40271000	Backup register region
BACKUP_BREG1	0x40271004	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG2	0x40271008	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG3	0x4027100C	Backup register region. See BACKUP_BREG0 for the details of bit fields.

10.1 BACKUP registers

BACKUP_CTL

Control
Address: 0x40270000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	None		
HW Access	None				A	None		
Name	None [7:4]				WCO_EN	None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None		RW	
HW Access	None		A		None		A	

Bits	15	14	13	12	11	10	9	8
Name	None [15:14]		PRESCALER [13:12]		None [11:10]		CLK_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							A
Name	None [23:17]							WCO_BYPASS

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	WCO_BYPASS	Configures the WCO for different board-level connections to the WCO pins. For example, this can be used to connect an external watch crystal oscillator instead of a watch crystal. In all cases, the two related GPIO pins (WCO input and output pins) must be configured as analog connections using GPIO registers, and they must be hooked at the board level as described below. Configure this field before enabling the WCO, and do not change this setting when WCO_EN=1. 0: Watch crystal. Connect a 32.768 kHz watch crystal between WCO input and output pins. 1: Clock signal, either a square wave or sine wave. See PRESCALER field for connection information. Default Value: 0.
13 : 12	PRESCALER	Prescaler for real time clock used when WCO_BYPASS=1 and CLK_SEL = WCO. Configure this field before enabling the WCO, and do not change this setting when WCO_EN=1. 0: 32768 Hz square wave. Connect a 32768 Hz square wave to WCO output pin. Do not connect WCO input pin. 1: reserved 2: reserved 3: reserved Default Value: 0
9 : 8	CLK_SEL	Clock select for RTC clock Default Value: 0
		0x0: WCO : Watch-crystal oscillator input, available in Active, DeepSleep and Hibernate

		0x1: ALTBAK : This allows to use the LFCLK selection as an alternate backup domain clock. Note that LFCLK is only available in Active and DeepSleep power modes. Note that LFCLK clock glitches can propagate into the backup logic when the clock is stopped. For this reason, if the WCO or ILO is intended as the clock source then choose it directly instead of routing through LFCLK.
		0x2: ILO : Internal Low frequency Oscillator, available in Active, DeepSleep and Hibernate. For Hibernate operation CLK_ILO_CONFIG. ILO_BACKUP must be set.
		0x3: RESERVED : Reserved
3	WCO_EN	Watch-crystal oscillator (WCO) enable. If there is a write in progress when this bit is cleared, the WCO will be internally kept on until the write completes. After enabling the WCO software must wait until STATUS.WCO_OK=1 before configuring any component that depends on clk_lf/clk_bak, like for example RTC or WDTs. Follow the procedure in BACKUP_RTC_RW to access this bit. Default Value: 0

BACKUP_RTC_RW

RTC Read Write register
Address: 0x40270008
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						A	A
Name	None [7:2]						WRITE	READ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	WRITE	Write bit Only when this bit is set can the RTC registers be written to (otherwise writes are ignored). This bit cannot be set if the RTC is still busy with a previous update (see RTC_BUSY bit) or if the Read bit is set or getting set. The user writes to the RTC user registers, when the Write bit is cleared by the user then the user registers content is copied to the actual RTC registers. Only user RTC registers that were written to will get copied, others will not be affected. When the SECONDS field is updated then TICKS will also be reset (WDT is not affected). When the Write bit is cleared by a reset (brown out/DeepSleep) then the RTC update will be ignored/lost. Do not set the Write bit if the RTC if the RTC is still busy with a previous update (see RTC_BUSY). Do not set the Write bit at the same time that the Read bit is cleared. Default Value: 0

0	READ	Read bit When this bit is set the RTC registers will be copied to user registers and frozen so that a coherent RTC value can safely be read. The RTC will keep on running. Do not set the read bit if the RTC is still busy with a previous update (see RTC_BUSY bit) or if the Write bit is set. Do not set the Read bit at the same time that the Write bit is cleared. Default Value: 0

BACKUP_CAL_CTL

Oscillator calibration for absolute frequency
Address: 0x4027000C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW					
HW Access	None	A	A					
Name	None	CALIB_SIGN	CALIB_VAL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None	RW		None			
HW Access	A	None	A		None			
Name	CAL_OUT	None	CAL_SEL [29:28]		None [27:24]			

Bits	Name	Description
31	CAL_OUT	Output enable for wave signal for calibration and allow CALIB_VAL to be written. Default Value: 0
29 : 28	CAL_SEL	Select calibration wave output signal Default Value: 0
		0x0: CAL512 : 512Hz wave, not affected by calibration setting (not supported for 50/60Hz input clock: CTL.PRESCALER!=0)
		0x1: RESERVED : reserved
		0x2: CAL2 : 2Hz wave, includes the effect of the calibration setting, (not supported for 50/60Hz input clock: CTL.PRESCALER!=0)
		0x3: CAL1 : 1Hz wave, includes the effect of the calibration setting (supported for all input clocks)

6	CALIB_SIGN	Calibration sign: 0= Negative sign: remove pulses (it takes more clock ticks to count one second) 1= Positive sign: add pulses (it takes less clock ticks to count one second) Default Value: 0
5 : 0	CALIB_VAL	Calibration value for absolute frequency (at a fixed temperature). Each step causes 128 ticks to be added or removed each hour. Effectively that means that each step is 1.085ppm (= 128/ (60*60*32,768)). Positive values 0x01-0x3c (1..60) add pulses, negative values remove pulses, thus giving a range of +/-65.1 ppm (limited by 60 minutes per hour, not the range of this field) Calibration is performed hourly, starting at 59 minutes and 59 seconds, and applied as 64 ticks every 30 seconds until there have been 2*CALIB_VAL adjustments. Default Value: 0

BACKUP_STATUS

Status
Address: 0x40270010
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	None	R
HW Access	None					W	None	W
Name	None [7:3]					WCO_OK	None	RTC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	WCO_OK	Indicates that output has transitioned. Default Value: 0
0	RTC_BUSY	Pending RTC write Default Value: 0

BACKUP_RTC_TIME

Calendar Seconds, Minutes, Hours, Day of Week
Address: 0x40270014
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		A					
Name	None [7:6]		RTC_SEC [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		A					
Name	None [15:14]		RTC_MIN [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW	None	RW				
HW Access	None	A	None	A				
Name	None	CTRL_12HR	None	RTC_HOUR [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					A		
Name	None [31:27]					RTC_DAY [26:24]		

Bits	Name	Description
26 : 24	RTC_DAY	Calendar Day of the week, 1-7 It is up to the user to define the meaning of the values, but 1=Monday is recommended Default Value: 1
22	CTRL_12HR	Select 12/24HR mode: 1=12HR, 0=24HR Default Value: 0
20 : 16	RTC_HOUR	Calendar hours, value depending on 12/24HR mode 0=24HR: [20:16]=0-23 1=12HR: [20]:0=AM, 1=PM, [19:16]=1-12 Default Value: 0
13 : 8	RTC_MIN	Calendar minutes, 0-59 Default Value: 0
5 : 0	RTC_SEC	Calendar seconds, 0-59 Default Value: 0

BACKUP_RTC_DATE

Calendar Day of Month, Month, Year
Address: 0x40270018
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			A				
Name	None [7:5]			RTC_DATE [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				A			
Name	None [15:12]				RTC_MON [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	A						
Name	None	RTC_YEAR [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22 : 16	RTC_YEAR	Calendar year, 0-99 Default Value: 0
11 : 8	RTC_MON	Calendar Month, 1-12 Default Value: 1
4 : 0	RTC_DATE	Calendar Day of the Month, 1-31 Automatic Leap Year Correction Default Value: 1

BACKUP_ALM1_TIME

Alarm 1 Seconds, Minute, Hours, Day of Week
Address: 0x4027001C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None	RW					
HW Access	A	None	A					
Name	ALM_SEC_EN	None	ALM_SEC [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None	RW					
HW Access	A	None	A					
Name	ALM_MIN_EN	None	ALM_MIN [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None		RW				
HW Access	A	None		A				
Name	ALM_HOUR_EN	None [22:21]		ALM_HOUR [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None				RW		
HW Access	A	None				A		
Name	ALM_DAY_EN	None [30:27]				ALM_DAY [26:24]		

Bits	Name	Description
31	ALM_DAY_EN	Alarm Day of the Week enable: 0=ignore, 1=match Default Value: 0
26 : 24	ALM_DAY	Alarm Day of the week, 1-7 It is up to the user to define the meaning of the values, but 1=Monday is recommended Default Value: 1
23	ALM_HOUR_EN	Alarm hour enable: 0=ignore, 1=match Default Value: 0
20 : 16	ALM_HOUR	Alarm hours, value depending on 12/24HR mode 24HR: [4:0]=0-23 12HR: [4]:0=AM, 1=PM, [3:0]=1-12 Default Value: 0
15	ALM_MIN_EN	Alarm minutes enable: 0=ignore, 1=match Default Value: 0
13 : 8	ALM_MIN	Alarm minutes, 0-59 Default Value: 0
7	ALM_SEC_EN	Alarm second enable: 0=ignore, 1=match Default Value: 0

5 : 0	ALM_SEC	Alarm seconds, 0-59 Default Value: 0

BACKUP_ALM1_DATE

Alarm 1 Day of Month, Month
Address: 0x40270020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None		RW				
HW Access	A	None		A				
Name	ALM_DATE_EN	None [6:5]		ALM_DATE [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None			RW			
HW Access	A	None			A			
Name	ALM_MON_EN	None [14:12]			ALM_MON [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	A	None						
Name	ALM_EN	None [30:24]						

Bits	Name	Description
31	ALM_EN	Master enable for alarm 1. 0: Alarm 1 is disabled. Fields for date and time are ignored. 1: Alarm 1 is enabled. Alarm triggers whenever the new date and time matches all the enabled date and time fields, which can happen more than once depending on configuration. If none of the date and time fields are enabled, then this alarm triggers once every second. Default Value: 0
15	ALM_MON_EN	Alarm Month enable: 0=ignore, 1=match Default Value: 0
11 : 8	ALM_MON	Alarm Month, 1-12 Default Value: 1
7	ALM_DATE_EN	Alarm Day of the Month enable: 0=ignore, 1=match Default Value: 0
4 : 0	ALM_DATE	Alarm Day of the Month, 1-31 Leap Year corrected Default Value: 1

BACKUP_ALM2_TIME

Alarm 2 Seconds, Minute, Hours, Day of Week
Address: 0x40270024
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None	RW					
HW Access	A	None	A					
Name	ALM_SEC_EN	None	ALM_SEC [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None	RW					
HW Access	A	None	A					
Name	ALM_MIN_EN	None	ALM_MIN [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None		RW				
HW Access	A	None		A				
Name	ALM_HOUR_EN	None [22:21]		ALM_HOUR [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None				RW		
HW Access	A	None				A		
Name	ALM_DAY_EN	None [30:27]				ALM_DAY [26:24]		

Bits	Name	Description
31	ALM_DAY_EN	Alarm Day of the Week enable: 0=ignore, 1=match Default Value: 0
26 : 24	ALM_DAY	Alarm Day of the week, 1-7 It is up to the user to define the meaning of the values, but 1=Monday is recommended Default Value: 1
23	ALM_HOUR_EN	Alarm hour enable: 0=ignore, 1=match Default Value: 0
20 : 16	ALM_HOUR	Alarm hours, value depending on 12/24HR mode 24HR: [4:0]=0-23 12HR: [4]:0=AM, 1=PM, [3:0]=1-12 Default Value: 0
15	ALM_MIN_EN	Alarm minutes enable: 0=ignore, 1=match Default Value: 0
13 : 8	ALM_MIN	Alarm minutes, 0-59 Default Value: 0
7	ALM_SEC_EN	Alarm second enable: 0=ignore, 1=match Default Value: 0

5 : 0	ALM_SEC	Alarm seconds, 0-59 Default Value: 0

BACKUP_ALM2_DATE

Alarm 2 Day of Month, Month
Address: 0x40270028
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None		RW				
HW Access	A	None		A				
Name	ALM_DATE_EN	None [6:5]		ALM_DATE [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None			RW			
HW Access	A	None			A			
Name	ALM_MON_EN	None [14:12]			ALM_MON [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	A	None						
Name	ALM_EN	None [30:24]						

Bits	Name	Description
31	ALM_EN	Master enable for alarm 2. 0: Alarm 2 is disabled. Fields for date and time are ignored. 1: Alarm 2 is enabled. Alarm triggers whenever the new date and time matches all the enabled date and time fields, which can happen more than once depending on configuration. If none of the date and time fields are enabled, then this alarm triggers once every second. Default Value: 0
15	ALM_MON_EN	Alarm Month enable: 0=ignore, 1=match Default Value: 0
11 : 8	ALM_MON	Alarm Month, 1-12 Default Value: 1
7	ALM_DATE_EN	Alarm Day of the Month enable: 0=ignore, 1=match Default Value: 0
4 : 0	ALM_DATE	Alarm Day of the Month, 1-31 Leap Year corrected Default Value: 1

BACKUP_INTR

Interrupt request register
Address: 0x4027002C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [7:3]					CENTURY	ALARM2	ALARM1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CENTURY	Century overflow interrupt Default Value: 0
1	ALARM2	Alarm 2 Interrupt Default Value: 0
0	ALARM1	Alarm 1 Interrupt Default Value: 0

BACKUP_INTR_SET

Interrupt set request register
Address: 0x40270030
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [7:3]					CENTURY	ALARM2	ALARM1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CENTURY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	ALARM2	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	ALARM1	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

BACKUP_INTR_MASK

Interrupt mask register
Address: 0x40270034
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					CENTURY	ALARM2	ALARM1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CENTURY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	ALARM2	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	ALARM1	Mask bit for corresponding bit in interrupt request register. Default Value: 0

BACKUP_INTR_MASKED

Interrupt masked request register
Address: 0x40270038
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					RW	RW	RW
Name	None [7:3]					CENTURY	ALARM2	ALARM1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CENTURY	Logical and of corresponding request and mask bits. Default Value: 0
1	ALARM2	Logical and of corresponding request and mask bits. Default Value: 0
0	ALARM1	Logical and of corresponding request and mask bits. Default Value: 0

BACKUP_RESET

Backup reset register
Address: 0x40270048
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	None						
HW Access	A	None						
Name	RESET	None [30:24]						

Bits	Name	Description
31	RESET	Writing 1 to this register resets the backup logic. Hardware clears it when the reset is complete. After setting this register, firmware should confirm it reads as 0 before attempting to write other backup registers. Default Value: 0

BACKUP_BREG0

Backup register region
Address: 0x40271000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	BREG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	BREG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	BREG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	BREG [31:24]							

Bits	Name	Description
31 : 0	BREG	Backup memory that contains application-specific data. Memory is retained on vbackup supply. Default Value: 0

11 IO subsystem

Register details

Register name	Address	Description
HSIOM_PRT0_PORT_SEL0	0x40300000	Port selection 0
HSIOM_PRT1_PORT_SEL0	0x40300010	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT2_PORT_SEL0	0x40300020	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT2_PORT_SEL1	0x40300024	Port selection 1
HSIOM_PRT3_PORT_SEL0	0x40300030	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT3_PORT_SEL1	0x40300034	Port selection 1. See HSIOM_PRT2_PORT_SEL1 for the details of bit fields.
HSIOM_PRT4_PORT_SEL0	0x40300040	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT4_PORT_SEL1	0x40300044	Port selection 1
HSIOM_PRT5_PORT_SEL0	0x40300050	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT5_PORT_SEL1	0x40300054	Port selection 1. See HSIOM_PRT2_PORT_SEL1 for the details of bit fields.
HSIOM_PRT6_PORT_SEL0	0x40300060	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT6_PORT_SEL1	0x40300064	Port selection 1
HSIOM_PRT7_PORT_SEL0	0x40300070	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT7_PORT_SEL1	0x40300074	Port selection 1. See HSIOM_PRT6_PORT_SEL1 for the details of bit fields.
HSIOM_PRT8_PORT_SEL0	0x40300080	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT8_PORT_SEL1	0x40300084	Port selection 1. See HSIOM_PRT4_PORT_SEL1 for the details of bit fields.
HSIOM_PRT9_PORT_SEL0	0x40300090	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT10_PORT_SEL0	0x403000A0	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT10_PORT_SEL1	0x403000A4	Port selection 1. See HSIOM_PRT6_PORT_SEL1 for the details of bit fields.
HSIOM_PRT11_PORT_SEL0	0x403000B0	Port selection 0
HSIOM_PRT12_PORT_SEL0	0x403000C0	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT12_PORT_SEL1	0x403000C4	Port selection 1. See HSIOM_PRT6_PORT_SEL1 for the details of bit fields.
HSIOM_PRT13_PORT_SEL0	0x403000D0	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.

Register name	Address	Description
HSIOM_PRT13_PORT_SEL1	0x403000D4	Port selection 1. See HSIOM_PRT6_PORT_SEL1 for the details of bit fields.
HSIOM_PRT14_PORT_SEL0	0x403000E0	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT14_PORT_SEL1	0x403000E4	Port selection 1. See HSIOM_PRT6_PORT_SEL1 for the details of bit fields.
HSIOM_PRT15_PORT_SEL0	0x403000F0	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT16_PORT_SEL0	0x40300100	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT17_PORT_SEL0	0x40300110	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT17_PORT_SEL1	0x40300114	Port selection 1. See HSIOM_PRT6_PORT_SEL1 for the details of bit fields.
HSIOM_PRT18_PORT_SEL0	0x40300120	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT18_PORT_SEL1	0x40300124	Port selection 1. See HSIOM_PRT6_PORT_SEL1 for the details of bit fields.
HSIOM_PRT19_PORT_SEL0	0x40300130	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT19_PORT_SEL1	0x40300134	Port selection 1. See HSIOM_PRT4_PORT_SEL1 for the details of bit fields.
HSIOM_PRT20_PORT_SEL0	0x40300140	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT20_PORT_SEL1	0x40300144	Port selection 1. See HSIOM_PRT6_PORT_SEL1 for the details of bit fields.
HSIOM_PRT21_PORT_SEL0	0x40300150	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT21_PORT_SEL1	0x40300154	Port selection 1. See HSIOM_PRT6_PORT_SEL1 for the details of bit fields.
HSIOM_PRT22_PORT_SEL0	0x40300160	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT22_PORT_SEL1	0x40300164	Port selection 1. See HSIOM_PRT6_PORT_SEL1 for the details of bit fields.
HSIOM_PRT23_PORT_SEL0	0x40300170	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT23_PORT_SEL1	0x40300174	Port selection 1. See HSIOM_PRT6_PORT_SEL1 for the details of bit fields.
HSIOM_AMUX_SPLIT_CTL0	0x40302000	AMUX splitter cell control
HSIOM_AMUX_SPLIT_CTL1	0x40302004	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.
HSIOM_AMUX_SPLIT_CTL2	0x40302008	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.
HSIOM_MONITOR_CTL_0	0x40302200	Power/Ground Monitor cell control 0
HSIOM_ALT_JTAG_EN	0x40302240	Alternate JTAG IF selection register

Register name	Address	Description
GPIO_PRT0_OUT	0x40310000	Port output data register
GPIO_PRT0_OUT_CLR	0x40310004	Port output data clear register
GPIO_PRT0_OUT_SET	0x40310008	Port output data set register
GPIO_PRT0_OUT_INV	0x4031000C	Port output data invert register
GPIO_PRT0_IN	0x40310010	Port input state register
GPIO_PRT0_INTR	0x40310014	Port interrupt status register
GPIO_PRT0_INTR_MASK	0x40310018	Port interrupt mask register
GPIO_PRT0_INTR_MASKED	0x4031001C	Port interrupt masked status register
GPIO_PRT0_INTR_SET	0x40310020	Port interrupt set register
GPIO_PRT0_INTR_CFG	0x40310040	Port interrupt configuration register
GPIO_PRT0_CFG	0x40310044	Port configuration register
GPIO_PRT0_CFG_IN	0x40310048	Port input buffer configuration register
GPIO_PRT0_CFG_OUT	0x4031004C	Port output buffer configuration register
GPIO_PRT0_CFG_IN_AUTOLVL	0x40310058	Port input buffer AUTOLVL configuration register
GPIO_PRT1_OUT	0x40310080	Port output data register. See GPIO_PRT0_OUT for the details of bit fields.
GPIO_PRT1_OUT_CLR	0x40310084	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT1_OUT_SET	0x40310088	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT1_OUT_INV	0x4031008C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT1_IN	0x40310090	Port input state register. See GPIO_PRT0_IN for the details of bit fields.
GPIO_PRT1_INTR	0x40310094	Port interrupt status register. See GPIO_PRT0_INTR for the details of bit fields.
GPIO_PRT1_INTR_MASK	0x40310098	Port interrupt mask register. See GPIO_PRT0_INTR_MASK for the details of bit fields.
GPIO_PRT1_INTR_MASKED	0x4031009C	Port interrupt masked status register. See GPIO_PRT0_INTR_MASKED for the details of bit fields.
GPIO_PRT1_INTR_SET	0x403100A0	Port interrupt set register. See GPIO_PRT0_INTR_SET for the details of bit fields.
GPIO_PRT1_INTR_CFG	0x403100C0	Port interrupt configuration register. See GPIO_PRT0_INTR_CFG for the details of bit fields.
GPIO_PRT1_CFG	0x403100C4	Port configuration register. See GPIO_PRT0_CFG for the details of bit fields.
GPIO_PRT1_CFG_IN	0x403100C8	Port input buffer configuration register. See GPIO_PRT0_CFG_IN for the details of bit fields.
GPIO_PRT1_CFG_OUT	0x403100CC	Port output buffer configuration register
GPIO_PRT1_CFG_IN_AUTOLVL	0x403100D8	Port input buffer AUTOLVL configuration register. See GPIO_PRT0_CFG_IN_AUTOLVL for the details of bit fields.

Register name	Address	Description
GPIO_PRT2_OUT	0x40310100	Port output data register
GPIO_PRT2_OUT_CLR	0x40310104	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT2_OUT_SET	0x40310108	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT2_OUT_INV	0x4031010C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT2_IN	0x40310110	Port input state register
GPIO_PRT2_INTR	0x40310114	Port interrupt status register
GPIO_PRT2_INTR_MASK	0x40310118	Port interrupt mask register
GPIO_PRT2_INTR_MASKED	0x4031011C	Port interrupt masked status register
GPIO_PRT2_INTR_SET	0x40310120	Port interrupt set register
GPIO_PRT2_INTR_CFG	0x40310140	Port interrupt configuration register
GPIO_PRT2_CFG	0x40310144	Port configuration register
GPIO_PRT2_CFG_IN	0x40310148	Port input buffer configuration register
GPIO_PRT2_CFG_OUT	0x4031014C	Port output buffer configuration register
GPIO_PRT2_CFG_IN_AUTOLVL	0x40310158	Port input buffer AUTOLVL configuration register
GPIO_PRT3_OUT	0x40310180	Port output data register. See GPIO_PRT2_OUT for the details of bit fields.
GPIO_PRT3_OUT_CLR	0x40310184	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT3_OUT_SET	0x40310188	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT3_OUT_INV	0x4031018C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT3_IN	0x40310190	Port input state register. See GPIO_PRT2_IN for the details of bit fields.
GPIO_PRT3_INTR	0x40310194	Port interrupt status register. See GPIO_PRT2_INTR for the details of bit fields.
GPIO_PRT3_INTR_MASK	0x40310198	Port interrupt mask register. See GPIO_PRT2_INTR_MASK for the details of bit fields.
GPIO_PRT3_INTR_MASKED	0x4031019C	Port interrupt masked status register. See GPIO_PRT2_INTR_MASKED for the details of bit fields.
GPIO_PRT3_INTR_SET	0x403101A0	Port interrupt set register. See GPIO_PRT2_INTR_SET for the details of bit fields.
GPIO_PRT3_INTR_CFG	0x403101C0	Port interrupt configuration register. See GPIO_PRT2_INTR_CFG for the details of bit fields.
GPIO_PRT3_CFG	0x403101C4	Port configuration register. See GPIO_PRT2_CFG for the details of bit fields.
GPIO_PRT3_CFG_IN	0x403101C8	Port input buffer configuration register. See GPIO_PRT2_CFG_IN for the details of bit fields.
GPIO_PRT3_CFG_OUT	0x403101CC	Port output buffer configuration register. See GPIO_PRT2_CFG_OUT for the details of bit fields.

Register name	Address	Description
GPIO_PRT3_CFG_IN_AUTOLVL	0x403101D8	Port input buffer AUTOLVL configuration register. See GPIO_PRT2_CFG_IN_AUTOLVL for the details of bit fields.
GPIO_PRT4_OUT	0x40310200	Port output data register
GPIO_PRT4_OUT_CLR	0x40310204	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT4_OUT_SET	0x40310208	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT4_OUT_INV	0x4031020C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT4_IN	0x40310210	Port input state register
GPIO_PRT4_INTR	0x40310214	Port interrupt status register
GPIO_PRT4_INTR_MASK	0x40310218	Port interrupt mask register
GPIO_PRT4_INTR_MASKED	0x4031021C	Port interrupt masked status register
GPIO_PRT4_INTR_SET	0x40310220	Port interrupt set register
GPIO_PRT4_INTR_CFG	0x40310240	Port interrupt configuration register
GPIO_PRT4_CFG	0x40310244	Port configuration register
GPIO_PRT4_CFG_IN	0x40310248	Port input buffer configuration register
GPIO_PRT4_CFG_OUT	0x4031024C	Port output buffer configuration register
GPIO_PRT4_CFG_IN_AUTOLVL	0x40310258	Port input buffer AUTOLVL configuration register
GPIO_PRT5_OUT	0x40310280	Port output data register. See GPIO_PRT2_OUT for the details of bit fields.
GPIO_PRT5_OUT_CLR	0x40310284	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT5_OUT_SET	0x40310288	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT5_OUT_INV	0x4031028C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT5_IN	0x40310290	Port input state register. See GPIO_PRT2_IN for the details of bit fields.
GPIO_PRT5_INTR	0x40310294	Port interrupt status register. See GPIO_PRT2_INTR for the details of bit fields.
GPIO_PRT5_INTR_MASK	0x40310298	Port interrupt mask register. See GPIO_PRT2_INTR_MASK for the details of bit fields.
GPIO_PRT5_INTR_MASKED	0x4031029C	Port interrupt masked status register. See GPIO_PRT2_INTR_MASKED for the details of bit fields.
GPIO_PRT5_INTR_SET	0x403102A0	Port interrupt set register. See GPIO_PRT2_INTR_SET for the details of bit fields.
GPIO_PRT5_INTR_CFG	0x403102C0	Port interrupt configuration register. See GPIO_PRT2_INTR_CFG for the details of bit fields.
GPIO_PRT5_CFG	0x403102C4	Port configuration register. See GPIO_PRT2_CFG for the details of bit fields.

Register name	Address	Description
GPIO_PRT5_CFG_IN	0x403102C8	Port input buffer configuration register. See GPIO_PRT2_CFG_IN for the details of bit fields.
GPIO_PRT5_CFG_OUT	0x403102CC	Port output buffer configuration register. See GPIO_PRT2_CFG_OUT for the details of bit fields.
GPIO_PRT5_CFG_IN_AUTOLVL	0x403102D8	Port input buffer AUTOLVL configuration register. See GPIO_PRT2_CFG_IN_AUTOLVL for the details of bit fields.
GPIO_PRT6_OUT	0x40310300	Port output data register
GPIO_PRT6_OUT_CLR	0x40310304	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT6_OUT_SET	0x40310308	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT6_OUT_INV	0x4031030C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT6_IN	0x40310310	Port input state register
GPIO_PRT6_INTR	0x40310314	Port interrupt status register
GPIO_PRT6_INTR_MASK	0x40310318	Port interrupt mask register
GPIO_PRT6_INTR_MASKED	0x4031031C	Port interrupt masked status register
GPIO_PRT6_INTR_SET	0x40310320	Port interrupt set register
GPIO_PRT6_INTR_CFG	0x40310340	Port interrupt configuration register
GPIO_PRT6_CFG	0x40310344	Port configuration register
GPIO_PRT6_CFG_IN	0x40310348	Port input buffer configuration register
GPIO_PRT6_CFG_OUT	0x4031034C	Port output buffer configuration register
GPIO_PRT6_CFG_IN_AUTOLVL	0x40310358	Port input buffer AUTOLVL configuration register
GPIO_PRT7_OUT	0x40310380	Port output data register. See GPIO_PRT6_OUT for the details of bit fields.
GPIO_PRT7_OUT_CLR	0x40310384	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT7_OUT_SET	0x40310388	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT7_OUT_INV	0x4031038C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT7_IN	0x40310390	Port input state register. See GPIO_PRT6_IN for the details of bit fields.
GPIO_PRT7_INTR	0x40310394	Port interrupt status register. See GPIO_PRT6_INTR for the details of bit fields.
GPIO_PRT7_INTR_MASK	0x40310398	Port interrupt mask register. See GPIO_PRT6_INTR_MASK for the details of bit fields.
GPIO_PRT7_INTR_MASKED	0x4031039C	Port interrupt masked status register. See GPIO_PRT6_INTR_MASKED for the details of bit fields.
GPIO_PRT7_INTR_SET	0x403103A0	Port interrupt set register. See GPIO_PRT6_INTR_SET for the details of bit fields.

Register name	Address	Description
GPIO_PRT7_INTR_CFG	0x403103C0	Port interrupt configuration register. See GPIO_PRT6_INTR_CFG for the details of bit fields.
GPIO_PRT7_CFG	0x403103C4	Port configuration register. See GPIO_PRT6_CFG for the details of bit fields.
GPIO_PRT7_CFG_IN	0x403103C8	Port input buffer configuration register. See GPIO_PRT6_CFG_IN for the details of bit fields.
GPIO_PRT7_CFG_OUT	0x403103CC	Port output buffer configuration register. See GPIO_PRT6_CFG_OUT for the details of bit fields.
GPIO_PRT7_CFG_IN_AUTOLVL	0x403103D8	Port input buffer AUTOLVL configuration register. See GPIO_PRT6_CFG_IN_AUTOLVL for the details of bit fields.
GPIO_PRT8_OUT	0x40310400	Port output data register. See GPIO_PRT4_OUT for the details of bit fields.
GPIO_PRT8_OUT_CLR	0x40310404	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT8_OUT_SET	0x40310408	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT8_OUT_INV	0x4031040C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT8_IN	0x40310410	Port input state register. See GPIO_PRT4_IN for the details of bit fields.
GPIO_PRT8_INTR	0x40310414	Port interrupt status register. See GPIO_PRT4_INTR for the details of bit fields.
GPIO_PRT8_INTR_MASK	0x40310418	Port interrupt mask register. See GPIO_PRT4_INTR_MASK for the details of bit fields.
GPIO_PRT8_INTR_MASKED	0x4031041C	Port interrupt masked status register. See GPIO_PRT4_INTR_MASKED for the details of bit fields.
GPIO_PRT8_INTR_SET	0x40310420	Port interrupt set register. See GPIO_PRT4_INTR_SET for the details of bit fields.
GPIO_PRT8_INTR_CFG	0x40310440	Port interrupt configuration register. See GPIO_PRT4_INTR_CFG for the details of bit fields.
GPIO_PRT8_CFG	0x40310444	Port configuration register. See GPIO_PRT4_CFG for the details of bit fields.
GPIO_PRT8_CFG_IN	0x40310448	Port input buffer configuration register. See GPIO_PRT4_CFG_IN for the details of bit fields.
GPIO_PRT8_CFG_OUT	0x4031044C	Port output buffer configuration register. See GPIO_PRT4_CFG_OUT for the details of bit fields.
GPIO_PRT8_CFG_IN_AUTOLVL	0x40310458	Port input buffer AUTOLVL configuration register. See GPIO_PRT4_CFG_IN_AUTOLVL for the details of bit fields.
GPIO_PRT9_OUT	0x40310480	Port output data register. See GPIO_PRT0_OUT for the details of bit fields.
GPIO_PRT9_OUT_CLR	0x40310484	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT9_OUT_SET	0x40310488	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.

Register name	Address	Description
GPIO_PRT9_OUT_INV	0x4031048C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT9_IN	0x40310490	Port input state register. See GPIO_PRT0_IN for the details of bit fields.
GPIO_PRT9_INTR	0x40310494	Port interrupt status register. See GPIO_PRT0_INTR for the details of bit fields.
GPIO_PRT9_INTR_MASK	0x40310498	Port interrupt mask register. See GPIO_PRT0_INTR_MASK for the details of bit fields.
GPIO_PRT9_INTR_MASKED	0x4031049C	Port interrupt masked status register. See GPIO_PRT0_INTR_MASKED for the details of bit fields.
GPIO_PRT9_INTR_SET	0x403104A0	Port interrupt set register. See GPIO_PRT0_INTR_SET for the details of bit fields.
GPIO_PRT9_INTR_CFG	0x403104C0	Port interrupt configuration register. See GPIO_PRT0_INTR_CFG for the details of bit fields.
GPIO_PRT9_CFG	0x403104C4	Port configuration register. See GPIO_PRT0_CFG for the details of bit fields.
GPIO_PRT9_CFG_IN	0x403104C8	Port input buffer configuration register. See GPIO_PRT0_CFG_IN for the details of bit fields.
GPIO_PRT9_CFG_OUT	0x403104CC	Port output buffer configuration register. See GPIO_PRT1_CFG_OUT for the details of bit fields.
GPIO_PRT9_CFG_IN_AUTOLVL	0x403104D8	Port input buffer AUTOLVL configuration register. See GPIO_PRT0_CFG_IN_AUTOLVL for the details of bit fields.
GPIO_PRT10_OUT	0x40310500	Port output data register. See GPIO_PRT6_OUT for the details of bit fields.
GPIO_PRT10_OUT_CLR	0x40310504	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT10_OUT_SET	0x40310508	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT10_OUT_INV	0x4031050C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT10_IN	0x40310510	Port input state register. See GPIO_PRT6_IN for the details of bit fields.
GPIO_PRT10_INTR	0x40310514	Port interrupt status register. See GPIO_PRT6_INTR for the details of bit fields.
GPIO_PRT10_INTR_MASK	0x40310518	Port interrupt mask register. See GPIO_PRT6_INTR_MASK for the details of bit fields.
GPIO_PRT10_INTR_MASKED	0x4031051C	Port interrupt masked status register. See GPIO_PRT6_INTR_MASKED for the details of bit fields.
GPIO_PRT10_INTR_SET	0x40310520	Port interrupt set register. See GPIO_PRT6_INTR_SET for the details of bit fields.
GPIO_PRT10_INTR_CFG	0x40310540	Port interrupt configuration register. See GPIO_PRT6_INTR_CFG for the details of bit fields.
GPIO_PRT10_CFG	0x40310544	Port configuration register. See GPIO_PRT6_CFG for the details of bit fields.

Register name	Address	Description
GPIO_PRT10_CFG_IN	0x40310548	Port input buffer configuration register. See GPIO_PRT6_CFG_IN for the details of bit fields.
GPIO_PRT10_CFG_OUT	0x4031054C	Port output buffer configuration register. See GPIO_PRT6_CFG_OUT for the details of bit fields.
GPIO_PRT10_CFG_IN_AUTOLVL	0x40310558	Port input buffer AUTOLVL configuration register. See GPIO_PRT6_CFG_IN_AUTOLVL for the details of bit fields.
GPIO_PRT11_OUT	0x40310580	Port output data register
GPIO_PRT11_OUT_CLR	0x40310584	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT11_OUT_SET	0x40310588	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT11_OUT_INV	0x4031058C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT11_IN	0x40310590	Port input state register
GPIO_PRT11_INTR	0x40310594	Port interrupt status register
GPIO_PRT11_INTR_MASK	0x40310598	Port interrupt mask register
GPIO_PRT11_INTR_MASKED	0x4031059C	Port interrupt masked status register
GPIO_PRT11_INTR_SET	0x403105A0	Port interrupt set register
GPIO_PRT11_INTR_CFG	0x403105C0	Port interrupt configuration register
GPIO_PRT11_CFG	0x403105C4	Port configuration register
GPIO_PRT11_CFG_IN	0x403105C8	Port input buffer configuration register
GPIO_PRT11_CFG_OUT	0x403105CC	Port output buffer configuration register
GPIO_PRT11_CFG_IN_AUTOLVL	0x403105D8	Port input buffer AUTOLVL configuration register
GPIO_PRT12_OUT	0x40310600	Port output data register. See GPIO_PRT6_OUT for the details of bit fields.
GPIO_PRT12_OUT_CLR	0x40310604	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT12_OUT_SET	0x40310608	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT12_OUT_INV	0x4031060C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT12_IN	0x40310610	Port input state register. See GPIO_PRT6_IN for the details of bit fields.
GPIO_PRT12_INTR	0x40310614	Port interrupt status register. See GPIO_PRT6_INTR for the details of bit fields.
GPIO_PRT12_INTR_MASK	0x40310618	Port interrupt mask register. See GPIO_PRT6_INTR_MASK for the details of bit fields.
GPIO_PRT12_INTR_MASKED	0x4031061C	Port interrupt masked status register. See GPIO_PRT6_INTR_MASKED for the details of bit fields.
GPIO_PRT12_INTR_SET	0x40310620	Port interrupt set register. See GPIO_PRT6_INTR_SET for the details of bit fields.

Register name	Address	Description
GPIO_PRT12_INTR_CFG	0x40310640	Port interrupt configuration register. See GPIO_PRT6_INTR_CFG for the details of bit fields.
GPIO_PRT12_CFG	0x40310644	Port configuration register. See GPIO_PRT6_CFG for the details of bit fields.
GPIO_PRT12_CFG_IN	0x40310648	Port input buffer configuration register. See GPIO_PRT6_CFG_IN for the details of bit fields.
GPIO_PRT12_CFG_OUT	0x4031064C	Port output buffer configuration register. See GPIO_PRT6_CFG_OUT for the details of bit fields.
GPIO_PRT12_CFG_IN_AUTOLVL	0x40310658	Port input buffer AUTOLVL configuration register. See GPIO_PRT6_CFG_IN_AUTOLVL for the details of bit fields.
GPIO_PRT13_OUT	0x40310680	Port output data register. See GPIO_PRT6_OUT for the details of bit fields.
GPIO_PRT13_OUT_CLR	0x40310684	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT13_OUT_SET	0x40310688	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT13_OUT_INV	0x4031068C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT13_IN	0x40310690	Port input state register. See GPIO_PRT6_IN for the details of bit fields.
GPIO_PRT13_INTR	0x40310694	Port interrupt status register. See GPIO_PRT6_INTR for the details of bit fields.
GPIO_PRT13_INTR_MASK	0x40310698	Port interrupt mask register. See GPIO_PRT6_INTR_MASK for the details of bit fields.
GPIO_PRT13_INTR_MASKED	0x4031069C	Port interrupt masked status register. See GPIO_PRT6_INTR_MASKED for the details of bit fields.
GPIO_PRT13_INTR_SET	0x403106A0	Port interrupt set register. See GPIO_PRT6_INTR_SET for the details of bit fields.
GPIO_PRT13_INTR_CFG	0x403106C0	Port interrupt configuration register. See GPIO_PRT6_INTR_CFG for the details of bit fields.
GPIO_PRT13_CFG	0x403106C4	Port configuration register. See GPIO_PRT6_CFG for the details of bit fields.
GPIO_PRT13_CFG_IN	0x403106C8	Port input buffer configuration register. See GPIO_PRT6_CFG_IN for the details of bit fields.
GPIO_PRT13_CFG_OUT	0x403106CC	Port output buffer configuration register. See GPIO_PRT6_CFG_OUT for the details of bit fields.
GPIO_PRT13_CFG_IN_AUTOLVL	0x403106D8	Port input buffer AUTOLVL configuration register. See GPIO_PRT6_CFG_IN_AUTOLVL for the details of bit fields.
GPIO_PRT14_OUT	0x40310700	Port output data register. See GPIO_PRT6_OUT for the details of bit fields.
GPIO_PRT14_OUT_CLR	0x40310704	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT14_OUT_SET	0x40310708	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.

Register name	Address	Description
GPIO_PRT14_OUT_INV	0x4031070C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT14_IN	0x40310710	Port input state register. See GPIO_PRT6_IN for the details of bit fields.
GPIO_PRT14_INTR	0x40310714	Port interrupt status register. See GPIO_PRT6_INTR for the details of bit fields.
GPIO_PRT14_INTR_MASK	0x40310718	Port interrupt mask register. See GPIO_PRT6_INTR_MASK for the details of bit fields.
GPIO_PRT14_INTR_MASKED	0x4031071C	Port interrupt masked status register. See GPIO_PRT6_INTR_MASKED for the details of bit fields.
GPIO_PRT14_INTR_SET	0x40310720	Port interrupt set register. See GPIO_PRT6_INTR_SET for the details of bit fields.
GPIO_PRT14_INTR_CFG	0x40310740	Port interrupt configuration register. See GPIO_PRT6_INTR_CFG for the details of bit fields.
GPIO_PRT14_CFG	0x40310744	Port configuration register. See GPIO_PRT6_CFG for the details of bit fields.
GPIO_PRT14_CFG_IN	0x40310748	Port input buffer configuration register. See GPIO_PRT6_CFG_IN for the details of bit fields.
GPIO_PRT14_CFG_OUT	0x4031074C	Port output buffer configuration register. See GPIO_PRT6_CFG_OUT for the details of bit fields.
GPIO_PRT14_CFG_IN_AUTOLVL	0x40310758	Port input buffer AUTOLVL configuration register. See GPIO_PRT6_CFG_IN_AUTOLVL for the details of bit fields.
GPIO_PRT15_OUT	0x40310780	Port output data register. See GPIO_PRT0_OUT for the details of bit fields.
GPIO_PRT15_OUT_CLR	0x40310784	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT15_OUT_SET	0x40310788	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT15_OUT_INV	0x4031078C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT15_IN	0x40310790	Port input state register. See GPIO_PRT0_IN for the details of bit fields.
GPIO_PRT15_INTR	0x40310794	Port interrupt status register. See GPIO_PRT0_INTR for the details of bit fields.
GPIO_PRT15_INTR_MASK	0x40310798	Port interrupt mask register. See GPIO_PRT0_INTR_MASK for the details of bit fields.
GPIO_PRT15_INTR_MASKED	0x4031079C	Port interrupt masked status register. See GPIO_PRT0_INTR_MASKED for the details of bit fields.
GPIO_PRT15_INTR_SET	0x403107A0	Port interrupt set register. See GPIO_PRT0_INTR_SET for the details of bit fields.
GPIO_PRT15_INTR_CFG	0x403107C0	Port interrupt configuration register. See GPIO_PRT0_INTR_CFG for the details of bit fields.
GPIO_PRT15_CFG	0x403107C4	Port configuration register. See GPIO_PRT0_CFG for the details of bit fields.

Register name	Address	Description
GPIO_PRT15_CFG_IN	0x403107C8	Port input buffer configuration register. See GPIO_PRT0_CFG_IN for the details of bit fields.
GPIO_PRT15_CFG_OUT	0x403107CC	Port output buffer configuration register. See GPIO_PRT1_CFG_OUT for the details of bit fields.
GPIO_PRT15_CFG_IN_AUTOLVL	0x403107D8	Port input buffer AUTOLVL configuration register. See GPIO_PRT0_CFG_IN_AUTOLVL for the details of bit fields.
GPIO_PRT16_OUT	0x40310800	Port output data register. See GPIO_PRT0_OUT for the details of bit fields.
GPIO_PRT16_OUT_CLR	0x40310804	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT16_OUT_SET	0x40310808	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT16_OUT_INV	0x4031080C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT16_IN	0x40310810	Port input state register. See GPIO_PRT0_IN for the details of bit fields.
GPIO_PRT16_INTR	0x40310814	Port interrupt status register. See GPIO_PRT0_INTR for the details of bit fields.
GPIO_PRT16_INTR_MASK	0x40310818	Port interrupt mask register. See GPIO_PRT0_INTR_MASK for the details of bit fields.
GPIO_PRT16_INTR_MASKED	0x4031081C	Port interrupt masked status register. See GPIO_PRT0_INTR_MASKED for the details of bit fields.
GPIO_PRT16_INTR_SET	0x40310820	Port interrupt set register. See GPIO_PRT0_INTR_SET for the details of bit fields.
GPIO_PRT16_INTR_CFG	0x40310840	Port interrupt configuration register. See GPIO_PRT0_INTR_CFG for the details of bit fields.
GPIO_PRT16_CFG	0x40310844	Port configuration register. See GPIO_PRT0_CFG for the details of bit fields.
GPIO_PRT16_CFG_IN	0x40310848	Port input buffer configuration register. See GPIO_PRT0_CFG_IN for the details of bit fields.
GPIO_PRT16_CFG_OUT	0x4031084C	Port output buffer configuration register. See GPIO_PRT1_CFG_OUT for the details of bit fields.
GPIO_PRT16_CFG_IN_AUTOLVL	0x40310858	Port input buffer AUTOLVL configuration register. See GPIO_PRT0_CFG_IN_AUTOLVL for the details of bit fields.
GPIO_PRT17_OUT	0x40310880	Port output data register. See GPIO_PRT6_OUT for the details of bit fields.
GPIO_PRT17_OUT_CLR	0x40310884	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT17_OUT_SET	0x40310888	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT17_OUT_INV	0x4031088C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT17_IN	0x40310890	Port input state register. See GPIO_PRT6_IN for the details of bit fields.

Register name	Address	Description
GPIO_PRT17_INTR	0x40310894	Port interrupt status register. See GPIO_PRT6_INTR for the details of bit fields.
GPIO_PRT17_INTR_MASK	0x40310898	Port interrupt mask register. See GPIO_PRT6_INTR_MASK for the details of bit fields.
GPIO_PRT17_INTR_MASKED	0x4031089C	Port interrupt masked status register. See GPIO_PRT6_INTR_MASKED for the details of bit fields.
GPIO_PRT17_INTR_SET	0x403108A0	Port interrupt set register. See GPIO_PRT6_INTR_SET for the details of bit fields.
GPIO_PRT17_INTR_CFG	0x403108C0	Port interrupt configuration register. See GPIO_PRT6_INTR_CFG for the details of bit fields.
GPIO_PRT17_CFG	0x403108C4	Port configuration register. See GPIO_PRT6_CFG for the details of bit fields.
GPIO_PRT17_CFG_IN	0x403108C8	Port input buffer configuration register. See GPIO_PRT6_CFG_IN for the details of bit fields.
GPIO_PRT17_CFG_OUT	0x403108CC	Port output buffer configuration register. See GPIO_PRT6_CFG_OUT for the details of bit fields.
GPIO_PRT17_CFG_IN_AUTOLVL	0x403108D8	Port input buffer AUTOLVL configuration register. See GPIO_PRT6_CFG_IN_AUTOLVL for the details of bit fields.
GPIO_PRT18_OUT	0x40310900	Port output data register. See GPIO_PRT6_OUT for the details of bit fields.
GPIO_PRT18_OUT_CLR	0x40310904	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT18_OUT_SET	0x40310908	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT18_OUT_INV	0x4031090C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT18_IN	0x40310910	Port input state register. See GPIO_PRT6_IN for the details of bit fields.
GPIO_PRT18_INTR	0x40310914	Port interrupt status register. See GPIO_PRT6_INTR for the details of bit fields.
GPIO_PRT18_INTR_MASK	0x40310918	Port interrupt mask register. See GPIO_PRT6_INTR_MASK for the details of bit fields.
GPIO_PRT18_INTR_MASKED	0x4031091C	Port interrupt masked status register. See GPIO_PRT6_INTR_MASKED for the details of bit fields.
GPIO_PRT18_INTR_SET	0x40310920	Port interrupt set register. See GPIO_PRT6_INTR_SET for the details of bit fields.
GPIO_PRT18_INTR_CFG	0x40310940	Port interrupt configuration register. See GPIO_PRT6_INTR_CFG for the details of bit fields.
GPIO_PRT18_CFG	0x40310944	Port configuration register. See GPIO_PRT6_CFG for the details of bit fields.
GPIO_PRT18_CFG_IN	0x40310948	Port input buffer configuration register. See GPIO_PRT6_CFG_IN for the details of bit fields.
GPIO_PRT18_CFG_OUT	0x4031094C	Port output buffer configuration register. See GPIO_PRT6_CFG_OUT for the details of bit fields.

Register name	Address	Description
GPIO_PRT18_CFG_IN_AUTOLVL	0x40310958	Port input buffer AUTOLVL configuration register. See GPIO_PRT6_CFG_IN_AUTOLVL for the details of bit fields.
GPIO_PRT19_OUT	0x40310980	Port output data register. See GPIO_PRT4_OUT for the details of bit fields.
GPIO_PRT19_OUT_CLR	0x40310984	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT19_OUT_SET	0x40310988	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT19_OUT_INV	0x4031098C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT19_IN	0x40310990	Port input state register. See GPIO_PRT4_IN for the details of bit fields.
GPIO_PRT19_INTR	0x40310994	Port interrupt status register. See GPIO_PRT4_INTR for the details of bit fields.
GPIO_PRT19_INTR_MASK	0x40310998	Port interrupt mask register. See GPIO_PRT4_INTR_MASK for the details of bit fields.
GPIO_PRT19_INTR_MASKED	0x4031099C	Port interrupt masked status register. See GPIO_PRT4_INTR_MASKED for the details of bit fields.
GPIO_PRT19_INTR_SET	0x403109A0	Port interrupt set register. See GPIO_PRT4_INTR_SET for the details of bit fields.
GPIO_PRT19_INTR_CFG	0x403109C0	Port interrupt configuration register. See GPIO_PRT4_INTR_CFG for the details of bit fields.
GPIO_PRT19_CFG	0x403109C4	Port configuration register. See GPIO_PRT4_CFG for the details of bit fields.
GPIO_PRT19_CFG_IN	0x403109C8	Port input buffer configuration register. See GPIO_PRT4_CFG_IN for the details of bit fields.
GPIO_PRT19_CFG_OUT	0x403109CC	Port output buffer configuration register. See GPIO_PRT4_CFG_OUT for the details of bit fields.
GPIO_PRT19_CFG_IN_AUTOLVL	0x403109D8	Port input buffer AUTOLVL configuration register. See GPIO_PRT4_CFG_IN_AUTOLVL for the details of bit fields.
GPIO_PRT20_OUT	0x40310A00	Port output data register. See GPIO_PRT6_OUT for the details of bit fields.
GPIO_PRT20_OUT_CLR	0x40310A04	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT20_OUT_SET	0x40310A08	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT20_OUT_INV	0x40310A0C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT20_IN	0x40310A10	Port input state register. See GPIO_PRT6_IN for the details of bit fields.
GPIO_PRT20_INTR	0x40310A14	Port interrupt status register. See GPIO_PRT6_INTR for the details of bit fields.
GPIO_PRT20_INTR_MASK	0x40310A18	Port interrupt mask register. See GPIO_PRT6_INTR_MASK for the details of bit fields.

Register name	Address	Description
GPIO_PRT20_INTR_MASKED	0x40310A1C	Port interrupt masked status register. See GPIO_PRT6_INTR_MASKED for the details of bit fields.
GPIO_PRT20_INTR_SET	0x40310A20	Port interrupt set register. See GPIO_PRT6_INTR_SET for the details of bit fields.
GPIO_PRT20_INTR_CFG	0x40310A40	Port interrupt configuration register. See GPIO_PRT6_INTR_CFG for the details of bit fields.
GPIO_PRT20_CFG	0x40310A44	Port configuration register. See GPIO_PRT6_CFG for the details of bit fields.
GPIO_PRT20_CFG_IN	0x40310A48	Port input buffer configuration register. See GPIO_PRT6_CFG_IN for the details of bit fields.
GPIO_PRT20_CFG_OUT	0x40310A4C	Port output buffer configuration register. See GPIO_PRT6_CFG_OUT for the details of bit fields.
GPIO_PRT20_CFG_IN_AUTOLVL	0x40310A58	Port input buffer AUTOLVL configuration register. See GPIO_PRT6_CFG_IN_AUTOLVL for the details of bit fields.
GPIO_PRT21_OUT	0x40310A80	Port output data register. See GPIO_PRT6_OUT for the details of bit fields.
GPIO_PRT21_OUT_CLR	0x40310A84	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT21_OUT_SET	0x40310A88	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT21_OUT_INV	0x40310A8C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT21_IN	0x40310A90	Port input state register. See GPIO_PRT6_IN for the details of bit fields.
GPIO_PRT21_INTR	0x40310A94	Port interrupt status register. See GPIO_PRT6_INTR for the details of bit fields.
GPIO_PRT21_INTR_MASK	0x40310A98	Port interrupt mask register. See GPIO_PRT6_INTR_MASK for the details of bit fields.
GPIO_PRT21_INTR_MASKED	0x40310A9C	Port interrupt masked status register. See GPIO_PRT6_INTR_MASKED for the details of bit fields.
GPIO_PRT21_INTR_SET	0x40310AA0	Port interrupt set register. See GPIO_PRT6_INTR_SET for the details of bit fields.
GPIO_PRT21_INTR_CFG	0x40310AC0	Port interrupt configuration register. See GPIO_PRT6_INTR_CFG for the details of bit fields.
GPIO_PRT21_CFG	0x40310AC4	Port configuration register. See GPIO_PRT6_CFG for the details of bit fields.
GPIO_PRT21_CFG_IN	0x40310AC8	Port input buffer configuration register. See GPIO_PRT6_CFG_IN for the details of bit fields.
GPIO_PRT21_CFG_OUT	0x40310ACC	Port output buffer configuration register. See GPIO_PRT6_CFG_OUT for the details of bit fields.
GPIO_PRT21_CFG_IN_AUTOLVL	0x40310AD8	Port input buffer AUTOLVL configuration register. See GPIO_PRT6_CFG_IN_AUTOLVL for the details of bit fields.
GPIO_PRT22_OUT	0x40310B00	Port output data register. See GPIO_PRT6_OUT for the details of bit fields.

Register name	Address	Description
GPIO_PRT22_OUT_CLR	0x40310B04	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT22_OUT_SET	0x40310B08	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT22_OUT_INV	0x40310B0C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT22_IN	0x40310B10	Port input state register. See GPIO_PRT6_IN for the details of bit fields.
GPIO_PRT22_INTR	0x40310B14	Port interrupt status register. See GPIO_PRT6_INTR for the details of bit fields.
GPIO_PRT22_INTR_MASK	0x40310B18	Port interrupt mask register. See GPIO_PRT6_INTR_MASK for the details of bit fields.
GPIO_PRT22_INTR_MASKED	0x40310B1C	Port interrupt masked status register. See GPIO_PRT6_INTR_MASKED for the details of bit fields.
GPIO_PRT22_INTR_SET	0x40310B20	Port interrupt set register. See GPIO_PRT6_INTR_SET for the details of bit fields.
GPIO_PRT22_INTR_CFG	0x40310B40	Port interrupt configuration register. See GPIO_PRT6_INTR_CFG for the details of bit fields.
GPIO_PRT22_CFG	0x40310B44	Port configuration register. See GPIO_PRT6_CFG for the details of bit fields.
GPIO_PRT22_CFG_IN	0x40310B48	Port input buffer configuration register. See GPIO_PRT6_CFG_IN for the details of bit fields.
GPIO_PRT22_CFG_OUT	0x40310B4C	Port output buffer configuration register. See GPIO_PRT6_CFG_OUT for the details of bit fields.
GPIO_PRT22_CFG_IN_AUTOLVL	0x40310B58	Port input buffer AUTOLVL configuration register. See GPIO_PRT6_CFG_IN_AUTOLVL for the details of bit fields.
GPIO_PRT23_OUT	0x40310B80	Port output data register. See GPIO_PRT6_OUT for the details of bit fields.
GPIO_PRT23_OUT_CLR	0x40310B84	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT23_OUT_SET	0x40310B88	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT23_OUT_INV	0x40310B8C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT23_IN	0x40310B90	Port input state register. See GPIO_PRT6_IN for the details of bit fields.
GPIO_PRT23_INTR	0x40310B94	Port interrupt status register. See GPIO_PRT6_INTR for the details of bit fields.
GPIO_PRT23_INTR_MASK	0x40310B98	Port interrupt mask register. See GPIO_PRT6_INTR_MASK for the details of bit fields.
GPIO_PRT23_INTR_MASKED	0x40310B9C	Port interrupt masked status register. See GPIO_PRT6_INTR_MASKED for the details of bit fields.
GPIO_PRT23_INTR_SET	0x40310BA0	Port interrupt set register. See GPIO_PRT6_INTR_SET for the details of bit fields.

Register name	Address	Description
GPIO_PRT23_INTR_CFG	0x40310BC0	Port interrupt configuration register. See GPIO_PRT6_INTR_CFG for the details of bit fields.
GPIO_PRT23_CFG	0x40310BC4	Port configuration register. See GPIO_PRT6_CFG for the details of bit fields.
GPIO_PRT23_CFG_IN	0x40310BC8	Port input buffer configuration register. See GPIO_PRT6_CFG_IN for the details of bit fields.
GPIO_PRT23_CFG_OUT	0x40310BCC	Port output buffer configuration register. See GPIO_PRT6_CFG_OUT for the details of bit fields.
GPIO_PRT23_CFG_IN_AUTOLVL	0x40310BD8	Port input buffer AUTOLVL configuration register. See GPIO_PRT6_CFG_IN_AUTOLVL for the details of bit fields.
GPIO_INTR_CAUSE0	0x40314000	Interrupt port cause register 0
GPIO_VDD_ACTIVE	0x40314010	Extern power supply detection register
GPIO_VDD_INTR	0x40314014	Supply detection interrupt register
GPIO_VDD_INTR_MASK	0x40314018	Supply detection interrupt mask register
GPIO_VDD_INTR_MASKED	0x4031401C	Supply detection interrupt masked register
GPIO_VDD_INTR_SET	0x40314020	Supply detection interrupt set register
SMARTIO_PRT12_CTL	0x40320C00	Control register
SMARTIO_PRT12_SYNC_CTL	0x40320C10	Synchronization control register
SMARTIO_PRT12_LUT_SEL0	0x40320C20	LUT component input selection
SMARTIO_PRT12_LUT_SEL1	0x40320C24	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT12_LUT_SEL2	0x40320C28	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT12_LUT_SEL3	0x40320C2C	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT12_LUT_SEL4	0x40320C30	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT12_LUT_SEL5	0x40320C34	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT12_LUT_SEL6	0x40320C38	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT12_LUT_SEL7	0x40320C3C	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT12_LUT_CTL0	0x40320C40	LUT component control register
SMARTIO_PRT12_LUT_CTL1	0x40320C44	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.

Register name	Address	Description
SMARTIO_PRT12_LUT_CTL2	0x40320C48	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT12_LUT_CTL3	0x40320C4C	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT12_LUT_CTL4	0x40320C50	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT12_LUT_CTL5	0x40320C54	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT12_LUT_CTL6	0x40320C58	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT12_LUT_CTL7	0x40320C5C	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT12_DU_SEL	0x40320CC0	Data unit component input selection
SMARTIO_PRT12_DU_CTL	0x40320CC4	Data unit component control register
SMARTIO_PRT12_DATA	0x40320CF0	Data register
SMARTIO_PRT13_CTL	0x40320D00	Control register. See SMARTIO_PRT12_CTL for the details of bit fields.
SMARTIO_PRT13_SYNC_CTL	0x40320D10	Synchronization control register. See SMARTIO_PRT12_SYNC_CTL for the details of bit fields.
SMARTIO_PRT13_LUT_SEL0	0x40320D20	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT13_LUT_SEL1	0x40320D24	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT13_LUT_SEL2	0x40320D28	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT13_LUT_SEL3	0x40320D2C	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT13_LUT_SEL4	0x40320D30	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT13_LUT_SEL5	0x40320D34	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT13_LUT_SEL6	0x40320D38	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.

Register name	Address	Description
SMARTIO_PRT13_LUT_SEL7	0x40320D3C	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT13_LUT_CTL0	0x40320D40	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT13_LUT_CTL1	0x40320D44	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT13_LUT_CTL2	0x40320D48	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT13_LUT_CTL3	0x40320D4C	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT13_LUT_CTL4	0x40320D50	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT13_LUT_CTL5	0x40320D54	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT13_LUT_CTL6	0x40320D58	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT13_LUT_CTL7	0x40320D5C	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT13_DU_SEL	0x40320DC0	Data unit component input selection. See SMARTIO_PRT12_DU_SEL for the details of bit fields.
SMARTIO_PRT13_DU_CTL	0x40320DC4	Data unit component control register. See SMARTIO_PRT12_DU_CTL for the details of bit fields.
SMARTIO_PRT13_DATA	0x40320DF0	Data register. See SMARTIO_PRT12_DATA for the details of bit fields.
SMARTIO_PRT14_CTL	0x40320E00	Control register. See SMARTIO_PRT12_CTL for the details of bit fields.
SMARTIO_PRT14_SYNC_CTL	0x40320E10	Synchronization control register. See SMARTIO_PRT12_SYNC_CTL for the details of bit fields.
SMARTIO_PRT14_LUT_SEL0	0x40320E20	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT14_LUT_SEL1	0x40320E24	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT14_LUT_SEL2	0x40320E28	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.

Register name	Address	Description
SMARTIO_PRT14_LUT_SEL3	0x40320E2C	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT14_LUT_SEL4	0x40320E30	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT14_LUT_SEL5	0x40320E34	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT14_LUT_SEL6	0x40320E38	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT14_LUT_SEL7	0x40320E3C	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT14_LUT_CTL0	0x40320E40	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT14_LUT_CTL1	0x40320E44	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT14_LUT_CTL2	0x40320E48	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT14_LUT_CTL3	0x40320E4C	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT14_LUT_CTL4	0x40320E50	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT14_LUT_CTL5	0x40320E54	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT14_LUT_CTL6	0x40320E58	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT14_LUT_CTL7	0x40320E5C	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT14_DU_SEL	0x40320EC0	Data unit component input selection. See SMARTIO_PRT12_DU_SEL for the details of bit fields.
SMARTIO_PRT14_DU_CTL	0x40320EC4	Data unit component control register. See SMARTIO_PRT12_DU_CTL for the details of bit fields.
SMARTIO_PRT14_DATA	0x40320EF0	Data register. See SMARTIO_PRT12_DATA for the details of bit fields.
SMARTIO_PRT15_CTL	0x40320F00	Control register. See SMARTIO_PRT12_CTL for the details of bit fields.

Register name	Address	Description
SMARTIO_PRT15_SYNC_CTL	0x40320F10	Synchronization control register. See SMARTIO_PRT12_SYNC_CTL for the details of bit fields.
SMARTIO_PRT15_LUT_SEL0	0x40320F20	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT15_LUT_SEL1	0x40320F24	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT15_LUT_SEL2	0x40320F28	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT15_LUT_SEL3	0x40320F2C	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT15_LUT_SEL4	0x40320F30	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT15_LUT_SEL5	0x40320F34	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT15_LUT_SEL6	0x40320F38	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT15_LUT_SEL7	0x40320F3C	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT15_LUT_CTL0	0x40320F40	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT15_LUT_CTL1	0x40320F44	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT15_LUT_CTL2	0x40320F48	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT15_LUT_CTL3	0x40320F4C	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT15_LUT_CTL4	0x40320F50	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT15_LUT_CTL5	0x40320F54	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT15_LUT_CTL6	0x40320F58	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.

Register name	Address	Description
SMARTIO_PRT15_LUT_CTL7	0x40320F5C	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT15_DU_SEL	0x40320FC0	Data unit component input selection. See SMARTIO_PRT12_DU_SEL for the details of bit fields.
SMARTIO_PRT15_DU_CTL	0x40320FC4	Data unit component control register. See SMARTIO_PRT12_DU_CTL for the details of bit fields.
SMARTIO_PRT15_DATA	0x40320FF0	Data register. See SMARTIO_PRT12_DATA for the details of bit fields.
SMARTIO_PRT17_CTL	0x40321100	Control register. See SMARTIO_PRT12_CTL for the details of bit fields.
SMARTIO_PRT17_SYNC_CTL	0x40321110	Synchronization control register. See SMARTIO_PRT12_SYNC_CTL for the details of bit fields.
SMARTIO_PRT17_LUT_SEL0	0x40321120	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT17_LUT_SEL1	0x40321124	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT17_LUT_SEL2	0x40321128	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT17_LUT_SEL3	0x4032112C	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT17_LUT_SEL4	0x40321130	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT17_LUT_SEL5	0x40321134	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT17_LUT_SEL6	0x40321138	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT17_LUT_SEL7	0x4032113C	LUT component input selection. See SMARTIO_PRT12_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT17_LUT_CTL0	0x40321140	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT17_LUT_CTL1	0x40321144	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT17_LUT_CTL2	0x40321148	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.

Register name	Address	Description
SMARTIO_PRT17_LUT_CTL3	0x4032114C	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT17_LUT_CTL4	0x40321150	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT17_LUT_CTL5	0x40321154	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT17_LUT_CTL6	0x40321158	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT17_LUT_CTL7	0x4032115C	LUT component control register. See SMARTIO_PRT12_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT17_DU_SEL	0x403211C0	Data unit component input selection. See SMARTIO_PRT12_DU_SEL for the details of bit fields.
SMARTIO_PRT17_DU_CTL	0x403211C4	Data unit component control register. See SMARTIO_PRT12_DU_CTL for the details of bit fields.
SMARTIO_PRT17_DATA	0x403211F0	Data register. See SMARTIO_PRT12_DATA for the details of bit fields.

11.1 IO subsystem registers

HSIOM_PRT0_PORT_SEL0

Port selection 0
Address: 0x40300000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			RW				
Name	None [7:5]			IO0_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			RW				
Name	None [15:13]			IO1_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			RW				
Name	None [23:21]			IO2_SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				

Bits	31	30	29	28	27	26	25	24
HW Access	None			RW				
Name	None [31:29]			IO3_SEL [28:24]				

Bits	Name	Description
28 : 24	IO3_SEL	Selects the peripheral connections of Pin 3. Default Value: 0
20 : 16	IO2_SEL	Selects the peripheral connections of Pin 2. Default Value: 0
12 : 8	IO1_SEL	Selects the peripheral connections of Pin 1. Default Value: 0
4 : 0	IO0_SEL	Selects the peripheral connections of Pin 0. Note that available connectivity options vary depending on the device, port and the pin. See the device Datasheet for a list of peripheral connections available at each pin. Default Value: 0
		0x0: GPIO : GPIO controls "out"
		0x1: GPIO_DSI : GPIO controls "out", DSI controls "output enable"
		0x2: DSI_DSI : DSI controls "out" and "output enable"
		0x3: DSI_GPIO : DSI controls "out", GPIO controls "output enable"
		0x4: AMUXA : AMUXBUS A
		0x5: AMUXB : AMUXBUS B
		0x6: AMUXA_DSI : Analog mux bus A, DSI control
		0x7: AMUXB_DSI : Analog mux bus B, DSI control
		0x8: ACT_0 : Active peripheral 0
		0x9: ACT_1 : Active peripheral 1
		0xa: ACT_2 : Active peripheral 2
		0xb: ACT_3 : Active peripheral 3
		0xc: DS_0 : Deep Sleep peripheral 0
		0xd: DS_1 : Deep Sleep peripheral 1
		0xe: DS_2 : Deep Sleep peripheral 2
		0xf: DS_3 : Deep Sleep peripheral 3
		0x10: ACT_4 : Active peripheral 4
		0x11: ACT_5 : Active peripheral 5
		0x12: ACT_6 : Active peripheral 6
		0x13: ACT_7 : Active peripheral 7
		0x14: ACT_8 : Active peripheral 8

		0x15: ACT_9 : Active peripheral 9
		0x16: ACT_10 : Active peripheral 10
		0x17: ACT_11 : Active peripheral 11
		0x18: ACT_12 : Active peripheral 12
		0x19: ACT_13 : Active peripheral 13
		0x1a: ACT_14 : Active peripheral 14
		0x1b: ACT_15 : Active peripheral 15
		0x1c: DS_4 : Deep Sleep peripheral 4
		0x1d: DS_5 : Deep Sleep peripheral 5
		0x1e: DS_6 : Deep Sleep peripheral 6
		0x1f: DS_7 : Deep Sleep peripheral 7

HSIOM_PRT2_PORT_SEL1

Port selection 1
Address: 0x40300024
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			RW				
Name	None [7:5]			IO4_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			RW				
Name	None [15:13]			IO5_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12 : 8	IO5_SEL	Selects the peripheral connections of Pin 4. Default Value: 0
4 : 0	IO4_SEL	Selects the peripheral connections of Pin 4. See PORT_SEL0 for connection details. Default Value: 0

HSIOM_PRT4_PORT_SEL1

Port selection 1
Address: 0x40300044
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			RW				
Name	None [7:5]			IO4_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	IO4_SEL	Selects the peripheral connections of Pin 4. See PORT_SEL0 for connection details. Default Value: 0

HSIOM_PRT6_PORT_SEL1

Port selection 1
Address: 0x40300064
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			RW				
Name	None [7:5]			IO4_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			RW				
Name	None [15:13]			IO5_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			RW				
Name	None [23:21]			IO6_SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			RW				
Name	None [31:29]			IO7_SEL [28:24]				

Bits	Name	Description
28 : 24	IO7_SEL	Selects the peripheral connections of Pin 6. Default Value: 0
20 : 16	IO6_SEL	Selects the peripheral connections of Pin 5. Default Value: 0
12 : 8	IO5_SEL	Selects the peripheral connections of Pin 4. Default Value: 0
4 : 0	IO4_SEL	Selects the peripheral connections of Pin 4. See PORT_SEL0 for connection details. Default Value: 0

HSIOM_PRT11_PORT_SEL0

Port selection 0
Address: 0x403000B0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			RW				
Name	None [7:5]			IO0_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			RW				
Name	None [15:13]			IO1_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			RW				
Name	None [23:21]			IO2_SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 16	IO2_SEL	Selects the peripheral connections of Pin 2. Default Value: 0
12 : 8	IO1_SEL	Selects the peripheral connections of Pin 1. Default Value: 0
4 : 0	IO0_SEL	Selects the peripheral connections of Pin 0. Note that available connectivity options vary depending on the device, port and the pin. See the device Datasheet for a list of peripheral connections available at each pin. Default Value: 0
		0x0: GPIO : GPIO controls "out"
		0x1: GPIO_DSI : GPIO controls "out", DSI controls "output enable"
		0x2: DSI_DSI : DSI controls "out" and "output enable"
		0x3: DSI_GPIO : DSI controls "out", GPIO controls "output enable"
		0x4: AMUXA : AMUXBUS A
		0x5: AMUXB : AMUXBUS B

		0x6: AMUXA_DSI : Analog mux bus A, DSI control
		0x7: AMUXB_DSI : Analog mux bus B, DSI control
		0x8: ACT_0 : Active peripheral 0
		0x9: ACT_1 : Active peripheral 1
		0xa: ACT_2 : Active peripheral 2
		0xb: ACT_3 : Active peripheral 3
		0xc: DS_0 : Deep Sleep peripheral 0
		0xd: DS_1 : Deep Sleep peripheral 1
		0xe: DS_2 : Deep Sleep peripheral 2
		0xf: DS_3 : Deep Sleep peripheral 3
		0x10: ACT_4 : Active peripheral 4
		0x11: ACT_5 : Active peripheral 5
		0x12: ACT_6 : Active peripheral 6
		0x13: ACT_7 : Active peripheral 7
		0x14: ACT_8 : Active peripheral 8
		0x15: ACT_9 : Active peripheral 9
		0x16: ACT_10 : Active peripheral 10
		0x17: ACT_11 : Active peripheral 11
		0x18: ACT_12 : Active peripheral 12
		0x19: ACT_13 : Active peripheral 13
		0x1a: ACT_14 : Active peripheral 14
		0x1b: ACT_15 : Active peripheral 15
		0x1c: DS_4 : Deep Sleep peripheral 4
		0x1d: DS_5 : Deep Sleep peripheral 5
		0x1e: DS_6 : Deep Sleep peripheral 6
		0x1f: DS_7 : Deep Sleep peripheral 7

HSIOM_AMUX_SPLIT_CTL0

AMUX splitter cell control
Address: 0x40302000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW	RW	RW
HW Access	None	R	R	R	None	R	R	R
Name	None	SWITCH_BB_S0	SWITCH_BB_SR	SWITCH_BB_SL	None	SWITCH_AA_S0	SWITCH_AA_SR	SWITCH_AA_SL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6	SWITCH_BB_S0	T-switch control for AMUXBUSB vssa/ground switch. Default Value: 0
5	SWITCH_BB_SR	T-switch control for Right AMUXBUSB switch. Default Value: 0
4	SWITCH_BB_SL	T-switch control for Left AMUXBUSB switch. Default Value: 0
2	SWITCH_AA_S0	T-switch control for AMUXBUSA vssa/ground switch: '0': switch open. '1': switch closed. Default Value: 0
1	SWITCH_AA_SR	T-switch control for Right AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0
0	SWITCH_AA_SL	T-switch control for Left AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

HSIOM_MONITOR_CTL_0

Power/Ground Monitor cell control 0
Address: 0x40302200
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MONITOR_EN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MONITOR_EN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			MONITOR_EN [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 0	MONITOR_EN	control for switch, which connects the power/ground supply to AMUXBUS_A/B respectively when switch is closed: '0': switch open. '1': switch closed. Default Value: 0

HSIOM_ALT_JTAG_EN

Alternate JTAG IF selection register
Address: 0x40302240
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Provides the selection for alternate JTAG IF connectivity. 0: Primary JTAG interface is selected 1: Secondary (alternate) JTAG interface is selected. This connectivity works ONLY in ACTIVE mode. Default Value: 0

GPIO_PRT0_OUT

Port output data register
Address: 0x40310000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	OUT3	IO output data for pin 3 Default Value: 0
2	OUT2	IO output data for pin 2 Default Value: 0
1	OUT1	IO output data for pin 1 Default Value: 0
0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

GPIO_PRT0_OUT_CLR

Port output data clear register
Address: 0x40310004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	A	A	A	A	A	A	A	A
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	OUT7	IO clear output for pin 7 Default Value: 0
6	OUT6	IO clear output for pin 6 Default Value: 0
5	OUT5	IO clear output for pin 5 Default Value: 0
4	OUT4	IO clear output for pin 4 Default Value: 0
3	OUT3	IO clear output for pin 3 Default Value: 0
2	OUT2	IO clear output for pin 2 Default Value: 0
1	OUT1	IO clear output for pin 1 Default Value: 0
0	OUT0	IO clear output for pin 0: '0': Output state not affected. '1': Output state set to '0'. Default Value: 0

GPIO_PRT0_OUT_SET

Port output data set register
Address: 0x40310008
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	A	A	A	A	A	A	A	A
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	OUT7	IO set output for pin 7 Default Value: 0
6	OUT6	IO set output for pin 6 Default Value: 0
5	OUT5	IO set output for pin 5 Default Value: 0
4	OUT4	IO set output for pin 4 Default Value: 0
3	OUT3	IO set output for pin 3 Default Value: 0
2	OUT2	IO set output for pin 2 Default Value: 0
1	OUT1	IO set output for pin 1 Default Value: 0
0	OUT0	IO set output for pin 0: '0': Output state not affected. '1': Output state set to '1'. Default Value: 0

GPIO_PRT0_OUT_INV

Port output data invert register
Address: 0x4031000C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	A	A	A	A	A	A	A	A
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	OUT7	IO invert output for pin 7 Default Value: 0
6	OUT6	IO invert output for pin 6 Default Value: 0
5	OUT5	IO invert output for pin 5 Default Value: 0
4	OUT4	IO invert output for pin 4 Default Value: 0
3	OUT3	IO invert output for pin 3 Default Value: 0
2	OUT2	IO invert output for pin 2 Default Value: 0
1	OUT1	IO invert output for pin 1 Default Value: 0
0	OUT0	IO invert output for pin 0: '0': Output state not affected. '1': Output state inverted ('0' => '1', '1' => '0'). Default Value: 0

GPIO_PRT0_IN

Port input state register
Address: 0x40310010
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				IN3	IN2	IN1	IN0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the INTR_CFG.FLT_SEL register. Default Value: 0
3	IN3	IO pin state for pin 3 Default Value: 0
2	IN2	IO pin state for pin 2 Default Value: 0
1	IN1	IO pin state for pin 1 Default Value: 0
0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. On reset assertion , IN register will get reset. The Pad value takes 2 clock cycles to be reflected into IN Register. It's value then depends on the external pin value. Default Value: 0

GPIO_PRT0_INTR

Port interrupt status register
Address: 0x40310014
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [23:20]				IN_IN3	IN_IN2	IN_IN1	IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
19	IN_IN3	IO pin state for pin 3 Default Value: 0
18	IN_IN2	IO pin state for pin 2 Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0
16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
3	EDGE3	Edge detect for IO pin 3 Default Value: 0
2	EDGE2	Edge detect for IO pin 2 Default Value: 0
1	EDGE1	Edge detect for IO pin 1 Default Value: 0

0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

GPIO_PRT0_INTR_MASK

Port interrupt mask register
Address: 0x40310018
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
3	EDGE3	Masks edge interrupt on IO pin 3 Default Value: 0
2	EDGE2	Masks edge interrupt on IO pin 2 Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0
0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

GPIO_PRT0_INTR_MASKED

Port interrupt masked status register
Address: 0x4031001C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
3	EDGE3	Edge detected and masked on IO pin 3 Default Value: 0
2	EDGE2	Edge detected and masked on IO pin 2 Default Value: 0
1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0
0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

GPIO_PRT0_INTR_SET

Port interrupt set register
Address: 0x40310020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [7:4]				EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
3	EDGE3	Sets edge detect interrupt for IO pin 3 Default Value: 0
2	EDGE2	Sets edge detect interrupt for IO pin 2 Default Value: 0
1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0
0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

GPIO_PRT0_INTR_CFG

Port interrupt configuration register
Address: 0x40310040
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0
		0x0: DISABLE : Disabled
		0x1: RISING : Rising edge
		0x2: FALLING : Falling edge
		0x3: BOTH : Both rising and falling edges
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pin 3 Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pin 2 Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0

		0x0: DISABLE : Disabled
		0x1: RISING : Rising edge
		0x2: FALLING : Falling edge
		0x3: BOTH : Both rising and falling edges

GPIO_PRT0_CFG

Port configuration register
Address: 0x40310044
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN3	DRIVE_MODE3 [14:12]			IN_EN2	DRIVE_MODE2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	DRIVE_MODE5 [22:20]			None	DRIVE_MODE4 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	DRIVE_MODE7 [30:28]			None	DRIVE_MODE6 [26:24]		

Bits	Name	Description
30 : 28	DRIVE_MODE7	The GPIO drive mode for IO pin 7. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
26 : 24	DRIVE_MODE6	The GPIO drive mode for IO pin 6. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance

		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down
		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up

22 : 20	DRIVE_MODE5	The GPIO drive mode for IO pin 5. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up

		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down
		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
18 : 16	DRIVE_MODE4	The GPIO drive mode for IO pin 4. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
15	IN_EN3	Enables the input buffer for IO pin 3 Default Value: 0
14 : 12	DRIVE_MODE3	The GPIO drive mode for IO pin 3. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
11	IN_EN2	Enables the input buffer for IO pin 2 Default Value: 0
10 : 8	DRIVE_MODE2	The GPIO drive mode for IO pin 2. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0
2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up

GPIO_PRT0_CFG_IN

Port input buffer configuration register
Address: 0x40310048
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				VTRIP_SEL3_0	VTRIP_SEL2_0	VTRIP_SEL1_0	VTRIP_SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	VTRIP_SEL3_0	Configures the pin 3 input buffer mode (trip points and hysteresis) Default Value: 0
2	VTRIP_SEL2_0	Configures the pin 2 input buffer mode (trip points and hysteresis) Default Value: 0
1	VTRIP_SEL1_0	Configures the pin 1 input buffer mode (trip points and hysteresis) Default Value: 0
0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0
		0x0: CMOS : PSOC™ 6:: Input buffer compatible with CMOS and I2C interfaces XMC5000: Full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1

		0x1: TTL : PSOC™ 6:: Input buffer compatible with TTL and MediaLB interfaces XMC5000: full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1

GPIO_PRT0_CFG_OUT

Port output buffer configuration register
Address: 0x4031004C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				SLOW3	SLOW2	SLOW1	SLOW0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL3 [23:22]		DRIVE_SEL2 [21:20]		DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 22	DRIVE_SEL3	Sets the GPIO drive strength for IO pin 3 Default Value: 0
21 : 20	DRIVE_SEL2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
17 : 16	DRIVE_SEL0	Documentation: Note: DRIVE_SELx are used among GPIO cells and HSIO_STD but the encoding values may differ as shown on the right side of this table Default Value: 0
		0x0: DRIVE_SEL_ZERO : XMC5000: GPIO_STD/GPIO_ENH: Full drive strengh: GPIO drives current at its max rated spec. XMC5000:_GPIO_SMC: GPIO_SMC default mode. XMC5000:_HSIO_STD: HSIO default mode. PSOC™ 6: GPIO cells and HSIO_STD cells: Full drive strength: GPIO drives current at its max rated spec.

		0x1: DRIVE_SEL_ONE : XMC5000: GPIO_STD/GPIO_ENH: Full drive strengh: GPIO drives current at its max rated spec. XMC5000:_GPIO_SMC: GPIO full drive strength. XMC5000:_HSIO_STD: GPIO full drive strength. PSOC™ 6: GPIO cells and HSIO_STD cells: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec
		0x2: DRIVE_SEL_TWO : XMC5000: GPIO_STD/GPIO_ENH: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec. XMC5000:_GPIO_SMC: GPIO 1/2 drive strength. XMC5000:_HSIO_STD: GPIO 1/2 drive strength. PSoC 6: GPIO cells and HSIO_STD cells: 1/4 drive strength. GPIO drives current at 1/4 of its max rated spec.
		0x3: DRIVE_SEL_THREE : XMC5000: GPIO_STD/GPIO_ENH: 1/4 drive strength: GPIO drives current at 1/4 of its max rated spec. XMC5000:_GPIO_SMC: GPIO 1/4 drive strength. XMC5000:_HSIO_STD: GPIO 1/4 drive strength. PSoC 6: GPIO cells and HSIO_STD cells: 1/8 drive strength. GPIO drives current at 1/8 of its max rated spec.
3	SLOW3	Enables slow slew rate for IO pin 3 Default Value: 0
2	SLOW2	Enables slow slew rate for IO pin 2 Default Value: 0
1	SLOW1	Enables slow slew rate for IO pin 1 Default Value: 0
0	SLOW0	Enables slow slew rate for IO pin 0 '0': Fast slew rate '1': Slow slew rate Default Value: 0

GPIO_PRT0_CFG_IN_AUTOLVL

Port input buffer AUTOLVL configuration register
Address: 0x40310058
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				VTRIP_SEL3_1	VTRIP_SEL2_1	VTRIP_SEL1_1	VTRIP_SEL0_1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	VTRIP_SEL3_1	Input buffer compatible with automotive (elevated Vil) interfaces. Default Value: 0
2	VTRIP_SEL2_1	Input buffer compatible with automotive (elevated Vil) interfaces. Default Value: 0
1	VTRIP_SEL1_1	Input buffer compatible with automotive (elevated Vil) interfaces. Default Value: 0
0	VTRIP_SEL0_1	Configures the input buffer mode (trip points and hysteresis) for GPIO upper bit. Lower bit is still selected by CFG_IN.VTRIP_SEL0_0 field. This field is used along with CFG_IN.VTRIP_SEL0_0 field as below: {CFG_IN_AUTOLVL.VTRIP_SEL0_1,CFG_IN.VTRIP_SEL0_0}: 0,0: CMOS 0,1: TTL 1,0: input buffer is compatible with automotive. 1,1: input buffer is compatible with automotvie Default Value: 0

		0x0: CMOS_OR_TTL : Input buffer compatible with CMOS/TTL interfaces as described in CFG_IN.VTRIP_SEL0_0.
		0x1: AUTO : Input buffer compatible with AUTO (elevated Vil) interfaces when used along with CFG_IN.VTRIP_SEL0_0.

GPIO_PRT1_CFG_OUT

Port output buffer configuration register
Address: 0x403100CC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL3 [23:22]		DRIVE_SEL2 [21:20]		DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 22	DRIVE_SEL3	Sets the GPIO drive strength for IO pin 3 Default Value: 0
21 : 20	DRIVE_SEL2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
17 : 16	DRIVE_SEL0	Documentation: Note: DRIVE_SELx are used among GPIO cells and HSIO_STD but the encoding values may differ as shown on the right side of this table Default Value: 0
		0x0: DRIVE_SEL_ZERO : XMC5000: GPIO_STD/GPIO_ENH: Full drive strengh: GPIO drives current at its max rated spec. XMC5000:_GPIO_SMC: GPIO_SMC default mode. XMC5000:_HSIO_STD: HSIO default mode. PSOC™ 6: GPIO cells and HSIO_STD cells: Full drive strength: GPIO drives current at its max rated spec.

		0x1: DRIVE_SEL_ONE : XMC5000: GPIO_STD/GPIO_ENH: Full drive strengh: GPIO drives current at its max rated spec. XMC5000:_GPIO_SMC: GPIO full drive strength. XMC5000:_HSIO_STD: GPIO full drive strength. PSOC™ 6: GPIO cells and HSIO_STD cells: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec
		0x2: DRIVE_SEL_TWO : XMC5000: GPIO_STD/GPIO_ENH: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec. XMC5000:_GPIO_SMC: GPIO 1/2 drive strength. XMC5000:_HSIO_STD: GPIO 1/2 drive strength. PSOC™ 6: GPIO cells and HSIO_STD cells: 1/4 drive strength. GPIO drives current at 1/4 of its max rated spec.
		0x3: DRIVE_SEL_THREE : XMC5000: GPIO_STD/GPIO_ENH: 1/4 drive strength: GPIO drives current at 1/4 of its max rated spec. XMC5000:_GPIO_SMC: GPIO 1/4 drive strength. XMC5000:_HSIO_STD: GPIO 1/4 drive strength. PSOC™ 6: GPIO cells and HSIO_STD cells: 1/8 drive strength. GPIO drives current at 1/8 of its max rated spec.

GPIO_PRT2_OUT

Port output data register
Address: 0x40310100
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	OUT5	IO output data for pin 5 Default Value: 0
4	OUT4	IO output data for pin 4 Default Value: 0
3	OUT3	IO output data for pin 3 Default Value: 0
2	OUT2	IO output data for pin 2 Default Value: 0
1	OUT1	IO output data for pin 1 Default Value: 0
0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

GPIO_PRT2_IN

Port input state register
Address: 0x40310110
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		IN5	IN4	IN3	IN2	IN1	IN0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the INTR_CFG.FLT_SEL register. Default Value: 0
5	IN5	IO pin state for pin 5 Default Value: 0
4	IN4	IO pin state for pin 4 Default Value: 0
3	IN3	IO pin state for pin 3 Default Value: 0
2	IN2	IO pin state for pin 2 Default Value: 0
1	IN1	IO pin state for pin 1 Default Value: 0
0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. On reset assertion , IN register will get reset. The Pad value takes 2 clock cycles to be reflected into IN Register. It's value then depends on the external pin value. Default Value: 0

GPIO_PRT2_INTR

Port interrupt status register
Address: 0x40310114
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None		A	A	A	A	A	A
Name	None [7:6]		EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [23:22]		IN_IN5	IN_IN4	IN_IN3	IN_IN2	IN_IN1	IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
21	IN_IN5	IO pin state for pin 5 Default Value: 0
20	IN_IN4	IO pin state for pin 4 Default Value: 0
19	IN_IN3	IO pin state for pin 3 Default Value: 0
18	IN_IN2	IO pin state for pin 2 Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0
16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
5	EDGE5	Edge detect for IO pin 5 Default Value: 0
4	EDGE4	Edge detect for IO pin 4 Default Value: 0

3	EDGE3	Edge detect for IO pin 3 Default Value: 0
2	EDGE2	Edge detect for IO pin 2 Default Value: 0
1	EDGE1	Edge detect for IO pin 1 Default Value: 0
0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

GPIO_PRT2_INTR_MASK

Port interrupt mask register
Address: 0x40310118
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
5	EDGE5	Masks edge interrupt on IO pin 5 Default Value: 0
4	EDGE4	Masks edge interrupt on IO pin 4 Default Value: 0
3	EDGE3	Masks edge interrupt on IO pin 3 Default Value: 0
2	EDGE2	Masks edge interrupt on IO pin 2 Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0
0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

GPIO_PRT2_INTR_MASKED

Port interrupt masked status register
Address: 0x4031011C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
5	EDGE5	Edge detected and masked on IO pin 5 Default Value: 0
4	EDGE4	Edge detected and masked on IO pin 4 Default Value: 0
3	EDGE3	Edge detected and masked on IO pin 3 Default Value: 0
2	EDGE2	Edge detected and masked on IO pin 2 Default Value: 0
1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0
0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

GPIO_PRT2_INTR_SET

Port interrupt set register
Address: 0x40310120
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	None		A	A	A	A	A	A
Name	None [7:6]		EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
5	EDGE5	Sets edge detect interrupt for IO pin 5 Default Value: 0
4	EDGE4	Sets edge detect interrupt for IO pin 4 Default Value: 0
3	EDGE3	Sets edge detect interrupt for IO pin 3 Default Value: 0
2	EDGE2	Sets edge detect interrupt for IO pin 2 Default Value: 0
1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0
0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

GPIO_PRT2_INTR_CFG

Port interrupt configuration register
Address: 0x40310140
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [15:12]				EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0
		0x0: DISABLE : Disabled
		0x1: RISING : Rising edge
		0x2: FALLING : Falling edge
		0x3: BOTH : Both rising and falling edges
11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pin 5 Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pin 4 Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pin 3 Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pin 2 Default Value: 0

3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0
		0x0: DISABLE : Disabled
		0x1: RISING : Rising edge
		0x2: FALLING : Falling edge
		0x3: BOTH : Both rising and falling edges

GPIO_PRT2_CFG

Port configuration register
Address: 0x40310144
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN3	DRIVE_MODE3 [14:12]			IN_EN2	DRIVE_MODE2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN5	DRIVE_MODE5 [22:20]			IN_EN4	DRIVE_MODE4 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	DRIVE_MODE7 [30:28]			None	DRIVE_MODE6 [26:24]		

Bits	Name	Description
30 : 28	DRIVE_MODE7	The GPIO drive mode for IO pin 7. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
26 : 24	DRIVE_MODE6	The GPIO drive mode for IO pin 6. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance

		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down
		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
23	IN_EN5	Enables the input buffer for IO pin 5 Default Value: 0

22 : 20	DRIVE_MODE5	The GPIO drive mode for IO pin 5. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up

		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down
		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
19	IN_EN4	Enables the input buffer for IO pin 4 Default Value: 0
18 : 16	DRIVE_MODE4	The GPIO drive mode for IO pin 4. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
15	IN_EN3	Enables the input buffer for IO pin 3 Default Value: 0
14 : 12	DRIVE_MODE3	The GPIO drive mode for IO pin 3. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
11	IN_EN2	Enables the input buffer for IO pin 2 Default Value: 0
10 : 8	DRIVE_MODE2	The GPIO drive mode for IO pin 2. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0
2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up

GPIO_PRT2_CFG_IN

Port input buffer configuration register
Address: 0x40310148
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		VTRIP_SEL5_0	VTRIP_SEL4_0	VTRIP_SEL3_0	VTRIP_SEL2_0	VTRIP_SEL1_0	VTRIP_SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	VTRIP_SEL5_0	Configures the pin 5 input buffer mode (trip points and hysteresis) Default Value: 0
4	VTRIP_SEL4_0	Configures the pin 4 input buffer mode (trip points and hysteresis) Default Value: 0
3	VTRIP_SEL3_0	Configures the pin 3 input buffer mode (trip points and hysteresis) Default Value: 0
2	VTRIP_SEL2_0	Configures the pin 2 input buffer mode (trip points and hysteresis) Default Value: 0
1	VTRIP_SEL1_0	Configures the pin 1 input buffer mode (trip points and hysteresis) Default Value: 0
0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0

		0x0: CMOS : PSOC™ 6:: Input buffer compatible with CMOS and I2C interfaces XMC5000: Full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1
		0x1: TTL : PSOC™ 6:: Input buffer compatible with TTL and MediaLB interfaces XMC5000: full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1

GPIO_PRT2_CFG_OUT

Port output buffer configuration register
Address: 0x4031014C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL3 [23:22]		DRIVE_SEL2 [21:20]		DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [31:28]				DRIVE_SEL5 [27:26]		DRIVE_SEL4 [25:24]	

Bits	Name	Description
27 : 26	DRIVE_SEL5	Sets the GPIO drive strength for IO pin 5 Default Value: 0
25 : 24	DRIVE_SEL4	Sets the GPIO drive strength for IO pin 4 Default Value: 0
23 : 22	DRIVE_SEL3	Sets the GPIO drive strength for IO pin 3 Default Value: 0
21 : 20	DRIVE_SEL2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
17 : 16	DRIVE_SEL0	Documentation: Note: DRIVE_SELx are used among GPIO cells and HSIO_STD but the encoding values may differ as shown on the right side of this table Default Value: 0

		0x0: DRIVE_SEL_ZERO : XMC5000: GPIO_STD/GPIO_ENH: Full drive strengh: GPIO drives current at its max rated spec. XMC5000:_GPIO_SMC: GPIO_SMC default mode. XMC5000:_HSIO_STD: HSIO default mode. PSOC™ 6: GPIO cells and HSIO_STD cells: Full drive strength: GPIO drives current at its max rated spec.
		0x1: DRIVE_SEL_ONE : XMC5000: GPIO_STD/GPIO_ENH: Full drive strengh: GPIO drives current at its max rated spec. XMC5000:_GPIO_SMC: GPIO full drive strength. XMC5000:_HSIO_STD: GPIO full drive strength. PSOC™ 6: GPIO cells and HSIO_STD cells: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec
		0x2: DRIVE_SEL_TWO : XMC5000: GPIO_STD/GPIO_ENH: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec. XMC5000:_GPIO_SMC: GPIO 1/2 drive strength. XMC5000:_HSIO_STD: GPIO 1/2 drive strength. PSOC™ 6: GPIO cells and HSIO_STD cells: 1/4 drive strength. GPIO drives current at 1/4 of its max rated spec.
		0x3: DRIVE_SEL_THREE : XMC5000: GPIO_STD/GPIO_ENH: 1/4 drive strength: GPIO drives current at 1/4 of its max rated spec. XMC5000:_GPIO_SMC: GPIO 1/4 drive strength. XMC5000:_HSIO_STD: GPIO 1/4 drive strength. PSOC™ 6: GPIO cells and HSIO_STD cells: 1/8 drive strength. GPIO drives current at 1/8 of its max rated spec.

GPIO_PRT2_CFG_IN_AUTOLVL

Port input buffer AUTOLVL configuration register
Address: 0x40310158
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		VTRIP_SEL5_1	VTRIP_SEL4_1	VTRIP_SEL3_1	VTRIP_SEL2_1	VTRIP_SEL1_1	VTRIP_SEL0_1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	VTRIP_SEL5_1	Input buffer compatible with automotive (elevated Vil) interfaces. Default Value: 0
4	VTRIP_SEL4_1	Input buffer compatible with automotive (elevated Vil) interfaces. Default Value: 0
3	VTRIP_SEL3_1	Input buffer compatible with automotive (elevated Vil) interfaces. Default Value: 0
2	VTRIP_SEL2_1	Input buffer compatible with automotive (elevated Vil) interfaces. Default Value: 0
1	VTRIP_SEL1_1	Input buffer compatible with automotive (elevated Vil) interfaces. Default Value: 0

0	VTRIP_SEL0_1	Configures the input buffer mode (trip points and hysteresis) for GPIO upper bit. Lower bit is still selected by CFG_IN.VTRIP_SEL0_0 field. This field is used along with CFG_IN.VTRIP_SEL0_0 field as below: {CFG_IN_AUTOLVL.VTRIP_SEL0_1,CFG_IN.VTRIP_SEL0_0}: 0,0: CMOS 0,1: TTL 1,0: input buffer is compatible with automotive. 1,1: input buffer is compatible with automotvie Default Value: 0
		0x0: CMOS_OR_TTL : Input buffer compatible with CMOS/TTL interfaces as described in CFG_IN.VTRIP_SEL0_0.
		0x1: AUTO : Input buffer compatible with AUTO (elevated Vil) interfaces when used along with CFG_IN.VTRIP_SEL0_0.

GPIO_PRT4_OUT

Port output data register
Address: 0x40310200
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			RW	RW	RW	RW	RW
Name	None [7:5]			OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	OUT4	IO output data for pin 4 Default Value: 0
3	OUT3	IO output data for pin 3 Default Value: 0
2	OUT2	IO output data for pin 2 Default Value: 0
1	OUT1	IO output data for pin 1 Default Value: 0
0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

GPIO_PRT4_IN

Port input state register
Address: 0x40310210
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	R	R	R	R
HW Access	None			W	W	W	W	W
Name	None [7:5]			IN4	IN3	IN2	IN1	IN0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the INTR_CFG.FLT_SEL register. Default Value: 0
4	IN4	IO pin state for pin 4 Default Value: 0
3	IN3	IO pin state for pin 3 Default Value: 0
2	IN2	IO pin state for pin 2 Default Value: 0
1	IN1	IO pin state for pin 1 Default Value: 0
0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. On reset assertion , IN register will get reset. The Pad value takes 2 clock cycles to be reflected into IN Register. It's value then depends on the external pin value. Default Value: 0

GPIO_PRT4_INTR

Port interrupt status register
Address: 0x40310214
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None			A	A	A	A	A
Name	None [7:5]			EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None			R	R	R	R	R
HW Access	None			W	W	W	W	W
Name	None [23:21]			IN_IN4	IN_IN3	IN_IN2	IN_IN1	IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
20	IN_IN4	IO pin state for pin 4 Default Value: 0
19	IN_IN3	IO pin state for pin 3 Default Value: 0
18	IN_IN2	IO pin state for pin 2 Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0
16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
4	EDGE4	Edge detect for IO pin 4 Default Value: 0
3	EDGE3	Edge detect for IO pin 3 Default Value: 0
2	EDGE2	Edge detect for IO pin 2 Default Value: 0

1	EDGE1	Edge detect for IO pin 1 Default Value: 0
0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

GPIO_PRT4_INTR_MASK

Port interrupt mask register
Address: 0x40310218
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
4	EDGE4	Masks edge interrupt on IO pin 4 Default Value: 0
3	EDGE3	Masks edge interrupt on IO pin 3 Default Value: 0
2	EDGE2	Masks edge interrupt on IO pin 2 Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0
0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

GPIO_PRT4_INTR_MASKED

Port interrupt masked status register
Address: 0x4031021C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	R	R	R	R
HW Access	None			W	W	W	W	W
Name	None [7:5]			EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
4	EDGE4	Edge detected and masked on IO pin 4 Default Value: 0
3	EDGE3	Edge detected and masked on IO pin 3 Default Value: 0
2	EDGE2	Edge detected and masked on IO pin 2 Default Value: 0
1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0
0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

GPIO_PRT4_INTR_SET

Port interrupt set register
Address: 0x40310220
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	None			A	A	A	A	A
Name	None [7:5]			EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
4	EDGE4	Sets edge detect interrupt for IO pin 4 Default Value: 0
3	EDGE3	Sets edge detect interrupt for IO pin 3 Default Value: 0
2	EDGE2	Sets edge detect interrupt for IO pin 2 Default Value: 0
1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0
0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

GPIO_PRT4_INTR_CFG

Port interrupt configuration register
Address: 0x40310240
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0
		0x0: DISABLE : Disabled
		0x1: RISING : Rising edge
		0x2: FALLING : Falling edge
		0x3: BOTH : Both rising and falling edges
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pin 4 Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pin 3 Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pin 2 Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0

1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0
		0x0: DISABLE : Disabled
		0x1: RISING : Rising edge
		0x2: FALLING : Falling edge
		0x3: BOTH : Both rising and falling edges

GPIO_PRT4_CFG

Port configuration register
Address: 0x40310244
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN3	DRIVE_MODE3 [14:12]			IN_EN2	DRIVE_MODE2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW			RW	RW		
HW Access	None	R			R	R		
Name	None	DRIVE_MODE5 [22:20]			IN_EN4	DRIVE_MODE4 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	DRIVE_MODE7 [30:28]			None	DRIVE_MODE6 [26:24]		

Bits	Name	Description
30 : 28	DRIVE_MODE7	The GPIO drive mode for IO pin 7. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
26 : 24	DRIVE_MODE6	The GPIO drive mode for IO pin 6. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance

		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down
		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up

22 : 20	DRIVE_MODE5	The GPIO drive mode for IO pin 5. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up

		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down
		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
19	IN_EN4	Enables the input buffer for IO pin 4 Default Value: 0
18 : 16	DRIVE_MODE4	The GPIO drive mode for IO pin 4. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
15	IN_EN3	Enables the input buffer for IO pin 3 Default Value: 0
14 : 12	DRIVE_MODE3	The GPIO drive mode for IO pin 3. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
11	IN_EN2	Enables the input buffer for IO pin 2 Default Value: 0
10 : 8	DRIVE_MODE2	The GPIO drive mode for IO pin 2. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0
2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up

GPIO_PRT4_CFG_IN

Port input buffer configuration register
Address: 0x40310248
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			VTRIP_SEL4_0	VTRIP_SEL3_0	VTRIP_SEL2_0	VTRIP_SEL1_0	VTRIP_SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	VTRIP_SEL4_0	Configures the pin 4 input buffer mode (trip points and hysteresis) Default Value: 0
3	VTRIP_SEL3_0	Configures the pin 3 input buffer mode (trip points and hysteresis) Default Value: 0
2	VTRIP_SEL2_0	Configures the pin 2 input buffer mode (trip points and hysteresis) Default Value: 0
1	VTRIP_SEL1_0	Configures the pin 1 input buffer mode (trip points and hysteresis) Default Value: 0
0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0
		0x0: CMOS : PSOC™ 6:: Input buffer compatible with CMOS and I2C interfaces XMC5000: Full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1

		0x1: TTL : PSOC™ 6:: Input buffer compatible with TTL and MediaLB interfaces XMC5000: full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1

GPIO_PRT4_CFG_OUT

Port output buffer configuration register
Address: 0x4031024C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL3 [23:22]		DRIVE_SEL2 [21:20]		DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						DRIVE_SEL4 [25:24]	

Bits	Name	Description
25 : 24	DRIVE_SEL4	Sets the GPIO drive strength for IO pin 4 Default Value: 0
23 : 22	DRIVE_SEL3	Sets the GPIO drive strength for IO pin 3 Default Value: 0
21 : 20	DRIVE_SEL2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
17 : 16	DRIVE_SEL0	Documentation: Note: DRIVE_SELx are used among GPIO cells and HSIO_STD but the encoding values may differ as shown on the right side of this table Default Value: 0

		0x0: DRIVE_SEL_ZERO : XMC5000: GPIO_STD/GPIO_ENH: Full drive strengh: GPIO drives current at its max rated spec. XMC5000:_GPIO_SMC: GPIO_SMC default mode. XMC5000:_HSIO_STD: HSIO default mode. PSoC 6: GPIO cells and HSIO_STD cells: Full drive strength: GPIO drives current at its max rated spec.
		0x1: DRIVE_SEL_ONE : XMC5000: GPIO_STD/GPIO_ENH: Full drive strengh: GPIO drives current at its max rated spec. XMC5000:_GPIO_SMC: GPIO full drive strength. XMC5000:_HSIO_STD: GPIO full drive strength. PSoC 6: GPIO cells and HSIO_STD cells: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec
		0x2: DRIVE_SEL_TWO : XMC5000: GPIO_STD/GPIO_ENH: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec. XMC5000:_GPIO_SMC: GPIO 1/2 drive strength. XMC5000:_HSIO_STD: GPIO 1/2 drive strength. PSoC 6: GPIO cells and HSIO_STD cells: 1/4 drive strength. GPIO drives current at 1/4 of its max rated spec.
		0x3: DRIVE_SEL_THREE : XMC5000: GPIO_STD/GPIO_ENH: 1/4 drive strength: GPIO drives current at 1/4 of its max rated spec. XMC5000:_GPIO_SMC: GPIO 1/4 drive strength. XMC5000:_HSIO_STD: GPIO 1/4 drive strength. PSoC 6: GPIO cells and HSIO_STD cells: 1/8 drive strength. GPIO drives current at 1/8 of its max rated spec.

GPIO_PRT4_CFG_IN_AUTOLVL

Port input buffer AUTOLVL configuration register
Address: 0x40310258
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			VTRIP_SEL4_1	VTRIP_SEL3_1	VTRIP_SEL2_1	VTRIP_SEL1_1	VTRIP_SEL0_1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	VTRIP_SEL4_1	Input buffer compatible with automotive (elevated Vil) interfaces. Default Value: 0
3	VTRIP_SEL3_1	Input buffer compatible with automotive (elevated Vil) interfaces. Default Value: 0
2	VTRIP_SEL2_1	Input buffer compatible with automotive (elevated Vil) interfaces. Default Value: 0
1	VTRIP_SEL1_1	Input buffer compatible with automotive (elevated Vil) interfaces. Default Value: 0

0	VTRIP_SEL0_1	Configures the input buffer mode (trip points and hysteresis) for GPIO upper bit. Lower bit is still selected by CFG_IN.VTRIP_SEL0_0 field. This field is used along with CFG_IN.VTRIP_SEL0_0 field as below: {CFG_IN_AUTOLVL.VTRIP_SEL0_1,CFG_IN.VTRIP_SEL0_0}: 0,0: CMOS 0,1: TTL 1,0: input buffer is compatible with automotive. 1,1: input buffer is compatible with automotvie Default Value: 0
		0x0: CMOS_OR_TTL : Input buffer compatible with CMOS/TTL interfaces as described in CFG_IN.VTRIP_SEL0_0.
		0x1: AUTO : Input buffer compatible with AUTO (elevated Vil) interfaces when used along with CFG_IN.VTRIP_SEL0_0.

GPIO_PRT6_OUT

Port output data register
Address: 0x40310300
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	OUT7	IO output data for pin 7 Default Value: 0
6	OUT6	IO output data for pin 6 Default Value: 0
5	OUT5	IO output data for pin 5 Default Value: 0
4	OUT4	IO output data for pin 4 Default Value: 0
3	OUT3	IO output data for pin 3 Default Value: 0
2	OUT2	IO output data for pin 2 Default Value: 0
1	OUT1	IO output data for pin 1 Default Value: 0
0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

GPIO_PRT6_IN

Port input state register
Address: 0x40310310
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the INTR_CFG.FLT_SEL register. Default Value: 0
7	IN7	IO pin state for pin 7 Default Value: 0
6	IN6	IO pin state for pin 6 Default Value: 0
5	IN5	IO pin state for pin 5 Default Value: 0
4	IN4	IO pin state for pin 4 Default Value: 0
3	IN3	IO pin state for pin 3 Default Value: 0
2	IN2	IO pin state for pin 2 Default Value: 0
1	IN1	IO pin state for pin 1 Default Value: 0

0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. On reset assertion , IN register will get reset. The Pad value takes 2 clock cycles to be reflected into IN Register. It's value then depends on the external pin value. Default Value: 0

GPIO_PRT6_INTR

Port interrupt status register
Address: 0x40310314
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	IN_IN7	IN_IN6	IN_IN5	IN_IN4	IN_IN3	IN_IN2	IN_IN1	IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
23	IN_IN7	IO pin state for pin 7 Default Value: 0
22	IN_IN6	IO pin state for pin 6 Default Value: 0
21	IN_IN5	IO pin state for pin 5 Default Value: 0
20	IN_IN4	IO pin state for pin 4 Default Value: 0
19	IN_IN3	IO pin state for pin 3 Default Value: 0
18	IN_IN2	IO pin state for pin 2 Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0
16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0

7	EDGE7	Edge detect for IO pin 7 Default Value: 0
6	EDGE6	Edge detect for IO pin 6 Default Value: 0
5	EDGE5	Edge detect for IO pin 5 Default Value: 0
4	EDGE4	Edge detect for IO pin 4 Default Value: 0
3	EDGE3	Edge detect for IO pin 3 Default Value: 0
2	EDGE2	Edge detect for IO pin 2 Default Value: 0
1	EDGE1	Edge detect for IO pin 1 Default Value: 0
0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

GPIO_PRT6_INTR_MASK

Port interrupt mask register
Address: 0x40310318
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Masks edge interrupt on IO pin 7 Default Value: 0
6	EDGE6	Masks edge interrupt on IO pin 6 Default Value: 0
5	EDGE5	Masks edge interrupt on IO pin 5 Default Value: 0
4	EDGE4	Masks edge interrupt on IO pin 4 Default Value: 0
3	EDGE3	Masks edge interrupt on IO pin 3 Default Value: 0
2	EDGE2	Masks edge interrupt on IO pin 2 Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0
0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

GPIO_PRT6_INTR_MASKED

Port interrupt masked status register
Address: 0x4031031C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Edge detected and masked on IO pin 7 Default Value: 0
6	EDGE6	Edge detected and masked on IO pin 6 Default Value: 0
5	EDGE5	Edge detected and masked on IO pin 5 Default Value: 0
4	EDGE4	Edge detected and masked on IO pin 4 Default Value: 0
3	EDGE3	Edge detected and masked on IO pin 3 Default Value: 0
2	EDGE2	Edge detected and masked on IO pin 2 Default Value: 0
1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0

0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

GPIO_PRT6_INTR_SET

Port interrupt set register
Address: 0x40310320
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Sets edge detect interrupt for IO pin 7 Default Value: 0
6	EDGE6	Sets edge detect interrupt for IO pin 6 Default Value: 0
5	EDGE5	Sets edge detect interrupt for IO pin 5 Default Value: 0
4	EDGE4	Sets edge detect interrupt for IO pin 4 Default Value: 0
3	EDGE3	Sets edge detect interrupt for IO pin 3 Default Value: 0
2	EDGE2	Sets edge detect interrupt for IO pin 2 Default Value: 0
1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0
0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

GPIO_PRT6_INTR_CFG

Port interrupt configuration register
Address: 0x40310340
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0
		0x0: DISABLE : Disabled
		0x1: RISING : Rising edge
		0x2: FALLING : Falling edge
		0x3: BOTH : Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pin 7 Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pin 6 Default Value: 0
11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pin 5 Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pin 4 Default Value: 0

7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pin 3 Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pin 2 Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0
		0x0: DISABLE : Disabled
		0x1: RISING : Rising edge
		0x2: FALLING : Falling edge
		0x3: BOTH : Both rising and falling edges

GPIO_PRT6_CFG

Port configuration register
Address: 0x40310344
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN3	DRIVE_MODE3 [14:12]			IN_EN2	DRIVE_MODE2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN5	DRIVE_MODE5 [22:20]			IN_EN4	DRIVE_MODE4 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN7	DRIVE_MODE7 [30:28]			IN_EN6	DRIVE_MODE6 [26:24]		

Bits	Name	Description
31	IN_EN7	Enables the input buffer for IO pin 7 Default Value: 0
30 : 28	DRIVE_MODE7	The GPIO drive mode for IO pin 7. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
27	IN_EN6	Enables the input buffer for IO pin 6 Default Value: 0
26 : 24	DRIVE_MODE6	The GPIO drive mode for IO pin 6. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
23	IN_EN5	Enables the input buffer for IO pin 5 Default Value: 0
22 : 20	DRIVE_MODE5	The GPIO drive mode for IO pin 5. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
19	IN_EN4	Enables the input buffer for IO pin 4 Default Value: 0
18 : 16	DRIVE_MODE4	The GPIO drive mode for IO pin 4. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
15	IN_EN3	Enables the input buffer for IO pin 3 Default Value: 0
14 : 12	DRIVE_MODE3	The GPIO drive mode for IO pin 3. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
11	IN_EN2	Enables the input buffer for IO pin 2 Default Value: 0
10 : 8	DRIVE_MODE2	The GPIO drive mode for IO pin 2. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0
2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up

GPIO_PRT6_CFG_IN

Port input buffer configuration register
Address: 0x40310348
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	VTRIP_SEL7_0	VTRIP_SEL6_0	VTRIP_SEL5_0	VTRIP_SEL4_0	VTRIP_SEL3_0	VTRIP_SEL2_0	VTRIP_SEL1_0	VTRIP_SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	VTRIP_SEL7_0	Configures the pin 7 input buffer mode (trip points and hysteresis) Default Value: 0
6	VTRIP_SEL6_0	Configures the pin 6 input buffer mode (trip points and hysteresis) Default Value: 0
5	VTRIP_SEL5_0	Configures the pin 5 input buffer mode (trip points and hysteresis) Default Value: 0
4	VTRIP_SEL4_0	Configures the pin 4 input buffer mode (trip points and hysteresis) Default Value: 0
3	VTRIP_SEL3_0	Configures the pin 3 input buffer mode (trip points and hysteresis) Default Value: 0
2	VTRIP_SEL2_0	Configures the pin 2 input buffer mode (trip points and hysteresis) Default Value: 0
1	VTRIP_SEL1_0	Configures the pin 1 input buffer mode (trip points and hysteresis) Default Value: 0

0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0
		0x0: CMOS : PSoC 6:: Input buffer compatible with CMOS and I2C interfaces XMC5000: Full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1
		0x1: TTL : PSoC 6:: Input buffer compatible with TTL and MediaLB interfaces XMC5000: full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1

GPIO_PRT6_CFG_OUT

Port output buffer configuration register
Address: 0x4031034C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL3 [23:22]		DRIVE_SEL2 [21:20]		DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL7 [31:30]		DRIVE_SEL6 [29:28]		DRIVE_SEL5 [27:26]		DRIVE_SEL4 [25:24]	

Bits	Name	Description
31 : 30	DRIVE_SEL7	Sets the GPIO drive strength for IO pin 7 Default Value: 0
29 : 28	DRIVE_SEL6	Sets the GPIO drive strength for IO pin 6 Default Value: 0
27 : 26	DRIVE_SEL5	Sets the GPIO drive strength for IO pin 5 Default Value: 0
25 : 24	DRIVE_SEL4	Sets the GPIO drive strength for IO pin 4 Default Value: 0
23 : 22	DRIVE_SEL3	Sets the GPIO drive strength for IO pin 3 Default Value: 0
21 : 20	DRIVE_SEL2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
17 : 16	DRIVE_SEL0	Documentation: Note: DRIVE_SELx are used among GPIO cells and HSIO_STD but the encoding values may differ as shown on the right side of this table Default Value: 0

		0x0: DRIVE_SEL_ZERO : XMC5000: GPIO_STD/GPIO_ENH: Full drive strengh: GPIO drives current at its max rated spec. XMC5000:_GPIO_SMC: GPIO_SMC default mode. XMC5000:_HSIO_STD: HSIO default mode. PSoC 6: GPIO cells and HSIO_STD cells: Full drive strength: GPIO drives current at its max rated spec.
		0x1: DRIVE_SEL_ONE : XMC5000: GPIO_STD/GPIO_ENH: Full drive strengh: GPIO drives current at its max rated spec. XMC5000:_GPIO_SMC: GPIO full drive strength. XMC5000:_HSIO_STD: GPIO full drive strength. PSoC 6: GPIO cells and HSIO_STD cells: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec
		0x2: DRIVE_SEL_TWO : XMC5000: GPIO_STD/GPIO_ENH: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec. XMC5000:_GPIO_SMC: GPIO 1/2 drive strength. XMC5000:_HSIO_STD: GPIO 1/2 drive strength. PSoC 6: GPIO cells and HSIO_STD cells: 1/4 drive strength. GPIO drives current at 1/4 of its max rated spec.
		0x3: DRIVE_SEL_THREE : XMC5000: GPIO_STD/GPIO_ENH: 1/4 drive strength: GPIO drives current at 1/4 of its max rated spec. XMC5000:_GPIO_SMC: GPIO 1/4 drive strength. XMC5000:_HSIO_STD: GPIO 1/4 drive strength. PSoC 6: GPIO cells and HSIO_STD cells: 1/8 drive strength. GPIO drives current at 1/8 of its max rated spec.

GPIO_PRT6_CFG_IN_AUTOLVL

Port input buffer AUTOLVL configuration register
Address: 0x40310358
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	VTRIP_SEL7_1	VTRIP_SEL6_1	VTRIP_SEL5_1	VTRIP_SEL4_1	VTRIP_SEL3_1	VTRIP_SEL2_1	VTRIP_SEL1_1	VTRIP_SEL0_1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	VTRIP_SEL7_1	Input buffer compatible with automotive (elevated Vil) interfaces. Default Value: 0
6	VTRIP_SEL6_1	Input buffer compatible with automotive (elevated Vil) interfaces. Default Value: 0
5	VTRIP_SEL5_1	Input buffer compatible with automotive (elevated Vil) interfaces. Default Value: 0
4	VTRIP_SEL4_1	Input buffer compatible with automotive (elevated Vil) interfaces. Default Value: 0
3	VTRIP_SEL3_1	Input buffer compatible with automotive (elevated Vil) interfaces. Default Value: 0
2	VTRIP_SEL2_1	Input buffer compatible with automotive (elevated Vil) interfaces. Default Value: 0
1	VTRIP_SEL1_1	Input buffer compatible with automotive (elevated Vil) interfaces. Default Value: 0

0	VTRIP_SEL0_1	Configures the input buffer mode (trip points and hysteresis) for GPIO upper bit. Lower bit is still selected by CFG_IN.VTRIP_SEL0_0 field. This field is used along with CFG_IN.VTRIP_SEL0_0 field as below: {CFG_IN_AUTOLVL.VTRIP_SEL0_1,CFG_IN.VTRIP_SEL0_0}: 0,0: CMOS 0,1: TTL 1,0: input buffer is compatible with automotive. 1,1: input buffer is compatible with automotvie Default Value: 0
		0x0: CMOS_OR_TTL : Input buffer compatible with CMOS/TTL interfaces as described in CFG_IN.VTRIP_SEL0_0.
		0x1: AUTO : Input buffer compatible with AUTO (elevated Vil) interfaces when used along with CFG_IN.VTRIP_SEL0_0.

GPIO_PRT11_OUT

Port output data register
Address: 0x40310580
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					RW	RW	RW
Name	None [7:3]					OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	OUT2	IO output data for pin 2 Default Value: 0
1	OUT1	IO output data for pin 1 Default Value: 0
0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

GPIO_PRT11_IN

Port input state register
Address: 0x40310590
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					IN2	IN1	IN0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the INTR_CFG.FLT_SEL register. Default Value: 0
2	IN2	IO pin state for pin 2 Default Value: 0
1	IN1	IO pin state for pin 1 Default Value: 0
0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. On reset assertion , IN register will get reset. The Pad value takes 2 clock cycles to be reflected into IN Register. It's value then depends on the external pin value. Default Value: 0

GPIO_PRT11_INTR

Port interrupt status register
Address: 0x40310594
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					A	A	A
Name	None [7:3]					EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [23:19]					IN_IN2	IN_IN1	IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
18	IN_IN2	IO pin state for pin 2 Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0
16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
2	EDGE2	Edge detect for IO pin 2 Default Value: 0
1	EDGE1	Edge detect for IO pin 1 Default Value: 0
0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

GPIO_PRT11_INTR_MASK

Port interrupt mask register
Address: 0x40310598
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
2	EDGE2	Masks edge interrupt on IO pin 2 Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0
0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

GPIO_PRT11_INTR_MASKED

Port interrupt masked status register
Address: 0x4031059C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
2	EDGE2	Edge detected and masked on IO pin 2 Default Value: 0
1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0
0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

GPIO_PRT11_INTR_SET

Port interrupt set register
Address: 0x403105A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [7:3]					EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
2	EDGE2	Sets edge detect interrupt for IO pin 2 Default Value: 0
1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0
0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

GPIO_PRT11_INTR_CFG

Port interrupt configuration register
Address: 0x403105C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0
		0x0: DISABLE : Disabled
		0x1: RISING : Rising edge
		0x2: FALLING : Falling edge
		0x3: BOTH : Both rising and falling edges
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pin 2 Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0
		0x0: DISABLE : Disabled

		0x1: RISING : Rising edge
		0x2: FALLING : Falling edge
		0x3: BOTH : Both rising and falling edges

GPIO_PRT11_CFG

Port configuration register
Address: 0x403105C4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW			RW	RW		
HW Access	None	R			R	R		
Name	None	DRIVE_MODE3 [14:12]			IN_EN2	DRIVE_MODE2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	DRIVE_MODE5 [22:20]			None	DRIVE_MODE4 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	DRIVE_MODE7 [30:28]			None	DRIVE_MODE6 [26:24]		

Bits	Name	Description
30 : 28	DRIVE_MODE7	The GPIO drive mode for IO pin 7. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
26 : 24	DRIVE_MODE6	The GPIO drive mode for IO pin 6. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance

		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down
		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up

22 : 20	DRIVE_MODE5	The GPIO drive mode for IO pin 5. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up

		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down
		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
18 : 16	DRIVE_MODE4	The GPIO drive mode for IO pin 4. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
14 : 12	DRIVE_MODE3	The GPIO drive mode for IO pin 3. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance

		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down
		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
11	IN_EN2	Enables the input buffer for IO pin 2 Default Value: 0

10 : 8	DRIVE_MODE2	The GPIO drive mode for IO pin 2. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up

		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down
		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up
3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0
2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0
		0x0: HIGHZ : Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x1: RESERVED : This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance
		0x2: PULLUP : Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/ resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/ DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up
		0x3: PULLDOWN : Resistive pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull down D_OUT = '1': Weak/resistive pull down

		0x4: OD_DRIVESLOW : Open drain, drives low For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': High Impedance When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x5: OD_DRIVESHIGH : Open drain, drives high For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': High Impedance D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance
		0x6: STRONG : Strong D_OUTput buffer For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High Impedance D_OUT = '1': High Impedance

		0x7: PULLUP_DOWN : Pull up or pull down For GPIO & UDB/DSI peripherals: When D_OUT_EN = '0': GPIO_DSI_OUT = '0': Weak/ resistive pull down GPIO_DSI_OUT = '1': Weak/resistive pull up where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT. For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/ resistive pull down D_OUT = '1': Weak/resistive pull up

GPIO_PRT11_CFG_IN

Port input buffer configuration register
Address: 0x403105C8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					VTRIP_SEL2_0	VTRIP_SEL1_0	VTRIP_SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	VTRIP_SEL2_0	Configures the pin 2 input buffer mode (trip points and hysteresis) Default Value: 0
1	VTRIP_SEL1_0	Configures the pin 1 input buffer mode (trip points and hysteresis) Default Value: 0
0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0
		0x0: CMOS : PSoC 6:: Input buffer compatible with CMOS and I2C interfaces XMC5000: Full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1
		0x1: TTL : PSoC 6:: Input buffer compatible with TTL and MediaLB interfaces XMC5000: full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1

GPIO_PRT11_CFG_OUT

Port output buffer configuration register
Address: 0x403105CC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		DRIVE_SEL2 [21:20]		DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21 : 20	DRIVE_SEL2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
17 : 16	DRIVE_SEL0	Documentation: Note: DRIVE_SELx are used among GPIO cells and HSIO_STD but the encoding values may differ as shown on the right side of this table Default Value: 0
		0x0: DRIVE_SEL_ZERO : XMC5000: GPIO_STD/GPIO_ENH: Full drive strengh: GPIO drives current at its max rated spec. XMC5000:_GPIO_SMC: GPIO_SMC default mode. XMC5000:_HSIO_STD: HSIO default mode. PSoC 6: GPIO cells and HSIO_STD cells: Full drive strength: GPIO drives current at its max rated spec.

		0x1: DRIVE_SEL_ONE : XMC5000: GPIO_STD/GPIO_ENH: Full drive strengh: GPIO drives current at its max rated spec. XMC5000:_GPIO_SMC: GPIO full drive strength. XMC5000:_HSIO_STD: GPIO full drive strength. PSoC 6: GPIO cells and HSIO_STD cells: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec
		0x2: DRIVE_SEL_TWO : XMC5000: GPIO_STD/GPIO_ENH: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec. XMC5000:_GPIO_SMC: GPIO 1/2 drive strength. XMC5000:_HSIO_STD: GPIO 1/2 drive strength. PSoC 6: GPIO cells and HSIO_STD cells: 1/4 drive strength. GPIO drives current at 1/4 of its max rated spec.
		0x3: DRIVE_SEL_THREE : XMC5000: GPIO_STD/GPIO_ENH: 1/4 drive strength: GPIO drives current at 1/4 of its max rated spec. XMC5000:_GPIO_SMC: GPIO 1/4 drive strength. XMC5000:_HSIO_STD: GPIO 1/4 drive strength. PSoC 6: GPIO cells and HSIO_STD cells: 1/8 drive strength. GPIO drives current at 1/8 of its max rated spec.

GPIO_PRT11_CFG_IN_AUTOLVL

Port input buffer AUTOLVL configuration register
Address: 0x403105D8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					VTRIP_SEL2_1	VTRIP_SEL1_1	VTRIP_SEL0_1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	VTRIP_SEL2_1	Input buffer compatible with automotive (elevated Vil) interfaces. Default Value: 0
1	VTRIP_SEL1_1	Input buffer compatible with automotive (elevated Vil) interfaces. Default Value: 0
0	VTRIP_SEL0_1	Configures the input buffer mode (trip points and hysteresis) for GPIO upper bit. Lower bit is still selected by CFG_IN.VTRIP_SEL0_0 field. This field is used along with CFG_IN.VTRIP_SEL0_0 field as below: {CFG_IN_AUTOLVL.VTRIP_SEL0_1,CFG_IN.VTRIP_SEL0_0}: 0,0: CMOS 0,1: TTL 1,0: input buffer is compatible with automotive. 1,1: input buffer is compatible with automotvie Default Value: 0

		0x0: CMOS_OR_TTL : Input buffer compatible with CMOS/TTL interfaces as described in CFG_IN.VTRIP_SEL0_0.
		0x1: AUTO : Input buffer compatible with AUTO (elevated Vil) interfaces when used along with CFG_IN.VTRIP_SEL0_0.

GPIO_INTR_CAUSE0

Interrupt port cause register 0
Address: 0x40314000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	PORT_INT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	PORT_INT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	PORT_INT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	PORT_INT	Each IO port has an associated bit field in this register. The bit field reflects the IO port's interrupt line (bit field i reflects "gpio_interrupts[i]" for IO port i). The register is used when the system uses a combined interrupt line "gpio_interrupt". The software ISR reads the register to determine which IO port(s) is responsible for the combined interrupt line. Once, the IO port(s) is determined, the IO port's GPIO_PRT_INTR register is read to determine the IO pin(s) in the IO port that caused the interrupt. '0': Port has no pending interrupt '1': Port has pending interrupt Default Value: 0

GPIO_VDD_ACTIVE

Extern power supply detection register
Address: 0x40314010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	
HW Access	None						W	
Name	None [7:2]						VDDIO_ACTIVE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	VDDD_ACTIVE	VDDA_ACTIVE	None [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	This bit indicates presence of the VDDD supply. This bit will always read-back 1. The VDDD supply has robust brown-out protection monitoring and it is not possible to read back this register without a valid supply. (This bit is used in certain test-modes to observe the brown-out detector status.) Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0

1 : 0	VDDIO_ACTIVE	Indicates presence or absence of VDDIO supplies (i.e. other than VDDD, VDDA) on the device (supplies are numbered 0..n-1). Note that VDDIO supplies have basic (crude) supply detectors only. If separate, robust, brown-out detection is desired on IO supplies, on-chip or off-chip analog resources need to provide it. For these bits to work reliable, the supply must be within valid spec range (per datasheet) or held at ground. Any in-between voltage has an undefined result. '0': Supply is not present '1': Supply is present When multiple VDDIO supplies are present, they will be assigned in alphanumeric ascending order to these bits during implementation. For example "vddusb, vddio_0, vddio_a, vbackup, vddio_r, vddio_1" are present then they will be assigned to these bits as below: 0: vbackup, 1: vddio_0, 2: vddio_1, 3: vddio_a, 4: vddio_r, 5: vddusb" Default Value: 0

GPIO_VDD_INTR

Supply detection interrupt register
Address: 0x40314014
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	
HW Access	None						A	
Name	None [7:2]						VDDIO_ACTIVE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C	RW1C	None					
HW Access	A	A	None					
Name	VDDD_ACTIVE	VDDA_ACTIVE	None [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	The VDDD supply is always present during operation so a supply transition can not occur. This bit will always read back '1'. Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0
1 : 0	VDDIO_ACTIVE	Supply state change detected. '0': No change to supply detected '1': Change to supply detected Default Value: 0

GPIO_VDD_INTR_MASK

Supply detection interrupt mask register
Address: 0x40314018
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						VDDIO_ACTIVE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	VDDD_ACTIVE	VDDA_ACTIVE	None [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	Same as VDDIO_ACTIVE for the digital supply VDDD. Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0
1 : 0	VDDIO_ACTIVE	Masks supply interrupt on VDDIO. '0': VDDIO interrupt forwarding disabled '1': VDDIO interrupt forwarding enabled Default Value: 0

GPIO_VDD_INTR_MASKED

Supply detection interrupt masked register
Address: 0x4031401C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	
HW Access	None						W	
Name	None [7:2]						VDDIO_ACTIVE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	VDDD_ACTIVE	VDDA_ACTIVE	None [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	Same as VDDIO_ACTIVE for the digital supply VDDD. Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0
1 : 0	VDDIO_ACTIVE	Supply transition detected AND masked '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

GPIO_VDD_INTR_SET

Supply detection interrupt set register
Address: 0x40314020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	
HW Access	None						A	
Name	None [7:2]						VDDIO_ACTIVE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	RW1S	None					
HW Access	A	A	None					
Name	VDDD_ACTIVE	VDDA_ACTIVE	None [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	Same as VDDIO_ACTIVE for the digital supply VDDD. Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0
1 : 0	VDDIO_ACTIVE	Sets supply interrupt. '0': Interrupt state not affected '1': Interrupt set Default Value: 0

SMARTIO_PRT12_CTL

Control register
Address: 0x40320C00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BYPASS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			CLOCK_SRC [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	RW
HW Access	R	None					R	R
Name	ENABLED	None [30:26]					PIPELINE_EN	HLD_OVR

Bits	Name	Description
31	ENABLED	Enable for programmable IO. Should only be set to '1' when the programmable IO is completely configured: '0': Disabled (signals are bypassed; behavior as if BYPASS is 0xFF). When disabled, the fabric (data unit and LUTs) reset is activated. If the IP is disabled: - The PIPELINE_EN register field should be set to '1', to ensure low power consumption by preventing combinatorial loops. - The CLOCK_SRC register field should be set to "20"-"30" (clock is constant '0'), to ensure low power consumption. '1': Enabled. Once enabled, it takes 3 "clk_fabric" clock cycles till the fabric reset is de-activated and the fabric becomes fully functional. This ensures that the IO pins' input synchronizer states are flushed when the fabric is fully functional. Default Value: 0

25	PIPELINE_EN	Enable for pipeline register: '0': Disabled (register is bypassed). '1': Enabled. Default Value: 1
24	HLD_OVR	IO cell hold override functionality. In DeepSleep power mode, the HSIOM holds the IO cell output and output enable signals if Active functionality is connected to the IO pads. This is undesirable if the SMARTIO is supposed to deliver DeepSleep output functionality on these IO pads. This field is used to control the hold override functionality from the SMARTIO: '0': The HSIOM controls the IO cell hold override functionality ("hsiom_hld_ovr"). '1': The SMARTIO controls the IO cel hold override functionality: - In bypass mode (ENABLED is '0' or BYPASS[i] is '1'), the HSIOM control is used. - In NON bypass mode (ENABLED is '1' and BYPASS[i] is '0'), the SMARTIO sets hold override to "pwr_hld_ovr_hib" to enable SMARTIO functionality in DeepSleep power mode (but disables it in Hibernate or Stop power mode). Default Value: Undefined

12 : 8	CLOCK_SRC	Clock ("clk_fabric") and reset ("rst_fabric_n") source selection: "0": io_data_in[0]/'1'. ... "7": io_data_in[7]/'1'. "8": chip_data[0]/'1'. ... "15": chip_data[7]/'1'. "16": clk_smartio/ rst_sys_act_n. Used for both Active functionality synchronous logic on "clk_smartio". This selection is intended for synchronous operation on a PCLK specified clock frequency ("clock_smartio_pos_en"). Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to "clk_sys". "17": clk_smartio/rst_sys_dpslp_n. Used for both DeepSleep functionality synchronous logic on "clk_smartio" (note that "clk_smartio" is NOT available in DeepSleep and Hibernate power modes). This selection is intended for synchronous operation on a PCLK specified clock frequency ("clock_smartio_pos_en"). Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to "clk_sys". "18": Same as "17". Note that the M0S8 SMARTIO version used the Hibernate reset for this value, but the MXS40 SMARTIO version does not support Hibernate functionality. "19": clk_lf/rst_lf_dpslp_n (note that "clk_lf" is available in DeepSleep power mode). This selection is intended for synchronous operation on"clk_lf". Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to other "clk_lf" clocked elements. "20"-"30": Clock source is constant '0'. Any of these clock sources should be selected when the IP is disabled to ensure low power consumption. "31": asynchronous mode/'1'. Select this when clockless operation is configured. NOTE: Two positive edges of the selected clock are required for the block to be enabled (to deactivate reset). In asynchronous (clockless) mode clk_sys is used to enable the block,

		but is not available for clocking. Default Value: 0x14
7 : 0	BYPASS	Bypass of the programmable IO, one bit for each IO pin: BYPASS[i] is for IO pin i. When ENABLED is '1', this field is used. When ENABLED is '0', this field is NOT used and SMARTIO fabric is always bypassed. '0': No bypass (programmable SMARTIO fabric is exposed). '1': Bypass (programmable SMARTIOIO fabric is hidden). Default Value: Undefined

SMARTIO_PRT12_SYNC_CTL

Synchronization control register
Address: 0x40320C10
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IO_SYNC_EN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CHIP_SYNC_EN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	CHIP_SYNC_EN	Synchronization of the chip input signals to "clk_fabric", one bit for each input: CHIP_SYNC_EN[i] is for input i. '0': No synchronization. '1': Synchronization. Default Value: Undefined
7 : 0	IO_SYNC_EN	Synchronization of the IO pin input signals to "clk_fabric", one bit for each IO pin: IO_SYNC_EN[i] is for IO pin i. '0': No synchronization. '1': Synchronization. Default Value: Undefined

SMARTIO_PRT12_LUT_SEL0

LUT component input selection
Address: 0x40320C20
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined

11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined
3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

SMARTIO_PRT12_LUT_CTL0

LUT component control register
Address: 0x40320C40
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

SMARTIO_PRT12_DU_SEL

Data unit component input selection
Address: 0x40320CC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DU_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				DU_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				DU_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None		RW	
HW Access	None		R		None		R	
Name	None [31:30]		DU_DATA1_SEL [29:28]		None [27:26]		DU_DATA0_SEL [25:24]	

Bits	Name	Description
29 : 28	DU_DATA1_SEL	Data unit input data "data1_in" source selection. Encoding is the same as for DU_DATA0_SEL. Default Value: Undefined
25 : 24	DU_DATA0_SEL	Data unit input data "data0_in" source selection: "0": Constant "0". "1": chip_data[7:0]. "2": io_data_in[7:0]. "3": DATA.DATA MMIO register field. Default Value: Undefined
19 : 16	DU_TR2_SEL	Data unit input signal "tr2_in" source selection. Encoding is the same as for DU_TR0_SEL. Default Value: Undefined
11 : 8	DU_TR1_SEL	Data unit input signal "tr1_in" source selection. Encoding is the same as for DU_TR0_SEL. Default Value: Undefined

3 : 0	DU_TR0_SEL	Data unit input signal "tr0_in" source selection: "0": Constant '0'. "1": Constant '1'. "2": Data unit output. "10-3": LUT 7 - 0 outputs. Otherwise: Undefined. Default Value: Undefined

SMARTIO_PRT12_DU_CTL

Data unit component control register
Address: 0x40320CC4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					DU_SIZE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				DU_OPC [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 8	DU_OPC	Data unit opcode specifies the data unit operation: "1": INCR "2": DECR "3": INCR_WRAP "4": DECR_WRAP "5": INCR_DECR "6": INCR_DECR_WRAP "7": ROR "8": SHR "9": AND_OR "10": SHR_MAJ3 "11": SHR_EQL. Otherwise: Undefined. Default Value: Undefined
2 : 0	DU_SIZE	Size/width of the data unit data operands (in bits) is DU_SIZE+1. E.g., if DU_SIZE is 7, the width is 8 bits. Default Value: Undefined

SMARTIO_PRT12_DATA

Data register
Address: 0x40320CF0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Data unit input data source. Default Value: Undefined

12 Controller area network flexible datarate (CANFD)

Register details

Register name	Address	Description
CANFD0_CH0_CREL	0x40520000	Core Release Register
CANFD0_CH0_ENDN	0x40520004	Endian Register
CANFD0_CH0_DBTP	0x4052000C	Data Bit Timing & Prescaler Register
CANFD0_CH0_TEST	0x40520010	Test Register
CANFD0_CH0_RWD	0x40520014	RAM Watchdog
CANFD0_CH0_CCCR	0x40520018	CC Control Register
CANFD0_CH0_NBTP	0x4052001C	Nominal Bit Timing & Prescaler Register
CANFD0_CH0_TSCC	0x40520020	Timestamp Counter Configuration
CANFD0_CH0_TSCV	0x40520024	Timestamp Counter Value
CANFD0_CH0_TOCC	0x40520028	Timeout Counter Configuration
CANFD0_CH0_TOCV	0x4052002C	Timeout Counter Value
CANFD0_CH0_ECR	0x40520040	Error Counter Register
CANFD0_CH0_PSR	0x40520044	Protocol Status Register
CANFD0_CH0_TDCR	0x40520048	Transmitter Delay Compensation Register
CANFD0_CH0_IR	0x40520050	Interrupt Register
CANFD0_CH0_IE	0x40520054	Interrupt Enable
CANFD0_CH0_ILS	0x40520058	Interrupt Line Select
CANFD0_CH0_ILE	0x4052005C	Interrupt Line Enable
CANFD0_CH0_GFC	0x40520080	Global Filter Configuration
CANFD0_CH0_SIDFC	0x40520084	Standard ID Filter Configuration
CANFD0_CH0_XIDFC	0x40520088	Extended ID Filter Configuration
CANFD0_CH0_XIDAM	0x40520090	Extended ID AND Mask
CANFD0_CH0_HPMS	0x40520094	High Priority Message Status
CANFD0_CH0_NDAT1	0x40520098	New Data 1
CANFD0_CH0_NDAT2	0x4052009C	New Data 2
CANFD0_CH0_RXF0C	0x405200A0	Rx FIFO 0 Configuration
CANFD0_CH0_RXF0S	0x405200A4	Rx FIFO 0 Status
CANFD0_CH0_RXF0A	0x405200A8	Rx FIFO 0 Acknowledge
CANFD0_CH0_RXBC	0x405200AC	Rx Buffer Configuration
CANFD0_CH0_RXF1C	0x405200B0	Rx FIFO 1 Configuration
CANFD0_CH0_RXF1S	0x405200B4	Rx FIFO 1 Status
CANFD0_CH0_RXF1A	0x405200B8	Rx FIFO 1 Acknowledge
CANFD0_CH0_RXESC	0x405200BC	Rx Buffer / FIFO Element Size Configuration
CANFD0_CH0_TXBC	0x405200C0	Tx Buffer Configuration
CANFD0_CH0_TXFQS	0x405200C4	Tx FIFO/Queue Status

Register name	Address	Description
CANFD0_CH0_TXESC	0x405200C8	Tx Buffer Element Size Configuration
CANFD0_CH0_TXBRP	0x405200CC	Tx Buffer Request Pending
CANFD0_CH0_TXBAR	0x405200D0	Tx Buffer Add Request
CANFD0_CH0_TXBCR	0x405200D4	Tx Buffer Cancellation Request
CANFD0_CH0_TXBTO	0x405200D8	Tx Buffer Transmission Occurred
CANFD0_CH0_TXBCF	0x405200DC	Tx Buffer Cancellation Finished
CANFD0_CH0_TXBTIE	0x405200E0	Tx Buffer Transmission Interrupt Enable
CANFD0_CH0_TXBCIE	0x405200E4	Tx Buffer Cancellation Finished Interrupt Enable
CANFD0_CH0_TXEFC	0x405200F0	Tx Event FIFO Configuration
CANFD0_CH0_TXEFS	0x405200F4	Tx Event FIFO Status
CANFD0_CH0_TXEFA	0x405200F8	Tx Event FIFO Acknowledge
CANFD0_CH0_TTTMC	0x40520100	TT Trigger Memory Configuration
CANFD0_CH0_TTRMC	0x40520104	TT Reference Message Configuration
CANFD0_CH0_TTOCF	0x40520108	TT Operation Configuration
CANFD0_CH0_TTMLM	0x4052010C	TT Matrix Limits
CANFD0_CH0_TURCF	0x40520110	TUR Configuration
CANFD0_CH0_TTOCN	0x40520114	TT Operation Control
CANFD0_CH0_TTGTP	0x40520118	TT Global Time Preset
CANFD0_CH0_TTTMK	0x4052011C	TT Time Mark
CANFD0_CH0_TTIR	0x40520120	TT Interrupt Register
CANFD0_CH0_TTIE	0x40520124	TT Interrupt Enable
CANFD0_CH0_TTILS	0x40520128	TT Interrupt Line Select
CANFD0_CH0_TTOST	0x4052012C	TT Operation Status
CANFD0_CH0_TURNA	0x40520130	TUR Numerator Actual
CANFD0_CH0_TTLGT	0x40520134	TT Local & Global Time
CANFD0_CH0_TTCTC	0x40520138	TT Cycle Time & Count
CANFD0_CH0_TTCPT	0x4052013C	TT Capture Time
CANFD0_CH0_TTCSM	0x40520140	TT Cycle Sync Mark
CANFD0_CH0_RXFTOP_CTL	0x40520180	Receive FIFO Top control
CANFD0_CH0_RXFTOP0_STAT	0x405201A0	Receive FIFO 0 Top Status
CANFD0_CH0_RXFTOP0_DATA	0x405201A8	Receive FIFO 0 Top Data
CANFD0_CH0_RXFTOP1_STAT	0x405201B0	Receive FIFO 1 Top Status
CANFD0_CH0_RXFTOP1_DATA	0x405201B8	Receive FIFO 1 Top Data
CANFD0_CH1_CREL	0x40520200	Core Release Register. See CANFD0_CH0_CREL for the details of bit fields.
CANFD0_CH1_ENDN	0x40520204	Endian Register. See CANFD0_CH0_ENDN for the details of bit fields.
CANFD0_CH1_DBTP	0x4052020C	Data Bit Timing & Prescaler Register. See CANFD0_CH0_DBTP for the details of bit fields.

Register name	Address	Description
CANFD0_CH1_TEST	0x40520210	Test Register. See CANFD0_CH0_TEST for the details of bit fields.
CANFD0_CH1_RWD	0x40520214	RAM Watchdog. See CANFD0_CH0_RWD for the details of bit fields.
CANFD0_CH1_CCCR	0x40520218	CC Control Register. See CANFD0_CH0_CCCR for the details of bit fields.
CANFD0_CH1_NBTP	0x4052021C	Nominal Bit Timing & Prescaler Register. See CANFD0_CH0_NBTP for the details of bit fields.
CANFD0_CH1_TSCC	0x40520220	Timestamp Counter Configuration. See CANFD0_CH0_TSCC for the details of bit fields.
CANFD0_CH1_TSCV	0x40520224	Timestamp Counter Value. See CANFD0_CH0_TSCV for the details of bit fields.
CANFD0_CH1_TOCC	0x40520228	Timeout Counter Configuration. See CANFD0_CH0_TOCC for the details of bit fields.
CANFD0_CH1_TOCV	0x4052022C	Timeout Counter Value. See CANFD0_CH0_TOCV for the details of bit fields.
CANFD0_CH1_ECR	0x40520240	Error Counter Register. See CANFD0_CH0_ECR for the details of bit fields.
CANFD0_CH1_PSR	0x40520244	Protocol Status Register. See CANFD0_CH0_PSR for the details of bit fields.
CANFD0_CH1_TDCR	0x40520248	Transmitter Delay Compensation Register. See CANFD0_CH0_TDCR for the details of bit fields.
CANFD0_CH1_IR	0x40520250	Interrupt Register. See CANFD0_CH0_IR for the details of bit fields.
CANFD0_CH1_IE	0x40520254	Interrupt Enable. See CANFD0_CH0_IE for the details of bit fields.
CANFD0_CH1_ILS	0x40520258	Interrupt Line Select. See CANFD0_CH0_ILS for the details of bit fields.
CANFD0_CH1_ILE	0x4052025C	Interrupt Line Enable. See CANFD0_CH0_ILE for the details of bit fields.
CANFD0_CH1_GFC	0x40520280	Global Filter Configuration. See CANFD0_CH0_GFC for the details of bit fields.
CANFD0_CH1_SIDFC	0x40520284	Standard ID Filter Configuration. See CANFD0_CH0_SIDFC for the details of bit fields.
CANFD0_CH1_XIDFC	0x40520288	Extended ID Filter Configuration. See CANFD0_CH0_XIDFC for the details of bit fields.
CANFD0_CH1_XIDAM	0x40520290	Extended ID AND Mask. See CANFD0_CH0_XIDAM for the details of bit fields.
CANFD0_CH1_HPMS	0x40520294	High Priority Message Status. See CANFD0_CH0_HPMS for the details of bit fields.
CANFD0_CH1_NDAT1	0x40520298	New Data 1. See CANFD0_CH0_NDAT1 for the details of bit fields.
CANFD0_CH1_NDAT2	0x4052029C	New Data 2. See CANFD0_CH0_NDAT2 for the details of bit fields.

Register name	Address	Description
CANFD0_CH1_RXF0C	0x405202A0	Rx FIFO 0 Configuration. See CANFD0_CH0_RXF0C for the details of bit fields.
CANFD0_CH1_RXF0S	0x405202A4	Rx FIFO 0 Status. See CANFD0_CH0_RXF0S for the details of bit fields.
CANFD0_CH1_RXF0A	0x405202A8	Rx FIFO 0 Acknowledge. See CANFD0_CH0_RXF0A for the details of bit fields.
CANFD0_CH1_RXBC	0x405202AC	Rx Buffer Configuration. See CANFD0_CH0_RXBC for the details of bit fields.
CANFD0_CH1_RXF1C	0x405202B0	Rx FIFO 1 Configuration. See CANFD0_CH0_RXF1C for the details of bit fields.
CANFD0_CH1_RXF1S	0x405202B4	Rx FIFO 1 Status. See CANFD0_CH0_RXF1S for the details of bit fields.
CANFD0_CH1_RXF1A	0x405202B8	Rx FIFO 1 Acknowledge. See CANFD0_CH0_RXF1A for the details of bit fields.
CANFD0_CH1_RXESC	0x405202BC	Rx Buffer / FIFO Element Size Configuration. See CANFD0_CH0_RXESC for the details of bit fields.
CANFD0_CH1_TXBC	0x405202C0	Tx Buffer Configuration. See CANFD0_CH0_TXBC for the details of bit fields.
CANFD0_CH1_TXFQS	0x405202C4	Tx FIFO/Queue Status. See CANFD0_CH0_TXFQS for the details of bit fields.
CANFD0_CH1_TXESC	0x405202C8	Tx Buffer Element Size Configuration. See CANFD0_CH0_TXESC for the details of bit fields.
CANFD0_CH1_TXBRP	0x405202CC	Tx Buffer Request Pending. See CANFD0_CH0_TXBRP for the details of bit fields.
CANFD0_CH1_TXBAR	0x405202D0	Tx Buffer Add Request. See CANFD0_CH0_TXBAR for the details of bit fields.
CANFD0_CH1_TXBCR	0x405202D4	Tx Buffer Cancellation Request. See CANFD0_CH0_TXBCR for the details of bit fields.
CANFD0_CH1_TXBTO	0x405202D8	Tx Buffer Transmission Occurred. See CANFD0_CH0_TXBTO for the details of bit fields.
CANFD0_CH1_TXBCF	0x405202DC	Tx Buffer Cancellation Finished. See CANFD0_CH0_TXBCF for the details of bit fields.
CANFD0_CH1_TXBTIE	0x405202E0	Tx Buffer Transmission Interrupt Enable. See CANFD0_CH0_TXBTIE for the details of bit fields.
CANFD0_CH1_TXBCIE	0x405202E4	Tx Buffer Cancellation Finished Interrupt Enable. See CANFD0_CH0_TXBCIE for the details of bit fields.
CANFD0_CH1_TXEFC	0x405202F0	Tx Event FIFO Configuration. See CANFD0_CH0_TXEFC for the details of bit fields.
CANFD0_CH1_TXEFS	0x405202F4	Tx Event FIFO Status. See CANFD0_CH0_TXEFS for the details of bit fields.
CANFD0_CH1_TXEFA	0x405202F8	Tx Event FIFO Acknowledge. See CANFD0_CH0_TXEFA for the details of bit fields.
CANFD0_CH1_TTTMC	0x40520300	TT Trigger Memory Configuration. See CANFD0_CH0_TTTMC for the details of bit fields.

Register name	Address	Description
CANFD0_CH1_TTRMC	0x40520304	TT Reference Message Configuration. See CANFD0_CH0_TTRMC for the details of bit fields.
CANFD0_CH1_TTOCF	0x40520308	TT Operation Configuration. See CANFD0_CH0_TTOCF for the details of bit fields.
CANFD0_CH1_TTMLM	0x4052030C	TT Matrix Limits. See CANFD0_CH0_TTMLM for the details of bit fields.
CANFD0_CH1_TURCF	0x40520310	TUR Configuration. See CANFD0_CH0_TURCF for the details of bit fields.
CANFD0_CH1_TTOCN	0x40520314	TT Operation Control. See CANFD0_CH0_TTOCN for the details of bit fields.
CANFD0_CH1_TTGTP	0x40520318	TT Global Time Preset. See CANFD0_CH0_TTGTP for the details of bit fields.
CANFD0_CH1_TTTMK	0x4052031C	TT Time Mark. See CANFD0_CH0_TTTMK for the details of bit fields.
CANFD0_CH1_TTIR	0x40520320	TT Interrupt Register. See CANFD0_CH0_TTIR for the details of bit fields.
CANFD0_CH1_TTIE	0x40520324	TT Interrupt Enable. See CANFD0_CH0_TTIE for the details of bit fields.
CANFD0_CH1_TTILS	0x40520328	TT Interrupt Line Select. See CANFD0_CH0_TTILS for the details of bit fields.
CANFD0_CH1_TTOST	0x4052032C	TT Operation Status. See CANFD0_CH0_TTOST for the details of bit fields.
CANFD0_CH1_TURNA	0x40520330	TUR Numerator Actual. See CANFD0_CH0_TURNA for the details of bit fields.
CANFD0_CH1_TTLGT	0x40520334	TT Local & Global Time. See CANFD0_CH0_TTLGT for the details of bit fields.
CANFD0_CH1_TTCTC	0x40520338	TT Cycle Time & Count. See CANFD0_CH0_TTCTC for the details of bit fields.
CANFD0_CH1_TTCPT	0x4052033C	TT Capture Time. See CANFD0_CH0_TTCPT for the details of bit fields.
CANFD0_CH1_TTCSM	0x40520340	TT Cycle Sync Mark. See CANFD0_CH0_TTCSM for the details of bit fields.
CANFD0_CH1_RXFTOP_CTL	0x40520380	Receive FIFO Top control. See CANFD0_CH0_RXFTOP_CTL for the details of bit fields.
CANFD0_CH1_RXFTOP0_STAT	0x405203A0	Receive FIFO 0 Top Status. See CANFD0_CH0_RXFTOP0_STAT for the details of bit fields.
CANFD0_CH1_RXFTOP0_DATA	0x405203A8	Receive FIFO 0 Top Data. See CANFD0_CH0_RXFTOP0_DATA for the details of bit fields.
CANFD0_CH1_RXFTOP1_STAT	0x405203B0	Receive FIFO 1 Top Status. See CANFD0_CH0_RXFTOP1_STAT for the details of bit fields.
CANFD0_CH1_RXFTOP1_DATA	0x405203B8	Receive FIFO 1 Top Data. See CANFD0_CH0_RXFTOP1_DATA for the details of bit fields.

Register name	Address	Description
CANFD0_CH2_CREL	0x40520400	Core Release Register. See CANFD0_CH0_CREL for the details of bit fields.
CANFD0_CH2_ENDN	0x40520404	Endian Register. See CANFD0_CH0_ENDN for the details of bit fields.
CANFD0_CH2_DBTP	0x4052040C	Data Bit Timing & Prescaler Register. See CANFD0_CH0_DBTP for the details of bit fields.
CANFD0_CH2_TEST	0x40520410	Test Register. See CANFD0_CH0_TEST for the details of bit fields.
CANFD0_CH2_RWD	0x40520414	RAM Watchdog. See CANFD0_CH0_RWD for the details of bit fields.
CANFD0_CH2_CCCR	0x40520418	CC Control Register. See CANFD0_CH0_CCCR for the details of bit fields.
CANFD0_CH2_NBTP	0x4052041C	Nominal Bit Timing & Prescaler Register. See CANFD0_CH0_NBTP for the details of bit fields.
CANFD0_CH2_TSCC	0x40520420	Timestamp Counter Configuration. See CANFD0_CH0_TSCC for the details of bit fields.
CANFD0_CH2_TSCV	0x40520424	Timestamp Counter Value. See CANFD0_CH0_TSCV for the details of bit fields.
CANFD0_CH2_TOCC	0x40520428	Timeout Counter Configuration. See CANFD0_CH0_TOCC for the details of bit fields.
CANFD0_CH2_TOCV	0x4052042C	Timeout Counter Value. See CANFD0_CH0_TOCV for the details of bit fields.
CANFD0_CH2_ECR	0x40520440	Error Counter Register. See CANFD0_CH0_ECR for the details of bit fields.
CANFD0_CH2_PSR	0x40520444	Protocol Status Register. See CANFD0_CH0_PSR for the details of bit fields.
CANFD0_CH2_TDCR	0x40520448	Transmitter Delay Compensation Register. See CANFD0_CH0_TDCR for the details of bit fields.
CANFD0_CH2_IR	0x40520450	Interrupt Register. See CANFD0_CH0_IR for the details of bit fields.
CANFD0_CH2_IE	0x40520454	Interrupt Enable. See CANFD0_CH0_IE for the details of bit fields.
CANFD0_CH2_ILS	0x40520458	Interrupt Line Select. See CANFD0_CH0_ILS for the details of bit fields.
CANFD0_CH2_ILE	0x4052045C	Interrupt Line Enable. See CANFD0_CH0_ILE for the details of bit fields.
CANFD0_CH2_GFC	0x40520480	Global Filter Configuration. See CANFD0_CH0_GFC for the details of bit fields.
CANFD0_CH2_SIDFC	0x40520484	Standard ID Filter Configuration. See CANFD0_CH0_SIDFC for the details of bit fields.
CANFD0_CH2_XIDFC	0x40520488	Extended ID Filter Configuration. See CANFD0_CH0_XIDFC for the details of bit fields.
CANFD0_CH2_XIDAM	0x40520490	Extended ID AND Mask. See CANFD0_CH0_XIDAM for the details of bit fields.

Register name	Address	Description
CANFD0_CH2_HPMS	0x40520494	High Priority Message Status. See CANFD0_CH0_HPMS for the details of bit fields.
CANFD0_CH2_NDAT1	0x40520498	New Data 1. See CANFD0_CH0_NDAT1 for the details of bit fields.
CANFD0_CH2_NDAT2	0x4052049C	New Data 2. See CANFD0_CH0_NDAT2 for the details of bit fields.
CANFD0_CH2_RXF0C	0x405204A0	Rx FIFO 0 Configuration. See CANFD0_CH0_RXF0C for the details of bit fields.
CANFD0_CH2_RXF0S	0x405204A4	Rx FIFO 0 Status. See CANFD0_CH0_RXF0S for the details of bit fields.
CANFD0_CH2_RXF0A	0x405204A8	Rx FIFO 0 Acknowledge. See CANFD0_CH0_RXF0A for the details of bit fields.
CANFD0_CH2_RXBC	0x405204AC	Rx Buffer Configuration. See CANFD0_CH0_RXBC for the details of bit fields.
CANFD0_CH2_RXF1C	0x405204B0	Rx FIFO 1 Configuration. See CANFD0_CH0_RXF1C for the details of bit fields.
CANFD0_CH2_RXF1S	0x405204B4	Rx FIFO 1 Status. See CANFD0_CH0_RXF1S for the details of bit fields.
CANFD0_CH2_RXF1A	0x405204B8	Rx FIFO 1 Acknowledge. See CANFD0_CH0_RXF1A for the details of bit fields.
CANFD0_CH2_RXESC	0x405204BC	Rx Buffer / FIFO Element Size Configuration. See CANFD0_CH0_RXESC for the details of bit fields.
CANFD0_CH2_TXBC	0x405204C0	Tx Buffer Configuration. See CANFD0_CH0_TXBC for the details of bit fields.
CANFD0_CH2_TXFQS	0x405204C4	Tx FIFO/Queue Status. See CANFD0_CH0_TXFQS for the details of bit fields.
CANFD0_CH2_TXESC	0x405204C8	Tx Buffer Element Size Configuration. See CANFD0_CH0_TXESC for the details of bit fields.
CANFD0_CH2_TXBRP	0x405204CC	Tx Buffer Request Pending. See CANFD0_CH0_TXBRP for the details of bit fields.
CANFD0_CH2_TXBAR	0x405204D0	Tx Buffer Add Request. See CANFD0_CH0_TXBAR for the details of bit fields.
CANFD0_CH2_TXBCR	0x405204D4	Tx Buffer Cancellation Request. See CANFD0_CH0_TXBCR for the details of bit fields.
CANFD0_CH2_TXBTO	0x405204D8	Tx Buffer Transmission Occurred. See CANFD0_CH0_TXBTO for the details of bit fields.
CANFD0_CH2_TXBCF	0x405204DC	Tx Buffer Cancellation Finished. See CANFD0_CH0_TXBCF for the details of bit fields.
CANFD0_CH2_TXBTIE	0x405204E0	Tx Buffer Transmission Interrupt Enable. See CANFD0_CH0_TXBTIE for the details of bit fields.
CANFD0_CH2_TXBCIE	0x405204E4	Tx Buffer Cancellation Finished Interrupt Enable. See CANFD0_CH0_TXBCIE for the details of bit fields.
CANFD0_CH2_TXEFC	0x405204F0	Tx Event FIFO Configuration. See CANFD0_CH0_TXEFC for the details of bit fields.

Register name	Address	Description
CANFD0_CH2_TXEFS	0x405204F4	Tx Event FIFO Status. See CANFD0_CH0_TXEFS for the details of bit fields.
CANFD0_CH2_TXEFA	0x405204F8	Tx Event FIFO Acknowledge. See CANFD0_CH0_TXEFA for the details of bit fields.
CANFD0_CH2_TTTMC	0x40520500	TT Trigger Memory Configuration. See CANFD0_CH0_TTTMC for the details of bit fields.
CANFD0_CH2_TTRMC	0x40520504	TT Reference Message Configuration. See CANFD0_CH0_TTRMC for the details of bit fields.
CANFD0_CH2_TTOCF	0x40520508	TT Operation Configuration. See CANFD0_CH0_TTOCF for the details of bit fields.
CANFD0_CH2_TTMLM	0x4052050C	TT Matrix Limits. See CANFD0_CH0_TTMLM for the details of bit fields.
CANFD0_CH2_TURCF	0x40520510	TUR Configuration. See CANFD0_CH0_TURCF for the details of bit fields.
CANFD0_CH2_TTOCN	0x40520514	TT Operation Control. See CANFD0_CH0_TTOCN for the details of bit fields.
CANFD0_CH2_TTGTP	0x40520518	TT Global Time Preset. See CANFD0_CH0_TTGTP for the details of bit fields.
CANFD0_CH2_TTTMK	0x4052051C	TT Time Mark. See CANFD0_CH0_TTTMK for the details of bit fields.
CANFD0_CH2_TTIR	0x40520520	TT Interrupt Register. See CANFD0_CH0_TTIR for the details of bit fields.
CANFD0_CH2_TTIE	0x40520524	TT Interrupt Enable. See CANFD0_CH0_TTIE for the details of bit fields.
CANFD0_CH2_TTILS	0x40520528	TT Interrupt Line Select. See CANFD0_CH0_TTILS for the details of bit fields.
CANFD0_CH2_TTOST	0x4052052C	TT Operation Status. See CANFD0_CH0_TTOST for the details of bit fields.
CANFD0_CH2_TURNA	0x40520530	TUR Numerator Actual. See CANFD0_CH0_TURNA for the details of bit fields.
CANFD0_CH2_TTLGT	0x40520534	TT Local & Global Time. See CANFD0_CH0_TTLGT for the details of bit fields.
CANFD0_CH2_TTCTC	0x40520538	TT Cycle Time & Count. See CANFD0_CH0_TTCTC for the details of bit fields.
CANFD0_CH2_TTCPT	0x4052053C	TT Capture Time. See CANFD0_CH0_TTCPT for the details of bit fields.
CANFD0_CH2_TTCSM	0x40520540	TT Cycle Sync Mark. See CANFD0_CH0_TTCSM for the details of bit fields.
CANFD0_CH2_RXFTOP_CTL	0x40520580	Receive FIFO Top control. See CANFD0_CH0_RXFTOP_CTL for the details of bit fields.
CANFD0_CH2_RXFTOP0_STAT	0x405205A0	Receive FIFO 0 Top Status. See CANFD0_CH0_RXFTOP0_STAT for the details of bit fields.
CANFD0_CH2_RXFTOP0_DATA	0x405205A8	Receive FIFO 0 Top Data. See CANFD0_CH0_RXFTOP0_DATA for the details of bit fields.

Register name	Address	Description
CANFD0_CH2_RXFTOP1_STAT	0x405205B0	Receive FIFO 1 Top Status. See CANFD0_CH0_RXFTOP1_STAT for the details of bit fields.
CANFD0_CH2_RXFTOP1_DATA	0x405205B8	Receive FIFO 1 Top Data. See CANFD0_CH0_RXFTOP1_DATA for the details of bit fields.
CANFD0_CTL	0x40521000	Global CAN control register
CANFD0_STATUS	0x40521004	Global CAN status register
CANFD0_INTR0_CAUSE	0x40521010	Consolidated interrupt0 cause register
CANFD0_INTR1_CAUSE	0x40521014	Consolidated interrupt1 cause register
CANFD0_TS_CTL	0x40521020	Time Stamp control register
CANFD0_TS_CNT	0x40521024	Time Stamp counter value
CANFD0_ECC_CTL	0x40521080	ECC control
CANFD0_ECC_ERR_INJ	0x40521084	ECC error injection
CANFD1_CH0_CREL	0x40540000	Core Release Register. See CANFD0_CH0_CREL for the details of bit fields.
CANFD1_CH0_ENDN	0x40540004	Endian Register. See CANFD0_CH0_ENDN for the details of bit fields.
CANFD1_CH0_DBTP	0x4054000C	Data Bit Timing & Prescaler Register. See CANFD0_CH0_DBTP for the details of bit fields.
CANFD1_CH0_TEST	0x40540010	Test Register. See CANFD0_CH0_TEST for the details of bit fields.
CANFD1_CH0_RWD	0x40540014	RAM Watchdog. See CANFD0_CH0_RWD for the details of bit fields.
CANFD1_CH0_CCCR	0x40540018	CC Control Register. See CANFD0_CH0_CCCR for the details of bit fields.
CANFD1_CH0_NBTP	0x4054001C	Nominal Bit Timing & Prescaler Register. See CANFD0_CH0_NBTP for the details of bit fields.
CANFD1_CH0_TSCC	0x40540020	Timestamp Counter Configuration. See CANFD0_CH0_TSCC for the details of bit fields.
CANFD1_CH0_TSCV	0x40540024	Timestamp Counter Value. See CANFD0_CH0_TSCV for the details of bit fields.
CANFD1_CH0_TOCC	0x40540028	Timeout Counter Configuration. See CANFD0_CH0_TOCC for the details of bit fields.
CANFD1_CH0_TOCV	0x4054002C	Timeout Counter Value. See CANFD0_CH0_TOCV for the details of bit fields.
CANFD1_CH0_ECR	0x40540040	Error Counter Register. See CANFD0_CH0_ECR for the details of bit fields.
CANFD1_CH0_PSR	0x40540044	Protocol Status Register. See CANFD0_CH0_PSR for the details of bit fields.
CANFD1_CH0_TDCR	0x40540048	Transmitter Delay Compensation Register. See CANFD0_CH0_TDCR for the details of bit fields.
CANFD1_CH0_IR	0x40540050	Interrupt Register. See CANFD0_CH0_IR for the details of bit fields.

Register name	Address	Description
CANFD1_CH0_IE	0x40540054	Interrupt Enable. See CANFD0_CH0_IE for the details of bit fields.
CANFD1_CH0_ILS	0x40540058	Interrupt Line Select. See CANFD0_CH0_ILS for the details of bit fields.
CANFD1_CH0_ILE	0x4054005C	Interrupt Line Enable. See CANFD0_CH0_ILE for the details of bit fields.
CANFD1_CH0_GFC	0x40540080	Global Filter Configuration. See CANFD0_CH0_GFC for the details of bit fields.
CANFD1_CH0_SIDFC	0x40540084	Standard ID Filter Configuration. See CANFD0_CH0_SIDFC for the details of bit fields.
CANFD1_CH0_XIDFC	0x40540088	Extended ID Filter Configuration. See CANFD0_CH0_XIDFC for the details of bit fields.
CANFD1_CH0_XIDAM	0x40540090	Extended ID AND Mask. See CANFD0_CH0_XIDAM for the details of bit fields.
CANFD1_CH0_HPMS	0x40540094	High Priority Message Status. See CANFD0_CH0_HPMS for the details of bit fields.
CANFD1_CH0_NDAT1	0x40540098	New Data 1. See CANFD0_CH0_NDAT1 for the details of bit fields.
CANFD1_CH0_NDAT2	0x4054009C	New Data 2. See CANFD0_CH0_NDAT2 for the details of bit fields.
CANFD1_CH0_RXF0C	0x405400A0	Rx FIFO 0 Configuration. See CANFD0_CH0_RXF0C for the details of bit fields.
CANFD1_CH0_RXF0S	0x405400A4	Rx FIFO 0 Status. See CANFD0_CH0_RXF0S for the details of bit fields.
CANFD1_CH0_RXF0A	0x405400A8	Rx FIFO 0 Acknowledge. See CANFD0_CH0_RXF0A for the details of bit fields.
CANFD1_CH0_RXBC	0x405400AC	Rx Buffer Configuration. See CANFD0_CH0_RXBC for the details of bit fields.
CANFD1_CH0_RXF1C	0x405400B0	Rx FIFO 1 Configuration. See CANFD0_CH0_RXF1C for the details of bit fields.
CANFD1_CH0_RXF1S	0x405400B4	Rx FIFO 1 Status. See CANFD0_CH0_RXF1S for the details of bit fields.
CANFD1_CH0_RXF1A	0x405400B8	Rx FIFO 1 Acknowledge. See CANFD0_CH0_RXF1A for the details of bit fields.
CANFD1_CH0_RXESC	0x405400BC	Rx Buffer / FIFO Element Size Configuration. See CANFD0_CH0_RXESC for the details of bit fields.
CANFD1_CH0_TXBC	0x405400C0	Tx Buffer Configuration. See CANFD0_CH0_TXBC for the details of bit fields.
CANFD1_CH0_TXFQS	0x405400C4	Tx FIFO/Queue Status. See CANFD0_CH0_TXFQS for the details of bit fields.
CANFD1_CH0_TXESC	0x405400C8	Tx Buffer Element Size Configuration. See CANFD0_CH0_TXESC for the details of bit fields.
CANFD1_CH0_TXBRP	0x405400CC	Tx Buffer Request Pending. See CANFD0_CH0_TXBRP for the details of bit fields.

Register name	Address	Description
CANFD1_CH0_TXBAR	0x405400D0	Tx Buffer Add Request. See CANFD0_CH0_TXBAR for the details of bit fields.
CANFD1_CH0_TXBCR	0x405400D4	Tx Buffer Cancellation Request. See CANFD0_CH0_TXBCR for the details of bit fields.
CANFD1_CH0_TXBTO	0x405400D8	Tx Buffer Transmission Occurred. See CANFD0_CH0_TXBTO for the details of bit fields.
CANFD1_CH0_TXBCF	0x405400DC	Tx Buffer Cancellation Finished. See CANFD0_CH0_TXBCF for the details of bit fields.
CANFD1_CH0_TXBTIE	0x405400E0	Tx Buffer Transmission Interrupt Enable. See CANFD0_CH0_TXBTIE for the details of bit fields.
CANFD1_CH0_TXBCIE	0x405400E4	Tx Buffer Cancellation Finished Interrupt Enable. See CANFD0_CH0_TXBCIE for the details of bit fields.
CANFD1_CH0_TXEFC	0x405400F0	Tx Event FIFO Configuration. See CANFD0_CH0_TXEFC for the details of bit fields.
CANFD1_CH0_TXEFS	0x405400F4	Tx Event FIFO Status. See CANFD0_CH0_TXEFS for the details of bit fields.
CANFD1_CH0_TXEFA	0x405400F8	Tx Event FIFO Acknowledge. See CANFD0_CH0_TXEFA for the details of bit fields.
CANFD1_CH0_TTTMC	0x40540100	TT Trigger Memory Configuration. See CANFD0_CH0_TTTMC for the details of bit fields.
CANFD1_CH0_TTRMC	0x40540104	TT Reference Message Configuration. See CANFD0_CH0_TTRMC for the details of bit fields.
CANFD1_CH0_TTOCF	0x40540108	TT Operation Configuration. See CANFD0_CH0_TTOCF for the details of bit fields.
CANFD1_CH0_TTMLM	0x4054010C	TT Matrix Limits. See CANFD0_CH0_TTMLM for the details of bit fields.
CANFD1_CH0_TURCF	0x40540110	TUR Configuration. See CANFD0_CH0_TURCF for the details of bit fields.
CANFD1_CH0_TTOCN	0x40540114	TT Operation Control. See CANFD0_CH0_TTOCN for the details of bit fields.
CANFD1_CH0_TTGTP	0x40540118	TT Global Time Preset. See CANFD0_CH0_TTGTP for the details of bit fields.
CANFD1_CH0_TTTMK	0x4054011C	TT Time Mark. See CANFD0_CH0_TTTMK for the details of bit fields.
CANFD1_CH0_TTIR	0x40540120	TT Interrupt Register. See CANFD0_CH0_TTIR for the details of bit fields.
CANFD1_CH0_TTIE	0x40540124	TT Interrupt Enable. See CANFD0_CH0_TTIE for the details of bit fields.
CANFD1_CH0_TTILS	0x40540128	TT Interrupt Line Select. See CANFD0_CH0_TTILS for the details of bit fields.
CANFD1_CH0_TTOST	0x4054012C	TT Operation Status. See CANFD0_CH0_TTOST for the details of bit fields.
CANFD1_CH0_TURNA	0x40540130	TUR Numerator Actual. See CANFD0_CH0_TURNA for the details of bit fields.

Register name	Address	Description
CANFD1_CH0_TTLGT	0x40540134	TT Local & Global Time. See CANFD0_CH0_TTLGT for the details of bit fields.
CANFD1_CH0_TTCTC	0x40540138	TT Cycle Time & Count. See CANFD0_CH0_TTCTC for the details of bit fields.
CANFD1_CH0_TTCPT	0x4054013C	TT Capture Time. See CANFD0_CH0_TTCPT for the details of bit fields.
CANFD1_CH0_TTCSM	0x40540140	TT Cycle Sync Mark. See CANFD0_CH0_TTCSM for the details of bit fields.
CANFD1_CH0_RXFTOP_CTL	0x40540180	Receive FIFO Top control. See CANFD0_CH0_RXFTOP_CTL for the details of bit fields.
CANFD1_CH0_RXFTOP0_STAT	0x405401A0	Receive FIFO 0 Top Status. See CANFD0_CH0_RXFTOP0_STAT for the details of bit fields.
CANFD1_CH0_RXFTOP0_DATA	0x405401A8	Receive FIFO 0 Top Data. See CANFD0_CH0_RXFTOP0_DATA for the details of bit fields.
CANFD1_CH0_RXFTOP1_STAT	0x405401B0	Receive FIFO 1 Top Status. See CANFD0_CH0_RXFTOP1_STAT for the details of bit fields.
CANFD1_CH0_RXFTOP1_DATA	0x405401B8	Receive FIFO 1 Top Data. See CANFD0_CH0_RXFTOP1_DATA for the details of bit fields.
CANFD1_CH1_CREL	0x40540200	Core Release Register. See CANFD0_CH0_CREL for the details of bit fields.
CANFD1_CH1_ENDN	0x40540204	Endian Register. See CANFD0_CH0_ENDN for the details of bit fields.
CANFD1_CH1_DBTP	0x4054020C	Data Bit Timing & Prescaler Register. See CANFD0_CH0_DBTP for the details of bit fields.
CANFD1_CH1_TEST	0x40540210	Test Register. See CANFD0_CH0_TEST for the details of bit fields.
CANFD1_CH1_RWD	0x40540214	RAM Watchdog. See CANFD0_CH0_RWD for the details of bit fields.
CANFD1_CH1_CCCR	0x40540218	CC Control Register. See CANFD0_CH0_CCCR for the details of bit fields.
CANFD1_CH1_NBTP	0x4054021C	Nominal Bit Timing & Prescaler Register. See CANFD0_CH0_NBTP for the details of bit fields.
CANFD1_CH1_TSCC	0x40540220	Timestamp Counter Configuration. See CANFD0_CH0_TSCC for the details of bit fields.
CANFD1_CH1_TSCV	0x40540224	Timestamp Counter Value. See CANFD0_CH0_TSCV for the details of bit fields.
CANFD1_CH1_TOCC	0x40540228	Timeout Counter Configuration. See CANFD0_CH0_TOCC for the details of bit fields.
CANFD1_CH1_TOCV	0x4054022C	Timeout Counter Value. See CANFD0_CH0_TOCV for the details of bit fields.
CANFD1_CH1_ECR	0x40540240	Error Counter Register. See CANFD0_CH0_ECR for the details of bit fields.

Register name	Address	Description
CANFD1_CH1_PSR	0x40540244	Protocol Status Register. See CANFD0_CH0_PSR for the details of bit fields.
CANFD1_CH1_TDCR	0x40540248	Transmitter Delay Compensation Register. See CANFD0_CH0_TDCR for the details of bit fields.
CANFD1_CH1_IR	0x40540250	Interrupt Register. See CANFD0_CH0_IR for the details of bit fields.
CANFD1_CH1_IE	0x40540254	Interrupt Enable. See CANFD0_CH0_IE for the details of bit fields.
CANFD1_CH1_ILS	0x40540258	Interrupt Line Select. See CANFD0_CH0_ILS for the details of bit fields.
CANFD1_CH1_ILE	0x4054025C	Interrupt Line Enable. See CANFD0_CH0_ILE for the details of bit fields.
CANFD1_CH1_GFC	0x40540280	Global Filter Configuration. See CANFD0_CH0_GFC for the details of bit fields.
CANFD1_CH1_SIDFC	0x40540284	Standard ID Filter Configuration. See CANFD0_CH0_SIDFC for the details of bit fields.
CANFD1_CH1_XIDFC	0x40540288	Extended ID Filter Configuration. See CANFD0_CH0_XIDFC for the details of bit fields.
CANFD1_CH1_XIDAM	0x40540290	Extended ID AND Mask. See CANFD0_CH0_XIDAM for the details of bit fields.
CANFD1_CH1_HPMS	0x40540294	High Priority Message Status. See CANFD0_CH0_HPMS for the details of bit fields.
CANFD1_CH1_NDAT1	0x40540298	New Data 1. See CANFD0_CH0_NDAT1 for the details of bit fields.
CANFD1_CH1_NDAT2	0x4054029C	New Data 2. See CANFD0_CH0_NDAT2 for the details of bit fields.
CANFD1_CH1_RXF0C	0x405402A0	Rx FIFO 0 Configuration. See CANFD0_CH0_RXF0C for the details of bit fields.
CANFD1_CH1_RXF0S	0x405402A4	Rx FIFO 0 Status. See CANFD0_CH0_RXF0S for the details of bit fields.
CANFD1_CH1_RXF0A	0x405402A8	Rx FIFO 0 Acknowledge. See CANFD0_CH0_RXF0A for the details of bit fields.
CANFD1_CH1_RXBC	0x405402AC	Rx Buffer Configuration. See CANFD0_CH0_RXBC for the details of bit fields.
CANFD1_CH1_RXF1C	0x405402B0	Rx FIFO 1 Configuration. See CANFD0_CH0_RXF1C for the details of bit fields.
CANFD1_CH1_RXF1S	0x405402B4	Rx FIFO 1 Status. See CANFD0_CH0_RXF1S for the details of bit fields.
CANFD1_CH1_RXF1A	0x405402B8	Rx FIFO 1 Acknowledge. See CANFD0_CH0_RXF1A for the details of bit fields.
CANFD1_CH1_RXESC	0x405402BC	Rx Buffer / FIFO Element Size Configuration. See CANFD0_CH0_RXESC for the details of bit fields.
CANFD1_CH1_TXBC	0x405402C0	Tx Buffer Configuration. See CANFD0_CH0_TXBC for the details of bit fields.

Register name	Address	Description
CANFD1_CH1_TXFQS	0x405402C4	Tx FIFO/Queue Status. See CANFD0_CH0_TXFQS for the details of bit fields.
CANFD1_CH1_TXESC	0x405402C8	Tx Buffer Element Size Configuration. See CANFD0_CH0_TXESC for the details of bit fields.
CANFD1_CH1_TXBRP	0x405402CC	Tx Buffer Request Pending. See CANFD0_CH0_TXBRP for the details of bit fields.
CANFD1_CH1_TXBAR	0x405402D0	Tx Buffer Add Request. See CANFD0_CH0_TXBAR for the details of bit fields.
CANFD1_CH1_TXBCR	0x405402D4	Tx Buffer Cancellation Request. See CANFD0_CH0_TXBCR for the details of bit fields.
CANFD1_CH1_TXBTO	0x405402D8	Tx Buffer Transmission Occurred. See CANFD0_CH0_TXBTO for the details of bit fields.
CANFD1_CH1_TXBCF	0x405402DC	Tx Buffer Cancellation Finished. See CANFD0_CH0_TXBCF for the details of bit fields.
CANFD1_CH1_TXBTIE	0x405402E0	Tx Buffer Transmission Interrupt Enable. See CANFD0_CH0_TXBTIE for the details of bit fields.
CANFD1_CH1_TXBCIE	0x405402E4	Tx Buffer Cancellation Finished Interrupt Enable. See CANFD0_CH0_TXBCIE for the details of bit fields.
CANFD1_CH1_TXEFC	0x405402F0	Tx Event FIFO Configuration. See CANFD0_CH0_TXEFC for the details of bit fields.
CANFD1_CH1_TXEFS	0x405402F4	Tx Event FIFO Status. See CANFD0_CH0_TXEFS for the details of bit fields.
CANFD1_CH1_TXEFA	0x405402F8	Tx Event FIFO Acknowledge. See CANFD0_CH0_TXEFA for the details of bit fields.
CANFD1_CH1_TTTMC	0x40540300	TT Trigger Memory Configuration. See CANFD0_CH0_TTTMC for the details of bit fields.
CANFD1_CH1_TTRMC	0x40540304	TT Reference Message Configuration. See CANFD0_CH0_TTRMC for the details of bit fields.
CANFD1_CH1_TTOCF	0x40540308	TT Operation Configuration. See CANFD0_CH0_TTOCF for the details of bit fields.
CANFD1_CH1_TTMLM	0x4054030C	TT Matrix Limits. See CANFD0_CH0_TTMLM for the details of bit fields.
CANFD1_CH1_TURCF	0x40540310	TUR Configuration. See CANFD0_CH0_TURCF for the details of bit fields.
CANFD1_CH1_TTOCN	0x40540314	TT Operation Control. See CANFD0_CH0_TTOCN for the details of bit fields.
CANFD1_CH1_TTGTP	0x40540318	TT Global Time Preset. See CANFD0_CH0_TTGTP for the details of bit fields.
CANFD1_CH1_TTTMK	0x4054031C	TT Time Mark. See CANFD0_CH0_TTTMK for the details of bit fields.
CANFD1_CH1_TTIR	0x40540320	TT Interrupt Register. See CANFD0_CH0_TTIR for the details of bit fields.
CANFD1_CH1_TTIE	0x40540324	TT Interrupt Enable. See CANFD0_CH0_TTIE for the details of bit fields.

Register name	Address	Description
CANFD1_CH1_TTILS	0x40540328	TT Interrupt Line Select. See CANFD0_CH0_TTILS for the details of bit fields.
CANFD1_CH1_TTOST	0x4054032C	TT Operation Status. See CANFD0_CH0_TTOST for the details of bit fields.
CANFD1_CH1_TURNA	0x40540330	TUR Numerator Actual. See CANFD0_CH0_TURNA for the details of bit fields.
CANFD1_CH1_TTLGT	0x40540334	TT Local & Global Time. See CANFD0_CH0_TTLGT for the details of bit fields.
CANFD1_CH1_TTCTC	0x40540338	TT Cycle Time & Count. See CANFD0_CH0_TTCTC for the details of bit fields.
CANFD1_CH1_TTCPT	0x4054033C	TT Capture Time. See CANFD0_CH0_TTCPT for the details of bit fields.
CANFD1_CH1_TTCSM	0x40540340	TT Cycle Sync Mark. See CANFD0_CH0_TTCSM for the details of bit fields.
CANFD1_CH1_RXFTOP_CTL	0x40540380	Receive FIFO Top control. See CANFD0_CH0_RXFTOP_CTL for the details of bit fields.
CANFD1_CH1_RXFTOP0_STAT	0x405403A0	Receive FIFO 0 Top Status. See CANFD0_CH0_RXFTOP0_STAT for the details of bit fields.
CANFD1_CH1_RXFTOP0_DATA	0x405403A8	Receive FIFO 0 Top Data. See CANFD0_CH0_RXFTOP0_DATA for the details of bit fields.
CANFD1_CH1_RXFTOP1_STAT	0x405403B0	Receive FIFO 1 Top Status. See CANFD0_CH0_RXFTOP1_STAT for the details of bit fields.
CANFD1_CH1_RXFTOP1_DATA	0x405403B8	Receive FIFO 1 Top Data. See CANFD0_CH0_RXFTOP1_DATA for the details of bit fields.
CANFD1_CH2_CREL	0x40540400	Core Release Register. See CANFD0_CH0_CREL for the details of bit fields.
CANFD1_CH2_ENDN	0x40540404	Endian Register. See CANFD0_CH0_ENDN for the details of bit fields.
CANFD1_CH2_DBTP	0x4054040C	Data Bit Timing & Prescaler Register. See CANFD0_CH0_DBTP for the details of bit fields.
CANFD1_CH2_TEST	0x40540410	Test Register. See CANFD0_CH0_TEST for the details of bit fields.
CANFD1_CH2_RWD	0x40540414	RAM Watchdog. See CANFD0_CH0_RWD for the details of bit fields.
CANFD1_CH2_CCCR	0x40540418	CC Control Register. See CANFD0_CH0_CCCR for the details of bit fields.
CANFD1_CH2_NBTP	0x4054041C	Nominal Bit Timing & Prescaler Register. See CANFD0_CH0_NBTP for the details of bit fields.
CANFD1_CH2_TSCC	0x40540420	Timestamp Counter Configuration. See CANFD0_CH0_TSCC for the details of bit fields.
CANFD1_CH2_TSCV	0x40540424	Timestamp Counter Value. See CANFD0_CH0_TSCV for the details of bit fields.

Register name	Address	Description
CANFD1_CH2_TOCC	0x40540428	Timeout Counter Configuration. See CANFD0_CH0_TOCC for the details of bit fields.
CANFD1_CH2_TOCV	0x4054042C	Timeout Counter Value. See CANFD0_CH0_TOCV for the details of bit fields.
CANFD1_CH2_ECR	0x40540440	Error Counter Register. See CANFD0_CH0_ECR for the details of bit fields.
CANFD1_CH2_PSR	0x40540444	Protocol Status Register. See CANFD0_CH0_PSR for the details of bit fields.
CANFD1_CH2_TDCR	0x40540448	Transmitter Delay Compensation Register. See CANFD0_CH0_TDCR for the details of bit fields.
CANFD1_CH2_IR	0x40540450	Interrupt Register. See CANFD0_CH0_IR for the details of bit fields.
CANFD1_CH2_IE	0x40540454	Interrupt Enable. See CANFD0_CH0_IE for the details of bit fields.
CANFD1_CH2_ILS	0x40540458	Interrupt Line Select. See CANFD0_CH0_ILS for the details of bit fields.
CANFD1_CH2_ILE	0x4054045C	Interrupt Line Enable. See CANFD0_CH0_ILE for the details of bit fields.
CANFD1_CH2_GFC	0x40540480	Global Filter Configuration. See CANFD0_CH0_GFC for the details of bit fields.
CANFD1_CH2_SIDFC	0x40540484	Standard ID Filter Configuration. See CANFD0_CH0_SIDFC for the details of bit fields.
CANFD1_CH2_XIDFC	0x40540488	Extended ID Filter Configuration. See CANFD0_CH0_XIDFC for the details of bit fields.
CANFD1_CH2_XIDAM	0x40540490	Extended ID AND Mask. See CANFD0_CH0_XIDAM for the details of bit fields.
CANFD1_CH2_HPMS	0x40540494	High Priority Message Status. See CANFD0_CH0_HPMS for the details of bit fields.
CANFD1_CH2_NDAT1	0x40540498	New Data 1. See CANFD0_CH0_NDAT1 for the details of bit fields.
CANFD1_CH2_NDAT2	0x4054049C	New Data 2. See CANFD0_CH0_NDAT2 for the details of bit fields.
CANFD1_CH2_RXF0C	0x405404A0	Rx FIFO 0 Configuration. See CANFD0_CH0_RXF0C for the details of bit fields.
CANFD1_CH2_RXF0S	0x405404A4	Rx FIFO 0 Status. See CANFD0_CH0_RXF0S for the details of bit fields.
CANFD1_CH2_RXF0A	0x405404A8	Rx FIFO 0 Acknowledge. See CANFD0_CH0_RXF0A for the details of bit fields.
CANFD1_CH2_RXBC	0x405404AC	Rx Buffer Configuration. See CANFD0_CH0_RXBC for the details of bit fields.
CANFD1_CH2_RXF1C	0x405404B0	Rx FIFO 1 Configuration. See CANFD0_CH0_RXF1C for the details of bit fields.
CANFD1_CH2_RXF1S	0x405404B4	Rx FIFO 1 Status. See CANFD0_CH0_RXF1S for the details of bit fields.

Register name	Address	Description
CANFD1_CH2_RXF1A	0x405404B8	Rx FIFO 1 Acknowledge. See CANFD0_CH0_RXF1A for the details of bit fields.
CANFD1_CH2_RXESC	0x405404BC	Rx Buffer / FIFO Element Size Configuration. See CANFD0_CH0_RXESC for the details of bit fields.
CANFD1_CH2_TXBC	0x405404C0	Tx Buffer Configuration. See CANFD0_CH0_TXBC for the details of bit fields.
CANFD1_CH2_TXFQS	0x405404C4	Tx FIFO/Queue Status. See CANFD0_CH0_TXFQS for the details of bit fields.
CANFD1_CH2_TXESC	0x405404C8	Tx Buffer Element Size Configuration. See CANFD0_CH0_TXESC for the details of bit fields.
CANFD1_CH2_TXBRP	0x405404CC	Tx Buffer Request Pending. See CANFD0_CH0_TXBRP for the details of bit fields.
CANFD1_CH2_TXBAR	0x405404D0	Tx Buffer Add Request. See CANFD0_CH0_TXBAR for the details of bit fields.
CANFD1_CH2_TXBCR	0x405404D4	Tx Buffer Cancellation Request. See CANFD0_CH0_TXBCR for the details of bit fields.
CANFD1_CH2_TXBTO	0x405404D8	Tx Buffer Transmission Occurred. See CANFD0_CH0_TXBTO for the details of bit fields.
CANFD1_CH2_TXBCF	0x405404DC	Tx Buffer Cancellation Finished. See CANFD0_CH0_TXBCF for the details of bit fields.
CANFD1_CH2_TXBTIE	0x405404E0	Tx Buffer Transmission Interrupt Enable. See CANFD0_CH0_TXBTIE for the details of bit fields.
CANFD1_CH2_TXBCIE	0x405404E4	Tx Buffer Cancellation Finished Interrupt Enable. See CANFD0_CH0_TXBCIE for the details of bit fields.
CANFD1_CH2_TXEFC	0x405404F0	Tx Event FIFO Configuration. See CANFD0_CH0_TXEFC for the details of bit fields.
CANFD1_CH2_TXEFS	0x405404F4	Tx Event FIFO Status. See CANFD0_CH0_TXEFS for the details of bit fields.
CANFD1_CH2_TXEFA	0x405404F8	Tx Event FIFO Acknowledge. See CANFD0_CH0_TXEFA for the details of bit fields.
CANFD1_CH2_TTTMC	0x40540500	TT Trigger Memory Configuration. See CANFD0_CH0_TTTMC for the details of bit fields.
CANFD1_CH2_TTRMC	0x40540504	TT Reference Message Configuration. See CANFD0_CH0_TTRMC for the details of bit fields.
CANFD1_CH2_TTOCF	0x40540508	TT Operation Configuration. See CANFD0_CH0_TTOCF for the details of bit fields.
CANFD1_CH2_TTMLM	0x4054050C	TT Matrix Limits. See CANFD0_CH0_TTMLM for the details of bit fields.
CANFD1_CH2_TURCF	0x40540510	TUR Configuration. See CANFD0_CH0_TURCF for the details of bit fields.
CANFD1_CH2_TTOCN	0x40540514	TT Operation Control. See CANFD0_CH0_TTOCN for the details of bit fields.
CANFD1_CH2_TTGTP	0x40540518	TT Global Time Preset. See CANFD0_CH0_TTGTP for the details of bit fields.

Register name	Address	Description
CANFD1_CH2_TTTMK	0x4054051C	TT Time Mark. See CANFD0_CH0_TTTMK for the details of bit fields.
CANFD1_CH2_TTIR	0x40540520	TT Interrupt Register. See CANFD0_CH0_TTIR for the details of bit fields.
CANFD1_CH2_TTIE	0x40540524	TT Interrupt Enable. See CANFD0_CH0_TTIE for the details of bit fields.
CANFD1_CH2_TTILS	0x40540528	TT Interrupt Line Select. See CANFD0_CH0_TTILS for the details of bit fields.
CANFD1_CH2_TTOST	0x4054052C	TT Operation Status. See CANFD0_CH0_TTOST for the details of bit fields.
CANFD1_CH2_TURNA	0x40540530	TUR Numerator Actual. See CANFD0_CH0_TURNA for the details of bit fields.
CANFD1_CH2_TTLGT	0x40540534	TT Local & Global Time. See CANFD0_CH0_TTLGT for the details of bit fields.
CANFD1_CH2_TTCTC	0x40540538	TT Cycle Time & Count. See CANFD0_CH0_TTCTC for the details of bit fields.
CANFD1_CH2_TTCPT	0x4054053C	TT Capture Time. See CANFD0_CH0_TTCPT for the details of bit fields.
CANFD1_CH2_TTCSM	0x40540540	TT Cycle Sync Mark. See CANFD0_CH0_TTCSM for the details of bit fields.
CANFD1_CH2_RXFTOP_CTL	0x40540580	Receive FIFO Top control. See CANFD0_CH0_RXFTOP_CTL for the details of bit fields.
CANFD1_CH2_RXFTOP0_STAT	0x405405A0	Receive FIFO 0 Top Status. See CANFD0_CH0_RXFTOP0_STAT for the details of bit fields.
CANFD1_CH2_RXFTOP0_DATA	0x405405A8	Receive FIFO 0 Top Data. See CANFD0_CH0_RXFTOP0_DATA for the details of bit fields.
CANFD1_CH2_RXFTOP1_STAT	0x405405B0	Receive FIFO 1 Top Status. See CANFD0_CH0_RXFTOP1_STAT for the details of bit fields.
CANFD1_CH2_RXFTOP1_DATA	0x405405B8	Receive FIFO 1 Top Data. See CANFD0_CH0_RXFTOP1_DATA for the details of bit fields.
CANFD1_CTL	0x40541000	Global CAN control register. See CANFD0_CTL for the details of bit fields.
CANFD1_STATUS	0x40541004	Global CAN status register. See CANFD0_STATUS for the details of bit fields.
CANFD1_INTR0_CAUSE	0x40541010	Consolidated interrupt0 cause register. See CANFD0_INTR0_CAUSE for the details of bit fields.
CANFD1_INTR1_CAUSE	0x40541014	Consolidated interrupt1 cause register. See CANFD0_INTR1_CAUSE for the details of bit fields.
CANFD1_ECC_CTL	0x40541080	ECC control. See CANFD0_ECC_CTL for the details of bit fields.
CANFD1_ECC_ERR_INJ	0x40541084	ECC error injection. See CANFD0_ECC_ERR_INJ for the details of bit fields.

12.1 CANFD registers

CANFD0_CH0_CREL

Core Release Register
Address: 0x40520000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	DAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	MON [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	R				R			
Name	SUBSTEP [23:20]				YEAR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			
HW Access	R				R			
Name	REL [31:28]				STEP [27:24]			

Bits	Name	Description
31 : 28	REL	Core Release One digit, BCD-coded. Default Value: 0x3
27 : 24	STEP	Step of Core Release One digit, BCD-coded. Default Value: 0x2
23 : 20	SUBSTEP	Sub-step of Core Release One digit, BCD-coded. Default Value: 0x3
19 : 16	YEAR	Time Stamp Year One digit, BCD-coded. This field is set by generic parameter on M_TTCAN synthesis. Default Value: 0x8
15 : 8	MON	Time Stamp Month Two digits, BCD-coded. This field is set by generic parameter on M_TTCAN synthesis. Default Value: 0x06
7 : 0	DAY	Time Stamp Day Two digits, BCD-coded. This field is set by generic parameter on M_TTCAN synthesis. Default Value: 0x09

CANFD0_CH0_ENDN

Endian Register
Address: 0x40520004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	ETV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ETV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ETV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ETV [31:24]							

Bits	Name	Description
31 : 0	ETV	Endianness Test Value The endianness test value is 0x87654321. Default Value: 0x87654321

CANFD0_CH0_DBTP

Data Bit Timing & Prescaler Register
Address: 0x4052000C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DTSEG2 [7:4]				DSJW [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			DTSEG1 [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None		RW				
HW Access	R	None		R				
Name	TDC	None [22:21]		DBRP [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	TDC	Transmitter Delay Compensation 0= Transmitter Delay Compensation disabled 1= Transmitter Delay Compensation enabled Default Value: 0
20 : 16	DBRP	Data Bit Rate Prescaler 0x00-0x1F The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Bit Rate Prescaler are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Default Value: 0
12 : 8	DTSEG1	Data time segment before sample point 0x00-0x1F Valid values are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Default Value: 0xA

7 : 4	DTSEG2	Data time segment after sample point 0x0-0xF Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Default Value: 3
3 : 0	DSJW	Data (Re)Synchronization Jump Width 0x0-0xF Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Default Value: 3

CANFD0_CH0_TEST

Test Register
Address: 0x40520010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	RW		RW	RW	RW	RW	RW
HW Access	R	R		R	R	R	R	R
Name	RX	TX [6:5]		LBCK	CAT	CAM	TAT	TAM

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	RX	Receive Pin Monitors the actual value of pin m_ttcan_rx 0= The CAN bus is dominant (m_ttcan_rx = '0') 1= The CAN bus is recessive (m_ttcan_rx = '1') Default Value: Undefined
6 : 5	TX	Control of Transmit Pin 00 Reset value, m_ttcan_tx controlled by the CAN Core, updated at the end of the CAN bit time 01 Sample Point can be monitored at pin m_ttcan_tx 10 Dominant ('0') level at pin m_ttcan_tx 11 Recessive ('1') at pin m_ttcan_tx Default Value: 0
4	LBCK	Loop Back Mode 0= Reset value, Loop Back Mode is disabled 1= Loop Back Mode is enabled (see Section 3.1.9, Test Modes) Default Value: 0

3	CAT	ASC is not supported by M_TTCAN Check ASC Transmit Control Monitors level at output pin m_ttcan_asct. 0= Output pin m_ttcan_asct = '0' Default Value: 0
2	CAM	ASC is not supported by M_TTCAN Check ASC Multiplexer Control Monitors level at output pin m_ttcan_ascm. 0= Output pin m_ttcan_ascm = '0' 1= Output pin m_ttcan_ascm = '1' Default Value: 0
1	TAT	ASC is not supported by M_TTCAN Test ASC Transmit Control Controls output pin m_ttcan_asct in test mode, ORed with the signal from the FSE 0= Level at pin m_ttcan_asct controlled by FSE 1= Level at pin m_ttcan_asct = '1' Default Value: 0
0	TAM	ASC is not supported by M_TTCAN Test ASC Multiplexer Control Controls output pin m_ttcan_ascm in test mode, ORed with the signal from the FSE 0= Level at pin m_ttcan_ascm controlled by FSE 1= Level at pin m_ttcan_ascm = '1' Default Value: 0

CANFD0_CH0_RWD

RAM Watchdog
Address: 0x40520014
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WDC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	WDV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	WDV	Watchdog Value Actual Message RAM Watchdog Counter Value. Default Value: 0
7 : 0	WDC	Watchdog Configuration Start value of the Message RAM Watchdog Counter. With the reset value of '00' the counter is disabled. Default Value: 0

CANFD0_CH0_CCCR

CC Control Register
Address: 0x40520018
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	TEST	DAR	MON_	CSR	CSA	ASM	CCE	INIT

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	None		RW	RW
HW Access	R	R	R	R	None		R	R
Name	NISO	TXP	EFBI	PXHD	None [11:10]		BRSE	FDOE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	NISO	Non ISO Operation If this bit is set, the M_TTCAN uses the CAN FD frame format as specified by the Bosch CAN FD Specification V1.0. 0= CAN FD frame format according to ISO 11898-1:2015 1= CAN FD frame format according to Bosch CAN FD Specification V1.0 addressing the non-ISO CAN FD Default Value: 0
14	TXP	Transmit Pause If this bit is set, the M_TTCAN pauses for two CAN bit times before starting the next transmission after itself has successfully transmitted a frame (see Section 3.5). 0= Transmit pause disabled 1= Transmit pause enabled Default Value: 0
13	EFBI	Edge Filtering during Bus Integration 0= Edge filtering disabled 1= Two consecutive dominant tq required to detect an edge for hard synchronization Default Value: 0

12	PXHD	Protocol Exception Handling Disable 0= Protocol exception handling enabled 1= Protocol exception handling disabled Default Value: 0
9	BRSE	Bit Rate Switch Enable 0= Bit rate switching for transmissions disabled 1= Bit rate switching for transmissions enabled Default Value: 0
8	FDOE	FD Operation Enable 0= FD operation disabled 1= FD operation enabled Default Value: 0
7	TEST	Test Mode Enable 0= Normal operation, register TEST holds reset values 1= Test Mode, write access to register TEST enabled Default Value: 0
6	DAR	Disable Automatic Retransmission 0= Automatic retransmission of messages not transmitted successfully enabled 1= Automatic retransmission disabled Default Value: 0
5	MON_	Bus Monitoring Mode Bit MON can only be set by the Host when both CCE and INIT are set to '1'. The bit can be reset by the Host at any time. 0= Bus Monitoring Mode is disabled 1= Bus Monitoring Mode is enabled Default Value: 0
4	CSR	Clock Stop Request, not supported by M_TTCAN use CTL.STOP_REQ at the group level instead. 0= No clock stop is requested 1= Clock stop requested. When clock stop is requested, first INIT and then CSA will be set after all pending transfer requests have been completed and the CAN bus reached idle. Default Value: 0
3	CSA	Clock Stop Acknowledge 0= No clock stop acknowledged 1= M_TTCAN may be set in power down by stopping m_ttcan_hclk and m_ttcan_cclk Default Value: 0

2	ASM	Restricted Operation Mode Bit ASM can only be set by the Host when both CCE and INIT are set to '1'. The bit can be reset by the Host at any time. For a description of the Restricted Operation Mode see Section 3.1.5. 0= Normal CAN operation 1= Restricted Operation Mode active Default Value: 0
1	CCE	Configuration Change Enable 0= The CPU has no write access to the protected configuration registers 1= The CPU has write access to the protected configuration registers (while CCCR.INIT = '1') Default Value: 0
0	INIT	Initialization 0= Normal Operation 1= Initialization is started Default Value: 1

CANFD0_CH0_NBTP

Nominal Bit Timing & Prescaler Register
Address: 0x4052001C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	NTSEG2 [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	NTSEG1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	NBRP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							RW
HW Access	R							R
Name	NSJW [31:25]							NBRP

Bits	Name	Description
31 : 25	NSJW	Nominal (Re)Synchronization Jump Width 0x00-0x7F Valid values are 0 to 127. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Default Value: 3
24 : 16	NBRP	Nominal Bit Rate Prescaler 0x000-0x1FFThe value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Bit Rate Prescaler are 0 to 511. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Default Value: 0

15 : 8	NTSEG1	Nominal Time segment before sample point 0x01-0xFF Valid values are 1 to 255. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Default Value: 0xA
6 : 0	NTSEG2	Nominal Time segment after sample point 0x01-0x7F Valid values are 1 to 127. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Default Value: 3

CANFD0_CH0_TSCC

Timestamp Counter Configuration
Address: 0x40520020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						TSS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				TCP [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	TCP	Timestamp Counter Prescaler (still used for TOCC) 0x0-0xF Configures the timestamp and timeout counters time unit in multiples of CAN bit times [1...16]. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Default Value: 0
1 : 0	TSS	Timestamp Select, should always be set to external timestamp counter 00= Timestamp counter value always 0x0000 01= Timestamp counter value incremented according to TCP 10= External timestamp counter value used 11= Same as '00' Default Value: 0

CANFD0_CH0_TSCV

Timestamp Counter Value
Address: 0x40520024
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TSC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TSC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	TSC	Timestamp Counter, not used for M_TTCAN The internal/external Timestamp Counter value is captured on start of frame (both Rx and Tx). When TSCC.TSS = '01', the Timestamp Counter is incremented in multiples of CAN bit times [1...16] depending on the configuration of TSCC.TCP. A wrap around sets interrupt flag IR.TSW. Write access resets the counter to zero. When TSCC.TSS = '10', TSC reflects the external Timestamp Counter value. A write access has no impact. Default Value: 0

CANFD0_CH0_TOCC

Timeout Counter Configuration
Address: 0x40520028
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		RW
HW Access	None					R		R
Name	None [7:3]					TOS [2:1]		ETOC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TOP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	TOP [31:24]							

Bits	Name	Description
31 : 16	TOP	Timeout Period Start value of the Timeout Counter (down-counter). Configures the Timeout Period. Default Value: 0xFFFF
2 : 1	TOS	Timeout Select When operating in Continuous mode, a write to TOCV presets the counter to the value configured by TOCC.TOP and continues down-counting. When the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by TOCC.TOP. Down-counting is started when the first FIFO element is stored. 00= Continuous operation 01= Timeout controlled by Tx Event FIFO 10= Timeout controlled by Rx FIFO 0 11= Timeout controlled by Rx FIFO 1 Default Value: 0
0	ETOC	Enable Timeout Counter 0= Timeout Counter disabled 1= Timeout Counter enabled Default Value: 0

CANFD0_CH0_TOCV

Timeout Counter Value
Address: 0x4052002C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TOC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TOC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	TOC	Timeout Counter The Timeout Counter is decremented in multiples of CAN bit times [1...16] depending on the configuration of TSCC.TCP. When decremented to zero, interrupt flag IR.TOO is set and the Timeout Counter is stopped. Start and reset/restart conditions are configured via TOCC.TOS. Default Value: 0xFFFF

CANFD0_CH0_ECR

Error Counter Register
Address: 0x40520040
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TEC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R	R						
HW Access	RW	RW						
Name	RP	REC [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW1C							
Name	CEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	CEL	CAN Error Logging The counter is incremented each time when a CAN protocol error causes the Transmit Error Counter or the Receive Error Counter to be incremented. It is reset by read access to CEL. The counter stops at 0xFF; the next increment of TEC or REC sets interrupt flag IR.ELO. Default Value: 0
15	RP	Receive Error Passive 0= The Receive Error Counter is below the error passive level of 128 1= The Receive Error Counter has reached the error passive level of 128 Default Value: 0
14 : 8	REC	Receive Error Counter Actual state of the Receive Error Counter, values between 0 and 127 Default Value: 0
7 : 0	TEC	Transmit Error Counter Actual state of the Transmit Error Counter, values between 0 and 255 Default Value: 0

CANFD0_CH0_PSR

Protocol Status Register
Address: 0x40520044
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R		R		
HW Access	RW	RW	RW	RW		RW1S		
Name	BO	EW	EP	ACT [4:3]		LEC [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None	R	R	R	R	R		
HW Access	None	RW1C	RW1C	RW1C	RW1C	RW1S		
Name	None	PXE	RFDF	RBRS	RESI	DLEC [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None	R						
HW Access	None	RW						
Name	None	TDCV [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22 : 16	TDCV	Transmitter Delay Compensation Value 0x00-0x7F Position of the secondary sample point, defined by the sum of the measured delay from m_can_tx to m_can_rx and TDCR.TDCO. The SSP position is, in the data phase, the number of mtq between the start of the transmitted bit and the secondary sample point. Valid values are 0 to 127 mtq. Default Value: 0
14	PXE	Protocol Exception Event , Reset on Read 0= No protocol exception event occurred since last read access 1= Protocol exception event occurred Default Value: 0
13	RFDF	Received a CAN FD Message , Reset on Read This bit is set independent of acceptance filtering. 0= Since this bit was reset by the CPU, no CAN FD message has been received 1= Message in CAN FD format with FDF flag set has been received Default Value: 0

12	RBRS	BRS flag of last received CAN FD Message , Reset on Read This bit is set together with RFDF, independent of acceptance filtering. 0= Last received CAN FD message did not have its BRS flag set 1= Last received CAN FD message had its BRS flag set Default Value: 0
11	RESI	ESI flag of last received CAN FD Message , Reset on Read This bit is set together with RFDF, independent of acceptance filtering. 0= Last received CAN FD message did not have its ESI flag set 1= Last received CAN FD message had its ESI flag set Default Value: 0
10 : 8	DLEC	Data Phase Last Error Code , Set on Read Type of last error that occurred in the data phase of a CAN FD format frame with its BRS flag set. Coding is the same as for LEC. This field will be cleared to zero when a CAN FD format frame with its BRS flag set has been transferred (reception or transmission) without error. Default Value: 7
7	BO	Bus_Off Status 0= The M_CAN is not Bus_Off 1= The M_CAN is in Bus_Off state Default Value: 0
6	EW	Warning Status 0= Both error counters are below the Error_Warning limit of 96 1= At least one of error counter has reached the Error_Warning limit of 96 Default Value: 0
5	EP	Error Passive 0= The M_CAN is in the Error_Active state. It normally takes part in bus communication and sends an active error flag when an error has been detected 1= The M_CAN is in the Error_Passive state Default Value: 0

4 : 3	ACT	Activity Monitors the module's CAN communication state. 00= Synchronizing - node is synchronizing on CAN communication 01= Idle - node is neither receiver nor transmitter 10= Receiver - node is operating as receiver 11= Transmitter - node is operating as transmitter Default Value: 0

2 : 0	LEC	Last Error Code, Set on Read0 The LEC indicates the type of the last error to occur on the CAN bus. This field will be cleared to '0' when a message has been transferred (reception or transmission) without error. 0= No Error: No error occurred since LEC has been reset by successful reception or transmission. 1= Stuff Error: More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed. 2= Form Error: A fixed format part of a received frame has the wrong format. 3= AckError: The message transmitted by the M_TTCAN was not acknowledged by another node. 4= Bit1Error: During the transmission of a message (with the exception of the arbitration field), the device wanted to send a recessive level (bit of logical value '1'), but the monitored bus value was dominant. 5= Bit0Error: During the transmission of a message (or acknowledge bit, or active error flag, or overload flag), the device wanted to send a dominant level (data or identifier bit logical value 0'), but the monitored bus value was recessive. During Bus_Off recovery this status is set each time a sequence of 11 recessive bits has been monitored. This enables the CPU to monitor the proceeding of the Bus_Off recovery sequence (indicating the bus is not stuck at dominant or continuously disturbed). 6= CRCError: The CRC check sum of a received message was incorrect. The CRC of an incoming message does not match with the CRC calculated from the received data. 7= NoChange: Any read access to the Protocol Status Register re-initializes the LEC to '7'. When the LEC shows the value '7', no CAN bus event was detected since the last CPU read access to the Protocol Status Register. Default Value: 7

CANFD0_CH0_TDCR

Transmitter Delay Compensation Register
Address: 0x40520048
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TDCF [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None	TDCO [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14 : 8	TDCO	Transmitter Delay Compensation Offset 0x00-0x7F Offset value defining the distance between the measured delay from m_ttcan_tx to m_ttcan_rx and the secondary sample point. Valid values are 0 to 127 mtq. Default Value: 0
6 : 0	TDCF	Transmitter Delay Compensation Filter Window Length 0x00-0x7F Defines the minimum value for the SSP position, dominant edges on m_ttcan_rx that would result in an earlier SSP position are ignored for transmitter delay measurement. The feature is enabled when TDCF is configured to a value greater than TDCO. Valid values are 0 to 127 mtq Default Value: 0

CANFD0_CH0_IR

Interrupt Register
Address: 0x40520050
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	RF1L_	RF1F	RF1W	RF1N	RF0L_	RF0F	RF0W	RF0N

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	TEFL_	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	EP_	ELO	BEU	BEC	DRX	TOO	MRAF	TSW

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [31:30]		ARA	PED	PEA	WDI	BO_	EW_

Bits	Name	Description
29	ARA	Access to Reserved Address 0= No access to reserved address occurred 1= Access to reserved address occurred Default Value: 0
28	PED	Protocol Error in Data Phase (Data Bit Time is used) 0= No protocol error in data phase 1= Protocol error in data phase detected (PSR.DLEC != 0,7) Default Value: 0
27	PEA	Protocol Error in Arbitration Phase (Nominal Bit Time is used) 0= No protocol error in arbitration phase 1= Protocol error in arbitration phase detected (PSR.LEC != 0,7) Default Value: 0
26	WDI	Watchdog Interrupt 0= No Message RAM Watchdog event occurred 1= Message RAM Watchdog event due to missing READY Default Value: 0
25	BO_	Bus_Off Status 0= Bus_Off status unchanged 1= Bus_Off status changed Default Value: 0

24	EW_	Warning Status 0= Error_Warning status unchanged 1= Error_Warning status changed Default Value: 0
23	EP_	Error Passive 0= Error_Passive status unchanged 1= Error_Passive status changed Default Value: 0
22	ELO	Error Logging Overflow 0= CAN Error Logging Counter did not overflow 1= Overflow of CAN Error Logging Counter occurred Default Value: 0
21	BEU	Bit Error Uncorrected Message RAM bit error detected, uncorrected. The flag is set in the folloiwng cases. - M_TTCAN detects uncorrectable ECC error from Message RAM when ECC is enabled and ECC error injection is disabled. - M_TTCAN reads from an out of range Message RAM address. Message RAM bit error sets CCCR.INIT to '1'. This is done to avoid transmission of corrupted data. 0= No bit error detected when reading from Message RAM 1= Bit error detected, uncorrected Default Value: 0
20	BEC	Bit Error Corrected This bit always reads as 0. Default Value: 0
19	DRX	Message stored to Dedicated Rx Buffer The flag is set whenever a received message has been stored into a dedicated Rx Buffer. 0= No Rx Buffer updated 1= At least one received message stored into a Rx Buffer Default Value: 0
18	TOO	Timeout Occurred 0= No timeout 1= Timeout reached Default Value: 0

17	MRAF	Message RAM Access Failure The flag is set, when the Rx Handler - has not completed acceptance filtering or storage of an accepted message until the arbitration field of the following message has been received. In this case acceptance filtering or message storage is aborted and the Rx Handler starts processing of the following message. - was not able to write a message to the Message RAM. In this case message storage is aborted. In both cases the FIFO put index is not updated resp. the New Data flag for a dedicated Rx Buffer is not set, a partly stored message is overwritten when the next message is stored to this location. The flag is also set when the Tx Handler was not able to read a message from the Message RAM in time. In this case message transmission is aborted. In case of a Tx Handler access failure the M_TTCAN is switched into Restricted Operation Mode (see Section 3.1.5). To leave Restricted Operation Mode, the Host CPU has to reset CCCR.ASM. 0= No Message RAM access failure occurred 1= Message RAM access failure occurred Default Value: 0
16	TSW	Timestamp Wraparound 0= No timestamp counter wrap-around 1= Timestamp counter wrapped around Default Value: 0
15	TEFL_	Tx Event FIFO Element Lost 0= No Tx Event FIFO element lost 1= Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero Default Value: 0
14	TEFF	Tx Event FIFO Full 0= Tx Event FIFO not full 1= Tx Event FIFO full Default Value: 0
13	TEFW	Tx Event FIFO Watermark Reached 0= Tx Event FIFO fill level below watermark 1= Tx Event FIFO fill level reached watermark Default Value: 0
12	TEFN	Tx Event FIFO New Entry 0= Tx Event FIFO unchanged 1= Tx Handler wrote Tx Event FIFO element Default Value: 0

11	TFE	Tx FIFO Empty 0= Tx FIFO non-empty 1= Tx FIFO empty Default Value: 0
10	TCF	Transmission Cancellation Finished 0= No transmission cancellation finished 1= Transmission cancellation finished Default Value: 0
9	TC	Transmission Completed 0= No transmission completed 1= Transmission completed Default Value: 0
8	HPM	High Priority Message 0= No high priority message received 1= High priority message received Default Value: 0
7	RF1L_	Rx FIFO 1 Message Lost 0= No Rx FIFO 1 message lost 1= Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero Default Value: 0
6	RF1F	Rx FIFO 1 Full 0= Rx FIFO 1 not full 1= Rx FIFO 1 full Default Value: 0
5	RF1W	Rx FIFO 1 Watermark Reached 0= Rx FIFO 1 fill level below watermark 1= Rx FIFO 1 fill level reached watermark Default Value: 0
4	RF1N	Rx FIFO 1 New Message 0= No new message written to Rx FIFO 1 1= New message written to Rx FIFO 1 Default Value: 0
3	RF0L_	Rx FIFO 0 Message Lost 0= No Rx FIFO 0 message lost 1= Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero Default Value: 0
2	RF0F	Rx FIFO 0 Full 0= Rx FIFO 0 not full 1= Rx FIFO 0 full Default Value: 0
1	RF0W	Rx FIFO 0 Watermark Reached 0= Rx FIFO 0 fill level below watermark 1= Rx FIFO 0 fill level reached watermark Default Value: 0
0	RF0N	Rx FIFO 0 New Message 0= No new message written to Rx FIFO 0 1= New message written to Rx FIFO 0 Default Value: 0

CANFD0_CH0_IE

Interrupt Enable
Address: 0x40520054
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	RF1LE	RF1FE	RF1WE	RF1NE	RF0LE	RF0FE	RF0WE	RF0NE
Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	TEFLE	TEFFE	TEFWE	TEFNE	TFEE	TCFE	TCE	HPME
Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EPE	ELOE	BEUE	BECE	DRXE	TOOE	MRAFE	TSWE
Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [31:30]		ARAE	PEDE	PEAE	WDIE	BOE	EWE

Bits	Name	Description
29	ARAE	Access to Reserved Address Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
28	PEDE	Protocol Error in Data Phase Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
27	PEAE	Protocol Error in Arbitration Phase Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
26	WDIE	Watchdog Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
25	BOE	Bus_Off Status Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
24	EWE	Warning Status Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
23	EPE	Error Passive Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

22	ELOE	Error Logging Overflow Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
21	BEUE	Bit Error Uncorrected Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
20	BECE	Bit Error Corrected Interrupt Enable (not used in M_TTCAN) 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
19	DRXE	Message stored to Dedicated Rx Buffer Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
18	TOOE	Timeout Occurred Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
17	MRAFE	Message RAM Access Failure Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
16	TSWE	Timestamp Wraparound Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
15	TEFLE	Tx Event FIFO Event Lost Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
14	TEFFE	Tx Event FIFO Full Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
13	TEFWE	Tx Event FIFO Watermark Reached Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
12	TEFNE	Tx Event FIDO New Entry Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
11	TFEE	Tx FIFO Empty Interrupt Enable 0= Interrupt Disabled 1= Interrupt EnabledTx FIFO Empty Interrupt Enable Default Value: 0
10	TCFE	Transmission Cancellation Finished Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
9	TCE	Transmission Completed Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
8	HPME	High Priority Message Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

7	RF1LE	Rx FIFO 1 Message Lost Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
6	RF1FE	Rx FIFO 1 Full Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
5	RF1WE	Rx FIFO 1 Watermark Reached Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
4	RF1NE	Rx FIFO 1 New Message Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
3	RF0LE	Rx FIFO 0 Message Lost Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
2	RF0FE	Rx FIFO 0 Full Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
1	RF0WE	Rx FIFO 0 Watermark Reached Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
0	RF0NE	Rx FIFO 0 New Message Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

CANFD0_CH0_ILS

Interrupt Line Select
Address: 0x40520058
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL
Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	TEFLL	TEFFL	TEFWL	TEFNL	TFEL	TCFL	TCL	HPML
Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EPL	ELOL	BEUL	BECL	DRXL	TOOL	MRAFL	TSWL
Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [31:30]		ARAL	PEDL	PEAL	WDIL	BOL	EWL

Bits	Name	Description
29	ARAL	Access to Reserved Address Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
28	PEDL	Protocol Error in Data Phase Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
27	PEAL	Protocol Error in Arbitration Phase Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
26	WDIL	Watchdog Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

25	BOL	Bus_Off Status Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
24	EWL	Warning Status Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
23	EPL	Error Passive Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
22	ELOL	Error Logging Overflow Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
21	BEUL	Bit Error Uncorrected Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
20	BECL	Bit Error Corrected Interrupt Select (not used in M_TTCAN) 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
19	DRXL	Message stored to Dedicated Rx Buffer Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
18	TOOL	Timeout Occurred Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
17	MRAFL	Message RAM Access Failure Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
16	TSWL	Timestamp Wraparound Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

15	TEFLL	Tx Event FIFO Event Lost Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
14	TEFFL	Tx Event FIFO Full Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
13	TEFWL	Tx Event FIFO Watermark Reached Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
12	TEFNL	Tx Event FIFO New Entry Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
11	TFEL	Tx FIFO Empty Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
10	TCFL	Transmission Cancellation Finished Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
9	TCL	Transmission Completed Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
8	HPML	High Priority Message Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
7	RF1LL	Rx FIFO 1 Message Lost Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
6	RF1FL	Rx FIFO 1 Full Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

5	RF1WL	Rx FIFO 1 Watermark Reached Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
4	RF1NL	Rx FIFO 1 New Message Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
3	RF0LL	Rx FIFO 0 Message Lost Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
2	RF0FL	Rx FIFO 0 Full Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
1	RF0WL	Rx FIFO 0 Watermark Reached Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
0	RF0NL	Rx FIFO 0 New Message Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

CANFD0_CH0_ILE

Interrupt Line Enable
Address: 0x4052005C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						EINT1	EINT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	EINT1	Enable Interrupt Line 1 0= Interrupt line m_ttcan_int1 disabled 1= Interrupt line m_ttcan_int1 enabled Default Value: 0
0	EINT0	Enable Interrupt Line 0 0= Interrupt line m_ttcan_int0 disabled 1= Interrupt line m_ttcan_int0 enabled Default Value: 0

CANFD0_CH0_GFC

Global Filter Configuration
Address: 0x40520080
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	RW
HW Access	None		R		R		R	R
Name	None [7:6]		ANFS [5:4]		ANFE [3:2]		RRFS	RRFE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	ANFS	Accept Non-matching Frames Standard Defines how received messages with 11-bit IDs that do not match any element of the filter list are treated. 00= Accept in Rx FIFO 0 01= Accept in Rx FIFO 1 10= Reject 11= Reject Default Value: 0
3 : 2	ANFE	Accept Non-matching Frames Extended Defines how received messages with 29-bit IDs that do not match any element of the filter list are treated. 00= Accept in Rx FIFO 0 01= Accept in Rx FIFO 1 10= Reject 11= Reject Default Value: 0
1	RRFS	Reject Remote Frames Standard 0= Filter remote frames with 11-bit standard IDs 1= Reject all remote frames with 11-bit standard IDs Default Value: 0

0	RRFE	Reject Remote Frames Extended 0= Filter remote frames with 29-bit extended IDs 1= Reject all remote frames with 29-bit extended IDs Default Value: 0

CANFD0_CH0_SIDFC

Standard ID Filter Configuration
Address: 0x40520084
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	FLSSA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FLSSA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LSS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	LSS	List Size Standard 0= No standard Message ID filter 1-128= Number of standard Message ID filter elements 128= Values greater than 128 are interpreted as 128 Default Value: 0
15 : 2	FLSSA	Filter List Standard Start Address Start address of standard Message ID filter list (32-bit word address, see Figure 2). Default Value: 0

CANFD0_CH0_XIDFC

Extended ID Filter Configuration
Address: 0x40520088
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	FLESA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FLESA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	LSE [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22 : 16	LSE	List Size Extended 0= No extended Message ID filter 1-64= Number of extended Message ID filter elements 64= Values greater than 64 are interpreted as 64 Default Value: 0
15 : 2	FLESA	Filter List Extended Start Address Start address of extended Message ID filter list (32-bit word address, see Figure 2). Default Value: 0

CANFD0_CH0_XIDAM

Extended ID AND Mask
Address: 0x40520090
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	EIDM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	EIDM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	EIDM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			R				
Name	None [31:29]			EIDM [28:24]				

Bits	Name	Description
28 : 0	EIDM	Extended ID Mask For acceptance filtering of extended frames the Extended ID AND Mask is ANDed with the Message ID of a received frame. Intended for masking of 29-bit IDs in SAE J1939. With the reset value of all bits set to one the mask is not active. Default Value: 0x1FFFFFFF

CANFD0_CH0_HPMS

High Priority Message Status
Address: 0x40520094
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R					
HW Access	RW		RW					
Name	MSI [7:6]		BIDX [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R	R						
HW Access	RW	RW						
Name	FLST	FIDX [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	FLST	Filter List Indicates the filter list of the matching filter element. 0= Standard Filter List 1= Extended Filter List Default Value: 0
14 : 8	FIDX	Filter Index Index of matching filter element. Range is 0 to SIDFC.LSS - 1 resp. XIDFC.LSE - 1. Default Value: 0
7 : 6	MSI	Message Storage Indicator 00= No FIFO selected 01= FIFO message lost 10= Message stored in FIFO 0 11= Message stored in FIFO 1 Default Value: 0
5 : 0	BIDX	Buffer Index Index of Rx FIFO element to which the message was stored. Only valid when MSI[1] = '1'. Default Value: 0

CANFD0_CH0_NDAT1

New Data 1
Address: 0x40520098
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW							
Name	ND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW							
Name	ND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	RW							
Name	ND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	RW							
Name	ND [31:24]							

Bits	Name	Description
31 : 0	ND	New Data The register holds the New Data flags of Rx Buffers 0 to 31. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them. A flag is cleared by writing a '1' to the corresponding bit position. Writing a '0' has no effect. A hard reset will clear the register. 0= Rx Buffer not updated 1= Rx Buffer updated from new message Default Value: 0

CANFD0_CH0_NDAT2

New Data 2
Address: 0x4052009C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW							
Name	ND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW							
Name	ND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	RW							
Name	ND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	RW							
Name	ND [31:24]							

Bits	Name	Description
31 : 0	ND	New Data The register holds the New Data flags of Rx Buffers 32 to 63. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them. A flag is cleared by writing a '1' to the corresponding bit position. Writing a '0' has no effect. A hard reset will clear the register. 0= Rx Buffer not updated 1= Rx Buffer updated from new message Default Value: 0

CANFD0_CH0_RXF0C

Rx FIFO 0 Configuration
Address: 0x405200A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	F0SA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	F0SA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	F0S [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW						
HW Access	R	R						
Name	F0OM	F0WM [30:24]						

Bits	Name	Description
31	F0OM	FIFO 0 Operation Mode FIFO 0 can be operated in blocking or in overwrite mode (see Section 3.4.2). 0= FIFO 0 blocking mode 1= FIFO 0 overwrite mode Default Value: 0
30 : 24	F0WM	Rx FIFO 0 Watermark 0= Watermark interrupt disabled 1-64= Level for Rx FIFO 0 watermark interrupt (IR.RF0W) 64= Watermark interrupt disabled Default Value: 0
22 : 16	F0S	Rx FIFO 0 Size 0= No Rx FIFO 0 1-64= Number of Rx FIFO 0 elements 64= Values greater than 64 are interpreted as 64 The Rx FIFO 0 elements are indexed from 0 to F0S-1 Default Value: 0
15 : 2	F0SA	Rx FIFO 0 Start Address Start address of Rx FIFO 0 in Message RAM (32-bit word address, see Figure 2). Default Value: 0

CANFD0_CH0_RXF0S

Rx FIFO 0 Status
Address: 0x405200A4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R						
HW Access	None	RW						
Name	None	F0FL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None		R					
HW Access	None		RW					
Name	None [15:14]		F0GI [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None		R					
HW Access	None		RW					
Name	None [23:22]		F0PI [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None						R	R
HW Access	None						RW	RW
Name	None [31:26]						RF0L	F0F

Bits	Name	Description
25	RF0L	Rx FIFO 0 Message Lost This bit is a copy of interrupt flag IR.RF0L. When IR.RF0L is reset, this bit is also reset. 0= No Rx FIFO 0 message lost 1= Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero Default Value: 0
24	F0F	Rx FIFO 0 Full 0= Rx FIFO 0 not full 1= Rx FIFO 0 full When the software reading the value immediately after writing to RXF0A.F0AI, this value should be read twice to ensure that the update is reflected. Default Value: 0
21 : 16	F0PI	Rx FIFO 0 Put Index Rx FIFO 0 write index pointer, range 0 to 63. Default Value: 0

13 : 8	F0GI	Rx FIFO 0 Get Index Rx FIFO 0 read index pointer, range 0 to 63. This field is updated by the software writing to RXF0A.F0AI. When the software reading the value immediately after writing to RXF0A.F0AI, this value should be read twice to ensure that the update is reflected. Default Value: 0
6 : 0	F0FL	Rx FIFO 0 Fill Level Number of elements stored in Rx FIFO 0, range 0 to 64. When the software reading the value immediately after writing to RXF0A.F0AI, this value should be read twice to ensure that the update is reflected. Default Value: 0

CANFD0_CH0_RXF0A

Rx FIFO 0 Acknowledge
Address: 0x405200A8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		A					
Name	None [7:6]		F0AI [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	F0AI	Rx FIFO 0 Acknowledge Index After the Host has read a message or a sequence of messages from Rx FIFO 0 it has to write the buffer index of the last element read from Rx FIFO 0 to F0AI. This will set the Rx FIFO 0 Get Index RXF0S.F0GI to F0AI + 1 and update the FIFO 0 Fill Level RXF0S.F0FL. Default Value: 0

CANFD0_CH0_RXBC

Rx Buffer Configuration
Address: 0x405200AC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	RBSA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RBSA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 2	RBSA	Rx Buffer Start Address Configures the start address of the Rx Buffers section in the Message RAM (32-bit word address). Also used to reference debug messages A,B,C. Default Value: 0

CANFD0_CH0_RXF1C

Rx FIFO 1 Configuration
Address: 0x405200B0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	F1SA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	F1SA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	F1S [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW						
HW Access	R	R						
Name	F1OM	F1WM [30:24]						

Bits	Name	Description
31	F1OM	FIFO 1 Operation Mode FIFO 1 can be operated in blocking or in overwrite mode (see Section 3.4.2). 0= FIFO 1 blocking mode 1= FIFO 1 overwrite mode Default Value: 0
30 : 24	F1WM	Rx FIFO 1 Watermark 0= Watermark interrupt disabled 1-64= Level for Rx FIFO 1 watermark interrupt (IR.RF1W) 64= Watermark interrupt disabled Default Value: 0
22 : 16	F1S	Rx FIFO 1 Size 0= No Rx FIFO 1 1-64= Number of Rx FIFO 1 elements 64= Values greater than 64 are interpreted as 64 The Rx FIFO 1 elements are indexed from 0 to F1S - 1 Default Value: 0
15 : 2	F1SA	Rx FIFO 1 Start Address Start address of Rx FIFO 1 in Message RAM (32-bit word address, see Figure 2). Default Value: 0

CANFD0_CH0_RXF1S

Rx FIFO 1 Status
Address: 0x405200B4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R						
HW Access	None	RW						
Name	None	F1FL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None		R					
HW Access	None		RW					
Name	None [15:14]		F1GI [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None		R					
HW Access	None		RW					
Name	None [23:22]		F1PI [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	R		None				R	R
HW Access	RW		None				RW	RW
Name	DMS [31:30]		None [29:26]				RF1L	F1F

Bits	Name	Description
31 : 30	DMS	Debug Message Status 00= Idle state, wait for reception of debug messages, DMA request is cleared 01= Debug message A received 10= Debug messages A, B received 11= Debug messages A, B, C received, DMA request is set Default Value: 0
25	RF1L	Rx FIFO 1 Message Lost This bit is a copy of interrupt flag IR.RF1L. When IR.RF1L is reset, this bit is also reset. 0= No Rx FIFO 1 message lost 1= Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero Default Value: 0
24	F1F	Rx FIFO 1 Full 0= Rx FIFO 1 not full 1= Rx FIFO 1 full When the software reading the value immediately after writing to RXF1A.F1AI, this value should be read twice to ensure that the update is reflected. Default Value: 0

21 : 16	F1PI	Rx FIFO 1 Put Index Rx FIFO 1 write index pointer, range 0 to 63. Default Value: 0
13 : 8	F1GI	Rx FIFO 1 Get Index Rx FIFO 1 read index pointer, range 0 to 63. This field is updated by the software writing to RXF1A.F1AI. When the software reading the value immediately after writing to RXF1A.F1AI, this value should be read twice to ensure that the update is reflected. Default Value: 0
6 : 0	F1FL	Rx FIFO 1 Fill Level Number of elements stored in Rx FIFO 1, range 0 to 64. When the software reading the value immediately after writing to RXF1A.F1AI, this value should be read twice to ensure that the update is reflected. Default Value: 0

CANFD0_CH0_RXF1A

Rx FIFO 1 Acknowledge
Address: 0x405200B8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		A					
Name	None [7:6]		F1AI [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	F1AI	Rx FIFO 1 Acknowledge Index After the Host has read a message or a sequence of messages from Rx FIFO 1 it has to write the buffer index of the last element read from Rx FIFO 1 to F1AI. This will set the Rx FIFO 1 Get Index RXF1S.F1GI to F1AI + 1 and update the FIFO 1 Fill Level RXF1S.F1FL. Default Value: 0

CANFD0_CH0_RXESC

Rx Buffer / FIFO Element Size Configuration
Address: 0x405200BC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	F1DS [6:4]			None	F0DS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					RBDS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 8	RBDS	Rx Buffer Data Field Size 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field Default Value: 0
6 : 4	F1DS	Rx FIFO 1 Data Field Size 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field Default Value: 0
2 : 0	F0DS	Rx FIFO 0 Data Field Size 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field Default Value: 0

CANFD0_CH0_TXBC

Tx Buffer Configuration
Address: 0x405200C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	TBSA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TBSA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW					
HW Access	None		R					
Name	None [23:22]		NDTB [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW	RW					
HW Access	None	R	R					
Name	None	TFQM	TFQS [29:24]					

Bits	Name	Description
30	TFQM	Tx FIFO/Queue Mode 0= Tx FIFO operation 1= Tx Queue operation Default Value: 0
29 : 24	TFQS	Transmit FIFO/Queue Size 0= No Tx FIFO/Queue 1-32= Number of Tx Buffers used for Tx FIFO/Queue 32= Values greater than 32 are interpreted as 32 Default Value: 0
21 : 16	NDTB	Number of Dedicated Transmit Buffers 0= No Dedicated Tx Buffers 1-32= Number of Dedicated Tx Buffers 32= Values greater than 32 are interpreted as 32 Default Value: 0
15 : 2	TBSA	Tx Buffers Start Address Start address of Tx Buffers section in Message RAM (32-bit word address, see Figure 2). Default Value: 0

CANFD0_CH0_TXFQS

Tx FIFO/Queue Status
Address: 0x405200C4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		RW					
Name	None [7:6]		TFFL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None			R				
HW Access	None			RW				
Name	None [15:13]			TFGI [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None		R	R				
HW Access	None		RW	RW				
Name	None [23:22]		TFQF	TFQPI [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	TFQF	Tx FIFO/Queue Full 0= Tx FIFO/ Queue not full 1= Tx FIFO/Queue full Default Value: 0
20 : 16	TFQPI	Tx FIFO/Queue Put Index Tx FIFO/ Queue write index pointer, range 0 to 31. Default Value: 0
12 : 8	TFGI	Tx FIFO Get Index Tx FIFO read index pointer, range 0 to 31. Read as zero when Tx Queue operation is configured TXBC.TFQM = '1'). Default Value: 0
5 : 0	TFFL	Tx FIFO Free Level Number of consecutive free Tx FIFO elements starting from TFGI, range 0 to 32. Read as zero when Tx Queue operation is configured (TXBC.TFQM = '1') Default Value: 0

CANFD0_CH0_TXESC

Tx Buffer Element Size Configuration
Address: 0x405200C8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					TBDS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	TBDS	Tx Buffer Data Field Size 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field Default Value: 0

CANFD0_CH0_TXBRP

Tx Buffer Request Pending
Address: 0x405200CC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TRP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	TRP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	TRP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	TRP [31:24]							

Bits	Name	Description

31 : 0	TRP	Transmission Request Pending Each Tx Buffer has its own Transmission Request Pending bit. The bits are set via register TXBAR. The bits are reset after a requested transmission has completed or has been cancelled via register TXBCR. TXBRP bits are set only for those Tx Buffers configured via TXBC. After a TXBRP bit has been set, a Tx scan (see Section 3.5, Tx Handling) is started to check for the pending Tx request with the highest priority (Tx Buffer with lowest Message ID). A cancellation request resets the corresponding transmission request pending bit of register TXBRP. In case a transmission has already been started when a cancellation is requested, this is done at the end of the transmission, regardless whether the transmission was successful or not. The cancellation request bits are reset directly after the corresponding TXBRP bit has been reset. After a cancellation has been requested, a finished cancellation is signaled via TXBCF after successful transmission together with the corresponding TXBTO bit when the transmission has not yet been started at the point of cancellation when the transmission has been aborted due to lost arbitration when an error occurred during frame transmission In DAR mode all transmissions are automatically cancelled if they are not successful. The corresponding TXBCF bit is set for all unsuccessful transmissions. 0= No transmission request pending 1= Transmission request pending Default Value: 0

CANFD0_CH0_TXBAR

Tx Buffer Add Request
Address: 0x405200D0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	AR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	AR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	AR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	AR [31:24]							

Bits	Name	Description
31 : 0	AR	Add Request Each Tx Buffer has its own Add Request bit. Writing a '1' will set the corresponding Add Request bit; writing a '0' has no impact. This enables the Host to set transmission requests for multiple Tx Buffers with one write to TXBAR. TXBAR bits are set only for those Tx Buffers configured via TXBC. When no Tx scan is running, the bits are reset immediately, else the bits remain set until the Tx scan process has completed. 0= No transmission request added 1= Transmission requested added Default Value: 0

CANFD0_CH0_TXBCR

Tx Buffer Cancellation Request
Address: 0x405200D4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CR [31:24]							

Bits	Name	Description
31 : 0	CR	Cancellation Request Each Tx Buffer has its own Cancellation Request bit. Writing a '1' will set the corresponding Cancellation Request bit; writing a '0' has no impact. This enables the Host to set cancellation requests for multiple Tx Buffers with one write to TXBCR. TXBCR bits are set only for those Tx Buffers configured via TXBC. The bits remain set until the corresponding bit of TXBRP is reset. 0= No cancellation pending 1= Cancellation pending Default Value: 0

CANFD0_CH0_TXBTO

Tx Buffer Transmission Occurred
Address: 0x405200D8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TO [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	TO [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	TO [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	TO [31:24]							

Bits	Name	Description
31 : 0	TO	Transmission Occurred Each Tx Buffer has its own Transmission Occurred bit. The bits are set when the corresponding TXBRP bit is cleared after a successful transmission. The bits are reset when a new transmission is requested by writing a '1' to the corresponding bit of register TXBAR. 0= No transmission occurred 1= Transmission occurred Default Value: 0

CANFD0_CH0_TXBCF

Tx Buffer Cancellation Finished
Address: 0x405200DC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CF [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	CF [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	CF [31:24]							

Bits	Name	Description
31 : 0	CF	Cancellation Finished Each Tx Buffer has its own Cancellation Finished bit. The bits are set when the corresponding TXBRP bit is cleared after a cancellation was requested via TXBCR. In case the corresponding TXBRP bit was not set at the point of cancellation, CF is set immediately. The bits are reset when a new transmission is requested by writing a '1' to the corresponding bit of register TXBAR. 0= No transmit buffer cancellation 1= Transmit buffer cancellation finished Default Value: 0

CANFD0_CH0_TXBTIE

Tx Buffer Transmission Interrupt Enable
Address: 0x405200E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TIE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TIE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TIE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	TIE [31:24]							

Bits	Name	Description
31 : 0	TIE	Transmission Interrupt Enable Each Tx Buffer has its own Transmission Interrupt Enable bit. 0= Transmission interrupt disabled 1= Transmission interrupt enable Default Value: 0

CANFD0_CH0_TXBCIE

Tx Buffer Cancellation Finished Interrupt Enable
Address: 0x405200E4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CFIE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CFIE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CFIE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CFIE [31:24]							

Bits	Name	Description
31 : 0	CFIE	Cancellation Finished Interrupt Enable Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0= Cancellation finished interrupt disabled 1= Cancellation finished interrupt enabled Default Value: 0

CANFD0_CH0_TXEFC

Tx Event FIFO Configuration
Address: 0x405200F0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	EFSA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	EFSA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW					
HW Access	None		R					
Name	None [23:22]		EFS [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW					
HW Access	None		R					
Name	None [31:30]		EFWM [29:24]					

Bits	Name	Description
29 : 24	EFWM	Event FIFO Watermark 0= Watermark interrupt disabled 1-32= Level for Tx Event FIFO watermark interrupt (IR.TEFW) 32= Watermark interrupt disabled Default Value: 0
21 : 16	EFS	Event FIFO Size 0= Tx Event FIFO disabled 1-32= Number of Tx Event FIFO elements 32= Values greater than 32 are interpreted as 32 The Tx Event FIFO elements are indexed from 0 to EFS-1 Default Value: 0
15 : 2	EFSA	Event FIFO Start Address Start address of Tx Event FIFO in Message RAM (32-bit word address, see Figure 2). Default Value: 0

CANFD0_CH0_TXEFS

Tx Event FIFO Status
Address: 0x405200F4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		RW					
Name	None [7:6]		EFFL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None			R				
HW Access	None			RW				
Name	None [15:13]			EFGI [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			R				
HW Access	None			RW				
Name	None [23:21]			EFPI [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None						R	R
HW Access	None						RW	RW
Name	None [31:26]						TEFL	EFF

Bits	Name	Description
25	TEFL	Tx Event FIFO Element Lost This bit is a copy of interrupt flag IR.TEFL. When IR.TEFL is reset, this bit is also reset. 0= No Tx Event FIFO element lost 1= Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero. Default Value: 0
24	EFF	Event FIFO Full 0= Tx Event FIFO not full 1= Tx Event FIFO full When the software reading the value immediately after writing to TXEFA.EFAI, this value should be read twice to ensure that the update is reflected. Default Value: 0
20 : 16	EFPI	Event FIFO Put Index Tx Event FIFO write index pointer, range 0 to 31. Default Value: 0

12 : 8	EFGI	Event FIFO Get Index Tx Event FIFO read index pointer, range 0 to 31. This field is updated by the software writing to TXEFA.EFAI. When the software reading the value immediately after writing to TXEFA.EFAI, this value should be read twice to ensure that the update is reflected. Default Value: 0
5 : 0	EFFL	Event FIFO Fill Level Number of elements stored in Tx Event FIFO, range 0 to 32. When the software reading the value immediately after writing to TXEFA.EFAI, this value should be read twice to ensure that the update is reflected. Default Value: 0

CANFD0_CH0_TXEFA

Tx Event FIFO Acknowledge
Address: 0x405200F8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			EFAI [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	EFAI	Event FIFO Acknowledge Index After the Host has read an element or a sequence of elements from the Tx Event FIFO it has to write the index of the last element read from Tx Event FIFO to EFAI. This will set the Tx Event FIFO Get Index TXEFS.EFGI to EFAI + 1 and update the Event FIFO Fill Level TXEFS.EFFL. Default Value: 0

CANFD0_CH0_TTTMC

TT Trigger Memory Configuration
Address: 0x40520100
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	TMSA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TMSA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	TME [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22 : 16	TME	Trigger Memory Elements 0= No Trigger Memory 1-64= Number of Trigger Memory elements 64= Values greater than 64 are interpreted as 64 Default Value: 0
15 : 2	TMSA	Trigger Memory Start Address Start address of Trigger Memory in Message RAM (32-bit word address, see Figure 2). Default Value: 0

CANFD0_CH0_TTRMC

TT Reference Message Configuration
Address: 0x40520104
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	RW				
HW Access	R	R	None	R				
Name	RMPS	XTD	None	RID [28:24]				

Bits	Name	Description
31	RMPS	Reference Message Payload Select Ignored in case of time slaves. 0= Reference message has no additional payload 1= The following elements are taken from Tx Buffer 0: Message Marker MM, Event FIFO Control EFC, Data Length Code DLC, Data Bytes DB Level 1: bytes 2-8, Level 0,2: bytes 5-8) Default Value: 0
30	XTD	Extended Identifier 0= 11-bit standard identifier 1= 29-bit extended identifier Default Value: 0
28 : 0	RID	Reference Identifier Identifier transmitted with reference message and used for reference message filtering. Standard or extended reference identifier depending on bit XTD. A standard identifier has to be written to ID[28:18]. Default Value: 0

CANFD0_CH0_TTOCF

TT Operation Configuration
Address: 0x40520108
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW	RW	None	RW	
HW Access	R			R	R	None	R	
Name	LDSDL [7:5]			TM	GEN	None	OM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW						
HW Access	R	R						
Name	EECS	IRTO [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	AWL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [31:27]					EVTP	ECC	EGTF

Bits	Name	Description
26	EVTP	Event Trigger Polarity 0= Rising edge trigger 1= Falling edge trigger Default Value: 0
25	ECC	Enable Clock Calibration 0= Automatic clock calibration in TTCAN Level 0,2 is disabled 1= Automatic clock calibration in TTCAN Level 0,2 is enabled Default Value: 0
24	EGTF	Enable Global Time Filtering 0= Global time filtering in TTCAN Level 0,2 is disabled 1= Global time filtering in TTCAN Level 0,2 is enabled Default Value: 0
23 : 16	AWL	Application Watchdog Limit The application watchdog can be disabled by programming AWL to 0x00. 0x00-FF Maximum time after which the application has to serve the application watchdog. The application watchdog is incremented once each 256 NTUs. Default Value: 1

15	EECS	Enable External Clock Synchronization If enabled, TUR configuration (TURCF.NCL only) may be updated during TTCAN operation. 0= External clock synchronization in TTCAN Level 0,2 disabled 1= External clock synchronization in TTCAN Level 0,2 enabled Default Value: 0
14 : 8	IRTO	Initial Reference Trigger Offset 0x00-7F Positive offset, range from 0 to 127 Default Value: 0
7 : 5	LDSDL	LD of Synchronization Deviation Limit The Synchronization Deviation Limit SDL is configured by its dual logarithm LDSDL with SDL = 2(LDSDL + 5). It should not exceed the clock tolerance given by the CAN bit timing configuration. 0x0-7 LD of Synchronization Deviation Limit (SDL <= 32...4096) Default Value: 0
4	TM	Time Master 0= Time Master function disabled 1= Potential Time Master Default Value: 0
3	GEN	Gap Enable 0= Strictly time-triggered operation 1= External event-synchronized time-triggered operation Default Value: 0
1 : 0	OM	Operation Mode 00= Event-driven CAN communication, default 01= TTCAN level 1 10= TTCAN level 2 11= TTCAN level 0 Default Value: 0

CANFD0_CH0_TTMLM

TT Matrix Limits
Address: 0x4052010C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW					
HW Access	R		R					
Name	CSS [7:6]		CCM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				TXEW [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ENTT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW			
HW Access	None				R			
Name	None [31:28]				ENTT [27:24]			

Bits	Name	Description
27 : 16	ENTT	Expected Number of Tx Triggers 0x000-FFF Expected number of Tx Triggers in one Matrix Cycle Default Value: 0
11 : 8	TXEW	Tx Enable Window 0x0-F Length of Tx enable window, 1-16 NTU cycles Default Value: 0
7 : 6	CSS	Cycle Start Synchronization Enables sync pulse output at pin m_ttcan_soc. 00= No sync pulse 01= Sync pulse at start of basic cycle 10= Sync pulse at start of matrix cycle 11= Reserved Default Value: 0
5 : 0	CCM	Cycle Count Max 0x00 1 Basic Cycle per Matrix Cycle 0x01 2 Basic Cycles per Matrix Cycle 0x03 4 Basic Cycles per Matrix Cycle 0x07 8 Basic Cycles per Matrix Cycle 0x0F 16 Basic Cycles per Matrix Cycle 0x1F 32 Basic Cycles per Matrix Cycle 0x3F 64 Basic Cycles per Matrix Cycle others Reserved Default Value: 0

CANFD0_CH0_TURCF

TUR Configuration
Address: 0x40520110
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	NCL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	NCL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None	RW					
HW Access	R	None	R					
Name	ELT	None	DC [29:24]					

Bits	Name	Description
31	ELT	Enable Local Time 0= Local time is stopped, default 1= Local time is enabled Default Value: 0
29 : 16	DC	Denominator Configuration 0x0000 Illegal value 0x0001-3FFF Denominator Configuration Default Value: 0x1000
15 : 0	NCL	Numerator Configuration Low Write access to the TUR Numerator Configuration Low is only possible during configuration with TURCF.ELT = '0' or if TTOCF.EECS (external clock synchronization enabled) is set. When a new value for NCL is written outside TT Configuration Mode, the new value takes effect when TTOST.WECS is cleared to '0'. NCL is locked TTOST.WECS is '1'. 0x0000-FFFF Numerator Configuration Low Default Value: 0

CANFD0_CH0_TTOCN

TT Operation Control
Address: 0x40520114
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW		RW	RW	RW
HW Access	R		R	R		R	R	R
Name	TMC [7:6]		RTIE	SWS [4:3]		SWP	ECS	SGT

Bits	15	14	13	12	11	10	9	8
SW Access	R	None	RW	RW	RW	RW	RW	RW
HW Access	RW	None	R	R	R	R	R	R
Name	LCKC	None	ESCN	NIG	TMG	FGP	GCS	TTIE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	LCKC	TT Operation Control Register Locked Set by a write access to register TTOCN. Reset when the updated configuration has been synchronized into the CAN clock domain. 0= Write access to TTOCN enabled 1= Write access to TTOCN locked Default Value: 0
13	ESCN	External Synchronization Control If enabled the M_TTCAN synchronizes its cycle time phase to an external event signaled by a rising edge at pin m_ttcan_evt (see Section 4.11). 0= External synchronization disabled 1= External synchronization enabled Default Value: 0

12	NIG	Next is Gap This bit can only be set when the M_TTCAN is the actual Time Master and when it is configured for external event-synchronized time-triggered operation (TTOCF.GEN = '1') 0= No action, reset by reception of any reference message 1= Transmit next reference message with Next_is_Gap = '1' Default Value: 0
11	TMG	Time Mark Gap 0= Reset by each reference message 1= Next reference message started when Register Time Mark interrupt TTIR.RTMI is activated Default Value: 0
10	FGP	Finish Gap Set by the CPU, reset by each reference message 0= No reference message requested 1= Application requested start of reference message Default Value: 0
9	GCS	Gap Control Select 0= Gap control independent from m_ttcan_evt 1= Gap control by input pin m_ttcan_evt Default Value: 0
8	TTIE	Trigger Time Mark Interrupt Pulse Enable External time mark events are configured by trigger memory element TMEX (see Section 2.4.7). A trigger time mark interrupt pulse is generated when the trigger memory element becomes active, and the M_TTCAN is in synchronization state In_Schedule or In_Gap. 0= Trigger Time Mark Interrupt output m_ttcan_tmp disabled 1= Trigger Time Mark Interrupt output m_ttcan_tmp enabled Default Value: 0
7 : 6	TMC	Register Time Mark Compare 00= No Register Time Mark Interrupt generated 01= Register Time Mark Interrupt if Time Mark = cycle time 10= Register Time Mark Interrupt if Time Mark = local time 11= Register Time Mark Interrupt if Time Mark = global time Default Value: 0

5	RTIE	Register Time Mark Interrupt Pulse Enable Register time mark interrupts are configured by register TTTMK. A register time mark interrupt pulse with the length of one NTU is generated when the time referenced by TTOCN.TMC (cycle, local, or global) equals TTTMK.TM, independent of the synchronization state. 0= Register Time Mark Interrupt output m_ttcan_rtp disabled 1= Register Time Mark Interrupt output m_ttcan_rtp enabled Default Value: 0
4 : 3	SWS	Stop Watch Source 00= Stop Watch disabled 01= Actual value of cycle time is copied to TTCPT.SWV 10= Actual value of local time is copied to TTCPT.SWV 11= Actual value of global time is copied to TTCPT.SWV Default Value: 0
2	SWP	Stop Watch Polarity 0= Rising edge trigger 1= Falling edge trigger Default Value: 0
1	ECS	External Clock Synchronization Writing a '1' to ECS sets TTOST.WECS if the node is the actual Time Master. ECS is reset after one Host clock period. The external clock synchronization takes effect at the start of the next basic cycle. Default Value: 0
0	SGT	Set Global time Writing a '1' to SGT sets TTOST.WGDT if the node is the actual Time Master. SGT is reset after one Host clock period. The global time preset takes effect when the node transmits the next reference message with the Master_Ref_Mark modified by the preset value written to TTGTP. Default Value: 0

CANFD0_CH0_TTGTP

TT Global Time Preset
Address: 0x40520118
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CTP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CTP [31:24]							

Bits	Name	Description
31 : 16	CTP	Cycle Time Target Phase CTP is write-protected while TTOCN.ESCN or TTOST.SPL are set (see Section 4.11). 0x0000-FFFF Defines target value of cycle time when a rising edge of m_ttcan_evt is expected Default Value: 0
15 : 0	TP	Time Preset TP is write-protected while TTOST.WGTD is set. 0x0000-7FFF Next Master Reference Mark = Master Reference Mark + TP 0x8000 reserved 0x8001-FFFF Next Master Reference Mark = Master Reference Mark - (0x10000 - TP) Default Value: 0

CANFD0_CH0_TTTMK

TT Time Mark
Address: 0x4052011C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TM_ [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TM_ [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	TICC [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	LCKM	None [30:24]						

Bits	Name	Description
31	LCKM	TT Time Mark Register Locked Always set by a write access to registers TTOCN. Set by write access to register TTTMK when TTOCN.TMC != '00'. Reset when the registers have been synchronized into the CAN clock domain. 0= Write access to TTTMK enabled 1= Write access to TTTMK locked Default Value: 0

22 : 16	TICC	Time Mark Cycle Code Cycle count for which the time mark is valid. 0b000000x valid for all cycles 0b000001c valid every second cycle at cycle count mod2 = c 0b00001cc valid every fourth cycle at cycle count mod4 = cc 0b0001ccc valid every eighth cycle at cycle count mod8 = ccc 0b001cccc valid every sixteenth cycle at cycle count mod16 = cccc 0b01ccccc valid every thirty-second cycle at cycle count mod32 = ccccc 0b1cccccc valid every sixty-fourth cycle at cycle count mod64 = cccccc Default Value: 0
15 : 0	TM_	Time Mark 0x0000-FFFF Time Mark Default Value: 0

CANFD0_CH0_TTIR

TT Interrupt Register
Address: 0x40520120
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	GTW	SWE	TTMI	RTMI	SOG	CSM_	SMC	SBC

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	IWT	ELC	SE2	SE1	TXO	TXU	GTE	GTD

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW	RW	RW
Name	None [23:19]					CER	AW	WT

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18	CER	Configuration Error Trigger out of order. 0= No error found in trigger list 1= Error found in trigger list Default Value: 0
17	AW	Application Watchdog 0= Application watchdog served in time 1= Application watchdog not served in time Default Value: 0
16	WT	Watch Trigger 0= No missing reference message 1= Missing reference message (Level 0: cycle time 0xFF00) Default Value: 0
15	IWT	Initialization Watch Trigger The initialization is restarted by resetting IWT. 0= No missing reference message during system startup 1= No system startup due to missing reference message Default Value: 0

14	ELC	Error Level Changed Not set when error level changed during initialization. 0= No change in error level 1= Error level changed Default Value: 0
13	SE2	Scheduling Error 2 0= No scheduling error 2 1= Scheduling error 2 occurred Default Value: 0
12	SE1	Scheduling Error 1 0= No scheduling error 1 1= Scheduling error 1 occurred Default Value: 0
11	TXO	Tx Count Overflow 0= Number of Tx Trigger as expected 1= More Tx trigger than expected in one matrix cycle Default Value: 0
10	TXU	Tx Count Underflow 0= Number of Tx Trigger as expected 1= Less Tx trigger than expected in one matrix cycle Default Value: 0
9	GTE	Global Time Error Synchronization deviation SD exceeds limit specified by TTOCF.LDSDL, TTCAN Level 0,2 only. 0= Synchronization deviation within limit 1= Synchronization deviation exceeded limit Default Value: 0
8	GTD	Global Time Discontinuity 0= No discontinuity of global time 1= Discontinuity of global time Default Value: 0
7	GTW	Global Time Wrap 0= No global time wrap occurred 1= Global time wrap from 0xFFFF to 0x0000 occurred Default Value: 0
6	SWE	Stop Watch Event 0= No rising/ falling edge at stop watch trigger pin m_ttcan_swt detected 1= Rising/falling edge at stop watch trigger pin m_ttcan_swt detected Default Value: 0
5	TTMI	Trigger Time Mark Event Internal Internal time mark events are configured by trigger memory element TMIN (see Section 2.4.7). Set when the trigger memory element becomes active, and the M_TTCAN is in synchronization state In_Gap or In_Schedule. 0= Time mark not reached 1= Time mark reached (Level 0: cycle time TTOCF.IRTO * 0x200) Default Value: 0

4	RTMI	Register Time Mark Interrupt Set when time referenced by TTOCN.TMC (cycle, local, or global) equals TTTMK.TM, independent of the synchronization state. 0= Time mark not reached 1= Time mark reached Default Value: 0
3	SOG	Start of Gap 0= No reference message seen with Next_is_Gap bit set 1= Reference message with Next_is_Gap bit set becomes valid Default Value: 0
2	CSM_	Change of Synchronization Mode 0= No change in master to slave relation or schedule synchronization 1= Master to slave relation or schedule synchronization changed, also set when TTOST.SPL is reset Default Value: 0
1	SMC	Start of Matrix Cycle 0= No Matrix Cycle started since bit has been reset 1= Matrix Cycle started Default Value: 0
0	SBC	Start of Basic Cycle 0= No Basic Cycle started since bit has been reset 1= Basic Cycle started Default Value: 0

CANFD0_CH0_TTIE

TT Interrupt Enable
Address: 0x40520124
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	GTWE	SWEE	TTMIE	RTMIE	SOGE	CSME	SMCE	SBCE

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	IWTE	ELCE	SE2E	SE1E	TXOE	TXUE	GTEE	GTDE

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [23:19]					CERE	AWE_	WTE

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18	CERE	Configuration Error Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
17	AWE_	Application Watchdog Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
16	WTE	Watch Trigger Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
15	IWTE	Initialization Watch Trigger Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
14	ELCE	Change Error Level Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
13	SE2E	Scheduling Error 2 Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
12	SE1E	Scheduling Error 1 Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

11	TXOE	Tx Count Overflow Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
10	TXUE	Tx Count Underflow Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
9	GTEE	Global Time Error Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
8	GTDE	Global Time Discontinuity Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
7	GTWE	Global Time Wrap Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
6	SWEE	Stop Watch Event Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
5	TTMIE	Trigger Time Mark Event Internal Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
4	RTMIE	Register Time Mark Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
3	SOGE	Start of Gap Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
2	CSME	Change of Synchronization Mode Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
1	SMCE	Start of Matrix Cycle Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
0	SBCE	Start of Basic Cycle Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

CANFD0_CH0_TTILS

TT Interrupt Line Select
Address: 0x40520128
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	GTWL	SWEL	TTMIL	RTMIL	SOGL	CSML	SMCL	SBCL
Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	IWTL	ELCL	SE2L	SE1L	TXOL	TXUL	GTEL	GTDL
Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [23:19]					CERL	AWL_	WTL
Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18	CERL	Configuration Error Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
17	AWL_	Application Watchdog Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
16	WTL	Watch Trigger Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
15	IWTL	Initialization Watch Trigger Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

14	ELCL	Change Error Level Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
13	SE2L	Scheduling Error 2 Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
12	SE1L	Scheduling Error 1 Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
11	TXOL	Tx Count Overflow Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
10	TXUL	Tx Count Underflow Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
9	GTEL	Global Time Error Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
8	GTDL	Global Time Discontinuity Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
7	GTWL	Global Time Wrap Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
6	SWEL	Stop Watch Event Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
5	TTMIL	Trigger Time Mark Event Internal Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

4	RTMIL	Register Time Mark Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
3	SOGL	Start of Gap Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
2	CSML	Change of Synchronization Mode Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
1	SMCL	Start of Matrix Cycle Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
0	SBCL	Start of Basic Cycle Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

CANFD0_CH0_TTOST

TT Operation Status
Address: 0x4052012C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R		R		R	
HW Access	RW	RW	RW		RW		RW	
Name	QCS	QGTP	SYS [5:4]		MS [3:2]		EL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	RTO [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	None					
HW Access	RW	RW	None					
Name	GFI	WGTD	None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	R	R	R		
HW Access	RW	RW	RW	RW	RW	RW		
Name	SPL	WECS	AWE	WFE	GSI	TMP [26:24]		

Bits	Name	Description
31	SPL	Schedule Phase Lock The bit is valid only when external synchronization is enabled (TTOCN.ESCN = '1'). In this case it signals that the difference between cycle time configured by TTGTP.CTP and the cycle time at the rising edge at pin m_ttcan_evt is less or equal 9 NTU (see Section 4.11). 0= Phase outside range 1= Phase inside range Default Value: 0
30	WECS	Wait for External Clock Synchronization 0= No external clock synchronization pending 1= Node waits for external clock synchronization to take effect. The bit is reset at the start of the next basic cycle. Default Value: 0

29	AWE	Application Watchdog Event The application watchdog is served by reading TTOST. When the watchdog is not served in time, bit AWE is set, all TTCAN communication is stopped, and the M_TTCAN is set into Bus Monitoring Mode. 0= Application Watchdog served in time 1= Failed to serve Application Watchdog in time Default Value: 0
28	WFE	Wait for Event 0= No Gap announced, reset by a reference message with Next_is_Gap = '0' 1= Reference message with Next_is_Gap = '1' received Default Value: 0
27	GSI	Gap Started Indicator 0= No Gap in schedule, reset by each reference message and for all time slaves 1= Gap time after Basic Cycle has started Default Value: 0
26 : 24	TMP	Time Master Priority 0x0-7 Priority of actual Time Master Default Value: 0
23	GFI	Gap Finished Indicator Set when the CPU writes TTOCN.FGP, or by a time mark interrupt if TMG = '1', or via input pin m_ttcan_evt if TTOCN.GCS = '1'. Not set by Ref_Trigger_Gap or when Gap is finished by another node sending a reference message. 0= Reset at the end of each reference message 1= Gap finished by M_TTCAN Default Value: 0
22	WGTD	Wait for Global Time Discontinuity 0= No global time preset pending 1= Node waits for the global time preset to take effect. The bit is reset when the node has transmitted a reference message with Disc_Bit = '1' or after it received a reference message. Default Value: 0

15 : 8	RTO	Reference Trigger Offset The Reference Trigger Offset value is a signed integer with a range from -127 (0x81) to 127 (0x7F). There is no notification when the lower limit of -127 is reached. In case the M_TTCAN becomes Time Master (MS[1:0] = '11'), the reset of RTO is delayed due to synchronization between Host and CAN clock domain. For time slaves the value configured by TTOCF.IRTO is read. 0x00-FF Actual Reference Trigger offset value Default Value: 0
7	QCS	Quality of Clock Speed Only relevant in TTCAN Level 0 and Level 2, otherwise fixed to '1'. 0= Local clock speed not synchronized to Time Master clock speed 1= Synchronization Deviation <= SDL Default Value: 1
6	QGTP	Quality of Global Time Phase Only relevant in TTCAN Level 0 and Level 2, otherwise fixed to '0'. 0= Global time not valid 1= Global time in phase with Time Master Default Value: 0
5 : 4	SYS	Synchronization State 00= Out of Synchronization 01= Synchronizing to TTCAN communication 10= Schedule suspended by Gap (In_Gap) 11= Synchronized to schedule (In_Schedule) Default Value: 0
3 : 2	MS	Master State 00= Master_Off, no master properties relevant 01= Operating as Time Slave 10= Operating as Backup Time Master 11= Operating as current Time Master Default Value: 0
1 : 0	EL	Error Level 00= Severity 0 - No Error 01= Severity 1 - Warning 10= Severity 2 - Error 11= Severity 3 - Severe Error Default Value: 0

CANFD0_CH0_TURNA

TUR Numerator Actual
Address: 0x40520130
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	NAV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	NAV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						R	
HW Access	None						RW	
Name	None [23:18]						NAV [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 0	NAV	Numerator Actual Value 0x0EFFF reserved 0x0F000-20FFF Actual numerator value 0x21000 reserved Default Value: 0x10000

CANFD0_CH0_TTLGT

TT Local & Global Time
Address: 0x40520134
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	LT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	LT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	GT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	GT [31:24]							

Bits	Name	Description
31 : 16	GT	Global Time Non-fractional part of the sum of the node's local time and its local offset (see Section 4.5). 0x0000-FFFF Global time value of TTCAN network Default Value: 0
15 : 0	LT	Local Time Non-fractional part of local time, incremented once each local NTU (see Section 4.5). 0x0000-FFFF Local time value of TTCAN node Default Value: 0

CANFD0_CH0_TTCTC

TT Cycle Time & Count
Address: 0x40520138
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		R					
HW Access	None		RW					
Name	None [23:22]		CC [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21 : 16	CC	Cycle Count 0x00-3F Number of actual Basic Cycle in the System Matrix Default Value: 0x3F
15 : 0	CT	Cycle Time Non-fractional part of the difference of the node's local time and Ref_Mark (see Section 4.5). 0x0000-FFFF Cycle time value of TTCAN Basic Cycle Default Value: 0

CANFD0_CH0_TTCPT

TT Capture Time
Address: 0x4052013C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		RW					
Name	None [7:6]		CCV [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	SWV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	SWV [31:24]							

Bits	Name	Description
31 : 16	SWV	Stop Watch Value On a rising/ falling edge (as configured via TTOCN.SWP) at the Stop Watch Trigger pin m_ttcan_swt, when TTOCN.SWS is != '00' and TTIR.SWE is '0', the actual time value as selected by TTOCN.SWS (cycle, local, global) is copied to SWV and TTIR.SWE will be set to '1'. Capturing of the next stop watch value is enabled by resetting TTIR.SWE. 0x0000-FFFF Captured Stop Watch value Default Value: 0
5 : 0	CCV	Cycle Count Value Cycle count value captured together with SWV. 0x00-3F Captured cycle count value Default Value: 0

CANFD0_CH0_TTCSM

TT Cycle Sync Mark
Address: 0x40520140
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CSM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CSM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CSM	Cycle Sync Mark The Cycle Sync Mark is measured Default Value: 0

CANFD0_CH0_RXFTOP_CTL

Receive FIFO Top control
Address: 0x40520180
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						F1TPE	F0TPE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	F1TPE	FIFO 1 Top Pointer Enable. Default Value: 0
0	F0TPE	FIFO 0 Top Pointer Enable. This enables the FIFO top pointer logic to set the FIFO Top Address (FnTA) and message word counter. This logic is also disabled when the IP is being reconfigured (CCCR.CCE=1). When this logic is disabled a Read from RXFTOP0_DATA is undefined. Default Value: 0

CANFD0_CH0_RXFTOP0_STAT

Receive FIFO 0 Top Status
Address: 0x405201A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	F0TA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	F0TA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	F0TA	Current FIFO 0 Top Address. This is a pointer to the next word in the message buffer defined by the FIFO Start Address (FnSA), Get Index (FnGI), the FIFO message size (FnDS) and the message word counter (FnMWC) FnTA = FnSA + FnGI * msg_size[FnDS] + FnMWC Default Value: 0

CANFD0_CH0_RXFTOP0_DATA

Receive FIFO 0 Top Data
Address: 0x405201A8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	F0TD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	F0TD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	F0TD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	F0TD [31:24]							

Bits	Name	Description
31 : 0	F0TD	When enabled (F0TPE=1) read data from MRAM at location FnTA. This register can have a read side effect if the following conditions are met: - M_TTCAN not being reconfigured (CCCR.CCE=0) - FIFO Top Pointer logic is enabled (FnTPE=1) - FIFO is not empty (FnFL!=0) The read side effect is as follows: - if FnMWC pointed to the last word of the message (as indicated by FnDS) then the corresponding message index (FnGI) is automatically acknowledge by a write to FnAI - FnMWC is incremented (or restarted if FnMWC pointed to the last word of the message) - the FIFO top address FnTA is incremented (with FIFO wrap around) When this logic is disabled (F0TPE=0) a Read from this register returns undefined data. Default Value: Undefined

CANFD0_CH0_RXFTOP1_STAT

Receive FIFO 1 Top Status
Address: 0x405201B0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	F1TA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	F1TA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	F1TA	See F0TA description Default Value: 0

CANFD0_CH0_RXFTOP1_DATA

Receive FIFO 1 Top Data
Address: 0x405201B8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	F1TD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	F1TD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	F1TD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	F1TD [31:24]							

Bits	Name	Description
31 : 0	F1TD	See F0TD description Default Value: Undefined

CANFD0_CTL

Global CAN control register
Address: 0x40521000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					STOP_REQ [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	MRAM_OFF	None [30:24]						

Bits	Name	Description
31	MRAM_OFF	MRAM off 0= Default MRAM on (with MRAM retained in DeepSleep). 1= Switch MRAM off (not retained) to save power. Before setting this bit all the CAN channels have to be powered down using the STOP_REQ/ACK bits. When the MRAM is off any access attempt to it is considered an address error (as if MRAM_SIZE=0). After switching the MRAM on again software needs to allow for a certain power up time before MRAM can be used, i.e. before STOP_REQ can be de-asserted. The power up time is equivalent to the system SRAM power up time specified in the CPUSS.RAM_PWR_DELAY_CTL register. MRAM_OFF should be set to 0 prior to transitioning to Hibernate mode. Default Value: 0

2 : 0	STOP_REQ	Clock Stop Request for each TTCAN IP . The m_ttcan_clkstop_req of each TTCAN IP is directly driven by these bits. Default Value: 0

CANFD0_STATUS

Global CAN status register
Address: 0x40521004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R		
HW Access	None					RW		
Name	None [7:3]					STOP_ACK [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	STOP_ACK	Clock Stop Acknowledge for each TTCAN IP. These bits are directly driven by m_ttcan_clkstop_ack of each TTCAN IP. When this bit is set the corresponding TTCAN IP clocks will be gated off, except HCLK will enabled for each AHB write Default Value: 0

CANFD0_INTR0_CAUSE

Consolidated interrupt0 cause register
Address: 0x40521010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R		
HW Access	None					RW		
Name	None [7:3]					INT0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	INT0	Show pending m_ttcan_int0 of each channel Default Value: 0

CANFD0_INTR1_CAUSE

Consolidated interrupt1 cause register
Address: 0x40521014
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R		
HW Access	None					RW		
Name	None [7:3]					INT1 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	INT1	Show pending m_ttcan_int1 of each channel Default Value: 0

CANFD0_TS_CTL

Time Stamp control register
Address: 0x40521020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PRESCALE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PRESCALE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	Counter enable bit 0 = Count disabled. Stop counting up and keep the counter value 1 = Count enabled. Start counting up from the current value Default Value: 0
15 : 0	PRESCALE	Time Stamp counter prescale value. When enabled divide the Host clock (HCLK) by PRESCALE+1 to create Time Stamp clock ticks. Default Value: 0

CANFD0_TS_CNT

Time Stamp counter value
Address: 0x40521024
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	VALUE	The counter value of the Time Stamp Counter. When enabled this counter will count Time Stamp clock ticks from the pre-scaler. When written this counter and the pre-scaler will reset to 0 (write data is ignored). Default Value: 0

CANFD0_ECC_CTL

ECC control
Address: 0x40521080
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							ECC_EN

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	ECC_EN	Enable ECC for CANFD SRAM When disabled also all error injection functionality is disabled. Default Value: 0

CANFD0_ECC_ERR_INJ

ECC error injection
Address: 0x40521084
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	ERR_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ERR_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	None			
HW Access	None			R	None			
Name	None [23:21]			ERR_EN	None [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	ERR_PAR [30:24]						

Bits	Name	Description
30 : 24	ERR_PAR	ECC Parity bits to use for ECC error injection at address ERR_ADDR. Default Value: 0
20	ERR_EN	Enable error injection (ECC_EN must be 1). When this bit is set the error parity (ERR_PAR) will be used when an AHB write is done to the ERR_ADDR address. When the error word is read a single or double error will be reported to the fault structure just like for a real ECC error (even if this bit is no longer set). When this bit is set (and ECC_EN=1) a non-correctable error (ECC or address error) for the ERR_ADDR will not be reported back to the CAN channel or AHB bus. Default Value: 0

15 : 2	ERR_ADDR	Specifies the address of the word where an error will be injected on write or an non-correctable error will be suppressed. When the ERR_EN bit is set an error parity (ERR_PAR) is injected when any write, from bus or a CAN channel, is done to this address. When the ERR_EN bit is set and the access address matches ERR_ADDR then a non-correctable ECC error or an Address error will NOT result in a bus error or CAN channel shutdown. Note that error reporting to the fault structure cannot be suppressed. Default Value: 0x3FFF

13 Serial Communication Block (SCB)

Register details

Register names	Address	Description
SCB0_CTRL	0x40600000	Generic control
SCB0_STATUS	0x40600004	Generic status
SCB0_CMD_RESP_CTRL	0x40600008	Command/response control
SCB0_CMD_RESP_STATUS	0x4060000C	Command/response status
SCB0_SPI_CTRL	0x40600020	SPI control
SCB0_SPI_STATUS	0x40600024	SPI status
SCB0_SPI_TX_CTRL	0x40600028	SPI transmitter control
SCB0_SPI_RX_CTRL	0x4060002C	SPI receiver control
SCB0_UART_CTRL	0x40600040	UART control
SCB0_UART_TX_CTRL	0x40600044	UART transmitter control
SCB0_UART_RX_CTRL	0x40600048	UART receiver control
SCB0_UART_RX_STATUS	0x4060004C	UART receiver status
SCB0_UART_FLOW_CTRL	0x40600050	UART flow control
SCB0_I2C_CTRL	0x40600060	I2C control
SCB0_I2C_STATUS	0x40600064	I2C status
SCB0_I2C_M_CMD	0x40600068	I2C master command
SCB0_I2C_S_CMD	0x4060006C	I2C slave command
SCB0_I2C_CFG	0x40600070	I2C configuration
SCB0_TX_CTRL	0x40600200	Transmitter control
SCB0_TX_FIFO_CTRL	0x40600204	Transmitter FIFO control
SCB0_TX_FIFO_STATUS	0x40600208	Transmitter FIFO status
SCB0_TX_FIFO_WR	0x40600240	Transmitter FIFO write
SCB0_RX_CTRL	0x40600300	Receiver control
SCB0_RX_FIFO_CTRL	0x40600304	Receiver FIFO control
SCB0_RX_FIFO_STATUS	0x40600308	Receiver FIFO status
SCB0_RX_MATCH	0x40600310	Slave address and mask
SCB0_RX_FIFO_RD	0x40600340	Receiver FIFO read
SCB0_RX_FIFO_RD_SILENT	0x40600344	Receiver FIFO read silent
SCB0_EZ_DATA0	0x40600400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB0_EZ_DATA0 to SCB0_EZ_DATA255).
SCB0_INTR_CAUSE	0x40600E00	Active clocked interrupt signal
SCB0_INTR_I2C_EC	0x40600E80	Externally clocked I2C interrupt request
SCB0_INTR_I2C_EC_MASK	0x40600E88	Externally clocked I2C interrupt mask
SCB0_INTR_I2C_EC_MASKED	0x40600E8C	Externally clocked I2C interrupt masked

Register names	Address	Description
SCB0_INTR_SPI_EC	0x40600EC0	Externally clocked SPI interrupt request
SCB0_INTR_SPI_EC_MASK	0x40600EC8	Externally clocked SPI interrupt mask
SCB0_INTR_SPI_EC_MASKED	0x40600ECC	Externally clocked SPI interrupt masked
SCB0_INTR_M	0x40600F00	Master interrupt request
SCB0_INTR_M_SET	0x40600F04	Master interrupt set request
SCB0_INTR_M_MASK	0x40600F08	Master interrupt mask
SCB0_INTR_M_MASKED	0x40600F0C	Master interrupt masked request
SCB0_INTR_S	0x40600F40	Slave interrupt request
SCB0_INTR_S_SET	0x40600F44	Slave interrupt set request
SCB0_INTR_S_MASK	0x40600F48	Slave interrupt mask
SCB0_INTR_S_MASKED	0x40600F4C	Slave interrupt masked request
SCB0_INTR_TX	0x40600F80	Transmitter interrupt request
SCB0_INTR_TX_SET	0x40600F84	Transmitter interrupt set request
SCB0_INTR_TX_MASK	0x40600F88	Transmitter interrupt mask
SCB0_INTR_TX_MASKED	0x40600F8C	Transmitter interrupt masked request
SCB0_INTR_RX	0x40600FC0	Receiver interrupt request
SCB0_INTR_RX_SET	0x40600FC4	Receiver interrupt set request
SCB0_INTR_RX_MASK	0x40600FC8	Receiver interrupt mask
SCB0_INTR_RX_MASKED	0x40600FCC	Receiver interrupt masked request
SCB1_CTRL	0x40610000	Generic control
SCB1_STATUS	0x40610004	Generic status. See SCB0_STATUS for the details of bit fields.
SCB1_SPI_CTRL	0x40610020	SPI control. See SCB0_SPI_CTRL for the details of bit fields.
SCB1_SPI_STATUS	0x40610024	SPI status. See SCB0_SPI_STATUS for the details of bit fields.
SCB1_SPI_TX_CTRL	0x40610028	SPI transmitter control. See SCB0_SPI_TX_CTRL for the details of bit fields.
SCB1_SPI_RX_CTRL	0x4061002C	SPI receiver control. See SCB0_SPI_RX_CTRL for the details of bit fields.
SCB1_UART_CTRL	0x40610040	UART control. See SCB0_UART_CTRL for the details of bit fields.
SCB1_UART_TX_CTRL	0x40610044	UART transmitter control. See SCB0_UART_TX_CTRL for the details of bit fields.
SCB1_UART_RX_CTRL	0x40610048	UART receiver control. See SCB0_UART_RX_CTRL for the details of bit fields.
SCB1_UART_RX_STATUS	0x4061004C	UART receiver status. See SCB0_UART_RX_STATUS for the details of bit fields.
SCB1_UART_FLOW_CTRL	0x40610050	UART flow control. See SCB0_UART_FLOW_CTRL for the details of bit fields.

Register names	Address	Description
SCB1_I2C_CTRL	0x40610060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB1_I2C_STATUS	0x40610064	I2C status
SCB1_I2C_M_CMD	0x40610068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB1_I2C_S_CMD	0x4061006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB1_I2C_CFG	0x40610070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB1_TX_CTRL	0x40610200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB1_TX_FIFO_CTRL	0x40610204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB1_TX_FIFO_STATUS	0x40610208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB1_TX_FIFO_WR	0x40610240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB1_RX_CTRL	0x40610300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB1_RX_FIFO_CTRL	0x40610304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB1_RX_FIFO_STATUS	0x40610308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB1_RX_MATCH	0x40610310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB1_RX_FIFO_RD	0x40610340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.
SCB1_RX_FIFO_RD_SILENT	0x40610344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB1_EZ_DATA0	0x40610400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB1_EZ_DATA0 to SCB1_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_INTR_CAUSE	0x40610E00	Active clocked interrupt signal
SCB1_INTR_SPI_EC	0x40610EC0	Externally clocked SPI interrupt request. See SCB0_INTR_SPI_EC for the details of bit fields.
SCB1_INTR_SPI_EC_MASK	0x40610EC8	Externally clocked SPI interrupt mask. See SCB0_INTR_SPI_EC_MASK for the details of bit fields.
SCB1_INTR_SPI_EC_MASKED	0x40610ECC	Externally clocked SPI interrupt masked. See SCB0_INTR_SPI_EC_MASKED for the details of bit fields.
SCB1_INTR_M	0x40610F00	Master interrupt request. See SCB0_INTR_M for the details of bit fields.
SCB1_INTR_M_SET	0x40610F04	Master interrupt set request. See SCB0_INTR_M_SET for the details of bit fields.

Register names	Address	Description
SCB1_INTR_M_MASK	0x40610F08	Master interrupt mask. See SCB0_INTR_M_MASK for the details of bit fields.
SCB1_INTR_M_MASKED	0x40610F0C	Master interrupt masked request. See SCB0_INTR_M_MASKED for the details of bit fields.
SCB1_INTR_S	0x40610F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB1_INTR_S_SET	0x40610F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB1_INTR_S_MASK	0x40610F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB1_INTR_S_MASKED	0x40610F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB1_INTR_TX	0x40610F80	Transmitter interrupt request. See SCB0_INTR_TX for the details of bit fields.
SCB1_INTR_TX_SET	0x40610F84	Transmitter interrupt set request. See SCB0_INTR_TX_SET for the details of bit fields.
SCB1_INTR_TX_MASK	0x40610F88	Transmitter interrupt mask. See SCB0_INTR_TX_MASK for the details of bit fields.
SCB1_INTR_TX_MASKED	0x40610F8C	Transmitter interrupt masked request. See SCB0_INTR_TX_MASKED for the details of bit fields.
SCB1_INTR_RX	0x40610FC0	Receiver interrupt request. See SCB0_INTR_RX for the details of bit fields.
SCB1_INTR_RX_SET	0x40610FC4	Receiver interrupt set request. See SCB0_INTR_RX_SET for the details of bit fields.
SCB1_INTR_RX_MASK	0x40610FC8	Receiver interrupt mask. See SCB0_INTR_RX_MASK for the details of bit fields.
SCB1_INTR_RX_MASKED	0x40610FCC	Receiver interrupt masked request. See SCB0_INTR_RX_MASKED for the details of bit fields.
SCB2_CTRL	0x40620000	Generic control. See SCB1_CTRL for the details of bit fields.
SCB2_STATUS	0x40620004	Generic status. See SCB0_STATUS for the details of bit fields.
SCB2_SPI_CTRL	0x40620020	SPI control. See SCB0_SPI_CTRL for the details of bit fields.
SCB2_SPI_STATUS	0x40620024	SPI status. See SCB0_SPI_STATUS for the details of bit fields.
SCB2_SPI_TX_CTRL	0x40620028	SPI transmitter control. See SCB0_SPI_TX_CTRL for the details of bit fields.
SCB2_SPI_RX_CTRL	0x4062002C	SPI receiver control. See SCB0_SPI_RX_CTRL for the details of bit fields.
SCB2_UART_CTRL	0x40620040	UART control. See SCB0_UART_CTRL for the details of bit fields.
SCB2_UART_TX_CTRL	0x40620044	UART transmitter control. See SCB0_UART_TX_CTRL for the details of bit fields.

Register names	Address	Description
SCB2_UART_RX_CTRL	0x40620048	UART receiver control. See SCB0_UART_RX_CTRL for the details of bit fields.
SCB2_UART_RX_STATUS	0x4062004C	UART receiver status. See SCB0_UART_RX_STATUS for the details of bit fields.
SCB2_UART_FLOW_CTRL	0x40620050	UART flow control. See SCB0_UART_FLOW_CTRL for the details of bit fields.
SCB2_I2C_CTRL	0x40620060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB2_I2C_STATUS	0x40620064	I2C status. See SCB1_I2C_STATUS for the details of bit fields.
SCB2_I2C_M_CMD	0x40620068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB2_I2C_S_CMD	0x4062006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB2_I2C_CFG	0x40620070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB2_TX_CTRL	0x40620200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB2_TX_FIFO_CTRL	0x40620204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB2_TX_FIFO_STATUS	0x40620208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB2_TX_FIFO_WR	0x40620240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB2_RX_CTRL	0x40620300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB2_RX_FIFO_CTRL	0x40620304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB2_RX_FIFO_STATUS	0x40620308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB2_RX_MATCH	0x40620310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB2_RX_FIFO_RD	0x40620340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.
SCB2_RX_FIFO_RD_SILENT	0x40620344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB2_EZ_DATA0	0x40620400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB2_EZ_DATA0 to SCB2_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_INTR_CAUSE	0x40620E00	Active clocked interrupt signal. See SCB1_INTR_CAUSE for the details of bit fields.
SCB2_INTR_SPI_EC	0x40620EC0	Externally clocked SPI interrupt request. See SCB0_INTR_SPI_EC for the details of bit fields.
SCB2_INTR_SPI_EC_MASK	0x40620EC8	Externally clocked SPI interrupt mask. See SCB0_INTR_SPI_EC_MASK for the details of bit fields.

Register names	Address	Description
SCB2_INTR_SPI_EC_MASKED	0x40620ECC	Externally clocked SPI interrupt masked. See SCB0_INTR_SPI_EC_MASKED for the details of bit fields.
SCB2_INTR_M	0x40620F00	Master interrupt request. See SCB0_INTR_M for the details of bit fields.
SCB2_INTR_M_SET	0x40620F04	Master interrupt set request. See SCB0_INTR_M_SET for the details of bit fields.
SCB2_INTR_M_MASK	0x40620F08	Master interrupt mask. See SCB0_INTR_M_MASK for the details of bit fields.
SCB2_INTR_M_MASKED	0x40620F0C	Master interrupt masked request. See SCB0_INTR_M_MASKED for the details of bit fields.
SCB2_INTR_S	0x40620F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB2_INTR_S_SET	0x40620F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB2_INTR_S_MASK	0x40620F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB2_INTR_S_MASKED	0x40620F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB2_INTR_TX	0x40620F80	Transmitter interrupt request. See SCB0_INTR_TX for the details of bit fields.
SCB2_INTR_TX_SET	0x40620F84	Transmitter interrupt set request. See SCB0_INTR_TX_SET for the details of bit fields.
SCB2_INTR_TX_MASK	0x40620F88	Transmitter interrupt mask. See SCB0_INTR_TX_MASK for the details of bit fields.
SCB2_INTR_TX_MASKED	0x40620F8C	Transmitter interrupt masked request. See SCB0_INTR_TX_MASKED for the details of bit fields.
SCB2_INTR_RX	0x40620FC0	Receiver interrupt request. See SCB0_INTR_RX for the details of bit fields.
SCB2_INTR_RX_SET	0x40620FC4	Receiver interrupt set request. See SCB0_INTR_RX_SET for the details of bit fields.
SCB2_INTR_RX_MASK	0x40620FC8	Receiver interrupt mask. See SCB0_INTR_RX_MASK for the details of bit fields.
SCB2_INTR_RX_MASKED	0x40620FCC	Receiver interrupt masked request. See SCB0_INTR_RX_MASKED for the details of bit fields.
SCB3_CTRL	0x40630000	Generic control. See SCB1_CTRL for the details of bit fields.
SCB3_STATUS	0x40630004	Generic status. See SCB0_STATUS for the details of bit fields.
SCB3_SPI_CTRL	0x40630020	SPI control. See SCB0_SPI_CTRL for the details of bit fields.
SCB3_SPI_STATUS	0x40630024	SPI status. See SCB0_SPI_STATUS for the details of bit fields.
SCB3_SPI_TX_CTRL	0x40630028	SPI transmitter control. See SCB0_SPI_TX_CTRL for the details of bit fields.

Register names	Address	Description
SCB3_SPI_RX_CTRL	0x4063002C	SPI receiver control. See SCB0_SPI_RX_CTRL for the details of bit fields.
SCB3_UART_CTRL	0x40630040	UART control. See SCB0_UART_CTRL for the details of bit fields.
SCB3_UART_TX_CTRL	0x40630044	UART transmitter control. See SCB0_UART_TX_CTRL for the details of bit fields.
SCB3_UART_RX_CTRL	0x40630048	UART receiver control. See SCB0_UART_RX_CTRL for the details of bit fields.
SCB3_UART_RX_STATUS	0x4063004C	UART receiver status. See SCB0_UART_RX_STATUS for the details of bit fields.
SCB3_UART_FLOW_CTRL	0x40630050	UART flow control. See SCB0_UART_FLOW_CTRL for the details of bit fields.
SCB3_I2C_CTRL	0x40630060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB3_I2C_STATUS	0x40630064	I2C status. See SCB1_I2C_STATUS for the details of bit fields.
SCB3_I2C_M_CMD	0x40630068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB3_I2C_S_CMD	0x4063006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB3_I2C_CFG	0x40630070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB3_TX_CTRL	0x40630200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB3_TX_FIFO_CTRL	0x40630204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB3_TX_FIFO_STATUS	0x40630208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB3_TX_FIFO_WR	0x40630240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB3_RX_CTRL	0x40630300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB3_RX_FIFO_CTRL	0x40630304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB3_RX_FIFO_STATUS	0x40630308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB3_RX_MATCH	0x40630310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB3_RX_FIFO_RD	0x40630340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.
SCB3_RX_FIFO_RD_SILENT	0x40630344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB3_EZ_DATA0	0x40630400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB3_EZ_DATA0 to SCB3_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.

Register names	Address	Description
SCB3_INTR_CAUSE	0x40630E00	Active clocked interrupt signal. See SCB1_INTR_CAUSE for the details of bit fields.
SCB3_INTR_SPI_EC	0x40630EC0	Externally clocked SPI interrupt request. See SCB0_INTR_SPI_EC for the details of bit fields.
SCB3_INTR_SPI_EC_MASK	0x40630EC8	Externally clocked SPI interrupt mask. See SCB0_INTR_SPI_EC_MASK for the details of bit fields.
SCB3_INTR_SPI_EC_MASKED	0x40630ECC	Externally clocked SPI interrupt masked. See SCB0_INTR_SPI_EC_MASKED for the details of bit fields.
SCB3_INTR_M	0x40630F00	Master interrupt request. See SCB0_INTR_M for the details of bit fields.
SCB3_INTR_M_SET	0x40630F04	Master interrupt set request. See SCB0_INTR_M_SET for the details of bit fields.
SCB3_INTR_M_MASK	0x40630F08	Master interrupt mask. See SCB0_INTR_M_MASK for the details of bit fields.
SCB3_INTR_M_MASKED	0x40630F0C	Master interrupt masked request. See SCB0_INTR_M_MASKED for the details of bit fields.
SCB3_INTR_S	0x40630F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB3_INTR_S_SET	0x40630F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB3_INTR_S_MASK	0x40630F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB3_INTR_S_MASKED	0x40630F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB3_INTR_TX	0x40630F80	Transmitter interrupt request. See SCB0_INTR_TX for the details of bit fields.
SCB3_INTR_TX_SET	0x40630F84	Transmitter interrupt set request. See SCB0_INTR_TX_SET for the details of bit fields.
SCB3_INTR_TX_MASK	0x40630F88	Transmitter interrupt mask. See SCB0_INTR_TX_MASK for the details of bit fields.
SCB3_INTR_TX_MASKED	0x40630F8C	Transmitter interrupt masked request. See SCB0_INTR_TX_MASKED for the details of bit fields.
SCB3_INTR_RX	0x40630FC0	Receiver interrupt request. See SCB0_INTR_RX for the details of bit fields.
SCB3_INTR_RX_SET	0x40630FC4	Receiver interrupt set request. See SCB0_INTR_RX_SET for the details of bit fields.
SCB3_INTR_RX_MASK	0x40630FC8	Receiver interrupt mask. See SCB0_INTR_RX_MASK for the details of bit fields.
SCB3_INTR_RX_MASKED	0x40630FCC	Receiver interrupt masked request. See SCB0_INTR_RX_MASKED for the details of bit fields.
SCB4_CTRL	0x40640000	Generic control. See SCB1_CTRL for the details of bit fields.
SCB4_STATUS	0x40640004	Generic status. See SCB0_STATUS for the details of bit fields.

Register names	Address	Description
SCB4_SPI_CTRL	0x40640020	SPI control. See SCB0_SPI_CTRL for the details of bit fields.
SCB4_SPI_STATUS	0x40640024	SPI status. See SCB0_SPI_STATUS for the details of bit fields.
SCB4_SPI_TX_CTRL	0x40640028	SPI transmitter control. See SCB0_SPI_TX_CTRL for the details of bit fields.
SCB4_SPI_RX_CTRL	0x4064002C	SPI receiver control. See SCB0_SPI_RX_CTRL for the details of bit fields.
SCB4_UART_CTRL	0x40640040	UART control. See SCB0_UART_CTRL for the details of bit fields.
SCB4_UART_TX_CTRL	0x40640044	UART transmitter control. See SCB0_UART_TX_CTRL for the details of bit fields.
SCB4_UART_RX_CTRL	0x40640048	UART receiver control. See SCB0_UART_RX_CTRL for the details of bit fields.
SCB4_UART_RX_STATUS	0x4064004C	UART receiver status. See SCB0_UART_RX_STATUS for the details of bit fields.
SCB4_UART_FLOW_CTRL	0x40640050	UART flow control. See SCB0_UART_FLOW_CTRL for the details of bit fields.
SCB4_I2C_CTRL	0x40640060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB4_I2C_STATUS	0x40640064	I2C status. See SCB1_I2C_STATUS for the details of bit fields.
SCB4_I2C_M_CMD	0x40640068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB4_I2C_S_CMD	0x4064006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB4_I2C_CFG	0x40640070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB4_TX_CTRL	0x40640200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB4_TX_FIFO_CTRL	0x40640204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB4_TX_FIFO_STATUS	0x40640208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB4_TX_FIFO_WR	0x40640240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB4_RX_CTRL	0x40640300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB4_RX_FIFO_CTRL	0x40640304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB4_RX_FIFO_STATUS	0x40640308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB4_RX_MATCH	0x40640310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.

Register names	Address	Description
SCB4_RX_FIFO_RD	0x40640340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.
SCB4_RX_FIFO_RD_SILENT	0x40640344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB4_EZ_DATA0	0x40640400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB4_EZ_DATA0 to SCB4_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_INTR_CAUSE	0x40640E00	Active clocked interrupt signal. See SCB1_INTR_CAUSE for the details of bit fields.
SCB4_INTR_SPI_EC	0x40640EC0	Externally clocked SPI interrupt request. See SCB0_INTR_SPI_EC for the details of bit fields.
SCB4_INTR_SPI_EC_MASK	0x40640EC8	Externally clocked SPI interrupt mask. See SCB0_INTR_SPI_EC_MASK for the details of bit fields.
SCB4_INTR_SPI_EC_MASKED	0x40640ECC	Externally clocked SPI interrupt masked. See SCB0_INTR_SPI_EC_MASKED for the details of bit fields.
SCB4_INTR_M	0x40640F00	Master interrupt request. See SCB0_INTR_M for the details of bit fields.
SCB4_INTR_M_SET	0x40640F04	Master interrupt set request. See SCB0_INTR_M_SET for the details of bit fields.
SCB4_INTR_M_MASK	0x40640F08	Master interrupt mask. See SCB0_INTR_M_MASK for the details of bit fields.
SCB4_INTR_M_MASKED	0x40640F0C	Master interrupt masked request. See SCB0_INTR_M_MASKED for the details of bit fields.
SCB4_INTR_S	0x40640F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB4_INTR_S_SET	0x40640F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB4_INTR_S_MASK	0x40640F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB4_INTR_S_MASKED	0x40640F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB4_INTR_TX	0x40640F80	Transmitter interrupt request. See SCB0_INTR_TX for the details of bit fields.
SCB4_INTR_TX_SET	0x40640F84	Transmitter interrupt set request. See SCB0_INTR_TX_SET for the details of bit fields.
SCB4_INTR_TX_MASK	0x40640F88	Transmitter interrupt mask. See SCB0_INTR_TX_MASK for the details of bit fields.
SCB4_INTR_TX_MASKED	0x40640F8C	Transmitter interrupt masked request. See SCB0_INTR_TX_MASKED for the details of bit fields.
SCB4_INTR_RX	0x40640FC0	Receiver interrupt request. See SCB0_INTR_RX for the details of bit fields.
SCB4_INTR_RX_SET	0x40640FC4	Receiver interrupt set request. See SCB0_INTR_RX_SET for the details of bit fields.

Register names	Address	Description
SCB4_INTR_RX_MASK	0x40640FC8	Receiver interrupt mask. See SCB0_INTR_RX_MASK for the details of bit fields.
SCB4_INTR_RX_MASKED	0x40640FCC	Receiver interrupt masked request. See SCB0_INTR_RX_MASKED for the details of bit fields.
SCB5_CTRL	0x40650000	Generic control. See SCB1_CTRL for the details of bit fields.
SCB5_STATUS	0x40650004	Generic status. See SCB0_STATUS for the details of bit fields.
SCB5_SPI_CTRL	0x40650020	SPI control. See SCB0_SPI_CTRL for the details of bit fields.
SCB5_SPI_STATUS	0x40650024	SPI status. See SCB0_SPI_STATUS for the details of bit fields.
SCB5_SPI_TX_CTRL	0x40650028	SPI transmitter control. See SCB0_SPI_TX_CTRL for the details of bit fields.
SCB5_SPI_RX_CTRL	0x4065002C	SPI receiver control. See SCB0_SPI_RX_CTRL for the details of bit fields.
SCB5_UART_CTRL	0x40650040	UART control. See SCB0_UART_CTRL for the details of bit fields.
SCB5_UART_TX_CTRL	0x40650044	UART transmitter control. See SCB0_UART_TX_CTRL for the details of bit fields.
SCB5_UART_RX_CTRL	0x40650048	UART receiver control. See SCB0_UART_RX_CTRL for the details of bit fields.
SCB5_UART_RX_STATUS	0x4065004C	UART receiver status. See SCB0_UART_RX_STATUS for the details of bit fields.
SCB5_UART_FLOW_CTRL	0x40650050	UART flow control. See SCB0_UART_FLOW_CTRL for the details of bit fields.
SCB5_I2C_CTRL	0x40650060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB5_I2C_STATUS	0x40650064	I2C status. See SCB1_I2C_STATUS for the details of bit fields.
SCB5_I2C_M_CMD	0x40650068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB5_I2C_S_CMD	0x4065006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB5_I2C_CFG	0x40650070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB5_TX_CTRL	0x40650200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB5_TX_FIFO_CTRL	0x40650204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB5_TX_FIFO_STATUS	0x40650208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB5_TX_FIFO_WR	0x40650240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.

Register names	Address	Description
SCB5_RX_CTRL	0x40650300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB5_RX_FIFO_CTRL	0x40650304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB5_RX_FIFO_STATUS	0x40650308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB5_RX_MATCH	0x40650310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB5_RX_FIFO_RD	0x40650340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.
SCB5_RX_FIFO_RD_SILENT	0x40650344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB5_EZ_DATA0	0x40650400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB5_EZ_DATA0 to SCB5_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.
SCB5_INTR_CAUSE	0x40650E00	Active clocked interrupt signal. See SCB1_INTR_CAUSE for the details of bit fields.
SCB5_INTR_SPI_EC	0x40650EC0	Externally clocked SPI interrupt request. See SCB0_INTR_SPI_EC for the details of bit fields.
SCB5_INTR_SPI_EC_MASK	0x40650EC8	Externally clocked SPI interrupt mask. See SCB0_INTR_SPI_EC_MASK for the details of bit fields.
SCB5_INTR_SPI_EC_MASKED	0x40650ECC	Externally clocked SPI interrupt masked. See SCB0_INTR_SPI_EC_MASKED for the details of bit fields.
SCB5_INTR_M	0x40650F00	Master interrupt request. See SCB0_INTR_M for the details of bit fields.
SCB5_INTR_M_SET	0x40650F04	Master interrupt set request. See SCB0_INTR_M_SET for the details of bit fields.
SCB5_INTR_M_MASK	0x40650F08	Master interrupt mask. See SCB0_INTR_M_MASK for the details of bit fields.
SCB5_INTR_M_MASKED	0x40650F0C	Master interrupt masked request. See SCB0_INTR_M_MASKED for the details of bit fields.
SCB5_INTR_S	0x40650F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB5_INTR_S_SET	0x40650F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB5_INTR_S_MASK	0x40650F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB5_INTR_S_MASKED	0x40650F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB5_INTR_TX	0x40650F80	Transmitter interrupt request. See SCB0_INTR_TX for the details of bit fields.
SCB5_INTR_TX_SET	0x40650F84	Transmitter interrupt set request. See SCB0_INTR_TX_SET for the details of bit fields.

Register names	Address	Description
SCB5_INTR_TX_MASK	0x40650F88	Transmitter interrupt mask. See SCB0_INTR_TX_MASK for the details of bit fields.
SCB5_INTR_TX_MASKED	0x40650F8C	Transmitter interrupt masked request. See SCB0_INTR_TX_MASKED for the details of bit fields.
SCB5_INTR_RX	0x40650FC0	Receiver interrupt request. See SCB0_INTR_RX for the details of bit fields.
SCB5_INTR_RX_SET	0x40650FC4	Receiver interrupt set request. See SCB0_INTR_RX_SET for the details of bit fields.
SCB5_INTR_RX_MASK	0x40650FC8	Receiver interrupt mask. See SCB0_INTR_RX_MASK for the details of bit fields.
SCB5_INTR_RX_MASKED	0x40650FCC	Receiver interrupt masked request. See SCB0_INTR_RX_MASKED for the details of bit fields.
SCB6_CTRL	0x40660000	Generic control. See SCB1_CTRL for the details of bit fields.
SCB6_STATUS	0x40660004	Generic status. See SCB0_STATUS for the details of bit fields.
SCB6_SPI_CTRL	0x40660020	SPI control. See SCB0_SPI_CTRL for the details of bit fields.
SCB6_SPI_STATUS	0x40660024	SPI status. See SCB0_SPI_STATUS for the details of bit fields.
SCB6_SPI_TX_CTRL	0x40660028	SPI transmitter control. See SCB0_SPI_TX_CTRL for the details of bit fields.
SCB6_SPI_RX_CTRL	0x4066002C	SPI receiver control. See SCB0_SPI_RX_CTRL for the details of bit fields.
SCB6_UART_CTRL	0x40660040	UART control. See SCB0_UART_CTRL for the details of bit fields.
SCB6_UART_TX_CTRL	0x40660044	UART transmitter control. See SCB0_UART_TX_CTRL for the details of bit fields.
SCB6_UART_RX_CTRL	0x40660048	UART receiver control. See SCB0_UART_RX_CTRL for the details of bit fields.
SCB6_UART_RX_STATUS	0x4066004C	UART receiver status. See SCB0_UART_RX_STATUS for the details of bit fields.
SCB6_UART_FLOW_CTRL	0x40660050	UART flow control. See SCB0_UART_FLOW_CTRL for the details of bit fields.
SCB6_I2C_CTRL	0x40660060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB6_I2C_STATUS	0x40660064	I2C status. See SCB1_I2C_STATUS for the details of bit fields.
SCB6_I2C_M_CMD	0x40660068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB6_I2C_S_CMD	0x4066006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB6_I2C_CFG	0x40660070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.

Register names	Address	Description
SCB6_TX_CTRL	0x40660200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB6_TX_FIFO_CTRL	0x40660204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB6_TX_FIFO_STATUS	0x40660208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB6_TX_FIFO_WR	0x40660240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB6_RX_CTRL	0x40660300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB6_RX_FIFO_CTRL	0x40660304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB6_RX_FIFO_STATUS	0x40660308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB6_RX_MATCH	0x40660310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB6_RX_FIFO_RD	0x40660340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.
SCB6_RX_FIFO_RD_SILENT	0x40660344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB6_EZ_DATA0	0x40660400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB6_EZ_DATA0 to SCB6_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.
SCB6_INTR_CAUSE	0x40660E00	Active clocked interrupt signal. See SCB1_INTR_CAUSE for the details of bit fields.
SCB6_INTR_SPI_EC	0x40660EC0	Externally clocked SPI interrupt request. See SCB0_INTR_SPI_EC for the details of bit fields.
SCB6_INTR_SPI_EC_MASK	0x40660EC8	Externally clocked SPI interrupt mask. See SCB0_INTR_SPI_EC_MASK for the details of bit fields.
SCB6_INTR_SPI_EC_MASKED	0x40660ECC	Externally clocked SPI interrupt masked. See SCB0_INTR_SPI_EC_MASKED for the details of bit fields.
SCB6_INTR_M	0x40660F00	Master interrupt request. See SCB0_INTR_M for the details of bit fields.
SCB6_INTR_M_SET	0x40660F04	Master interrupt set request. See SCB0_INTR_M_SET for the details of bit fields.
SCB6_INTR_M_MASK	0x40660F08	Master interrupt mask. See SCB0_INTR_M_MASK for the details of bit fields.
SCB6_INTR_M_MASKED	0x40660F0C	Master interrupt masked request. See SCB0_INTR_M_MASKED for the details of bit fields.
SCB6_INTR_S	0x40660F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB6_INTR_S_SET	0x40660F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.

Register names	Address	Description
SCB6_INTR_S_MASK	0x40660F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB6_INTR_S_MASKED	0x40660F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB6_INTR_TX	0x40660F80	Transmitter interrupt request. See SCB0_INTR_TX for the details of bit fields.
SCB6_INTR_TX_SET	0x40660F84	Transmitter interrupt set request. See SCB0_INTR_TX_SET for the details of bit fields.
SCB6_INTR_TX_MASK	0x40660F88	Transmitter interrupt mask. See SCB0_INTR_TX_MASK for the details of bit fields.
SCB6_INTR_TX_MASKED	0x40660F8C	Transmitter interrupt masked request. See SCB0_INTR_TX_MASKED for the details of bit fields.
SCB6_INTR_RX	0x40660FC0	Receiver interrupt request. See SCB0_INTR_RX for the details of bit fields.
SCB6_INTR_RX_SET	0x40660FC4	Receiver interrupt set request. See SCB0_INTR_RX_SET for the details of bit fields.
SCB6_INTR_RX_MASK	0x40660FC8	Receiver interrupt mask. See SCB0_INTR_RX_MASK for the details of bit fields.
SCB6_INTR_RX_MASKED	0x40660FCC	Receiver interrupt masked request. See SCB0_INTR_RX_MASKED for the details of bit fields.
SCB7_CTRL	0x40670000	Generic control. See SCB1_CTRL for the details of bit fields.
SCB7_STATUS	0x40670004	Generic status. See SCB0_STATUS for the details of bit fields.
SCB7_SPI_CTRL	0x40670020	SPI control. See SCB0_SPI_CTRL for the details of bit fields.
SCB7_SPI_STATUS	0x40670024	SPI status. See SCB0_SPI_STATUS for the details of bit fields.
SCB7_SPI_TX_CTRL	0x40670028	SPI transmitter control. See SCB0_SPI_TX_CTRL for the details of bit fields.
SCB7_SPI_RX_CTRL	0x4067002C	SPI receiver control. See SCB0_SPI_RX_CTRL for the details of bit fields.
SCB7_UART_CTRL	0x40670040	UART control. See SCB0_UART_CTRL for the details of bit fields.
SCB7_UART_TX_CTRL	0x40670044	UART transmitter control. See SCB0_UART_TX_CTRL for the details of bit fields.
SCB7_UART_RX_CTRL	0x40670048	UART receiver control. See SCB0_UART_RX_CTRL for the details of bit fields.
SCB7_UART_RX_STATUS	0x4067004C	UART receiver status. See SCB0_UART_RX_STATUS for the details of bit fields.
SCB7_UART_FLOW_CTRL	0x40670050	UART flow control. See SCB0_UART_FLOW_CTRL for the details of bit fields.
SCB7_I2C_CTRL	0x40670060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.

Register names	Address	Description
SCB7_I2C_STATUS	0x40670064	I2C status. See SCB1_I2C_STATUS for the details of bit fields.
SCB7_I2C_M_CMD	0x40670068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB7_I2C_S_CMD	0x4067006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB7_I2C_CFG	0x40670070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB7_TX_CTRL	0x40670200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB7_TX_FIFO_CTRL	0x40670204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB7_TX_FIFO_STATUS	0x40670208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB7_TX_FIFO_WR	0x40670240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB7_RX_CTRL	0x40670300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB7_RX_FIFO_CTRL	0x40670304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB7_RX_FIFO_STATUS	0x40670308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB7_RX_MATCH	0x40670310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB7_RX_FIFO_RD	0x40670340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.
SCB7_RX_FIFO_RD_SILENT	0x40670344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB7_EZ_DATA0	0x40670400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB7_EZ_DATA0 to SCB7_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.
SCB7_INTR_CAUSE	0x40670E00	Active clocked interrupt signal. See SCB1_INTR_CAUSE for the details of bit fields.
SCB7_INTR_SPI_EC	0x40670EC0	Externally clocked SPI interrupt request. See SCB0_INTR_SPI_EC for the details of bit fields.
SCB7_INTR_SPI_EC_MASK	0x40670EC8	Externally clocked SPI interrupt mask. See SCB0_INTR_SPI_EC_MASK for the details of bit fields.
SCB7_INTR_SPI_EC_MASKED	0x40670ECC	Externally clocked SPI interrupt masked. See SCB0_INTR_SPI_EC_MASKED for the details of bit fields.
SCB7_INTR_M	0x40670F00	Master interrupt request. See SCB0_INTR_M for the details of bit fields.
SCB7_INTR_M_SET	0x40670F04	Master interrupt set request. See SCB0_INTR_M_SET for the details of bit fields.

Register names	Address	Description
SCB7_INTR_M_MASK	0x40670F08	Master interrupt mask. See SCB0_INTR_M_MASK for the details of bit fields.
SCB7_INTR_M_MASKED	0x40670F0C	Master interrupt masked request. See SCB0_INTR_M_MASKED for the details of bit fields.
SCB7_INTR_S	0x40670F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB7_INTR_S_SET	0x40670F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB7_INTR_S_MASK	0x40670F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB7_INTR_S_MASKED	0x40670F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB7_INTR_TX	0x40670F80	Transmitter interrupt request. See SCB0_INTR_TX for the details of bit fields.
SCB7_INTR_TX_SET	0x40670F84	Transmitter interrupt set request. See SCB0_INTR_TX_SET for the details of bit fields.
SCB7_INTR_TX_MASK	0x40670F88	Transmitter interrupt mask. See SCB0_INTR_TX_MASK for the details of bit fields.
SCB7_INTR_TX_MASKED	0x40670F8C	Transmitter interrupt masked request. See SCB0_INTR_TX_MASKED for the details of bit fields.
SCB7_INTR_RX	0x40670FC0	Receiver interrupt request. See SCB0_INTR_RX for the details of bit fields.
SCB7_INTR_RX_SET	0x40670FC4	Receiver interrupt set request. See SCB0_INTR_RX_SET for the details of bit fields.
SCB7_INTR_RX_MASK	0x40670FC8	Receiver interrupt mask. See SCB0_INTR_RX_MASK for the details of bit fields.
SCB7_INTR_RX_MASKED	0x40670FCC	Receiver interrupt masked request. See SCB0_INTR_RX_MASKED for the details of bit fields.

13.1 SCB registers

SCB0_CTRL

Generic control
Address: 0x40600000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None	RW	None	RW	RW	RW
HW Access	R		None	R	None	R	R	R

Bits	15	14	13	12	11	10	9	8
Name	MEM_WIDTH [15:14]		None	CMD_RESP_MODE	None	EZ_MODE	EC_OP_MODE	EC_AM_MODE
Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						BLOCK	ADDR_ACCEPT
Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	RW	None		RW	None		RW	
HW Access	R	None		R	None		R	
Name	ENABLED	None [30:29]		EC_ACCESS	None [27:26]		MODE [25:24]	

Bits	Name	Description

31	ENABLED	SCB block is enabled ('1') or not ('0'). The proper order in which to initialize SCB is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL registers. This includes selection of a submode, master/slave functionality and transmitter/ receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL register to enable SCB, select the specific operation mode and oversampling factor. Generally when this block is enabled, no control information should be changed. Changes should be made AFTER disabling this block, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the block is re-enabled. Note that disabling the block will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Specific to SPI master case, when SCB is idle, below registers can be changed without disabling SCB block, TX_CTRL TX_FIFO_CTRL RX_CTRL RX_FIFO_CTRL SPI_CTRL.SSEL, Default Value: 0
28	EC_ACCESS	EC_ACCESS is used to enable I2CS_EC or SPIS_EC access to internal EZ memory. 1: enable clk_scb 0: disable clk_scb Before going to deepsleep this field should be set to 1. when waking up from DeepSleep power mode, and PLL is locked (clk_scb is at expected frequency), this filed should be set to 0. Default Value: 0
25 : 24	MODE	Mode of operation (3: Reserved) Default Value: 3
		0x0: I2C : Inter-Integrated Circuits (I2C) mode.

		0x1: SPI : Serial Peripheral Interface (SPI) mode.
		0x2: UART : Universal Asynchronous Receiver/Transmitter (UART) mode.
17	BLOCK	Only used in externally clocked mode. If the externally clocked logic and the internal CPU accesses to EZ memory coincide/collide, this bit determines whether the CPU access should block and result in bus wait states ('BLOCK is 1') or not (BLOCK is '0'). IF BLOCK is '0' and the accesses collide, CPU read operations return 0xffff:ffff and CPU write operations are ignored. Colliding accesses are registered as interrupt causes: INTR_TX.BLOCKED and INTR_RX.BLOCKED. Default Value: 0
16	ADDR_ACCEPT	Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0'). In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when this bit is '1' for both I2C read and write transfers. In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. Default Value: 0
15 : 14	MEM_WIDTH	Determines the number of bits per FIFO data element. Default Value: 1
		0x0: BYTE : 8-bit FIFO data elements. This mode provides the biggest amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7].
		0x1: HALFWORD : 16-bit FIFO data elements. TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 15].
		0x2: WORD : 32-bit FIFO data elements. This mode provides the smallest amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH can be in a range of [0, 31].

		0x3: Reserved : This setting is reserved. Do not use.
12	CMD_RESP_MODE	Determines CMD_RESP mode of operation: '0': CMD_RESP mode disabled. '1': CMD_RESP mode enabled (also requires EC_AM_MODE and EC_OP_MODE to be set to '1'). Default Value: 0
10	EZ_MODE	Non EZ mode ('0') or EZ mode ('1'). In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported and the transmitter should use continuous data frames; i.e. data frames not separated by slave deselection. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field should be '0'. Default Value: 0

9	EC_OP_MODE	This field specifies the clocking for the SCB block '0': Internally clocked mode '1': externally clocked mode In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate). In UART mode this field should be '0'. Default Value: 0
8	EC_AM_MODE	This field specifies the clocking for the address matching (I2C) or slave selection detection logic (SPI) '0': Internally clocked mode '1': Externally clocked mode In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. The clocking for the rest of the logic is determined by CTRL.EC_OP_MODE. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. In UART mode this field should be '0'. Default Value: 0

3 : 0	OVS	Serial interface bit period oversampling factor expressed in SCB clock cycles. Used for SPI and UART functionality. OVS + 1 SCB clock cycles constitute a single serial interface clock/bit cycle. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the low and high phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the low and high phase can differ by 1 SCB clock period. In SPI master mode, the valid range is [3, 15]. At an SCB frequency of 48 MHz, the maximum SPI bit rate is 12 Mbps, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. The effective system bit rate is dependent on the external SPI slave that we communicate with. If the SPI output clock to SPI MISO input round trip delay is significant (multiple SPI output clock cycles), it may be necessary to increase OVS and/or to set SPI_CTRL.LATE_MISO_SAMPLE to '1' to achieve the maximum possible system bit rate. In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the SPI input clock (IF) on the interface to guarantee functional correct behavior. This requirement is expressed as a ratio: SCB clock/IF clock. The ratio is dependent on the setting of RX_CTRL.MEDIAN and the external SPI master's capability to support "late MISO sample" functionality (similar to our SPI master functionality represented by SPI_CTRL.LATE_MISO_SAMPLE): - MEDIAN is '0' and external SPI master has NO "late MISO sample functionality": SCB clock/IF clock >= 6. At a SCB frequency of 48 MHz, the maximum bit rate is 8 Mbps. - MEDIAN is '0' and external SPI master has "late MISO sample functionality": SCB clock/IF clock >= 3. At a SCB frequency of 48 MHz, the maximum bit rate is 16 Mbps.

		- MEDIAN is '1' and external SPI master has NO "late MISO sample functionality": SCB clock/IF clock >= 8. At a SCB frequency of 48 MHz, the maximum bit rate is 6 Mbps. - MEDIAN is '1' and external SPI master has "late MISO sample functionality": SCB clock/IF clock >= 4. At a SCB frequency of 48 MHz, the maximum bit rate is 12 Mbps. As discussed earlier, the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. In UART standard submode, the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15]. In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value: - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. SCB clock frequency of 16*57.6 KHz for 57.6 Kbps. SCB clock frequency of 16*38.4 KHz for 38.4 Kbps. SCB clock frequency of 16*19.2 KHz for 19.2 Kbps. SCB clock frequency of 16*9.6 KHz for 9.6 Kbps. SCB clock frequency of 16*2.4 KHz for 2.4 Kbps. SCB clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 Kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two SCB clock cycles are guaranteed to be detected by

		the receiver. Pulse widths less than two SCB clock cycles and greater or equal than one SCB clock cycle may be detected by the receiver. Pulse widths less than one SCB clock cycle will not be detected by the receiver. RX_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The SCB clock (as provided by the programmable clock block) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. SCB clock frequency of 16*57.6 KHz for 57.6 Kbps. SCB clock frequency of 16*38.4 KHz for 38.4 Kbps. SCB clock frequency of 16*19.2 KHz for 19.2 Kbps. SCB clock frequency of 16*9.6 KHz for 9.6 Kbps. SCB clock frequency of 16*2.4 KHz for 2.4 Kbps. SCB clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. Low power mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. - 1: 32 times oversampling. SCB clock frequency of 32*57.6 KHz for 57.6 Kbps. - 2: 48 times oversampling. SCB clock frequency of 48*38.4 KHz for 38.4 Kbps. - 3: 96 times oversampling. SCB clock frequency of 96*19.2 KHz for 19.2 Kbps. - 4: 192 times oversampling. SCB clock frequency of 192*9.6 KHz for 9.6 Kbps. - 5: 768 times oversampling. SCB clock frequency of 768*2.4 KHz for 2.4 Kbps. - 6: 1536 times oversampling. SCB clock frequency of 1536*1.2 KHz for 1.2 Kbps. - all other values are not used in low power mode. Default Value: 15

SCB0_STATUS

Generic status
Address: 0x40600004
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							EC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	EC_BUSY	Indicates whether the externally clocked logic is potentially accessing the EZ memory (this is only possible in EZ mode). This bit can be used by SW to determine whether it is safe to issue a SW access to the EZ memory (without bus wait states (a blocked SW access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether a SW access was actually blocked by externally clocked logic. Default Value: Undefined

SCB0_CMD_RESP_CTRL

Command/response control
Address: 0x40600008
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BASE_RD_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	BASE_WR_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_WR_ADDR	I2C/SPI write base address for CMD_RESP mode. At the start of a write transfer this BASE_WR_ADDR is copied to CMD_RESP_STATUS.CURR_WR_ADDR. This field should not be modified during ongoing bus transfers. Default Value: 0
7 : 0	BASE_RD_ADDR	I2C/SPI read base address for CMD_RESP mode. At the start of a read transfer this BASE_RD_ADDR is copied to CMD_RESP_STATUS.CURR_RD_ADDR. This field should not be modified during ongoing bus transfers. Default Value: 0

SCB0_CMD_RESP_STATUS

Command/response status
Address: 0x4060000C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CURR_RD_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	CURR_WR_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	CMD_RESP_EC_BUSY	CMD_RESP_EC_BUS_BUSY	None [29:24]					

Bits	Name	Description

31	CMD_RESP_EC_BUSY	Indicates whether the CURR_RD_ADDR and CURR_WR_ADDR fields in this register are reliable (when CMD_RESP_EC_BUSY is '0') or not reliable (when CMD_RESP_EC_BUSY is '1'). Note: - When there is no ongoing bus transfer, CMD_RESP_EC_BUSY is '0' (reliable). - When there is a ongoing bus transfer, CMD_RESP_EC_BUSY is '0' (reliable), when the CURR_RD_ADDR and CURR_WR_ADDR are not being updated by the HW. - When there is a ongoing bus transfer, CMD_RESP_EC_BUSY is '1' (not reliable), when the CURR_RD_ADDR or CURR_WR_ADDR are being updated by the HW. Note that this update lasts one I2C clock cycle, or two SPI clock cycles. Default Value: Undefined
30	CMD_RESP_EC_BUS_BUSY	Indicates whether there is an ongoing bus transfer to the IP. '0': no ongoing bus transfer. '1': ongoing bus transfer. For SPI, the field is '1' when slave mode is selected. For I2C, the field is set to '1' at a I2C START/RESTART. In case of an address match, the field is set to '0' on a I2C STOP. In case of NO address match, the field is set to '0' after the failing address match. Default Value: Undefined
23 : 16	CURR_WR_ADDR	I2C/SPI write current address for CMD_RESP mode. HW increments the field after a write access to the memory buffer. However, when the last memory buffer address is reached, the address is NOT incremented (but remains at the maximum memory buffer address). The field is used to determine how many bytes have been written (# bytes = CURR_WR_ADDR - CMD_RESP_CTRL.BASE_WR_ADDR) . This field is reliable when there is no bus transfer. This field is potentially unreliable when there is a ongoing bus transfer, i.e. when CMD_RESP_EC_BUSY is '0', the field is reliable. Default Value: Undefined

7 : 0	CURR_RD_ADDR	I2C/SPI read current address for CMD_RESP mode. HW increments the field after a read access to the memory buffer. However, when the last memory buffer address is reached, the address is NOT incremented (but remains at the maximum memory buffer address). The field is used to determine how many bytes have been read (# bytes = CURR_RD_ADDR - CMD_RESP_CTRL.BASE_RD_ADDR). This field is reliable when there is no bus transfer. This field is potentially unreliable when there is a ongoing bus transfer, i.e. when CMD_RESP_EC_BUSY is '0', the field is reliable. Default Value: Undefined

SCB0_SPI_CTRL

SPI control
Address: 0x40600020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		SCLK_CONTINUOUS	LATE_MISO_SAMPLE	CPOL	CPHA	SELECT_PRECEDE	SSEL_CONTINUOUS

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW	RW	RW	RW	RW	RW	RW
HW Access	None	R	R	R	R	R	R	R
Name	None	SSEL_INTER_FRAME_DEL	SSEL_HOLD_DEL	SSEL_SETUP_DEL	SSEL_POLARITY3	SSEL_POLARITY2	SSEL_POLARITY1	SSEL_POLARITY0

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None			RW		RW	
HW Access	R	None			R		R	
Name	MASTER_MODE	None [30:28]			SSEL [27:26]		MODE [25:24]	

Bits	Name	Description
31	MASTER_MODE	Master ('1') or slave ('0') mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all '1's. In both master and slave modes, received data frames will be lost if the RX FIFO is full. Default Value: 0
27 : 26	SSEL	Selects one of the four incoming/ outgoing SPI slave select signals: - 0: Slave 0, SSEL[0]. - 1: Slave 1, SSEL[1]. - 2: Slave 2, SSEL[2]. - 3: Slave 3, SSEL[3]. Default Value: 0
25 : 24	MODE	Submode of SPI operation (3: Reserved). Default Value: 3

		0x0: SPI_MOTOROLA : SPI Motorola submode. In master mode, when not transmitting data (Slave SELECT is inactive), SCLK is stable at CPOL. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive.
		0x1: SPI_TI : SPI Texas Instruments submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive; i.e. no pulse is generated.
		0x2: SPI_NS : SPI National Semiconductors submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only used in master mode. Not used in National Semiconductors submode. '0': No local loopback '1': the SPI master MISO line is connected to the SPI master MOSI line. In other words, in loopback mode the SPI master receives on MISO what it transmits on MOSI. Default Value: 0
14	SSEL_INTER_FRAME_DEL	Indicates the SPI SELECT inter-dataframe delay (between SELECT deactivation and SELECT activation). '0': 1.5 SPI clock cycles '1': 2.5 SPI clock cycles Only applies in SPI MOTOROLA submode and when SPI_CTRL.SSEL_CONTINUOUS=0, CTRL.OVS>=3. above are ideal case at SCB block level, and there is inaccuracy of one clk_scb cycle. Default Value: 0

13	SSEL_HOLD_DEL	Indicates the SPI SELECT hold delay (between SPI clock edge to sample the last MOSI bit, and SELECT deactivation). '0': 0.75 SPI clock cycles '1': 1.75 SPI clock cycles Only applies in SPI MOTOROLA submode and when SCLK_CONTINUOUS=0, CTRL.OVS>=3. above are ideal case at SCB block level, and there is inaccuracy of one clk_scb cycle. Default Value: 0
12	SSEL_SETUP_DEL	Indicates the SPI SELECT setup delay (between SELECT activation and SCLK clock edge to sample the first MOSI bit). '0': 0.75 SPI clock cycles '1': 1.75 SPI clock cycles Only applies in SPI MOTOROLA submode and when SCLK_CONTINUOUS=0, CTRL.OVS>=3. above are ideal case at SCB block level, and there is inaccuracy of one clk_scb cycle. Default Value: 0
11	SSEL_POLARITY3	Slave select polarity. Default Value: 0
10	SSEL_POLARITY2	Slave select polarity. Default Value: 0
9	SSEL_POLARITY1	Slave select polarity. Default Value: 0
8	SSEL_POLARITY0	Slave select polarity. SSEL_POLARITY0 applies to the outgoing SPI slave select signal 0 (master mode) and to the incoming SPI slave select signal (slave mode). For Motorola and National Semiconductors submodes: '0': slave select is low/'0' active. '1': slave select is high/'1' active. For Texas Instruments submode: '0': high/'1' active precede/coincide pulse. '1': low/'0' active precede/ coincide pulse. Default Value: 0
5	SCLK_CONTINUOUS	Only applicable in master mode. '0': SCLK is generated, when the SPI master is enabled and data is transmitted. '1': SCLK is generated, when the SPI master is enabled. This mode is useful for slave devices that use SCLK for functional operation other than just SPI functionality. Default Value: 0

4	LATE_MISO_SAMPLE	Changes the SCLK edge on which MISO is captured. Only used in master mode. When '0', the default applies (for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK and for National Semiconductors on the rising edge of SCLK). When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master. Default Value: 1
3	CPOL	Indicates the clock polarity. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured: - CPOL is '0': SCLK is '0' when not transmitting data. - CPOL is '1': SCLK is '1' when not transmitting data. Default Value: 0
2	CPHA	Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured: - Motorola mode 0. CPOL is '0', CPHA is '0': MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. - Motorola mode 1. CPOL is '0', CPHA is '1': MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 2. CPOL is '1', CPHA is '0': MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 3. CPOL is '1', CPHA is '1': MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. In SPI Motorola submode, all four CPOL/CPHA modes are valid. in SPI NS submode, only CPOL=0 CPHA=0 mode is valid. in SPI TI submode, only CPOL=0 CPHA=1 mode is valid. Default Value: 0

1	SELECT_PRECEDE	Only used in SPI Texas Instruments' submode. When '1', the data frame start indication is a pulse on the Slave SELECT line that precedes the transfer of the first data frame bit. When '0', the data frame start indication is a pulse on the Slave SELECT line that coincides with the transfer of the first data frame bit. Default Value: 0
0	SSEL_CONTINUOUS	Continuous SPI data transfers enabled ('1') or not ('0'). This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported independent of this field. When continuous transfers are enabled individual data frame transfers are not necessarily separated by slave deselection (as indicated by the level or pulse on the SELECT line): if the TX FIFO has multiple data frames, data frames are send out without slave deselection. When continuous transfers are not enabled individual data frame transfers are always separated by slave deselection: independent of the availability of TX FIFO data frames, data frames are sent out with slave deselection. Default Value: 0

SCB0_SPI_STATUS

SPI status
Address: 0x40600024
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						SPI_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	SPI base EZ address. Address as provided by a SPI write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	SPI current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when SPI_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined

1	SPI_EC_BUSY	Indicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. Default Value: Undefined

SCB0_SPI_TX_CTRL

SPI transmitter control
Address: 0x40600028
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None			
HW Access	None		R	R	None			
Name	None [7:6]		PARITY_ENABLED	PARITY	None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	PARITY_ENABLED	Parity generation enabled ('1') or not ('0'). Default Value: 0
4	PARITY	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Default Value: 0

SCB0_SPI_RX_CTRL

SPI receiver control
Address: 0x4060002C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None			
HW Access	None		R	R	None			
Name	None [7:6]		PARITY_ENABLED	PARITY	None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							DROP_ON_PARITY_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	DROP_ON_PARITY_ERROR	Behavior when a parity check fails. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Default Value: 0
5	PARITY_ENABLED	Parity checking enabled ('1') or not ('0'). Default Value: 0
4	PARITY	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Default Value: 0

SCB0_UART_CTRL

UART control
Address: 0x40600040
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						MODE [25:24]	

Bits	Name	Description
25 : 24	MODE	Submode of UART operation (3: Reserved) Default Value: 3
		0x0: UART_STD : Standard UART submode.
		0x1: UART_SMARTCARD : SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side.
		0x2: UART_IRDA : Infrared Data Association (IrDA) submode. Return to Zero modulation scheme. In this mode, the oversampling factor should be 16, that is OVS should be set to 15.

16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). 0: Loopback is not enabled 1: UART_TX is connected to UART_RX. UART_RTS is connected to UART_CTS. This allows a SCB UART transmitter to communicate with its receiver counterpart. Default Value: 0

SCB0_UART_TX_CTRL

UART transmitter control
Address: 0x40600044
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None	RW		
HW Access	None		R	R	None	R		
Name	None [7:6]		PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RETRY_ON_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	RETRY_ON_NACK	When '1', a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode. Default Value: 0
5	PARITY_ENABLED	Parity generation enabled ('1') or not ('0'). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware Default Value: 0
4	PARITY	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0

2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Default Value: 2

SCB0_UART_RX_CTRL

UART receiver control
Address: 0x40600048
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW		
HW Access	None	R	R	R	None	R		
Name	None	POLARITY	PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	None	RW	RW	RW
HW Access	None		R	R	None	R	R	R
Name	None [15:14]		SKIP_START	Reserved	None	MP_MODE	DROP_ON_FRAME_ERROR	DROP_ON_PARITY_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				BREAK_WIDTH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							BREAK_LEVEL

Bits	Name	Description
24	BREAK_LEVEL	0: low level pulse detection 1: high level pulse detection, like idle line state in UART Default Value: 0

19 : 16	BREAK_WIDTH	Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is '0'. This feature is useful for standard UART submode ("break field" detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to '1'. Note that break detection precedes baud rate detection, which is used to synchronize/ refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receiver's definition of a bit period is imprecise and the setting of this field should take this imprecision into account. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of 10+1 = 11 bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value. Default Value: 10

13	SKIP_START	Only applicable in standard UART submode. When '1', the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a '1'. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle ('1') to START ('0') on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO2 IP. The woken up CPU will enable the SCB's UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will synchronize to a '0' to '1' transition, which indicates the first data frame bit is received (first data frame bit should be '1'). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit. Default Value: 0
12	Reserved	Default Value: 0
10	MP_MODE	Multi-processor mode. When '1', multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH should indicate a 9-bit data frame. In multi-processor mode, the 9th received bit of a data frame separates addresses (bit is '1') from data (bit is '0'). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data are sent to the RX FIFO. In the case of NO match, subsequent received data are dropped. Default Value: 0
9	DROP_ON_FRAME_ERROR	Behavior when an error is detected in a start or stop period. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost. Default Value: 0

8	DROP_ON_PARITY_ERROR	Behavior when a parity check fails. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost. Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field). Default Value: 0
6	POLARITY	Inverts incoming RX line signal. Inversion is after local loopback. This functionality is intended for IrDA receiver functionality. Default Value: 0
5	PARITY_ENABLED	Parity checking enabled ('1') or not ('0'). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware. Default Value: 0
4	PARITY	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0
2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of half bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle time between data frames and the data frame value. Default Value: 2

SCB0_UART_RX_STATUS

UART receiver status
Address: 0x4060004C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	BR_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				BR_COUNTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	BR_COUNTER	Amount of SCB clock periods that constitute the transmission of a 0x55 data frame (sent least significant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of SCB clock periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DETECT is set to '1'. Default Value: Undefined

SCB0_UART_FLOW_CTRL

UART flow control
Address: 0x40600050
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TRIGGER_LEVEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							RTS_POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						CTS_ENABLED	CTS_POLARITY

Bits	Name	Description
25	CTS_ENABLED	Enable use of CTS input signal by the UART transmitter: '0': Disabled. The UART transmitter ignores the CTS input signal and transmits when a data frame is available for transmission in the TX FIFO or the TX shift register. '1': Enabled. The UART transmitter uses CTS input signal to qualify the transmission of data. It transmits when CTS input signal is active and a data frame is available for transmission in the TX FIFO or the TX shift register. If UART_CTRL.LOOPBACK is '1', the CTS input signal is driven by the RTS output signal locally in SCB (both signals are subjected to signal polarity changes are indicated by RTS_POLARITY and CTS_POLARITY). Default Value: 0

24	CTS_POLARITY	Polarity of the CTS input signal '0': CTS is active low ; '1': CTS is active high; Default Value: 0
16	RTS_POLARITY	Polarity of the RTS output signal: '0': RTS is active low; '1': RTS is active high; During SCB reset (Hibernate system power mode), RTS output signal is '1'. This represents an inactive state assuming an active low polarity. Default Value: 0
6 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has less entries than the amount of this field, a Ready To Send (RTS) output signal is activated. By setting this field to "0", flow control is effectively disabled (may be useful for debug purposes). Default Value: 0

SCB0_I2C_CTRL

I2C control
Address: 0x40600060
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LOW_PHASE_OVS [7:4]				HIGH_PHASE_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	None	RW	RW
HW Access	R	R	R	R	R	None	R	R
Name	S_NOT_READY_DATA_NACK	S_NOT_READY_ADDR_NACK	S_READY_DATA_ACK	S_READY_ADDR_ACK	S_GENERAL_IGNORE	None	M_NOT_READY_DATA_NACK	M_READY_DATA_ACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	MASTER_MODE	SLAVE_MODE	None [29:24]					

Bits	Name	Description
31	MASTER_MODE	Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the IP to address itself. Default Value: 0
30	SLAVE_MODE	Slave mode enabled ('1') or not ('0'). Default Value: 0
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode. When '0', no loopback When '1', loopback is enabled internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself. Default Value: 0

15	S_NOT_READY_DATA_NACK	Only used when: - non EZ mode Functionality is as follows: - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). Default Value: 1
14	S_NOT_READY_ADDR_NACK	This field is used during an address match or general call address in internally clocked mode Only used when: - EC_AM_MODE is '0', EC_OP_MODE is '0', S_GENERAL_IGNORE is '0] and non EZ mode. Functionality is as follows: - 1: a received (matching) slave address is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). For externally clocked logic (EC_AM is '1') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when (NOT used when EC_AM is '1' and EC_OP is '1' and address match and EZ mode): - EC_AM is '1' and EC_OP is '0'. - EC_AM is '1' and general call address match. - EC_AM is '1' and non EZ mode. Functionality is as follows: - 1: a received (matching or general) slave address is always immediately NACK'd. There are two possibilities: 1). the SCB clock is available (in Active system power mode) and it handles the rest of the current transfer. In this case the I2C master will not observe the NACK. 2).SCB clock is not present (in DeepSleep system power mode). In this case the I2C master will observe the NACK and may retry the transfer in the future (which gives the internally clocked logic the time to wake up from DeepSleep system power mode). - 0: clock stretching is performed (till the SCB clock is available). The logic will handle the ongoing transfer as soon as the clock is enabled. Default Value: 1

13	S_READY_DATA_ACK	When '1', a received data element by the slave is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
12	S_READY_ADDR_ACK	When '1', a received (matching) slave address is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
11	S_GENERAL_IGNORE	When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure. Default Value: 1
9	M_NOT_READY_DATA_NACK	When '1', a received data element byte the master is immediately NACK'd when the receiver FIFO is full. When '0', clock stretching is used instead (till the receiver FIFO is no longer full). Default Value: 1
8	M_READY_DATA_ACK	When '1', a received data element by the master is immediately ACK'd when the receiver FIFO is not full. Default Value: 1
7 : 4	LOW_PHASE_OVS	Serial I2C interface low phase oversampling factor. LOW_PHASE_OVS + 1 SCB clock periods constitute the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular (no stretching) interface (IF) low time to guarantee functionally correct behavior. With input signal median filtering, the IF low time should be >= 8 SCB clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF low time should be >= 7 SCB clock cycles and <= 16 SCB clock cycles. in slave mode, this field is used to define number of clk_scb cycles for tSU-DAT timing (from ACK/NACK/data ready, to SCL rising edge (released from I2C slave clock stretching)) Default Value: 8

3 : 0	HIGH_PHASE_OVS	Serial I2C interface high phase oversampling factor. HIGH_PHASE_OVS + 1 SCB clock periods constitute the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular interface (IF) high time to guarantee functional correct behavior. With input signal median filtering, the IF high time should be >= 6 SCB clock cycles and <= 16 SCB clock cycles. Without input signal median filtering, the IF high time should be >= 5 SCB clock cycles and <= 16 SCB clock cycles. Default Value: 8

SCB0_I2C_STATUS

I2C status
Address: 0x40600064
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None	R	R	R
HW Access	None		W	W	None	W	W	W
Name	None [7:6]		M_READ	S_READ	None	I2CS_IC_BUSY	I2C_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined

5	M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0''. Default Value: 0
4	S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0''. Default Value: 0
2	I2CS_IC_BUSY	Indicates whether the internally clocked slave logic is being accessed by external I2C master. --set at ADDR_MATCH --clear at START/RESET, STOP detection, or BUS_ERROR This bit can be used by SW to determine whether I2CS_IC is busy before entering DeepSleep. Default Value: 0
1	I2C_EC_BUSY	Indicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_EZ_ADDR or CURR_EZ_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_EZ_ADDR and CURR_EZ_ADDR are reliable. Default Value: Undefined

0	BUS_BUSY	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If SCB block is disabled, BUS_BUSY is '0'. After enabling the block, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0

SCB0_I2C_M_CMD

I2C master command
Address: 0x40600068
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:5]			M_STOP	M_NACK	M_ACK	M_START_ON_IDLE	M_START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	M_STOP	When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. I2C_M_CMD.M_START has a higher priority than this command: in situations where both a STOP and a REPEATED START could be transmitted, M_START takes precedence over M_STOP. Default Value: 0
3	M_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
2	M_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0

1	M_START_ON_IDLE	When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0') . A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'. Default Value: 0
0	M_START	When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'. Default Value: 0

SCB0_I2C_S_CMD

I2C slave command
Address: 0x4060006C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1C	RW1C
Name	None [7:2]						S_NACK	S_ACK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	S_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK. Default Value: 0
0	S_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). Default Value: 0

SCB0_I2C_CFG

I2C configuration
Address: 0x40600070
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [7:5]			SDA_IN_FILT_SEL	None [3:2]		SDA_IN_FILT_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [15:13]			SCL_IN_FILT_SEL	None [11:10]		SCL_IN_FILT_TRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		SDA_OUT_FILT2_TRIM [21:20]		SDA_OUT_FILT1_TRIM [19:18]		SDA_OUT_FILT0_TRIM [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None			
HW Access	None		R		None			
Name	None [31:30]		SDA_OUT_FILT_SEL [29:28]		None [27:24]			

Bits	Name	Description
29 : 28	SDA_OUT_FILT_SEL	Selection of cumulative filter delay on SDA output to meet tHD_DAT parameter "0": 0 ns. "1": 50 ns (filter 0 enabled). "2": 100 ns (filters 0 and 1 enabled). "3": 150 ns (filters 0, 1 and 2 enabled). Default Value: 0
21 : 20	SDA_OUT_FILT2_TRIM	Trim settings for the 50ns delay filter on SDA output used to guarantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2
19 : 18	SDA_OUT_FILT1_TRIM	Trim settings for the 50ns delay filter on SDA output used to guarantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2

17 : 16	SDA_OUT_FILT0_TRIM	Trim settings for the 50ns delay filter on SDA output used to guarantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2
12	SCL_IN_FILT_SEL	Enable for 50ns glitch filter on SCL input '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
9 : 8	SCL_IN_FILT_TRIM	Trim settings for the 50ns glitch filter on the SDA input. Default setting meets the I2C glitch rejections specs. Programmability available if required Default Value: 0
4	SDA_IN_FILT_SEL	Enable for 50ns glitch filter on SDA input '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
1 : 0	SDA_IN_FILT_TRIM	Trim settings for the 50ns glitch filter on the SDA input. Default setting meets the I2C glitch rejections specs. Programmability available if required Default Value: 3

SCB0_TX_CTRL

Transmitter control
Address: 0x40600200
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			DATA_WIDTH [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							MSB_FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							OPEN_DRAIN

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

16	OPEN_DRAIN	Each IO cell "xxx" has two associated IP output signals "xxx_out_en" and "xxx_out". '0': Normal operation mode. Typically, this operation mode is used for IO cells that are connected to (board) wires/lines that are driven by a single IO cell. In this operation mode, for an IO cell "xxx" that is used as an output, the "xxx_out_en" output enable signal is typically constant '1' the "xxx_out" output is the outputted value. In other words, in normal operation mode, the "xxx_out" output is used to control the IO cell output value: "xxx_out" is '0' to drive an IO cell output value of '0' and "xxx_out" is '1' to drive an IO cell output value of '1'. '1': Open drain operation mode. Typically this operation mode is used for IO cells that are connected to (board) wires/lines that are driven by multiple IO cells (possibly on multiple chips). In this operation mode, for and IO cell "xxx" that is used as an output, the "xxx_out_en" output controls the outputted value. Typically, open drain operation mode drives low/'0' and the "xxx_out" output is constant '1'. In other words, in open drain operation mode, the "xxx_out_en" output is used to control the IO cell output value: in drive low/'0' mode: "xxx_out_en" is '1' (drive enabled) to drive an IO cell output value of '0' and "xxx_out_en" is '1' (drive disabled) to not drive an IO cell output value (another IO cell can drive the wire/line or a pull up results in a wire/line value '1'). The open drain mode is supported for: - UART mode, "uart_tx" IO cell. - SPI mode, "spi_miso" IO cell. not applicable to I2C mode, "i2c_scl" and "i2c_sda" IO cells. (I2C SCL/SDA always work in open-drain mode) Default Value: 0
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1

4 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 31]. For I2C the only valid value is 7. Default Value: 7

SCB0_TX_FIFO_CTRL

Transmitter FIFO control
Address: 0x40600204
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TRIGGER_LEVEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. Default Value: 0
16	CLEAR	When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
6 : 0	TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries than the number of this field, a transmitter trigger event INTR_TX.TRIGGER is generated. Default Value: 0

SCB0_TX_FIFO_STATUS

Transmitter FIFO status
Address: 0x40600208
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	USED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None	R						
HW Access	None	W						
Name	None	RD_PTR [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None	R						
HW Access	None	W						
Name	None	WR_PTR [30:24]						

Bits	Name	Description
30 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written. Default Value: 0
22 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read by the hardware. Default Value: 0
15	SR_VALID	Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is transmitted next (when the protocol state machine is not transmitting a data frame). Default Value: 0

7 : 0	USED	Amount of entries in the transmitter FIFO. The value of this field ranges from 0 to FF_DATA_NR (EZ_DATA_NR/2). Default Value: 0

SCB0_TX_FIFO_WR

Transmitter FIFO write
Address: 0x40600240
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Note that when CTRL.MEM_WIDTH is "0", only DATA[7:0] are used and when CTRL.MEM_WIDTH is "1", only DATA[15:0] are used. A write to a full TX FIFO sets INTR_TX.OVERFLOW to '1'. Default Value: 0

SCB0_RX_CTRL

Receiver control
Address: 0x40600300
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			DATA_WIDTH [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						MEDIAN	MSB_FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	MEDIAN	Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptibility to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'. Default Value: 0
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
4 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 31]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

SCB0_RX_FIFO_CTRL

Receiver FIFO control
Address: 0x40600304
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TRIGGER_LEVEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer. Default Value: 0
16	CLEAR	When '1', the receiver FIFO and receiver shift register are cleared/ invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
6 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has more entries than the number of this field, a receiver trigger event INTR_RX.TRIGGER is generated. Default Value: 0

SCB0_RX_FIFO_STATUS

Receiver FIFO status
Address: 0x40600308
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	USED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None	R						
HW Access	None	W						
Name	None	RD_PTR [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None	R						
HW Access	None	W						
Name	None	WR_PTR [30:24]						

Bits	Name	Description
30 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written by the hardware. Default Value: 0
22 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read. Default Value: 0
15	SR_VALID	Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). Default Value: 0
7 : 0	USED	Amount of entries in the receiver FIFO. The value of this field ranges from 0 to FF_DATA_NR (EZ_DATA_NR/2). Default Value: 0

SCB0_RX_MATCH

Slave address and mask
Address: 0x40600310
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	MASK	Slave device address mask. This field is a mask that specifies which of the slave address bits take part in the matching. MATCH = ((ADDR & MASK) == ("slave address" & MASK)). Default Value: 0
7 : 0	ADDR	Slave device address. In UART multi-processor mode, all 8 bits are used. In I2C slave mode, only bits 7 down to 1 are used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the last 1 bit is a read/write indicator ('0': write, '1': read). Default Value: 0

SCB0_RX_FIFO_RD

Receiver FIFO read
Address: 0x40600340
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. Note that when CTRL.MEM_WIDTH is "0", only DATA[7:0] are used and when CTRL.MEM_WIDTH is "1", only DATA[15:0] are used A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. When this register is read through the debugger, the data frame will not be removed from the FIFO. Similar in operation to RX_FIFO_RD_SILENT Default Value: Undefined

SCB0_RX_FIFO_RD_SILENT

Receiver FIFO read silent
Address: 0x40600344
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Note that when CTRL.MEM_WIDTH is "0", only DATA[7:0] are used and when CTRL.MEM_WIDTH is "1", only DATA[15:0] are used A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

SCB0_EZ_DATA0

Memory buffer
Address: 0x40600400
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

SCB0_INTR_CAUSE

Active clocked interrupt signal
Address: 0x40600E00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		SPI_EC	I2C_EC	RX	TX	S	M

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	SPI_EC	Externally clocked SPI interrupt active ("interrupt_spi_ec"): INTR_SPI_EC_MASKED != 0. Default Value: 0
4	I2C_EC	Externally clock I2C interrupt active ("interrupt_i2c_ec"): INTR_I2C_EC_MASKED != 0. Default Value: 0
3	RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0

0	M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

SCB0_INTR_I2C_EC

Externally clocked I2C interrupt request
Address: 0x40600E80
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (I2C STOP). This event is an indication that a buffer memory location has been read from. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (I2C STOP). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0

1	EZ_STOP	STOP detection. Activated on the end of a every transfer (I2C STOP). Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0
0	WAKE_UP	Wake up request. Active on incoming slave request (with address match). Only used when CTRL.EC_AM_MODE is '1'. Default Value: 0

SCB0_INTR_I2C_EC_MASK

Externally clocked I2C interrupt mask
Address: 0x40600E88
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

SCB0_INTR_I2C_EC_MASKED

Externally clocked I2C interrupt masked
Address: 0x40600E8C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

SCB0_INTR_SPI_EC

Externally clocked SPI interrupt request
Address: 0x40600EC0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (SPI deselection). This event is an indication that a buffer memory location has been read from. Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (SPI deselection). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'. Default Value: 0

1	EZ_STOP	STOP detection. Activated on the end of a every transfer (SPI deselection). Only available in EZ and CMD_RESP mode and when CTRL.EC_OP_MODE is '1'. Default Value: 0
0	WAKE_UP	Wake up request. Active on incoming slave request when externally clocked selection is '1'. Only used when CTRL.EC_AM_MODE is '1'. Default Value: 0

SCB0_INTR_SPI_EC_MASK

Externally clocked SPI interrupt mask
Address: 0x40600EC8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

SCB0_INTR_SPI_EC_MASKED

Externally clocked SPI interrupt masked
Address: 0x40600ECC
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

SCB0_INTR_M

Master interrupt request
Address: 0x40600F00
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None	RW1C	RW1C	RW1C
HW Access	None			RW1S	None	RW1S	RW1S	RW1S
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	SPI master transfer done event: all data frames in the transmit FIFO are sent, the transmit FIFO is empty (both TX FIFO and transmit shifter register are empty), and SPI select output pin is deselected. Default Value: 0
8	I2C_BUS_ERROR	I2C master bus error (unexpected detection of START or STOP condition). Default Value: 0
4	I2C_STOP	I2C master STOP. Set to '1', when the master has transmitted a STOP. Default Value: 0
2	I2C_ACK	I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data). Default Value: 0

1	I2C_NACK	I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data). Default Value: 0
0	I2C_ARB_LOST	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. Default Value: 0

SCB0_INTR_M_SET

Master interrupt set request
Address: 0x40600F04
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None	RW1S	RW1S	RW1S
HW Access	None			A	None	A	A	A
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

SCB0_INTR_M_MASK

Master interrupt mask
Address: 0x40600F08
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

SCB0_INTR_M_MASKED

Master interrupt masked request
Address: 0x40600F0C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None	R	R	R
HW Access	None			W	None	W	W	W
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	R
HW Access	None						W	W
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

SCB0_INTR_S

Slave interrupt request
Address: 0x40600F40
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	SPI slave deselected at an unexpected time in the SPI transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0
10	SPI_EZ_STOP	SPI slave deselected after any EZ SPI transfer occurred. Default Value: 0
9	SPI_EZ_WRITE_STOP	SPI slave deselected after a write EZ SPI transfer occurred. Default Value: 0

8	I2C_BUS_ERROR	I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behavior. In case of a bus error, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0
7	I2C_GENERAL	I2C slave general call address received. If CTRL.ADDR_ACCEPT, the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
6	I2C_ADDR_MATCH	I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
5	I2C_START	I2C slave START received. Set to '1', when START or REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. The Firmware should use INTR_S_EC.WAKE_UP, INTR_S.I2C_ADDR_MATCH and INTR_S.I2C_GENERAL. Default Value: 0

4	I2C_STOP	I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. The event is detected on any I2C transfer intended for this slave. Note that a I2C address intended for the slave (address is matching) will result in a I2C_STOP event independent of whether the I2C address is ACK'd or NACK'd. Default Value: 0
3	I2C_WRITE_STOP	I2C STOP event for I2C write transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. In non EZ mode, the event is detected on any I2C write transfer intended for this slave. Note that a I2C write address intended for the slave (address is matching and a it is a write transfer) will result in a I2C_WRITE_STOP event independent of whether the I2C address is ACK'd or NACK'd. In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an I2C address and EZ address, will not result in this event being detected). Default Value: 0

2	I2C_ACK	I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data). Default Value: 0
1	I2C_NACK	I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data). Default Value: 0
0	I2C_ARB_LOST	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behavior. In case of lost arbitration, the I2C slave state machine aborts the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

SCB0_INTR_S_SET

Slave interrupt set request
Address: 0x40600F44
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST
Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR
Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

5	I2C_START	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

SCB0_INTR_S_MASK

Slave interrupt mask
Address: 0x40600F48
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0

5	I2C_START	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

SCB0_INTR_S_MASKED

Slave interrupt masked request
Address: 0x40600F4C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST
Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR
Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
10	SPI_EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
9	SPI_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	I2C_GENERAL	Logical and of corresponding request and mask bits. Default Value: 0
6	I2C_ADDR_MATCH	Logical and of corresponding request and mask bits. Default Value: 0

5	I2C_START	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
3	I2C_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

SCB0_INTR_TX

Transmitter interrupt request
Address: 0x40600F80
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None		RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
Name	BLOCKED	UNDERFLOW	OVERFLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is useful when transmitter and receiver share a TX/RX line. This is the case in SmartCard modes. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
9	UART_DONE	UART transmitter done event. This happens when the IP is done transferring all data in the TX FIFO, and the last stop field is transmitted (both TX FIFO and transmit shifter register are empty). Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

8	UART_NACK	UART transmitter received a negative acknowledgement in SmartCard mode. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
7	BLOCKED	SW cannot get access to the EZ memory (EZ data access), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. (Note: This bit may be set unintentionally, even if the FIFO is not empty. Workaround: Ignore the bit when the clock frequency of the AHB bus is greater than 3x the internal frequency of SCB and the FIFO is not empty) Default Value: 0
5	OVERFLOW	Attempt to write to a full TX FIFO. Only used in FIFO mode. Default Value: 0
4	EMPTY	TX FIFO is empty; i.e. it has 0 entries. Only used in FIFO mode. Default Value: 0
1	NOT_FULL	TX FIFO is not full. Dependent on CTRL.MEM_WIDTH: (FF_DATA_NR = EZ_DATA_NR/2) MEM_WIDTH is "0": # entries != FF_DATA_NR. MEM_WIDTH is "1": # entries != FF_DATA_NR/2. MEM_WIDTH is "2": # entries != FF_DATA_NR/4. Only used in FIFO mode. Default Value: 0
0	TRIGGER	Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL.TRIGGER_LEVEL. Only used in FIFO mode. Default Value: 0

SCB0_INTR_TX_SET

Transmitter interrupt set request
Address: 0x40600F84
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
HW Access	A	A	A	A	None		A	A
Name	BLOCKED	UNDERFLOW	OVERFLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

4	EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

SCB0_INTR_TX_MASK

Transmitter interrupt mask
Address: 0x40600F88
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None		RW	RW
HW Access	R	R	R	R	None		R	R
Name	BLOCKED	UNDERFLOW	OVERFLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0

4	EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

SCB0_INTR_TX_MASKED

Transmitter interrupt masked request
Address: 0x40600F8C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None		R	R
HW Access	W	W	W	W	None		W	W
Name	BLOCKED	UNDERFLOW	OVERFLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0
9	UART_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	UART_NACK	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0

4	EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
1	NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

SCB0_INTR_RX

Receiver interrupt request
Address: 0x40600FC0
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	None	RW1C	RW1C	None	RW1C
HW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
Name	BLOCKED	UNDERFLOW	OVERFLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Break detection is successful: the line is '0' for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. "break-in-data" is supported. This feature is supported for the UART standard. For the UART standard submodes, ongoing receipt of data frames is NOT affected; i.e. Firmware is expected to take the proper action. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

10	BAUD_DETECT	The baudrate detection is completed. The receiver software uses the UART_RX_STATUS.BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first data frame (Protected Identifier Field) after the synchronization byte. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
9	PARITY_ERROR	Parity error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO. Default Value: 0

8	FRAME_ERROR	Frame error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. This can be either a start or stop bit(s) error: Start bit error: after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1'). Note: a start bit error is detected BEFORE a data frame is received. Stop bit error: the RX line is sampled as '0', but a '1' was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received. A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '1', the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '0', the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames. Default Value: 0
7	BLOCKED	SW cannot get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty RX FIFO. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in FIFO mode. Default Value: 0

3	FULL	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on CTRL.MEM_WIDTH: (FF_DATA_NR = EZ_DATA_NR/2) MEM_WIDTH is "0": # entries == FF_DATA_NR. MEM_WIDTH is "1": # entries == FF_DATA_NR/2. MEM_WIDTH is "2": # entries == FF_DATA_NR/4. Only used in FIFO mode. Default Value: 0
2	NOT_EMPTY	RX FIFO is not empty. Only used in FIFO mode. Default Value: 0
0	TRIGGER	More entries in the RX FIFO than the value specified by RX_FIFO_CTRL.TRIGGER_LEVEL. Only used in FIFO mode. Default Value: 0

SCB0_INTR_RX_SET

Receiver interrupt set request
Address: 0x40600FC4
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
HW Access	A	A	A	None	A	A	None	A
Name	BLOCKED	UNDERFLOW	OVERFLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
10	BAUD_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
9	PARITY_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
8	FRAME_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0

5	OVERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
3	FULL	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
2	NOT_EMPTY	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

SCB0_INTR_RX_MASK

Receiver interrupt mask
Address: 0x40600FC8
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None	RW	RW	None	RW
HW Access	R	R	R	None	R	R	None	R
Name	BLOCKED	UNDERFLOW	OVERFLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	BAUD_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	PARITY_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	FRAME_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0

5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

SCB0_INTR_RX_MASKED

Receiver interrupt masked request
Address: 0x40600FCC
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	None	R	R	None	R
HW Access	W	W	W	None	W	W	None	W
Name	BLOCKED	UNDERFLOW	OVERFLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
10	BAUD_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
9	PARITY_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
8	FRAME_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0

5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
3	FULL	Logical and of corresponding request and mask bits. Default Value: 0
2	NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

SCB1_CTRL

Generic control
Address: 0x40610000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None			RW	RW	RW
HW Access	R		None			R	R	R
Name	MEM_WIDTH [15:14]		None [13:11]			EZ_MODE	EC_OP_MODE	EC_AM_MODE

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						BLOCK	ADDR_ACCEPT

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None		RW	None		RW	
HW Access	R	None		R	None		R	
Name	ENABLED	None [30:29]		EC_ACCESS	None [27:26]		MODE [25:24]	

Bits	Name	Description

31	ENABLED	SCB block is enabled ('1') or not ('0'). The proper order in which to initialize SCB is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL registers. This includes selection of a submode, master/slave functionality and transmitter/ receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL register to enable SCB, select the specific operation mode and oversampling factor. Generally when this block is enabled, no control information should be changed. Changes should be made AFTER disabling this block, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the block is re-enabled. Note that disabling the block will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Specific to SPI master case, when SCB is idle, below registers can be changed without disabling SCB block, TX_CTRL TX_FIFO_CTRL RX_CTRL RX_FIFO_CTRL SPI_CTRL.SSEL, Default Value: 0
28	EC_ACCESS	EC_ACCESS is used to enable I2CS_EC or SPIS_EC access to internal EZ memory. 1: enable clk_scb 0: disable clk_scb Before going to deepsleep this field should be set to 1. when waking up from DeepSleep power mode, and PLL is locked (clk_scb is at expected frequency), this filed should be set to 0. Default Value: 0
25 : 24	MODE	Mode of operation (3: Reserved) Default Value: 3
		0x0: I2C : Inter-Integrated Circuits (I2C) mode.

		0x1: SPI : Serial Peripheral Interface (SPI) mode.
		0x2: UART : Universal Asynchronous Receiver/Transmitter (UART) mode.
17	BLOCK	Only used in externally clocked mode. If the externally clocked logic and the internal CPU accesses to EZ memory coincide/collide, this bit determines whether the CPU access should block and result in bus wait states ('BLOCK is 1') or not (BLOCK is '0'). IF BLOCK is '0' and the accesses collide, CPU read operations return 0xffff:ffff and CPU write operations are ignored. Colliding accesses are registered as interrupt causes: INTR_TX.BLOCKED and INTR_RX.BLOCKED. Default Value: 0
16	ADDR_ACCEPT	Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0'). In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when this bit is '1' for both I2C read and write transfers. In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. Default Value: 0
15 : 14	MEM_WIDTH	Determines the number of bits per FIFO data element. Default Value: 1
		0x0: BYTE : 8-bit FIFO data elements. This mode provides the biggest amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7].
		0x1: HALFWORD : 16-bit FIFO data elements. TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 15].
		0x2: WORD : 32-bit FIFO data elements. This mode provides the smallest amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH can be in a range of [0, 31].

		0x3: Reserved : This setting is reserved. Do not use.
10	EZ_MODE	Non EZ mode ('0') or EZ mode ('1'). In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported and the transmitter should use continuous data frames; i.e. data frames not separated by slave deselection. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field should be '0'. Default Value: 0
9	EC_OP_MODE	This field specifies the clocking for the SCB block '0': Internally clocked mode '1': externally clocked mode In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate). In UART mode this field should be '0'. Default Value: 0

8	EC_AM_MODE	This field specifies the clocking for the address matching (I2C) or slave selection detection logic (SPI) '0': Internally clocked mode '1': Externally clocked mode In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. The clocking for the rest of the logic is determined by CTRL.EC_OP_MODE. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. In UART mode this field should be '0'. Default Value: 0

3 : 0	OVS	Serial interface bit period oversampling factor expressed in SCB clock cycles. Used for SPI and UART functionality. OVS + 1 SCB clock cycles constitute a single serial interface clock/bit cycle. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the low and high phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the low and high phase can differ by 1 SCB clock period. In SPI master mode, the valid range is [3, 15]. At an SCB frequency of 48 MHz, the maximum SPI bit rate is 12 Mbps, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. The effective system bit rate is dependent on the external SPI slave that we communicate with. If the SPI output clock to SPI MISO input round trip delay is significant (multiple SPI output clock cycles), it may be necessary to increase OVS and/or to set SPI_CTRL.LATE_MISO_SAMPLE to '1' to achieve the maximum possible system bit rate. In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the SPI input clock (IF) on the interface to guarantee functional correct behavior. This requirement is expressed as a ratio: SCB clock/IF clock. The ratio is dependent on the setting of RX_CTRL.MEDIAN and the external SPI master's capability to support "late MISO sample" functionality (similar to our SPI master functionality represented by SPI_CTRL.LATE_MISO_SAMPLE): - MEDIAN is '0' and external SPI master has NO "late MISO sample functionality": SCB clock/IF clock >= 6. At a SCB frequency of 48 MHz, the maximum bit rate is 8 Mbps. - MEDIAN is '0' and external SPI master has "late MISO sample functionality": SCB clock/IF clock >= 3. At a SCB frequency of 48 MHz, the maximum bit rate is 16 Mbps.

		- MEDIAN is '1' and external SPI master has NO "late MISO sample functionality": SCB clock/IF clock >= 8. At a SCB frequency of 48 MHz, the maximum bit rate is 6 Mbps. - MEDIAN is '1' and external SPI master has "late MISO sample functionality": SCB clock/IF clock >= 4. At a SCB frequency of 48 MHz, the maximum bit rate is 12 Mbps. As discussed earlier, the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. In UART standard submode, the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15]. In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value: - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. SCB clock frequency of 16*57.6 KHz for 57.6 Kbps. SCB clock frequency of 16*38.4 KHz for 38.4 Kbps. SCB clock frequency of 16*19.2 KHz for 19.2 Kbps. SCB clock frequency of 16*9.6 KHz for 9.6 Kbps. SCB clock frequency of 16*2.4 KHz for 2.4 Kbps. SCB clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 Kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two SCB clock cycles are guaranteed to be detected by

		the receiver. Pulse widths less than two SCB clock cycles and greater or equal than one SCB clock cycle may be detected by the receiver. Pulse widths less than one SCB clock cycle will not be detected by the receiver. RX_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The SCB clock (as provided by the programmable clock block) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. SCB clock frequency of 16*57.6 KHz for 57.6 Kbps. SCB clock frequency of 16*38.4 KHz for 38.4 Kbps. SCB clock frequency of 16*19.2 KHz for 19.2 Kbps. SCB clock frequency of 16*9.6 KHz for 9.6 Kbps. SCB clock frequency of 16*2.4 KHz for 2.4 Kbps. SCB clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. Low power mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. - 1: 32 times oversampling. SCB clock frequency of 32*57.6 KHz for 57.6 Kbps. - 2: 48 times oversampling. SCB clock frequency of 48*38.4 KHz for 38.4 Kbps. - 3: 96 times oversampling. SCB clock frequency of 96*19.2 KHz for 19.2 Kbps. - 4: 192 times oversampling. SCB clock frequency of 192*9.6 KHz for 9.6 Kbps. - 5: 768 times oversampling. SCB clock frequency of 768*2.4 KHz for 2.4 Kbps. - 6: 1536 times oversampling. SCB clock frequency of 1536*1.2 KHz for 1.2 Kbps. - all other values are not used in low power mode. Default Value: 15

SCB1_I2C_STATUS

I2C status
Address: 0x40610064
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None	R	None	R
HW Access	None		W	W	None	W	None	W
Name	None [7:6]		M_READ	S_READ	None	I2CS_IC_BUSY	None	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined

5	M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0''. Default Value: 0
4	S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0''. Default Value: 0
2	I2CS_IC_BUSY	Indicates whether the internally clocked slave logic is being accessed by external I2C master. --set at ADDR_MATCH --clear at START/RESET, STOP detection, or BUS_ERROR This bit can be used by SW to determine whether I2CS_IC is busy before entering DeepSleep. Default Value: 0
0	BUS_BUSY	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If SCB block is disabled, BUS_BUSY is '0'. After enabling the block, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0

SCB1_INTR_CAUSE

Active clocked interrupt signal
Address: 0x40610E00
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	None	R	R	R	R
HW Access	None		W	None	W	W	W	W
Name	None [7:6]		SPI_EC	None	RX	TX	S	M

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	SPI_EC	Externally clocked SPI interrupt active ("interrupt_spi_ec"): INTR_SPI_EC_MASKED != 0. Default Value: 0
3	RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0
0	M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

14 Timer, counter, and pulse width modulator (TCPWM)

Register details

Register name	Address	Description
TCPWM0_GRP0_CNT0_CTRL	0x40380000	Counter control register
TCPWM0_GRP0_CNT0_STATUS	0x40380004	Counter status register
TCPWM0_GRP0_CNT0_COUNTER	0x40380008	Counter count register
TCPWM0_GRP0_CNT0_CC0	0x40380010	Counter compare/capture 0 register
TCPWM0_GRP0_CNT0_CC0_BUFF	0x40380014	Counter buffered compare/capture 0 register
TCPWM0_GRP0_CNT0_CC1	0x40380018	Counter compare/capture 1 register
TCPWM0_GRP0_CNT0_CC1_BUFF	0x4038001C	Counter buffered compare/capture 1 register
TCPWM0_GRP0_CNT0_PERIOD	0x40380020	Counter period register
TCPWM0_GRP0_CNT0_PERIOD_BUFF	0x40380024	Counter buffered period register
TCPWM0_GRP0_CNT0_DT	0x40380030	Counter PWM dead time register
TCPWM0_GRP0_CNT0_TR_CMD	0x40380040	Counter trigger command register
TCPWM0_GRP0_CNT0_TR_IN_SEL0	0x40380044	Counter input trigger selection register 0
TCPWM0_GRP0_CNT0_TR_IN_SEL1	0x40380048	Counter input trigger selection register 1
TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL	0x4038004C	Counter input trigger edge selection register
TCPWM0_GRP0_CNT0_TR_PWM_CTRL	0x40380050	Counter trigger PWM control register
TCPWM0_GRP0_CNT0_TR_OUT_SEL	0x40380054	Counter output trigger selection register
TCPWM0_GRP0_CNT0_INTR	0x40380070	Interrupt request register
TCPWM0_GRP0_CNT0_INTR_SET	0x40380074	Interrupt set request register
TCPWM0_GRP0_CNT0_INTR_MASK	0x40380078	Interrupt mask register
TCPWM0_GRP0_CNT0_INTR_MASKED	0x4038007C	Interrupt masked request register
TCPWM0_GRP0_CNT1_CTRL	0x40380080	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT1_STATUS	0x40380084	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT1_COUNTER	0x40380088	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT1_CC0	0x40380090	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT1_CC0_BUFF	0x40380094	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT1_CC1	0x40380098	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT1_CC1_BUFF	0x4038009C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT1_PERIOD	0x403800A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT1_PERIOD_BUFF	0x403800A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT1_DT	0x403800B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT1_TR_CMD	0x403800C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT1_TR_IN_SEL0	0x403800C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT1_TR_IN_SEL1	0x403800C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT1_TR_IN_EDGE_SEL	0x403800CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT1_TR_PWM_CTRL	0x403800D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT1_TR_OUT_SEL	0x403800D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT1_INTR	0x403800F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT1_INTR_SET	0x403800F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT1_INTR_MASK	0x403800F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT1_INTR_MASKED	0x403800FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT2_CTRL	0x40380100	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT2_STATUS	0x40380104	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT2_COUNTER	0x40380108	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT2_CC0	0x40380110	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT2_CC0_BUFF	0x40380114	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT2_CC1	0x40380118	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT2_CC1_BUFF	0x4038011C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT2_PERIOD	0x40380120	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT2_PERIOD_BUFF	0x40380124	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT2_DT	0x40380130	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT2_TR_CMD	0x40380140	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT2_TR_IN_SEL0	0x40380144	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT2_TR_IN_SEL1	0x40380148	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT2_TR_IN_EDGE_SEL	0x4038014C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT2_TR_PWM_CTRL	0x40380150	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT2_TR_OUT_SEL	0x40380154	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT2_INTR	0x40380170	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT2_INTR_SET	0x40380174	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT2_INTR_MASK	0x40380178	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT2_INTR_MASKED	0x4038017C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT3_CTRL	0x40380180	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT3_STATUS	0x40380184	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT3_COUNTER	0x40380188	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT3_CC0	0x40380190	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT3_CC0_BUFF	0x40380194	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT3_CC1	0x40380198	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT3_CC1_BUFF	0x4038019C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT3_PERIOD	0x403801A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT3_PERIOD_BUFF	0x403801A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT3_DT	0x403801B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT3_TR_CMD	0x403801C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT3_TR_IN_SEL0	0x403801C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT3_TR_IN_SEL1	0x403801C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT3_TR_IN_EDGE_SEL	0x403801CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT3_TR_PWM_CTRL	0x403801D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT3_TR_OUT_SEL	0x403801D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT3_INTR	0x403801F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT3_INTR_SET	0x403801F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT3_INTR_MASK	0x403801F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT3_INTR_MASKED	0x403801FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT4_CTRL	0x40380200	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT4_STATUS	0x40380204	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT4_COUNTER	0x40380208	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT4_CC0	0x40380210	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT4_CC0_BUFF	0x40380214	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT4_CC1	0x40380218	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT4_CC1_BUFF	0x4038021C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT4_PERIOD	0x40380220	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT4_PERIOD_BUFF	0x40380224	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT4_DT	0x40380230	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT4_TR_CMD	0x40380240	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT4_TR_IN_SEL0	0x40380244	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT4_TR_IN_SEL1	0x40380248	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT4_TR_IN_EDGE_SEL	0x4038024C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT4_TR_PWM_CTRL	0x40380250	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT4_TR_OUT_SEL	0x40380254	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT4_INTR	0x40380270	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT4_INTR_SET	0x40380274	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT4_INTR_MASK	0x40380278	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT4_INTR_MASKED	0x4038027C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT5_CTRL	0x40380280	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT5_STATUS	0x40380284	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT5_COUNTER	0x40380288	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT5_CC0	0x40380290	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT5_CC0_BUFF	0x40380294	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT5_CC1	0x40380298	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT5_CC1_BUFF	0x4038029C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT5_PERIOD	0x403802A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT5_PERIOD_BUFF	0x403802A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT5_DT	0x403802B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT5_TR_CMD	0x403802C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT5_TR_IN_SEL0	0x403802C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT5_TR_IN_SEL1	0x403802C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT5_TR_IN_EDGE_SEL	0x403802CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT5_TR_PWM_CTRL	0x403802D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT5_TR_OUT_SEL	0x403802D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT5_INTR	0x403802F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT5_INTR_SET	0x403802F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT5_INTR_MASK	0x403802F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT5_INTR_MASKED	0x403802FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT6_CTRL	0x40380300	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT6_STATUS	0x40380304	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT6_COUNTER	0x40380308	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT6_CC0	0x40380310	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT6_CC0_BUFF	0x40380314	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT6_CC1	0x40380318	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT6_CC1_BUFF	0x4038031C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT6_PERIOD	0x40380320	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT6_PERIOD_BUFF	0x40380324	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT6_DT	0x40380330	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT6_TR_CMD	0x40380340	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT6_TR_IN_SEL0	0x40380344	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT6_TR_IN_SEL1	0x40380348	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT6_TR_IN_EDGE_SEL	0x4038034C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT6_TR_PWM_CTRL	0x40380350	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT6_TR_OUT_SEL	0x40380354	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT6_INTR	0x40380370	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT6_INTR_SET	0x40380374	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT6_INTR_MASK	0x40380378	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT6_INTR_MASKED	0x4038037C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT7_CTRL	0x40380380	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT7_STATUS	0x40380384	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT7_COUNTER	0x40380388	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT7_CC0	0x40380390	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT7_CC0_BUFF	0x40380394	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT7_CC1	0x40380398	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT7_CC1_BUFF	0x4038039C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT7_PERIOD	0x403803A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT7_PERIOD_BUFF	0x403803A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT7_DT	0x403803B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT7_TR_CMD	0x403803C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT7_TR_IN_SEL0	0x403803C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT7_TR_IN_SEL1	0x403803C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT7_TR_IN_EDGE_SEL	0x403803CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT7_TR_PWM_CTRL	0x403803D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT7_TR_OUT_SEL	0x403803D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT7_INTR	0x403803F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT7_INTR_SET	0x403803F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT7_INTR_MASK	0x403803F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT7_INTR_MASKED	0x403803FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT8_CTRL	0x40380400	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT8_STATUS	0x40380404	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT8_COUNTER	0x40380408	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT8_CC0	0x40380410	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT8_CC0_BUFF	0x40380414	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT8_CC1	0x40380418	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT8_CC1_BUFF	0x4038041C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT8_PERIOD	0x40380420	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT8_PERIOD_BUFF	0x40380424	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT8_DT	0x40380430	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT8_TR_CMD	0x40380440	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT8_TR_IN_SEL0	0x40380444	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT8_TR_IN_SEL1	0x40380448	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT8_TR_IN_EDGE_SEL	0x4038044C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT8_TR_PWM_CTRL	0x40380450	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT8_TR_OUT_SEL	0x40380454	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT8_INTR	0x40380470	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT8_INTR_SET	0x40380474	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT8_INTR_MASK	0x40380478	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT8_INTR_MASKED	0x4038047C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT9_CTRL	0x40380480	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT9_STATUS	0x40380484	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT9_COUNTER	0x40380488	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT9_CC0	0x40380490	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT9_CC0_BUFF	0x40380494	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT9_CC1	0x40380498	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT9_CC1_BUFF	0x4038049C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT9_PERIOD	0x403804A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT9_PERIOD_BUFF	0x403804A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT9_DT	0x403804B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT9_TR_CMD	0x403804C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT9_TR_IN_SEL0	0x403804C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT9_TR_IN_SEL1	0x403804C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT9_TR_IN_EDGE_SEL	0x403804CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT9_TR_PWM_CTRL	0x403804D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT9_TR_OUT_SEL	0x403804D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT9_INTR	0x403804F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT9_INTR_SET	0x403804F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT9_INTR_MASK	0x403804F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT9_INTR_MASKED	0x403804FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT10_CTRL	0x40380500	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT10_STATUS	0x40380504	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT10_COUNTER	0x40380508	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT10_CC0	0x40380510	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT10_CC0_BUFF	0x40380514	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT10_CC1	0x40380518	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT10_CC1_BUFF	0x4038051C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT10_PERIOD	0x40380520	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT10_PERIOD_BUFF	0x40380524	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT10_DT	0x40380530	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT10_TR_CMD	0x40380540	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT10_TR_IN_SEL0	0x40380544	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT10_TR_IN_SEL1	0x40380548	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT10_TR_IN_EDGE_SEL	0x4038054C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT10_TR_PWM_CTRL	0x40380550	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT10_TR_OUT_SEL	0x40380554	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT10_INTR	0x40380570	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT10_INTR_SET	0x40380574	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT10_INTR_MASK	0x40380578	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT10_INTR_MASKED	0x4038057C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT11_CTRL	0x40380580	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT11_STATUS	0x40380584	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT11_COUNTER	0x40380588	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT11_CC0	0x40380590	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT11_CC0_BUFF	0x40380594	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT11_CC1	0x40380598	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT11_CC1_BUFF	0x4038059C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT11_PERIOD	0x403805A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT11_PERIOD_BUFF	0x403805A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT11_DT	0x403805B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT11_TR_CMD	0x403805C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT11_TR_IN_SEL0	0x403805C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT11_TR_IN_SEL1	0x403805C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT11_TR_IN_EDGE_SEL	0x403805CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT11_TR_PWM_CTRL	0x403805D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT11_TR_OUT_SEL	0x403805D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT11_INTR	0x403805F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT11_INTR_SET	0x403805F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT11_INTR_MASK	0x403805F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT11_INTR_MASKED	0x403805FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT12_CTRL	0x40380600	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT12_STATUS	0x40380604	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT12_COUNTER	0x40380608	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT12_CC0	0x40380610	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT12_CC0_BUFF	0x40380614	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT12_CC1	0x40380618	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT12_CC1_BUFF	0x4038061C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT12_PERIOD	0x40380620	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT12_PERIOD_BUFF	0x40380624	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT12_DT	0x40380630	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT12_TR_CMD	0x40380640	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT12_TR_IN_SEL0	0x40380644	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT12_TR_IN_SEL1	0x40380648	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT12_TR_IN_EDGE_SEL	0x4038064C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT12_TR_PWM_CTRL	0x40380650	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT12_TR_OUT_SEL	0x40380654	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT12_INTR	0x40380670	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT12_INTR_SET	0x40380674	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT12_INTR_MASK	0x40380678	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT12_INTR_MASKED	0x4038067C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT13_CTRL	0x40380680	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT13_STATUS	0x40380684	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT13_COUNTER	0x40380688	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT13_CC0	0x40380690	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT13_CC0_BUFF	0x40380694	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT13_CC1	0x40380698	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT13_CC1_BUFF	0x4038069C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT13_PERIOD	0x403806A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT13_PERIOD_BUFF	0x403806A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT13_DT	0x403806B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT13_TR_CMD	0x403806C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT13_TR_IN_SEL0	0x403806C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT13_TR_IN_SEL1	0x403806C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT13_TR_IN_EDGE_SEL	0x403806CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT13_TR_PWM_CTRL	0x403806D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT13_TR_OUT_SEL	0x403806D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT13_INTR	0x403806F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT13_INTR_SET	0x403806F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT13_INTR_MASK	0x403806F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT13_INTR_MASKED	0x403806FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT14_CTRL	0x40380700	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT14_STATUS	0x40380704	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT14_COUNTER	0x40380708	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT14_CC0	0x40380710	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT14_CC0_BUFF	0x40380714	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT14_CC1	0x40380718	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT14_CC1_BUFF	0x4038071C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT14_PERIOD	0x40380720	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT14_PERIOD_BUFF	0x40380724	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT14_DT	0x40380730	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT14_TR_CMD	0x40380740	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT14_TR_IN_SEL0	0x40380744	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT14_TR_IN_SEL1	0x40380748	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT14_TR_IN_EDGE_SEL	0x4038074C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT14_TR_PWM_CTRL	0x40380750	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT14_TR_OUT_SEL	0x40380754	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT14_INTR	0x40380770	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT14_INTR_SET	0x40380774	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT14_INTR_MASK	0x40380778	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT14_INTR_MASKED	0x4038077C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT15_CTRL	0x40380780	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT15_STATUS	0x40380784	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT15_COUNTER	0x40380788	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT15_CC0	0x40380790	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT15_CC0_BUFF	0x40380794	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT15_CC1	0x40380798	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT15_CC1_BUFF	0x4038079C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT15_PERIOD	0x403807A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT15_PERIOD_BUFF	0x403807A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT15_DT	0x403807B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT15_TR_CMD	0x403807C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT15_TR_IN_SEL0	0x403807C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT15_TR_IN_SEL1	0x403807C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT15_TR_IN_EDGE_SEL	0x403807CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT15_TR_PWM_CTRL	0x403807D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT15_TR_OUT_SEL	0x403807D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT15_INTR	0x403807F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT15_INTR_SET	0x403807F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT15_INTR_MASK	0x403807F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT15_INTR_MASKED	0x403807FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT16_CTRL	0x40380800	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT16_STATUS	0x40380804	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT16_COUNTER	0x40380808	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT16_CC0	0x40380810	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT16_CC0_BUFF	0x40380814	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT16_CC1	0x40380818	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT16_CC1_BUFF	0x4038081C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT16_PERIOD	0x40380820	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT16_PERIOD_BUFF	0x40380824	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT16_DT	0x40380830	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT16_TR_CMD	0x40380840	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT16_TR_IN_SEL0	0x40380844	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT16_TR_IN_SEL1	0x40380848	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT16_TR_IN_EDGE_SEL	0x4038084C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT16_TR_PWM_CTRL	0x40380850	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT16_TR_OUT_SEL	0x40380854	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT16_INTR	0x40380870	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT16_INTR_SET	0x40380874	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT16_INTR_MASK	0x40380878	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT16_INTR_MASKED	0x4038087C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT17_CTRL	0x40380880	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT17_STATUS	0x40380884	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT17_COUNTER	0x40380888	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT17_CC0	0x40380890	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT17_CC0_BUFF	0x40380894	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT17_CC1	0x40380898	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT17_CC1_BUFF	0x4038089C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT17_PERIOD	0x403808A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT17_PERIOD_BUFF	0x403808A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT17_DT	0x403808B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT17_TR_CMD	0x403808C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT17_TR_IN_SEL0	0x403808C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT17_TR_IN_SEL1	0x403808C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT17_TR_IN_EDGE_SEL	0x403808CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT17_TR_PWM_CTRL	0x403808D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT17_TR_OUT_SEL	0x403808D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT17_INTR	0x403808F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT17_INTR_SET	0x403808F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT17_INTR_MASK	0x403808F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT17_INTR_MASKED	0x403808FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT18_CTRL	0x40380900	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT18_STATUS	0x40380904	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT18_COUNTER	0x40380908	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT18_CC0	0x40380910	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT18_CC0_BUFF	0x40380914	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT18_CC1	0x40380918	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT18_CC1_BUFF	0x4038091C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT18_PERIOD	0x40380920	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT18_PERIOD_BUFF	0x40380924	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT18_DT	0x40380930	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT18_TR_CMD	0x40380940	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT18_TR_IN_SEL0	0x40380944	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT18_TR_IN_SEL1	0x40380948	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT18_TR_IN_EDGE_SEL	0x4038094C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT18_TR_PWM_CTRL	0x40380950	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT18_TR_OUT_SEL	0x40380954	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT18_INTR	0x40380970	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT18_INTR_SET	0x40380974	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT18_INTR_MASK	0x40380978	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT18_INTR_MASKED	0x4038097C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT19_CTRL	0x40380980	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT19_STATUS	0x40380984	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT19_COUNTER	0x40380988	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT19_CC0	0x40380990	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT19_CC0_BUFF	0x40380994	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT19_CC1	0x40380998	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT19_CC1_BUFF	0x4038099C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT19_PERIOD	0x403809A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT19_PERIOD_BUFF	0x403809A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT19_DT	0x403809B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT19_TR_CMD	0x403809C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT19_TR_IN_SEL0	0x403809C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT19_TR_IN_SEL1	0x403809C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT19_TR_IN_EDGE_SEL	0x403809CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT19_TR_PWM_CTRL	0x403809D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT19_TR_OUT_SEL	0x403809D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT19_INTR	0x403809F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT19_INTR_SET	0x403809F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT19_INTR_MASK	0x403809F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT19_INTR_MASKED	0x403809FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT20_CTRL	0x40380A00	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT20_STATUS	0x40380A04	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT20_COUNTER	0x40380A08	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT20_CC0	0x40380A10	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT20_CC0_BUFF	0x40380A14	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT20_CC1	0x40380A18	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT20_CC1_BUFF	0x40380A1C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT20_PERIOD	0x40380A20	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT20_PERIOD_BUFF	0x40380A24	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT20_DT	0x40380A30	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT20_TR_CMD	0x40380A40	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT20_TR_IN_SEL0	0x40380A44	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT20_TR_IN_SEL1	0x40380A48	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT20_TR_IN_EDGE_SEL	0x40380A4C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT20_TR_PWM_CTRL	0x40380A50	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT20_TR_OUT_SEL	0x40380A54	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT20_INTR	0x40380A70	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT20_INTR_SET	0x40380A74	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT20_INTR_MASK	0x40380A78	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT20_INTR_MASKED	0x40380A7C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT21_CTRL	0x40380A80	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT21_STATUS	0x40380A84	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT21_COUNTER	0x40380A88	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT21_CC0	0x40380A90	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT21_CC0_BUFF	0x40380A94	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT21_CC1	0x40380A98	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT21_CC1_BUFF	0x40380A9C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT21_PERIOD	0x40380AA0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT21_PERIOD_BUFF	0x40380AA4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT21_DT	0x40380AB0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT21_TR_CMD	0x40380AC0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT21_TR_IN_SEL0	0x40380AC4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT21_TR_IN_SEL1	0x40380AC8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT21_TR_IN_EDGE_SEL	0x40380ACC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT21_TR_PWM_CTRL	0x40380AD0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT21_TR_OUT_SEL	0x40380AD4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT21_INTR	0x40380AF0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT21_INTR_SET	0x40380AF4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT21_INTR_MASK	0x40380AF8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT21_INTR_MASKED	0x40380AFC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT22_CTRL	0x40380B00	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT22_STATUS	0x40380B04	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT22_COUNTER	0x40380B08	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT22_CC0	0x40380B10	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT22_CC0_BUFF	0x40380B14	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT22_CC1	0x40380B18	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT22_CC1_BUFF	0x40380B1C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT22_PERIOD	0x40380B20	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT22_PERIOD_BUFF	0x40380B24	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT22_DT	0x40380B30	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT22_TR_CMD	0x40380B40	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT22_TR_IN_SEL0	0x40380B44	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT22_TR_IN_SEL1	0x40380B48	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT22_TR_IN_EDGE_SEL	0x40380B4C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT22_TR_PWM_CTRL	0x40380B50	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT22_TR_OUT_SEL	0x40380B54	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT22_INTR	0x40380B70	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT22_INTR_SET	0x40380B74	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT22_INTR_MASK	0x40380B78	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT22_INTR_MASKED	0x40380B7C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT23_CTRL	0x40380B80	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT23_STATUS	0x40380B84	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT23_COUNTER	0x40380B88	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT23_CC0	0x40380B90	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT23_CC0_BUFF	0x40380B94	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT23_CC1	0x40380B98	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT23_CC1_BUFF	0x40380B9C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT23_PERIOD	0x40380BA0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT23_PERIOD_BUFF	0x40380BA4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT23_DT	0x40380BB0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT23_TR_CMD	0x40380BC0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT23_TR_IN_SEL0	0x40380BC4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT23_TR_IN_SEL1	0x40380BC8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT23_TR_IN_EDGE_SEL	0x40380BCC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT23_TR_PWM_CTRL	0x40380BD0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT23_TR_OUT_SEL	0x40380BD4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT23_INTR	0x40380BF0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT23_INTR_SET	0x40380BF4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT23_INTR_MASK	0x40380BF8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT23_INTR_MASKED	0x40380BFC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT24_CTRL	0x40380C00	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT24_STATUS	0x40380C04	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT24_COUNTER	0x40380C08	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT24_CC0	0x40380C10	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT24_CC0_BUFF	0x40380C14	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT24_CC1	0x40380C18	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT24_CC1_BUFF	0x40380C1C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT24_PERIOD	0x40380C20	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT24_PERIOD_BUFF	0x40380C24	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT24_DT	0x40380C30	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT24_TR_CMD	0x40380C40	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT24_TR_IN_SEL0	0x40380C44	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT24_TR_IN_SEL1	0x40380C48	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT24_TR_IN_EDGE_SEL	0x40380C4C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT24_TR_PWM_CTRL	0x40380C50	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT24_TR_OUT_SEL	0x40380C54	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT24_INTR	0x40380C70	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT24_INTR_SET	0x40380C74	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT24_INTR_MASK	0x40380C78	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT24_INTR_MASKED	0x40380C7C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT25_CTRL	0x40380C80	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT25_STATUS	0x40380C84	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT25_COUNTER	0x40380C88	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT25_CC0	0x40380C90	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT25_CC0_BUFF	0x40380C94	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT25_CC1	0x40380C98	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT25_CC1_BUFF	0x40380C9C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT25_PERIOD	0x40380CA0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT25_PERIOD_BUFF	0x40380CA4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT25_DT	0x40380CB0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT25_TR_CMD	0x40380CC0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT25_TR_IN_SEL0	0x40380CC4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT25_TR_IN_SEL1	0x40380CC8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT25_TR_IN_EDGE_SEL	0x40380CCC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT25_TR_PWM_CTRL	0x40380CD0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT25_TR_OUT_SEL	0x40380CD4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT25_INTR	0x40380CF0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT25_INTR_SET	0x40380CF4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT25_INTR_MASK	0x40380CF8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT25_INTR_MASKED	0x40380CFC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT26_CTRL	0x40380D00	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT26_STATUS	0x40380D04	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT26_COUNTER	0x40380D08	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT26_CC0	0x40380D10	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT26_CC0_BUFF	0x40380D14	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT26_CC1	0x40380D18	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT26_CC1_BUFF	0x40380D1C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT26_PERIOD	0x40380D20	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT26_PERIOD_BUFF	0x40380D24	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT26_DT	0x40380D30	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT26_TR_CMD	0x40380D40	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT26_TR_IN_SEL0	0x40380D44	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT26_TR_IN_SEL1	0x40380D48	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT26_TR_IN_EDGE_SEL	0x40380D4C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT26_TR_PWM_CTRL	0x40380D50	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT26_TR_OUT_SEL	0x40380D54	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT26_INTR	0x40380D70	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT26_INTR_SET	0x40380D74	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT26_INTR_MASK	0x40380D78	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT26_INTR_MASKED	0x40380D7C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT27_CTRL	0x40380D80	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT27_STATUS	0x40380D84	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT27_COUNTER	0x40380D88	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT27_CC0	0x40380D90	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT27_CC0_BUFF	0x40380D94	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT27_CC1	0x40380D98	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT27_CC1_BUFF	0x40380D9C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT27_PERIOD	0x40380DA0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT27_PERIOD_BUFF	0x40380DA4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT27_DT	0x40380DB0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT27_TR_CMD	0x40380DC0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT27_TR_IN_SEL0	0x40380DC4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT27_TR_IN_SEL1	0x40380DC8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT27_TR_IN_EDGE_SEL	0x40380DCC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT27_TR_PWM_CTRL	0x40380DD0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT27_TR_OUT_SEL	0x40380DD4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT27_INTR	0x40380DF0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT27_INTR_SET	0x40380DF4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT27_INTR_MASK	0x40380DF8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT27_INTR_MASKED	0x40380DFC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT28_CTRL	0x40380E00	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT28_STATUS	0x40380E04	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT28_COUNTER	0x40380E08	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT28_CC0	0x40380E10	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT28_CC0_BUFF	0x40380E14	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT28_CC1	0x40380E18	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT28_CC1_BUFF	0x40380E1C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT28_PERIOD	0x40380E20	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT28_PERIOD_BUFF	0x40380E24	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT28_DT	0x40380E30	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT28_TR_CMD	0x40380E40	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT28_TR_IN_SEL0	0x40380E44	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT28_TR_IN_SEL1	0x40380E48	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT28_TR_IN_EDGE_SEL	0x40380E4C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT28_TR_PWM_CTRL	0x40380E50	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT28_TR_OUT_SEL	0x40380E54	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT28_INTR	0x40380E70	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT28_INTR_SET	0x40380E74	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT28_INTR_MASK	0x40380E78	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT28_INTR_MASKED	0x40380E7C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT29_CTRL	0x40380E80	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT29_STATUS	0x40380E84	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT29_COUNTER	0x40380E88	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT29_CC0	0x40380E90	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT29_CC0_BUFF	0x40380E94	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT29_CC1	0x40380E98	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT29_CC1_BUFF	0x40380E9C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT29_PERIOD	0x40380EA0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT29_PERIOD_BUFF	0x40380EA4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT29_DT	0x40380EB0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT29_TR_CMD	0x40380EC0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT29_TR_IN_SEL0	0x40380EC4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT29_TR_IN_SEL1	0x40380EC8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT29_TR_IN_EDGE_SEL	0x40380ECC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT29_TR_PWM_CTRL	0x40380ED0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT29_TR_OUT_SEL	0x40380ED4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT29_INTR	0x40380EF0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT29_INTR_SET	0x40380EF4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT29_INTR_MASK	0x40380EF8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT29_INTR_MASKED	0x40380EFC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT30_CTRL	0x40380F00	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT30_STATUS	0x40380F04	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT30_COUNTER	0x40380F08	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT30_CC0	0x40380F10	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT30_CC0_BUFF	0x40380F14	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT30_CC1	0x40380F18	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT30_CC1_BUFF	0x40380F1C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT30_PERIOD	0x40380F20	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT30_PERIOD_BUFF	0x40380F24	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT30_DT	0x40380F30	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT30_TR_CMD	0x40380F40	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT30_TR_IN_SEL0	0x40380F44	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT30_TR_IN_SEL1	0x40380F48	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT30_TR_IN_EDGE_SEL	0x40380F4C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT30_TR_PWM_CTRL	0x40380F50	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT30_TR_OUT_SEL	0x40380F54	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT30_INTR	0x40380F70	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT30_INTR_SET	0x40380F74	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT30_INTR_MASK	0x40380F78	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT30_INTR_MASKED	0x40380F7C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT31_CTRL	0x40380F80	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT31_STATUS	0x40380F84	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT31_COUNTER	0x40380F88	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT31_CC0	0x40380F90	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT31_CC0_BUFF	0x40380F94	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT31_CC1	0x40380F98	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT31_CC1_BUFF	0x40380F9C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT31_PERIOD	0x40380FA0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT31_PERIOD_BUFF	0x40380FA4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT31_DT	0x40380FB0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT31_TR_CMD	0x40380FC0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT31_TR_IN_SEL0	0x40380FC4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT31_TR_IN_SEL1	0x40380FC8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT31_TR_IN_EDGE_SEL	0x40380FCC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT31_TR_PWM_CTRL	0x40380FD0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT31_TR_OUT_SEL	0x40380FD4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT31_INTR	0x40380FF0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT31_INTR_SET	0x40380FF4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT31_INTR_MASK	0x40380FF8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT31_INTR_MASKED	0x40380FFC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT32_CTRL	0x40381000	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT32_STATUS	0x40381004	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT32_COUNTER	0x40381008	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT32_CC0	0x40381010	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT32_CC0_BUFF	0x40381014	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT32_CC1	0x40381018	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT32_CC1_BUFF	0x4038101C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT32_PERIOD	0x40381020	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT32_PERIOD_BUFF	0x40381024	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT32_DT	0x40381030	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT32_TR_CMD	0x40381040	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT32_TR_IN_SEL0	0x40381044	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT32_TR_IN_SEL1	0x40381048	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT32_TR_IN_EDGE_SEL	0x4038104C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT32_TR_PWM_CTRL	0x40381050	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT32_TR_OUT_SEL	0x40381054	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT32_INTR	0x40381070	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT32_INTR_SET	0x40381074	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT32_INTR_MASK	0x40381078	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT32_INTR_MASKED	0x4038107C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT33_CTRL	0x40381080	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT33_STATUS	0x40381084	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT33_COUNTER	0x40381088	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT33_CC0	0x40381090	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT33_CC0_BUFF	0x40381094	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT33_CC1	0x40381098	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT33_CC1_BUFF	0x4038109C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT33_PERIOD	0x403810A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT33_PERIOD_BUFF	0x403810A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT33_DT	0x403810B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT33_TR_CMD	0x403810C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT33_TR_IN_SEL0	0x403810C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT33_TR_IN_SEL1	0x403810C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT33_TR_IN_EDGE_SEL	0x403810CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT33_TR_PWM_CTRL	0x403810D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT33_TR_OUT_SEL	0x403810D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT33_INTR	0x403810F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT33_INTR_SET	0x403810F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT33_INTR_MASK	0x403810F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT33_INTR_MASKED	0x403810FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT34_CTRL	0x40381100	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT34_STATUS	0x40381104	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT34_COUNTER	0x40381108	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT34_CC0	0x40381110	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT34_CC0_BUFF	0x40381114	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT34_CC1	0x40381118	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT34_CC1_BUFF	0x4038111C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT34_PERIOD	0x40381120	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT34_PERIOD_BUFF	0x40381124	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT34_DT	0x40381130	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT34_TR_CMD	0x40381140	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT34_TR_IN_SEL0	0x40381144	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT34_TR_IN_SEL1	0x40381148	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT34_TR_IN_EDGE_SEL	0x4038114C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT34_TR_PWM_CTRL	0x40381150	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT34_TR_OUT_SEL	0x40381154	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT34_INTR	0x40381170	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT34_INTR_SET	0x40381174	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT34_INTR_MASK	0x40381178	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT34_INTR_MASKED	0x4038117C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT35_CTRL	0x40381180	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT35_STATUS	0x40381184	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT35_COUNTER	0x40381188	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT35_CC0	0x40381190	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT35_CC0_BUFF	0x40381194	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT35_CC1	0x40381198	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT35_CC1_BUFF	0x4038119C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT35_PERIOD	0x403811A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT35_PERIOD_BUFF	0x403811A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT35_DT	0x403811B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT35_TR_CMD	0x403811C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT35_TR_IN_SEL0	0x403811C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT35_TR_IN_SEL1	0x403811C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT35_TR_IN_EDGE_SEL	0x403811CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT35_TR_PWM_CTRL	0x403811D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT35_TR_OUT_SEL	0x403811D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT35_INTR	0x403811F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT35_INTR_SET	0x403811F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT35_INTR_MASK	0x403811F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT35_INTR_MASKED	0x403811FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT36_CTRL	0x40381200	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT36_STATUS	0x40381204	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT36_COUNTER	0x40381208	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT36_CC0	0x40381210	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT36_CC0_BUFF	0x40381214	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT36_CC1	0x40381218	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT36_CC1_BUFF	0x4038121C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT36_PERIOD	0x40381220	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT36_PERIOD_BUFF	0x40381224	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT36_DT	0x40381230	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT36_TR_CMD	0x40381240	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT36_TR_IN_SEL0	0x40381244	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT36_TR_IN_SEL1	0x40381248	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT36_TR_IN_EDGE_SEL	0x4038124C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT36_TR_PWM_CTRL	0x40381250	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT36_TR_OUT_SEL	0x40381254	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT36_INTR	0x40381270	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT36_INTR_SET	0x40381274	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT36_INTR_MASK	0x40381278	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT36_INTR_MASKED	0x4038127C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT37_CTRL	0x40381280	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT37_STATUS	0x40381284	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT37_COUNTER	0x40381288	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT37_CC0	0x40381290	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT37_CC0_BUFF	0x40381294	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT37_CC1	0x40381298	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT37_CC1_BUFF	0x4038129C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT37_PERIOD	0x403812A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT37_PERIOD_BUFF	0x403812A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT37_DT	0x403812B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT37_TR_CMD	0x403812C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT37_TR_IN_SEL0	0x403812C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT37_TR_IN_SEL1	0x403812C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT37_TR_IN_EDGE_SEL	0x403812CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT37_TR_PWM_CTRL	0x403812D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT37_TR_OUT_SEL	0x403812D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT37_INTR	0x403812F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT37_INTR_SET	0x403812F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT37_INTR_MASK	0x403812F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT37_INTR_MASKED	0x403812FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT38_CTRL	0x40381300	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT38_STATUS	0x40381304	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT38_COUNTER	0x40381308	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT38_CC0	0x40381310	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT38_CC0_BUFF	0x40381314	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT38_CC1	0x40381318	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT38_CC1_BUFF	0x4038131C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT38_PERIOD	0x40381320	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT38_PERIOD_BUFF	0x40381324	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT38_DT	0x40381330	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT38_TR_CMD	0x40381340	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT38_TR_IN_SEL0	0x40381344	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT38_TR_IN_SEL1	0x40381348	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT38_TR_IN_EDGE_SEL	0x4038134C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT38_TR_PWM_CTRL	0x40381350	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT38_TR_OUT_SEL	0x40381354	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT38_INTR	0x40381370	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT38_INTR_SET	0x40381374	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT38_INTR_MASK	0x40381378	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT38_INTR_MASKED	0x4038137C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT39_CTRL	0x40381380	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT39_STATUS	0x40381384	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT39_COUNTER	0x40381388	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT39_CC0	0x40381390	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT39_CC0_BUFF	0x40381394	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT39_CC1	0x40381398	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT39_CC1_BUFF	0x4038139C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT39_PERIOD	0x403813A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT39_PERIOD_BUFF	0x403813A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT39_DT	0x403813B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT39_TR_CMD	0x403813C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT39_TR_IN_SEL0	0x403813C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT39_TR_IN_SEL1	0x403813C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT39_TR_IN_EDGE_SEL	0x403813CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT39_TR_PWM_CTRL	0x403813D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT39_TR_OUT_SEL	0x403813D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT39_INTR	0x403813F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT39_INTR_SET	0x403813F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT39_INTR_MASK	0x403813F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT39_INTR_MASKED	0x403813FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT40_CTRL	0x40381400	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT40_STATUS	0x40381404	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT40_COUNTER	0x40381408	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT40_CC0	0x40381410	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT40_CC0_BUFF	0x40381414	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT40_CC1	0x40381418	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT40_CC1_BUFF	0x4038141C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT40_PERIOD	0x40381420	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT40_PERIOD_BUFF	0x40381424	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT40_DT	0x40381430	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT40_TR_CMD	0x40381440	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT40_TR_IN_SEL0	0x40381444	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT40_TR_IN_SEL1	0x40381448	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT40_TR_IN_EDGE_SEL	0x4038144C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT40_TR_PWM_CTRL	0x40381450	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT40_TR_OUT_SEL	0x40381454	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT40_INTR	0x40381470	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT40_INTR_SET	0x40381474	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT40_INTR_MASK	0x40381478	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT40_INTR_MASKED	0x4038147C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT41_CTRL	0x40381480	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT41_STATUS	0x40381484	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT41_COUNTER	0x40381488	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT41_CC0	0x40381490	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT41_CC0_BUFF	0x40381494	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT41_CC1	0x40381498	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT41_CC1_BUFF	0x4038149C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT41_PERIOD	0x403814A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT41_PERIOD_BUFF	0x403814A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT41_DT	0x403814B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT41_TR_CMD	0x403814C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT41_TR_IN_SEL0	0x403814C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT41_TR_IN_SEL1	0x403814C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT41_TR_IN_EDGE_SEL	0x403814CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT41_TR_PWM_CTRL	0x403814D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT41_TR_OUT_SEL	0x403814D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT41_INTR	0x403814F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT41_INTR_SET	0x403814F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT41_INTR_MASK	0x403814F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT41_INTR_MASKED	0x403814FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT42_CTRL	0x40381500	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT42_STATUS	0x40381504	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT42_COUNTER	0x40381508	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT42_CC0	0x40381510	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT42_CC0_BUFF	0x40381514	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT42_CC1	0x40381518	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT42_CC1_BUFF	0x4038151C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT42_PERIOD	0x40381520	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT42_PERIOD_BUFF	0x40381524	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT42_DT	0x40381530	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT42_TR_CMD	0x40381540	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT42_TR_IN_SEL0	0x40381544	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT42_TR_IN_SEL1	0x40381548	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT42_TR_IN_EDGE_SEL	0x4038154C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT42_TR_PWM_CTRL	0x40381550	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT42_TR_OUT_SEL	0x40381554	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT42_INTR	0x40381570	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT42_INTR_SET	0x40381574	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT42_INTR_MASK	0x40381578	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT42_INTR_MASKED	0x4038157C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT43_CTRL	0x40381580	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT43_STATUS	0x40381584	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT43_COUNTER	0x40381588	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT43_CC0	0x40381590	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT43_CC0_BUFF	0x40381594	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT43_CC1	0x40381598	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT43_CC1_BUFF	0x4038159C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT43_PERIOD	0x403815A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT43_PERIOD_BUFF	0x403815A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT43_DT	0x403815B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT43_TR_CMD	0x403815C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT43_TR_IN_SEL0	0x403815C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT43_TR_IN_SEL1	0x403815C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT43_TR_IN_EDGE_SEL	0x403815CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT43_TR_PWM_CTRL	0x403815D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT43_TR_OUT_SEL	0x403815D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT43_INTR	0x403815F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT43_INTR_SET	0x403815F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT43_INTR_MASK	0x403815F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT43_INTR_MASKED	0x403815FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT44_CTRL	0x40381600	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT44_STATUS	0x40381604	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT44_COUNTER	0x40381608	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT44_CC0	0x40381610	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT44_CC0_BUFF	0x40381614	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT44_CC1	0x40381618	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT44_CC1_BUFF	0x4038161C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT44_PERIOD	0x40381620	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT44_PERIOD_BUFF	0x40381624	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT44_DT	0x40381630	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT44_TR_CMD	0x40381640	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT44_TR_IN_SEL0	0x40381644	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT44_TR_IN_SEL1	0x40381648	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT44_TR_IN_EDGE_SEL	0x4038164C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT44_TR_PWM_CTRL	0x40381650	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT44_TR_OUT_SEL	0x40381654	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT44_INTR	0x40381670	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT44_INTR_SET	0x40381674	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT44_INTR_MASK	0x40381678	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT44_INTR_MASKED	0x4038167C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT45_CTRL	0x40381680	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT45_STATUS	0x40381684	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT45_COUNTER	0x40381688	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT45_CC0	0x40381690	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT45_CC0_BUFF	0x40381694	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT45_CC1	0x40381698	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT45_CC1_BUFF	0x4038169C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT45_PERIOD	0x403816A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT45_PERIOD_BUFF	0x403816A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT45_DT	0x403816B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT45_TR_CMD	0x403816C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT45_TR_IN_SEL0	0x403816C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT45_TR_IN_SEL1	0x403816C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT45_TR_IN_EDGE_SEL	0x403816CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT45_TR_PWM_CTRL	0x403816D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT45_TR_OUT_SEL	0x403816D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT45_INTR	0x403816F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT45_INTR_SET	0x403816F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT45_INTR_MASK	0x403816F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT45_INTR_MASKED	0x403816FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT46_CTRL	0x40381700	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT46_STATUS	0x40381704	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT46_COUNTER	0x40381708	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT46_CC0	0x40381710	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT46_CC0_BUFF	0x40381714	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT46_CC1	0x40381718	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT46_CC1_BUFF	0x4038171C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT46_PERIOD	0x40381720	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT46_PERIOD_BUFF	0x40381724	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT46_DT	0x40381730	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT46_TR_CMD	0x40381740	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT46_TR_IN_SEL0	0x40381744	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT46_TR_IN_SEL1	0x40381748	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT46_TR_IN_EDGE_SEL	0x4038174C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT46_TR_PWM_CTRL	0x40381750	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT46_TR_OUT_SEL	0x40381754	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT46_INTR	0x40381770	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT46_INTR_SET	0x40381774	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT46_INTR_MASK	0x40381778	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT46_INTR_MASKED	0x4038177C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT47_CTRL	0x40381780	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT47_STATUS	0x40381784	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT47_COUNTER	0x40381788	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT47_CC0	0x40381790	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT47_CC0_BUFF	0x40381794	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT47_CC1	0x40381798	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT47_CC1_BUFF	0x4038179C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT47_PERIOD	0x403817A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT47_PERIOD_BUFF	0x403817A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT47_DT	0x403817B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT47_TR_CMD	0x403817C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT47_TR_IN_SEL0	0x403817C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT47_TR_IN_SEL1	0x403817C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT47_TR_IN_EDGE_SEL	0x403817CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT47_TR_PWM_CTRL	0x403817D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT47_TR_OUT_SEL	0x403817D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT47_INTR	0x403817F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT47_INTR_SET	0x403817F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT47_INTR_MASK	0x403817F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT47_INTR_MASKED	0x403817FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT48_CTRL	0x40381800	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT48_STATUS	0x40381804	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT48_COUNTER	0x40381808	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT48_CC0	0x40381810	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT48_CC0_BUFF	0x40381814	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT48_CC1	0x40381818	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT48_CC1_BUFF	0x4038181C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT48_PERIOD	0x40381820	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT48_PERIOD_BUFF	0x40381824	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT48_DT	0x40381830	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT48_TR_CMD	0x40381840	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT48_TR_IN_SEL0	0x40381844	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT48_TR_IN_SEL1	0x40381848	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT48_TR_IN_EDGE_SEL	0x4038184C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT48_TR_PWM_CTRL	0x40381850	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT48_TR_OUT_SEL	0x40381854	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT48_INTR	0x40381870	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT48_INTR_SET	0x40381874	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT48_INTR_MASK	0x40381878	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT48_INTR_MASKED	0x4038187C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT49_CTRL	0x40381880	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT49_STATUS	0x40381884	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT49_COUNTER	0x40381888	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT49_CC0	0x40381890	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT49_CC0_BUFF	0x40381894	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT49_CC1	0x40381898	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT49_CC1_BUFF	0x4038189C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT49_PERIOD	0x403818A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT49_PERIOD_BUFF	0x403818A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT49_DT	0x403818B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT49_TR_CMD	0x403818C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT49_TR_IN_SEL0	0x403818C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT49_TR_IN_SEL1	0x403818C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT49_TR_IN_EDGE_SEL	0x403818CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT49_TR_PWM_CTRL	0x403818D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT49_TR_OUT_SEL	0x403818D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT49_INTR	0x403818F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT49_INTR_SET	0x403818F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT49_INTR_MASK	0x403818F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT49_INTR_MASKED	0x403818FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT50_CTRL	0x40381900	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT50_STATUS	0x40381904	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT50_COUNTER	0x40381908	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT50_CC0	0x40381910	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT50_CC0_BUFF	0x40381914	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT50_CC1	0x40381918	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT50_CC1_BUFF	0x4038191C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT50_PERIOD	0x40381920	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT50_PERIOD_BUFF	0x40381924	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT50_DT	0x40381930	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT50_TR_CMD	0x40381940	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT50_TR_IN_SEL0	0x40381944	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT50_TR_IN_SEL1	0x40381948	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT50_TR_IN_EDGE_SEL	0x4038194C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT50_TR_PWM_CTRL	0x40381950	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT50_TR_OUT_SEL	0x40381954	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT50_INTR	0x40381970	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT50_INTR_SET	0x40381974	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT50_INTR_MASK	0x40381978	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT50_INTR_MASKED	0x4038197C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT51_CTRL	0x40381980	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT51_STATUS	0x40381984	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT51_COUNTER	0x40381988	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT51_CC0	0x40381990	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT51_CC0_BUFF	0x40381994	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT51_CC1	0x40381998	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT51_CC1_BUFF	0x4038199C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT51_PERIOD	0x403819A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT51_PERIOD_BUFF	0x403819A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT51_DT	0x403819B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT51_TR_CMD	0x403819C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT51_TR_IN_SEL0	0x403819C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT51_TR_IN_SEL1	0x403819C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT51_TR_IN_EDGE_SEL	0x403819CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT51_TR_PWM_CTRL	0x403819D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT51_TR_OUT_SEL	0x403819D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT51_INTR	0x403819F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT51_INTR_SET	0x403819F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT51_INTR_MASK	0x403819F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT51_INTR_MASKED	0x403819FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT52_CTRL	0x40381A00	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT52_STATUS	0x40381A04	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT52_COUNTER	0x40381A08	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT52_CC0	0x40381A10	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT52_CC0_BUFF	0x40381A14	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT52_CC1	0x40381A18	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT52_CC1_BUFF	0x40381A1C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT52_PERIOD	0x40381A20	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT52_PERIOD_BUFF	0x40381A24	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT52_DT	0x40381A30	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT52_TR_CMD	0x40381A40	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT52_TR_IN_SEL0	0x40381A44	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT52_TR_IN_SEL1	0x40381A48	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT52_TR_IN_EDGE_SEL	0x40381A4C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT52_TR_PWM_CTRL	0x40381A50	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT52_TR_OUT_SEL	0x40381A54	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT52_INTR	0x40381A70	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT52_INTR_SET	0x40381A74	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT52_INTR_MASK	0x40381A78	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT52_INTR_MASKED	0x40381A7C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT53_CTRL	0x40381A80	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT53_STATUS	0x40381A84	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT53_COUNTER	0x40381A88	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT53_CC0	0x40381A90	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT53_CC0_BUFF	0x40381A94	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT53_CC1	0x40381A98	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT53_CC1_BUFF	0x40381A9C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT53_PERIOD	0x40381AA0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT53_PERIOD_BUFF	0x40381AA4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT53_DT	0x40381AB0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT53_TR_CMD	0x40381AC0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT53_TR_IN_SEL0	0x40381AC4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT53_TR_IN_SEL1	0x40381AC8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT53_TR_IN_EDGE_SEL	0x40381ACC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT53_TR_PWM_CTRL	0x40381AD0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT53_TR_OUT_SEL	0x40381AD4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT53_INTR	0x40381AF0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT53_INTR_SET	0x40381AF4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT53_INTR_MASK	0x40381AF8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT53_INTR_MASKED	0x40381AFC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT54_CTRL	0x40381B00	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT54_STATUS	0x40381B04	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT54_COUNTER	0x40381B08	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT54_CC0	0x40381B10	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT54_CC0_BUFF	0x40381B14	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT54_CC1	0x40381B18	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT54_CC1_BUFF	0x40381B1C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT54_PERIOD	0x40381B20	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT54_PERIOD_BUFF	0x40381B24	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT54_DT	0x40381B30	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT54_TR_CMD	0x40381B40	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT54_TR_IN_SEL0	0x40381B44	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT54_TR_IN_SEL1	0x40381B48	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT54_TR_IN_EDGE_SEL	0x40381B4C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT54_TR_PWM_CTRL	0x40381B50	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT54_TR_OUT_SEL	0x40381B54	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT54_INTR	0x40381B70	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT54_INTR_SET	0x40381B74	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT54_INTR_MASK	0x40381B78	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT54_INTR_MASKED	0x40381B7C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT55_CTRL	0x40381B80	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT55_STATUS	0x40381B84	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT55_COUNTER	0x40381B88	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT55_CC0	0x40381B90	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT55_CC0_BUFF	0x40381B94	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT55_CC1	0x40381B98	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT55_CC1_BUFF	0x40381B9C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT55_PERIOD	0x40381BA0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT55_PERIOD_BUFF	0x40381BA4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT55_DT	0x40381BB0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT55_TR_CMD	0x40381BC0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT55_TR_IN_SEL0	0x40381BC4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT55_TR_IN_SEL1	0x40381BC8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT55_TR_IN_EDGE_SEL	0x40381BCC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT55_TR_PWM_CTRL	0x40381BD0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT55_TR_OUT_SEL	0x40381BD4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT55_INTR	0x40381BF0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT55_INTR_SET	0x40381BF4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT55_INTR_MASK	0x40381BF8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT55_INTR_MASKED	0x40381BFC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT56_CTRL	0x40381C00	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT56_STATUS	0x40381C04	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT56_COUNTER	0x40381C08	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT56_CC0	0x40381C10	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT56_CC0_BUFF	0x40381C14	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT56_CC1	0x40381C18	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT56_CC1_BUFF	0x40381C1C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT56_PERIOD	0x40381C20	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT56_PERIOD_BUFF	0x40381C24	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT56_DT	0x40381C30	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT56_TR_CMD	0x40381C40	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT56_TR_IN_SEL0	0x40381C44	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT56_TR_IN_SEL1	0x40381C48	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT56_TR_IN_EDGE_SEL	0x40381C4C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT56_TR_PWM_CTRL	0x40381C50	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT56_TR_OUT_SEL	0x40381C54	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT56_INTR	0x40381C70	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT56_INTR_SET	0x40381C74	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT56_INTR_MASK	0x40381C78	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT56_INTR_MASKED	0x40381C7C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT57_CTRL	0x40381C80	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT57_STATUS	0x40381C84	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT57_COUNTER	0x40381C88	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT57_CC0	0x40381C90	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT57_CC0_BUFF	0x40381C94	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT57_CC1	0x40381C98	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT57_CC1_BUFF	0x40381C9C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT57_PERIOD	0x40381CA0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT57_PERIOD_BUFF	0x40381CA4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT57_DT	0x40381CB0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT57_TR_CMD	0x40381CC0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT57_TR_IN_SEL0	0x40381CC4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT57_TR_IN_SEL1	0x40381CC8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT57_TR_IN_EDGE_SEL	0x40381CCC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT57_TR_PWM_CTRL	0x40381CD0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT57_TR_OUT_SEL	0x40381CD4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT57_INTR	0x40381CF0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT57_INTR_SET	0x40381CF4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT57_INTR_MASK	0x40381CF8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT57_INTR_MASKED	0x40381CFC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT58_CTRL	0x40381D00	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT58_STATUS	0x40381D04	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT58_COUNTER	0x40381D08	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT58_CC0	0x40381D10	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT58_CC0_BUFF	0x40381D14	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT58_CC1	0x40381D18	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT58_CC1_BUFF	0x40381D1C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT58_PERIOD	0x40381D20	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT58_PERIOD_BUFF	0x40381D24	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT58_DT	0x40381D30	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT58_TR_CMD	0x40381D40	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT58_TR_IN_SEL0	0x40381D44	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT58_TR_IN_SEL1	0x40381D48	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT58_TR_IN_EDGE_SEL	0x40381D4C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT58_TR_PWM_CTRL	0x40381D50	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT58_TR_OUT_SEL	0x40381D54	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT58_INTR	0x40381D70	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT58_INTR_SET	0x40381D74	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT58_INTR_MASK	0x40381D78	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT58_INTR_MASKED	0x40381D7C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT59_CTRL	0x40381D80	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT59_STATUS	0x40381D84	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT59_COUNTER	0x40381D88	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT59_CC0	0x40381D90	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT59_CC0_BUFF	0x40381D94	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT59_CC1	0x40381D98	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT59_CC1_BUFF	0x40381D9C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT59_PERIOD	0x40381DA0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT59_PERIOD_BUFF	0x40381DA4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT59_DT	0x40381DB0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT59_TR_CMD	0x40381DC0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT59_TR_IN_SEL0	0x40381DC4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT59_TR_IN_SEL1	0x40381DC8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT59_TR_IN_EDGE_SEL	0x40381DCC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT59_TR_PWM_CTRL	0x40381DD0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT59_TR_OUT_SEL	0x40381DD4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT59_INTR	0x40381DF0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT59_INTR_SET	0x40381DF4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT59_INTR_MASK	0x40381DF8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT59_INTR_MASKED	0x40381DFC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT60_CTRL	0x40381E00	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT60_STATUS	0x40381E04	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT60_COUNTER	0x40381E08	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT60_CC0	0x40381E10	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT60_CC0_BUFF	0x40381E14	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT60_CC1	0x40381E18	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT60_CC1_BUFF	0x40381E1C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT60_PERIOD	0x40381E20	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT60_PERIOD_BUFF	0x40381E24	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT60_DT	0x40381E30	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT60_TR_CMD	0x40381E40	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT60_TR_IN_SEL0	0x40381E44	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT60_TR_IN_SEL1	0x40381E48	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT60_TR_IN_EDGE_SEL	0x40381E4C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT60_TR_PWM_CTRL	0x40381E50	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT60_TR_OUT_SEL	0x40381E54	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT60_INTR	0x40381E70	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT60_INTR_SET	0x40381E74	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT60_INTR_MASK	0x40381E78	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT60_INTR_MASKED	0x40381E7C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT61_CTRL	0x40381E80	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT61_STATUS	0x40381E84	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT61_COUNTER	0x40381E88	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT61_CC0	0x40381E90	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT61_CC0_BUFF	0x40381E94	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT61_CC1	0x40381E98	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT61_CC1_BUFF	0x40381E9C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT61_PERIOD	0x40381EA0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT61_PERIOD_BUFF	0x40381EA4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT61_DT	0x40381EB0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT61_TR_CMD	0x40381EC0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT61_TR_IN_SEL0	0x40381EC4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT61_TR_IN_SEL1	0x40381EC8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT61_TR_IN_EDGE_SEL	0x40381ECC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT61_TR_PWM_CTRL	0x40381ED0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT61_TR_OUT_SEL	0x40381ED4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT61_INTR	0x40381EF0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT61_INTR_SET	0x40381EF4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT61_INTR_MASK	0x40381EF8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT61_INTR_MASKED	0x40381EFC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT62_CTRL	0x40381F00	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT62_STATUS	0x40381F04	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT62_COUNTER	0x40381F08	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT62_CC0	0x40381F10	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT62_CC0_BUFF	0x40381F14	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT62_CC1	0x40381F18	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT62_CC1_BUFF	0x40381F1C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT62_PERIOD	0x40381F20	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT62_PERIOD_BUFF	0x40381F24	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT62_DT	0x40381F30	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT62_TR_CMD	0x40381F40	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT62_TR_IN_SEL0	0x40381F44	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT62_TR_IN_SEL1	0x40381F48	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT62_TR_IN_EDGE_SEL	0x40381F4C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT62_TR_PWM_CTRL	0x40381F50	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT62_TR_OUT_SEL	0x40381F54	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT62_INTR	0x40381F70	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP0_CNT62_INTR_SET	0x40381F74	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT62_INTR_MASK	0x40381F78	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT62_INTR_MASKED	0x40381F7C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT0_CTRL	0x40388000	Counter control register
TCPWM0_GRP1_CNT0_STATUS	0x40388004	Counter status register
TCPWM0_GRP1_CNT0_COUNTER	0x40388008	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT0_CC0	0x40388010	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT0_CC0_BUFF	0x40388014	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT0_CC1	0x40388018	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT0_CC1_BUFF	0x4038801C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT0_PERIOD	0x40388020	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT0_PERIOD_BUFF	0x40388024	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT0_LINE_SEL	0x40388028	Counter line selection register
TCPWM0_GRP1_CNT0_LINE_SEL_BUFF	0x4038802C	Counter buffered line selection register
TCPWM0_GRP1_CNT0_DT	0x40388030	Counter PWM dead time register
TCPWM0_GRP1_CNT0_TR_CMD	0x40388040	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT0_TR_IN_SEL0	0x40388044	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT0_TR_IN_SEL1	0x40388048	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL	0x4038804C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT0_TR_PWM_CTRL	0x40388050	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT0_TR_OUT_SEL	0x40388054	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT0_INTR	0x40388070	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT0_INTR_SET	0x40388074	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT0_INTR_MASK	0x40388078	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT0_INTR_MASKED	0x4038807C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT1_CTRL	0x40388080	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT1_STATUS	0x40388084	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT1_COUNTER	0x40388088	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT1_CC0	0x40388090	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT1_CC0_BUFF	0x40388094	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT1_CC1	0x40388098	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT1_CC1_BUFF	0x4038809C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT1_PERIOD	0x403880A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT1_PERIOD_BUFF	0x403880A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT1_LINE_SEL	0x403880A8	Counter line selection register. See TCPWM0_GRP1_CNT0_LINE_SEL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT1_LINE_SEL_BUFF	0x403880AC	Counter buffered line selection register. See TCPWM0_GRP1_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT1_DT	0x403880B0	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT1_TR_CMD	0x403880C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT1_TR_IN_SEL0	0x403880C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT1_TR_IN_SEL1	0x403880C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT1_TR_IN_EDGE_SEL	0x403880CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT1_TR_PWM_CTRL	0x403880D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT1_TR_OUT_SEL	0x403880D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT1_INTR	0x403880F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT1_INTR_SET	0x403880F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT1_INTR_MASK	0x403880F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT1_INTR_MASKED	0x403880FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT2_CTRL	0x40388100	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT2_STATUS	0x40388104	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT2_COUNTER	0x40388108	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT2_CC0	0x40388110	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT2_CC0_BUFF	0x40388114	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT2_CC1	0x40388118	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT2_CC1_BUFF	0x4038811C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT2_PERIOD	0x40388120	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT2_PERIOD_BUFF	0x40388124	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT2_LINE_SEL	0x40388128	Counter line selection register. See TCPWM0_GRP1_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT2_LINE_SEL_BUFF	0x4038812C	Counter buffered line selection register. See TCPWM0_GRP1_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT2_DT	0x40388130	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT2_TR_CMD	0x40388140	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT2_TR_IN_SEL0	0x40388144	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT2_TR_IN_SEL1	0x40388148	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT2_TR_IN_EDGE_SEL	0x4038814C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT2_TR_PWM_CTRL	0x40388150	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT2_TR_OUT_SEL	0x40388154	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT2_INTR	0x40388170	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT2_INTR_SET	0x40388174	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT2_INTR_MASK	0x40388178	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT2_INTR_MASKED	0x4038817C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT3_CTRL	0x40388180	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT3_STATUS	0x40388184	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT3_COUNTER	0x40388188	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT3_CC0	0x40388190	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT3_CC0_BUFF	0x40388194	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT3_CC1	0x40388198	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT3_CC1_BUFF	0x4038819C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT3_PERIOD	0x403881A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT3_PERIOD_BUFF	0x403881A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT3_LINE_SEL	0x403881A8	Counter line selection register. See TCPWM0_GRP1_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT3_LINE_SEL_BUFF	0x403881AC	Counter buffered line selection register. See TCPWM0_GRP1_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT3_DT	0x403881B0	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT3_TR_CMD	0x403881C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT3_TR_IN_SEL0	0x403881C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT3_TR_IN_SEL1	0x403881C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT3_TR_IN_EDGE_SEL	0x403881CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT3_TR_PWM_CTRL	0x403881D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT3_TR_OUT_SEL	0x403881D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT3_INTR	0x403881F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT3_INTR_SET	0x403881F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT3_INTR_MASK	0x403881F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT3_INTR_MASKED	0x403881FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT4_CTRL	0x40388200	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT4_STATUS	0x40388204	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT4_COUNTER	0x40388208	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT4_CC0	0x40388210	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT4_CC0_BUFF	0x40388214	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT4_CC1	0x40388218	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT4_CC1_BUFF	0x4038821C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT4_PERIOD	0x40388220	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT4_PERIOD_BUFF	0x40388224	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT4_LINE_SEL	0x40388228	Counter line selection register. See TCPWM0_GRP1_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT4_LINE_SEL_BUFF	0x4038822C	Counter buffered line selection register. See TCPWM0_GRP1_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT4_DT	0x40388230	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT4_TR_CMD	0x40388240	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT4_TR_IN_SEL0	0x40388244	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT4_TR_IN_SEL1	0x40388248	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT4_TR_IN_EDGE_SEL	0x4038824C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT4_TR_PWM_CTRL	0x40388250	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT4_TR_OUT_SEL	0x40388254	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT4_INTR	0x40388270	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT4_INTR_SET	0x40388274	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT4_INTR_MASK	0x40388278	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT4_INTR_MASKED	0x4038827C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT5_CTRL	0x40388280	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT5_STATUS	0x40388284	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT5_COUNTER	0x40388288	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT5_CC0	0x40388290	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT5_CC0_BUFF	0x40388294	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT5_CC1	0x40388298	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT5_CC1_BUFF	0x4038829C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT5_PERIOD	0x403882A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT5_PERIOD_BUFF	0x403882A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT5_LINE_SEL	0x403882A8	Counter line selection register. See TCPWM0_GRP1_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT5_LINE_SEL_BUFF	0x403882AC	Counter buffered line selection register. See TCPWM0_GRP1_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT5_DT	0x403882B0	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT5_TR_CMD	0x403882C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT5_TR_IN_SEL0	0x403882C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT5_TR_IN_SEL1	0x403882C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT5_TR_IN_EDGE_SEL	0x403882CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT5_TR_PWM_CTRL	0x403882D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT5_TR_OUT_SEL	0x403882D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT5_INTR	0x403882F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT5_INTR_SET	0x403882F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT5_INTR_MASK	0x403882F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT5_INTR_MASKED	0x403882FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT6_CTRL	0x40388300	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT6_STATUS	0x40388304	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT6_COUNTER	0x40388308	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT6_CC0	0x40388310	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT6_CC0_BUFF	0x40388314	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT6_CC1	0x40388318	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT6_CC1_BUFF	0x4038831C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT6_PERIOD	0x40388320	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT6_PERIOD_BUFF	0x40388324	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT6_LINE_SEL	0x40388328	Counter line selection register. See TCPWM0_GRP1_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT6_LINE_SEL_BUFF	0x4038832C	Counter buffered line selection register. See TCPWM0_GRP1_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT6_DT	0x40388330	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT6_TR_CMD	0x40388340	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT6_TR_IN_SEL0	0x40388344	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT6_TR_IN_SEL1	0x40388348	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT6_TR_IN_EDGE_SEL	0x4038834C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT6_TR_PWM_CTRL	0x40388350	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT6_TR_OUT_SEL	0x40388354	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT6_INTR	0x40388370	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT6_INTR_SET	0x40388374	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT6_INTR_MASK	0x40388378	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT6_INTR_MASKED	0x4038837C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT7_CTRL	0x40388380	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT7_STATUS	0x40388384	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT7_COUNTER	0x40388388	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT7_CC0	0x40388390	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT7_CC0_BUFF	0x40388394	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT7_CC1	0x40388398	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT7_CC1_BUFF	0x4038839C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT7_PERIOD	0x403883A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT7_PERIOD_BUFF	0x403883A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT7_LINE_SEL	0x403883A8	Counter line selection register. See TCPWM0_GRP1_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT7_LINE_SEL_BUFF	0x403883AC	Counter buffered line selection register. See TCPWM0_GRP1_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT7_DT	0x403883B0	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT7_TR_CMD	0x403883C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT7_TR_IN_SEL0	0x403883C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT7_TR_IN_SEL1	0x403883C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT7_TR_IN_EDGE_SEL	0x403883CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT7_TR_PWM_CTRL	0x403883D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT7_TR_OUT_SEL	0x403883D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT7_INTR	0x403883F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT7_INTR_SET	0x403883F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT7_INTR_MASK	0x403883F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT7_INTR_MASKED	0x403883FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT8_CTRL	0x40388400	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT8_STATUS	0x40388404	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT8_COUNTER	0x40388408	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT8_CC0	0x40388410	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT8_CC0_BUFF	0x40388414	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT8_CC1	0x40388418	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT8_CC1_BUFF	0x4038841C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT8_PERIOD	0x40388420	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT8_PERIOD_BUFF	0x40388424	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT8_LINE_SEL	0x40388428	Counter line selection register. See TCPWM0_GRP1_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT8_LINE_SEL_BUFF	0x4038842C	Counter buffered line selection register. See TCPWM0_GRP1_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT8_DT	0x40388430	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT8_TR_CMD	0x40388440	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT8_TR_IN_SEL0	0x40388444	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT8_TR_IN_SEL1	0x40388448	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT8_TR_IN_EDGE_SEL	0x4038844C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT8_TR_PWM_CTRL	0x40388450	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT8_TR_OUT_SEL	0x40388454	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT8_INTR	0x40388470	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT8_INTR_SET	0x40388474	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT8_INTR_MASK	0x40388478	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT8_INTR_MASKED	0x4038847C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT9_CTRL	0x40388480	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT9_STATUS	0x40388484	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT9_COUNTER	0x40388488	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT9_CC0	0x40388490	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT9_CC0_BUFF	0x40388494	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT9_CC1	0x40388498	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT9_CC1_BUFF	0x4038849C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT9_PERIOD	0x403884A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT9_PERIOD_BUFF	0x403884A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT9_LINE_SEL	0x403884A8	Counter line selection register. See TCPWM0_GRP1_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT9_LINE_SEL_BUFF	0x403884AC	Counter buffered line selection register. See TCPWM0_GRP1_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT9_DT	0x403884B0	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT9_TR_CMD	0x403884C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT9_TR_IN_SEL0	0x403884C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT9_TR_IN_SEL1	0x403884C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT9_TR_IN_EDGE_SEL	0x403884CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT9_TR_PWM_CTRL	0x403884D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT9_TR_OUT_SEL	0x403884D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT9_INTR	0x403884F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT9_INTR_SET	0x403884F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT9_INTR_MASK	0x403884F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT9_INTR_MASKED	0x403884FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT10_CTRL	0x40388500	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT10_STATUS	0x40388504	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT10_COUNTER	0x40388508	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT10_CC0	0x40388510	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT10_CC0_BUFF	0x40388514	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT10_CC1	0x40388518	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT10_CC1_BUFF	0x4038851C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT10_PERIOD	0x40388520	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT10_PERIOD_BUFF	0x40388524	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT10_LINE_SEL	0x40388528	Counter line selection register. See TCPWM0_GRP1_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT10_LINE_SEL_BUFF	0x4038852C	Counter buffered line selection register. See TCPWM0_GRP1_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT10_DT	0x40388530	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT10_TR_CMD	0x40388540	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT10_TR_IN_SEL0	0x40388544	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT10_TR_IN_SEL1	0x40388548	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT10_TR_IN_EDGE_SEL	0x4038854C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT10_TR_PWM_CTRL	0x40388550	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT10_TR_OUT_SEL	0x40388554	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT10_INTR	0x40388570	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT10_INTR_SET	0x40388574	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT10_INTR_MASK	0x40388578	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT10_INTR_MASKED	0x4038857C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT11_CTRL	0x40388580	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT11_STATUS	0x40388584	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT11_COUNTER	0x40388588	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT11_CC0	0x40388590	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT11_CC0_BUFF	0x40388594	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT11_CC1	0x40388598	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT11_CC1_BUFF	0x4038859C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT11_PERIOD	0x403885A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT11_PERIOD_BUFF	0x403885A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT11_LINE_SEL	0x403885A8	Counter line selection register. See TCPWM0_GRP1_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT11_LINE_SEL_BUFF	0x403885AC	Counter buffered line selection register. See TCPWM0_GRP1_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT11_DT	0x403885B0	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT11_TR_CMD	0x403885C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT11_TR_IN_SEL0	0x403885C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT11_TR_IN_SEL1	0x403885C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT11_TR_IN_EDGE_SEL	0x403885CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT11_TR_PWM_CTRL	0x403885D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT11_TR_OUT_SEL	0x403885D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT11_INTR	0x403885F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT11_INTR_SET	0x403885F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP1_CNT11_INTR_MASK	0x403885F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT11_INTR_MASKED	0x403885FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP2_CNT0_CTRL	0x40390000	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP2_CNT0_STATUS	0x40390004	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP2_CNT0_COUNTER	0x40390008	Counter count register
TCPWM0_GRP2_CNT0_CC0	0x40390010	Counter compare/capture 0 register
TCPWM0_GRP2_CNT0_CC0_BUFF	0x40390014	Counter buffered compare/capture 0 register
TCPWM0_GRP2_CNT0_CC1	0x40390018	Counter compare/capture 1 register
TCPWM0_GRP2_CNT0_CC1_BUFF	0x4039001C	Counter buffered compare/capture 1 register
TCPWM0_GRP2_CNT0_PERIOD	0x40390020	Counter period register
TCPWM0_GRP2_CNT0_PERIOD_BUFF	0x40390024	Counter buffered period register
TCPWM0_GRP2_CNT0_DT	0x40390030	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP2_CNT0_TR_CMD	0x40390040	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP2_CNT0_TR_IN_SEL0	0x40390044	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP2_CNT0_TR_IN_SEL1	0x40390048	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP2_CNT0_TR_IN_EDGE_SEL	0x4039004C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP2_CNT0_TR_PWM_CTRL	0x40390050	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP2_CNT0_TR_OUT_SEL	0x40390054	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP2_CNT0_INTR	0x40390070	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP2_CNT0_INTR_SET	0x40390074	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP2_CNT0_INTR_MASK	0x40390078	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP2_CNT0_INTR_MASKED	0x4039007C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP2_CNT1_CTRL	0x40390080	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP2_CNT1_STATUS	0x40390084	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP2_CNT1_COUNTER	0x40390088	Counter count register. See TCPWM0_GRP2_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP2_CNT1_CC0	0x40390090	Counter compare/capture 0 register. See TCPWM0_GRP2_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP2_CNT1_CC0_BUFF	0x40390094	Counter buffered compare/capture 0 register. See TCPWM0_GRP2_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT1_CC1	0x40390098	Counter compare/capture 1 register. See TCPWM0_GRP2_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP2_CNT1_CC1_BUFF	0x4039009C	Counter buffered compare/capture 1 register. See TCPWM0_GRP2_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT1_PERIOD	0x403900A0	Counter period register. See TCPWM0_GRP2_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP2_CNT1_PERIOD_BUFF	0x403900A4	Counter buffered period register. See TCPWM0_GRP2_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT1_DT	0x403900B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP2_CNT1_TR_CMD	0x403900C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP2_CNT1_TR_IN_SEL0	0x403900C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP2_CNT1_TR_IN_SEL1	0x403900C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP2_CNT1_TR_IN_EDGE_SEL	0x403900CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP2_CNT1_TR_PWM_CTRL	0x403900D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP2_CNT1_TR_OUT_SEL	0x403900D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP2_CNT1_INTR	0x403900F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP2_CNT1_INTR_SET	0x403900F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP2_CNT1_INTR_MASK	0x403900F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP2_CNT1_INTR_MASKED	0x403900FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP2_CNT2_CTRL	0x40390100	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP2_CNT2_STATUS	0x40390104	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP2_CNT2_COUNTER	0x40390108	Counter count register. See TCPWM0_GRP2_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP2_CNT2_CC0	0x40390110	Counter compare/capture 0 register. See TCPWM0_GRP2_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP2_CNT2_CC0_BUFF	0x40390114	Counter buffered compare/capture 0 register. See TCPWM0_GRP2_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT2_CC1	0x40390118	Counter compare/capture 1 register. See TCPWM0_GRP2_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP2_CNT2_CC1_BUFF	0x4039011C	Counter buffered compare/capture 1 register. See TCPWM0_GRP2_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT2_PERIOD	0x40390120	Counter period register. See TCPWM0_GRP2_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP2_CNT2_PERIOD_BUFF	0x40390124	Counter buffered period register. See TCPWM0_GRP2_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT2_DT	0x40390130	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP2_CNT2_TR_CMD	0x40390140	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP2_CNT2_TR_IN_SEL0	0x40390144	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP2_CNT2_TR_IN_SEL1	0x40390148	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP2_CNT2_TR_IN_EDGE_SEL	0x4039014C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP2_CNT2_TR_PWM_CTRL	0x40390150	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP2_CNT2_TR_OUT_SEL	0x40390154	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP2_CNT2_INTR	0x40390170	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP2_CNT2_INTR_SET	0x40390174	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP2_CNT2_INTR_MASK	0x40390178	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP2_CNT2_INTR_MASKED	0x4039017C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP2_CNT3_CTRL	0x40390180	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP2_CNT3_STATUS	0x40390184	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP2_CNT3_COUNTER	0x40390188	Counter count register. See TCPWM0_GRP2_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP2_CNT3_CC0	0x40390190	Counter compare/capture 0 register. See TCPWM0_GRP2_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP2_CNT3_CC0_BUFF	0x40390194	Counter buffered compare/capture 0 register. See TCPWM0_GRP2_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT3_CC1	0x40390198	Counter compare/capture 1 register. See TCPWM0_GRP2_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP2_CNT3_CC1_BUFF	0x4039019C	Counter buffered compare/capture 1 register. See TCPWM0_GRP2_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT3_PERIOD	0x403901A0	Counter period register. See TCPWM0_GRP2_CNT0_PERIOD for the details of bit fields.

Register name	Address	Description
TCPWM0_GRP2_CNT3_PERIOD_BUFF	0x403901A4	Counter buffered period register. See TCPWM0_GRP2_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT3_DT	0x403901B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP2_CNT3_TR_CMD	0x403901C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP2_CNT3_TR_IN_SEL0	0x403901C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP2_CNT3_TR_IN_SEL1	0x403901C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP2_CNT3_TR_IN_EDGE_SEL	0x403901CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP2_CNT3_TR_PWM_CTRL	0x403901D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP2_CNT3_TR_OUT_SEL	0x403901D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP2_CNT3_INTR	0x403901F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP2_CNT3_INTR_SET	0x403901F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP2_CNT3_INTR_MASK	0x403901F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP2_CNT3_INTR_MASKED	0x403901FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.

14.1 TCPWM registers

TCPWM0_GRP0_CNT0_CTRL

Counter control register
Address: 0x40380000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R

Bits	7	6	5	4	3	2	1	0
Name	None [7:3]					AUTO_RELOAD_PERIOD	AUTO_RELOAD_CC1	AUTO_RELOAD_CC0
Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		PWM_DISABLE_MODE [13:12]		None	PWM_SYNC_KILL	PWM_STOP_ON_KILL	PWM_IMM_KILL
Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUAD_ENCODING_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	
Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	RW	RW	None			RW		
HW Access	R	R	None			R		
Name	ENABLED	DBG_FREEZE_EN	None [29:27]			MODE [26:24]		

Bits	Name	Description
31	ENABLED	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). Default Value: 0

30	DBG_FREEZE_EN	Specifies the counter behavior in debug mode. '0': The counter operation continues in debug mode. '1': The counter operation freezes in debug mode. Default Value: 0
26 : 24	MODE	Counter mode. Default Value: 0
		0x0: TIMER : Timer mode
		0x1: Reserved1 : N/A
		0x2: CAPTURE : Capture mode
		0x3: QUAD : Quadrature mode Different encoding modes can be selected by QUAD_ENCODING_MODE including up/down count functionality. Different counter range, reload value and capture behavior can be selected by QUAD_RANGE_MODE (overloaded field UP_DOWN_MODE).
		0x4: PWM : Pulse width modulation (PWM) mode
		0x5: PWM_DT : PWM with deadtime insertion mode
		0x6: PWM_PR : Pseudo random pulse width modulation
		0x7: SR : Shift register mode.
21 : 20	QUAD_ENCODING_MODE	In QUAD mode this field selects the quadrature encoding mode (X1/X2/X4) or the Up / Down rotary counting mode. In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUAD_ENCODING_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUAD_ENCODING_MODE[1]. Default Value: 0
		0x0: X1 : X1 encoding (QUAD mode) This encoding is identical with an up / down counting functionality of the following way: Rising edges of input phiA increment or decrement the counter depending on the state of input phiB (direction input).

		0x1: X2 : X2 encoding (QUAD mode)
		0x2: X4 : X4 encoding (QUAD mode)
		0x3: UP_DOWN : Up / Down rotary counting mode. Input phiA increments the counter, input phiB decrements the counter. The trigger edge detection settings apply.
		0x1: INV_OUT : When bit 0 is '1', QUADRATURE_ENCODING_MODE[0] inverts "dt_line_out" (PWM/ PWM_DT modes)
		0x2: INV_COMPL_OUT : When bit 1 is '1', QUADRATURE_ENCODING_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. In QUAD mode this field acts as QUAD_RANGE_MODE field selecting between different counter range, reload value and compare / capture behavior. Default Value: 0
		0x0: COUNT_UP : Count up (to PERIOD). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. A terminal count event is generated when the counter changes from a state in which COUNTER equals PERIOD.
		0x1: COUNT_DOWN : Count down (to "0"). An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0".

		0x2: COUNT_UPDN1 : Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0".
		0x3: COUNT_UPDN2 : Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0" AND when the counter changes from a state in which COUNTER equals PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
		0x0: QUAD_RANGE0 : In QUAD mode this setting selects the QUAD_RANGE0 mode with the following behavior: - COUNTER range is between 0x0000 and 0xFFFF / 0xFFFFFFFF (for GRP_CNT_WIDTH = 16 / 32) - on reload / index event: - CC0 is copied to CC0_BUFF - COUNTER is copied to CC0 - COUNTER is set to midpoint (0x8000 / 0x80000000) - tc and cc0_match events are generated - when COUNTER is 0x0000 or 0xFFFF / 0xFFFFFFFF: - CC0 is copied to CC0_BUFF - COUNTER (0x0000 or 0xFFFF / 0xFFFFFFFF) is copied to CC0 - COUNTER is set to midpoint (0x8000 / 0x80000000) - cc0_match event is generated

		0x1: QUAD_RANGE0_CMP : In QUAD mode this setting selects the QUAD_RANGE0_CMP mode with the following behavior: - COUNTER range is between 0x0000 and 0xFFFF / 0xFFFFFFFF (for GRP_CNT_WIDTH = 16 / 32) - the capture0 event acts as 2nd reload / index event - on reload / index event: - COUNTER is set to midpoint (0x8000 / 0x80000000) - when 'capture on index' is selected (AUTO_RELOAD_PERIOD=0): - tc event is generated - PERIOD is copied to PERIOD_BUFF - COUNTER is copied to PERIOD - when COUNTER is 0x0000 or 0xFFFF / 0xFFFFFFFF: - COUNTER is set to midpoint (0x8000 / 0x80000000) - when 'capture on wrap-around' is selected (AUTO_RELOAD_PERIOD=1): - tc event is generated - PERIOD is copied to PERIOD_BUFF - COUNTER (0x0000 or 0xFFFF / 0xFFFFFFFF) is copied to PERIOD - 1 or 2 compare functions (depending on CC1_PRESENT) available This mode is to a certain extend backward compatible with previous TCPWM quadrature behavior but allows a compare function during quadrature decoding using the CC0/CC_BUFF registers and the cc0_match event. Because of that the PERIOD/PERIOD_BUFF registers are used instead of CC0/CC_BUFF registers to capture COUNTER at reload / index event or wrap-around.

		0x2: QUAD_RANGE1_CAPT : In QUAD mode this setting selects the QUAD_RANGE1_CAPT mode with the following behavior: - COUNTER range is between 0x0000 and PERIOD - on reload / index event: - COUNTER is set to 0x0000 - tc event is generated - when COUNTER is 0x0000 and decrementing: - COUNTER is set to PERIOD - tc event is generated - when COUNTER equals PERIOD and is incrementing: - COUNTER is set to 0x0000 - tc event is generated - 1 or 2 capture functions (depending on CC1_PRESENT) available - on capture0 / capture1 event: - CC0 / CC1 is copied to CC0_BUFF / CC1_BUFF - COUNTER value is copied to CC0 It allows that the COUNTER register reflects the current angle position of the rotary encoder, i.e. no MOD or SUB calculations need to be done in SW on the COUNTER value to get the current angle position. This allows a DMA copy of the angle position from the COUNTER register. However, a disadvantage of this mode is that fast sequences of tc interrupts can occur (when encoder moves back and forth around start position). It is recommended to not use the tc interrupt in this mode.
		0x3: QUAD_RANGE1_CMP : In QUAD mode this setting selects the QUAD_RANGE1_CMP mode. The behavior is the same as for QUAD_RANGE1_CAPT mode described above with the only difference that 1 or 2 compare functions (depending on CC1_PRESENT) are available instead of 1 or 2 capture functions.
13 : 12	PWM_DISABLE_MODE	Specifies the behavior of the PWM outputs "line_out" and "line_compl_out" while the TCPWM counter is disabled (CTL.ENABLED='0') or stopped. Note: The output signal of this selection can be further modified by the immediate kill logic and line_out polarity settings (CTRL.QUAD_ENCODING_MODE). Default Value: 0

		0x0: Z : When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are NOT driven by the TCPWM. Instead the port default level configuration applies, e.g. "Z" (high impedance). Note: This is realized by driving the TCPWM output "line_out_en" to 0. When the counter is stopped upon a stop event the PWM outputs are deactivated (to the polarity defined by CTL.QUAD_ENCODING_MODE).
		0x1: RETAIN : When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are driven by the TCPWM. When the counter is disabled or stopped upon a stop event the PWM outputs are retained (keep their previous levels). While the counter is disabled or stopped the PWM outputs can be changed via LINE_SEL (when parameter GRP_SMC_PRESENT = 1).
		0x2: L : When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are driven by the TCPWM. When the counter is disabled or stopped upon a stop event the PWM output "line_out" is driven as a fixed '0' and the PWM output "line_compl_out" is driven as a fixed '1'.
		0x3: H : When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are driven by the TCPWM. When the counter is disabled or stopped upon a stop event the PWM output "line_out" is driven as a fixed '1' and the PWM output "line_compl_out" is driven as a fixed '0'.

10	PWM_SYNC_KILL	Specifies asynchronous/ synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
9	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
8	PWM_IMM_KILL	Specifies whether the kill event immediately deactivates the "dt_line_out" and "dt_line_compl_out" signals or with the next module clock ("active count" pre-scaled "clk_counter"). '0': synchronous kill activation. Deactivates the "dt_line_out" and "dt_line_compl_out" signals with the next module clock ("active count" pre-scaled "clk_counter"). '1': immediate kill activation. Immediately deactivates the "dt_line_out" and "dt_line_compl_out" signals. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0

2	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff. Default Value: 0
1	AUTO_RELOAD_CC1	Specifies switching of the CC1 and buffered CC1 values. This field has a function in TIMER, QUAD (QUAD_RANGE0_CMP, QUAD_RANGE1_CMP range modes), SR, PWM, PWM_DT and PWM_PR modes. Timer, QUAD, SR modes: '0': never switch. '1': switch on a compare match 1 event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0
0	AUTO_RELOAD_CC0	Specifies switching of the CC0 and buffered CC0 values. This field has a function in TIMER, QUAD (QUAD_RANGE0_CMP, QUAD_RANGE1_CMP range modes), SR, PWM, PWM_DT and PWM_PR modes. Timer, QUAD, SR modes: '0': never switch. '1': switch on a compare match 0 event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

TCPWM0_GRP0_CNT0_STATUS

Counter status register
Address: 0x40380004
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None			R
HW Access	RW	RW	RW	RW	None			RW
Name	TR_STOP	TR_RELOAD	TR_COUNT	TR_CAPTURE0	None [3:1]			DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R	None			R	R	R	R
HW Access	RW	None			RW	RW	RW	RW
Name	RUNNING	None [14:12]			LINE_COMPL_OUT	LINE_OUT	TR_CAPTURE1	TR_START

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DT_CNT_L [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	DT_CNT_L	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion (8bit dead time counter or low byte of 16-bit dead time counter). In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
15	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. This field is used to indicate that the counter is running after a start/reload event and that the counter is stopped after a stop event. When a running counter operation is paused in debug state (see CTRL.DBG_PAUSE) then the RUNNING bit is still '1'. Default Value: 0

11	LINE_COMPL_OUT	Indicates the actual level of the complementary PWM line output signal. Default Value: 0
10	LINE_OUT	Indicates the actual level of the PWM line output signal. Default Value: 0
9	TR_CAPTURE1	Indicates the actual level of the selected capture 1 trigger. Default Value: 0
8	TR_START	Indicates the actual level of the selected start trigger. Default Value: 0
7	TR_STOP	Indicates the actual level of the selected stop trigger. Default Value: 0
6	TR_RELOAD	Indicates the actual level of the selected reload trigger. Default Value: 0
5	TR_COUNT	Indicates the actual level of the selected count trigger. Default Value: 1
4	TR_CAPTURE0	Indicates the actual level of the selected capture 0 trigger. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

TCPWM0_GRP0_CNT0_COUNTER

Counter count register
Address: 0x40380008
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit / 32-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

TCPWM0_GRP0_CNT0_CC0

Counter compare/capture 0 register
Address: 0x40380010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

TCPWM0_GRP0_CNT0_CC0_BUFF

Counter buffered compare/capture 0 register
Address: 0x40380014
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

TCPWM0_GRP0_CNT0_CC1

Counter compare/capture 1 register
Address: 0x40380018
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

TCPWM0_GRP0_CNT0_CC1_BUFF

Counter buffered compare/capture 1 register
Address: 0x4038001C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC1 register. Default Value: 65535

TCPWM0_GRP0_CNT0_PERIOD

Counter period register
Address: 0x40380020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

TCPWM0_GRP0_CNT0_PERIOD_BUFF

Counter buffered period register
Address: 0x40380024
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

15 : 0	PERIOD	Additional buffer for counter PERIOD register. In PWM_PR mode PEROD_BUFF defines the LFSR polynomial. Each bit represents a tap of the shift register which can be feed back to the MSB via an XOR tree. Examples for GRP_CNT_WIDTH = 16: - Maximum length 16bit LFSR - polynomial x^16 + x^14 + x^13 + x^11 + 1 - taps 0,2,3,5 -> PERIOD = 0x002d - period is 2^16-1 = 65535 cycles - Maximum length 8bit LFSR: - polynomial x^8 + x^6 + x^5 + x^4 + 1 - taps 8,10,11,12 (realized in 8 MSBs of 16bit LFSR) - period is 2^8-1 = 255 cycles In SR mode PERIOD_BUFF defines which tap of the shift register generates the PWM output signals. For a delay of n cycles (from capture event to PWM output) the bit CNT_WIDTH-n should be set to '1'. For a shift register function only one tap should be use, i.e. a one-hot value must be written to PERIOD_BUFF. If multiple bits in PERIOD_BUFF are set then the taps are XOR combined. Default Value: 65535

TCPWM0_GRP0_CNT0_DT

Counter PWM dead time register
Address: 0x40380030
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DT_LINE_OUT_L [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DT_LINE_OUT_L	In PWM_DT mode, this field is used to determine the low byte of the dead time before activating the PWM line output signal "line_out": amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Note: This field determines the low byte of the 16-bit dead time before activating "line_out" when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8 bit wide and the same dead time specified by this DT_LINE_OUT_L field is used before activating "line_out" and "line_compl_out". Default Value: 0
		0x0: DIVBY1 : Divide by 1 (other-than-PWM_DT mode)
		0x1: DIVBY2 : Divide by 2 (other-than-PWM_DT mode)

		0x2: DIVBY4 : Divide by 4 (other-than-PWM_DT mode)
		0x3: DIVBY8 : Divide by 8 (other-than-PWM_DT mode)
		0x4: DIVBY16 : Divide by 16 (other-than-PWM_DT mode)
		0x5: DIVBY32 : Divide by 32 (other-than-PWM_DT mode)
		0x6: DIVBY64 : Divide by 64 (other-than-PWM_DT mode)
		0x7: DIVBY128 : Divide by 128 (other-than-PWM_DT mode)

TCPWM0_GRP0_CNT0_TR_CMD

Counter trigger command register
Address: 0x40380040
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1S	RW1S	RW1S	RW1S	None	RW1S
HW Access	None		RW1C	RW1C	RW1C	RW1C	None	RW1C
Name	None [7:6]		CAPTURE1	START	STOP	RELOAD	None	CAPTURE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	CAPTURE1	SW capture 1 trigger. For HW behavior, see COUNTER_CAPTURE0 field. Default Value: 0
4	START	SW start trigger. For HW behavior, see COUNTER_CAPTURE0 field. Default Value: 0
3	STOP	SW stop trigger. For HW behavior, see COUNTER_CAPTURE0 field. Default Value: 0
2	RELOAD	SW reload trigger. For HW behavior, see COUNTER_CAPTURE0 field. Default Value: 0
0	CAPTURE0	SW capture 0 trigger. When written with '1', a capture 0 trigger is generated and the HW sets the field to '0' when the SW trigger has taken effect. It should be noted that the HW operates on the counter frequency. If the counter is disabled through CTRL.ENABLED, the field is immediately set to '0'. Default Value: 0

TCPWM0_GRP0_CNT0_TR_IN_SEL0

Counter input trigger selection register 0
Address: 0x40380044
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			CAPTURE0_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			COUNT_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			RELOAD_SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			R				
Name	None [31:29]			STOP_SEL [28:24]				

Bits	Name	Description
28 : 24	STOP_SEL	Selects one of the 256 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0

20 : 16	RELOAD_SEL	Selects one of the 256 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In these modes, it will update the counter with 0x8000 (counter midpoint) or 0x0000 depending on the QUAD_RANGE_MODE. Default Value: 0
12 : 8	COUNT_SEL	Selects one of the 256 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Note: In the modes: TIMER, CAPTURE, PWM, PWM_DT, and SR, If the counter is externally triggered (COUNT_SEL > 1), an external trigger will be required for each TR_CMD to execute. For example, a write to TR_CMD.START will not start the counter until the trigger selected by COUNT_SEL asserts. The next trigger will increment the counter since the counter is now running. This goes for all TR_CMD fields. Default Value: 1
4 : 0	CAPTURE0_SEL	Selects one of the up to 256 input triggers as a capture0 trigger. Input trigger 0 is always '0' and input trigger 1 is always '1'. If existing, the one-to-one trigger inputs "tr_one_cnt_in" (different to each counter) are selected by setting 2 and above. The settings above are used for the general purpose trigger inputs "tr_all_cnt_in" connected to all counters selected. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

TCPWM0_GRP0_CNT0_TR_IN_SEL1

Counter input trigger selection register 1
Address: 0x40380048
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			START_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			CAPTURE1_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12 : 8	CAPTURE1_SEL	Selects one of the 256 input triggers as a capture 1 trigger. Default Value: 0
4 : 0	START_SEL	Selects one of the 256 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0

TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL

Counter input trigger edge selection register
Address: 0x4038004C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE0_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [15:12]				CAPTURE1_EDGE [11:10]		START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 10	CAPTURE1_EDGE	A capture 1 event will copy the counter value into the CC1 register. Default Value: 3
		0x0: RISING_EDGE : Rising edge. Any rising edge generates an event.
		0x1: FALLING_EDGE : Falling edge. Any falling edge generates an event.
		0x2: ANY_EDGE : Rising AND falling edge. Any odd amount of edges generates an event.
		0x3: NO_EDGE_DET : No edge detection, use trigger as is.
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3
		0x0: RISING_EDGE : Rising edge. Any rising edge generates an event.

		0x1: FALLING_EDGE : Falling edge. Any falling edge generates an event.
		0x2: ANY_EDGE : Rising AND falling edge. Any odd amount of edges generates an event.
		0x3: NO_EDGE_DET : No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3
		0x0: RISING_EDGE : Rising edge. Any rising edge generates an event.
		0x1: FALLING_EDGE : Falling edge. Any falling edge generates an event.
		0x2: ANY_EDGE : Rising AND falling edge. Any odd amount of edges generates an event.
		0x3: NO_EDGE_DET : No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3
		0x0: RISING_EDGE : Rising edge. Any rising edge generates an event.
		0x1: FALLING_EDGE : Falling edge. Any falling edge generates an event.
		0x2: ANY_EDGE : Rising AND falling edge. Any odd amount of edges generates an event.
		0x3: NO_EDGE_DET : No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3
		0x0: RISING_EDGE : Rising edge. Any rising edge generates an event.
		0x1: FALLING_EDGE : Falling edge. Any falling edge generates an event.
		0x2: ANY_EDGE : Rising AND falling edge. Any odd amount of edges generates an event.

		0x3: NO_EDGE_DET : No edge detection, use trigger as is.
1 : 0	CAPTURE0_EDGE	A capture 0 event will copy the counter value into the CC0 register. Default Value: 3
		0x0: RISING_EDGE : Rising edge. Any rising edge generates an event.
		0x1: FALLING_EDGE : Falling edge. Any falling edge generates an event.
		0x2: ANY_EDGE : Rising AND falling edge. Any odd amount of edges generates an event.
		0x3: NO_EDGE_DET : No edge detection, use trigger as is.

TCPWM0_GRP0_CNT0_TR_PWM_CTRL

Counter trigger PWM control register
Address: 0x40380050
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CC1_MATCH_MODE [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC0_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	CC1_MATCH_MODE	Determines the effect of a compare match 1 event (COUNTER equals CC1 register) on the "line_out" output signals. Default Value: 3
		0x0: SET : Set to '1'
		0x1: CLEAR : Set to '0'
		0x2: INVERT : Invert
		0x3: NO_CHANGE : No Change
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3
		0x0: SET : Set to '1'
		0x1: CLEAR : Set to '0'
		0x2: INVERT : Invert
		0x3: NO_CHANGE : No Change

3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3
		0x0: SET : Set to '1'
		0x1: CLEAR : Set to '0'
		0x2: INVERT : Invert
		0x3: NO_CHANGE : No Change
1 : 0	CC0_MATCH_MODE	Determines the effect of a compare match 0 event (COUNTER equals CC0 register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC0 register should be set to "0". For a 100% duty cycle, the counter CC0 register should be set to larger than the counter PERIOD register. Default Value: 3
		0x0: SET : Set to '1'
		0x1: CLEAR : Set to '0'
		0x2: INVERT : Invert
		0x3: NO_CHANGE : No Change

TCPWM0_GRP0_CNT0_TR_OUT_SEL

Counter output trigger selection register
Address: 0x40380054
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	OUT1 [6:4]			None	OUT0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 4	OUT1	Selects one of the internal events to generate the output trigger 1. Default setting selects the compare match 0 event. Default Value: 3
		0x0: OVERFLOW : Overflow event
		0x1: UNDERFLOW : Underflow event
		0x2: TC : Terminal count event
		0x3: CC0_MATCH : Compare match 0 event (default selection)
		0x4: CC1_MATCH : Compare match 1 event
		0x5: LINE_OUT : PWM output signal "line_out"
		0x6: Reserved6 : This setting is reserved. Do not use.
		0x7: Disabled : Output trigger disabled.
2 : 0	OUT0	Selects one of the internal events to generate the output trigger 0. Default setting selects the terminal count event. Default Value: 2

		0x0: OVERFLOW : Overflow event
		0x1: UNDERFLOW : Underflow event
		0x2: TC : Terminal count event (default selection)
		0x3: CC0_MATCH : Compare match 0 event
		0x4: CC1_MATCH : Compare match 1 event
		0x5: LINE_OUT : PWM output signal "line_out"
		0x6: Reserved6 : This setting is reserved. Do not use.
		0x7: Disabled : Output trigger disabled.

TCPWM0_GRP0_CNT0_INTR

Interrupt request register
Address: 0x40380070
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [7:3]					CC1_MATCH	CC0_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CC1_MATCH	Counter matches CC1 register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
1	CC0_MATCH	Counter matches CC0 register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

TCPWM0_GRP0_CNT0_INTR_SET

Interrupt set request register
Address: 0x40380074
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [7:3]					CC1_MATCH	CC0_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CC1_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	CC0_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

TCPWM0_GRP0_CNT0_INTR_MASK

Interrupt mask register
Address: 0x40380078
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					CC1_MATCH	CC0_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CC1_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	CC0_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

TCPWM0_GRP0_CNT0_INTR_MASKED

Interrupt masked request register
Address: 0x4038007C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					CC1_MATCH	CC0_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CC1_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
1	CC0_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

TCPWM0_GRP1_CNT0_CTRL

Counter control register
Address: 0x40388000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	CC1_MATCH_DOWN_EN	CC1_MATCH_UP_EN	CC0_MATCH_DOWN_EN	CC0_MATCH_UP_EN	AUTO_RELOAD_LINE_SEL	AUTO_RELOAD_PERIOD	AUTO_RELOAD_CC1	AUTO_RELOAD_CC0

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		PWM_DISABLE_MODE [13:12]		None	PWM_SYNC_KILL	PWM_STOP_ON_KILL	PWM_IMM_KILL

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUAD_ENCODING_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None			RW		
HW Access	R	R	None			R		
Name	ENABLED	DBG_FREEZE_EN	None [29:27]			MODE [26:24]		

Bits	Name	Description

31	ENABLED	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). Default Value: 0
30	DBG_FREEZE_EN	Specifies the counter behavior in debug mode. '0': The counter operation continues in debug mode. '1': The counter operation freezes in debug mode. Default Value: 0
26 : 24	MODE	Counter mode. Default Value: 0
		0x0: TIMER : Timer mode
		0x1: Reserved1 : N/A
		0x2: CAPTURE : Capture mode
		0x3: QUAD : Quadrature mode Different encoding modes can be selected by QUAD_ENCODING_MODE including up/down count functionality. Different counter range, reload value and capture behavior can be selected by QUAD_RANGE_MODE (overloaded field UP_DOWN_MODE).
		0x4: PWM : Pulse width modulation (PWM) mode
		0x5: PWM_DT : PWM with deadtime insertion mode
		0x6: PWM_PR : Pseudo random pulse width modulation
		0x7: SR : Shift register mode.

21 : 20	QUAD_ENCODING_MODE	In QUAD mode this field selects the quadrature encoding mode (X1/X2/X4) or the Up / Down rotary counting mode. In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUAD_ENCODING_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUAD_ENCODING_MODE[1]. Default Value: 0
		0x0: X1 : X1 encoding (QUAD mode) This encoding is identical with an up / down counting functionality of the following way: Rising edges of input phiA increment or decrement the counter depending on the state of input phiB (direction input).
		0x1: X2 : X2 encoding (QUAD mode)
		0x2: X4 : X4 encoding (QUAD mode)
		0x3: UP_DOWN : Up / Down rotary counting mode. Input phiA increments the counter, input phiB decrements the counter. The trigger edge detection settings apply.
		0x1: INV_OUT : When bit 0 is '1', QUADRATURE_ENCODING_MODE[0] inverts "dt_line_out" (PWM/ PWM_DT modes)
		0x2: INV_COMPL_OUT : When bit 1 is '1', QUADRATURE_ENCODING_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. In QUAD mode this field acts as QUAD_RANGE_MODE field selecting between different counter range, reload value and compare / capture behavior. Default Value: 0

		0x0: COUNT_UP : Count up (to PERIOD). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. A terminal count event is generated when the counter changes from a state in which COUNTER equals PERIOD.
		0x1: COUNT_DOWN : Count down (to "0"). An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0".
		0x2: COUNT_UPDN1 : Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0".
		0x3: COUNT_UPDN2 : Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0" AND when the counter changes from a state in which COUNTER equals PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).

		0x0: QUAD_RANGE0 : In QUAD mode this setting selects the QUAD_RANGE0 mode with the following behavior: - COUNTER range is between 0x0000 and 0xFFFF / 0xFFFFFFFF (for GRP_CNT_WIDTH = 16 / 32) - on reload / index event: - CC0 is copied to CC0_BUFF - COUNTER is copied to CC0 - COUNTER is set to midpoint (0x8000 / 0x80000000) - tc and cc0_match events are generated - when COUNTER is 0x0000 or 0xFFFF / 0xFFFFFFFF: - CC0 is copied to CC0_BUFF - COUNTER (0x0000 or 0xFFFF / 0xFFFFFFFF) is copied to CC0 - COUNTER is set to midpoint (0x8000 / 0x80000000) - cc0_match event is generated

		0x1: QUAD_RANGE0_CMP : In QUAD mode this setting selects the QUAD_RANGE0_CMP mode with the following behavior: - COUNTER range is between 0x0000 and 0xFFFF / 0xFFFFFFFF (for GRP_CNT_WIDTH = 16 / 32) - the capture0 event acts as 2nd reload / index event - on reload / index event: - COUNTER is set to midpoint (0x8000 / 0x80000000) - when 'capture on index' is selected (AUTO_RELOAD_PERIOD=0): - tc event is generated - PERIOD is copied to PERIOD_BUFF - COUNTER is copied to PERIOD - when COUNTER is 0x0000 or 0xFFFF / 0xFFFFFFFF: - COUNTER is set to midpoint (0x8000 / 0x80000000) - when 'capture on wrap-around' is selected (AUTO_RELOAD_PERIOD=1): - tc event is generated - PERIOD is copied to PERIOD_BUFF - COUNTER (0x0000 or 0xFFFF / 0xFFFFFFFF) is copied to PERIOD - 1 or 2 compare functions (depending on CC1_PRESENT) available This mode is to a certain extend backward compatible with previous TCPWM quadrature behavior but allows a compare function during quadrature decoding using the CC0/CC_BUFF registers and the cc0_match event. Because of that the PERIOD/PERIOD_BUFF registers are used instead of CC0/CC_BUFF registers to capture COUNTER at reload / index event or wrap-around.

		0x2: QUAD_RANGE1_CAPT : In QUAD mode this setting selects the QUAD_RANGE1_CAPT mode with the following behavior: - COUNTER range is between 0x0000 and PERIOD - on reload / index event: - COUNTER is set to 0x0000 - tc event is generated - when COUNTER is 0x0000 and decrementing: - COUNTER is set to PERIOD - tc event is generated - when COUNTER equals PERIOD and is incrementing: - COUNTER is set to 0x0000 - tc event is generated - 1 or 2 capture functions (depending on CC1_PRESENT) available - on capture0 / capture1 event: - CC0 / CC1 is copied to CC0_BUFF / CC1_BUFF - COUNTER value is copied to CC0 It allows that the COUNTER register reflects the current angle position of the rotary encoder, i.e. no MOD or SUB calculations need to be done in SW on the COUNTER value to get the current angle position. This allows a DMA copy of the angle position from the COUNTER register. However, a disadvantage of this mode is that fast sequences of tc interrupts can occur (when encoder moves back and forth around start position). It is recommended to not use the tc interrupt in this mode.
		0x3: QUAD_RANGE1_CMP : In QUAD mode this setting selects the QUAD_RANGE1_CMP mode. The behavior is the same as for QUAD_RANGE1_CAPT mode described above with the only difference that 1 or 2 compare functions (depending on CC1_PRESENT) are available instead of 1 or 2 capture functions.
13 : 12	PWM_DISABLE_MODE	Specifies the behavior of the PWM outputs "line_out" and "line_compl_out" while the TCPWM counter is disabled (CTL.ENABLED='0') or stopped. Note: The output signal of this selection can be further modified by the immediate kill logic and line_out polarity settings (CTRL.QUAD_ENCODING_MODE). Default Value: 0

		0x0: Z : When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are NOT driven by the TCPWM. Instead the port default level configuration applies, e.g. "Z" (high impedance). Note: This is realized by driving the TCPWM output "line_out_en" to 0. When the counter is stopped upon a stop event the PWM outputs are deactivated (to the polarity defined by CTL.QUAD_ENCODING_MODE).
		0x1: RETAIN : When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are driven by the TCPWM. When the counter is disabled or stopped upon a stop event the PWM outputs are retained (keep their previous levels). While the counter is disabled or stopped the PWM outputs can be changed via LINE_SEL (when parameter GRP_SMC_PRESENT = 1).
		0x2: L : When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are driven by the TCPWM. When the counter is disabled or stopped upon a stop event the PWM output "line_out" is driven as a fixed '0' and the PWM output "line_compl_out" is driven as a fixed '1'.
		0x3: H : When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are driven by the TCPWM. When the counter is disabled or stopped upon a stop event the PWM output "line_out" is driven as a fixed '1' and the PWM output "line_compl_out" is driven as a fixed '0'.

10	PWM_SYNC_KILL	Specifies asynchronous/ synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
9	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
8	PWM_IMM_KILL	Specifies whether the kill event immediately deactivates the "dt_line_out" and "dt_line_compl_out" signals or with the next module clock ("active count" pre-scaled "clk_counter"). '0': synchronous kill activation. Deactivates the "dt_line_out" and "dt_line_compl_out" signals with the next module clock ("active count" pre-scaled "clk_counter"). '1': immediate kill activation. Immediately deactivates the "dt_line_out" and "dt_line_compl_out" signals. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
7	CC1_MATCH_DOWN_EN	Enables / disables the compare match 1 event generation (COUNTER equals CC0 register) when counting down (STATUS.DOWN = 1) in CNT_UPDN1/2 mode. '0': compare match 1 event generation disabled when counting down '1': compare match 1 event generation enabled when counting down This field has a function in PWM and PWM_DT modes only. Default Value: 1

6	CC1_MATCH_UP_EN	Enables / disables the compare match 1 event generation (COUNTER equals CC0 register) when counting up (STATUS.DOWN = 0) in CNT_UPDN1/2 mode. '0': compare match 1 event generation disabled when counting up '1': compare match 1 event generation enabled when counting up This field has a function in PWM and PWM_DT modes only. Default Value: 1
5	CC0_MATCH_DOWN_EN	Enables / disables the compare match 0 event generation (COUNTER equals CC0 register) when counting down (STATUS.DOWN = 1) in CNT_UPDN1/2 mode. '0': compare match 0 event generation disabled when counting down '1': compare match 0 event generation enabled when counting down This field has a function in PWM and PWM_DT modes only. Default Value: 1
4	CC0_MATCH_UP_EN	Enables / disables the compare match 0 event generation (COUNTER equals CC0 register) when counting up (STATUS.DOWN = 0) in CNT_UPDN1/2 mode. '0': compare match 0 event generation disabled when counting up '1': compare match 0 event generation enabled when counting up This field has a function in PWM and PWM_DT modes only. Default Value: 1
3	AUTO_RELOAD_LINE_SEL	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. Default Value: 0

2	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff. Default Value: 0
1	AUTO_RELOAD_CC1	Specifies switching of the CC1 and buffered CC1 values. This field has a function in TIMER, QUAD (QUAD_RANGE0_CMP, QUAD_RANGE1_CMP range modes), SR, PWM, PWM_DT and PWM_PR modes. Timer, QUAD, SR modes: '0': never switch. '1': switch on a compare match 1 event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0
0	AUTO_RELOAD_CC0	Specifies switching of the CC0 and buffered CC0 values. This field has a function in TIMER, QUAD (QUAD_RANGE0_CMP, QUAD_RANGE1_CMP range modes), SR, PWM, PWM_DT and PWM_PR modes. Timer, QUAD, SR modes: '0': never switch. '1': switch on a compare match 0 event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

TCPWM0_GRP1_CNT0_STATUS

Counter status register
Address: 0x40388004
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None			R
HW Access	RW	RW	RW	RW	None			RW
Name	TR_STOP	TR_RELOAD	TR_COUNT	TR_CAPTURE0	None [3:1]			DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R	None			R	R	R	R
HW Access	RW	None			RW	RW	RW	RW
Name	RUNNING	None [14:12]			LINE_COMPL_OUT	LINE_OUT	TR_CAPTURE1	TR_START

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DT_CNT_L [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	DT_CNT_H [31:24]							

Bits	Name	Description
31 : 24	DT_CNT_H	High byte of 16-bit dead time counter. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this field has no effect. Note: This field only exists when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8bit wide and the only the field DT_CNT_L is used as dead time counter. Default Value: 0
23 : 16	DT_CNT_L	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion (8bit dead time counter or low byte of 16-bit dead time counter). In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0

15	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. This field is used to indicate that the counter is running after a start/reload event and that the counter is stopped after a stop event. When a running counter operation is paused in debug state (see CTRL.DBG_PAUSE) then the RUNNING bit is still '1'. Default Value: 0
11	LINE_COMPL_OUT	Indicates the actual level of the complementary PWM line output signal. Default Value: 0
10	LINE_OUT	Indicates the actual level of the PWM line output signal. Default Value: 0
9	TR_CAPTURE1	Indicates the actual level of the selected capture 1 trigger. Default Value: 0
8	TR_START	Indicates the actual level of the selected start trigger. Default Value: 0
7	TR_STOP	Indicates the actual level of the selected stop trigger. Default Value: 0
6	TR_RELOAD	Indicates the actual level of the selected reload trigger. Default Value: 0
5	TR_COUNT	Indicates the actual level of the selected count trigger. Default Value: 1
4	TR_CAPTURE0	Indicates the actual level of the selected capture 0 trigger. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

TCPWM0_GRP1_CNT0_LINE_SEL

Counter line selection register
Address: 0x40388028
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	RW			None	RW		
Name	None	COMPL_OUT_SEL [6:4]			None	OUT_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 4	COMPL_OUT_SEL	Selects the source for the output signal "line_compl_out". Default setting is the inverted PWM signal "line". Other settings are useful for Stepper Motor Control. This field has a function in PWM and PWM_PR modes only. Note: The output signal of this selection can be further modified by the stop / kill logic and line_compl_out polarity setting (CTRL.QUAD_ENCODING_MODE[1]). Default Value: 3
		0x0: L : fixed '0'
		0x1: H : fixed '1'
		0x2: PWM : PWM signal "line"
		0x3: PWM_INV : inverted PWM signal "line"

		0x4: Z : The output "line_compl_out" is not driven by the TCPWM. Instead the port default level configuration applies, e.g. "Z" (high impedance). Note: This is realized by driving the output "line_compl_out_en" to 0.
		0x5: Reserved5 : This setting is reserved. Do not use.
		0x6: Reserved6 : This setting is reserved. Do not use.
		0x7: Reserved7 : This setting is reserved. Do not use.
2 : 0	OUT_SEL	Selects the source for the output signal "line_out". Default setting is the PWM signal "line". Other settings are useful for Stepper Motor Control. This field has a function in PWM and PWM_PR modes only. Note: The output signal of this selection can be further modified by the stop / kill logic and line_out polarity setting (CTRL.QUAD_ENCODING_MODE[0]). Default Value: 2
		0x0: L : fixed '0'
		0x1: H : fixed '1'
		0x2: PWM : PWM signal "line"
		0x3: PWM_INV : inverted PWM signal "line"
		0x4: Z : The output "line_out" is not driven by the TCPWM. Instead the port default level configuration applies, e.g. "Z" (high impedance). Note: This is realized by driving the output "line_out_en" to 0.
		0x5: Reserved5 : This setting is reserved. Do not use.
		0x6: Reserved6 : This setting is reserved. Do not use.
		0x7: Reserved7 : This setting is reserved. Do not use.

TCPWM0_GRP1_CNT0_LINE_SEL_BUFF

Counter buffered line selection register
Address: 0x4038802C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	RW			None	RW		
Name	None	COMPL_OUT_SEL [6:4]			None	OUT_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 4	COMPL_OUT_SEL	Buffer for LINE_SEL.COMPL.OUT_SEL. Can be exchanged with LINE_SEL.LINE_COMPL_OUT_SEL on a terminal count event with an actively pending switch event. This field has a function in PWM and PWM_PR modes only. Default Value: 3
2 : 0	OUT_SEL	Buffer for LINE_SEL.OUT_SEL. Can be exchanged with LINE_SEL.LINE_OUT_SEL on a terminal count event with an actively pending switch event. This field has a function in PWM and PWM_PR modes only. Default Value: 2

TCPWM0_GRP1_CNT0_DT

Counter PWM dead time register
Address: 0x40388030
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DT_LINE_OUT_L [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DT_LINE_OUT_H [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DT_LINE_COMPL_OUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DT_LINE_COMPL_OUT [31:24]							

Bits	Name	Description
31 : 16	DT_LINE_COMPL_OUT	In PWM_DT mode, this field is used to determine the dead time before activating the complementary PWM line output signal "line_compl_out": amount of dead time cycles in the counter clock domain. In all other modes, this field has no effect. Note: This field only exists when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8 bit wide and the same dead time specified by field DT_LINE_OUT_L is used before activating "line_out" and "line_compl_out". Default Value: 0

15 : 8	DT_LINE_OUT_H	In PWM_DT mode, this field is used to determine the high byte of the dead time before activating the PWM line output signal "line_out": amount of dead time cycles in the counter clock domain. In all other modes, this field has no effect. Note: This field only exists when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8 bit wide and the same dead time specified by field DT_LINE_OUT_L is used before activating "line_out" and "line_compl_out". Default Value: 0
7 : 0	DT_LINE_OUT_L	In PWM_DT mode, this field is used to determine the low byte of the dead time before activating the PWM line output signal "line_out": amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Note: This field determines the low byte of the 16-bit dead time before activating "line_out" when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8 bit wide and the same dead time specified by this DT_LINE_OUT_L field is used before activating "line_out" and "line_compl_out". Default Value: 0
		0x0: DIVBY1 : Divide by 1 (other-than-PWM_DT mode)
		0x1: DIVBY2 : Divide by 2 (other-than-PWM_DT mode)
		0x2: DIVBY4 : Divide by 4 (other-than-PWM_DT mode)
		0x3: DIVBY8 : Divide by 8 (other-than-PWM_DT mode)
		0x4: DIVBY16 : Divide by 16 (other-than-PWM_DT mode)
		0x5: DIVBY32 : Divide by 32 (other-than-PWM_DT mode)
		0x6: DIVBY64 : Divide by 64 (other-than-PWM_DT mode)
		0x7: DIVBY128 : Divide by 128 (other-than-PWM_DT mode)

TCPWM0_GRP2_CNT0_COUNTER

Counter count register
Address: 0x40390008
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	COUNTER [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	COUNTER [31:24]							

Bits	Name	Description
31 : 0	COUNTER	16-bit / 32-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

TCPWM0_GRP2_CNT0_CC0

Counter compare/capture 0 register
Address: 0x40390010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	CC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	CC [31:24]							

Bits	Name	Description
31 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 4294967295

TCPWM0_GRP2_CNT0_CC0_BUFF

Counter buffered compare/capture 0 register
Address: 0x40390014
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	CC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	CC [31:24]							

Bits	Name	Description
31 : 0	CC	Additional buffer for counter CC register. Default Value: 4294967295

TCPWM0_GRP2_CNT0_CC1

Counter compare/capture 1 register
Address: 0x40390018
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	CC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	CC [31:24]							

Bits	Name	Description
31 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 4294967295

TCPWM0_GRP2_CNT0_CC1_BUFF

Counter buffered compare/capture 1 register
Address: 0x4039001C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	CC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	CC [31:24]							

Bits	Name	Description
31 : 0	CC	Additional buffer for counter CC1 register. Default Value: 4294967295

TCPWM0_GRP2_CNT0_PERIOD

Counter period register
Address: 0x40390020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	PERIOD [31:24]							

Bits	Name	Description
31 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 4294967295

TCPWM0_GRP2_CNT0_PERIOD_BUFF

Counter buffered period register
Address: 0x40390024
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	PERIOD [31:24]							

Bits	Name	Description

31 : 0	PERIOD	Additional buffer for counter PERIOD register. In PWM_PR mode PEROD_BUFF defines the LFSR polynomial. Each bit represents a tap of the shift register which can be feed back to the MSB via an XOR tree. Examples for GRP_CNT_WIDTH = 16: - Maximum length 16bit LFSR - polynomial x^16 + x^14 + x^13 + x^11 + 1 - taps 0,2,3,5 -> PERIOD = 0x002d - period is 2^16-1 = 65535 cycles - Maximum length 8bit LFSR: - polynomial x^8 + x^6 + x^5 + x^4 + 1 - taps 8,10,11,12 (realized in 8 MSBs of 16bit LFSR) - period is 2^8-1 = 255 cycles In SR mode PERIOD_BUFF defines which tap of the shift register generates the PWM output signals. For a delay of n cycles (from capture event to PWM output) the bit CNT_WIDTH-n should be set to '1'. For a shift register function only one tap should be use, i.e. a one-hot value must be written to PERIOD_BUFF. If multiple bits in PERIOD_BUFF are set then the taps are XOR combined. Default Value: 4294967295

15 Cryptography block (CRYPTO)

Register details

Register name	Address	Description
CRYPTO_CTL	0x40100000	Control
CRYPTO_RAM_PWR_CTL	0x40100008	SRAM power control
CRYPTO_RAM_PWR_DELAY_CTL	0x4010000C	SRAM power delay control
CRYPTO_ECC_CTL	0x40100010	ECC control
CRYPTO_ERROR_STATUS0	0x40100020	Error status 0
CRYPTO_ERROR_STATUS1	0x40100024	Error status 1
CRYPTO_INTR	0x40100100	Interrupt register
CRYPTO_INTR_SET	0x40100104	Interrupt set register
CRYPTO_INTR_MASK	0x40100108	Interrupt mask register
CRYPTO_INTR_MASKED	0x4010010C	Interrupt masked register
CRYPTO_PR_LFSR_CTL0	0x40100200	Pseudo random LFSR control 0
CRYPTO_PR_LFSR_CTL1	0x40100204	Pseudo random LFSR control 1
CRYPTO_PR_LFSR_CTL2	0x40100208	Pseudo random LFSR control 2
CRYPTO_PR_MAX_CTL	0x4010020C	Pseudo random maximum control
CRYPTO_PR_CMD	0x40100210	Pseudo random command
CRYPTO_PR_RESULT	0x40100218	Pseudo random result
CRYPTO_TR_CTL0	0x40100280	True random control 0
CRYPTO_TR_CTL1	0x40100284	True random control 1
CRYPTO_TR_CTL2	0x40100288	True random control 2
CRYPTO_TR_STATUS	0x4010028C	True random status
CRYPTO_TR_CMD	0x40100290	True random command
CRYPTO_TR_RESULT	0x40100298	True random result
CRYPTO_TR_GARO_CTL	0x401002A0	True random GARO control
CRYPTO_TR_FIRO_CTL	0x401002A4	True random FIRO control
CRYPTO_TR_MON_CTL	0x401002C0	True random monitor control
CRYPTO_TR_MON_CMD	0x401002C8	True random monitor command
CRYPTO_TR_MON_RC_CTL	0x401002D0	True random monitor RC control
CRYPTO_TR_MON_RC_STATUS0	0x401002D8	True random monitor RC status 0
CRYPTO_TR_MON_RC_STATUS1	0x401002DC	True random monitor RC status 1
CRYPTO_TR_MON_AP_CTL	0x401002E0	True random monitor AP control
CRYPTO_TR_MON_AP_STATUS0	0x401002E8	True random monitor AP status 0
CRYPTO_TR_MON_AP_STATUS1	0x401002EC	True random monitor AP status 1
CRYPTO_STATUS	0x40101004	Status
CRYPTO_INSTR_FF_CTL	0x40101040	Instruction FIFO control
CRYPTO_INSTR_FF_STATUS	0x40101044	Instruction FIFO status

Register name	Address	Description
CRYPTO_INSTR_FF_WR	0x40101048	Instruction FIFO write
CRYPTO_LOAD0_FF_STATUS	0x401010C0	Load 0 FIFO status
CRYPTO_LOAD1_FF_STATUS	0x401010D0	Load 1 FIFO status
CRYPTO_STORE_FF_STATUS	0x401010F0	Store FIFO status
CRYPTO_AES_CTL	0x40101100	AES control
CRYPTO_RESULT	0x40101180	Result
CRYPTO_CRC_CTL	0x40101400	CRC control
CRYPTO_CRC_DATA_CTL	0x40101410	CRC data control
CRYPTO_CRC_POL_CTL	0x40101420	CRC polynomial control
CRYPTO_CRC_REM_CTL	0x40101440	CRC remainder control
CRYPTO_CRC_REM_RESULT	0x40101448	CRC remainder result
CRYPTO_VU_CTL0	0x40101480	Vector unit control 0
CRYPTO_VU_CTL1	0x40101484	Vector unit control 1
CRYPTO_VU_CTL2	0x40101488	Vector unit control 2
CRYPTO_VU_STATUS	0x40101490	Vector unit status
CRYPTO_VU_RF_DATA0	0x401014C0	Vector unit register-file
CRYPTO_VU_RF_DATA1	0x401014C4	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA2	0x401014C8	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA3	0x401014CC	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA4	0x401014D0	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA5	0x401014D4	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA6	0x401014D8	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA7	0x401014DC	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA8	0x401014E0	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA9	0x401014E4	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA10	0x401014E8	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA11	0x401014EC	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA12	0x401014F0	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA13	0x401014F4	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.

Register name	Address	Description
CRYPTO_VU_RF_DATA14	0x401014F8	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA15	0x401014FC	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_DEV_KEY_ADDR0_CTL	0x40102000	Device key address 0 control
CRYPTO_DEV_KEY_ADDR0	0x40102004	Device key address 0
CRYPTO_DEV_KEY_ADDR1_CTL	0x40102020	Device key address 1 control
CRYPTO_DEV_KEY_ADDR1	0x40102024	Device key address 1 control
CRYPTO_DEV_KEY_STATUS	0x40102080	Device key status
CRYPTO_DEV_KEY_CTL0	0x40102100	Device key control 0
CRYPTO_DEV_KEY_CTL1	0x40102120	Device key control 1
CRYPTO_MEM_BUFF0	0x40108000	Memory buffer. This is the starting address of a register bank containing 2048 registers (CRYPTO_MEM_BUFF0 to CRYPTO_MEM_BUFF2047).

15.1 CRYPTO registers

CRYPTO_CTL

Control
Address: 0x40100000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				None		RW	RW
HW Access	R				None		R	R
Name	PC [7:4]				None [3:2]		NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						ECC_INJ_EN	ECC_EN

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description

31	ENABLED	IP enable: '0': Disabled. All non-retention registers (command and status registers, instruct FIFO, internal component state machines) are reset to their default value when the IP is disabled. All retention registers retain their value when the IP is disabled. '1': Enabled. When the IP is enabled, the IP register buffer is set to "0". Default Value: 0
		0x0: DISABLED :
		0x1: ENABLED :
17	ECC_INJ_EN	Enable parity injection for SRAM. When '1', the parity (ECC_CTL.PARITY) is used when a full 32-bit write is done to the ECC_CTL.WORD_ADDR word address of the SRAM. Default Value: 0
16	ECC_EN	Enable ECC checking: '0': Disabled. '1': Enabled. Default Value: 1
7 : 4	PC	Protection context. This field is set with the protection context of the transaction that writes this register; i.e. the context is inherited from the write transaction and not specified by the transaction write data. All IP master transactions use the PC field for the protection context. There is one exception: the LOAD_DEV_KEY instruction IP master transactions are always performed with protection context "0". Default Value: 0
1	NS	Secure/on-secure access control: '0': secure. '1': non-secure. This field is set with the secure/non-secure access control of the transaction that writes this register; i.e. the access control is inherited from the write transaction and not specified by the transaction write data. All IP master transactions use the NS field for the secure/non-secure access control ("hprot[4]"). Default Value: 1

0	P	User/privileged access control: '0': user mode. '1': privileged mode. This field is set with the user/ privileged access control of the transaction that writes this register; i.e. the access control is inherited from the write transaction and not specified by the transaction write data. All IP master transactions use the P field for the user/privileged access control ("hprot[1]"). Default Value: 0

CRYPTO_RAM_PWR_CTL

SRAM power control
Address: 0x40100008
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	PWR_MODE	Set power mode for memory buffer SRAM. Default Value: 3
		0x0: OFF : See CM4_PWR_CTL
		0x1: RESERVED : undefined
		0x2: RETAINED : See CM4_PWR_CTL
		0x3: ENABLED : See CM4_PWR_CTL

CRYPTO_RAM_PWR_DELAY_CTL

SRAM power delay control
Address: 0x4010000C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	UP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						UP [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	UP	Number clock cycles delay needed after power domain power up Default Value: 0x96

CRYPTO_ECC_CTL

ECC control
Address: 0x40100010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WORD_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			WORD_ADDR [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							None
HW Access	R							None
Name	PARITY [31:25]							None

Bits	Name	Description
31 : 25	PARITY	ECC parity to use for ECC error injection at address WORD_ADDR. Default Value: 0
12 : 0	WORD_ADDR	Specifies the word address where the parity is injected. - On a 32-bit write access to this SRAM address and when CTL.ECC_INJ_EN bit is '1', the parity (PARITY) is injected. Default Value: 0

CRYPTO_ERROR_STATUS0

Error status 0
Address: 0x40100020
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Specifies error description information. - For INSTR_OPC_ERROR/ INSTR_CC_ERROR/ INSTR_DEV_KEY_ERROR: - Violating instruction (from instruction FIFO). - For BUS_ERROR: - Violating transfer, address. Default Value: Undefined

CRYPTO_ERROR_STATUS1

Error status 1
Address: 0x40100024
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DATA24 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	DATA24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DATA24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None				R		
HW Access	RW	None				RW		
Name	VALID	None [30:27]				IDX [26:24]		

Bits	Name	Description
31	VALID	Specifies if ERROR_STATUS0 and ERROR_STATUS1 specify valid error information. No new error information is captured as long as VALID is '1'; i.e. the error information of the first detected error is NOT overwritten. Default Value: 0
26 : 24	IDX	Error source: "0": INSTR_OPC_ERROR (instruction FIFO decoder error). "1": INSTR_CC_ERROR (instruction FIFO decoder, VU CC error). "2": BUS_ERROR (bus master interface AHB-Lite bus error). "3": TR_AP_DETECT_ERROR. "4": TR_RC_DETECT_ERROR. "5": INSTR_DEV_KEY_ERROR. "6"-"7": Undefined. Default Value: Undefined

23 : 0	DATA24	Specifies error description information. - For BUS_ERROR: - Violating transfer, read attribute (DATA[0]). - Violating transfer, size attribute (DATA[5:4]). "0": 8-bit transfer, "1": 16 bits transfer, "2": 32-bit transfer. Default Value: Undefined

CRYPTO_INTR

Interrupt register
Address: 0x40100100
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None			RW1S	RW1S	RW1S	RW1S	RW1S
Name	None [7:5]			PR_DATA_AVAILABLE	TR_DATA_AVAILABLE	TR_INITIALIZED	INSTR_FF_OVERFLOW	INSTR_FF_LEVEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None		RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	None [23:22]		INSTR_DEV_KEY_ERROR	TR_RC_DETECT_ERROR	TR_AP_DETECT_ERROR	BUS_ERROR	INSTR_CC_ERROR	INSTR_OPC_ERROR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	INSTR_DEV_KEY_ERROR	This interrupt cause is activated (HW sets the field to '1') when the LOAD_DEV_KEY instruction tries to load a device key whose DEV_KEY_ADDR_CTL.VALID or DEV_KEY_CTL.ALLOWED is set to '0'. Default Value: 0
20	TR_RC_DETECT_ERROR	This interrupt cause is activated (HW sets the field to '1') when the true random number generator monitor adaptive proportion test detects a disproportionate occurrence of a specific bit value. Default Value: 0
19	TR_AP_DETECT_ERROR	This interrupt cause is activated (HW sets the field to '1') when the true random number generator monitor adaptive proportion test detects a repetition of a specific bit value. Default Value: 0

18	BUS_ERROR	This interrupt cause is activated (HW sets the field to '1') when a AHB-Lite bus error is observed on the AHB-Lite master interface. When the interrupt cause is activated, HW sets INSTR_FF_CTL.CLEAR to '1'. Default Value: 0
17	INSTR_CC_ERROR	This interrupt cause is activated (HW sets the field to '1') when the instruction decoder encounters an instruction with a non-defined condition code. This error is only generated for VU instructions. When the interrupt cause is activated, HW sets INSTR_FF_CTL.CLEAR to '1'. Default Value: 0
16	INSTR_OPC_ERROR	This interrupt cause is activated (HW sets the field to '1') when the instruction decoder encounters an instruction with a non-defined operation code (opcode). When the interrupt cause is activated, HW sets INSTR_FF_CTL.CLEAR to '1'. Default Value: 0
4	PR_DATA_AVAILABLE	This interrupt cause is activated (HW sets the field to '1') when the pseudo random number generator has generated a data value. Default Value: 0
3	TR_DATA_AVAILABLE	This interrupt cause is activated (HW sets the field to '1') when the true random number generator has generated a data value of the specified bit size. Default Value: 0
2	TR_INITIALIZED	This interrupt cause is activated (HW sets the field to '1') when the true random number generator is initialized. Default Value: 0
1	INSTR_FF_OVERFLOW	This interrupt cause is activated (HW sets the field to '1') when the instruction FIFO overflows (an attempt is made to write to a full FIFO). Default Value: 0
0	INSTR_FF_LEVEL	This interrupt cause is activated (HW sets the field to '1') when the instruction FIFO event is activated. Default Value: 0

CRYPTO_INTR_SET

Interrupt set register
Address: 0x40100104
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	None			A	A	A	A	A
Name	None [7:5]			PR_DATA_AVAILABLE	TR_DATA_AVAILABLE	TR_INITIALIZED	INSTR_FF_OVERFLOW	INSTR_FF_LEVEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	None		A	A	A	A	A	A
Name	None [23:22]		INSTR_DEV_KEY_ERROR	TR_RC_DETECT_ERROR	TR_AP_DETECT_ERROR	BUS_ERROR	INSTR_CC_ERROR	INSTR_OPC_ERROR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	INSTR_DEV_KEY_ERROR	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
20	TR_RC_DETECT_ERROR	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
19	TR_AP_DETECT_ERROR	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
18	BUS_ERROR	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
17	INSTR_CC_ERROR	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
16	INSTR_OPC_ERROR	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0

4	PR_DATA_AVAILABLE	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
3	TR_DATA_AVAILABLE	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
2	TR_INITIALIZED	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
1	INSTR_FF_OVERFLOW	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
0	INSTR_FF_LEVEL	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0

CRYPTO_INTR_MASK

Interrupt mask register
Address: 0x40100108
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			PR_DATA_AVAILABLE	TR_DATA_AVAILABLE	TR_INITIALIZED	INSTR_FF_OVERFLOW	INSTR_FF_LEVEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [23:22]		INSTR_DEV_KEY_ERROR	TR_RC_DETECT_ERROR	TR_AP_DETECT_ERROR	BUS_ERROR	INSTR_CC_ERROR	INSTR_OPC_ERROR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	INSTR_DEV_KEY_ERROR	Mask bit for corresponding field in interrupt request register. Default Value: 0
20	TR_RC_DETECT_ERROR	Mask bit for corresponding field in interrupt request register. Default Value: 0
19	TR_AP_DETECT_ERROR	Mask bit for corresponding field in interrupt request register. Default Value: 0
18	BUS_ERROR	Mask bit for corresponding field in interrupt request register. Default Value: 0
17	INSTR_CC_ERROR	Mask bit for corresponding field in interrupt request register. Default Value: 0
16	INSTR_OPC_ERROR	Mask bit for corresponding field in interrupt request register. Default Value: 0

4	PR_DATA_AVAILABLE	Mask bit for corresponding field in interrupt request register. Default Value: 0
3	TR_DATA_AVAILABLE	Mask bit for corresponding field in interrupt request register. Default Value: 0
2	TR_INITIALIZED	Mask bit for corresponding field in interrupt request register. Default Value: 0
1	INSTR_FF_OVERFLOW	Mask bit for corresponding field in interrupt request register. Default Value: 0
0	INSTR_FF_LEVEL	Mask bit for corresponding field in interrupt request register. Default Value: 0

CRYPTO_INTR_MASKED

Interrupt masked register
Address: 0x4010010C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	R	R	R	R
HW Access	None			W	W	W	W	W
Name	None [7:5]			PR_DATA_AVAILABLE	TR_DATA_AVAILABLE	TR_INITIALIZED	INSTR_FF_OVERFLOW	INSTR_FF_LEVEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [23:22]		INSTR_DEV_KEY_ERROR	TR_RC_DETECT_ERROR	TR_AP_DETECT_ERROR	BUS_ERROR	INSTR_CC_ERROR	INSTR_OPC_ERROR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	INSTR_DEV_KEY_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
20	TR_RC_DETECT_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
19	TR_AP_DETECT_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
18	BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
17	INSTR_CC_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
16	INSTR_OPC_ERROR	Logical and of corresponding request and mask bits. Default Value: 0

4	PR_DATA_AVAILABLE	Logical and of corresponding request and mask bits. Default Value: 0
3	TR_DATA_AVAILABLE	Logical and of corresponding request and mask bits. Default Value: 0
2	TR_INITIALIZED	Logical and of corresponding request and mask bits. Default Value: 0
1	INSTR_FF_OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
0	INSTR_FF_LEVEL	Logical and of corresponding request and mask bits. Default Value: 0

CRYPTO_PR_LFSR_CTL0

Pseudo random LFSR control 0
Address: 0x40100200
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	LFSR32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	LFSR32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	LFSR32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	LFSR32 [31:24]							

Bits	Name	Description

31 : 0	LFSR32	State of a 32-bit Linear Feedback Shift Registers (LFSR) that is used to generate a pseudo random bit sequence. This register needs to be initialized by SW. The initialization value should be different from "0". The three PR_LFSR_CTL registers represents the state of a 32-bit, 31-bit and 29-bit LFSR. Individually, these LFSRs generate a pseudo random bit sequence that repeats itself after (2^32)-1, (2^31)-1 and (2^29)-1 bits. The numbers (2^32)-1, (2^31)-1 and (2^29)-1 are relatively prime (their greatest common denominator is "1"). The three bit sequence are combined (XOR'd) into a single bitstream to create a pseudo random bit sequence that repeats itself after ((2^32)-1) * ((2^31)-1) * ((2*29)-1) bits. The following polynomials are used: - 32-bit irreducible polynomial: x^32+x^30+x^26+x^25+1. - 31-bit irreducible polynomial: x^31+x^28+1. - 29-bit irreducible polynomial: x^29+x^27+1. Default Value: 0xD8959BC9

CRYPTO_PR_LFSR_CTL1

Pseudo random LFSR control 1
Address: 0x40100204
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	LFSR31 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	LFSR31 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	LFSR31 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	RW						
Name	None	LFSR31 [30:24]						

Bits	Name	Description
30 : 0	LFSR31	State of a 31-bit Linear Feedback Shift Registers (LFSR) that is used to generate a pseudo random bit sequence. See PR_LFSR_CTL0. Default Value: 0x2BB911F8

CRYPTO_PR_LFSR_CTL2

Pseudo random LFSR control 2
Address: 0x40100208
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	LFSR29 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	LFSR29 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	LFSR29 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			RW				
Name	None [31:29]			LFSR29 [28:24]				

Bits	Name	Description
28 : 0	LFSR29	State of a 29-bit Linear Feedback Shift Registers (LFSR) that is used to generate a pseudo random bit sequence. See PR_LFSR_CTL0. Default Value: 0x060C31B7

CRYPTO_PR_MAX_CTL

Pseudo random maximum control
Address: 0x4010020C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Maximum value of to be generated random number Default Value: 0xFFFFFFFF

CRYPTO_PR_CMD

Pseudo random command
Address: 0x40100210
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	START	Pseudo random command. On a generated number, HW sets this field to '0' and sets INTR.PR_DATA_AVAILABLE to '1. Default Value: 0

CRYPTO_PR_RESULT

Pseudo random result
Address: 0x40100218
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Result of a pseudo random number generation operation. The resulting value DATA is in the range [0, PR_MAX_CTL.DATA32]. The PR_DATA_AVAILABLE interrupt cause is activated when the number is generated. Note that SW can write this field. This functionality can be used prevent information leakage. Default Value: 0

CRYPTO_TR_CTL0

True random control 0
Address: 0x40100280
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAMPLE_CLOCK_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RED_CLOCK_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INIT_DELAY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW	RW	None			RW
HW Access	None		R	R	None			R
Name	None [31:30]		STOP_ON_RC_DETECT	STOP_ON_AP_DETECT	None [27:25]			VON_NEUMANN_CORR

Bits	Name	Description
29	STOP_ON_RC_DETECT	Specifies if TRNG functionality is stopped on a repetition count test detection (when HW sets INTR.TR_RC_DETECT to '1'): '0': Functionality is NOT stopped. '1': Functionality is stopped (TR_CTL1 fields are set to '0' by HW). Default Value: 0
28	STOP_ON_AP_DETECT	Specifies if TRNG functionality is stopped on an adaptive proportion test detection (when HW sets INTR.TR_AP_DETECT to '1'): '0': Functionality is NOT stopped. '1': Functionality is stopped (TR_CTL1 fields are set to '0' by HW). Default Value: 0

24	VON_NEUMANN_CORR	Specifies if the "von Neumann corrector" is disabled or enabled: '0': disabled. '1': enabled. The "von Neumann corrector" post-processes the reduced bits to remove a '0' or '1' bias. The corrector operates on reduced bit pairs ("oldest bit, newest bit"): "00": no bit is produced. "01": '0' bit is produced (oldest bit). "10": '1' bit is produced (oldest bit). "11": no bit is produced. Note that the corrector produces bits at a random pace and at a frequency that is 1/4 of the reduced bit frequency (reduced bits are processed in pairs, and half of the pairs do NOT produce a bit). Default Value: 0
23 : 16	INIT_DELAY	Specifies an initialization delay: number of removed/dropped samples before reduced bits are generated. This field should be programmed in the range [1, 255]. After starting the oscillators, at least the first 2 samples should be removed/dropped to clear the state of internal synchronizers. In addition, it is advised to drop at least the second 2 samples from the oscillators (to circumvent the semi-predictable oscillator startup behavior). This result in the default field value of "3". Field encoding is as follows: "0": 1 sample is dropped. "1": 2 samples are dropped. ... "255": 256 samples are dropped. The TR_INITIALIZED interrupt cause is set to '1', when the initialization delay is passed. Default Value: 3
15 : 8	RED_CLOCK_DIV	Specifies the clock divider that is used to produce reduced bits. "0": 1 reduced bit is produced for each sample. "1": 1 reduced bit is produced for each 2 samples. ... "255": 1 reduced bit is produced for each 256 samples. The reduced bits are considered random bits and shifted into TR_RESULT0.DATA32. Default Value: 0

7 : 0	SAMPLE_CLOCK_DIV	Specifies the clock divider that is used to sample oscillator data. This clock divider is wrt. "clk_sys". "0": sample clock is "clk_sys". "1": sample clock is "clk_sys"/2. ... "255": sample clock is "clk_sys"/ 256. Default Value: 0

CRYPTO_TR_CTL1

True random control 1
Address: 0x40100284
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:6]		FIRO31_EN	FIRO15_EN	GARO31_EN	GARO15_EN	RO15_EN	RO11_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	FIRO31_EN	FW sets this field to '1' to enable the programmable Fibonacci ring oscillator with up to 31 inverters. The TR_FIRO_CTL register specifies the programmable polynomial. Default Value: 0
4	FIRO15_EN	FW sets this field to '1' to enable the fixed Fibonacci ring oscillator with 15 inverters. Default Value: 0
3	GARO31_EN	FW sets this field to '1' to enable the programmable Galois ring oscillator with up to 31 inverters. The TR_GARO_CTL register specifies the programmable polynomial. Default Value: 0
2	GARO15_EN	FW sets this field to '1' to enable the fixed Galois ring oscillator with 15 inverters. Default Value: 0
1	RO15_EN	FW sets this field to '1' to enable the ring oscillator with 15 inverters. Default Value: 0

0	RO11_EN	FW sets this field to '1' to enable the ring oscillator with 11 inverters. Default Value: 0

CRYPTO_TR_CTL2

True random control 2
Address: 0x40100288
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		SIZE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	SIZE	Bit size of generated random number in TR_RESULT. Legal range is in [0, 32]. Default Value: 0

CRYPTO_TR_STATUS

True random status
Address: 0x4010028C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							INITIALIZED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INITIALIZED	Reflects the state of the true random number generator: '0': Not initialized (TR_CTL0.INIT_DELAY has NOT passed). '1': Initialized (TR_CTL0.INIT_DELAY has passed). Default Value: 0

CRYPTO_TR_CMD

True random command
Address: 0x40100290
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	START	True random command. On completion of the command, HW sets this field to '0' and sets INTR.TR_DATA_AVAILABLE to '1 when: - A random number is generated in TR_RESULT. - All ring oscillators are off (per TR_CTL1). - A repetition count (RC) or adaptive proportion (AP) error is detected during the random number generation (INTR.TR_RC/ AP_DETECT_ERROR). Note: On completion of the command, SW should check TR_CTL1 and INTR.TR_RC/AP_DETECT_ERROR to ensure that no unexpected error occurred during random number generation. Default Value: 0

CRYPTO_TR_RESULT

True random result
Address: 0x40100298
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Generated true random number. HW generates the number in the least significant bit positions (TR_CTL2.SIZE) of this field. The TR_DATA_AVAILABLE interrupt cause is activated when the number is generated. Note that SW can write this field. This functionality can be used prevent information leakage. Default Value: 0

CRYPTO_TR_GARO_CTL

True random GARO control
Address: 0x401002A0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	POLYNOMIAL31 [30:24]						

Bits	Name	Description
30 : 0	POLYNOMIAL31	Polynomial for programmable Galois ring oscillator. The polynomial is represented WITHOUT the high order bit (this bit is always assumed '1'). The polynomial should be aligned such that the more significant bits (bit 30 and down) contain the polynomial and the less significant bits (bit 0 and up) contain padding '0's. Default Value: 0

CRYPTO_TR_FIRO_CTL

True random FIRO control
Address: 0x401002A4
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	POLYNOMIAL31 [30:24]						

Bits	Name	Description
30 : 0	POLYNOMIAL31	Polynomial for programmable Fibonacci ring oscillator. The polynomial is represented WITHOUT the high order bit (this bit is always assumed '1'). The polynomial should be aligned such that the more significant bits (bit 30 and down) contain the polynomial and the less significant bits (bit 0 and up) contain padding '0's. Default Value: 0

CRYPTO_TR_MON_CTL

True random monitor control
Address: 0x401002C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						BITSTREAM_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	BITSTREAM_SEL	Selection of the bitstream: "0": DAS bitstream. "1": RED bitstream. "2": TR bitstream. "3": Undefined. Default Value: 2

CRYPTO_TR_MON_CMD

True random monitor command
Address: 0x401002C8
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1C	RW1C
Name	None [7:2]						START_RC	START_AP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	START_RC	Repetition count (RC) test enable: '0': Disabled. '1': Enabled. On a RC detection, HW sets this field to '0' and sets INTR.TR_RC_DETECT to '1. Default Value: 0
0	START_AP	Adaptive proportion (AP) test enable: '0': Stopped. '1': Started. On a AP detection, HW sets this field to '0' and sets INTR.TR_AP_DETECT to '1. Default Value: 0

CRYPTO_TR_MON_RC_CTL

True random monitor RC control
Address: 0x401002D0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CUTOFF_COUNT8 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CUTOFF_COUNT8	Cutoff count (legal range is [1, 255]): "0": Illegal. "1": 1 repetition. ... "255": 255 repetitions. Default Value: 255

CRYPTO_TR_MON_RC_STATUS0

True random monitor RC status 0
Address: 0x401002D8
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							BIT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	BIT	Current active bit value: '0': '0'. '1': '1'. This field is only valid when TR_MON_RC_STATUS1.REP_COUNT is NOT equal to "0". Default Value: 0

CRYPTO_TR_MON_RC_STATUS1

True random monitor RC status 1
Address: 0x401002DC
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	REP_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	REP_COUNT	Number of repetitions of the current active bit counter: "0": 0 repetitions. ... "255": 255 repetitions. Default Value: 0

CRYPTO_TR_MON_AP_CTL

True random monitor AP control
Address: 0x401002E0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CUTOFF_COUNT16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CUTOFF_COUNT16 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	WINDOW_SIZE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	WINDOW_SIZE [31:24]							

Bits	Name	Description
31 : 16	WINDOW_SIZE	Window size (minus 1) : "0": 1 bit. ... "65535": 65536 bits. Default Value: 65535
15 : 0	CUTOFF_COUNT16	Cutoff count (legal range is [1, 65535]). "0": Illegal. "1": 1 occurrence. ... "65535": 65535 occurrences. Default Value: 65535

CRYPTO_TR_MON_AP_STATUS0

True random monitor AP status 0
Address: 0x401002E8
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							BIT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	BIT	Current active bit value: '0': '0'. '1': '1'. This field is only valid when TR_MON_AP_STATUS1.OCC_COUNT is NOT equal to "0". Default Value: 0

CRYPTO_TR_MON_AP_STATUS1

True random monitor AP status 1
Address: 0x401002EC
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	OCC_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	OCC_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	WINDOW_INDEX [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	WINDOW_INDEX [31:24]							

Bits	Name	Description
31 : 16	WINDOW_INDEX	Counter to keep track of the current index in the window (counts from "0" to TR_MON_AP_CTL.WINDOW_SIZE to "0"). Default Value: 0
15 : 0	OCC_COUNT	Number of occurrences of the current active bit counter: "0": 0 occurrences ... "65535": 65535 occurrences Default Value: 0

CRYPTO_STATUS

Status
Address: 0x40101004
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	BUSY	None [30:24]						

Bits	Name	Description
31	BUSY	Reflects the state of the IP: '0': Idle/no busy. '1': Busy: - Instruction is pending in the instruction FIFO. - Instruction is busy in a IP component (e.g. SHA1, SHA2, SHA3, DES, TDES, AES, CHACHA, ...). - Store FIFO is busy. - TR or PR command is busy. Default Value: 0

CRYPTO_INSTR_FF_CTL

Instruction FIFO control
Address: 0x40101040
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					EVENT_LEVEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	RW1S
Name	None [23:18]						BLOCK	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

17	BLOCK	This field specifies the behavior when an instruction is written to a full FIFO (INSTR_FIFO_WR MMIO register): '0': The write is ignored/dropped and the INTR.INSTR_FF_OVERFLOW interrupt cause is set to '1'. '1': The write is blocked, resulting in AHB-Lite wait states and the INTR.INSTR_FF_OVERFLOW interrupt cause is set to '1' (this cause may be masked out). The instruction is written to the FIFO as soon as a FIFO entry becomes available. The maximum time is roughly the time of the execution of the slowest/longest instruction. Note that this setting may "lock up" /stall the CPU. When the CPU is "locked up"/stalled it can not respond to any system interrupts. As a result, the interrupt latency is increased. Note that this may not be an issue if the associated CPU is only performing cryptography functionality, e.g. the CM0+ during boot time. Default Value: 1
16	CLEAR	When '1', the instruction FIFO is cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. HW sets this field to '1' on when a INSTR_OPC_ERROR, INSTR_CC_ERROR or BUS_ERROR interrupt cause is activated. Default Value: 0
2 : 0	EVENT_LEVEL	Event level. When the number of entries in the instruction FIFO is less than the amount of this field, an event is generated: - "event" = INSTR_FF_STATUS.USED < EVENT_LEVEL. Default Value: 0

CRYPTO_INSTR_FF_STATUS

Instruction FIFO status
Address: 0x40101044
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				USED [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							W
Name	None [23:17]							EVENT

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	EVENT	Instruction FIFO event. Default Value: 0
3 : 0	USED	Number of instructions in the instruction FIFO. The value of this field ranges from 0 to 8. Default Value: 0

CRYPTO_INSTR_FF_WR

Instruction FIFO write
Address: 0x40101048
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Instruction or instruction operand data that is written to the instruction FIFO. Default Value: 0

CRYPTO_LOAD0_FF_STATUS

Load 0 FIFO status
Address: 0x401010C0
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			USED5 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	BUSY	None [30:24]						

Bits	Name	Description
31	BUSY	Reflects the state of the FIFO: '0': FIFO load engine is idle and a new FIFO instruction can be accepted. '1': FIFO load engine is busy and NO new FIFO instruction can be accepted. Default Value: 0
4 : 0	USED5	Number of Bytes in the FIFO. The value of this field is in the range [0, 19]. Default Value: 0

CRYPTO_LOAD1_FF_STATUS

Load 1 FIFO status
Address: 0x401010D0
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			USED5 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	BUSY	None [30:24]						

Bits	Name	Description
31	BUSY	See LOAD1_FF_STATUS.BUSY. Default Value: 0
4 : 0	USED5	See LOAD1_FF_STATUS.USED. Default Value: 0

CRYPTO_STORE_FF_STATUS

Store FIFO status
Address: 0x401010F0
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			USED5 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	BUSY	None [30:24]						

Bits	Name	Description
31	BUSY	Reflects the state of the FIFO: '0': FIFO store engine is idle and a new FIFO instruction can be accepted (USED is "0"). '1': FIFO store engine is busy and NO new FIFO instruction can be accepted. Default Value: 0
4 : 0	USED5	Number of Bytes in the FIFO. The value of this field is in the range [0, 16]. Default Value: 0

CRYPTO_AES_CTL

AES control
Address: 0x40101100
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						KEY_SIZE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	KEY_SIZE	AES key size: "0": 128-bit key, 10 rounds AES (inverse) cipher operation. "1": 192-bit key, 12 rounds AES (inverse) cipher operation. "2": 256-bit key, 14 rounds AES (inverse) cipher operation. "3": Undefined Default Value: 0
		0x0: AES128 :
		0x1: AES192 :
		0x2: AES256 :

CRYPTO_RESULT

Result
Address: 0x40101180
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	BLOCK_CMP operation (DATA[0]): "0": source 0 equals source 1. "1": source 0 does NOT equal source 1. CRC operation (DATA[31:0]). State of a 32-bit Linear Feedback Shift Registers (LFSR) that is used to implement CRC. This register needs to be initialized by SW to provide the CRC seed value. The seed value should be aligned such that the more significant bits (bit 31 and down) contain the seed value and the less significant bits (bit 0 and up) contain padding '0's. Note that SW can write this field. This functionality can be used prevent information leakage. Default Value: 0

CRYPTO_CRC_CTL

CRC control
Address: 0x40101400
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							DATA_REVERSE

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							REM_REVERSE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	REM_REVERSE	Specifies whether the remainder is bit reversed (reversal is performed after XORing): '0': No. '1': Yes. Default Value: 0
0	DATA_REVERSE	Specifies the bit order in which a data Byte is processed (reversal is performed after XORing): '0': Most significant bit (bit 1) first. '1': Least significant bit (bit 0) first. Default Value: 0

CRYPTO_CRC_DATA_CTL

CRC data control
Address: 0x40101410
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA_XOR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA_XOR	Specifies a byte mask with which each data byte is XOR'd. The XOR is performed before data reversal. Default Value: 0

CRYPTO_CRC_POL_CTL

CRC polynomial control
Address: 0x40101420
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [31:24]							

Bits	Name	Description
31 : 0	POLYNOMIAL	CRC polynomial. The polynomial is represented WITHOUT the high order bit (this bit is always assumed '1'). The polynomial should be aligned/shifted such that the more significant bits (bit 31 and down) contain the polynomial and the less significant bits (bit 0 and up) contain padding '0's. Some frequently used polynomials: - CRC32: POLYNOMIAL is 0x04c11db7 (x^32 + x^26 + x^23 + x^22 + x^16 + x^12 + x^11 + x^10 + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1). - CRC16: POLYNOMIAL is 0x80050000 (x^16 + x^15 + x^2 + 1, shifted by 16 bit positions). - CRC16 CCITT: POLYNOMIAL is 0x10210000 (x^16 + x^12 + x^5 + 1, shifted by 16 bit positions). Default Value: 0

CRYPTO_CRC_REM_CTL

CRC remainder control
Address: 0x40101440
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	REM_XOR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	REM_XOR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	REM_XOR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	REM_XOR [31:24]							

Bits	Name	Description
31 : 0	REM_XOR	Specifies a mask with which the CRC_LFSR_CTL.LFSR32 register is XOR'd to produce a remainder. The XOR is performed before remainder reversal. Default Value: 0

CRYPTO_CRC_REM_RESULT

CRC remainder result
Address: 0x40101448
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	REM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	REM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	REM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	REM [31:24]							

Bits	Name	Description
31 : 0	REM	Remainder value. The alignment of the remainder depends on CRC_REM_CTL0.REM_REVERSE: '0': the more significant bits (bit 31 and down) contain the remainder. '1': the less significant bits (bit 0 and up) contain the remainder. Note: This field is combinatorially derived from CRC_LFSR_CTL.LFSR32, CRC_REM_CTL0.REM_REVERSE and CRC_REM_CTL1.REM_XOR. Default Value: 0

CRYPTO_VU_CTL0

Vector unit control 0
Address: 0x40101480
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							ALWAYS_EXECUTE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	ALWAYS_EXECUTE	Specifies if a conditional instruction is executed or not, when its condition code evaluates to false/'0'. '0': The instruction is NOT executed. As a result, the instruction may be handled faster than when it is executed. '1': The instruction is executed, but the execution result (including status field information) is not reflected in the IP. The instruction is handled just as fast as when it is executed. Note: a conditional instruction with a condition code that evaluates to false/'0' does not affect the architectural state: VU_STATUS fields, memory or register-file data. Note: Always execution is useful to prevent/ complicate differential timing and differential power attacks. Default Value: 0

CRYPTO_VU_CTL1

Vector unit control 1
Address: 0x40101484
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description

31 : 8	ADDR24	Specifies the memory address for the vector unit operand memory region. The register-file registers provide 13-bit word offsets within this memory region. Given ADDR[31:8], VU_VTL2.MASK[14:8] and a 13-bit word offset offset[14:2], a vector operand memory address VU_OPERAND_ADDR[31:0] is calculated as follows: - VU_OPERAND_ADDR[31:15] = ADDR[31:15] - VU_OPERAND_ADDR[14:8] = (ADDR[14:8] & MASK[14:8]) | (offset[14:8] & ~MASK[14:8]) - VU_OPERAND_ADDR[7:2] = offset[7:2] - VU_OPERAND_ADDR[1:0] = 0 (always word aligned) The vector unit operand memory region uses either the IP's memory buffer or system memory. For best performance, the IP's memory buffer should be used and ADDR should be set to MEM_BUFF and MASK should specify the IP memory buffer size. If a vector operand memory address is mapped on a memory hole, read accesses return a "0" and write accesses are ignored. Note: The base address of the IP internal memory buffer is equal to IP_ADDR + MEM_BUFF where. - IP_ADDR is the top-level design time parameter. - MEM_BUFF is address offset value for MEM_BUFF MMIO register. Default Value: 0

CRYPTO_VU_CTL2

Vector unit control 2
Address: 0x40101488
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None	MASK [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14 : 8	MASK	Specifies the size of the vector operand memory region. Legal values: "0b0000000": 32 KB memory region (VU_VTL1.ADDR[14:8] ignored). "0b1000000": 16 KB memory region (VU_VTL1.ADDR[13:8] ignored). "0b1100000": 8 KB memory region (VU_VTL1.ADDR[12:8] ignored). "0b1110000": 4 KB memory region (VU_VTL1.ADDR[11:8] ignored). "0b1111000": 2 KB memory region (VU_VTL1.ADDR[10:8] ignored). "0b1111100": 1 KB memory region (VU_VTL1.ADDR[9:8] ignored). "0b1111110": 512 B memory region (VU_VTL1.ADDR[8] ignored). "0b1111111": 256 B memory region. Note: the default specifies a 256 B memory region. Default Value: 0x7F

CRYPTO_VU_STATUS

Vector unit status
Address: 0x40101490
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				ONE	ZERO	EVEN	CARRY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	ONE	STATUS ONE field. Default Value: 0
2	ZERO	STATUS ZERO field. Default Value: 0
1	EVEN	STATUS EVEN field. Default Value: 0
0	CARRY	STATUS CARRY field. Default Value: 0

CRYPTO_VU_RF_DATA0

Vector unit register-file
Address: 0x401014C0
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Vector unit register-file data. A register-file register has the following layout: DATA[28:16]: data (typically used as a word offset in vector unit operand memory). DATA[12:0]: bit size minus 1. Default Value: 0

CRYPTO_DEV_KEY_ADDR0_CTL

Device key address 0 control
Address: 0x40102000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	Specifies if the address in the associated DEV_KEY_ADDR0 is valid: '0': Address not valid; i.e. no device key specified. '1': Address valid; i.e. device key specified. Note: A LOAD_DEV_KEY instruction requires that the device key's valid field is '1'. Default Value: 0

CRYPTO_DEV_KEY_ADDR0

Device key address 0
Address: 0x40102004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR32 [31:24]							

Bits	Name	Description
31 : 0	ADDR32	Specifies the memory address of the device key in memory. A LOAD_DEV_KEY instruction uses this address to load a device key from memory into the IP register buffer blocks 4 and 5. Default Value: 0

CRYPTO_DEV_KEY_ADDR1_CTL

Device key address 1 control
Address: 0x40102020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See DEV_KEY_ADDR0_CTL. Default Value: 0

CRYPTO_DEV_KEY_ADDR1

Device key address 1 control
Address: 0x40102024
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR32 [31:24]							

Bits	Name	Description
31 : 0	ADDR32	See DEV_KEY_ADDR0. Default Value: 0

CRYPTO_DEV_KEY_STATUS

Device key status
Address: 0x40102080
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							LOADED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	LOADED	Specifies if a device key is present in the IP register buffer blocks 4 and 5. HW sets this field to '1' on successful completion of a LOAD_DEV_KEY instruction. HW clears this field to '0' when a CLEAR instruction is executed (the CLEAR instruction also sets the IP register buffer to "0"). Default Value: 0

CRYPTO_DEV_KEY_CTL0

Device key control 0
Address: 0x40102100
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							ALLOWED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	ALLOWED	Specifies if a LOAD_DEV_KEY instruction is allowed to use the device key in memory: '0': Not allowed. '1': Allowed. Note: For successful completion of a LOAD_DEV_KEY instruction, both the associated DEV_KEY_ADDR_CTL.VALID and DEV_KEY_CTL.ALLOWED fields must be '1'. On successful instruction completion, DEV_KEY_STATUS.LOADED is set to '1'. On unsuccessful completion, the instruction FIFO is cleared and the IP is locked; an Active reset or an IP reset (CTL.ENABLED), which reinitializes the IP, is required. Note: A LOAD_DEV_KEY loads the device key from memory with protection context "0". Default Value: 0

CRYPTO_DEV_KEY_CTL1

Device key control 1
Address: 0x40102120
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							ALLOWED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	ALLOWED	See DEV_KEY_CTL0. Default Value: 0

CRYPTO_MEM_BUFF0

Memory buffer
Address: 0x40108000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: Undefined

16 Event generator (EVTGEN)

Register details

Register name	Address	Description
EVTGEN0_CTL	0x403F0000	Control
EVTGEN0_COMP0_STATUS	0x403F0004	Comparator structures comparator 0 status
EVTGEN0_COMP1_STATUS	0x403F0008	Comparator structures comparator 1 status
EVTGEN0_COUNTER_STATUS	0x403F0010	Counter status
EVTGEN0_COUNTER	0x403F0014	Counter
EVTGEN0_RATIO_CTL	0x403F0020	Ratio control
EVTGEN0_RATIO	0x403F0024	Ratio
EVTGEN0_REF_CLOCK_CTL	0x403F0030	Reference clock control
EVTGEN0_INTR	0x403F0700	Interrupt
EVTGEN0_INTR_SET	0x403F0704	Interrupt set
EVTGEN0_INTR_MASK	0x403F0708	Interrupt mask
EVTGEN0_INTR_MASKED	0x403F070C	Interrupt masked
EVTGEN0_INTR_DPSLP	0x403F0710	DeepSleep interrupt
EVTGEN0_INTR_DPSLP_SET	0x403F0714	DeepSleep interrupt set
EVTGEN0_INTR_DPSLP_MASK	0x403F0718	DeepSleep interrupt mask
EVTGEN0_INTR_DPSLP_MASKED	0x403F071C	DeepSleep interrupt masked
EVTGEN0_COMP_STRUCT0_COMP_CTL	0x403F0800	Comparator control
EVTGEN0_COMP_STRUCT0_COMP0	0x403F0804	Comparator 0 (Active functionality)
EVTGEN0_COMP_STRUCT0_COMP1	0x403F0808	Comparator 1 (DeepSleep functionality)
EVTGEN0_COMP_STRUCT1_COMP_CTL	0x403F0820	Comparator control. See EVTGEN0_COMP_STRUCT0_COMP_CTL for the details of bit fields.
EVTGEN0_COMP_STRUCT1_COMP0	0x403F0824	Comparator 0 (Active functionality). See EVTGEN0_COMP_STRUCT0_COMP0 for the details of bit fields.
EVTGEN0_COMP_STRUCT1_COMP1	0x403F0828	Comparator 1 (DeepSleep functionality). See EVTGEN0_COMP_STRUCT0_COMP1 for the details of bit fields.
EVTGEN0_COMP_STRUCT2_COMP_CTL	0x403F0840	Comparator control. See EVTGEN0_COMP_STRUCT0_COMP_CTL for the details of bit fields.
EVTGEN0_COMP_STRUCT2_COMP0	0x403F0844	Comparator 0 (Active functionality). See EVTGEN0_COMP_STRUCT0_COMP0 for the details of bit fields.
EVTGEN0_COMP_STRUCT2_COMP1	0x403F0848	Comparator 1 (DeepSleep functionality). See EVTGEN0_COMP_STRUCT0_COMP1 for the details of bit fields.

Register name	Address	Description
EVTGEN0_COMP_STRUCT3_COMP_CTL	0x403F0860	Comparator control. See EVTGEN0_COMP_STRUCT0_COMP_CTL for the details of bit fields.
EVTGEN0_COMP_STRUCT3_COMP0	0x403F0864	Comparator 0 (Active functionality). See EVTGEN0_COMP_STRUCT0_COMP0 for the details of bit fields.
EVTGEN0_COMP_STRUCT3_COMP1	0x403F0868	Comparator 1 (DeepSleep functionality). See EVTGEN0_COMP_STRUCT0_COMP1 for the details of bit fields.
EVTGEN0_COMP_STRUCT4_COMP_CTL	0x403F0880	Comparator control. See EVTGEN0_COMP_STRUCT0_COMP_CTL for the details of bit fields.
EVTGEN0_COMP_STRUCT4_COMP0	0x403F0884	Comparator 0 (Active functionality). See EVTGEN0_COMP_STRUCT0_COMP0 for the details of bit fields.
EVTGEN0_COMP_STRUCT4_COMP1	0x403F0888	Comparator 1 (DeepSleep functionality). See EVTGEN0_COMP_STRUCT0_COMP1 for the details of bit fields.
EVTGEN0_COMP_STRUCT5_COMP_CTL	0x403F08A0	Comparator control. See EVTGEN0_COMP_STRUCT0_COMP_CTL for the details of bit fields.
EVTGEN0_COMP_STRUCT5_COMP0	0x403F08A4	Comparator 0 (Active functionality). See EVTGEN0_COMP_STRUCT0_COMP0 for the details of bit fields.
EVTGEN0_COMP_STRUCT5_COMP1	0x403F08A8	Comparator 1 (DeepSleep functionality). See EVTGEN0_COMP_STRUCT0_COMP1 for the details of bit fields.
EVTGEN0_COMP_STRUCT6_COMP_CTL	0x403F08C0	Comparator control. See EVTGEN0_COMP_STRUCT0_COMP_CTL for the details of bit fields.
EVTGEN0_COMP_STRUCT6_COMP0	0x403F08C4	Comparator 0 (Active functionality). See EVTGEN0_COMP_STRUCT0_COMP0 for the details of bit fields.
EVTGEN0_COMP_STRUCT6_COMP1	0x403F08C8	Comparator 1 (DeepSleep functionality). See EVTGEN0_COMP_STRUCT0_COMP1 for the details of bit fields.
EVTGEN0_COMP_STRUCT7_COMP_CTL	0x403F08E0	Comparator control. See EVTGEN0_COMP_STRUCT0_COMP_CTL for the details of bit fields.
EVTGEN0_COMP_STRUCT7_COMP0	0x403F08E4	Comparator 0 (Active functionality). See EVTGEN0_COMP_STRUCT0_COMP0 for the details of bit fields.
EVTGEN0_COMP_STRUCT7_COMP1	0x403F08E8	Comparator 1 (DeepSleep functionality). See EVTGEN0_COMP_STRUCT0_COMP1 for the details of bit fields.
EVTGEN0_COMP_STRUCT8_COMP_CTL	0x403F0900	Comparator control. See EVTGEN0_COMP_STRUCT0_COMP_CTL for the details of bit fields.

Register name	Address	Description
EVTGEN0_COMP_STRUCT8_COMP0	0x403F0904	Comparator 0 (Active functionality). See EVTGEN0_COMP_STRUCT0_COMP0 for the details of bit fields.
EVTGEN0_COMP_STRUCT8_COMP1	0x403F0908	Comparator 1 (DeepSleep functionality). See EVTGEN0_COMP_STRUCT0_COMP1 for the details of bit fields.
EVTGEN0_COMP_STRUCT9_COMP_CTL	0x403F0920	Comparator control. See EVTGEN0_COMP_STRUCT0_COMP_CTL for the details of bit fields.
EVTGEN0_COMP_STRUCT9_COMP0	0x403F0924	Comparator 0 (Active functionality). See EVTGEN0_COMP_STRUCT0_COMP0 for the details of bit fields.
EVTGEN0_COMP_STRUCT9_COMP1	0x403F0928	Comparator 1 (DeepSleep functionality). See EVTGEN0_COMP_STRUCT0_COMP1 for the details of bit fields.
EVTGEN0_COMP_STRUCT10_COMP_CTL	0x403F0940	Comparator control. See EVTGEN0_COMP_STRUCT0_COMP_CTL for the details of bit fields.
EVTGEN0_COMP_STRUCT10_COMP0	0x403F0944	Comparator 0 (Active functionality). See EVTGEN0_COMP_STRUCT0_COMP0 for the details of bit fields.
EVTGEN0_COMP_STRUCT10_COMP1	0x403F0948	Comparator 1 (DeepSleep functionality). See EVTGEN0_COMP_STRUCT0_COMP1 for the details of bit fields.

16.1 EVTGEN registers

EVTGEN0_CTL

Control

Address: 0x403F0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	IP enable: '0': Disabled. All non-retention registers (command and status registers) are reset to their default value when the IP is disabled. All retention registers retain their value when the IP is disabled. '1': Enabled. Default Value: 0
		0x0: DISABLED :
		0x1: ENABLED :

EVTGEN0_COMP0_STATUS

Comparator structures comparator 0 status
Address: 0x403F0004
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	COMP0_OUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None	R						
HW Access	None	W						
Name	None [15:11]	COMP0_OUT [10:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 0	COMP0_OUT	Active comparator "comp0_out[]" outputs. Default Value: 0

EVTGEN0_COMP1_STATUS

Comparator structures comparator 1 status
Address: 0x403F0008
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	COMP1_OUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None	R						
HW Access	None	W						
Name	None [15:11]	COMP1_OUT [10:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 0	COMP1_OUT	DeepSleep comparator "comp1_out_lf[]" outputs (synchronized from clk_lf to the IP clock). Default Value: 0

EVTGEN0_COUNTER_STATUS

Counter status
Address: 0x403F0010
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	Active counter validity: '0': Invalid. '1': Valid. The COUNTER register field INT32 is only valid when VALID is '1'. The COUNTER_STATUS and COUNTER registers are non-retention registers; i.e. the COUNTER_STATUS and COUNTER registers are reset during DeepSleep power mode. After entering the Active power mode, the Active counter is initialized with the DeepSleep counter. This initialization may take up to 1 clk_lf cycle. Default Value: 0

EVTGEN0_COUNTER

Counter
Address: 0x403F0014
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	INT32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	INT32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	INT32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							

Bits	31	30	29	28	27	26	25	24
Name	INT32 [31:24]							

Bits	Name	Description
31 : 0	INT32	Active counter "counter_int[31:0]" on clk_ref_div. Default Value: Undefined

EVTGEN0_RATIO_CTL

Ratio control
Address: 0x403F0020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None [23:19]	DYNAMIC_MODE [18:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	RW1S	R	None					
Name	VALID	DYNAMIC	None [29:24]					

Bits	Name	Description
31	VALID	Ratio value valid: '0': Invalid. '1': Valid. The RATIO register fields INT16 and FRAC8 are only valid when VALID is '1'. Default Value: 0
30	DYNAMIC	Specifies if RATIO_CTL.VALID and RATIO are under SW or HW control: '0': SW control. '1: HW control. Auto calibration is used to derive the RATIO value. HW measures the number of clk_ref_div cycles per clk_lf cycle. This measurement is combined with the current ratio value to calculate a new ratio value. Default Value: 0

18 : 16	DYNAMIC_MODE	Weighted average calculation (only used when DYNAMIC is '1'): "0": new RATIO value = (RATIO + measurement + 1) / 2. "1": new RATIO value = (3*RATIO + measurement + 2) / 4. "2": new RATIO value = (7*RATIO + measurement + 4) / 8. "3": new RATIO value = (15*RATIO + measurement + 8) / 16. "4": new RATIO value = (31*RATIO + measurement + 16) / 32. "5": new RATIO value = (63*RATIO + measurement + 32) / 64. "6": new RATIO value = (127*RATIO + measurement + 64) / 128. "7": new RATIO value = (255*RATIO + measurement + 128) / 256. Note: "measurement" (integer component only) is defined as: 256 * "number of measured clk_ref_div cycles per clk_lf cycle". The RATIO value (integer and fractional component) is defined as: 256*RATIO.INT16 + RATIO.FRAC8 (RATIO.INT16 = RATIO >> 8 and RATIO.FRAC8 = RATIO % 256). Default Value: 0

EVTGEN0_RATIO

Ratio

Address: 0x403F0024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	FRAC8 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	INT16 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							

Bits	31	30	29	28	27	26	25	24
Name	INT16 [31:24]							

Bits	Name	Description
31 : 16	INT16	Integer component of ratio value. Default Value: Undefined
15 : 8	FRAC8	Fractional component of ratio value. Default Value: Undefined

EVTGEN0_REF_CLOCK_CTL

Reference clock control
Address: 0x403F0030
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	INT_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	INT_DIV	Divider control for clk_ref_div: "0": Divide by 1. ... "255": Divide by "256". Fclk_ref_div = Fclk_ref / (INT_DIV + 1) Default Value: 0

EVTGEN0_INTR

Interrupt
Address: 0x403F0700
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							

Bits	7	6	5	4	3	2	1	0
Name	COMP0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1C						
HW Access	None	RW1S						
Name	None [15:11]	COMP0 [10:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 0	COMP0	This interrupt cause field is activated (HW sets the field to '1') when a comparator 0 event is generated (Active counter "counter_int[31:0]" becomes greater or equal to COMP0.INT[31:0]). Default Value: 0

EVTGEN0_INTR_SET

Interrupt set
Address: 0x403F0704
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	COMP0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1S						
HW Access	None	A						
Name	None [15:11]	COMP0 [10:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 0	COMP0	SW writes a '1' to this field to set the corresponding field in the INTR register. Default Value: 0

EVTGEN0_INTR_MASK

Interrupt mask
Address: 0x403F0708
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COMP0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None [15:11]	COMP0 [10:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 0	COMP0	Mask bit for corresponding field in the INTR register. Default Value: 0

EVTGEN0_INTR_MASKED

Interrupt masked
Address: 0x403F070C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							

Bits	7	6	5	4	3	2	1	0
HW Access	W							
Name	COMP0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None	R						
HW Access	None	W						
Name	None [15:11]	COMP0 [10:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 0	COMP0	Logical and of corresponding INTR and INTR_MASK fields. Default Value: 0

EVTGEN0_INTR_DPSLP

DeepSleep interrupt
Address: 0x403F0710
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	A							
Name	COMP1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1C						
HW Access	None	A						
Name	None [15:11]	COMP1 [10:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 0	COMP1	This interrupt cause field is activated (HW sets the field to '1') when a comparator 1 event is generated (DeepSleep counter "counter_int_lf[31:0]" becomes greater or equal to COMP1.INT[31:0]). Default Value: 0

EVTGEN0_INTR_DPSLP_SET

DeepSleep interrupt set
Address: 0x403F0714
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	COMP1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1S						
HW Access	None	A						
Name	None [15:11]	COMP1 [10:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 0	COMP1	SW writes a '1' to this field to set the corresponding field in the INTR register. Default Value: 0

EVTGEN0_INTR_DPSLP_MASK

DeepSleep interrupt mask
Address: 0x403F0718

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COMP1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None [15:11]	COMP1 [10:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 0	COMP1	Mask bit for corresponding field in the INTR register. Default Value: 0

EVTGEN0_INTR_DPSLP_MASKED

DeepSleep interrupt masked
Address: 0x403F071C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	COMP1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None	R						
HW Access	None	W						
Name	None [15:11]	COMP1 [10:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 0	COMP1	Logical and of corresponding INTR and INTR_MASK fields. Default Value: 0

EVTGEN0_COMP_STRUCT0_COMP_CTL

Comparator control
Address: 0x403F0800
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW					
HW Access	None	R	R					
Name	None [7:2]	COMP1_EN	COMP0_EN					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None [23:17]	TR_OUT_EDGE						

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	Comparator structure enable: '0': Disabled. '1': Enabled. Default Value: 0

16	TR_OUT_EDGE	Specifies the "tr_out" output trigger: '0': The trigger is a level sensitive trigger. The Active comparator output ("comp0_out") is reflected on "tr_out". '1': The trigger is an edge sensitive trigger. Activation of the Active comparator output (rising edge on "comp0_out") results in a two cycle '1'/high pulse on "tr_out". Default Value: 0
1	COMP1_EN	DeepSleep comparator (COMP1) enable: '0': Disabled. The comparator output "comp1_out_lf" is '0'. '1': Enabled. Default Value: 0
0	COMP0_EN	Active comparator (COMP0) enable: '0': Disabled. The comparator output "comp0_out" is '0'. '1': Enabled. Default Value: 0

EVTGEN0_COMP_STRUCT0_COMP0

Comparator 0 (Active functionality)
Address: 0x403F0804
Retention: Retained

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SW Access	RW							
HW Access	R							
Name	INT32 [7:0]							
Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	RW							
HW Access	R							
Name	INT32 [15:8]							
Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	RW							
HW Access	R							
Name	INT32 [23:16]							
Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	RW							
HW Access	R							
Name	INT32 [31:24]							

Bits	**Name**	**Description**

31 : 0	INT32	This value is a 32-bit unsigned integer in the range [0, 2^32-1]. The comparator "comp0_out" output is activated when the Active counter "counter_int[31:0]" becomes greater or equal to COMP0. Note: SW must ensure that COMP_CTL.COMP_EN[0] is '0' when COMP0 is written. Default Value: Undefined

EVTGEN0_COMP_STRUCT0_COMP1

Comparator 1 (DeepSleep functionality)
Address: 0x403F0808
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	INT32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	INT32 [31:24]							

Bits	Name	Description
31 : 0	INT32	This value is a 32-bit unsigned integer in the range [0, 2^32-1]. The comparator "comp1_out_lf" output is activated when the DeepSleep counter "counter_int_lf[31:0]" becomes greater or equal to COMP1. Note: SW must ensure that COMP_CTL.COMP_EN[1] is '0' when COMP1 is written. Default Value: Undefined

17 Programmable analog subsystem (PASS)

Register details

Register name	Address	Description
PASS0_SAR0_CTL	0x40900000	Analog control register.
PASS0_SAR0_DIAG_CTL	0x40900004	Diagnostic Reference control register.
PASS0_SAR0_PRECOND_CTL	0x40900010	Preconditioning control register.
PASS0_SAR0_ANA_CAL	0x40900080	Current analog calibration values
PASS0_SAR0_DIG_CAL	0x40900084	Current digital calibration values
PASS0_SAR0_ANA_CAL_ALT	0x40900090	Alternate analog calibration values
PASS0_SAR0_DIG_CAL_ALT	0x40900094	Alternate digital calibration values
PASS0_SAR0_CAL_UPD_CMD	0x40900098	Calibration update command
PASS0_SAR0_TR_PEND	0x40900100	Trigger pending status
PASS0_SAR0_WORK_VALID	0x40900180	Channel working data register 'valid' bits
PASS0_SAR0_WORK_RANGE	0x40900184	Range detected
PASS0_SAR0_WORK_RANGE_HI	0x40900188	Range detect above Hi flag
PASS0_SAR0_WORK_PULSE	0x4090018C	Pulse detected
PASS0_SAR0_RESULT_VALID	0x409001A0	Channel result data register 'valid' bits
PASS0_SAR0_RESULT_RANGE_HI	0x409001A4	Channel Range above Hi flags
PASS0_SAR0_STATUS	0x40900200	Current status of internal SAR registers (mostly for debug)
PASS0_SAR0_AVG_STAT	0x40900204	Current averaging status (for debug)
PASS0_SAR0_CH0_TR_CTL	0x40900800	Trigger control.
PASS0_SAR0_CH0_SAMPLE_CTL	0x40900804	Sample control.
PASS0_SAR0_CH0_POST_CTL	0x40900808	Post processing control
PASS0_SAR0_CH0_RANGE_CTL	0x4090080C	Range thresholds
PASS0_SAR0_CH0_INTR	0x40900810	Interrupt request register.
PASS0_SAR0_CH0_INTR_SET	0x40900814	Interrupt set request register
PASS0_SAR0_CH0_INTR_MASK	0x40900818	Interrupt mask register.
PASS0_SAR0_CH0_INTR_MASKED	0x4090081C	Interrupt masked request register
PASS0_SAR0_CH0_WORK	0x40900820	Working data register
PASS0_SAR0_CH0_RESULT	0x40900824	Result data register
PASS0_SAR0_CH0_GRP_STAT	0x40900828	Group status register
PASS0_SAR0_CH0_ENABLE	0x40900838	Enable register
PASS0_SAR0_CH0_TR_CMD	0x4090083C	Software triggers
PASS0_SAR0_CH1_TR_CTL	0x40900840	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR0_CH1_SAMPLE_CTL	0x40900844	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.

Register name	Address	Description
PASS0_SAR0_CH1_POST_CTL	0x40900848	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR0_CH1_RANGE_CTL	0x4090084C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR0_CH1_INTR	0x40900850	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR0_CH1_INTR_SET	0x40900854	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR0_CH1_INTR_MASK	0x40900858	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR0_CH1_INTR_MASKED	0x4090085C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR0_CH1_WORK	0x40900860	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR0_CH1_RESULT	0x40900864	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR0_CH1_GRP_STAT	0x40900868	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR0_CH1_ENABLE	0x40900878	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR0_CH1_TR_CMD	0x4090087C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR0_CH2_TR_CTL	0x40900880	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR0_CH2_SAMPLE_CTL	0x40900884	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR0_CH2_POST_CTL	0x40900888	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR0_CH2_RANGE_CTL	0x4090088C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR0_CH2_INTR	0x40900890	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR0_CH2_INTR_SET	0x40900894	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR0_CH2_INTR_MASK	0x40900898	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR0_CH2_INTR_MASKED	0x4090089C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
PASS0_SAR0_CH2_WORK	0x409008A0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR0_CH2_RESULT	0x409008A4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR0_CH2_GRP_STAT	0x409008A8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR0_CH2_ENABLE	0x409008B8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR0_CH2_TR_CMD	0x409008BC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR0_CH3_TR_CTL	0x409008C0	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR0_CH3_SAMPLE_CTL	0x409008C4	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR0_CH3_POST_CTL	0x409008C8	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR0_CH3_RANGE_CTL	0x409008CC	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR0_CH3_INTR	0x409008D0	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR0_CH3_INTR_SET	0x409008D4	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR0_CH3_INTR_MASK	0x409008D8	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR0_CH3_INTR_MASKED	0x409008DC	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR0_CH3_WORK	0x409008E0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR0_CH3_RESULT	0x409008E4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR0_CH3_GRP_STAT	0x409008E8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR0_CH3_ENABLE	0x409008F8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR0_CH3_TR_CMD	0x409008FC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR0_CH4_TR_CTL	0x40900900	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR0_CH4_SAMPLE_CTL	0x40900904	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.

Register name	Address	Description
PASS0_SAR0_CH4_POST_CTL	0x40900908	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR0_CH4_RANGE_CTL	0x4090090C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR0_CH4_INTR	0x40900910	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR0_CH4_INTR_SET	0x40900914	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR0_CH4_INTR_MASK	0x40900918	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR0_CH4_INTR_MASKED	0x4090091C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR0_CH4_WORK	0x40900920	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR0_CH4_RESULT	0x40900924	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR0_CH4_GRP_STAT	0x40900928	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR0_CH4_ENABLE	0x40900938	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR0_CH4_TR_CMD	0x4090093C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR0_CH5_TR_CTL	0x40900940	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR0_CH5_SAMPLE_CTL	0x40900944	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR0_CH5_POST_CTL	0x40900948	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR0_CH5_RANGE_CTL	0x4090094C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR0_CH5_INTR	0x40900950	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR0_CH5_INTR_SET	0x40900954	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR0_CH5_INTR_MASK	0x40900958	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR0_CH5_INTR_MASKED	0x4090095C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
PASS0_SAR0_CH5_WORK	0x40900960	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR0_CH5_RESULT	0x40900964	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR0_CH5_GRP_STAT	0x40900968	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR0_CH5_ENABLE	0x40900978	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR0_CH5_TR_CMD	0x4090097C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR0_CH6_TR_CTL	0x40900980	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR0_CH6_SAMPLE_CTL	0x40900984	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR0_CH6_POST_CTL	0x40900988	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR0_CH6_RANGE_CTL	0x4090098C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR0_CH6_INTR	0x40900990	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR0_CH6_INTR_SET	0x40900994	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR0_CH6_INTR_MASK	0x40900998	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR0_CH6_INTR_MASKED	0x4090099C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR0_CH6_WORK	0x409009A0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR0_CH6_RESULT	0x409009A4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR0_CH6_GRP_STAT	0x409009A8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR0_CH6_ENABLE	0x409009B8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR0_CH6_TR_CMD	0x409009BC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR0_CH7_TR_CTL	0x409009C0	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR0_CH7_SAMPLE_CTL	0x409009C4	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.

Register name	Address	Description
PASS0_SAR0_CH7_POST_CTL	0x409009C8	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR0_CH7_RANGE_CTL	0x409009CC	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR0_CH7_INTR	0x409009D0	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR0_CH7_INTR_SET	0x409009D4	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR0_CH7_INTR_MASK	0x409009D8	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR0_CH7_INTR_MASKED	0x409009DC	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR0_CH7_WORK	0x409009E0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR0_CH7_RESULT	0x409009E4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR0_CH7_GRP_STAT	0x409009E8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR0_CH7_ENABLE	0x409009F8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR0_CH7_TR_CMD	0x409009FC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR0_CH8_TR_CTL	0x40900A00	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR0_CH8_SAMPLE_CTL	0x40900A04	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR0_CH8_POST_CTL	0x40900A08	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR0_CH8_RANGE_CTL	0x40900A0C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR0_CH8_INTR	0x40900A10	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR0_CH8_INTR_SET	0x40900A14	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR0_CH8_INTR_MASK	0x40900A18	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR0_CH8_INTR_MASKED	0x40900A1C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
PASS0_SAR0_CH8_WORK	0x40900A20	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR0_CH8_RESULT	0x40900A24	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR0_CH8_GRP_STAT	0x40900A28	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR0_CH8_ENABLE	0x40900A38	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR0_CH8_TR_CMD	0x40900A3C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR0_CH9_TR_CTL	0x40900A40	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR0_CH9_SAMPLE_CTL	0x40900A44	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR0_CH9_POST_CTL	0x40900A48	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR0_CH9_RANGE_CTL	0x40900A4C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR0_CH9_INTR	0x40900A50	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR0_CH9_INTR_SET	0x40900A54	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR0_CH9_INTR_MASK	0x40900A58	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR0_CH9_INTR_MASKED	0x40900A5C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR0_CH9_WORK	0x40900A60	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR0_CH9_RESULT	0x40900A64	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR0_CH9_GRP_STAT	0x40900A68	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR0_CH9_ENABLE	0x40900A78	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR0_CH9_TR_CMD	0x40900A7C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR0_CH10_TR_CTL	0x40900A80	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR0_CH10_SAMPLE_CTL	0x40900A84	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.

Register name	Address	Description
PASS0_SAR0_CH10_POST_CTL	0x40900A88	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR0_CH10_RANGE_CTL	0x40900A8C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR0_CH10_INTR	0x40900A90	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR0_CH10_INTR_SET	0x40900A94	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR0_CH10_INTR_MASK	0x40900A98	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR0_CH10_INTR_MASKED	0x40900A9C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR0_CH10_WORK	0x40900AA0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR0_CH10_RESULT	0x40900AA4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR0_CH10_GRP_STAT	0x40900AA8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR0_CH10_ENABLE	0x40900AB8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR0_CH10_TR_CMD	0x40900ABC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR0_CH11_TR_CTL	0x40900AC0	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR0_CH11_SAMPLE_CTL	0x40900AC4	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR0_CH11_POST_CTL	0x40900AC8	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR0_CH11_RANGE_CTL	0x40900ACC	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR0_CH11_INTR	0x40900AD0	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR0_CH11_INTR_SET	0x40900AD4	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR0_CH11_INTR_MASK	0x40900AD8	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR0_CH11_INTR_MASKED	0x40900ADC	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
PASS0_SAR0_CH11_WORK	0x40900AE0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR0_CH11_RESULT	0x40900AE4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR0_CH11_GRP_STAT	0x40900AE8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR0_CH11_ENABLE	0x40900AF8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR0_CH11_TR_CMD	0x40900AFC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR0_CH12_TR_CTL	0x40900B00	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR0_CH12_SAMPLE_CTL	0x40900B04	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR0_CH12_POST_CTL	0x40900B08	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR0_CH12_RANGE_CTL	0x40900B0C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR0_CH12_INTR	0x40900B10	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR0_CH12_INTR_SET	0x40900B14	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR0_CH12_INTR_MASK	0x40900B18	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR0_CH12_INTR_MASKED	0x40900B1C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR0_CH12_WORK	0x40900B20	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR0_CH12_RESULT	0x40900B24	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR0_CH12_GRP_STAT	0x40900B28	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR0_CH12_ENABLE	0x40900B38	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR0_CH12_TR_CMD	0x40900B3C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR0_CH13_TR_CTL	0x40900B40	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR0_CH13_SAMPLE_CTL	0x40900B44	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.

Register name	Address	Description
PASS0_SAR0_CH13_POST_CTL	0x40900B48	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR0_CH13_RANGE_CTL	0x40900B4C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR0_CH13_INTR	0x40900B50	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR0_CH13_INTR_SET	0x40900B54	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR0_CH13_INTR_MASK	0x40900B58	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR0_CH13_INTR_MASKED	0x40900B5C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR0_CH13_WORK	0x40900B60	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR0_CH13_RESULT	0x40900B64	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR0_CH13_GRP_STAT	0x40900B68	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR0_CH13_ENABLE	0x40900B78	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR0_CH13_TR_CMD	0x40900B7C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR0_CH14_TR_CTL	0x40900B80	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR0_CH14_SAMPLE_CTL	0x40900B84	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR0_CH14_POST_CTL	0x40900B88	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR0_CH14_RANGE_CTL	0x40900B8C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR0_CH14_INTR	0x40900B90	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR0_CH14_INTR_SET	0x40900B94	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR0_CH14_INTR_MASK	0x40900B98	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR0_CH14_INTR_MASKED	0x40900B9C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
PASS0_SAR0_CH14_WORK	0x40900BA0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR0_CH14_RESULT	0x40900BA4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR0_CH14_GRP_STAT	0x40900BA8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR0_CH14_ENABLE	0x40900BB8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR0_CH14_TR_CMD	0x40900BBC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR0_CH15_TR_CTL	0x40900BC0	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR0_CH15_SAMPLE_CTL	0x40900BC4	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR0_CH15_POST_CTL	0x40900BC8	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR0_CH15_RANGE_CTL	0x40900BCC	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR0_CH15_INTR	0x40900BD0	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR0_CH15_INTR_SET	0x40900BD4	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR0_CH15_INTR_MASK	0x40900BD8	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR0_CH15_INTR_MASKED	0x40900BDC	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR0_CH15_WORK	0x40900BE0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR0_CH15_RESULT	0x40900BE4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR0_CH15_GRP_STAT	0x40900BE8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR0_CH15_ENABLE	0x40900BF8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR0_CH15_TR_CMD	0x40900BFC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR0_CH16_TR_CTL	0x40900C00	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR0_CH16_SAMPLE_CTL	0x40900C04	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.

Register name	Address	Description
PASS0_SAR0_CH16_POST_CTL	0x40900C08	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR0_CH16_RANGE_CTL	0x40900C0C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR0_CH16_INTR	0x40900C10	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR0_CH16_INTR_SET	0x40900C14	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR0_CH16_INTR_MASK	0x40900C18	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR0_CH16_INTR_MASKED	0x40900C1C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR0_CH16_WORK	0x40900C20	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR0_CH16_RESULT	0x40900C24	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR0_CH16_GRP_STAT	0x40900C28	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR0_CH16_ENABLE	0x40900C38	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR0_CH16_TR_CMD	0x40900C3C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR0_CH17_TR_CTL	0x40900C40	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR0_CH17_SAMPLE_CTL	0x40900C44	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR0_CH17_POST_CTL	0x40900C48	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR0_CH17_RANGE_CTL	0x40900C4C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR0_CH17_INTR	0x40900C50	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR0_CH17_INTR_SET	0x40900C54	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR0_CH17_INTR_MASK	0x40900C58	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR0_CH17_INTR_MASKED	0x40900C5C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
PASS0_SAR0_CH17_WORK	0x40900C60	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR0_CH17_RESULT	0x40900C64	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR0_CH17_GRP_STAT	0x40900C68	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR0_CH17_ENABLE	0x40900C78	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR0_CH17_TR_CMD	0x40900C7C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR0_CH18_TR_CTL	0x40900C80	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR0_CH18_SAMPLE_CTL	0x40900C84	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR0_CH18_POST_CTL	0x40900C88	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR0_CH18_RANGE_CTL	0x40900C8C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR0_CH18_INTR	0x40900C90	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR0_CH18_INTR_SET	0x40900C94	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR0_CH18_INTR_MASK	0x40900C98	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR0_CH18_INTR_MASKED	0x40900C9C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR0_CH18_WORK	0x40900CA0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR0_CH18_RESULT	0x40900CA4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR0_CH18_GRP_STAT	0x40900CA8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR0_CH18_ENABLE	0x40900CB8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR0_CH18_TR_CMD	0x40900CBC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR0_CH19_TR_CTL	0x40900CC0	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR0_CH19_SAMPLE_CTL	0x40900CC4	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.

Register name	Address	Description
PASS0_SAR0_CH19_POST_CTL	0x40900CC8	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR0_CH19_RANGE_CTL	0x40900CCC	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR0_CH19_INTR	0x40900CD0	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR0_CH19_INTR_SET	0x40900CD4	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR0_CH19_INTR_MASK	0x40900CD8	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR0_CH19_INTR_MASKED	0x40900CDC	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR0_CH19_WORK	0x40900CE0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR0_CH19_RESULT	0x40900CE4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR0_CH19_GRP_STAT	0x40900CE8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR0_CH19_ENABLE	0x40900CF8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR0_CH19_TR_CMD	0x40900CFC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR0_CH20_TR_CTL	0x40900D00	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR0_CH20_SAMPLE_CTL	0x40900D04	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR0_CH20_POST_CTL	0x40900D08	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR0_CH20_RANGE_CTL	0x40900D0C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR0_CH20_INTR	0x40900D10	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR0_CH20_INTR_SET	0x40900D14	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR0_CH20_INTR_MASK	0x40900D18	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR0_CH20_INTR_MASKED	0x40900D1C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
PASS0_SAR0_CH20_WORK	0x40900D20	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR0_CH20_RESULT	0x40900D24	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR0_CH20_GRP_STAT	0x40900D28	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR0_CH20_ENABLE	0x40900D38	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR0_CH20_TR_CMD	0x40900D3C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR0_CH21_TR_CTL	0x40900D40	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR0_CH21_SAMPLE_CTL	0x40900D44	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR0_CH21_POST_CTL	0x40900D48	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR0_CH21_RANGE_CTL	0x40900D4C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR0_CH21_INTR	0x40900D50	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR0_CH21_INTR_SET	0x40900D54	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR0_CH21_INTR_MASK	0x40900D58	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR0_CH21_INTR_MASKED	0x40900D5C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR0_CH21_WORK	0x40900D60	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR0_CH21_RESULT	0x40900D64	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR0_CH21_GRP_STAT	0x40900D68	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR0_CH21_ENABLE	0x40900D78	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR0_CH21_TR_CMD	0x40900D7C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR0_CH22_TR_CTL	0x40900D80	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR0_CH22_SAMPLE_CTL	0x40900D84	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.

Register name	Address	Description
PASS0_SAR0_CH22_POST_CTL	0x40900D88	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR0_CH22_RANGE_CTL	0x40900D8C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR0_CH22_INTR	0x40900D90	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR0_CH22_INTR_SET	0x40900D94	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR0_CH22_INTR_MASK	0x40900D98	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR0_CH22_INTR_MASKED	0x40900D9C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR0_CH22_WORK	0x40900DA0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR0_CH22_RESULT	0x40900DA4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR0_CH22_GRP_STAT	0x40900DA8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR0_CH22_ENABLE	0x40900DB8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR0_CH22_TR_CMD	0x40900DBC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR0_CH23_TR_CTL	0x40900DC0	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR0_CH23_SAMPLE_CTL	0x40900DC4	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR0_CH23_POST_CTL	0x40900DC8	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR0_CH23_RANGE_CTL	0x40900DCC	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR0_CH23_INTR	0x40900DD0	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR0_CH23_INTR_SET	0x40900DD4	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR0_CH23_INTR_MASK	0x40900DD8	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR0_CH23_INTR_MASKED	0x40900DDC	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
PASS0_SAR0_CH23_WORK	0x40900DE0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR0_CH23_RESULT	0x40900DE4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR0_CH23_GRP_STAT	0x40900DE8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR0_CH23_ENABLE	0x40900DF8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR0_CH23_TR_CMD	0x40900DFC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CTL	0x40901000	Analog control register.. See PASS0_SAR0_CTL for the details of bit fields.
PASS0_SAR1_DIAG_CTL	0x40901004	Diagnostic Reference control register.. See PASS0_SAR0_DIAG_CTL for the details of bit fields.
PASS0_SAR1_PRECOND_CTL	0x40901010	Preconditioning control register.. See PASS0_SAR0_PRECOND_CTL for the details of bit fields.
PASS0_SAR1_ANA_CAL	0x40901080	Current analog calibration values. See PASS0_SAR0_ANA_CAL for the details of bit fields.
PASS0_SAR1_DIG_CAL	0x40901084	Current digital calibration values. See PASS0_SAR0_DIG_CAL for the details of bit fields.
PASS0_SAR1_ANA_CAL_ALT	0x40901090	Alternate analog calibration values. See PASS0_SAR0_ANA_CAL_ALT for the details of bit fields.
PASS0_SAR1_DIG_CAL_ALT	0x40901094	Alternate digital calibration values. See PASS0_SAR0_DIG_CAL_ALT for the details of bit fields.
PASS0_SAR1_CAL_UPD_CMD	0x40901098	Calibration update command. See PASS0_SAR0_CAL_UPD_CMD for the details of bit fields.
PASS0_SAR1_TR_PEND	0x40901100	Trigger pending status
PASS0_SAR1_WORK_VALID	0x40901180	Channel working data register 'valid' bits
PASS0_SAR1_WORK_RANGE	0x40901184	Range detected
PASS0_SAR1_WORK_RANGE_HI	0x40901188	Range detect above Hi flag
PASS0_SAR1_WORK_PULSE	0x4090118C	Pulse detected
PASS0_SAR1_RESULT_VALID	0x409011A0	Channel result data register 'valid' bits
PASS0_SAR1_RESULT_RANGE_HI	0x409011A4	Channel Range above Hi flags
PASS0_SAR1_STATUS	0x40901200	Current status of internal SAR registers (mostly for debug). See PASS0_SAR0_STATUS for the details of bit fields.
PASS0_SAR1_AVG_STAT	0x40901204	Current averaging status (for debug). See PASS0_SAR0_AVG_STAT for the details of bit fields.
PASS0_SAR1_CH0_TR_CTL	0x40901800	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH0_SAMPLE_CTL	0x40901804	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.

Register name	Address	Description
PASS0_SAR1_CH0_POST_CTL	0x40901808	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH0_RANGE_CTL	0x4090180C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH0_INTR	0x40901810	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH0_INTR_SET	0x40901814	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH0_INTR_MASK	0x40901818	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH0_INTR_MASKED	0x4090181C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR1_CH0_WORK	0x40901820	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH0_RESULT	0x40901824	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH0_GRP_STAT	0x40901828	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH0_ENABLE	0x40901838	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH0_TR_CMD	0x4090183C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH1_TR_CTL	0x40901840	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH1_SAMPLE_CTL	0x40901844	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR1_CH1_POST_CTL	0x40901848	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH1_RANGE_CTL	0x4090184C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH1_INTR	0x40901850	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH1_INTR_SET	0x40901854	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH1_INTR_MASK	0x40901858	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH1_INTR_MASKED	0x4090185C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
PASS0_SAR1_CH1_WORK	0x40901860	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH1_RESULT	0x40901864	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH1_GRP_STAT	0x40901868	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH1_ENABLE	0x40901878	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH1_TR_CMD	0x4090187C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH2_TR_CTL	0x40901880	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH2_SAMPLE_CTL	0x40901884	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR1_CH2_POST_CTL	0x40901888	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH2_RANGE_CTL	0x4090188C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH2_INTR	0x40901890	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH2_INTR_SET	0x40901894	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH2_INTR_MASK	0x40901898	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH2_INTR_MASKED	0x4090189C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR1_CH2_WORK	0x409018A0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH2_RESULT	0x409018A4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH2_GRP_STAT	0x409018A8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH2_ENABLE	0x409018B8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH2_TR_CMD	0x409018BC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH3_TR_CTL	0x409018C0	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH3_SAMPLE_CTL	0x409018C4	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.

Register name	Address	Description
PASS0_SAR1_CH3_POST_CTL	0x409018C8	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH3_RANGE_CTL	0x409018CC	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH3_INTR	0x409018D0	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH3_INTR_SET	0x409018D4	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH3_INTR_MASK	0x409018D8	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH3_INTR_MASKED	0x409018DC	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR1_CH3_WORK	0x409018E0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH3_RESULT	0x409018E4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH3_GRP_STAT	0x409018E8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH3_ENABLE	0x409018F8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH3_TR_CMD	0x409018FC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH4_TR_CTL	0x40901900	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH4_SAMPLE_CTL	0x40901904	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR1_CH4_POST_CTL	0x40901908	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH4_RANGE_CTL	0x4090190C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH4_INTR	0x40901910	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH4_INTR_SET	0x40901914	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH4_INTR_MASK	0x40901918	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH4_INTR_MASKED	0x4090191C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
PASS0_SAR1_CH4_WORK	0x40901920	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH4_RESULT	0x40901924	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH4_GRP_STAT	0x40901928	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH4_ENABLE	0x40901938	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH4_TR_CMD	0x4090193C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH5_TR_CTL	0x40901940	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH5_SAMPLE_CTL	0x40901944	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR1_CH5_POST_CTL	0x40901948	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH5_RANGE_CTL	0x4090194C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH5_INTR	0x40901950	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH5_INTR_SET	0x40901954	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH5_INTR_MASK	0x40901958	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH5_INTR_MASKED	0x4090195C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR1_CH5_WORK	0x40901960	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH5_RESULT	0x40901964	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH5_GRP_STAT	0x40901968	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH5_ENABLE	0x40901978	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH5_TR_CMD	0x4090197C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH6_TR_CTL	0x40901980	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH6_SAMPLE_CTL	0x40901984	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.

Register name	Address	Description
PASS0_SAR1_CH6_POST_CTL	0x40901988	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH6_RANGE_CTL	0x4090198C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH6_INTR	0x40901990	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH6_INTR_SET	0x40901994	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH6_INTR_MASK	0x40901998	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH6_INTR_MASKED	0x4090199C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR1_CH6_WORK	0x409019A0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH6_RESULT	0x409019A4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH6_GRP_STAT	0x409019A8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH6_ENABLE	0x409019B8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH6_TR_CMD	0x409019BC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH7_TR_CTL	0x409019C0	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH7_SAMPLE_CTL	0x409019C4	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR1_CH7_POST_CTL	0x409019C8	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH7_RANGE_CTL	0x409019CC	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH7_INTR	0x409019D0	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH7_INTR_SET	0x409019D4	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH7_INTR_MASK	0x409019D8	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH7_INTR_MASKED	0x409019DC	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
PASS0_SAR1_CH7_WORK	0x409019E0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH7_RESULT	0x409019E4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH7_GRP_STAT	0x409019E8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH7_ENABLE	0x409019F8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH7_TR_CMD	0x409019FC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH8_TR_CTL	0x40901A00	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH8_SAMPLE_CTL	0x40901A04	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR1_CH8_POST_CTL	0x40901A08	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH8_RANGE_CTL	0x40901A0C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH8_INTR	0x40901A10	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH8_INTR_SET	0x40901A14	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH8_INTR_MASK	0x40901A18	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH8_INTR_MASKED	0x40901A1C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR1_CH8_WORK	0x40901A20	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH8_RESULT	0x40901A24	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH8_GRP_STAT	0x40901A28	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH8_ENABLE	0x40901A38	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH8_TR_CMD	0x40901A3C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH9_TR_CTL	0x40901A40	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH9_SAMPLE_CTL	0x40901A44	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.

Register name	Address	Description
PASS0_SAR1_CH9_POST_CTL	0x40901A48	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH9_RANGE_CTL	0x40901A4C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH9_INTR	0x40901A50	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH9_INTR_SET	0x40901A54	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH9_INTR_MASK	0x40901A58	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH9_INTR_MASKED	0x40901A5C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR1_CH9_WORK	0x40901A60	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH9_RESULT	0x40901A64	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH9_GRP_STAT	0x40901A68	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH9_ENABLE	0x40901A78	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH9_TR_CMD	0x40901A7C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH10_TR_CTL	0x40901A80	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH10_SAMPLE_CTL	0x40901A84	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR1_CH10_POST_CTL	0x40901A88	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH10_RANGE_CTL	0x40901A8C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH10_INTR	0x40901A90	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH10_INTR_SET	0x40901A94	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH10_INTR_MASK	0x40901A98	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH10_INTR_MASKED	0x40901A9C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
PASS0_SAR1_CH10_WORK	0x40901AA0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH10_RESULT	0x40901AA4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH10_GRP_STAT	0x40901AA8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH10_ENABLE	0x40901AB8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH10_TR_CMD	0x40901ABC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH11_TR_CTL	0x40901AC0	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH11_SAMPLE_CTL	0x40901AC4	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR1_CH11_POST_CTL	0x40901AC8	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH11_RANGE_CTL	0x40901ACC	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH11_INTR	0x40901AD0	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH11_INTR_SET	0x40901AD4	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH11_INTR_MASK	0x40901AD8	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH11_INTR_MASKED	0x40901ADC	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR1_CH11_WORK	0x40901AE0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH11_RESULT	0x40901AE4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH11_GRP_STAT	0x40901AE8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH11_ENABLE	0x40901AF8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH11_TR_CMD	0x40901AFC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH12_TR_CTL	0x40901B00	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH12_SAMPLE_CTL	0x40901B04	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.

Register name	Address	Description
PASS0_SAR1_CH12_POST_CTL	0x40901B08	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH12_RANGE_CTL	0x40901B0C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH12_INTR	0x40901B10	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH12_INTR_SET	0x40901B14	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH12_INTR_MASK	0x40901B18	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH12_INTR_MASKED	0x40901B1C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR1_CH12_WORK	0x40901B20	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH12_RESULT	0x40901B24	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH12_GRP_STAT	0x40901B28	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH12_ENABLE	0x40901B38	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH12_TR_CMD	0x40901B3C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH13_TR_CTL	0x40901B40	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH13_SAMPLE_CTL	0x40901B44	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR1_CH13_POST_CTL	0x40901B48	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH13_RANGE_CTL	0x40901B4C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH13_INTR	0x40901B50	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH13_INTR_SET	0x40901B54	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH13_INTR_MASK	0x40901B58	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH13_INTR_MASKED	0x40901B5C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
PASS0_SAR1_CH13_WORK	0x40901B60	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH13_RESULT	0x40901B64	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH13_GRP_STAT	0x40901B68	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH13_ENABLE	0x40901B78	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH13_TR_CMD	0x40901B7C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH14_TR_CTL	0x40901B80	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH14_SAMPLE_CTL	0x40901B84	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR1_CH14_POST_CTL	0x40901B88	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH14_RANGE_CTL	0x40901B8C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH14_INTR	0x40901B90	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH14_INTR_SET	0x40901B94	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH14_INTR_MASK	0x40901B98	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH14_INTR_MASKED	0x40901B9C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR1_CH14_WORK	0x40901BA0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH14_RESULT	0x40901BA4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH14_GRP_STAT	0x40901BA8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH14_ENABLE	0x40901BB8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH14_TR_CMD	0x40901BBC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH15_TR_CTL	0x40901BC0	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH15_SAMPLE_CTL	0x40901BC4	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.

Register name	Address	Description
PASS0_SAR1_CH15_POST_CTL	0x40901BC8	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH15_RANGE_CTL	0x40901BCC	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH15_INTR	0x40901BD0	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH15_INTR_SET	0x40901BD4	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH15_INTR_MASK	0x40901BD8	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH15_INTR_MASKED	0x40901BDC	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR1_CH15_WORK	0x40901BE0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH15_RESULT	0x40901BE4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH15_GRP_STAT	0x40901BE8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH15_ENABLE	0x40901BF8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH15_TR_CMD	0x40901BFC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH16_TR_CTL	0x40901C00	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH16_SAMPLE_CTL	0x40901C04	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR1_CH16_POST_CTL	0x40901C08	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH16_RANGE_CTL	0x40901C0C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH16_INTR	0x40901C10	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH16_INTR_SET	0x40901C14	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH16_INTR_MASK	0x40901C18	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH16_INTR_MASKED	0x40901C1C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
PASS0_SAR1_CH16_WORK	0x40901C20	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH16_RESULT	0x40901C24	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH16_GRP_STAT	0x40901C28	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH16_ENABLE	0x40901C38	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH16_TR_CMD	0x40901C3C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH17_TR_CTL	0x40901C40	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH17_SAMPLE_CTL	0x40901C44	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR1_CH17_POST_CTL	0x40901C48	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH17_RANGE_CTL	0x40901C4C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH17_INTR	0x40901C50	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH17_INTR_SET	0x40901C54	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH17_INTR_MASK	0x40901C58	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH17_INTR_MASKED	0x40901C5C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR1_CH17_WORK	0x40901C60	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH17_RESULT	0x40901C64	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH17_GRP_STAT	0x40901C68	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH17_ENABLE	0x40901C78	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH17_TR_CMD	0x40901C7C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH18_TR_CTL	0x40901C80	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH18_SAMPLE_CTL	0x40901C84	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.

Register name	Address	Description
PASS0_SAR1_CH18_POST_CTL	0x40901C88	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH18_RANGE_CTL	0x40901C8C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH18_INTR	0x40901C90	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH18_INTR_SET	0x40901C94	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH18_INTR_MASK	0x40901C98	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH18_INTR_MASKED	0x40901C9C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR1_CH18_WORK	0x40901CA0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH18_RESULT	0x40901CA4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH18_GRP_STAT	0x40901CA8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH18_ENABLE	0x40901CB8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH18_TR_CMD	0x40901CBC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH19_TR_CTL	0x40901CC0	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH19_SAMPLE_CTL	0x40901CC4	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR1_CH19_POST_CTL	0x40901CC8	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH19_RANGE_CTL	0x40901CCC	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH19_INTR	0x40901CD0	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH19_INTR_SET	0x40901CD4	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH19_INTR_MASK	0x40901CD8	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH19_INTR_MASKED	0x40901CDC	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
PASS0_SAR1_CH19_WORK	0x40901CE0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH19_RESULT	0x40901CE4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH19_GRP_STAT	0x40901CE8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH19_ENABLE	0x40901CF8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH19_TR_CMD	0x40901CFC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH20_TR_CTL	0x40901D00	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH20_SAMPLE_CTL	0x40901D04	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR1_CH20_POST_CTL	0x40901D08	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH20_RANGE_CTL	0x40901D0C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH20_INTR	0x40901D10	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH20_INTR_SET	0x40901D14	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH20_INTR_MASK	0x40901D18	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH20_INTR_MASKED	0x40901D1C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR1_CH20_WORK	0x40901D20	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH20_RESULT	0x40901D24	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH20_GRP_STAT	0x40901D28	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH20_ENABLE	0x40901D38	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH20_TR_CMD	0x40901D3C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH21_TR_CTL	0x40901D40	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH21_SAMPLE_CTL	0x40901D44	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.

Register name	Address	Description
PASS0_SAR1_CH21_POST_CTL	0x40901D48	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH21_RANGE_CTL	0x40901D4C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH21_INTR	0x40901D50	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH21_INTR_SET	0x40901D54	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH21_INTR_MASK	0x40901D58	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH21_INTR_MASKED	0x40901D5C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR1_CH21_WORK	0x40901D60	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH21_RESULT	0x40901D64	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH21_GRP_STAT	0x40901D68	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH21_ENABLE	0x40901D78	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH21_TR_CMD	0x40901D7C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH22_TR_CTL	0x40901D80	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH22_SAMPLE_CTL	0x40901D84	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR1_CH22_POST_CTL	0x40901D88	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH22_RANGE_CTL	0x40901D8C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH22_INTR	0x40901D90	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH22_INTR_SET	0x40901D94	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH22_INTR_MASK	0x40901D98	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH22_INTR_MASKED	0x40901D9C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
PASS0_SAR1_CH22_WORK	0x40901DA0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH22_RESULT	0x40901DA4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH22_GRP_STAT	0x40901DA8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH22_ENABLE	0x40901DB8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH22_TR_CMD	0x40901DBC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH23_TR_CTL	0x40901DC0	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH23_SAMPLE_CTL	0x40901DC4	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR1_CH23_POST_CTL	0x40901DC8	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH23_RANGE_CTL	0x40901DCC	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH23_INTR	0x40901DD0	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH23_INTR_SET	0x40901DD4	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH23_INTR_MASK	0x40901DD8	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH23_INTR_MASKED	0x40901DDC	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR1_CH23_WORK	0x40901DE0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH23_RESULT	0x40901DE4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH23_GRP_STAT	0x40901DE8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH23_ENABLE	0x40901DF8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH23_TR_CMD	0x40901DFC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH24_TR_CTL	0x40901E00	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH24_SAMPLE_CTL	0x40901E04	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.

Register name	Address	Description
PASS0_SAR1_CH24_POST_CTL	0x40901E08	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH24_RANGE_CTL	0x40901E0C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH24_INTR	0x40901E10	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH24_INTR_SET	0x40901E14	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH24_INTR_MASK	0x40901E18	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH24_INTR_MASKED	0x40901E1C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR1_CH24_WORK	0x40901E20	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH24_RESULT	0x40901E24	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH24_GRP_STAT	0x40901E28	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH24_ENABLE	0x40901E38	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH24_TR_CMD	0x40901E3C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH25_TR_CTL	0x40901E40	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH25_SAMPLE_CTL	0x40901E44	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR1_CH25_POST_CTL	0x40901E48	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH25_RANGE_CTL	0x40901E4C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH25_INTR	0x40901E50	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH25_INTR_SET	0x40901E54	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH25_INTR_MASK	0x40901E58	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH25_INTR_MASKED	0x40901E5C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
PASS0_SAR1_CH25_WORK	0x40901E60	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH25_RESULT	0x40901E64	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH25_GRP_STAT	0x40901E68	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH25_ENABLE	0x40901E78	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH25_TR_CMD	0x40901E7C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH26_TR_CTL	0x40901E80	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH26_SAMPLE_CTL	0x40901E84	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR1_CH26_POST_CTL	0x40901E88	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH26_RANGE_CTL	0x40901E8C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH26_INTR	0x40901E90	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH26_INTR_SET	0x40901E94	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH26_INTR_MASK	0x40901E98	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH26_INTR_MASKED	0x40901E9C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR1_CH26_WORK	0x40901EA0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH26_RESULT	0x40901EA4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH26_GRP_STAT	0x40901EA8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH26_ENABLE	0x40901EB8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH26_TR_CMD	0x40901EBC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH27_TR_CTL	0x40901EC0	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH27_SAMPLE_CTL	0x40901EC4	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.

Register name	Address	Description
PASS0_SAR1_CH27_POST_CTL	0x40901EC8	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH27_RANGE_CTL	0x40901ECC	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH27_INTR	0x40901ED0	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH27_INTR_SET	0x40901ED4	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH27_INTR_MASK	0x40901ED8	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH27_INTR_MASKED	0x40901EDC	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR1_CH27_WORK	0x40901EE0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH27_RESULT	0x40901EE4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH27_GRP_STAT	0x40901EE8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH27_ENABLE	0x40901EF8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH27_TR_CMD	0x40901EFC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH28_TR_CTL	0x40901F00	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH28_SAMPLE_CTL	0x40901F04	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR1_CH28_POST_CTL	0x40901F08	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH28_RANGE_CTL	0x40901F0C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH28_INTR	0x40901F10	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH28_INTR_SET	0x40901F14	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH28_INTR_MASK	0x40901F18	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH28_INTR_MASKED	0x40901F1C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
PASS0_SAR1_CH28_WORK	0x40901F20	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH28_RESULT	0x40901F24	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH28_GRP_STAT	0x40901F28	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH28_ENABLE	0x40901F38	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH28_TR_CMD	0x40901F3C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH29_TR_CTL	0x40901F40	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH29_SAMPLE_CTL	0x40901F44	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR1_CH29_POST_CTL	0x40901F48	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH29_RANGE_CTL	0x40901F4C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH29_INTR	0x40901F50	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH29_INTR_SET	0x40901F54	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH29_INTR_MASK	0x40901F58	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH29_INTR_MASKED	0x40901F5C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR1_CH29_WORK	0x40901F60	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH29_RESULT	0x40901F64	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH29_GRP_STAT	0x40901F68	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH29_ENABLE	0x40901F78	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH29_TR_CMD	0x40901F7C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH30_TR_CTL	0x40901F80	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH30_SAMPLE_CTL	0x40901F84	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.

Register name	Address	Description
PASS0_SAR1_CH30_POST_CTL	0x40901F88	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH30_RANGE_CTL	0x40901F8C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH30_INTR	0x40901F90	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH30_INTR_SET	0x40901F94	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH30_INTR_MASK	0x40901F98	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH30_INTR_MASKED	0x40901F9C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR1_CH30_WORK	0x40901FA0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH30_RESULT	0x40901FA4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH30_GRP_STAT	0x40901FA8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH30_ENABLE	0x40901FB8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH30_TR_CMD	0x40901FBC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR1_CH31_TR_CTL	0x40901FC0	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR1_CH31_SAMPLE_CTL	0x40901FC4	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR1_CH31_POST_CTL	0x40901FC8	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR1_CH31_RANGE_CTL	0x40901FCC	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR1_CH31_INTR	0x40901FD0	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR1_CH31_INTR_SET	0x40901FD4	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR1_CH31_INTR_MASK	0x40901FD8	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR1_CH31_INTR_MASKED	0x40901FDC	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
PASS0_SAR1_CH31_WORK	0x40901FE0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR1_CH31_RESULT	0x40901FE4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR1_CH31_GRP_STAT	0x40901FE8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR1_CH31_ENABLE	0x40901FF8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR1_CH31_TR_CMD	0x40901FFC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR2_CTL	0x40902000	Analog control register.. See PASS0_SAR0_CTL for the details of bit fields.
PASS0_SAR2_DIAG_CTL	0x40902004	Diagnostic Reference control register.. See PASS0_SAR0_DIAG_CTL for the details of bit fields.
PASS0_SAR2_PRECOND_CTL	0x40902010	Preconditioning control register.. See PASS0_SAR0_PRECOND_CTL for the details of bit fields.
PASS0_SAR2_ANA_CAL	0x40902080	Current analog calibration values. See PASS0_SAR0_ANA_CAL for the details of bit fields.
PASS0_SAR2_DIG_CAL	0x40902084	Current digital calibration values. See PASS0_SAR0_DIG_CAL for the details of bit fields.
PASS0_SAR2_ANA_CAL_ALT	0x40902090	Alternate analog calibration values. See PASS0_SAR0_ANA_CAL_ALT for the details of bit fields.
PASS0_SAR2_DIG_CAL_ALT	0x40902094	Alternate digital calibration values. See PASS0_SAR0_DIG_CAL_ALT for the details of bit fields.
PASS0_SAR2_CAL_UPD_CMD	0x40902098	Calibration update command. See PASS0_SAR0_CAL_UPD_CMD for the details of bit fields.
PASS0_SAR2_TR_PEND	0x40902100	Trigger pending status
PASS0_SAR2_WORK_VALID	0x40902180	Channel working data register 'valid' bits
PASS0_SAR2_WORK_RANGE	0x40902184	Range detected
PASS0_SAR2_WORK_RANGE_HI	0x40902188	Range detect above Hi flag
PASS0_SAR2_WORK_PULSE	0x4090218C	Pulse detected
PASS0_SAR2_RESULT_VALID	0x409021A0	Channel result data register 'valid' bits
PASS0_SAR2_RESULT_RANGE_HI	0x409021A4	Channel Range above Hi flags
PASS0_SAR2_STATUS	0x40902200	Current status of internal SAR registers (mostly for debug). See PASS0_SAR0_STATUS for the details of bit fields.
PASS0_SAR2_AVG_STAT	0x40902204	Current averaging status (for debug). See PASS0_SAR0_AVG_STAT for the details of bit fields.
PASS0_SAR2_CH0_TR_CTL	0x40902800	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR2_CH0_SAMPLE_CTL	0x40902804	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.

Register name	Address	Description
PASS0_SAR2_CH0_POST_CTL	0x40902808	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR2_CH0_RANGE_CTL	0x4090280C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR2_CH0_INTR	0x40902810	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR2_CH0_INTR_SET	0x40902814	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR2_CH0_INTR_MASK	0x40902818	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR2_CH0_INTR_MASKED	0x4090281C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR2_CH0_WORK	0x40902820	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR2_CH0_RESULT	0x40902824	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR2_CH0_GRP_STAT	0x40902828	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR2_CH0_ENABLE	0x40902838	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR2_CH0_TR_CMD	0x4090283C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR2_CH1_TR_CTL	0x40902840	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR2_CH1_SAMPLE_CTL	0x40902844	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR2_CH1_POST_CTL	0x40902848	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR2_CH1_RANGE_CTL	0x4090284C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR2_CH1_INTR	0x40902850	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR2_CH1_INTR_SET	0x40902854	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR2_CH1_INTR_MASK	0x40902858	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR2_CH1_INTR_MASKED	0x4090285C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
PASS0_SAR2_CH1_WORK	0x40902860	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR2_CH1_RESULT	0x40902864	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR2_CH1_GRP_STAT	0x40902868	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR2_CH1_ENABLE	0x40902878	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR2_CH1_TR_CMD	0x4090287C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR2_CH2_TR_CTL	0x40902880	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR2_CH2_SAMPLE_CTL	0x40902884	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR2_CH2_POST_CTL	0x40902888	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR2_CH2_RANGE_CTL	0x4090288C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR2_CH2_INTR	0x40902890	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR2_CH2_INTR_SET	0x40902894	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR2_CH2_INTR_MASK	0x40902898	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR2_CH2_INTR_MASKED	0x4090289C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR2_CH2_WORK	0x409028A0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR2_CH2_RESULT	0x409028A4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR2_CH2_GRP_STAT	0x409028A8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR2_CH2_ENABLE	0x409028B8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR2_CH2_TR_CMD	0x409028BC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR2_CH3_TR_CTL	0x409028C0	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR2_CH3_SAMPLE_CTL	0x409028C4	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.

Register name	Address	Description
PASS0_SAR2_CH3_POST_CTL	0x409028C8	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR2_CH3_RANGE_CTL	0x409028CC	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR2_CH3_INTR	0x409028D0	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR2_CH3_INTR_SET	0x409028D4	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR2_CH3_INTR_MASK	0x409028D8	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR2_CH3_INTR_MASKED	0x409028DC	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR2_CH3_WORK	0x409028E0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR2_CH3_RESULT	0x409028E4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR2_CH3_GRP_STAT	0x409028E8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR2_CH3_ENABLE	0x409028F8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR2_CH3_TR_CMD	0x409028FC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR2_CH4_TR_CTL	0x40902900	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR2_CH4_SAMPLE_CTL	0x40902904	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR2_CH4_POST_CTL	0x40902908	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR2_CH4_RANGE_CTL	0x4090290C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR2_CH4_INTR	0x40902910	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR2_CH4_INTR_SET	0x40902914	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR2_CH4_INTR_MASK	0x40902918	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR2_CH4_INTR_MASKED	0x4090291C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
PASS0_SAR2_CH4_WORK	0x40902920	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR2_CH4_RESULT	0x40902924	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR2_CH4_GRP_STAT	0x40902928	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR2_CH4_ENABLE	0x40902938	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR2_CH4_TR_CMD	0x4090293C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR2_CH5_TR_CTL	0x40902940	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR2_CH5_SAMPLE_CTL	0x40902944	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR2_CH5_POST_CTL	0x40902948	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR2_CH5_RANGE_CTL	0x4090294C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR2_CH5_INTR	0x40902950	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR2_CH5_INTR_SET	0x40902954	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR2_CH5_INTR_MASK	0x40902958	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR2_CH5_INTR_MASKED	0x4090295C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR2_CH5_WORK	0x40902960	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR2_CH5_RESULT	0x40902964	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR2_CH5_GRP_STAT	0x40902968	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR2_CH5_ENABLE	0x40902978	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR2_CH5_TR_CMD	0x4090297C	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR2_CH6_TR_CTL	0x40902980	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR2_CH6_SAMPLE_CTL	0x40902984	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.

Register name	Address	Description
PASS0_SAR2_CH6_POST_CTL	0x40902988	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR2_CH6_RANGE_CTL	0x4090298C	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR2_CH6_INTR	0x40902990	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR2_CH6_INTR_SET	0x40902994	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR2_CH6_INTR_MASK	0x40902998	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR2_CH6_INTR_MASKED	0x4090299C	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.
PASS0_SAR2_CH6_WORK	0x409029A0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR2_CH6_RESULT	0x409029A4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR2_CH6_GRP_STAT	0x409029A8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR2_CH6_ENABLE	0x409029B8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR2_CH6_TR_CMD	0x409029BC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_SAR2_CH7_TR_CTL	0x409029C0	Trigger control.. See PASS0_SAR0_CH0_TR_CTL for the details of bit fields.
PASS0_SAR2_CH7_SAMPLE_CTL	0x409029C4	Sample control.. See PASS0_SAR0_CH0_SAMPLE_CTL for the details of bit fields.
PASS0_SAR2_CH7_POST_CTL	0x409029C8	Post processing control. See PASS0_SAR0_CH0_POST_CTL for the details of bit fields.
PASS0_SAR2_CH7_RANGE_CTL	0x409029CC	Range thresholds. See PASS0_SAR0_CH0_RANGE_CTL for the details of bit fields.
PASS0_SAR2_CH7_INTR	0x409029D0	Interrupt request register.. See PASS0_SAR0_CH0_INTR for the details of bit fields.
PASS0_SAR2_CH7_INTR_SET	0x409029D4	Interrupt set request register. See PASS0_SAR0_CH0_INTR_SET for the details of bit fields.
PASS0_SAR2_CH7_INTR_MASK	0x409029D8	Interrupt mask register.. See PASS0_SAR0_CH0_INTR_MASK for the details of bit fields.
PASS0_SAR2_CH7_INTR_MASKED	0x409029DC	Interrupt masked request register. See PASS0_SAR0_CH0_INTR_MASKED for the details of bit fields.

Register name	Address	Description
PASS0_SAR2_CH7_WORK	0x409029E0	Working data register. See PASS0_SAR0_CH0_WORK for the details of bit fields.
PASS0_SAR2_CH7_RESULT	0x409029E4	Result data register. See PASS0_SAR0_CH0_RESULT for the details of bit fields.
PASS0_SAR2_CH7_GRP_STAT	0x409029E8	Group status register. See PASS0_SAR0_CH0_GRP_STAT for the details of bit fields.
PASS0_SAR2_CH7_ENABLE	0x409029F8	Enable register. See PASS0_SAR0_CH0_ENABLE for the details of bit fields.
PASS0_SAR2_CH7_TR_CMD	0x409029FC	Software triggers. See PASS0_SAR0_CH0_TR_CMD for the details of bit fields.
PASS0_PASS_CTL	0x409F0000	PASS control register
PASS0_SAR_TR_IN_SEL0	0x409F0020	per SAR generic input trigger select
PASS0_SAR_TR_IN_SEL1	0x409F0024	per SAR generic input trigger select. See PASS0_SAR_TR_IN_SEL0 for the details of bit fields.
PASS0_SAR_TR_IN_SEL2	0x409F0028	per SAR generic input trigger select. See PASS0_SAR_TR_IN_SEL0 for the details of bit fields.
PASS0_SAR_TR_OUT_SEL0	0x409F0040	per SAR generic output trigger select
PASS0_SAR_TR_OUT_SEL1	0x409F0044	per SAR generic output trigger select. See PASS0_SAR_TR_OUT_SEL0 for the details of bit fields.
PASS0_SAR_TR_OUT_SEL2	0x409F0048	per SAR generic output trigger select. See PASS0_SAR_TR_OUT_SEL0 for the details of bit fields.
PASS0_TEST_CTL	0x409F0080	Test control bits

17.1 PASS registers

PASS0_SAR0_CTL

Analog control register.
Address: 0x40900000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PWRUP_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [15:11]					HALF_LSB	MSB_STRETCH	IDLE_PWRDWN

Bits	23	22	21	20	19	18	17	16
SW Access	None							

Bits	23	22	21	20	19	18	17	16
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	None				
HW Access	R	R	R	None				
Name	ENABLED	ADC_EN	SARMUX_EN	None [28:24]				

Bits	Name	Description
31	ENABLED	- 0: SAR IP disabled (put analog in power down and stop clocks), also clears all pending triggers. - 1: SAR IP enabled. Default Value: 0
30	ADC_EN	Enable the SAR ADC and SAR sequencer (only valid if ENABLED=1) - 0: SARADC and SARSEQ are disabled (put SARADC analog in power down and stop clocks), also clears all pending triggers. - 1: SAR ADC and SARSEQ are enabled. To enable ADC0 to borrow SARMUX1-3 the corresponding ADC_EN must be set to 0. Default Value: 0
29	SARMUX_EN	Enable the SARMUX (only valid if ENABLED=1) - 0: SARMUX disabled (put analog in power down) - 1: SARMUX enabled. Default Value: 0
10	HALF_LSB	When set take an extra cycle to convert the half LSB and add it to 12-bit result for Missing Code Recovery This bit should always be set to '1' - 0: disable half LSB conversion (not recommended) - 1: enable half LSB conversion Default Value: 0
9	MSB_STRETCH	When set use 2 cycles for the Most Significant Bit (MSB) - 0: Use 1 clock cycle for MSB - 1: Use 2 clock cycles for MSB Default Value: 0
8	IDLE_PWRDWN	When idle automatically power down the analog. After an automatic power down a new trigger will power up the analog, however it will take PWRUP_TIME cycles before the first acquisition can be started. Note that re-arbitration happens at that time, i.e. the trigger that caused the power up may not get handled first. Default Value: 0

7 : 0	PWRUP_TIME	Number cycles to wait to power up after IDLE_PWRDWN. Check the STATUS.PWRUP_BUSY flag to see if the delay is still in progress. The power up delay is 1 us. Default Value: 0

PASS0_SAR0_DIAG_CTL

Diagnostic Reference control register.
Address: 0x40900004
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DIAG_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DIAG_EN	None [30:24]						

Bits	Name	Description
31	DIAG_EN	Diagnostic Reference enable (only valid if ENABLED=1) - 0: Diagnostic Reference disabled (powered down resistor ladder and current mirrors, DiagOut = Vssa). - 1: Diagnostic Reference enabled, output signal select according to DIAG_SEL (note also EPASS_MMIO.PASS_CTL.REFBUF_EN must be set). Default Value: 0
3 : 0	DIAG_SEL	Select Diagnostic Reference function Default Value: 0
		0x0: VREFL : DiagOut = VrefL
		0x1: VREFH_1DIV8 : DiagOut = VrefH * 1/8
		0x2: VREFH_2DIV8 : DiagOut = VrefH * 2/8
		0x3: VREFH_3DIV8 : DiagOut = VrefH * 3/8
		0x4: VREFH_4DIV8 : DiagOut = VrefH * 4/8

		0x5: VREFH_5DIV8 : DiagOut = VrefH * 5/8
		0x6: VREFH_6DIV8 : DiagOut = VrefH * 6/8
		0x7: VREFH_7DIV8 : DiagOut = VrefH * 7/8
		0x8: VREFH : DiagOut = VrefH
		0x9: VREFX : DiagOut = VrefX = VrefH * 199/200
		0xa: VBG : DiagOut = Vbg from SRSS
		0xb: VIN1 : DiagOut = Vin1
		0xc: VIN2 : DiagOut = Vin2
		0xd: VIN3 : DiagOut = Vin3
		0xe: I_SOURCE : DiagOut = Isource (10uA)
		0xf: I_SINK : DiagOut = Isink (10uA)

PASS0_SAR0_PRECOND_CTL

Preconditioning control register.
Address: 0x40900010
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				PRECOND_TIME [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	PRECOND_TIME	Number ADC clock cycles that Preconditioning is done before the sample window starts. If OVERLAP_EN=0 there will be 1 additional break before make cycle between preconditioning and sampling. Note that the minimum value is 1 (0 gives the same result as 1). Default Value: 0

PASS0_SAR0_ANA_CAL

Current analog calibration values
Address: 0x40900080
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	AOFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			RW				
Name	None [23:21]			AGAIN [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 16	AGAIN	Analog gain correction Default Value: 0
7 : 0	AOFFSET	Analog offset correction Default Value: 0

PASS0_SAR0_DIG_CAL

Current digital calibration values
Address: 0x40900084
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DOFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				RW			
Name	None [15:12]				DOFFSET [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW					
HW Access	None		RW					
Name	None [23:22]		DGAIN [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21 : 16	DGAIN	Digital gain correction. Signed value to correct +/- 30 codes for the maximum input voltage. Corrected = (D - DOFFSET) + ((D - DOFFSET) * DGAIN + 0x800) / 0x1000 Default Value: 0
11 : 0	DOFFSET	Digital offset correction Subtract DOFFSET from ADC output. Default Value: 0

PASS0_SAR0_ANA_CAL_ALT

Alternate analog calibration values
Address: 0x40900090
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	AOFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			AGAIN [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 16	AGAIN	See corresponding ANA_CAL field Default Value: 0
7 : 0	AOFFSET	See corresponding ANA_CAL field Default Value: 0

PASS0_SAR0_DIG_CAL_ALT

Alternate digital calibration values
Address: 0x40900094
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DOFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				DOFFSET [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW					
HW Access	None		R					
Name	None [23:22]		DGAIN [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21 : 16	DGAIN	See corresponding DIG_CAL field Default Value: 0
11 : 0	DOFFSET	See corresponding DIG_CAL field Default Value: 0

PASS0_SAR0_CAL_UPD_CMD

Calibration update command
Address: 0x40900098
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							RW1C
Name	None [7:1]							UPDATE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

0	UPDATE	Calibration update command: coherently copy values from alternate calibration regs to current calibration regs. Software sets this bit when the alternate calibration values have been set with the new values. Hardware will do the calibration update as soon as the ADC is idle or a 'continuous' triggered group completes. This ensures that all acquisitions within a group scan (even if preempted) are done with the same calibration values. This bit is cleared at the same time the calibration update is done. By clearing this bit software can cancel a requested update. Note: if the ADC is always busy with acquisitions for non continuously triggered groups/channels then the calibration update will remain pending forever. In such a case the software can either do a non coherent update by writing directly to the current calibration registers, or software can force the ADC to idle by disabling some or all channels. Software can check/poll this bit to see if the calibration update has taken effect. Default Value: 0

PASS0_SAR0_TR_PEND

Trigger pending status
Address: 0x40900100
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	TR_PEND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	TR_PEND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	TR_PEND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	TR_PEND	Trigger Pending. Hardware will set this bit if a hardware trigger is received. Default Value: 0

PASS0_SAR0_WORK_VALID

Channel working data register 'valid' bits
Address: 0x40900180
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK_VALID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK_VALID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	WORK_VALID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	WORK_VALID	If set the corresponding WORK register is valid, i.e. was already acquired during the current group scan. If this bit is low then either the channel is not enabled, not yet acquired or it is used as a pulse detect channel. Default Value: 0

PASS0_SAR0_WORK_RANGE

Range detected
Address: 0x40900184
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	RANGE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	RANGE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	RANGE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	RANGE	Default Value: 0

PASS0_SAR0_WORK_RANGE_HI

Range detect above Hi flag
Address: 0x40900188
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ABOVE_HI [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	ABOVE_HI [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	ABOVE_HI [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	ABOVE_HI	Out of range was detected and the value was above the Hi threshold Default Value: 0

PASS0_SAR0_WORK_PULSE

Pulse detected
Address: 0x4090018C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	PULSE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	PULSE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	PULSE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	PULSE	Default Value: 0

PASS0_SAR0_RESULT_VALID

Channel result data register 'valid' bits
Address: 0x409001A0
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	RESULT_VALID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	RESULT_VALID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	RESULT_VALID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	RESULT_VALID	If set the corresponding RESULT register is valid, i.e. was acquired during the preceding group scan. If this bit is low, after a group scan completed, then either the channel is not enabled or is used as a pulse detect channel. Default Value: 0

PASS0_SAR0_RESULT_RANGE_HI

Channel Range above Hi flags
Address: 0x409001A4
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ABOVE_HI [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	ABOVE_HI [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	ABOVE_HI [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	ABOVE_HI	Out of range was detected and the value was above the Hi threshold Default Value: 0

PASS0_SAR0_STATUS

Current status of internal SAR registers (mostly for debug)
Address: 0x40900200
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			CUR_CHAN [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None		R		None	R		
HW Access	None		W		None	W		
Name	None [15:14]		CUR_PREEMPT_TYPE [13:12]		None	CUR_PRIO [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	BUSY	PWRUP_BUSY	DBG_FREEZE	None [28:24]				

Bits	Name	Description
31	BUSY	If high then the SAR is busy with a conversion. Default Value: 0
30	PWRUP_BUSY	If high then the SAR is waiting for PWRUP_TIME due to IDLE_PWRDWN Default Value: 0
29	DBG_FREEZE	If high then the SAR is prevented from starting a new acquisition, see DBG_FREEZE_EN. Default Value: 0
13 : 12	CUR_PREEMPT_TYPE	Preempting type of current group/ channel, only valid if BUSY. Default Value: 0
10 : 8	CUR_PRIO	priority of current group/channel, only valid if BUSY. Default Value: 0
4 : 0	CUR_CHAN	current channel being acquired, only valid if BUSY. Default Value: 0

PASS0_SAR0_AVG_STAT

Current averaging status (for debug)
Address: 0x40900204
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CUR_AVG_ACCU [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CUR_AVG_ACCU [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				CUR_AVG_ACCU [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	CUR_AVG_CNT [31:24]							

Bits	Name	Description
31 : 24	CUR_AVG_CNT	the current value of the averaging counter. Note that the value shown is updated after the sample window and therefore runs ahead of the accumulator update. Default Value: 0
19 : 0	CUR_AVG_ACCU	the current value of the averaging accumulator Default Value: 0

PASS0_SAR0_CH0_TR_CTL

Trigger control.
Address: 0x40900800
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PRIO [6:4]			None	SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	None	RW	
HW Access	None				R	None	R	
Name	None [15:12]				GROUP_END	None	PREEMPT_TYPE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DONE_LEVEL	None [30:24]						

Bits	Name	Description
31	DONE_LEVEL	select level or pulse for 'tr_ch_done' trigger output Also see POST_CTL.TR_DONE_GRP_VIO Default Value: 0
		0x0: PULSE : tr_ch_done generates a 2 cycle pulse (clk_sys), no need to read the result to clear (also no ch_overflow detection)
		0x1: LEVEL : tr_ch_done is a level output until the result register is read (typical for DW usage, this also enables ch_overflow detection when DW is too slow)
11	GROUP_END	0: continue group with next channel 1: last channel of a group. Note that for the channel with the highest index (SAR_CH_NR) this always needs to be set Default Value: 1
9 : 8	PREEMPT_TYPE	Preemption type allow for this group Default Value: 0

		0x0: ABORT_CANCEL : Abort ongoing acquisition, do not return Clear pending trigger for aborted group and set Cancelled interrupt. Also 'Abort' whenever this group (do not pend the trigger) is not immediately scheduled for acquisition after a new trigger arrives. For this preemption type only, only a positive edge on the trigger can trigger the channel, i.e. CONTINUOUS or level high operation is not supported (to avoid continuous Cancelled interrupts). In case CTL.IDLE_PWRDWN is used and the analog is powered down, the group cannot be immediately scheduled for acquisition and therefore a trigger for a group with this preemption type will power up the analog, but the group will ABORT and set the Cancelled interrupt
		0x1: ABORT_RESTART : Abort ongoing acquisition, up on return Restart group from first channel.
		0x2: ABORT_RESUME : Abort ongoing acquisition, up on return Resume group from aborted channel If averaging, discard averaging results so far and restart averaging.
		0x3: FINISH_RESUME : Complete ongoing acquisition (including averaging), up on return Resume group from next channel
6 : 4	PRIO	Channel priority: "0": highest priority. "1" ... "6" "7": lowest priority. Channels with the same priority constitute a priority level. Priority decoding determines the highest priority pending channel. This channel is determined as follows. First, the highest priority level with pending channels is identified. Second, within this priority level, round robin arbitration is applied. Round robin arbitration (within a priority level) gives the highest priority to the lower channel indices (within the priority level). Default Value: 0
2 : 0	SEL	Trigger select Default Value: 0

		0x0: OFF : Use for channels in group, except the first channel
		0x1: TCPWM : Trigger from corresponding TCPWM channel
		0x2: GENERIC0 : Generic trigger input 0
		0x3: GENERIC1 :
		0x4: GENERIC2 :
		0x5: GENERIC3 :
		0x6: GENERIC4 :
		0x7: CONTINUOUS : Always triggered (also called idle), can only be used for at most 1 channel

PASS0_SAR0_CH0_SAMPLE_CTL

Sample control.
Address: 0x40900804
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW					
HW Access	R		R					
Name	PORT_ADDR [7:6]		PIN_ADDR [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW	RW		
HW Access	R		R		R	R		
Name	OVERLAP_DIAG [15:14]		PRECOND_MODE [13:12]		EXT_MUX_EN	EXT_MUX_SEL [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None			RW			
HW Access	R	None			R			
Name	ALT_CAL	None [30:28]			SAMPLE_TIME [27:24]			

Bits	Name	Description
31	ALT_CAL	Use alternate calibration values instead of the current calibration values. This allows the firmware to allocate one or more channels to quietly re-calibrate the ADC in the background of regular processing. 0 = use regular calibration values (ANA/DIG_CAL) 1 = use alternate calibration values (ANA/DIG_CAL_ALT) Note: typically calibration measurements select VrefL (PIN_ADDR=62) or VrefH (PIN_ADDR=63) Default Value: Undefined
27 : 16	SAMPLE_TIME	Sample time (aperture) in ADC clock cycles. Minimum is 1 (0 gives the same result as 1), minimum time needed for proper settling is at least 412ns, i.e.11 clock cycles at the max frequency of 26.7MHz. Default Value: Undefined

15 : 14	OVERLAP_DIAG	Select Overlap mode or SARMUX Diagnostics, in both cases the Diagnostic reference is used. With Overlap the Diagnostic reference typically sources or sinks a small current which is connected at the same time as the analog signal being sampled. For SARMUX Diagnostics the Diagnostic reference should provide a reference voltage which is selected at the SARMUX input instead of the normal analog signal being sampled. Default Value: Undefined
		0x0: OFF : No overlap or SARMUX Diagnostics
		0x1: HALF : Sample the selected analog input for 2 SAMPLE_TIME periods. During the first period use overlap sampling, i.e. connect both the analog input and Diagnostic reference. During second period only connect the analog input.
		0x2: FULL : Like normal sample the selected analog input for a single SAMPLE_TIME period but use overlap sampling, i.e. connect both the analog input and Diagnostic reference.
		0x3: MUX_DIAG : Select Diagnostic reference instead of analog signal at the input of the SARMUX. This enables a functional safety check of the SARMUX analog connections.
13 : 12	PRECOND_MODE	Select preconditioning mode. Preconditioning (dis)charges the SAR sample capacitor to the selected reference voltage for PRECOND_TIME (global) cycles, a break before make cycle will be inserted before sampling starts (SAMPLE_TIME). Default Value: Undefined
		0x0: OFF : No preconditioning
		0x1: VREFL : Discharge to VREFL
		0x2: VREFH : Charge to VREFH

		0x3: DIAG : Connect the Diagnostic reference output during preconditioning. The Diagnostic reference should be configured to output a reference voltage. Note: this selection is mutual exclusive with using the Diagnostic reference to supply an ibias current for OVERLAP.
11	EXT_MUX_EN	External analog mux enable. This enable can be used as enable (chip select) for the external analog mux (this enable is not used as enable for the GPIO output driver). This enable also prevents unnecessary toggle activity on the select signals of the external analog mux. When this enable is low EXT_MUX_SEL value will be ignored and the previous value will be maintained. Note that an external analog mux can only be used in combination with a pin input, i.e. PIN_ADDR<32 or Vmotor. If an internal signal is selected this enable should be 0. Default Value: Undefined
10 : 8	EXT_MUX_SEL	External analog mux select. This bit setting is related to EXT_MUX[x]_y on pin assignment. 0x0: Select EXT_MUX[x]_0 pin 0x1: Select EXT_MUX[x]_1 pin Default Value: Undefined
7 : 6	PORT_ADDR	Select the physical port. This field is only valid for ADC0. ADC0 can control and connect to the SARMUX of the neighboring ADC1-3. This requires the corresponding ADC to be off while the SARMUX is left on. When ADC0 controls another SARMUX it uses the PIN_ADDR, EXT_MUX_EN/SEL of this channel to control the other SARMUX. Default Value: Undefined
		0x0: SARMUX0 : ADC uses it's own SARMUX
		0x1: SARMUX1 : ADC0 uses SARMUX1 (only valid for ADC0, undefined result if used for ADC1-3)
		0x2: SARMUX2 : ADC0 uses SARMUX2 (only valid for ADC0, undefined result if used for ADC1-3)
		0x3: SARMUX3 : ADC0 uses SARMUX3 (only valid for ADC0, undefined result if used for ADC1-3)

5 : 0	PIN_ADDR	Address of the analog signal (pin) to be sampled by this channel - 0..31 : Vout = AN0..31, select corresponding analog input - 32: Vout = Vmotor, select motor input - 33: Vout = Vaux, select auxiliary input - 34: Vout = AmuxbusA - 35: Vout = AmuxbusB - 36: Vout = Vccd - 37: Vout = Vdda - 38: Vout = Vbg, Bandgap voltage from SRSS - 39: Vout = Vtemp, select temperature sensor. Make sure that only 1 ADC is allowed to use this. - 40..61: Vout = undefined, reserved for future products - 62: Vout = VrefL (VrefL actually bypasses the SARMUX (XSL)) - 63: Vout = VrefH (VrefH actually bypasses the SARMUX (XSH)) Note: When PORT_ADDR is not set to SARMUX0, pin addresses from 32-63 are not available. Only addresses 0-31 can be accessed from SARMUX1-3 Default Value: Undefined

PASS0_SAR0_CH0_POST_CTL

Post processing control
Address: 0x40900808
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	None			RW		
HW Access	R	R	None			R		
Name	SIGN_EXT	LEFT_ALIGN	None [5:3]			POST_PROC [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	AVG_CNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None	RW				
HW Access	R		None	R				
Name	RANGE_MODE [23:22]		None	SHIFT_R [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	None
HW Access	None						R	None
Name	None [31:26]						TR_DONE_GRP_VIO	None

Bits	Name	Description
25	TR_DONE_GRP_VIO	Select tr_sar_ch_done mode for last channel of a group, ignored for all other channels Also see TR_CTL.DONE_LEVEL Default Value: Undefined
		0x0: DONE : Default: tr_sar_ch_done is set when the group is done
		0x1: GRP_RANGE_VIO : tr_sar_ch_done is only set if any of the channels in the group has a Range Violation. This mode is ignored if this is not the last channel in the group. Note that if none of the channels in the group have Range detection enabled then the trigger will never get set.
23 : 22	RANGE_MODE	Range detect mode Default Value: Undefined
		0x0: BELOW_LO : Below Low threshold (result < Lo)

		0x1: INSIDE_RANGE : Inside range (Lo <= result < Hi)
		0x2: ABOVE_HI : Above high threshold (Hi <= result)
		0x3: OUTSIDE_RANGE : Outside range (result < Lo || Hi <= result)
20 : 16	SHIFT_R	Either Shift Right (no pulse detection) or Pulse negative reload value (if pulse detection is enabled) Shift right SHIFT_R[3:0] = [0..12]: the result (typically after averaging) is shifted right as specified here. Software has to make sure that the result fits in less than 16 bits. Any value >12 will be treated as 12, bit [4] is always ignored. This can also be used to fit the 12-bit result in 8 bits. Pulse detect negative reload value PULSE_NEG_RL[4:0] Default Value: Undefined
15 : 8	AVG_CNT	Either averaging count (minus 1) or Pulse positive reload value Averaging Count for channels that have averaging enabled. A channel will be sampled (AVG_CNT+1) = [1..256] times. The signal will be acquired back to back (1st order accumulate and dump filter), the average result is calculated and stored and then the next enabled channel is sampled. If more than 16 sample are taken (AVG_CNT>=16) then AVG_SHIFT must be set so that the result after shifting fits in 16 bits Pulse detect positive reload value PULSE_POS_RL[7:0] Default Value: Undefined
7	SIGN_EXT	Output data is sign extended Default Value: Undefined
		0x0: UNSIGNED : Default: result data is unsigned (zero extended if needed)
		0x1: SIGNED : Result data is signed (sign extended if needed)

6	LEFT_ALIGN	Left or right align data in result[15:0]. 0: the data is right aligned in result[11:0], with sign extension to 16 bits if enabled 1: the data is left aligned in result[15:4] with the lower nibble 0. Caveat if the result was more than 12 bits (e.g. after averaging) then the bits above 12 will be discarded. Default Value: Undefined
2 : 0	POST_PROC	Post processing Default Value: Undefined
		0x0: NONE : No postprocessing
		0x1: AVG : Averaging
		0x2: AVG_RANGE : Averaging followed by Range detect
		0x3: RANGE : Range detect
		0x4: RANGE_PULSE : Range detect followed by pulse detect
		0x5: RESERVED0 :
		0x6: RESERVED1 :
		0x7: RESERVED2 :

PASS0_SAR0_CH0_RANGE_CTL

Range thresholds
Address: 0x4090080C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RANGE_LO [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RANGE_LO [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RANGE_HI [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RANGE_HI [31:24]							

Bits	Name	Description
31 : 16	RANGE_HI	Range detect high threshold (Hi) Default Value: Undefined
15 : 0	RANGE_LO	Range detect low threshold (Lo) Default Value: Undefined

PASS0_SAR0_CH0_INTR

Interrupt request register.
Address: 0x40900810
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [7:3]					GRP_OVERFLOW	GRP_CANCELLED	GRP_DONE

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [15:11]					CH_OVERFLOW	CH_PULSE	CH_RANGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	CH_OVERFLOW	Channel overflow Interrupt: hardware sets this interrupt for each channel if a new Pulse or Range interrupt is detected while the interrupt is still pending or when DW did not acknowledge data pickup. Write with '1' to clear bit. Default Value: 0
9	CH_PULSE	Pulse detect Interrupt: hardware sets this interrupt for each channel if the positive pulse counter reaches zero. This interrupt is mutual exclusive with Range detect interrupt. Write with '1' to clear bit. Default Value: 0

8	CH_RANGE	Range detect Interrupt: hardware sets this interrupt for each channel if the conversion result (after averaging) of that channel met the condition specified by the SAR_RANGE registers. This interrupt is mutual exclusive with Pulse detect interrupt. Write with '1' to clear bit. Default Value: 0
2	GRP_OVERFLOW	Overflow Interrupt: hardware sets this interrupt for the last channel of a group if the group scan is done and the Done interrupt is already (still) pending. Write with '1' to clear bit. Default Value: 0
1	GRP_CANCELLED	Cancelled Interrupt: hardware sets this interrupt for the last channel of a group if the group scan was preempted and CANCELLED. Note that it is possible that also the GRP_DONE interrupt is set. If that is the case one or more new triggers were detected while the group was already busy, i.e. triggers are too fast. Write with '1' to clear bit. Default Value: 0
0	GRP_DONE	Done Interrupt: hardware sets this interrupt for the last channel of a group if the group scan is done. Write with '1' to clear bit. Default Value: 0

PASS0_SAR0_CH0_INTR_SET

Interrupt set request register
Address: 0x40900814
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [7:3]					GRP_OVERFLOW_SET	GRP_CANCELLED_SET	GRP_DONE_SET

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [15:11]					CH_OVERFLOW_SET	CH_PULSE_SET	CH_RANGE_SET

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	CH_OVERFLOW_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	CH_PULSE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	CH_RANGE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	GRP_OVERFLOW_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	GRP_CANCELLED_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	GRP_DONE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

PASS0_SAR0_CH0_INTR_MASK

Interrupt mask register.
Address: 0x40900818
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					GRP_OVERFLOW_MASK	GRP_CANCELLED_MASK	GRP_DONE_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [15:11]					CH_OVERFLOW_MASK	CH_PULSE_MASK	CH_RANGE_MASK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	CH_OVERFLOW_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	CH_PULSE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	CH_RANGE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	GRP_OVERFLOW_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	GRP_CANCELLED_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	GRP_DONE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

PASS0_SAR0_CH0_INTR_MASKED

Interrupt masked request register
Address: 0x4090081C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					GRP_OVERFLOW_MASKED	GRP_CANCELLED_MASKED	GRP_DONE_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [15:11]					CH_OVERFLOW_MASKED	CH_PULSE_MASKED	CH_RANGE_MASKED

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	CH_OVERFLOW_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
9	CH_PULSE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
8	CH_RANGE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
2	GRP_OVERFLOW_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
1	GRP_CANCELLED_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
0	GRP_DONE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

PASS0_SAR0_CH0_WORK

Working data register
Address: 0x40900820
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	R	None			
HW Access	W	W	W	W	None			
Name	VALID_MIR	PULSE_MIR	RANGE_MIR	ABOVE_HI_MIR	None [27:24]			

Bits	Name	Description
31	VALID_MIR	mirror bit of corresponding bit in WORK_VALID register Default Value: 0
30	PULSE_MIR	mirror bit of corresponding bit in WORK_PULSE register Default Value: 0
29	RANGE_MIR	mirror bit of corresponding bit in WORK_RANGE register Default Value: 0
28	ABOVE_HI_MIR	mirror bit of the corresponding ABOVE_HI bit Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

PASS0_SAR0_CH0_RESULT

Result data register
Address: 0x40900824
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	R	None			
HW Access	W	W	W	W	None			
Name	VALID_MIR	PULSE_INTR_MIR	RANGE_INTR_MIR	ABOVE_HI_MIR	None [27:24]			

Bits	Name	Description
31	VALID_MIR	mirror bit of the corresponding bit in RESULT_VALID register Default Value: 0
30	PULSE_INTR_MIR	mirror bit of INTR.CH_PULSE bit Default Value: 0
29	RANGE_INTR_MIR	mirror bit of INTR.CH_RANGE bit Default Value: 0
28	ABOVE_HI_MIR	mirror bit of the corresponding ABOVE_HI bit Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

PASS0_SAR0_CH0_GRP_STAT

Group status register
Address: 0x40900828
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					GRP_OVERFLOW	GRP_CANCELLED	GRP_COMPLETE

Bits	15	14	13	12	11	10	9	8
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [15:11]					CH_OVERFLOW	CH_PULSE_COMPLETE	CH_RANGE_COMPLETE

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							W
Name	None [23:17]							GRP_BUSY

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	GRP_BUSY	Group acquisition busy. This is a copy of the TR_PENDING bit of the first channel of the group. Default Value: 0
10	CH_OVERFLOW	Channel Overflow. This is a copy of the INTR.CH_OVERFLOW bit. Default Value: 0
9	CH_PULSE_COMPLETE	Channel Pulse complete. This is a copy of the INTR.CH_PULSE bit. Default Value: 0
8	CH_RANGE_COMPLETE	Channel Range complete. This is a copy of the INTR.CH_RANGE bit. Default Value: 0
2	GRP_OVERFLOW	Group Overflow. This is a copy of the INTR.GRP_OVERFLOW bit. Default Value: 0
1	GRP_CANCELLED	Group Cancelled. This is a copy of the INTR.GRP_CANCELLED bit. Default Value: 0

0	GRP_COMPLETE	Group acquisition complete. This is a copy of the INTR.GRP_DONE bit. Default Value: 0

PASS0_SAR0_CH0_ENABLE

Enable register
Address: 0x40900838
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							CHAN_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CHAN_EN	Channel enable. - 0: the corresponding channel is disabled. Corresponding trigger will be reset immediately. - 1: the corresponding channel is enabled. Note: To disable a group either stop the trigger first or begin with disabling the lowest channel first. To enable a group either start with enabling the last channel first and the first channel last, or start the trigger after all channels are enabled. If these rules are not followed the result is undefined. Default Value: 0

PASS0_SAR0_CH0_TR_CMD

Software triggers
Address: 0x4090083C
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	START	Software start trigger. When written with '1', a start trigger is generated which sets the corresponding TR_PEND bit (only if the channel is enabled). A read always returns a 0. Default Value: 0

PASS0_SAR1_TR_PEND

Trigger pending status
Address: 0x40901100
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	TR_PEND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	TR_PEND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	TR_PEND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	TR_PEND [31:24]							

Bits	Name	Description
31 : 0	TR_PEND	Trigger Pending. Hardware will set this bit if a hardware trigger is received. Default Value: 0

PASS0_SAR1_WORK_VALID

Channel working data register 'valid' bits
Address: 0x40901180
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK_VALID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK_VALID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	WORK_VALID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	WORK_VALID [31:24]							

Bits	Name	Description
31 : 0	WORK_VALID	If set the corresponding WORK register is valid, i.e. was already acquired during the current group scan. If this bit is low then either the channel is not enabled, not yet acquired or it is used as a pulse detect channel. Default Value: 0

PASS0_SAR1_WORK_RANGE

Range detected
Address: 0x40901184
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	RANGE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	RANGE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	RANGE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	RANGE [31:24]							

Bits	Name	Description
31 : 0	RANGE	Default Value: 0

PASS0_SAR1_WORK_RANGE_HI

Range detect above Hi flag
Address: 0x40901188
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ABOVE_HI [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	ABOVE_HI [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	ABOVE_HI [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	ABOVE_HI [31:24]							

Bits	Name	Description
31 : 0	ABOVE_HI	Out of range was detected and the value was above the Hi threshold Default Value: 0

PASS0_SAR1_WORK_PULSE

Pulse detected
Address: 0x4090118C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	PULSE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	PULSE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	PULSE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	PULSE [31:24]							

Bits	Name	Description
31 : 0	PULSE	Default Value: 0

PASS0_SAR1_RESULT_VALID

Channel result data register 'valid' bits
Address: 0x409011A0
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	RESULT_VALID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	RESULT_VALID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	RESULT_VALID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	RESULT_VALID [31:24]							

Bits	Name	Description
31 : 0	RESULT_VALID	If set the corresponding RESULT register is valid, i.e. was acquired during the preceding group scan. If this bit is low, after a group scan completed, then either the channel is not enabled or is used as a pulse detect channel. Default Value: 0

PASS0_SAR1_RESULT_RANGE_HI

Channel Range above Hi flags
Address: 0x409011A4
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ABOVE_HI [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	ABOVE_HI [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	ABOVE_HI [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	ABOVE_HI [31:24]							

Bits	Name	Description
31 : 0	ABOVE_HI	Out of range was detected and the value was above the Hi threshold Default Value: 0

PASS0_SAR2_TR_PEND

Trigger pending status
Address: 0x40902100
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	TR_PEND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	TR_PEND	Trigger Pending. Hardware will set this bit if a hardware trigger is received. Default Value: 0

PASS0_SAR2_WORK_VALID

Channel working data register 'valid' bits
Address: 0x40902180
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK_VALID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	WORK_VALID	If set the corresponding WORK register is valid, i.e. was already acquired during the current group scan. If this bit is low then either the channel is not enabled, not yet acquired or it is used as a pulse detect channel. Default Value: 0

PASS0_SAR2_WORK_RANGE

Range detected
Address: 0x40902184
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	RANGE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	RANGE	Default Value: 0

PASS0_SAR2_WORK_RANGE_HI

Range detect above Hi flag
Address: 0x40902188
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ABOVE_HI [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	ABOVE_HI	Out of range was detected and the value was above the Hi threshold Default Value: 0

PASS0_SAR2_WORK_PULSE

Pulse detected
Address: 0x4090218C
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	PULSE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PULSE	Default Value: 0

PASS0_SAR2_RESULT_VALID

Channel result data register 'valid' bits
Address: 0x409021A0
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	RESULT_VALID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	RESULT_VALID	If set the corresponding RESULT register is valid, i.e. was acquired during the preceding group scan. If this bit is low, after a group scan completed, then either the channel is not enabled or is used as a pulse detect channel. Default Value: 0

PASS0_SAR2_RESULT_RANGE_HI

Channel Range above Hi flags
Address: 0x409021A4
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ABOVE_HI [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	ABOVE_HI	Out of range was detected and the value was above the Hi threshold Default Value: 0

PASS0_PASS_CTL

PASS control register
Address: 0x409F0000
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None		RW	RW
HW Access	None		R	R	None		R	R
Name	None [7:6]		SUPPLY_MON_LVL_B	SUPPLY_MON_EN_B	None [3:2]		SUPPLY_MON_LVL_A	SUPPLY_MON_EN_A

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW		None				
HW Access	None	R		None				
Name	None	REFBUF_MODE [22:21]		None [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW			None			
HW Access	None	R			None			
Name	None	DBG_FREEZE_EN [30:28]			None [27:24]			

Bits	Name	Description
30 : 28	DBG_FREEZE_EN	Debug pause enable, 1 per ADC. When set a high tr_debug_freeze trigger will prevent the scheduler from starting acquisitions on a new channel. Note that averaging for an already started channel will be completed. Default Value: 0
22 : 21	REFBUF_MODE	Reference mode. The reference needs to be present when using TEMP sensor or diagnostic reference (in addition to SAR.DIAG_CTL.DIAG_EN). Note that setting this mode is not required for the ADC operation itself. Default Value: 0
		0x0: OFF : No reference
		0x1: ON : Reference = buffered Vbg from SRSS
		0x2: RESERVED : undefined
		0x3: BYPASS : Reference = unbuffered Vbg from SRSS

5	SUPPLY_MON_LVL_B	Supply monitor level select for AMUXBUS_B Default Value: 0
		0x0: VRL : amuxbus_b_mon = VRL
		0x1: VRH : amuxbus_b_mon = VRH
4	SUPPLY_MON_EN_B	Supply monitor enable for AMUXBUS_B (amuxbus_b_mon) Default Value: 0
1	SUPPLY_MON_LVL_A	Supply monitor level select for AMUXBUS_A Default Value: 0
		0x0: VRL : amuxbus_a_mon = VRL
		0x1: VRH : amuxbus_a_mon = VRH
0	SUPPLY_MON_EN_A	Supply monitor enable for AMUXBUS_A (amuxbus_a_mon) Default Value: 0

PASS0_SAR_TR_IN_SEL0

per SAR generic input trigger select
Address: 0x409F0020
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	IN1_SEL [7:4]				IN0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	IN3_SEL [15:12]				IN2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				IN4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	IN4_SEL	Select generic trigger for SAR generic trigger input 4 Default Value: 4
15 : 12	IN3_SEL	Select generic trigger for SAR generic trigger input 3 Default Value: 3
11 : 8	IN2_SEL	Select generic trigger for SAR generic trigger input 2 Default Value: 2
7 : 4	IN1_SEL	Select generic trigger for SAR generic trigger input 1 Default Value: 1
3 : 0	IN0_SEL	Select generic trigger for SAR generic trigger input 0 Default Value: 0

PASS0_SAR_TR_OUT_SEL0

per SAR generic output trigger select
Address: 0x409F0040
Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OUT0_SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		R					
Name	None [15:14]		OUT1_SEL [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 8	OUT1_SEL	Select SAR output trigger for generic trigger output 1 Default Value: 1
5 : 0	OUT0_SEL	Select SAR output trigger for generic trigger output 0 0-31: selects a tr_sar_ch_done trigger 32-63: selects a tr_sar_ch_rangvio trigger Default Value: 0

PASS0_TEST_CTL

Test control bits
Address: 0x409F0080
Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	RW	RW	None	RW
HW Access	None	R	R	R	R	R	None	R
Name	None	TS_CAL_VI_SEL	TS_CAL_DIODE_PNP_EN	TS_CAL_DIODE_EN	TS_CAL_VE_OUT	TS_CAL_VB_OUT	None	TS_CAL_CUR_IN

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [15:13]			TS_CAL_SPARE	None [11:10]		TS_CAL_CUR_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	TS_CAL_SPARE	Spare Default Value: 0
9 : 8	TS_CAL_CUR_SEL	Select the current going into the BJT, for Temperature Sensor Calibration Default Value: 0
		0x0: I_1U : Select 1 uA
		0x1: I_2U : Select 2 uA
		0x2: I_5U : Select 5 uA
		0x3: I_10U : Select 10 uA
6	TS_CAL_VI_SEL	Select current or voltage output on "v_temp" pin, for Temperature Sensor Calibration Default Value: 0
		0x0: CURRENT : Current is selected
		0x1: VOLTAGE : Voltage is selected

5	TS_CAL_DIODE_PNP_EN	Enable signal for PNP transistor. This transistor will be used only during calibration for accurate estimation of chip temp. 0 = Turn PNP off 1 = Configure PNP as a diode (short base and collector) Default Value: 0
4	TS_CAL_DIODE_EN	Diode Enable, disconnect or connect the base and collector terminal of the BJT Default Value: 0
3	TS_CAL_VE_OUT	Voltage Emitter switch control, for Temperature Sensor Calibration Default Value: 0
2	TS_CAL_VB_OUT	Voltage Base switch control, for Temperature Sensor Calibration Default Value: 0
0	TS_CAL_CUR_IN	External current input switch control, for Temperature Sensor Calibration Default Value: 0

Revision history

Document revision	Date	Description of changes
**	2025-07-16	Initial release

Trademarks

PSOC™, formerly known as PSoC™, is a trademark of Infineon Technologies. Any references to PSoC™ in this document or others shall be deemed to refer to PSOC™.

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2025-07-16

Published by

Infineon Technologies AG

81726 Munich, Germany

© 2025 Infineon Technologies AG

All Rights Reserved.

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference
IFX-osl1747300325368

Important notice

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Warnings

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.