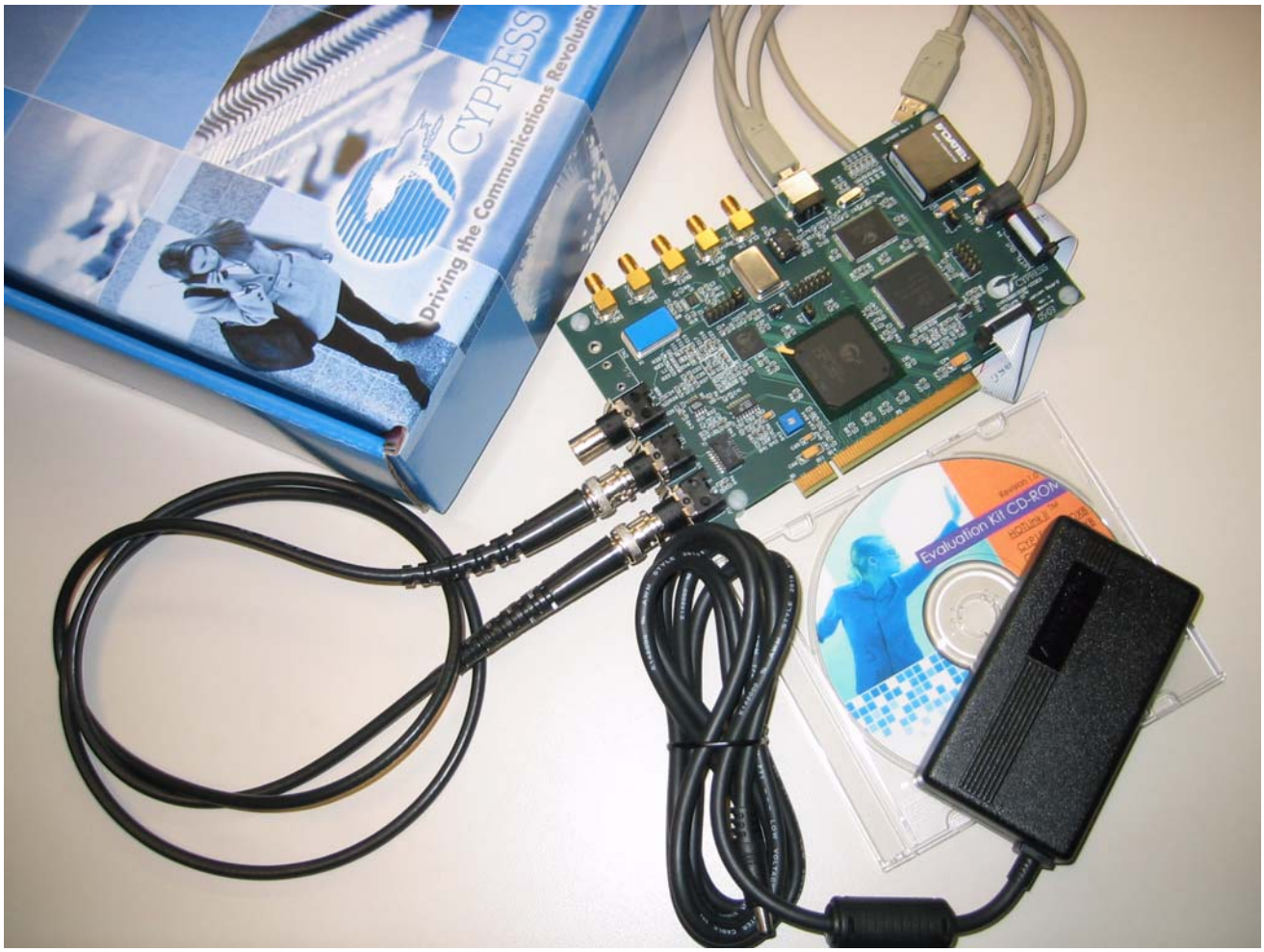
HOTLink II™ Video Evaluation Board



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1.0 Introduction

The HOTLink II™ transceiver is a point-to-point or point-to-multipoint communications building block allowing the transfer of data over high-speed serial links at signaling speeds ranging from 195 to 1500 MBaud.

The frequency agility of the HOTLink II transceiver enables its application in various data and video transmission standards. The HOTLink II transceiver supports serial video transmission, which includes Digital Video Broadcasting (DVB-ASI) and Society of Motion Picture Television Engineers (SMPTE) standards of video transmission. DVB is a widely accepted standard for digital video transmission, especially in the video-on-demand market segment. SMPTE has in turn developed several standards for serial and parallel video transmission at different speeds and formats.

The HOTLink II video evaluation board demonstrates the ability of the Cypress HOTLink II family of devices to pass video at signaling rates of up to 360 Mbps, the functionality of Delta39K™ CPLD as an ideal CPLD solution for SMPTE applications, the flexible clocking abilities of CyClocksRT™, and the use of EZ-USB *FX2*™ USB microcontroller for video data and in-system configuration applications.

2.0 Kit Contents

The kit contains the following:

1. HOTLink II video board, as shown in *Figure 2-1*.
2. CD containing:
   a. DVB/SMPTE Test software GUI (HEB Test)
   b. Application notes
   c. Evaluation board user's guide
   d. Cypress device data sheets
3. 75Ω Coaxial cable
4. AC/DC wall adapter

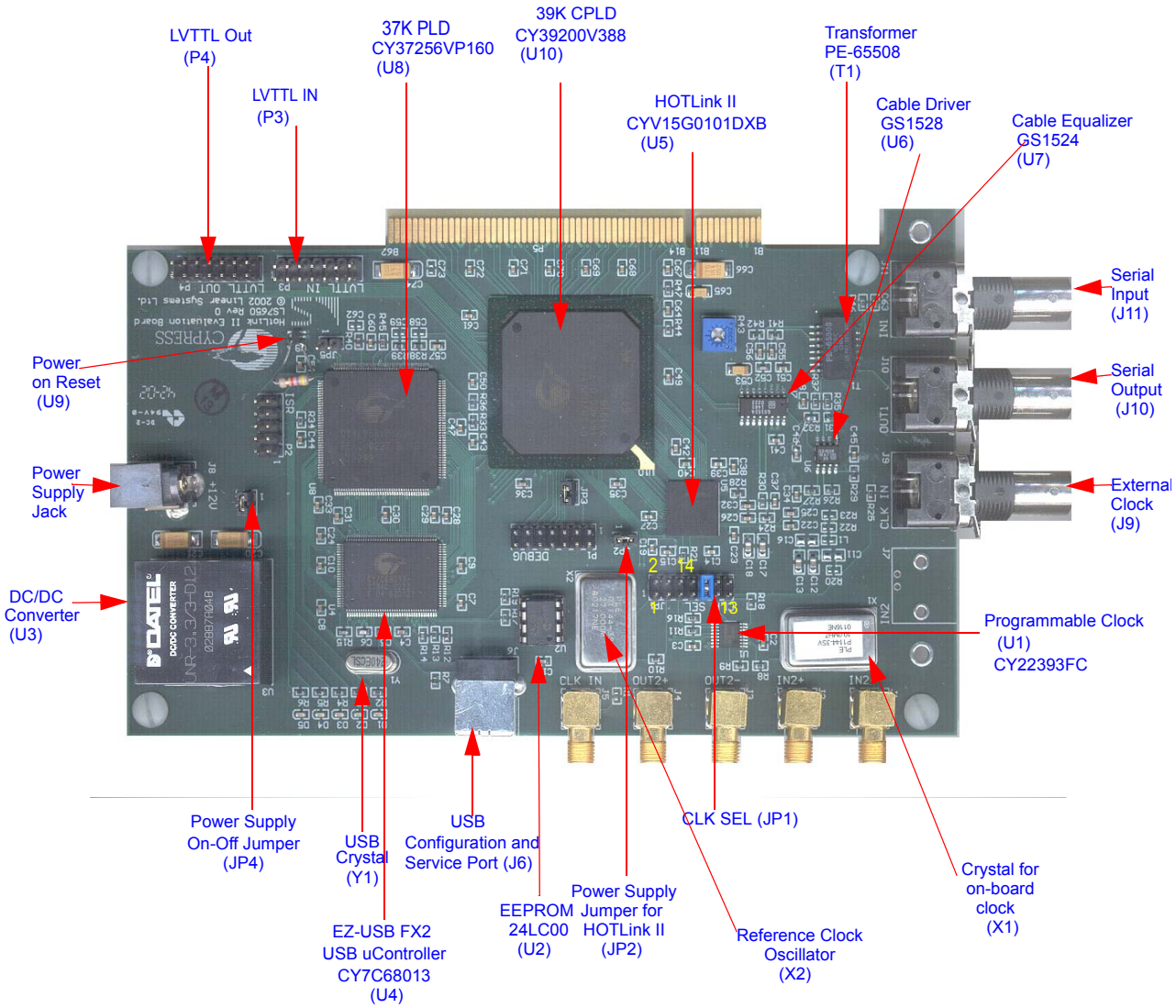


Figure 2-1.Top View of Video Board

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5. Jumper ribbon cable (on board)
6. HS USB cable
7. *Dear Customer* letter
8. Kit checklist.

Table 2-1.HOTLink II Video Board Core Components Description

Name — Part Number	Description
HOTLink II Transceiver — CYV15G0101DXB (U5)	Single-channel HOTLink II transceiver.
Delta39K CPLD — CY39200V388 (U10)	CPLD to configure the HOTLink II transceiver and programmable clock.
Ultra37000™ CPLD — CY37256VP160 (U8)	Interface to USB microcontroller.
EZ-USB *FX2* USB Microcontroller — CY7C68013 (U4)	USB microcontroller to configure 39K CPLD and programmable clock.
USB Configuration and Service Port (J6)	Used to configure CPLDs and Clock chip. Used as a service port.
Internal Clock — CY22393FC (U1)	Three-Phase-locked-Loop (PLL) Serial-programmable FLASH-programmable Clock Generator.
CLK SEL (JP1)	Clock Select Header with jumper to select between different clocking options.
External Clock — (J9) for BNC type connector (J5) for SMA type connector	Connector for external clock input to the video board.
Serial Output (J10)	Connector for data-out.
Serial Input (J11)	Connector for data-in.
LVTTL Headers (LVTTL IN (P3) and LVTTL OUT (P4))	Used for looping back the data in parallel loop test configurations.
EEPROM —24LC00 (U2)	Provides initial configuration information to USB microcontroller.
Transformer PE-65508 (T1)	Fibre Channel dual transformer.
Reset (U9)	Reset controller. Power-on Reset for all components on board.
Jumper JP4	Main power supply On-Off jumper.
Jumper JP2	Power supply jumper for HOTLink II transceiver. Can also be used to measure current drawn by HOTLink II transceiver.
Jumper JP3	Power supply jumper for Delta39K CPLD. Can also be used to measure current drawn by the Delta39K CPLD.
Jumper JP5	For internal use only — do not populate with jumper.
USB crystal oscillator (Y1)	24-MHz crystal oscillator for USB microcontroller.
On-board clock oscillator (X2)	Reference clock oscillator for CLK SEL (JP1) pins 1–2.

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3.0 Evaluation Board Features

This section highlights the key features of the HOTLink II Video Evaluation Board.

- User-friendly GUI
- Video transport at multiple data rates of 270 and 360 Mbps
- Supports DVB-ASI (270 Mbps)
- SMPTE scrambler/descrambler embedded in Delta39K CPLD
- USB port to establish board configuration
- High-speed USB *FX2* to configure Delta39K CPLD and programmable clock
- Flexible clocking abilities of CyClocksRT
- External and internal loop back capability for SMPTE and DVB-ASI
- Delta39K CPLD, reconfigurable via the USB or ISR Header or from the boot memory
- 12V DC supply with onboard voltage regulator to prevent noise transfer from external power sources
- On-board serial equalizer and cable driver
- LED status indicators

4.0 Functional Overview

4.1 Block Diagram

The block diagram of the evaluation board is shown in *Figure 4-1*.

The evaluation board can be used to test the HOTLink II transceiver in various GUI-based test modes for DVB-ASI- and SMPTE-based applications support. The core of the video board is the HOTLink II CYV15G0101DXB transceiver (as indicated in *Figure 2-1*). The transmit channel of the HOTLink II transceiver accepts parallel characters into its input register and converts them to serial data, after encoding if necessary. The receive channel accepts serial data and converts it to parallel data. The input and output data are received and transmitted through BNC connectors (J11 and J10 on board) and/or SMA connectors (J1, J2, J3 and J4 on board). A power supply jumper JP2 on board (shown in *Figure 2-1* and described in *Table 2-1*) can be used to measure the current drawn (and hence power consumed) by the HOTLink II transceiver. To do this, simply remove JP2 and place an ammeter across the pins to measure the current that is drawn by the HOTLink II transceiver alone. The data input and output BNC connectors, J11 and J10, are connected to a transformer located next to the BNC connectors.

The transformer is a Fibre Channel dual transformer PE-65508 (T1 on board), which can be used with a 75Ω coaxial cable or a 150Ω STP cable.

The Delta39K CPLD (U10 on board) is used to configure the HOTLink II transceiver. The internal memory feature of the Delta39K CPLD can be used for frame buffering, which is essential to most video applications. The Delta39K CPLD can be configured as an SMPTE scrambler/descrambler via the EZ-USB *FX2* USB microcontroller (CY7C68013), labelled as U4 on board, through the USB configuration and service port (J6 on board). The USB microcontroller requires a 24-MHz crystal, labelled Y1 on board. A EEPROM (24LC00), labelled U2, provides the initial configuration information to the USB microcontroller. The USB microcontroller is also used to configure the programmable clock. The Cypress programmable clock (CyClocksRT), labelled U1 on board, can provide up to six outputs, configurable from three integrated PLLs. It has a 10-MHz reference crystal labelled as X1 on board, and shown in *Figure 2-1*. The CyClocksRT programmable clock is serial-programmable and has configurable output buffers.

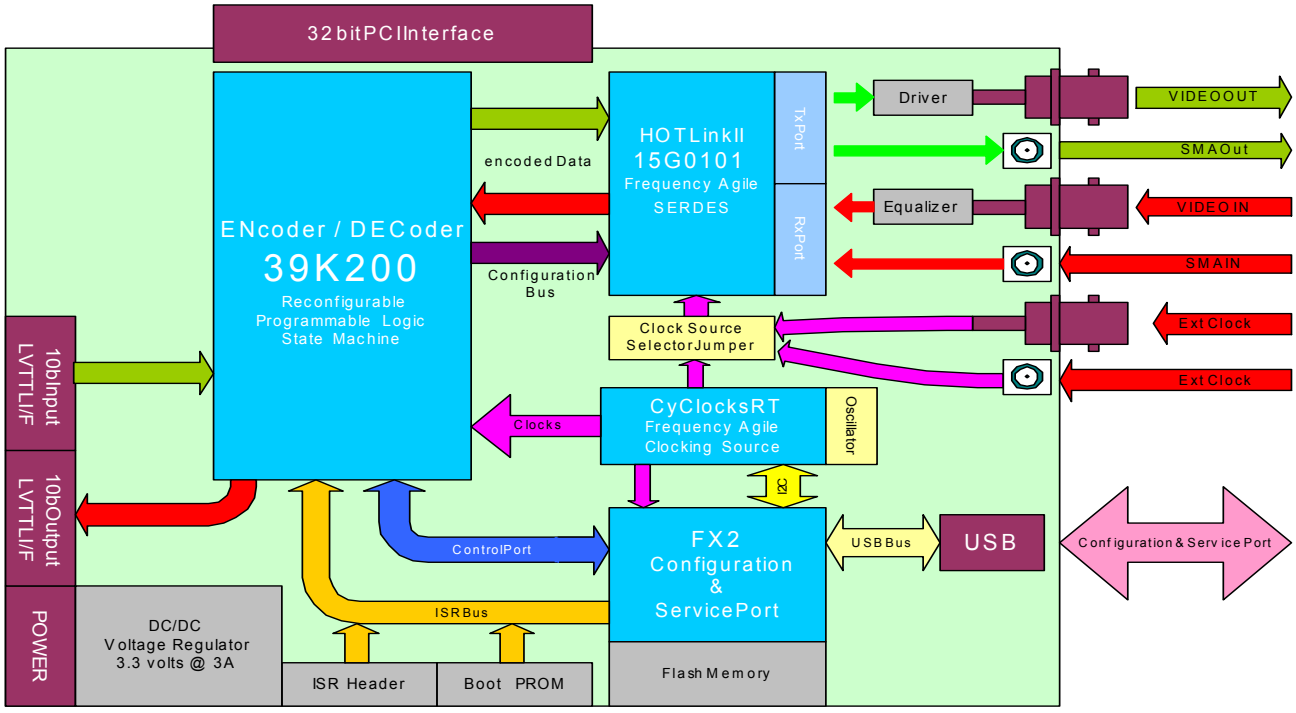


Figure 4-1.Block Diagram of HOTLink II Video Evaluation Board

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An external clock can also be supplied, through an SMA (J5 on board) or BNC (J9 on board) connector. Depending on whether an internal or external clock is used, the jumper settings on the CLK SEL jumper (JP1) on board have to be changed (a close view and description of the CLK SEL pins and jumper settings are shown in *Figure 5-2*, *Figure 5-3*, and *Table 5-1*).

Both LVTTL input and output headers are used for looping back the data in parallel loop back test configurations. The data from the Delta39K CPLD can be passed through the LVTTL output pin header (P4 on board) and looped back in through the LVTTL input pin header (P3 on board).

The power supply to the video board is supplied through a size O male jack whose center conductor is 12V DC. There is a power supply On-Off jumper, labelled JP4 on board. By removing this jumper and placing an ammeter across the pins, the current drawn by the entire board (including the HOTLink II transceiver) can be measured. The onboard voltage regulator (U3) has a single 3.3V output, provided by a non-isolated DC/DC converter with an input voltage range of 10.8V to 13.6V. It is required to prevent noise transfer from an external power source onto the board.

4.2 DVB and MPEG Overview

Digital Video Broadcasting is a video broadcast standard. Prior to DVB there were no universal standards for MPEG-2 transmission, and different manufacturers equipment did not always work together. To solve that problem, the DVB Standards Association created DVB as the standard interface to facilitate the integration of MPEG-2-based video delivery from multiple manufacturers.

DVB defines standards for television, multiple simultaneous standard definition television (SDTV), and communication to mobile TV receivers, with a choice of multicast and/or unicast. By using a DVB interactive return channel, enhanced user services can include customized web and television content, distance learning, interactive ordering and more.

Asynchronous Serial Interface (ASI) is a system for serial encoded transmission of different data rates, with a constant signaling rate, based on a layered structure of MPEG transport packets. A constant receiver clock is used. Data can be transported over several hundred meters on coaxial cable or many kilometers using fibre optics. The serial transfer of transport streams operates at a 270-MBaud rate and uses 8B/10B encoding. *Figure 4-2* shows the blocks of the coaxial cable Asynchronous Serial Transmission Link.

MPEG is a popular encoding and compression system for digital multimedia content defined by the Motion Picture Experts Group (MPEG). An uncompressed PAL TV picture requires a bandwidth of 216 Mbps which is far beyond the capacity of most radio frequency signals. Uncompressed NTSC requires 168 Mbps and the situation becomes more acute for HDTV with bandwidths exceeding 1 Gbps. MPEG-2 provides a way to compress this digital video signal to a more manageable rate. Because MPEG-2 provides good compression it has become a standard for digital TV.

The HOTLink II video board supports transmission of the MPEG-2 stream over DVB-ASI. MPEG-2 packet size can either be 188 or 204 bytes wide. This packet is comprised of a header and a payload. The header is a minimum of 4 bytes wide and starts with a Sync Byte (47'h). *Figure 4-3* shows the different fields of the MPEG-2 header. MPEG-2 addresses the combination of one or more elementary streams of video and auxiliary data into single or multiple streams which are suitable for storage or transmission. This is specified in two

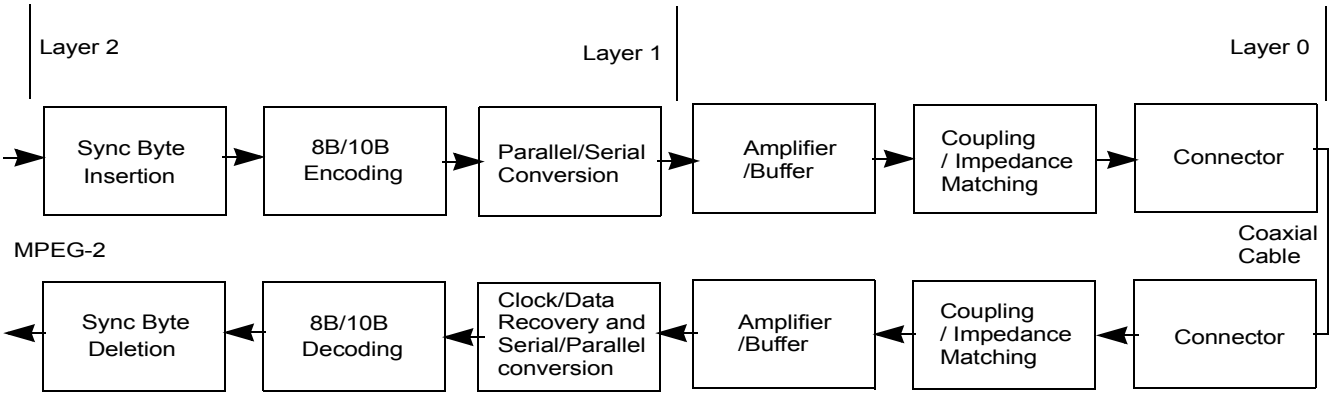


Figure 4-2.DVB-ASI Transmission Blocks

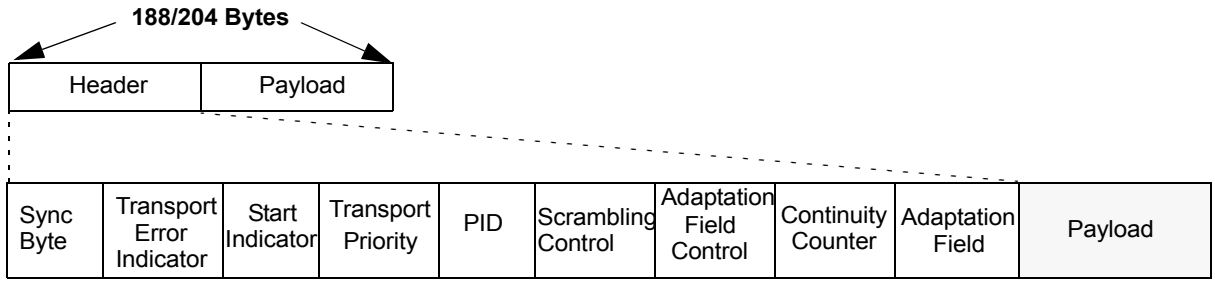


Figure 4-3.MPEG-2 Packet

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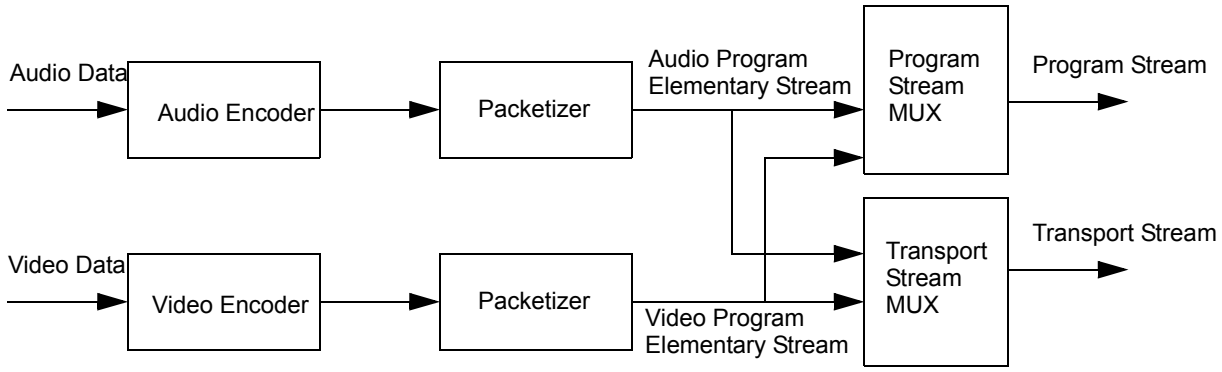


Figure 4-4.Example of MPEG-2 System Model

forms: the Program Stream and the Transport Stream. Each is optimized for a different set of applications. *Figure 4-4* shows a model for MPEG-2 systems.

The Program Stream is obtained by multiplexing one or more packetized elementary streams, which have a common time base into a single stream. It is designed for use in error free environments. Program Stream packets have variable lengths.

The Transport Stream is obtained by multiplexing one or more packetized elementary streams, which have one or more independent time bases, into a single stream. Packets in the same elementary stream all have the same PID (Packet Identifier), so that the decoder (or demultiplexer) can select the elementary stream(s) it wants and reject the rest. The Transport Stream is designed to be used in environments where errors are likely. Transport Stream packets are 188 bytes long. MPEG-2 signal is used in DBS (Direct Broadcast Satellite), CATV (Cable Television), HDTV (High Definition television), etc.

4.3 SMPTE 259M Overview

The ANSI/SMPTE 259M-1997 standard specifies a serial digital interface (SDI) for digital video equipment operating at either the 525 line, 60Hz video standard or the 625 line, 50Hz video standard. This standard describes how to transport standard definition video serially over a coaxial cable and also describes the encoding and decoding processes performed on the video bitstream for transportation across the physical layer.

The data rates supported by SDI range from 143Mb/s to 360Mb/s, depending on the digital format being transported. To be considered SMPTE 259M compliant, a device must support at least one of the data rates shown in *Table 4-1*.

Figure 4-5 shows the simplified block diagram of a SMPTE 259M link. On the transmit side, the data is scrambled and NRZI encoded before being passed to the serializer. The serializer performs the parallel to serial conversion and the NRZI encoded serial stream is then driven onto a coaxial cable via a cable/line driver. The character clock is multiplied by ten to provide the bit rate clock to the transmitter.

The receiver performs the inverse function of the transmitter. The clock and data recovery circuit accepts the serial data from the coaxial cable after equalization and extracts the bit rate clock, and the data from the transitions in the data stream. The bit rate clock is divided by ten to obtain a character rate clock. The received serial data is then deserialized and the parallel characters are passed to the descrambler/decoder which performs the NRZI-NRZ decoding and descrambling, to remove any extra transitions that were added at the transmitter. Finally, the bit stream is framed to the correct character boundaries to obtain the correct 10-bit parallel data.

Table 4-1.SDI Bit Rates

Support Level	Bit Rate (Mb/s)	Video Format	Standard
A	143	NTSC Composite	ANSI/SMPTE 244M–1995
B	177	PAL Composite	IEC 61179
C	270	4 x 3 Aspect Ratio 4:2:2 Component	ANSI/SMPTE 125M–1995 and ITU-R BT.601-5
D	360	16 x 9 Aspect Ratio 4:2:2 Component	ANSI/SMPTE 267M–1995 and ITU-R BT.601-5

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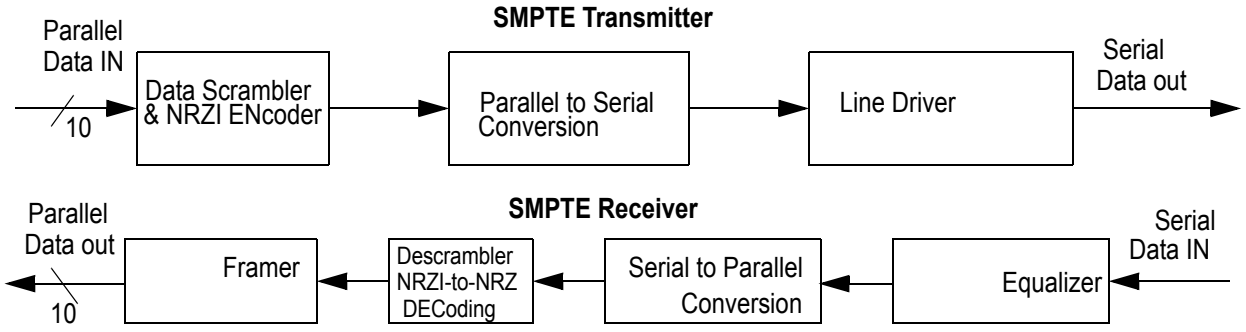


Figure 4-5.Cypress's SMPTE 259M Transmitter and Receiver Implementation

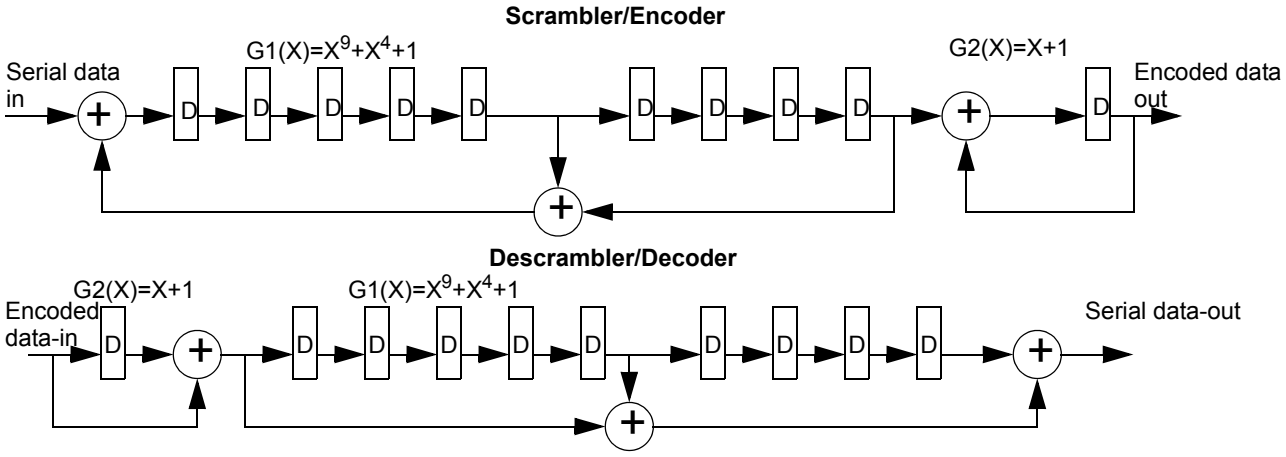


Figure 4-6.SMPTE 259M Scrambler/Encoder and Descrambler/Decoder

4.3.1 Scrambling/Descrambling

Scrambler codes are used to increase the number of transitions in the data stream in SMPTE 259M applications. The scrambler polynomial is $G1(X)=X^9+X^4+1$. *Figure 4-6* shows the implementation of the scrambler/NRZI encoder and the NRZ decoder/descrambler, as defined by SMPTE 259M. In the diagram, the box with a D inside represents a D flip flop. The circles with plus symbols inside are exclusive-OR gates. The LSB of the data word is sent first. The NRZ encoder converts the scrambled NRZ bitstream to a polarity free scrambled NRZI. The encode polynomial is G2(X) =X+1. At the receiver, the opposite function is performed i.e. from NRZI to NRZ using the G2(X)=X+1 function, followed by the descrambler polynomial $G1(X)=X^9+X^4+1$.

5.0 HEB Test Software Set-up and Operation

The software GUI needs to be installed from the resource CD included in the kit. Please follow instructions listed below for installing and running the various tests from the GUI.

5.1 HOTLink II Video Board Software Set-up Instructions

- Open the CD that was supplied with the kit and locate the file set-up.exe. Double click to run the executable.
- Follow the on screen instructions to set up the GUI. This will install the GUI for the HEB Test software to run on your PC/laptop. A Windows 2000/XP operating system environment is a minimum requirement to run the software.
- The HEBTest icon will now be available on your Desktop and/or as a Quick Launch item in your taskbar (depending on your selections during installation).
- Connect the 12V DC power supply to the power supply jack (J8) on the board. The board is now ready to be powered up.
- Connect the 12V AC/DC adapter to the mains power supply to power up the board. Initially, all the LEDs on the board will turn on.
- Connect the USB cable between the USB port of the video board and the PC/laptop. The LEDs will now turn off. Once the USB connection from PC/laptop is made, a window should pop up indicating that new hardware has been detected and the drivers are being configured. Note: The HS USB drivers may need to be installed if they are not present. This is left up to the user.
- Click on the HEBTest icon on your Desktop or Quick Launch taskbar. This will open the GUI interface for performing the tests as shown in *Figure 5-1*. The default window of the GUI is the Parallel Loop Back test window.
- Select the test to be performed on the Video Board by clicking on the appropriate tab, then on the applicable test, and then following the instructions in the "Notes" box. These tests will be described in subsequent sections.
- The tests that can be performed on the board are:

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1. Parallel Loop Back
2. Serial Loop Back
3. Function Test Suite.

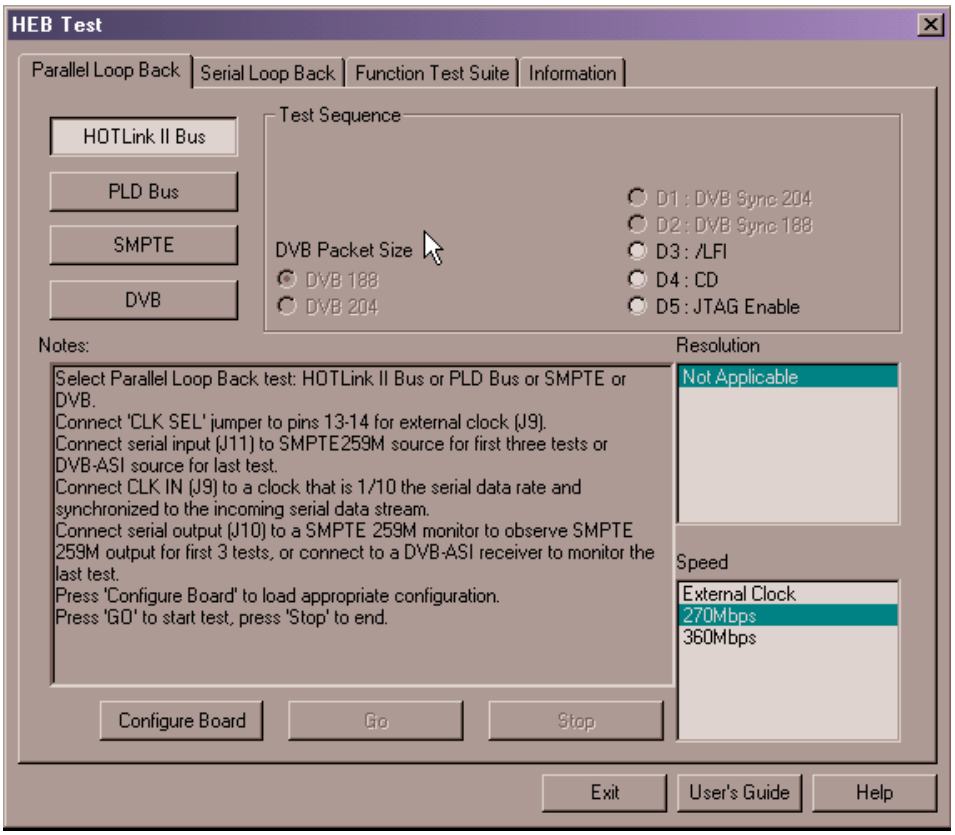


Figure 5-1.HEB Test GUI Window

5.2 Board Configuration Instructions

This section will explain how to configure the board for an arbitrary test. Please see the following sections for details on running specific tests.

- First select which set of tests you would like to run by clicking on the appropriate tab as mentioned in the previous section and shown in *Figure 5-1*. Within each tab there are four different methods of running that particular test. Choose the preferred method by pressing the appropriate button.
- The details regarding the connections to be made on the board for each test are specified in the “Notes” box of the test window. Follow the “Notes” box to configure the board for that test. A CLK SEL header, JP1 on board and a jumper are provided to select between different clocking options. The position of the jumper determines which clock is used as the REFCLK for the HOTLink II transceiver (a close view of the header pins and the pin descriptions are given in *Figure 5-2*, *Figure 5-3* and *Table 5-1*). The appropriate clock frequencies can be selected from the speed menu on the GUI test window.

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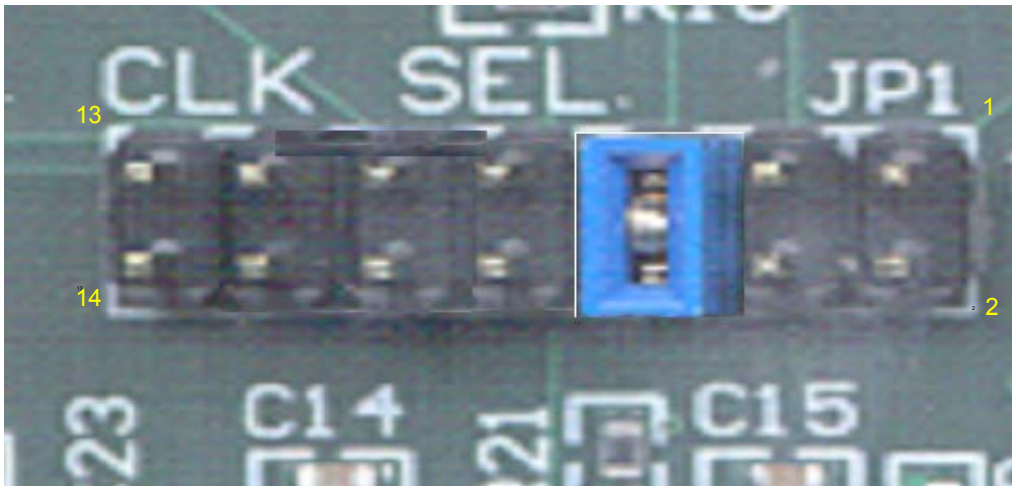


Figure 5-2.CLK SEL (JP1) Close View

Table 5-1.CLK SEL Pin Descriptions

Header Pin Number	Description
1 and 2	Jumper is connected to these two pins to use the on-board oscillator, X2.
3 and 4	Jumper is connected to these two pins when an external clock is used. The external clock input is given at SMA connector on board (J5).
5 and 6	Jumper is connected to these two pins to use the programmable CLKC output of CY22393. Currently not used.
7 and 8	Jumper is connected to these two pins to use the programmable CLKA output of CY22393. Currently 27 MHz or 36 MHz.
9 and 10	Jumper is connected to these two pins to use the programmable CLKB output of CY22393. Currently not used.
11 and 12	Jumper is connected to these two pins to use the programmable CLKD output of CY22393. Currently not used.
13 and 14	Jumper is connected to these two pins when an external clock is used.The external clock input is given at BNC connector on board (J9).

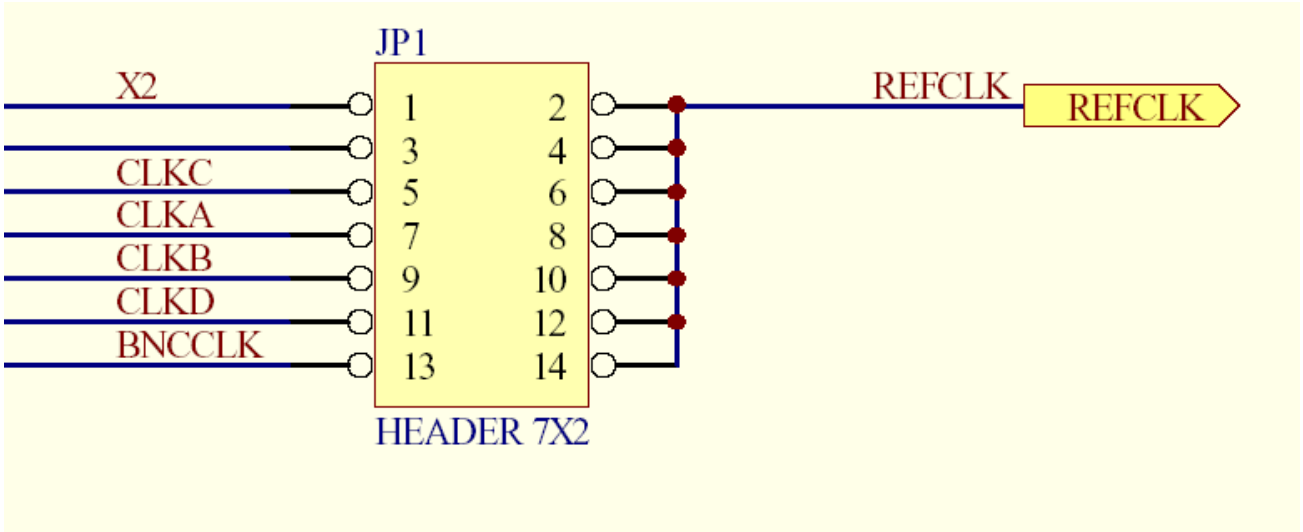


Figure 5-3. CLK SEL (JP1) Block Diagram

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- To configure the Delta 39K CPLD for the desired test, click on the “Configure Board” tab (the following sections will cover the detail of each configuration). A configuration window shown in *Figure 5-4*, is opened while the CPLD is being configured via the USB port. After the board is configured for the particular test selected, the configuration window closes automatically. The Delta39K is now configured with the desired test.
- Click on the “Go” tab to run the test and “Stop” to end it.
- The results can be viewed accordingly (the steps to run each and every test and the expected results are described in the next few sections).
- The indicators on the board and the test window are:

1. D1: DVB Sync 204/Board configuration
2. D2: DVB Sync 188
3. D3: /LFI (Link Fault Indicator)
4. D4: CD (Carrier Detect)
5. D5: JTAG Enable Indicator/Always ON when no JTAG.

A “Help” button at the bottom right hand corner of the test window shows the block diagrams and connections for each test, along with a description of each test.

5.3 Running the Tests

5.3.1 Parallel Loop Back Tests

These tests are a quick way of confirming that the board works for video applications. Other equipment required for this test (as shown in *Figure 5-5*) are a video source (DVD, video camera etc.), an A/D converter to convert the analog video from the source to a digital stream (either DVB-ASI or SMPTE 259M), a D/A converter to convert the digital streams back to analog, and a monitor to view the output from the source. The tests are performed by looping the serial outputs back to the serial inputs on the HOTLink II video board either through the CPLD or through external jumpers (LVTTL). Most of these tests require an external clock that is frequency and phase locked to 1/10 the input serial data rate to make the system synchronous (DVB loop back test can use one of the internal clocks). The clock for the example shown will need to

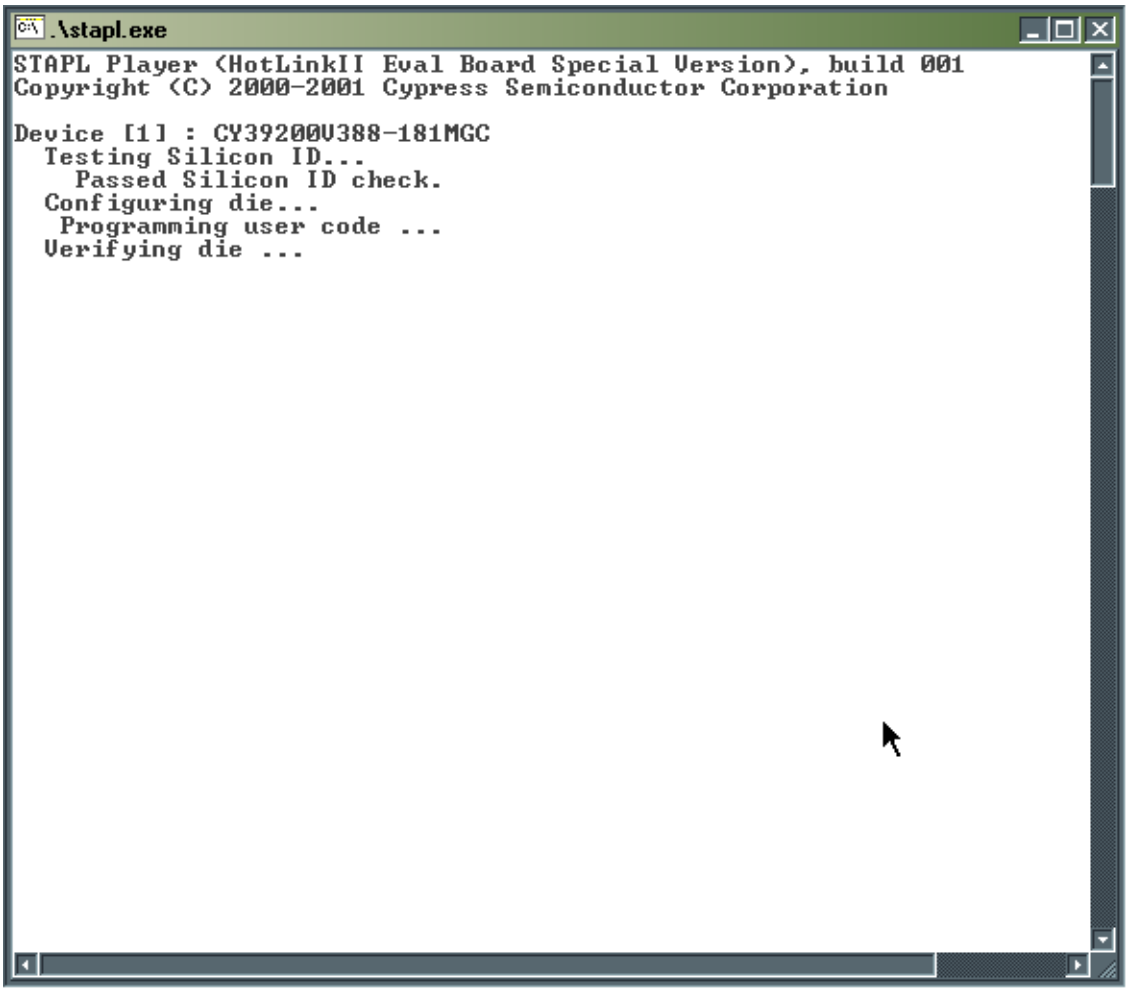


Figure 5-4.Configuration Window for All Tests

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come from the A/D converter and can be input to the HOTLink II video board via the BNC clock input (J9). This clock is needed as there will be a slight ppm difference in frequency between the crystal on the board and the clock in the A/D. If an on-board clock is used, e.g., X2, there will be a slight frequency mismatch between it and the source clock (A/D converter in the example shown). In this case, there will be a slight frequency mismatch because the transmit path of the HOTLink II transceiver is clocked with the REFCLK and the data will be clocked in to the transmit path with the recovered clock. This will be seen as green and pink lines on the monitor. If your particular application requires this exact type of functionality, please contact Cypress technical support for a solution.

The GUI for the Parallel Loop Back Tests is shown in *Figure 5-6*. The different parallel loop back test modes are described as follows:

1. HOTLink II Bus: The CPLD is configured to loop the HOTLink II transceiver parallel output data bus to the parallel input data bus.

   • In the HOTLink II Bus test, raw data from the HOTLink II transceiver is sent to the Delta39K CPLD and looped back into the HOTLink II transceiver. The data is not even registered in the CPLD i.e. it is passed through it.

2. PLD Bus: Using the external jumper cable, the LVTTL inputs and outputs are shorted, allowing the data in its raw state to be looped back through both the CPLD and the HOTLink II transceiver.

   • In the PLD Bus test, the raw data from the HOTLink II transceiver is sent to the Delta39K CPLD where it is registered and transferred to the LVTTL output header. It is then looped back into the LVTTL input and back to the CPLD, from where it is sent to the HOTLink II transceiver and out through the cable driver.

3. SMPTE: The SMPTE scrambler/descrambler are invoked in the CPLD. Once a SMPTE 259M video stream is accepted by the HOTLink II transceiver, it is passed to the CPLD which performs descrambling and framing functions. The decoded video data is then sent to the LVTTL output bus. This data can be looped back through the LVTTL input bus, or another video data stream can be placed on the LVTTL input bus.

   • In the SMPTE Loop Back test, raw data from the HOTLink II transceiver is sent to the Delta39K CPLD where it is descrambled, framed, and sent to the LVTTL output. The data is then looped back through the LVTTL input header and back to the Delta39K CPLD. The scrambler in the CPLD scrambles the data and then sends the data to the HOTLink II transceiver which serializes the data and transmits it via the cable driver.

4. DVB: In this test, the transmit and receive FIFOs and state machines are invoked in the CPLD. The HOTLink II transceiver performs the 8B/10B ENDEC. Once a video stream is injected into the HOTLink II transceiver the decoded video data is passed to the CPLD and then presented on the LVTTL output bus. This data can be looped back through the LVTTL input, or another video data stream can be placed on the LVTTL input bus.

   • In the DVB-ASI test, unencoded 8-bit data (in the form of MPEG-2 packets with two K28.5s between packets) is passed from the HOTLink II transceiver to the Delta39K CPLD. The CPLD uses the recovered clock from the HOTLink II transceiver to clock the state machine and RXFIFO. The receive state machine considers all K28.5s as idle characters and removes them, but retains the 47H MPEG sync byte and the data is then sent to the RXFIFO (used for rate matching in typical DVB-ASI systems). The transmit state machine inserts the K28.5s back into the frame and transfers the data from the TXFIFO to the HOTLink II transceiver. The K28.5s will not necessarily be inserted in the same order as they were received. If there is no data, K28.5s will be inserted between packets.

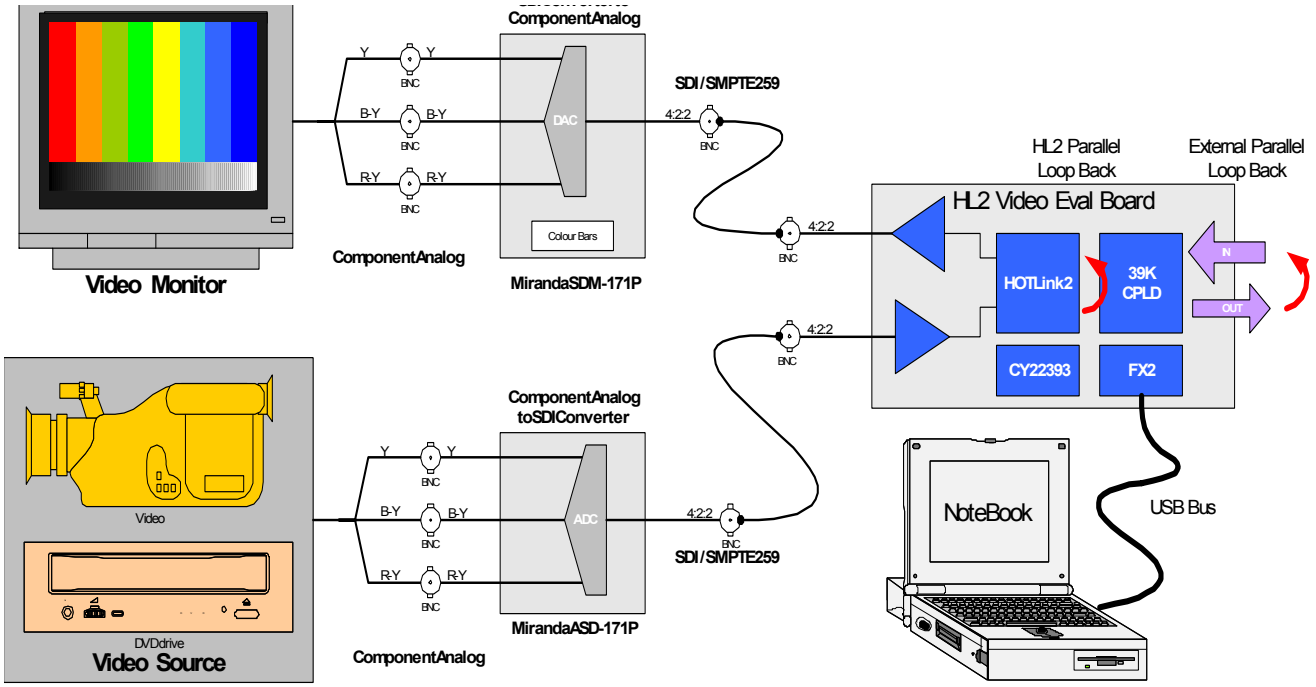


Figure 5-5.Parallel Loop Back Hardware Test Set-up

[+] Feedback

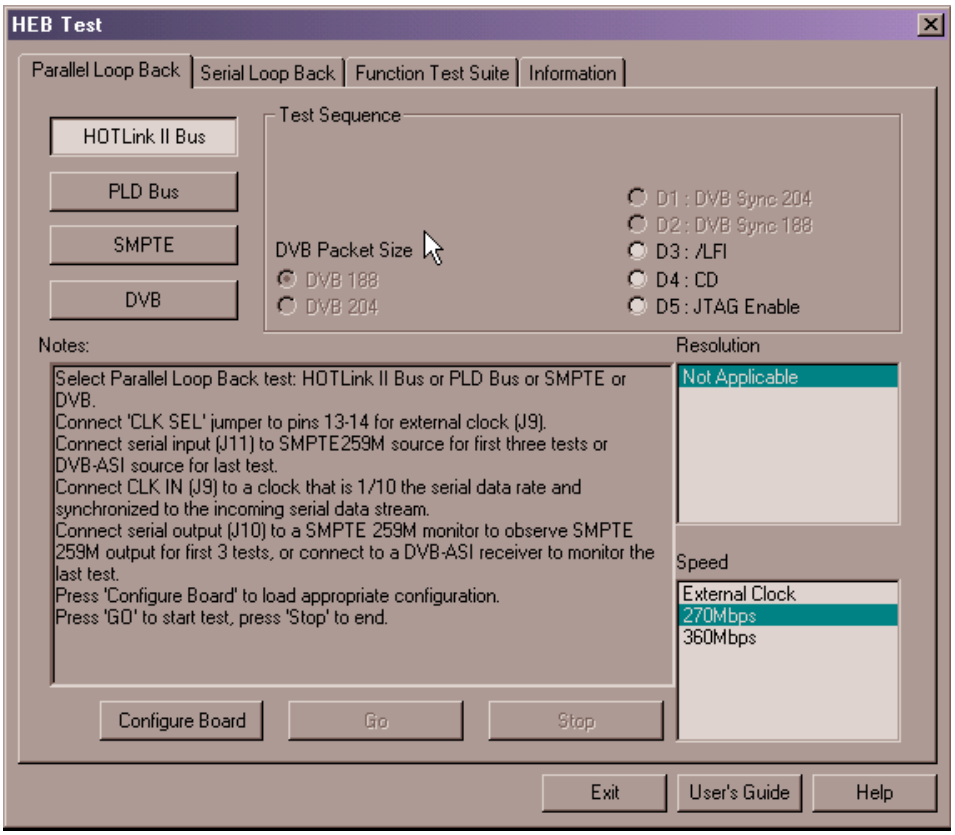


Figure 5-6.Parallel Loop Back Test Window

Running the Test:

- Click on the “Parallel Loop Back” tab of the GUI test window, as shown in *Figure 5-6*. Choose the desired test by pressing the appropriate button. HOTLink II Bus test is shown in *Figure 5-6*.
- Set up the board for the test by following the instructions in the “Notes:” section of the GUI.
- Connect the “CLK SEL” jumper across 13–14 of JP1 on board.
- Connect a serial input (J11) to a SMPTE 259M source for the first three tests or a DVB-ASI source for the fourth test. Hardware test set-up is shown in *Figure 5-5*.
- Connect CLK IN (J9) to a clock that is 1/10 the serial data rate and is synchronized to the incoming serial data stream (This connection is made when an external clock is used).
- Connect serial output (J10) to a SMPTE 259M monitor to observe SMPTE 259M output for the first 3 tests or connect a DVB-ASI receiver to monitor the fourth test.
- Ensure that LVTTL IN (P3) and LVTTL OUT (P4) are connected using a ribbon cable.
- Select the clock frequency from the “Speed” menu on the test window.
- Press “Configure Board” to load the appropriate configuration.
- Once the configuration window closes, press “Go” to start the test and “Stop” to end.
- The SMPTE 259M or DVB from the source will be viewable on the monitor.

Repeat the above procedure for each test, noting that the board will need to be reconfigured each time a different test is desired.

5.3.2 Serial Loop Back Tests

This test is a confirmation of the quality of the HOTLink II SERDES device to meet industry standard pathological test patterns. In the serial loop back tests, the SMPTE pathological test patterns (as per SMPTE EG 34-1999, see reference 7) are generated in the Delta39K CPLD and sent to the HOTLink II transmitter. The HOTLink II transmitter serializes the data and sends it out serially through the cable driver and transformer at J10 onto the cable. The data is then looped back to input J11 on board. It is then passed through a transformer and equalizer and sent to the HOTLink II transceiver serial inputs where it is deserialized. The received serial data is sent from the HOTLink II receiver to the Delta39K CPLD where it is framed and compared to the data pattern that is being sent. This is illustrated in *Figure 5-7*. The average number of bits in errors divided by the number of bits transmitted, or bit error rate (BER), is tracked and displayed in the GUI. Do not try to view the serial outputs from these tests on a SMPTE 259M monitor as the data is not scambled as required by the SMPTE 259M standard.

The serial loop back test window of the GUI is shown in *Figure 5-8*. The different serial loop back test modes are described as follows:

[+] Feedback

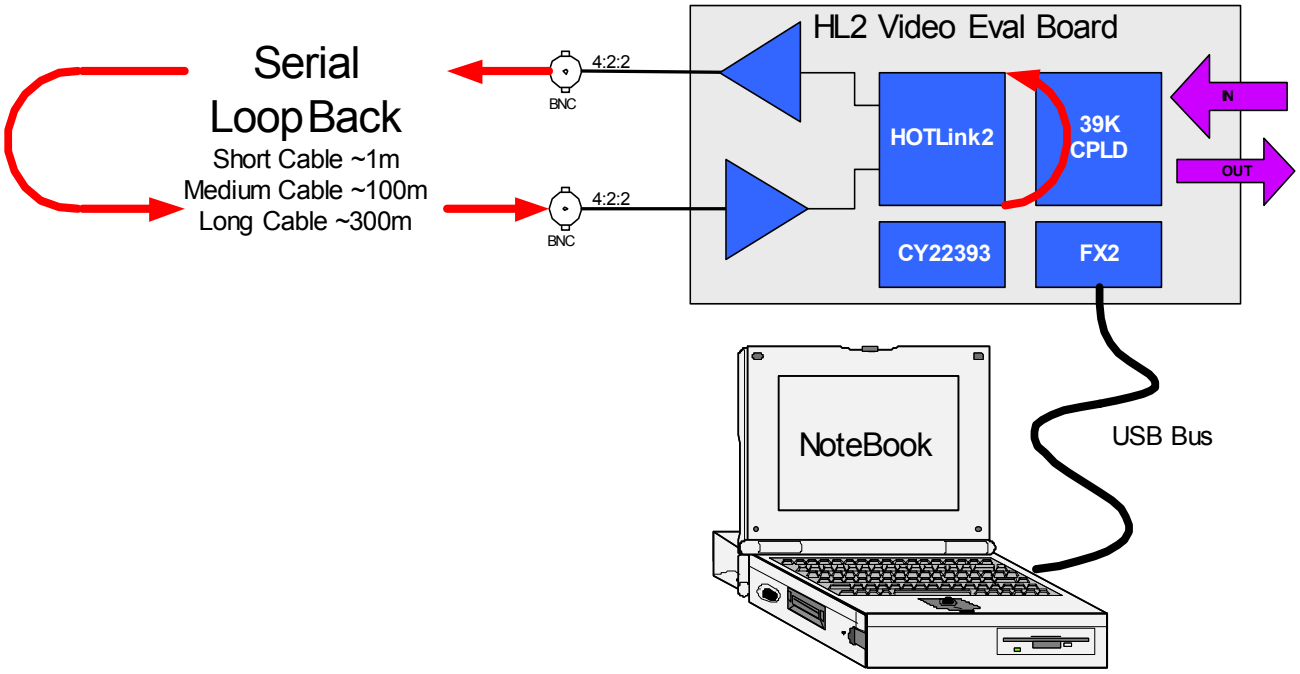


Figure 5-7.Serial Loop Back Hardware Set-up

1. Bit Error Rate: This test will enable the user to define the mark space ratio of one's and zero's and how many times the sequence is repeated. Once configured, the test will either loop for the number of frames specified, or indefinitely if a value of zero (or a blank) is entered in the Repeat Seq. (lines) box of the GUI test window. The BER will display the number of bits in error divided by the number of bits transmitted.

The pathological tests are performed by inserting the testing sequences in a pseudo video frame. In order to identify the beginning of a video frame, there is a preamble to get byte alignment. For the first pathological test, the testing sequence is inserted once per scan line in a video frame. The other two pathological tests give the user the option of repeating the patterns in multiple scan lines in a video frame, as specified in the Repeat Seq. (lines) box.

2. Pathological Test 1: In this test, there are 44 bit times without a transition in the serial data stream. Once configured, the test will loop indefinitely if a value of 0 (or a blank) is entered in the Repeat Seq. (lines) box. The BER will display the number of bits in error divided by the number of bits transmitted.
3. Pathological Test 2: In this test, the data stream is a pattern of 20 ones followed by 20 zeros. The user will be able to define how many times the sequence is injected. It is possible for a PLL to lock to the incorrect frequency and/or to maintain phase lock when it is provided with a signal with a low transition density. This is why a test such as this is particularly stressful on a clock and data recovery (CDR) PLL. Passing the pathological pattern however demonstrates the robustness of the HOTLink II CDR PLL. Once configured, the test will either loop for the number of frames specified, or indefinitely if a value of 0 (or a blank) is entered in the Repeat Seq. (lines) box. The BER will display the number of bits in error divided by the number of bits transmitted.
4. Pathological Test 3: In this test, the serial data pattern is either a one followed by 19 zeros or 19 ones followed by a zero (equalizer stress test). The user will be able to define how many times the sequence is repeated. Once configured, the test will either loop for the number of frames specified or indefinitely if a value of 0 (or a blank) is entered in the Repeat Seq. (lines) box. The BER will display the number of bits in error divided by the number of bits transmitted.

Running the Test

- Click on the "Serial Loop Back" tab on the GUI test window as shown in *Figure 5-8*. Select the test that has to be performed by pressing the appropriate button. Bit Error Rate test is selected in *Figure 5-8*.
- Set up the board for the test by following the instructions in the "Notes:" section of the GUI. The next few steps duplicate this section.
- Connect the serial input (J11) to the serial output (J10).
- Connect CLK IN (J9) to an external clock if required.
- Connect CLK SEL jumper to pins: 1–2 for onboard oscillator, pins 7–8 for programmable CLKA output of CY22393 (on board clock - U1), pins 13–14 for external clock on J9.
- Select the clock frequency from the "Speed" menu of the test window.
- Set the "Test Sequence" menu to the desired values by entering the values you wish to test. For Bit Error Test, fill in the zeros, ones, and Repeat Seq. (lines) boxes. For the Pathological test, the number of zeros and ones are predetermined as per the SMPTE Engineering Guidelines (EG-34).
- Press "Configure Board" to load appropriate configuration.

[+] Feedback

- Once the configuration window closes, press “Go” to start the test and “Stop” to end.

The detection of errors, if any, are indicated in the BER window. **Note**: to force errors, disconnect and then reconnect the serial cable. While the cable is disconnected, N/A will appear in the BER box. This indicates that when there is no signal, BER is Not Applicable (as all the bits are errors). When you reconnect the cable however, a value will appear in the BER box as the HOTLink II CDR PLL regains lock. This number will decrease over time as the BER box indicates:

BER = # of bits in error / # of bits transmitted Eq. 1

Therefore, as the number of bits in error decreases relative to the number of bits transmitted, the BER decreases.

The repeat sequence option indicates the number of times the particular pathological test sequence is repeated in a frame. The user is given the option of entering any positive number up to 240. The default value is 1.

The same procedure has to be followed for all the tests. The board has to be configured every time different test is performed.

5.3.3 Function Test Suite Tests

This test provides a quick confirmation that the board works for video applications. This test can be used to generate the standard video test patterns and display them on a SMPTE 259M compatible monitor. The functional test suite generates NTSC and PAL test patterns in SMPTE259 C and D digital formats. These patterns include EG1 Color Bars, Grey Pattern, RP178 and RP178 Alternate test patterns. These patterns can be viewed on an RGB color monitor using a D/A converter as shown in *Figure 5-9*.

The test patterns can be viewed using a SMPTE or DVB decoder module and a standard monitor connected to the output of the HOTLink II board via the 75-ohm cable connector. Based on the user defined variables and standard selected (image size and speed), the various frames will be loaded into the CPLD and transmitted to the output of the HOTLink II board. The LVTTL input and output buses will be put in a High-Z state and the HOTLink II receiver is also ignored.

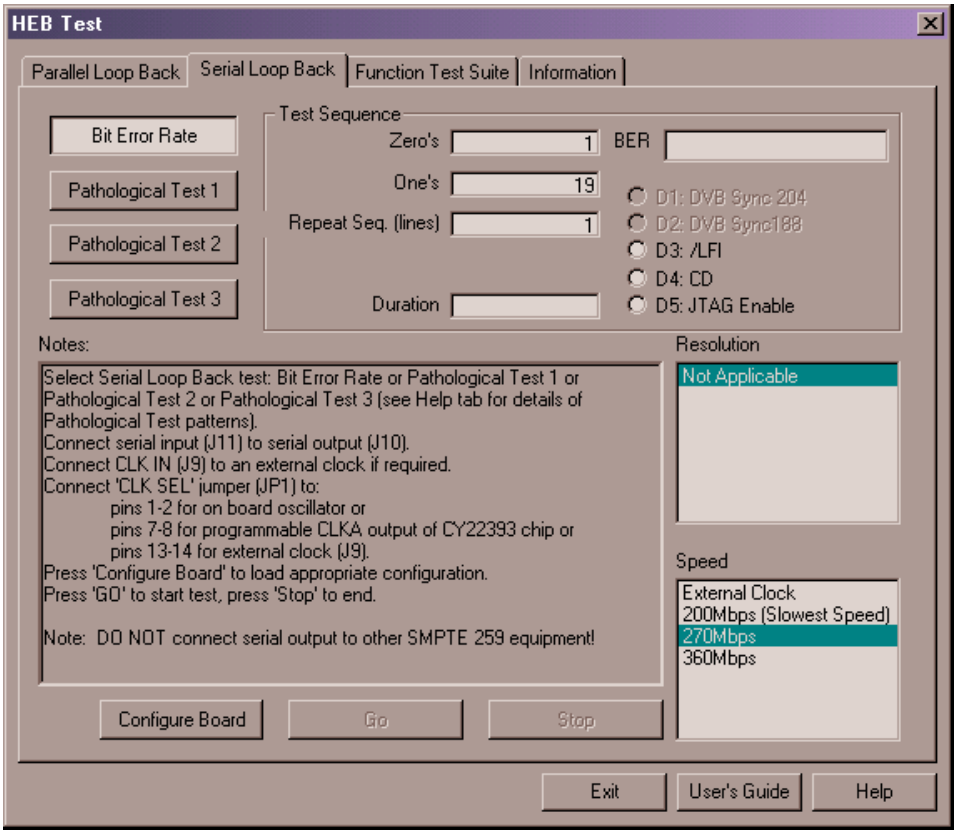


Figure 5-8.Serial Loop Back Test Window

[+] Feedback

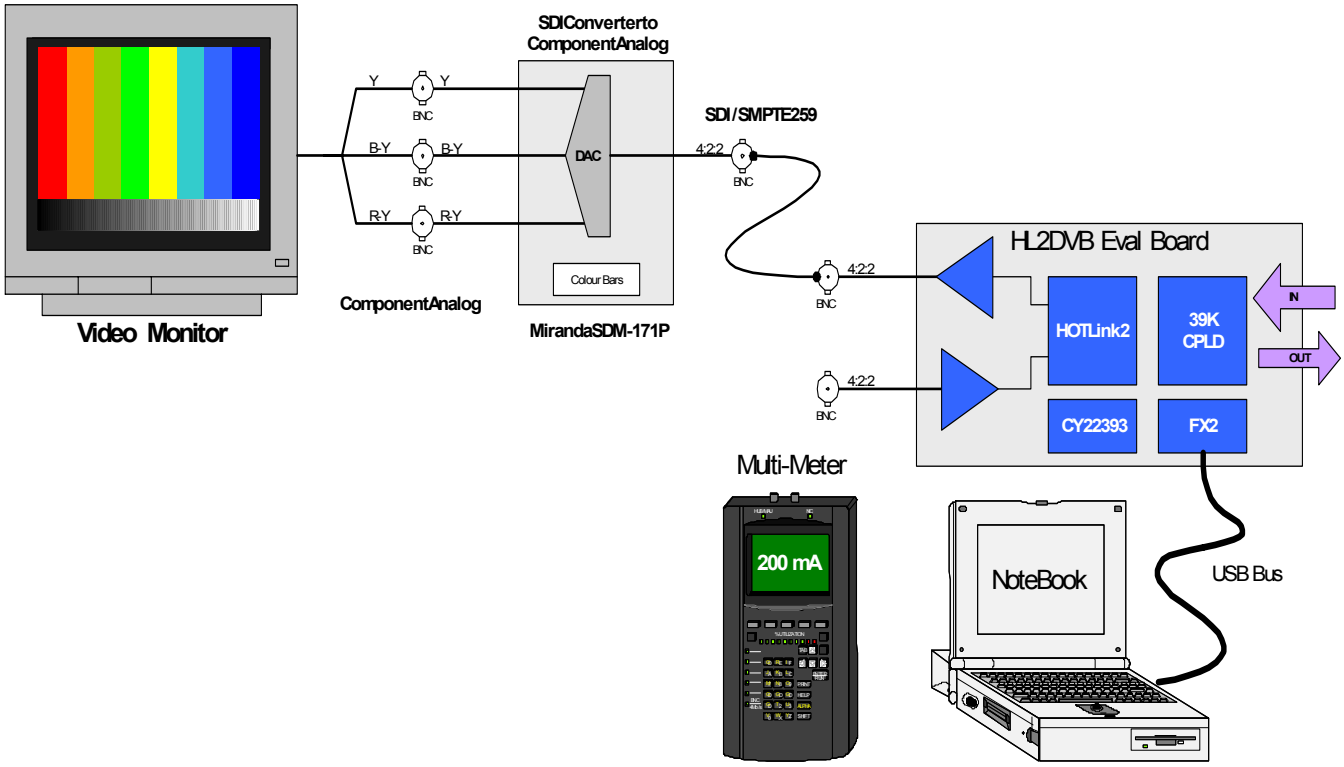


Figure 5-9.Functional Test Suite Hardware Set-up

The Delta39K CPLD is programmed through the USB Micro-controller with the Functional Test Suite. Different data patterns, depending on which test is selected, are generated by the state machines in the CPLD. The pattern generated is then SMPTE scrambled in the CPLD, serialized by the HOTLink II transmitter, converted back to analog form by the D/A converter, and displayed on the monitor. The GUI test window for this test is shown in *Figure 5-10*.

The different test modes in the Function Test Suite are as follows:

- Color Bars: Using a standard set of tabled images supporting the various screen sizes, a colored standard bar graph image will be transmitted to the HOTLink II board via the USB Link and then out to the monitor via the HOTLink II device. The expected result is shown in *Figure 5-11*.
- Grey Test: Using a standard set of tabled images supporting the various screen sizes, a grey standard image will be transmitted to the HOTLink II board via the USB link and then out to the monitor via the HOTLink II device. The expected result is shown in *Figure 5-11*.
- RP178 & RP178 Alternate: Using a standard set of tabled images, a sequence of images supporting the various screen sizes will be transmitted to the HOTLink II board via the USB link and then out to the monitor via the HOTLink II device. The expected results are shown in *Figure 5-12*.

Running the Test

- Click on the “Function Test Suite” tab on the GUI test window. *Figure 5-10* shows the “Function Test Suite” test tab selected and the EG1 Color Bars button pressed. Please note that for this test, the board need only be configured once at the beginning. To change the pattern displayed on the monitor, it is only necessary to “Stop” the present test, click on another and press “Go”.
- Set up the board for the test by following the instruction in the “Notes:” section of the GUI. The next few steps duplicate this section.
- Select the SMPTE 259M-C or SMPTE 259M-D configuration from the “Test Sequence” option on the test window.
- Select the “Resolution” on the test window to NTSC (525 Line) or PAL (625 Lines).

[+] Feedback

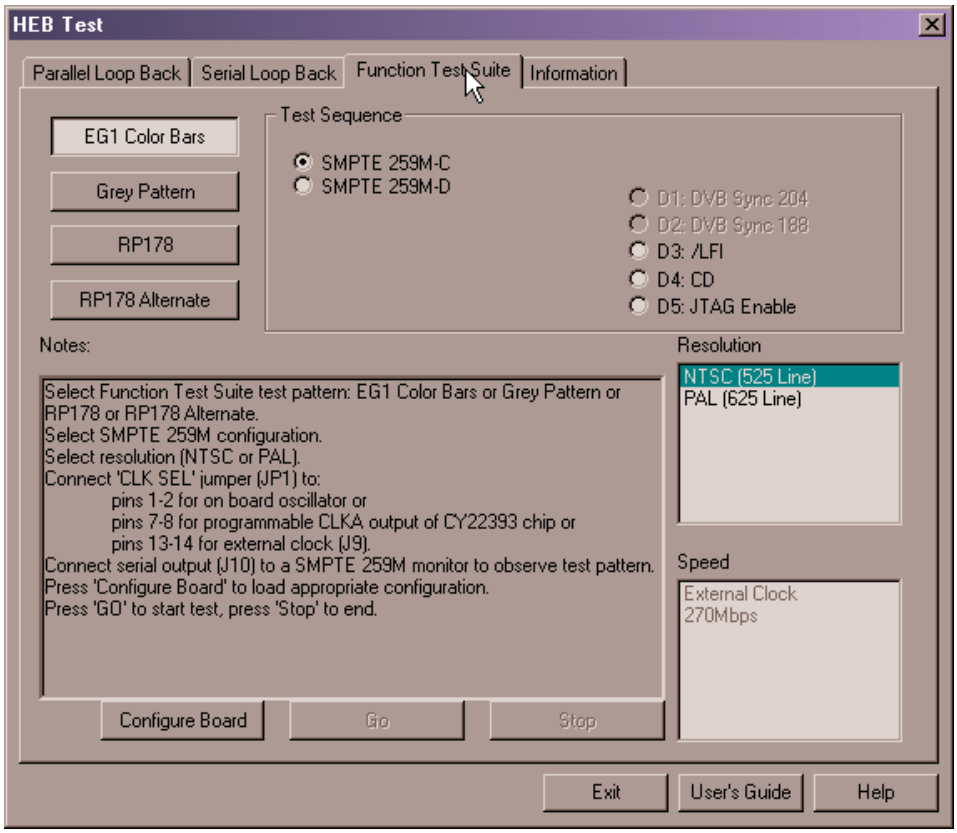


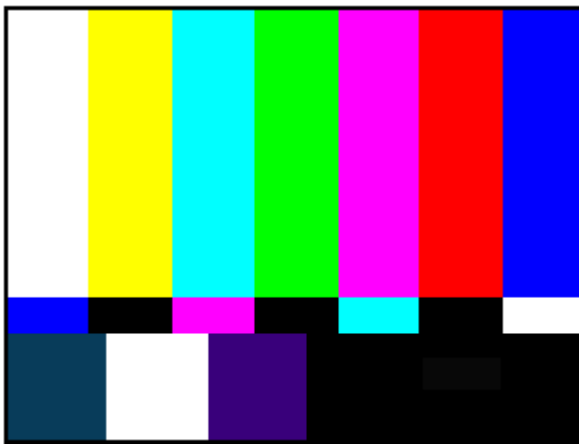
Figure 5-10.Functional Test Suite Test Window

- Connect CLK SEL jumper to pins: 1–2 for onboard oscillator, pins 7–8 for programmable CLKA output of CY22393 (on board clock - U1), pins 13–14 for external clock on J9.
- Connect serial output (J10) to a SMPTE 259M monitor (via a D/A converter) to observe the test pattern.
- Press “Configure Board” to load the appropriate configuration.
- Once the configuration window closes, press “Go” to start the test and “Stop” to end. The expected results are as shown in *Figure 5-11* and *Figure 5-12*.

Once the board is configured, any of the tests in the Function Test Suite can be performed, i.e. the board need not be reconfigured every time a different test is performed. Simply press “Stop” and then select the next test and press “Go” again to run each test.

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EG1 Color Bars



Grey Pattern

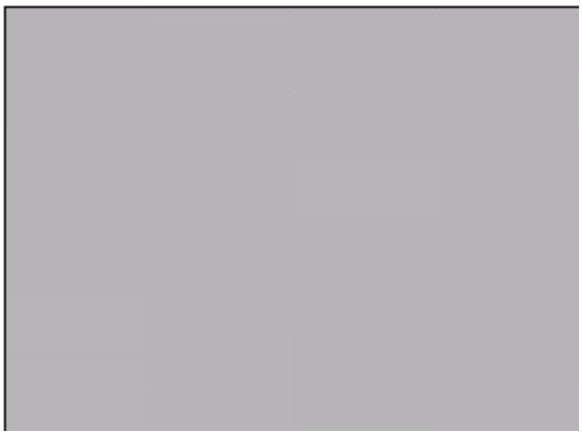


Figure 5-11.Functional Test Suite Expected Results

[+] Feedback

RP-178



RP-178 Alternate

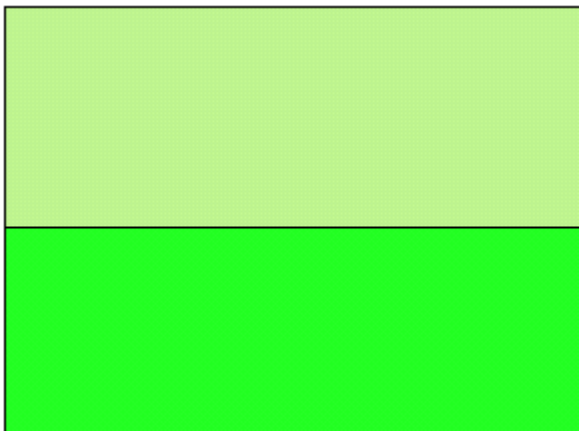


Figure 5-12.Functional Test Suite Expected Results

6.0 References

1. *Television — 10-Bit 4:2:2 Component and 4fSC Composite Digital Signals – Serial Digital Interface*, ANSI/SMPTE 259M –1997, Society of Motion Picture and Television Engineers, 1997.
2. *Television — Component Video Signal 4:2:2 – Bit-Parallel Digital Interface*, ANSI/SMPTE 125M–1995, Society of Motion Picture and Television Engineers, 1995.
3. *Television — System M/NTSC Composite Video Signals - Bit-Parallel Digital Interface*, ANSI/SMPTE 244M–1995, Society of Motion Picture and Television Engineers, 1995.
4. *Television — Bit-Parallel Digital Interface – Component Video Signal 4:2:2 16x9 Aspect Ratio*, ANSI/SMPTE 267M–1995, Society of Motion Picture and Television Engineers, 1995.
5. *Interfaces for CATV/SMATV Headends and Similar Professional Equipment*, DVB Document A010, October 1995.
6. *Fibre Channel Physical Standard*, ANSI X3.230–1994,American National Standards Institute, 1994.
7. *Pathological Conditions in Serial Digital Video Systems*, SMPTE Engineering Guidelines, EG 34–1999, Society of Motion Picture and Television Engineers, 1999.
8. *Serial Digital Interface Checkfield for 10-Bit 4:2:2 Component and 4fsc Composite Digital Signals*, SMPTE Recommended Practices, RP 178–1996, Society of Motion Picture and Television Engineers, 1996.

[+] Feedback

Appendix A: Schematics of HOTLink II Video Evaluation Board

[+] Feedback

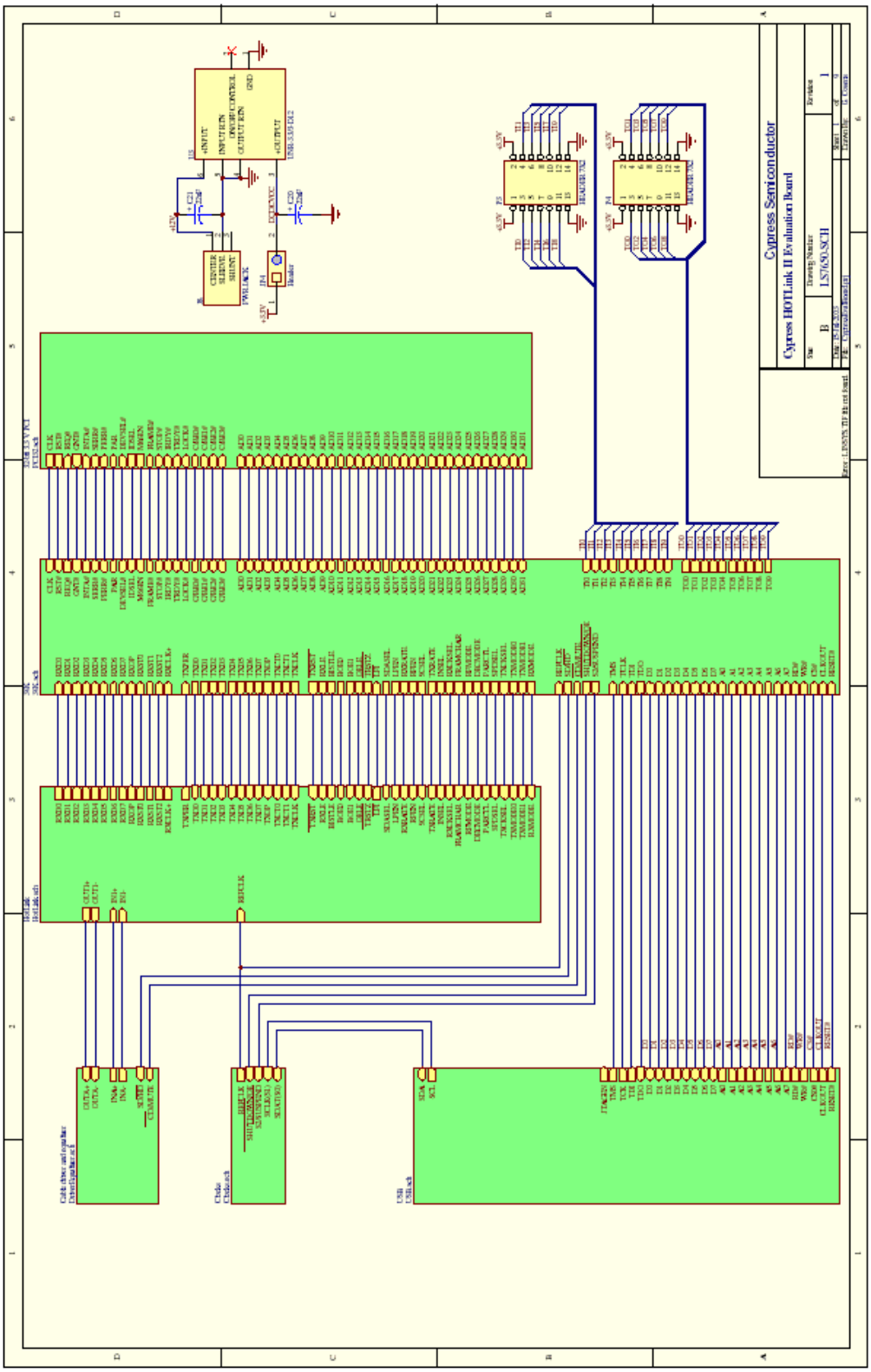


Figure A-1. Top Level Schematic (CypressEvalBoard.prj)

[+] Feedback

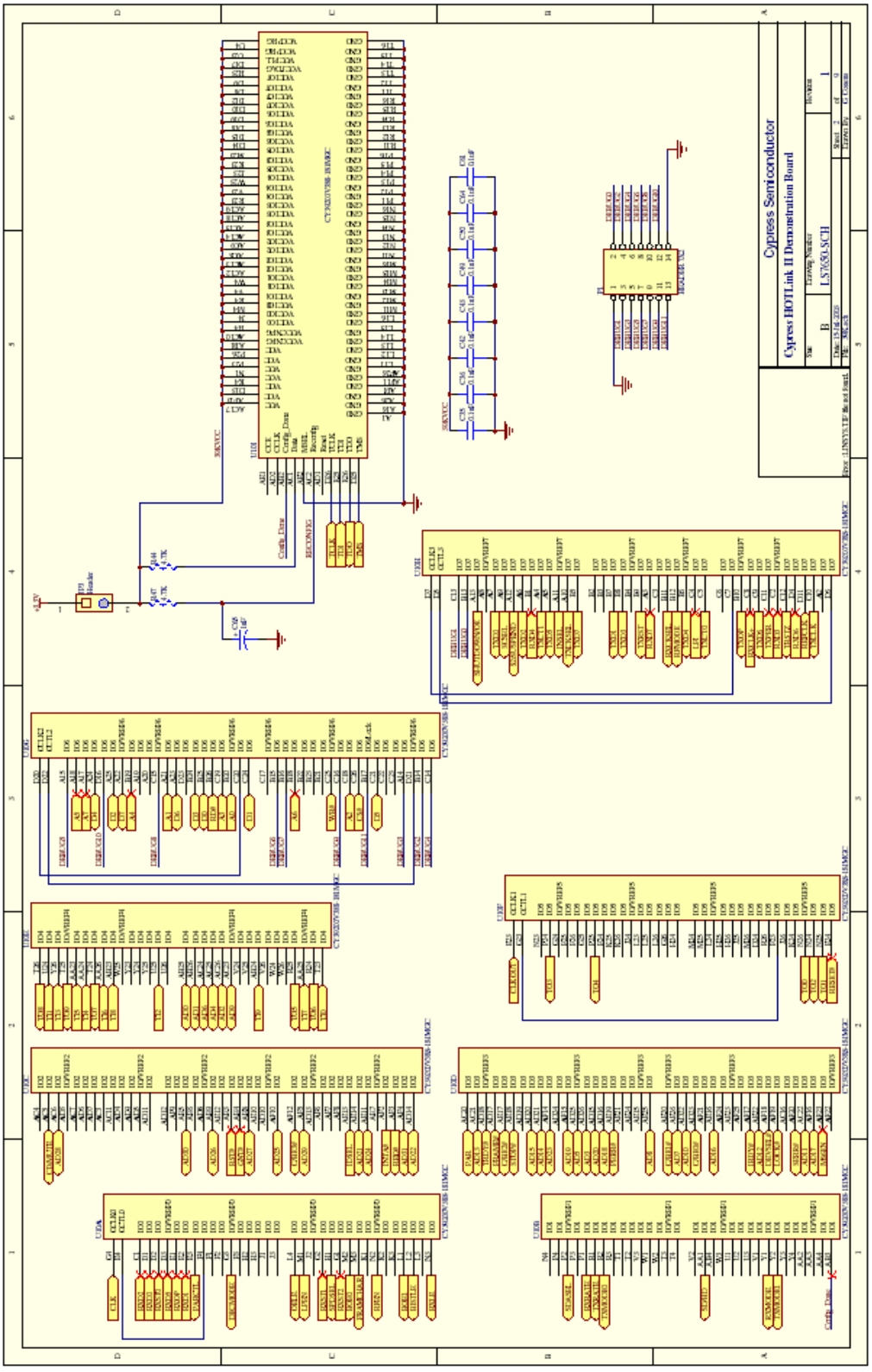


Figure A-2. Delta39K CPLD Schematics (39K.sch)

[+] Feedback

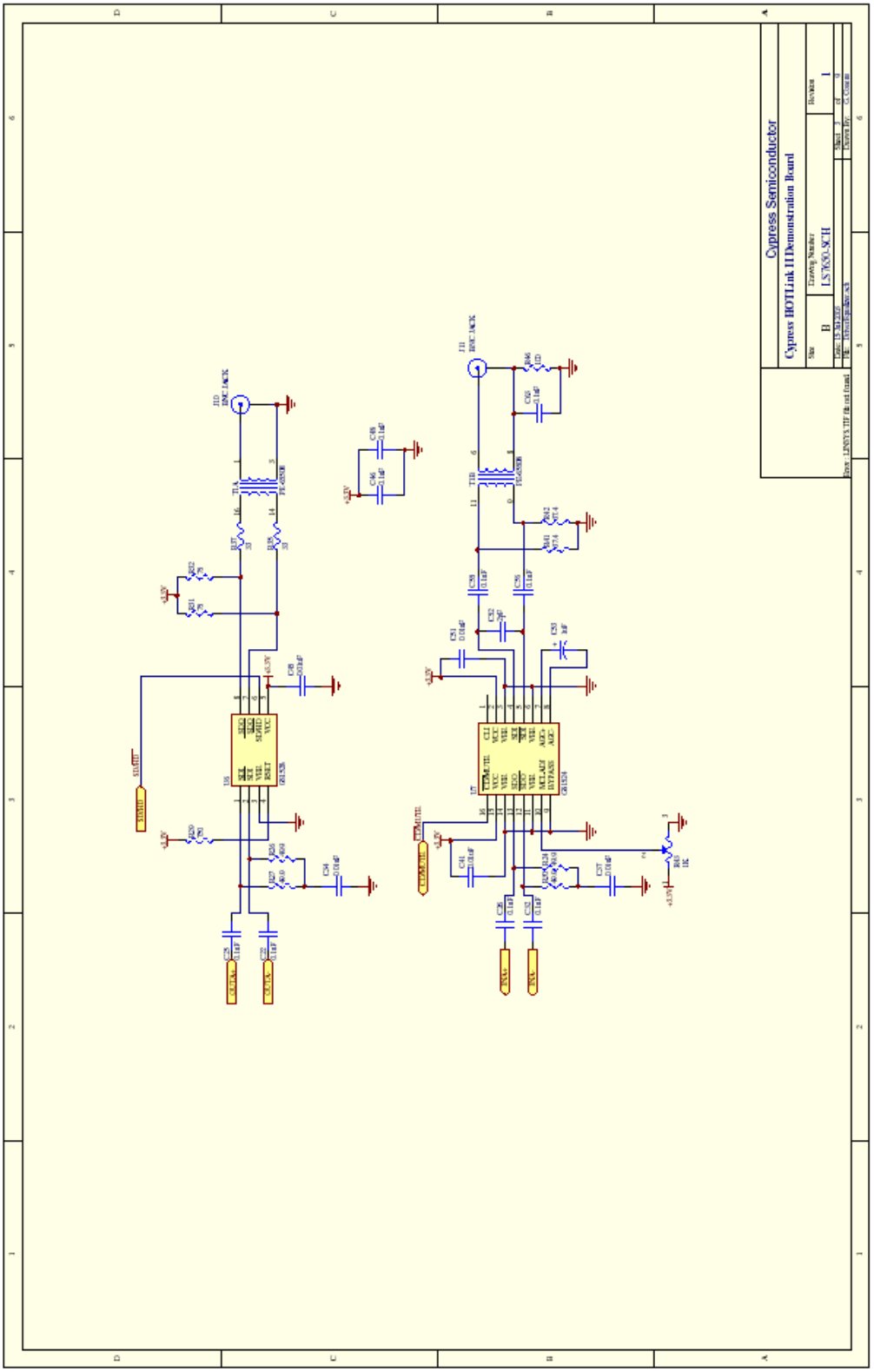


Figure A-3. Cable Driver and Equalizer Schematics (DriverEqualizer.sch)

[+] Feedback

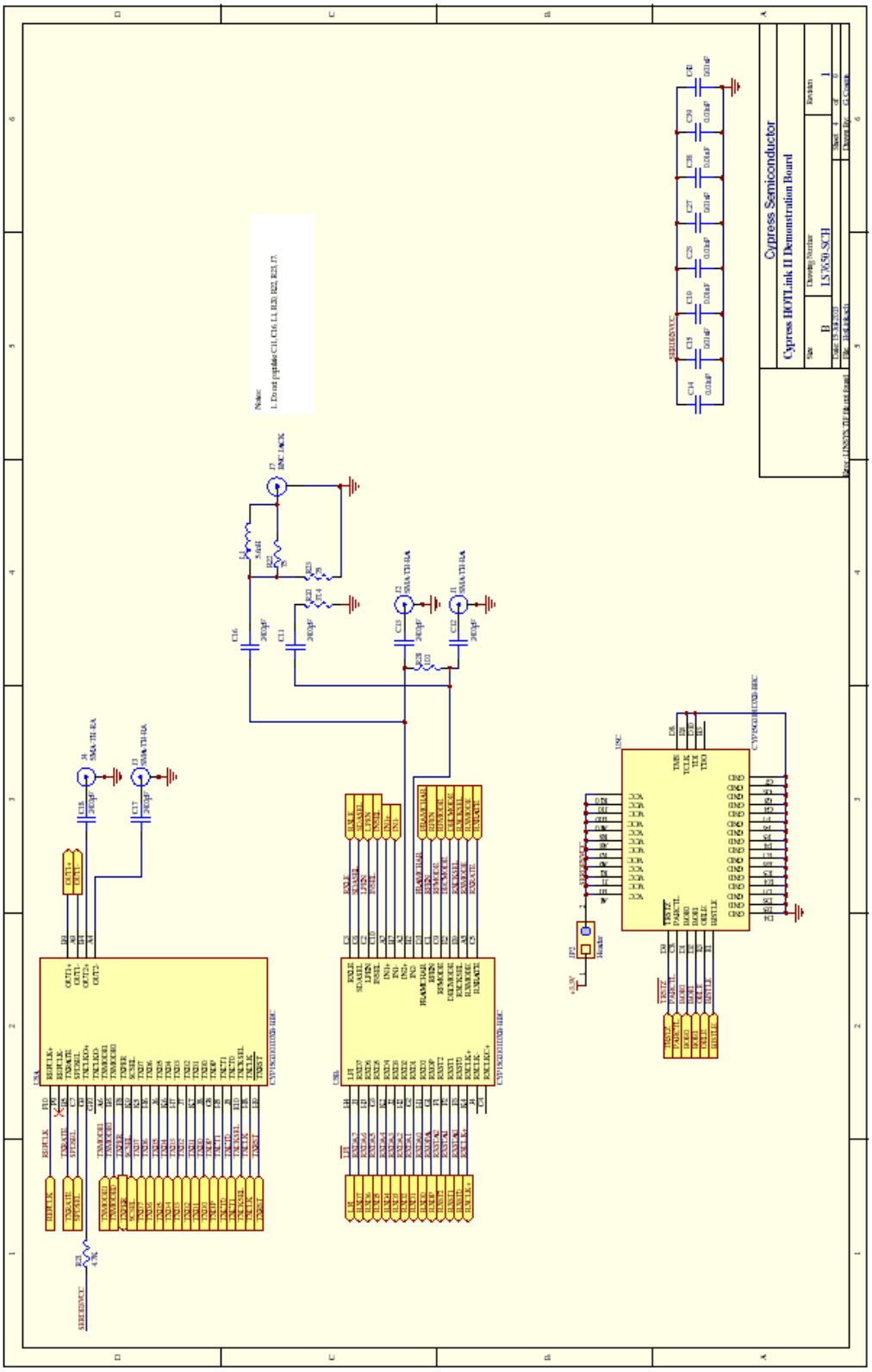


Figure A-4. HOTLink II Schematics (HOTLink.sch)

[+] Feedback

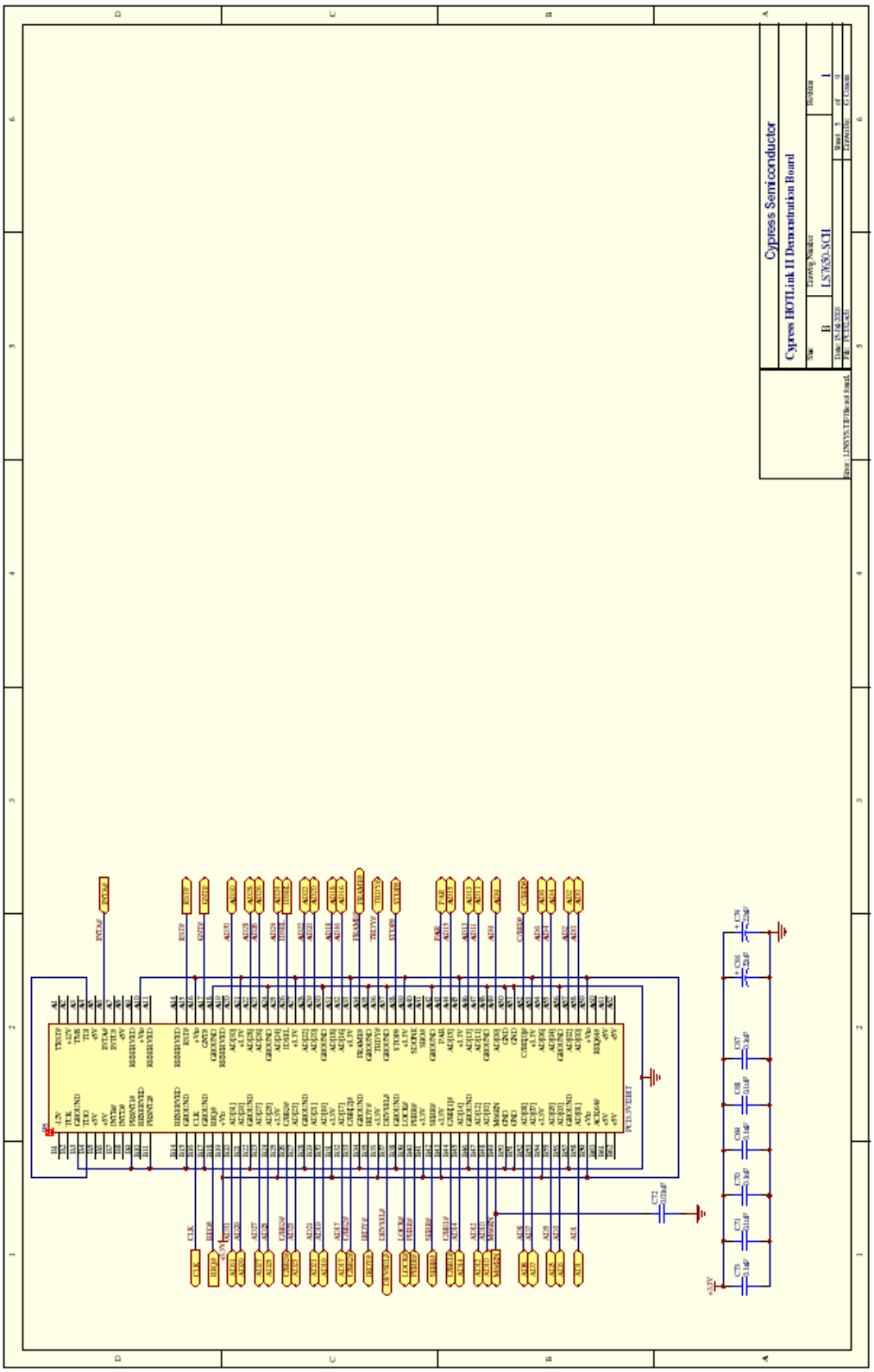


Figure A-5. PCI Bus Schematics (PCI32.sch)

[+] Feedback

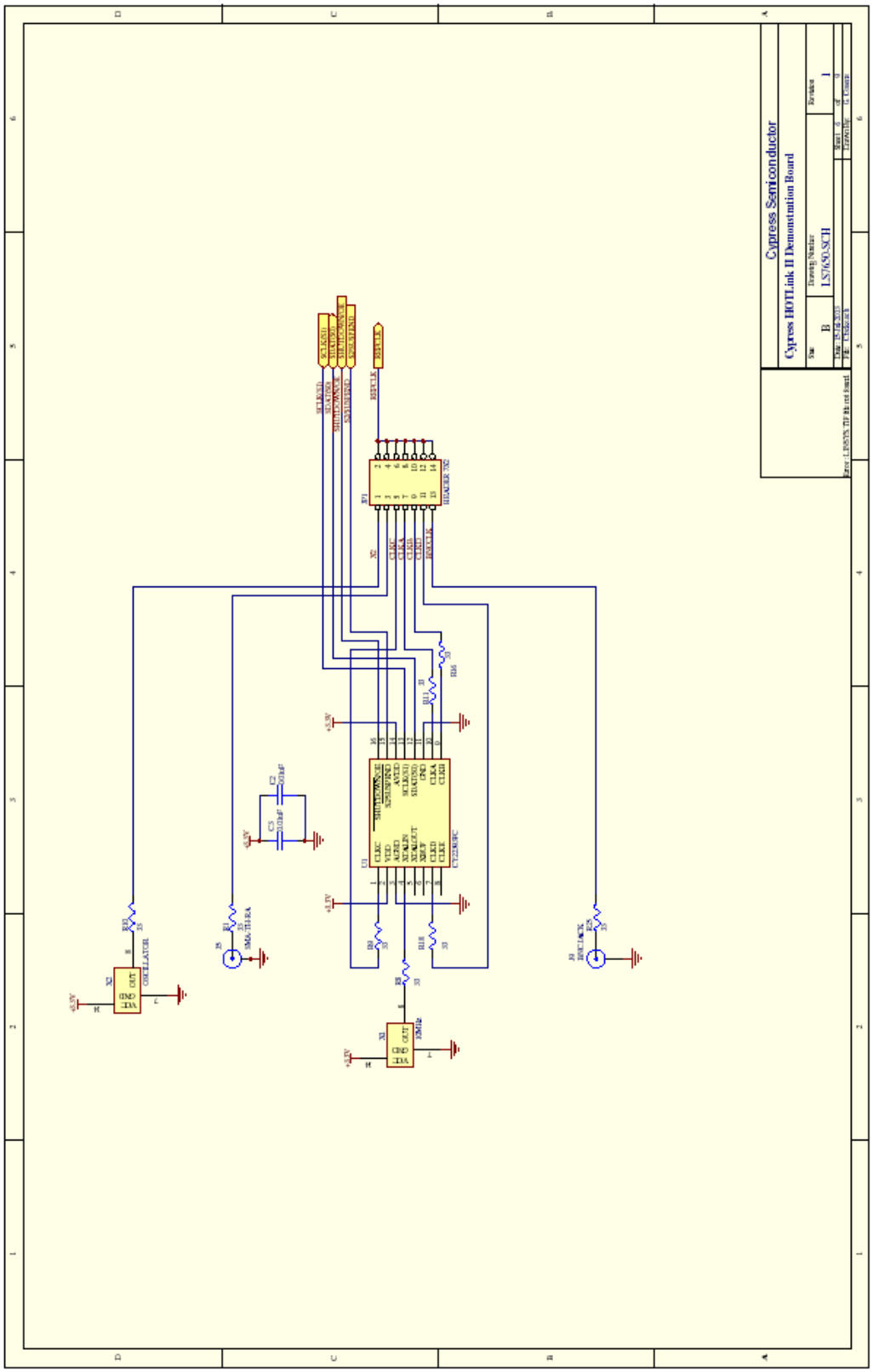


Figure A-6. Clocks Schematics (Clocks.sch)

[+] Feedback

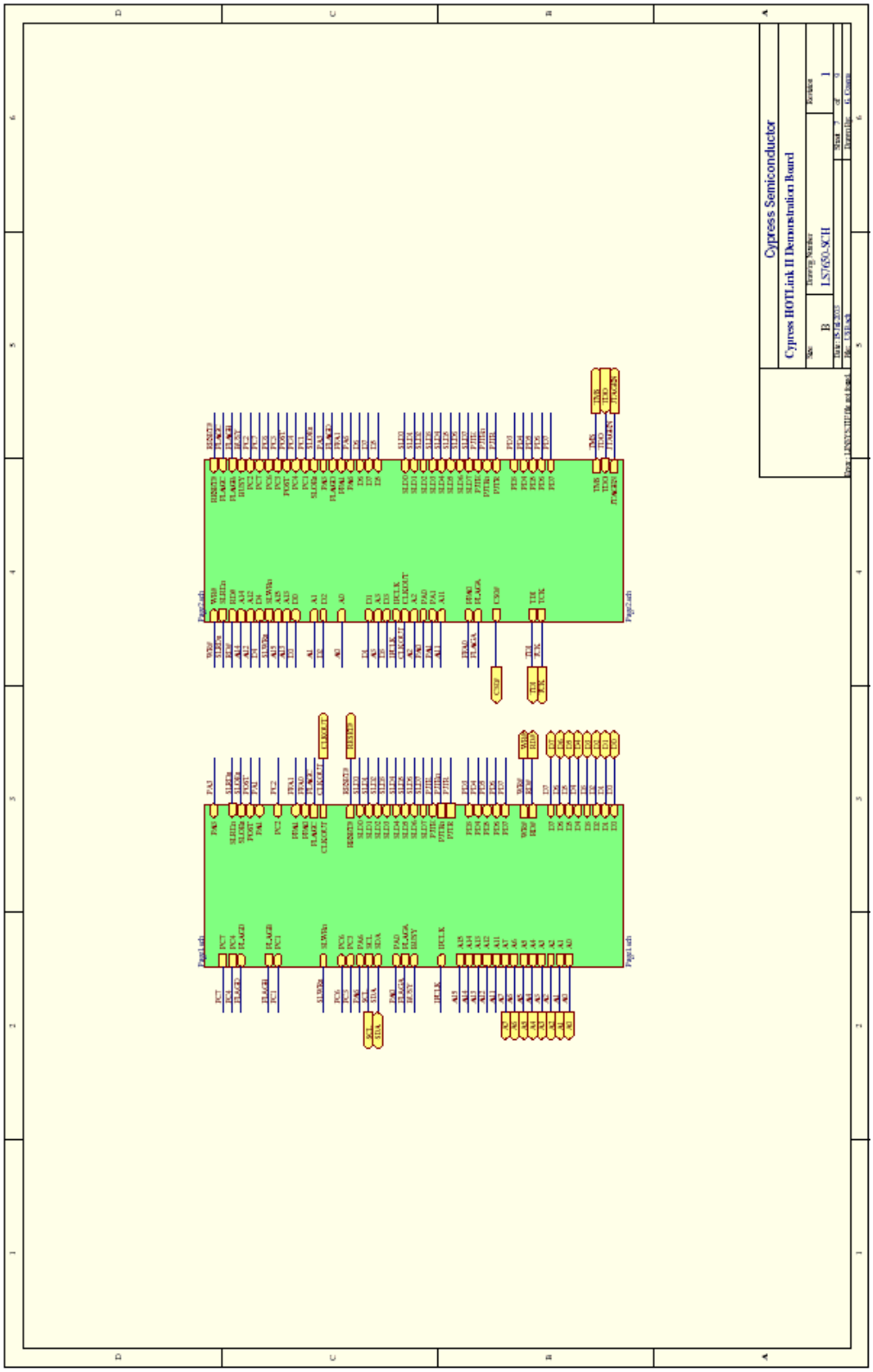


Figure A-7. EZ-USB FX2 USB Microcontroller Schematics (USB.sch)

[+] Feedback

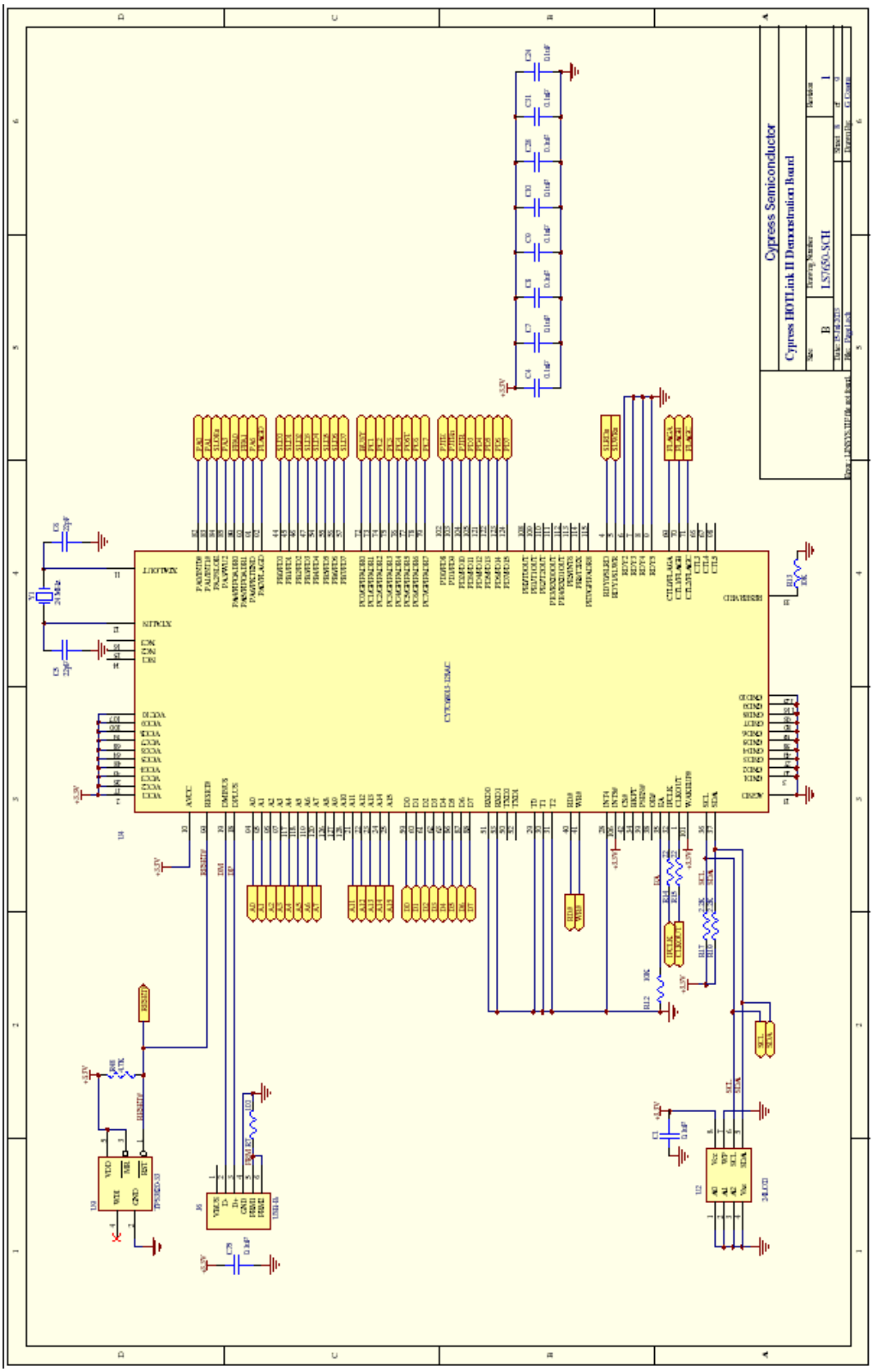


Figure A-8. USB Page 1 Schematics (Page1.sch)

[+] Feedback

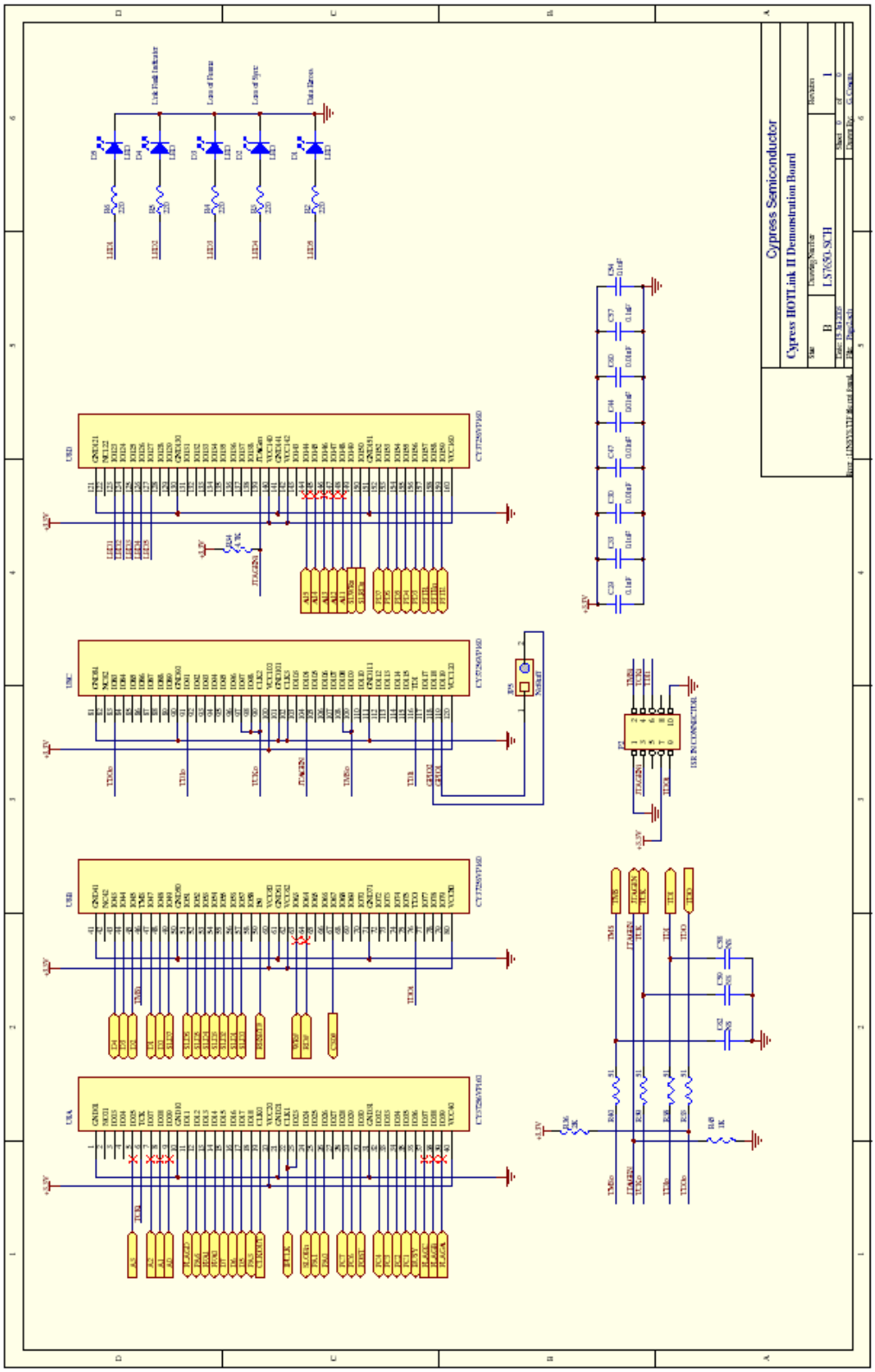


Figure A-9. USB Page 2 Schematics (Page2.sch)

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Appendix B: PCB Layout Diagrams of HOTLink II Video Evaluation Board

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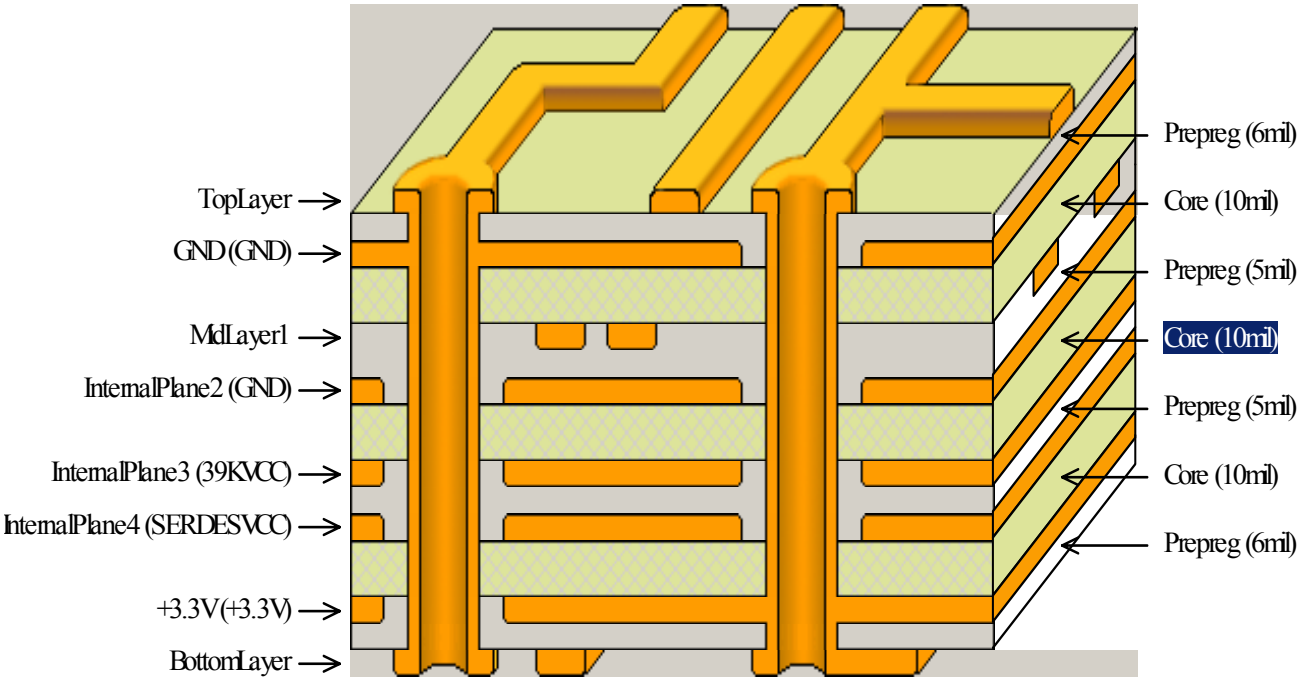


Figure B-1. Board Stackup

[+] Feedback

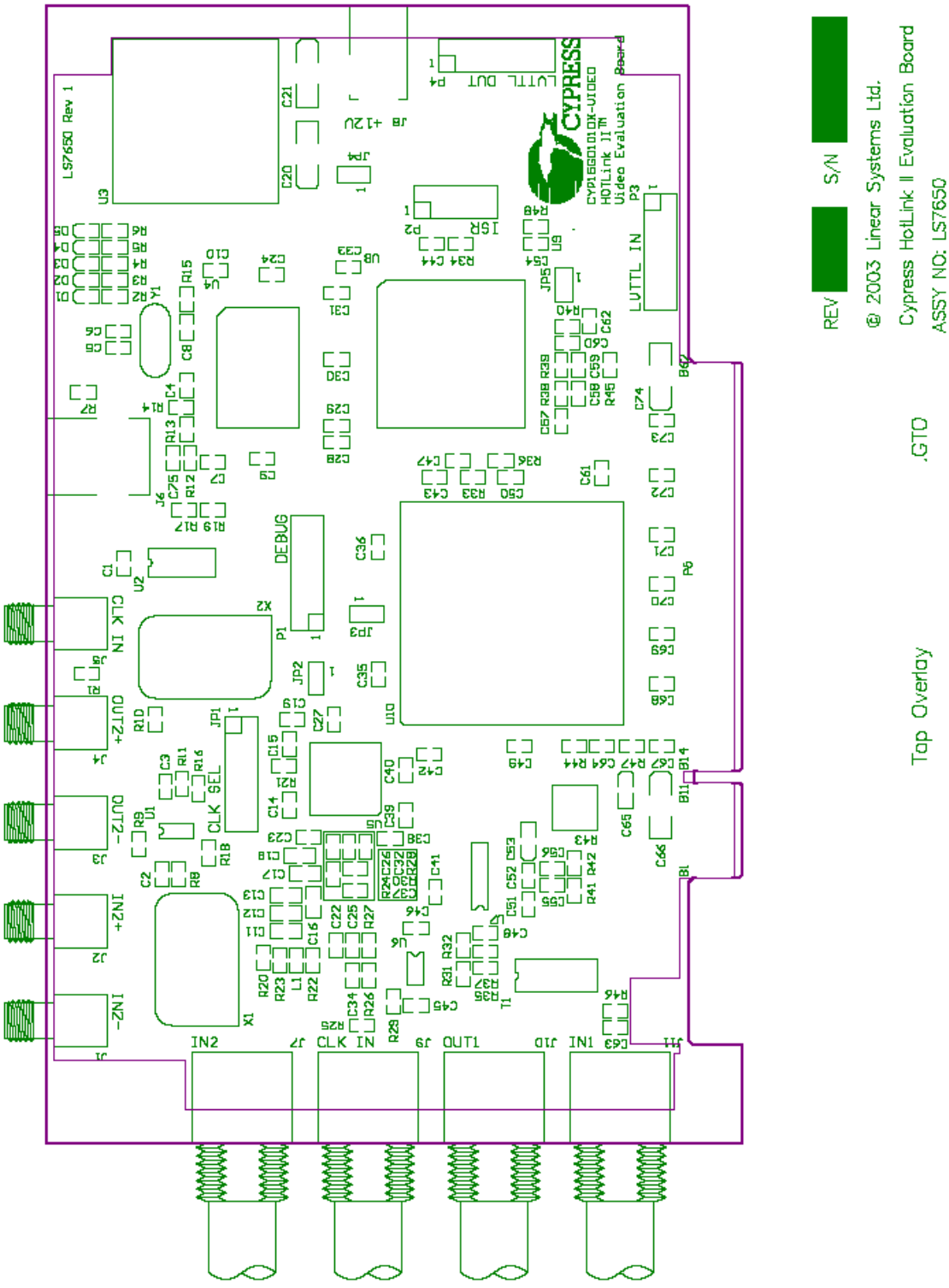


Figure B-2. Top Overlay

[+] Feedback

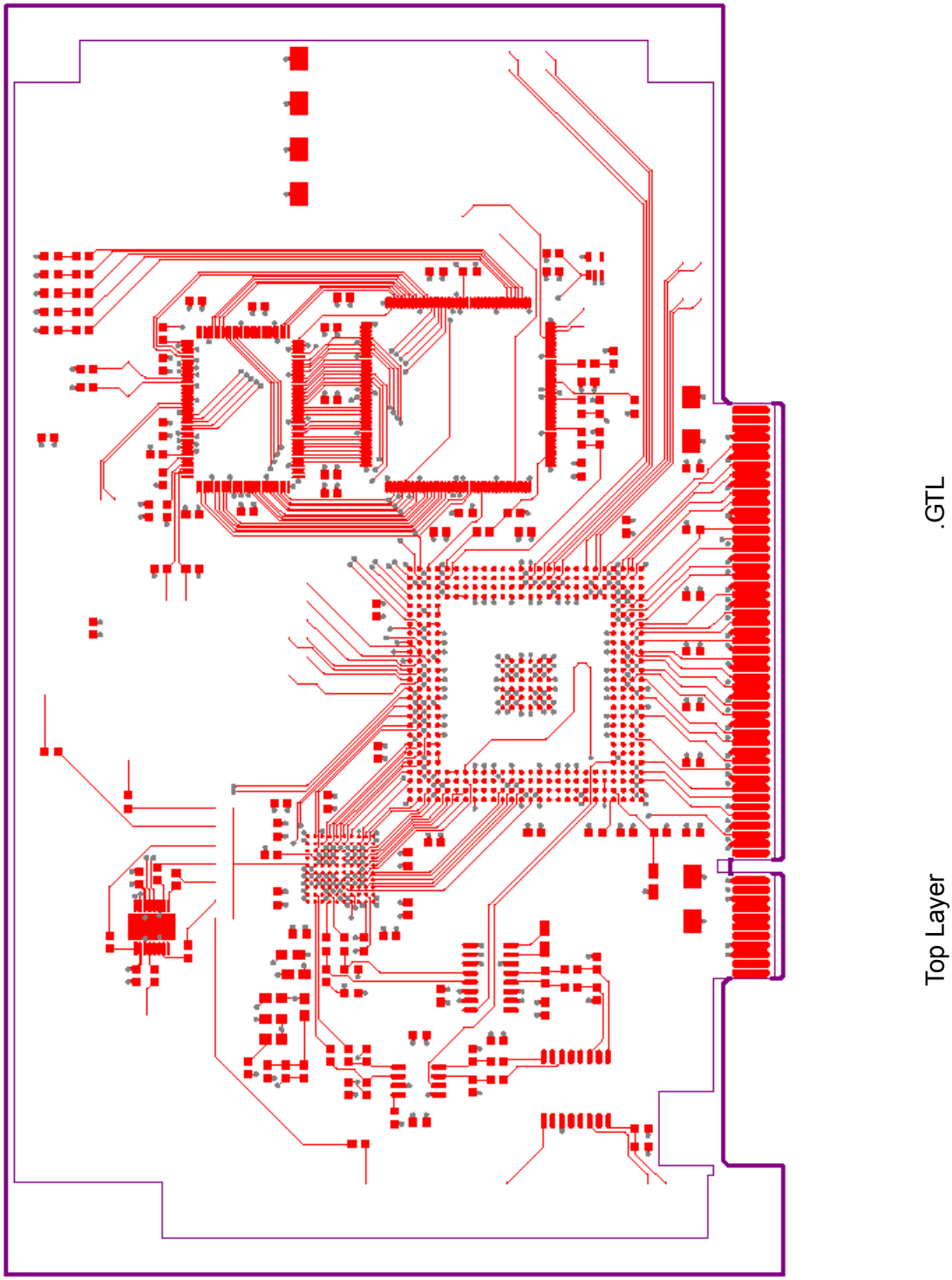


Figure B-3. Top Layer

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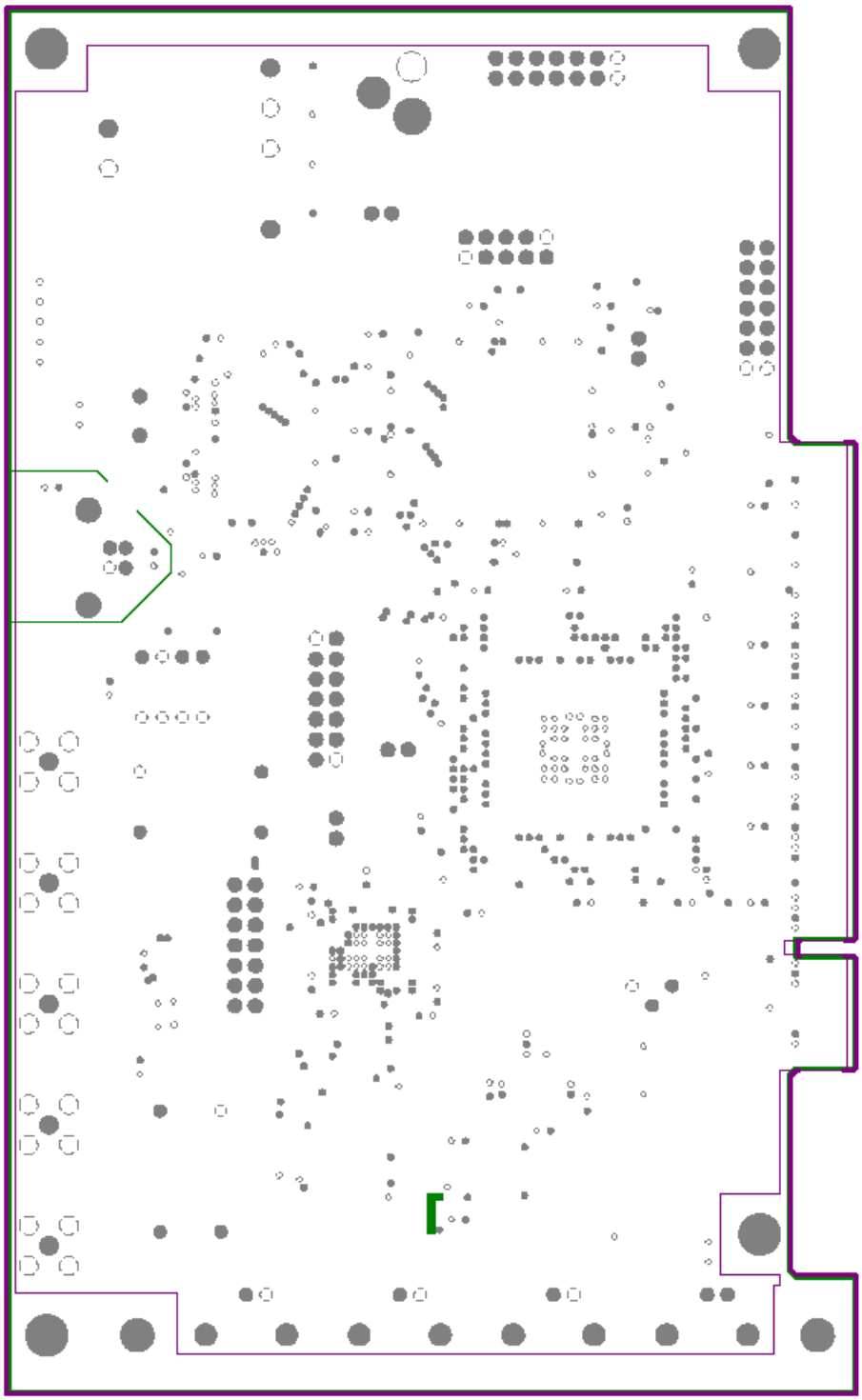


Figure B-4. GND Layer

[+] Feedback

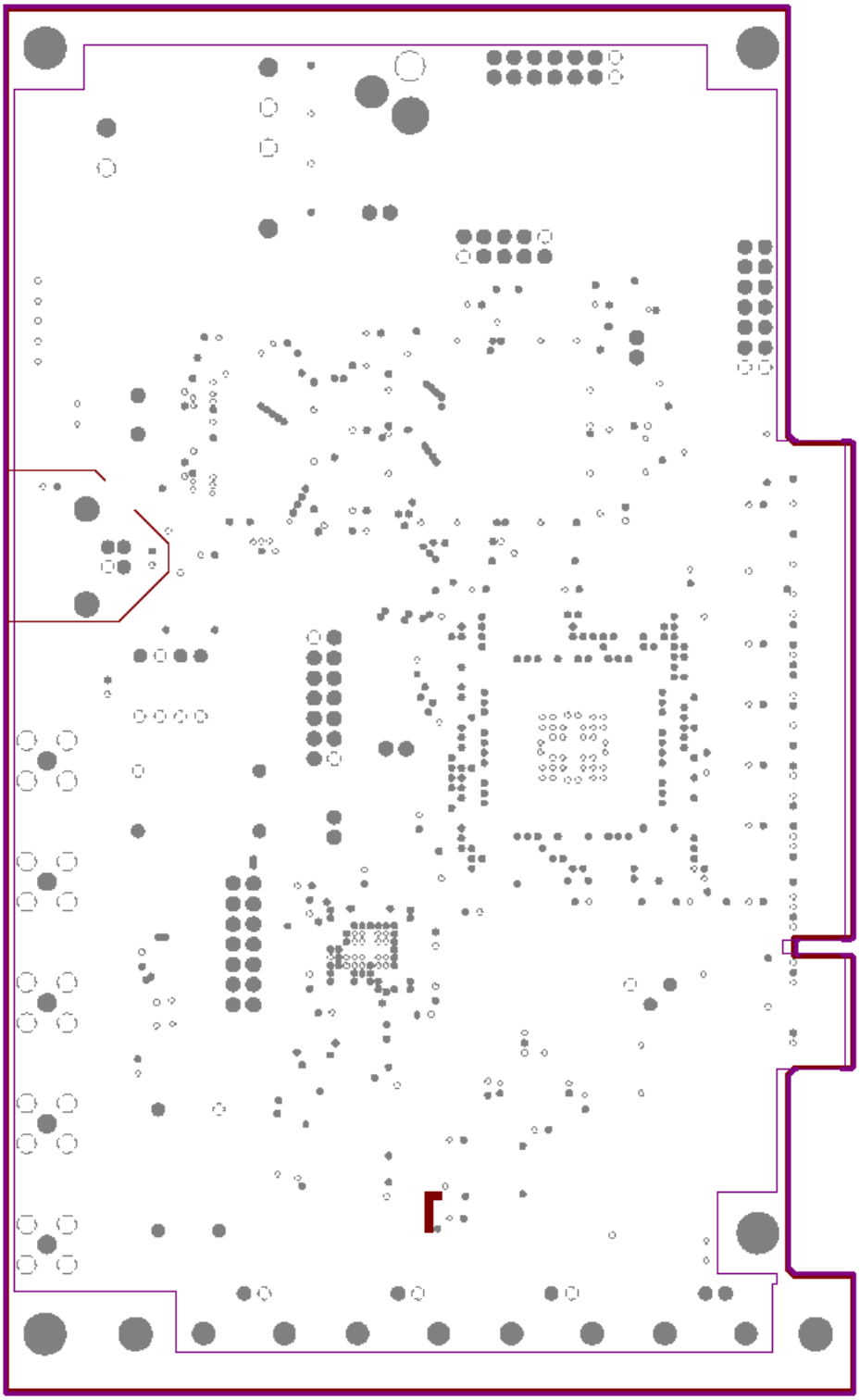


Figure B-5. Internal Plane 2

[+] Feedback

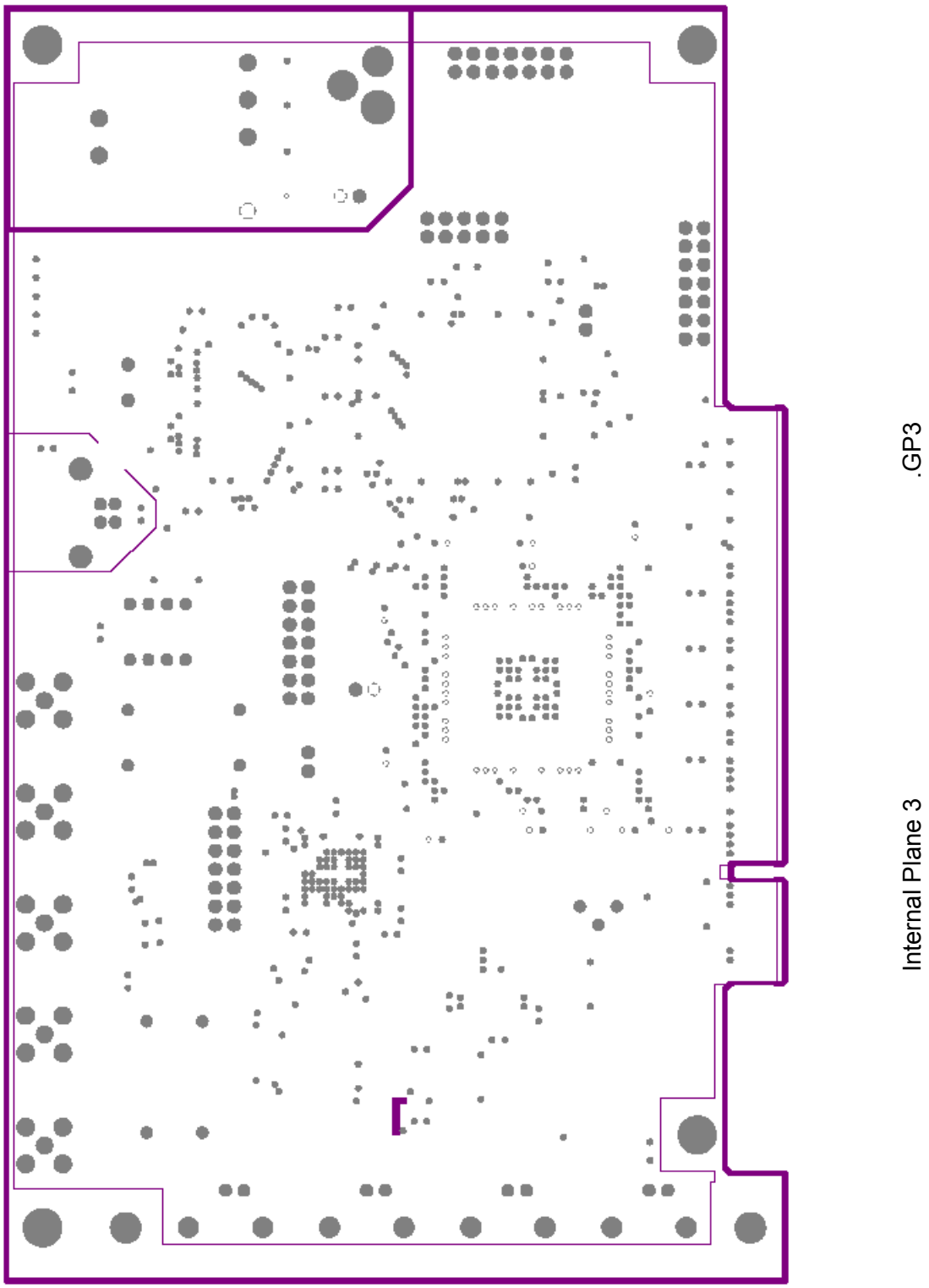


Figure B-6. Internal Plane 3

[+] Feedback

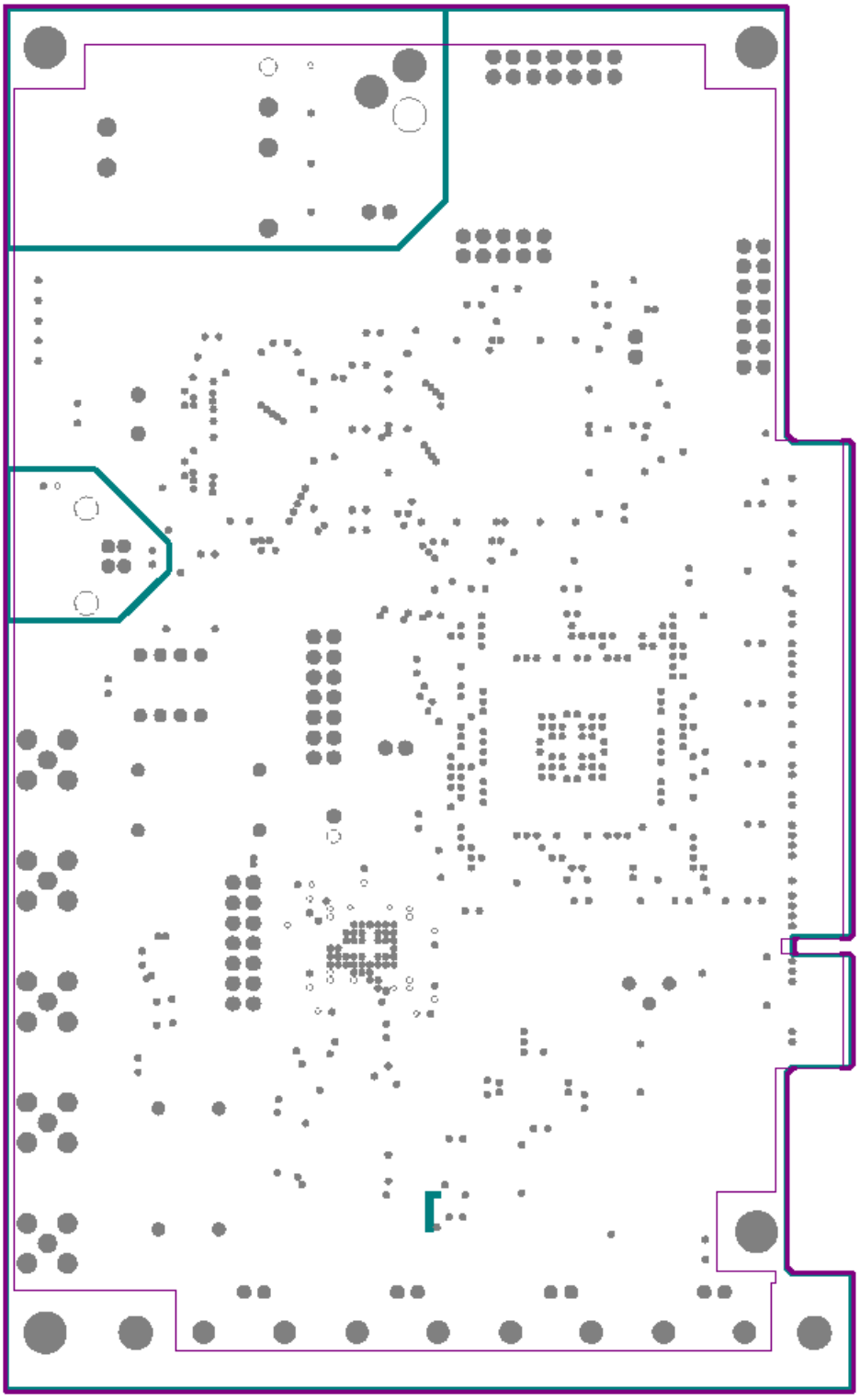


Figure B-7. Internal Plane 4

[+] Feedback

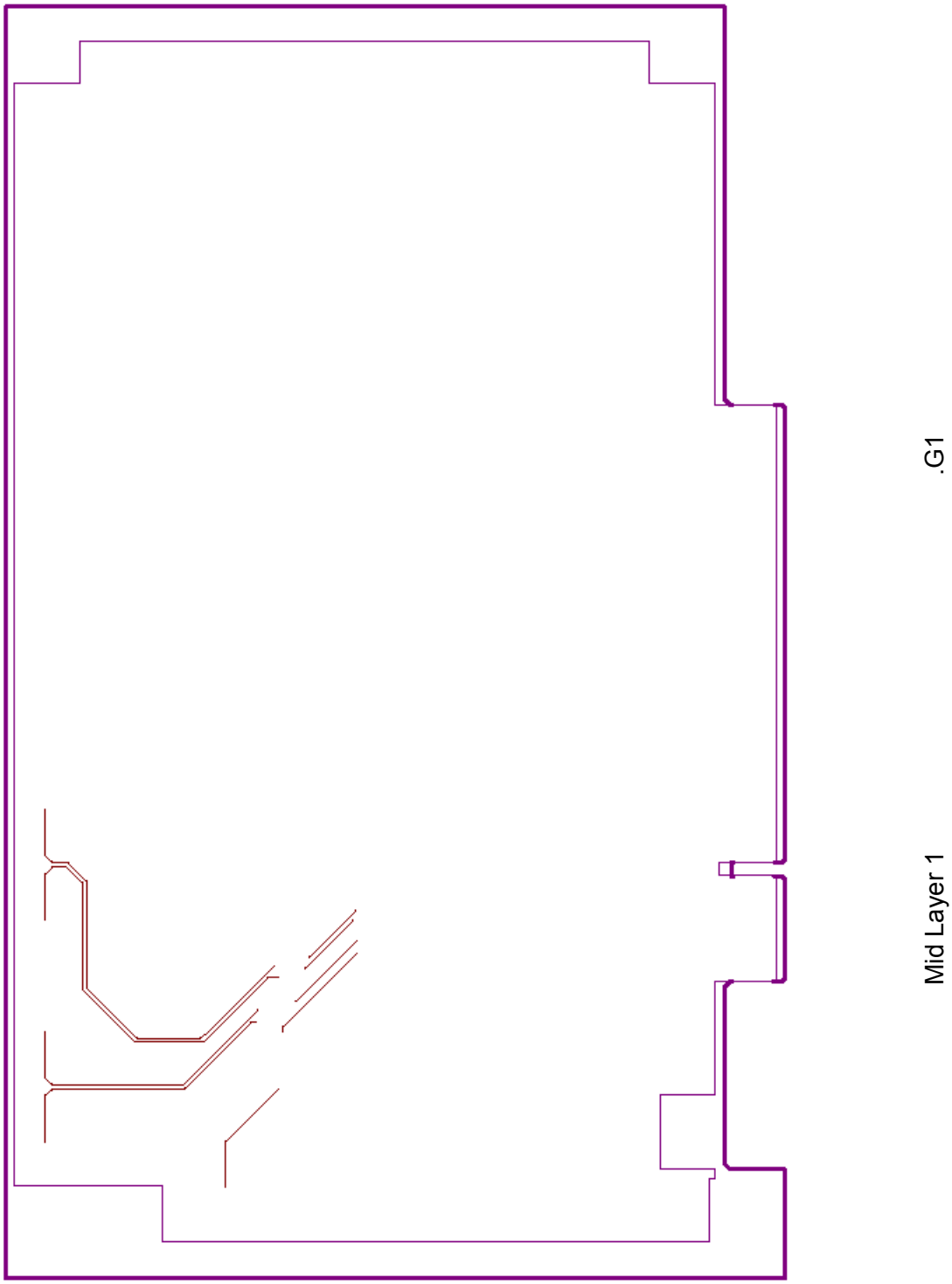


Figure B-8. MidLayer1

[+] Feedback

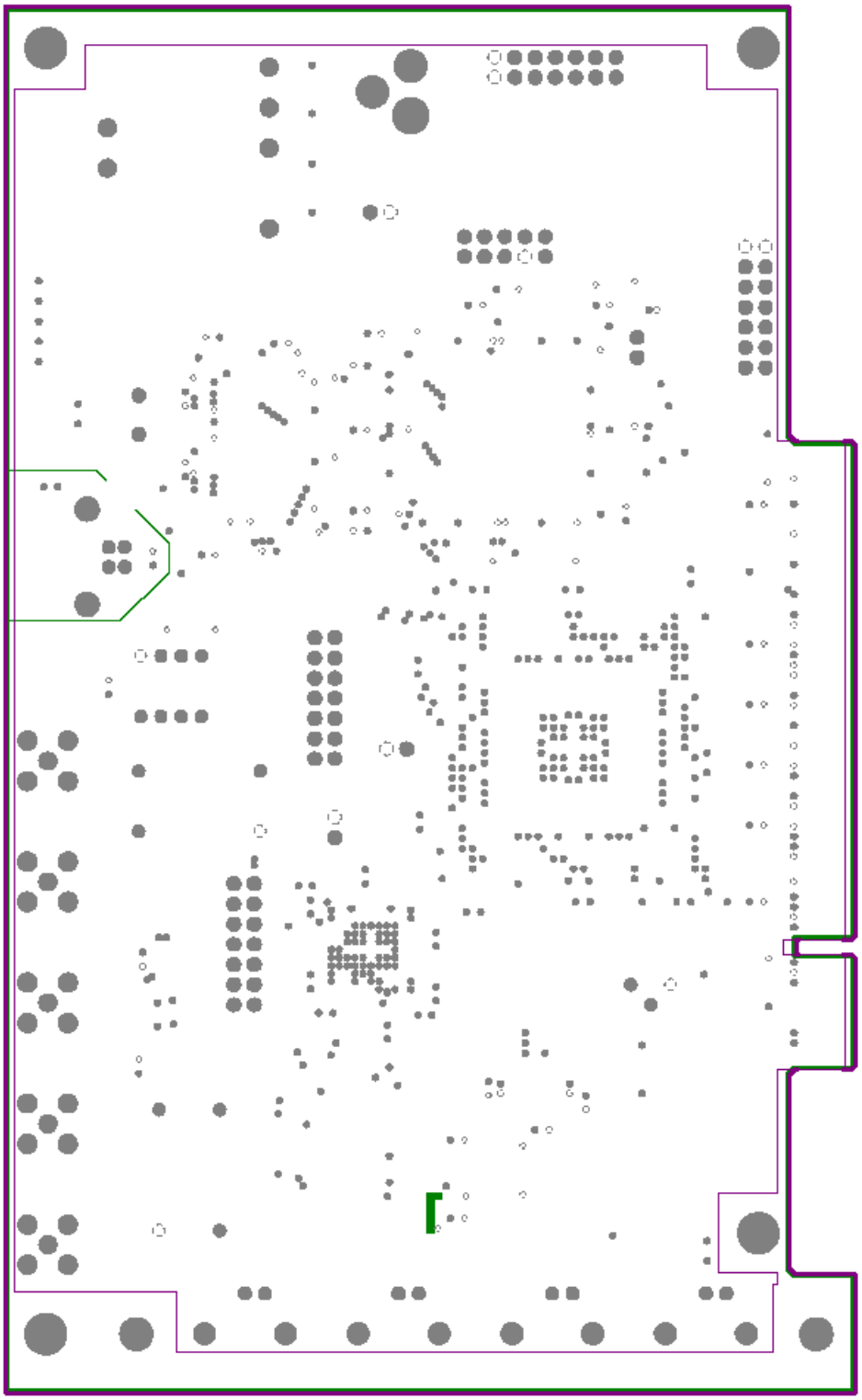


Figure B-9. +3.3V Layer

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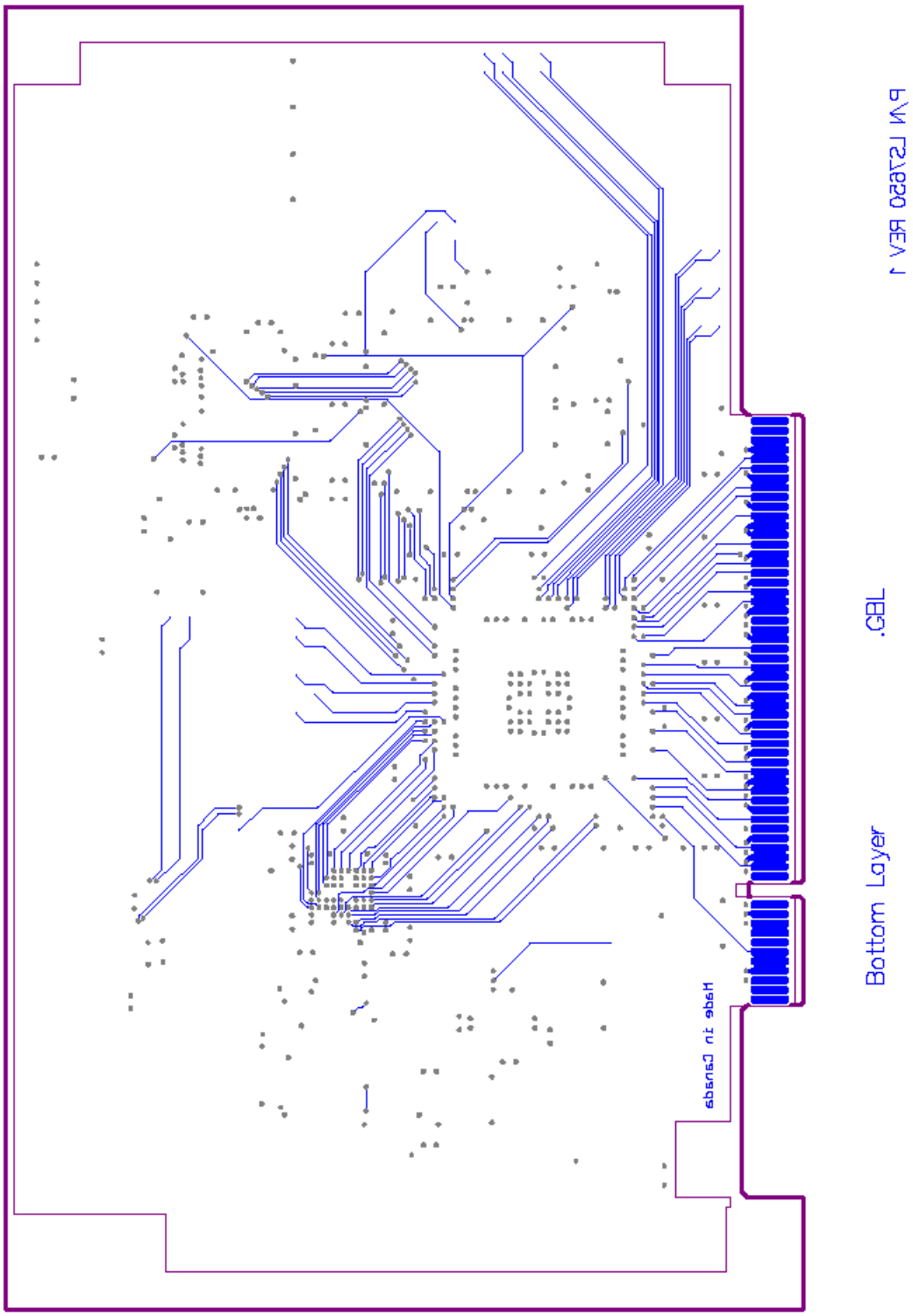


Figure B-10. Bottom Layer

[+] Feedback

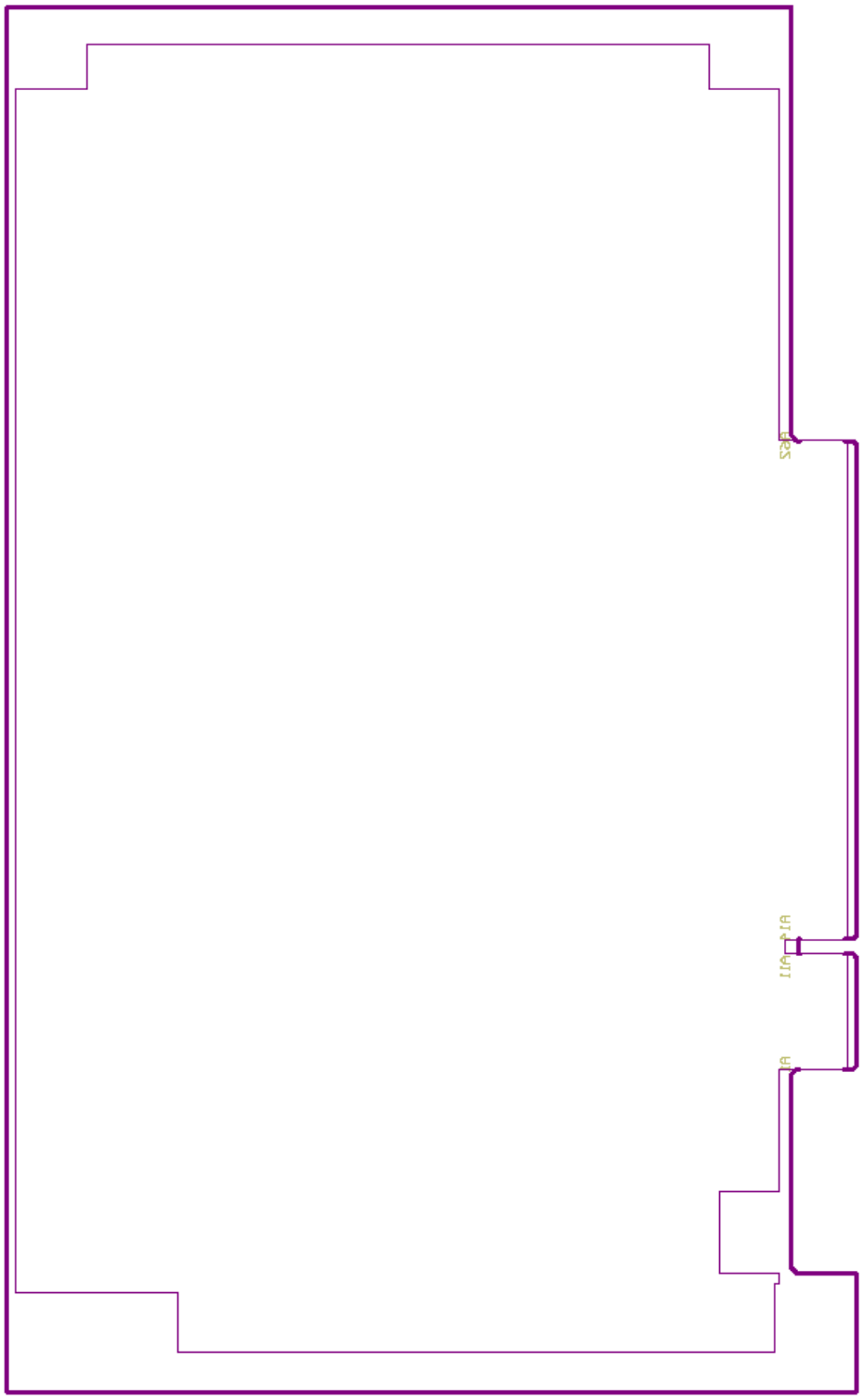


Figure B-11. Bottom Overlay

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Appendix C: Bill of Materials (BOM) of HOTLink II Video Evaluation Board

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Table C-1. Bill of Materials for HOTLink II Video Evaluation Board

Qty	Part No.	Manufacturer	Description	Designator
1	CYV15G0101DXB-BBC	Cypress	Single Channel HOTLink II Transceiver	U5
1	CY39200V388-181MGC	Cypress	Delta39K ISR CPLD	U10
1	CY37256VP160-66AC	Cypress	Ultra37000 CPLD	U8
1	CY22393FC	Cypress	Three-PLL Serial Programmable FLASH Programmable Clock Generator	U1
1	CY7C68013-128AC	Cypress	EZ-USB FX2 USB Microcontroller High-Speed USB Peripheral Controller	U4
1	GS1524-CKD	Gennum	HD-LINX II Multi-Rate SDI Adaptive Cable Equalizer	U7
1	GS1528-CKA	Gennum	HD-LINX II Multi-Rate SDI Dual Slew-Rate Cable Driver	U6
1	24LC00/P	Microchip	128-bit I2C Bus Serial EEPROM	U2, socketed
1	TPS3820-33DBVT	TI	3.3-v Processor Supervisor	U9
1	UNR-3.3/3-D12	Datel	Non-isolated 12-V in 3.3-V @ 3-A out DC/DC Converter	U3
1	P1144-3SV-10.0M	Pletronics	3.3-V 10-MHz 25-ppm crystal oscillator	X1
1	ECS-240-20-4	ECS	24-MHz 20-pF load quartz crystal	Y1
5	SML-LX0603GW-TR	Lumex	Surface Mount LED, Half-Moon Solder Terminals	D1 D2 D3 D4 D5
1	PE-65508	Pulse	Fibre Channel Dual Transformer, 531-Mbaud	T1
2	ERJ-3GEYJ220V	Panasonic	22-ohm 5% 0603	R14 R15
10	ERJ-3GEYJ330V	Panasonic	33-ohm 5% 0603	R1 R8 R9 R10 R11 R16 R18 R25 R35 R37
2	ERJ-3EKF37R4V	Panasonic	37.4-ohm 1% 0603	R41 R42
4	ERJ-3EKF49R9V	Panasonic	49.9-ohm 1% 0603	R24 R26 R27 R30
4	ERJ-3GEYJ510V	Panasonic	51-ohm 5% 0603	R33 R38 R39 R40
2	ERJ-3GEYJ750V	Panasonic	75-ohm 5% 0603	R31 R32
3	ERJ-3GEYJ101V	Panasonic	100-ohm 5% 0603	R7 R28 R46
5	ERJ-3GEYJ221V	Panasonic	220-ohm 5% 0603	R2 R3 R4 R5 R6
1	ERJ-3GEYJ751V	Panasonic	750-ohm 5% 0603	R29
1	ERJ-3GEYJ102V	Panasonic	1k 5% 0603	R45
1	ERJ-3GEYJ202V	Panasonic	2k 5% 0603	R36
2	ERJ-3GEYJ222V	Panasonic	2.2k 5% 0603	R17 R19
5	ERJ-3GEYJ472V	Panasonic	4.7k 5% 0603	R21 R34 R44 R47 R48
2	ERJ-3GEYJ103V	Panasonic	10k 5% 0603	R12 R13
1	3362R-1-102	Bourns	1k 6-mm square single-turn top-adjust sealed Cermet potentiometer	R43
1	ECJ-1VC1H020C	Panasonic	2pF 0.25-pF NPO ceramic 50-V 0603	C52
2	ECJ-1VC1H220J	Panasonic	22pF 5% NPO ceramic 50-V 0603	C5 C6
20	C0603C103K5RAC	Kernet	0.01uF 10% X7R ceramic 50-V 0603	C2 C3 C14 C15 C19 C23 C27 C30 C34 C37 C38 C39 C40 C41 C44 C45 C47 C51 C60 C72

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Table C-1. Bill of Materials for HOTLink II Video Evaluation Board (continued)

Qty	Part No.	Manufacturer	Description	Designator
4	C08BLBB1X5UX	Dielectric Laboratories	Ultra High Q Multi Layer Ceramic Capacitor	C12 C13 C17 C18
37	C0603C104K4RAC	Kernet	0.1uF 10% X7R ceramic 16-V 0603	C1 C4 C7 C8 C9 C10 C22 C24 C25 C26 C28 C29 C31 C32 C33 C35 C36 C42 C43 C46 C48 C49 C50 C54 C55 C56 C57 C61 C63 C64 C67 C68 C69 C70 C71 C73 C75
2	T491A105K016AS	Kernet	1uF 10% tantalum 16-V 3216	C53 C65
4	T491C226K016AS	Kernet	22uF 10% tantalum 16-V 6032	C20 C21 C66 C74
3	414094-2	AMP	Right Angle 75-ohm BNC jack	J9 J10 J11
5	142-0701-301	Johnson Components	Right Angle SMA jack	J1 J2 J3 J4 J5
1	787780-1	AMP	Type B Right Angle Through Hole Universal Serial Bus Receptacle	J6
1	RAPC712	Switchcraft	Right Angle Through Hole Miniature Power Jack	J8
4			7x2 0.1” straight male header, 15u gold plate	JP1 P1 P3 P4
1	10-89-1801	Molex	5x2 0.1” straight male header, 15u gold plate	P2
3			1x2 0.1” straight male header, 15u gold plate	JP2 JP3 JP4
4	90059-0009	Molex	0.1” shunt, 15u gold plate	JP1 JP2 JP3 JP4
1	ICS-8	RP Electronics	8-pin DIP socket	U2
1	1107741	Aries Electronics	4-pin oscillator socket	X2
1	LS7650 Rev 1		Printed Circuit Board	P5
4			6-32 threaded Nylon standoffs	
4			6-32 Nylon screws	
1	SSL20-7612	Artesyn	Universal input 12-V 20-W power supply, 2.5-mm center-positive plug	
1	P012-006	Tripp Lite	NEMA 1-15P to IEC 320 C7 power cable, 6’	
1	AK672	Assmann	USB A Male to USB B Male cable, 2-m	
			DO NOT POPULATE	C11 C16 C58 C59 C62 J7 JP5 L1 R20 R22 R23

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Approved UG004 9/22/03 kkv

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