BGT60LTR11AIP EBG shield

XENSIV™ 60 GHz radar system platform

Board version V3.1

About this document

Scope and purpose

This user guide describes the function, circuitry, and performance of the XENSIV™ BGT60LTR11AIP 60 GHz radar electromagnetic band gap (EBG) shield. The shield provides the supporting circuitry to the onboard BGT60LTR11AIP monolithic microwave integrated circuit (MMIC), Infineon's 60 GHz radar chipset with antenna-in-package (AIP). An EBG structure is added to reduce the impact of neighboring components, resulting in a homogeneous field of view (FoV). This makes BGT60LTR11AIP the appropriate choice for ceiling-mounted applications. In addition to the autonomous mode configuration, the shield offers a digital interface for configuration and transfer of the acquired radar data to a microcontroller board such as Radar Baseboard MCU7.

Intended audience

The intended audiences for this document are design engineers, technicians, and developers of electronic systems, working with Infineon's XENSIV™ 60 GHz radar sensors.

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Product(s) embedded on a PCB with a focus on specific applications and defined use cases that may include software. PCB and auxiliary circuits are optimized for the requirements of the target application.

Note: Boards do not necessarily meet safety, EMI, quality standards (for example UL, CE) requirements.

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Safety precautions

Note: *Please note the following warnings regarding the hazards associated with development systems.*

Table 1 Safety precautions

	Caution: *The reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*

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1 Introduction

1.1 Radar system platform

XENSIV™ BGT60LTR11AIP MMIC is a fully integrated microwave motion sensor. This includes AIP elements, built-in motion and direction of motion detectors, and a state machine allowing fully autonomous operation of the MMIC without any external microcontroller. An integrated frequency divider with a phase-locked loop (PLL) provides voltage-controlled oscillator (VCO) frequency stabilization. These features make the small-sized radar solution a compelling, smart, and cost-effective replacement for conventional passive infrared (PIR) sensors in low-power or battery-powered applications. The MMIC is designed to operate as a Doppler motion sensor in the 60 GHz ISM band.

The MMIC has four quad-state (QS1 to 4) input pins that give the performance parameters flexibility even when it is running in autonomous mode. These pins are used to configure the MMIC, as explained in Section 3.8.

The MMIC supports multiple operation modes, including autonomous mode and Serial Peripheral Interface (SPI) mode.

In autonomous mode, the following settings are possible through the input pins (QS2 to 4):

Table 1

Pin	Description
QS1	Sets the device operation mode. See Table 5.
QS2	Sets the detection threshold (or sensitivity) from among 16 different levels for a configurable detection range between 0.5 m and to 7 m with a typical human target radar cross-section (RCS). See Table 6.
QS3	Sets the hold time in 16 levels, which allows the detection status holding up to 30 minutes. See Table 7.
QS4	Sets the device operating frequency between 61.1 and 61.4 GHz. See Table 8.

In this mode, the integrated detectors deliver digital output signals indicating the motion and direction of motion (approaching or departing) of a target.

In SPI mode provides full flexibility, using an external microcontroller unit (MCU) to write the MMIC configuration by writing into the MMIC registers. These parameters include the detection threshold, hold time, and operating frequency. In this mode, the integrated detectors, if not disabled, will also deliver digital outputs indicating the motion and direction of motion. If further signal processing is required, the radar raw data can be extracted and sampled from the MMIC and then used to develop customized algorithms for maximum performance.

The BGT60LTR11AIP electromagnetic band gap (EBG) shield demonstrates the features of the BGT60LTR11AIP MMIC and gives you a “plug-and-play” radar solution. The shield can also be attached to an Arduino MKR board or an Infineon Radar Baseboard MCU7. A graphical user interface (GUI) is available via Developer Center to display and analyze the acquired data in the time and frequency domains.

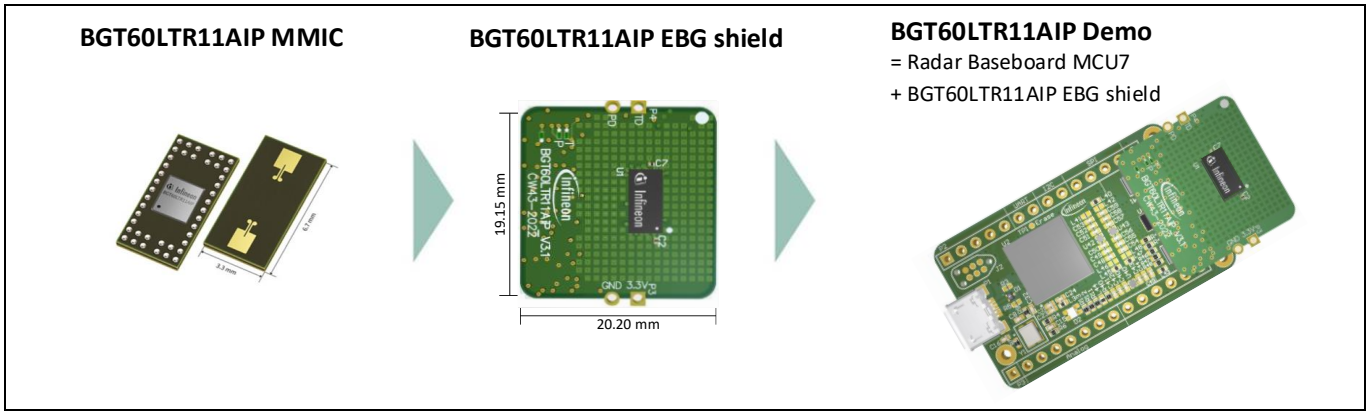


Figure 1 **BGT60LTR11AIP EBG shield using BGT60LTR11AIP MMIC**

1.2 Key features

The BGT60LTR11AIP EBG shield is optimized for fast prototyping design and system integration, as well as initial product feature evaluation. This sensor can be integrated into systems such as laptops, tablets, TVs, and speakers to “wake” them up based on the detection of motion (or direction of motion), put them to sleep or auto-lock when no motion is detected for a defined amount of time. This way, it can be a smart power-saving feature for these devices and might also eliminate the need for keyword-based activation. Radar sensors offer the possibility of being hidden inside the end product because they operate through non-metallic materials. This enables a seamless integration of technology into our day-to-day lives.

Some key features of the BGT60LTR11AIP EBG shield are as follows:

- 20.20 mm x 19.15 mm form factor for the BGT60LTR11AIP EBG shield
- Features an AIP MMIC of small size (6.7 mm x 3.3 mm x 0.56 mm), eliminating antenna design complexity at the user end
- Features an EBG structure, which can improve the isolation between the sensor package and PCB circuitry. This reduces the impact of the PCB layout and size on the radiation pattern and allows a symmetrical field of view (FoV) for on-ceiling applications.
- Detects motion and direction of movement (approaching or departing) for a human target
- Works standalone (autonomous mode) or with SPI mode to interface with an external microcontroller
- Configurable settings such as operation mode, detector threshold, detector hold time, operating frequency
- Low power consumption
- Option to solder onto other PCBs such as Arduino MKR for extra flexibility

2 System specifications

Table 2 BGT60LTR11AIP EBG shield specifications

Parameter	Unit	Min.	Typ.	Max.	Comments
System performance					
Detection range	m	–	5	7	Typical motion detection range for human target at low threshold (in both E-plane and H-plane orientations)
Power supply					
Supply voltage	V	1.5	3.3	5.0	–
Current consumption	mA	–	3.48	–	At 3.3 V supplied via castellated holes Pulse repetition time (PRT) = 500 µs Pulse width (PW) = 5 µs (LEDs off)
Antenna characteristics (measured)					
Antenna type	–	1 x 1			AIP
Horizontal – 3 dB beamwidth (HPBW)	Degrees	–	80	–	At frequency = 61.25 GHz
Elevation – 3 dB beamwidth (HPBW)	Degrees	–	80	–	At frequency = 61.25 GHz

3 Hardware description

3.1 Overview

The BGT60LTR11AIP EBG shield is a very small PCB of 20.2 mm x 19.15 mm size, with a XENSIV™ BGT60LTR11AIP 60 GHz radar sensor mounted on top of the PCB. The PCB can be manufactured using a standard FR4 laminate, as the antennas are integrated into the chip package. The bottom side of the shield has the connectors to the Radar Baseboard MCU7 [1] (P1 and P2 in Figure 2) and other components such as the LDO, quartz oscillator, and level shifter. Figure 3 shows the marker on the top of the shield that must be aligned with the marker on the Radar Baseboard MCU7 for correct alignment. The castellated holes on the edges of the PCB provide additional access to the detector outputs and power supply signals of the shield.

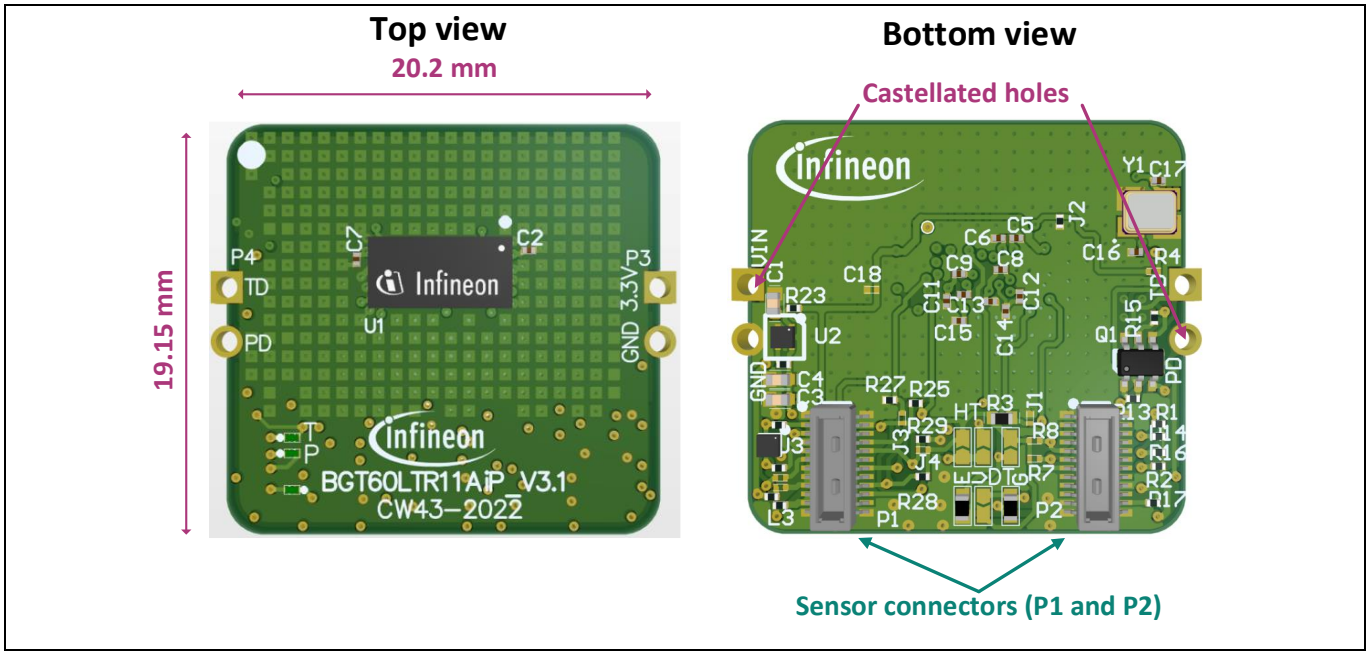


Figure 2 **Top and bottom views of the BGT60LTR11AIP EBG shield**

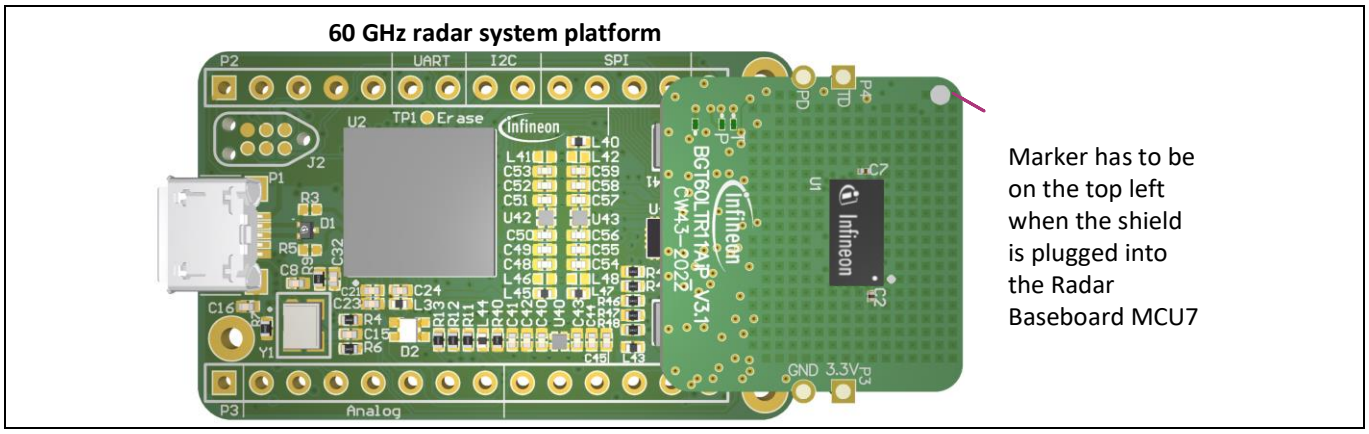


Figure 3 **Markers on Radar Baseboard MCU7 and BGT60LTR11AIP EBG shield for alignment**

Note: *There is a risk of the connectors wearing out when regularly plugged into and unplugged from the shield. To prevent this, do not lift the shield on the short side out of the connector. Instead, simply pull on the long side of the sensor, thereby tilting the short side. This will significantly increase the lifetime of the connectors.*

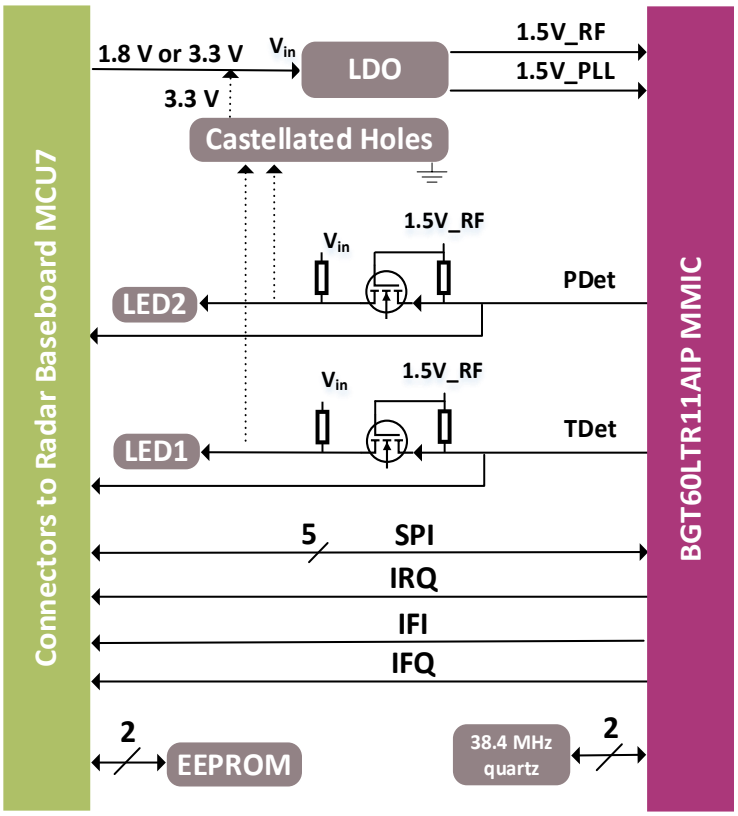


Figure 4 **BGT60LTR11AIP EBG shield block diagram**

The block diagram in Figure 4 shows the configuration of the shield. When the shield is plugged into the Radar Baseboard MCU7, the MMIC's supplies are initially deactivated; only the EEPROM is powered. The MCU reads the content of the EEPROM's memory to determine which shield is plugged into the connectors. The MMIC's supplies are activated only when the shield has been correctly identified.

Communication with the MMIC is mainly performed via SPI. The MCU can use the BGT_RTSN pin to perform a HW reset of the MMIC. The BGT_SELECT and BGT_RTSN lines of the SPI should be pulled up with 10 kΩ resistors. The interrupt request (IRQ) line can be used to trigger the MCU when new data need to be fetched.

3.2 BGT60LTR11AIP MMIC

The BGT60LTR11AIP MMIC (Figure 5) serves as the main element on the BGT60LTR11AIP EBG shield. The MMIC has one each transmit and receives antennas integrated into a 6.7 mm (±0.1 mm) x 3.3 mm (±0.1 mm) x 0.56 mm (±0.05 mm) package. See Figure 6 and Figure 7.

The MMIC has an integrated VCO and PLL for high-frequency signal generation. The transmit section consists of a medium-power amplifier (MPA) with configurable output power, which can be controlled via the SPI.

The chip features a low-noise quadrature receiver stage. The receiver uses a low-noise amplifier (LNA) in front of a quadrature homodyne down-conversion mixer to provide excellent receiver sensitivity. An RC polyphase filter (PPF) derived from the internal VCO signal generates quadrature LO signals for the quadrature mixer.

The analog baseband (ABB) unit consists of the following:

- An integrated sample-and-hold (S/H) circuit for low-power duty-cycled operation
- An externally configurable high-pass filter (HPF)
- A variable-gain amplifier (VGA) stage

- A low-pass filter (LPF)

The integrated target detector circuits in the MMIC indicate the detection of movement in front of the radar and the direction of movement with two digital signals (BGT_TARGET_DET and BGT_PHASE_DET). See Section 3.9 for more details. The detector circuit offers a user-configurable hold time for maximum flexibility.

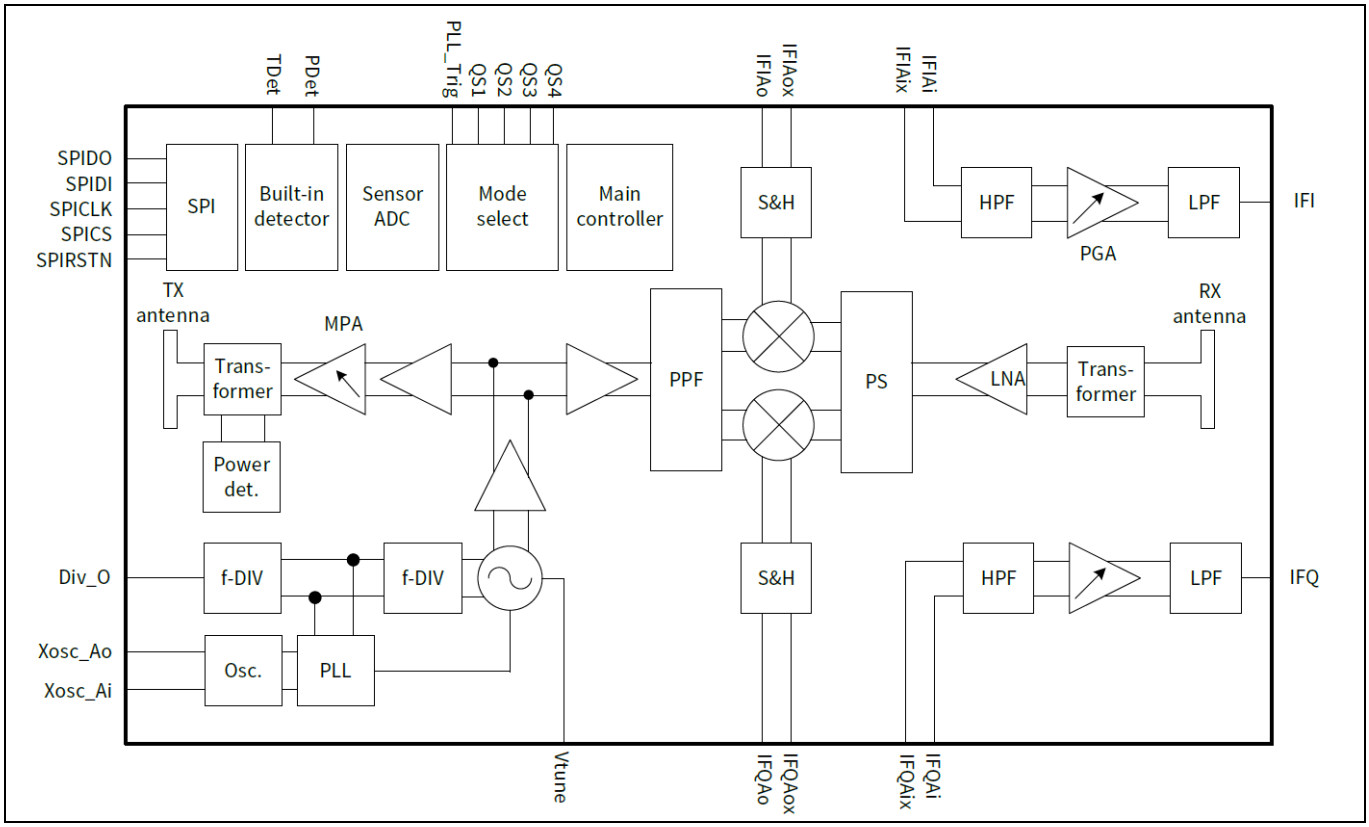


Figure 5 **BGT60LTR11AIP MMIC block diagram**

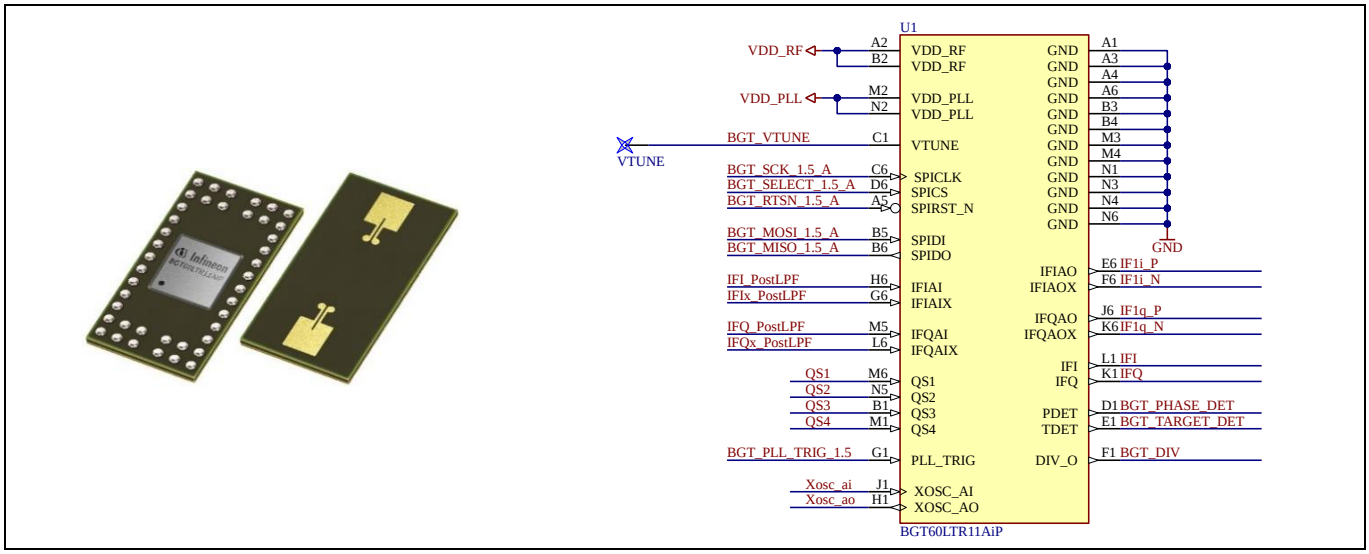


Figure 6 **Package and pin-signal assignment of the BGT60LTR11AIP MMIC**

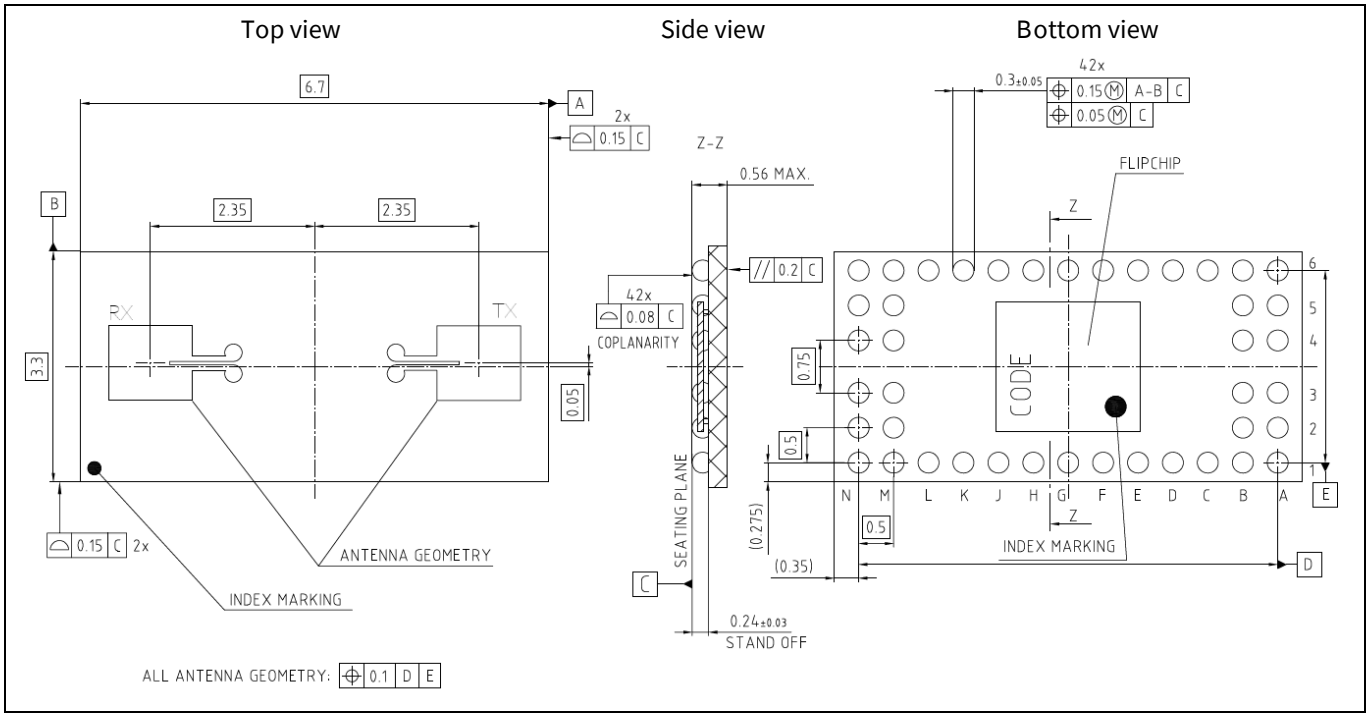


Figure 7 **Top, side, and bottom views of the BGT60LTR11AIP MMIC package – all dimensions in mm**

3.3 Sensor power supply

Because radar sensors are very sensitive to supply voltage fluctuations or crosstalk between different supply domains, a low-noise power supply and properly decoupled supply rails are critical. Radar Baseboard MCU7 provides a low-noise power supply. Figure 8 shows the schematics of the LPFs employed to decouple the supplies of the different power rails in the BGT60LTR11AIP EBG shield. Ferrite beads L1, L3, and L5 provide high attenuation of voltage fluctuations in the MHz regime.

For example, SPI that runs up to 50 MHz can induce voltage fluctuations on the digital domain. These fluctuations would then couple into and interfere with the analog domain without the decoupling filters. The ferrite beads are chosen such that they can handle the maximum current of the sensor with a low DC resistance (below 0.25 Ω) and an inductance as high as possible. The high inductance reduces the cut-off frequency of the LPF, which provides better decoupling for lower frequencies.

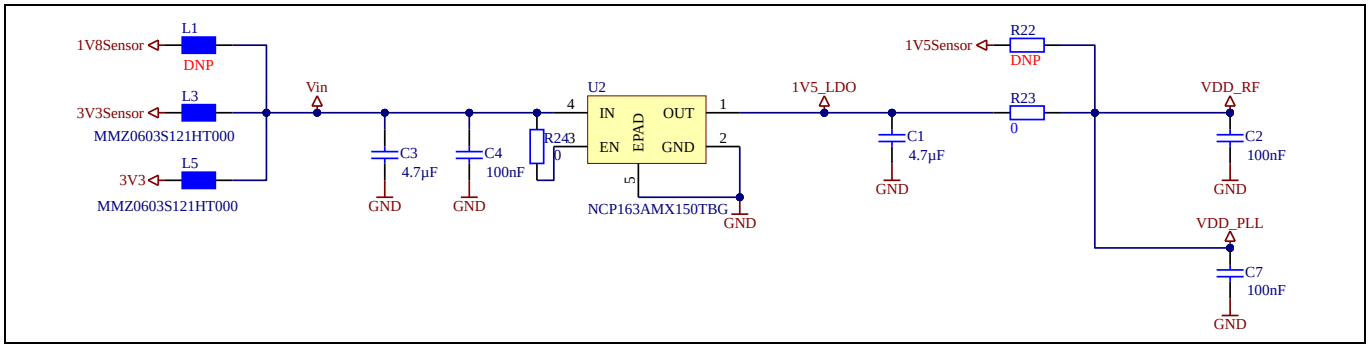


Figure 8 **Schematics of the sensor supply and LPFs**

3.4 Crystal

The MMIC requires an oscillator source with a stable reference clock providing low phase jitter and low phase noise; the oscillator is integrated inside the MMIC. This reduces the current consumption because crystal oscillators consume only a few milliamperes (mA) and run continuously. The BGT60LTR11AIP EBG shield uses a 38.4 MHz crystal oscillator as shown in Figure 9.

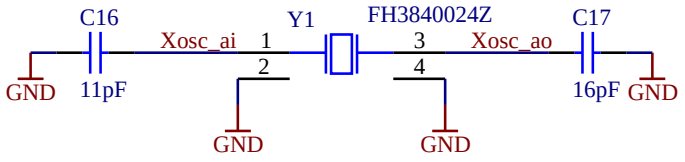


Figure 9 **The crystal circuit on the BGT60LTR11AIP EBG shield**

3.5 External capacitors

The BGT60LTR11AIP MMIC is duty-cycled and performs a S/H operation for lower power consumption. The S/H switches are integrated into the chip at each differential I/Q mixer output port. They are controlled synchronously via the internal state machine.

The capacitors between the S/H circuit and the HPF are external (Figure 10). C10, C11, C14, and C15 are 5.6 nF capacitors used as "hold" capacitors for the S/H circuitry. They can be configured for different PW settings, as shown in Table 3. C8, C9, C12, and C13 are the DC blocking (or high-pass) capacitors. They should have a value of 10 nF to get a high pass of 4 Hz (if internal high-pass resistor R_{HP} = 4 MΩ). It is not recommended to use higher values because this affects the ABB settling time. The DC blocking capacitors are important because the mixer output has a different DC voltage from that of the internal ABB. Figure 10 shows the external hold (C_{hold}) and high-pass capacitors (C_{HP}) for all four branches in the differential I/Q configuration.

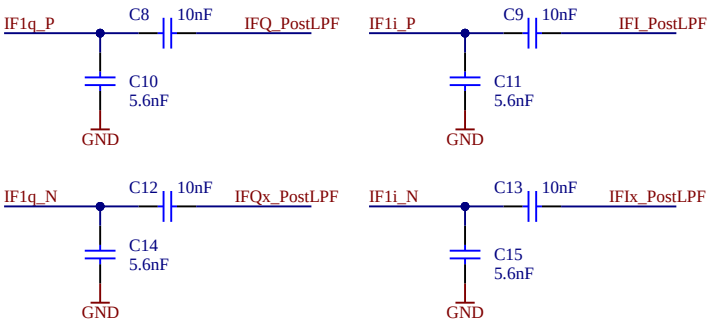


Figure 10 **External capacitors**

Table 3 **Recommended hold capacitors (C10, C11, C14, and C15) for different pulse width (PW) values**

PW (µs)	Hold capacitor value (nF)
3	4.7
4	5.6
5 (default)	5.6 (default)
10	15

The charging time of the hold capacitor (C_{hold}) is limited to the selected PW. Shorter PWs require smaller C_{hold} to become ~90% percent charged during one pulse. The rise time is controlled by the C_{hold} itself and the internal mixer output resistance (R_{mixer_out}) of 300 Ω in each branch.

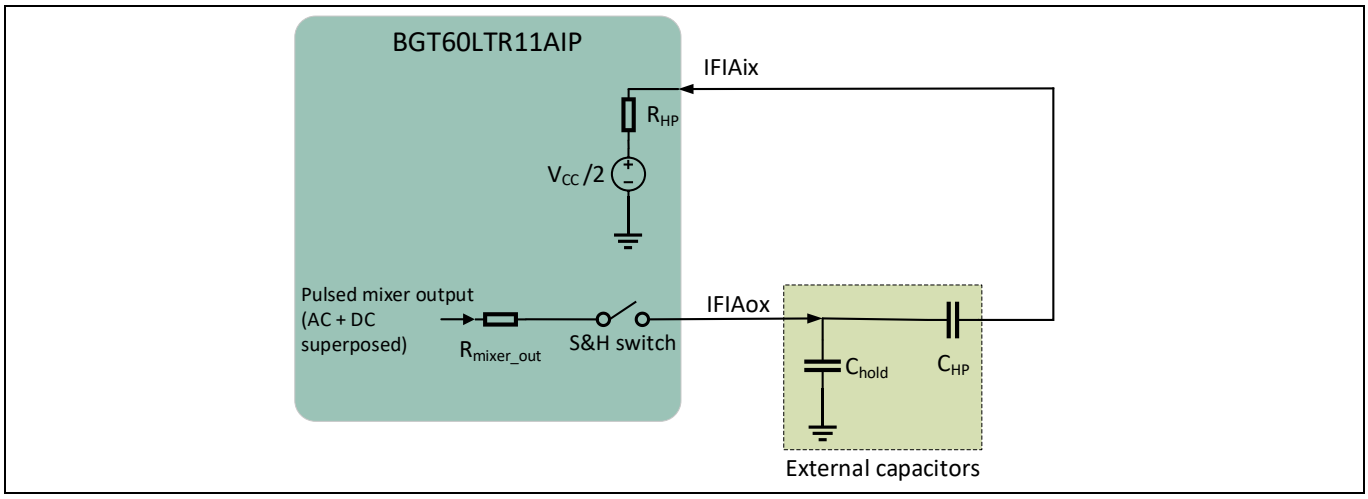


Figure 11 External capacitors for BGT60LTR11AIP

A longer PW can have a higher C_{hold} value, leading to a reduced BW of the RC filter (R_{mixer_out} & C_{hold}). Consequently, there will be a lower baseband noise because of the reduced noise folding BW.

For this RC structure, the low-pass 3 dB cut-off frequency ($f_{LP_{3dB}}$) can be calculated under the following conditions:

t_{rise} = 10% / 90% = S/H on-time = 4 µs

PW = 5 µs

R_{mixer_out} = 300 Ω

$$f_{LP_{3dB}} = \frac{0.35}{t_{rise}} = \frac{0.35}{4\mu s} = 87.5\ \text{kHz}$$

Or based on the formula:

$$f_{LP_{3dB}} = \frac{1}{2\pi \times R_{mixer_out} \times C_{hold}}$$

$$C_{hold} = 6.1\ \text{nF}$$

$$\rightarrow 5.6\ \text{nF (closest E12 series value)}$$

The high-pass 3 dB cut-off frequency ($f_{HP_{3dB}}$) can be calculated under the following conditions:

C_{HP} = 10 nF

R_{HP} = 4 MΩ

$$f_{HP_{3dB}} = \frac{1}{2\pi \times R_{HP} \times C_{HP}} = \frac{1}{2\pi \times 4\text{M}\Omega \times 10\text{nF}} = 4\ \text{Hz}$$

3.6 Connectors

The BGT60LTR11AIP EBG shield can be connected to an MCU board like Radar Baseboard MCU7 with the P1 and P2 connectors. Castellated holes (P3 and P4) are visible on the top and bottom sides of the PCB. TD and PD pins of the castellated holes correspond to the internal detector outputs of the MMIC.

The shield contains two Hirose DF40C-20DP-0.4 V connectors (P1 and P2). The corresponding DF40C-20DS-0.4 V connectors are on Radar Baseboard MCU7. Figure 12 shows the pinout of the Hirose connectors of the BGT60LTR11AIP EBG shield.

The IRQ signal is connected with a 0 Ω resistor (R5) to the divider output (BGT_DIV) of the MMIC. In SPI pulsed mode, BGT_DIV generates a signal that acts as an interrupt signal for the MCU to start ADC acquisition. BGT_DIV could also be used to measure the divider frequency.

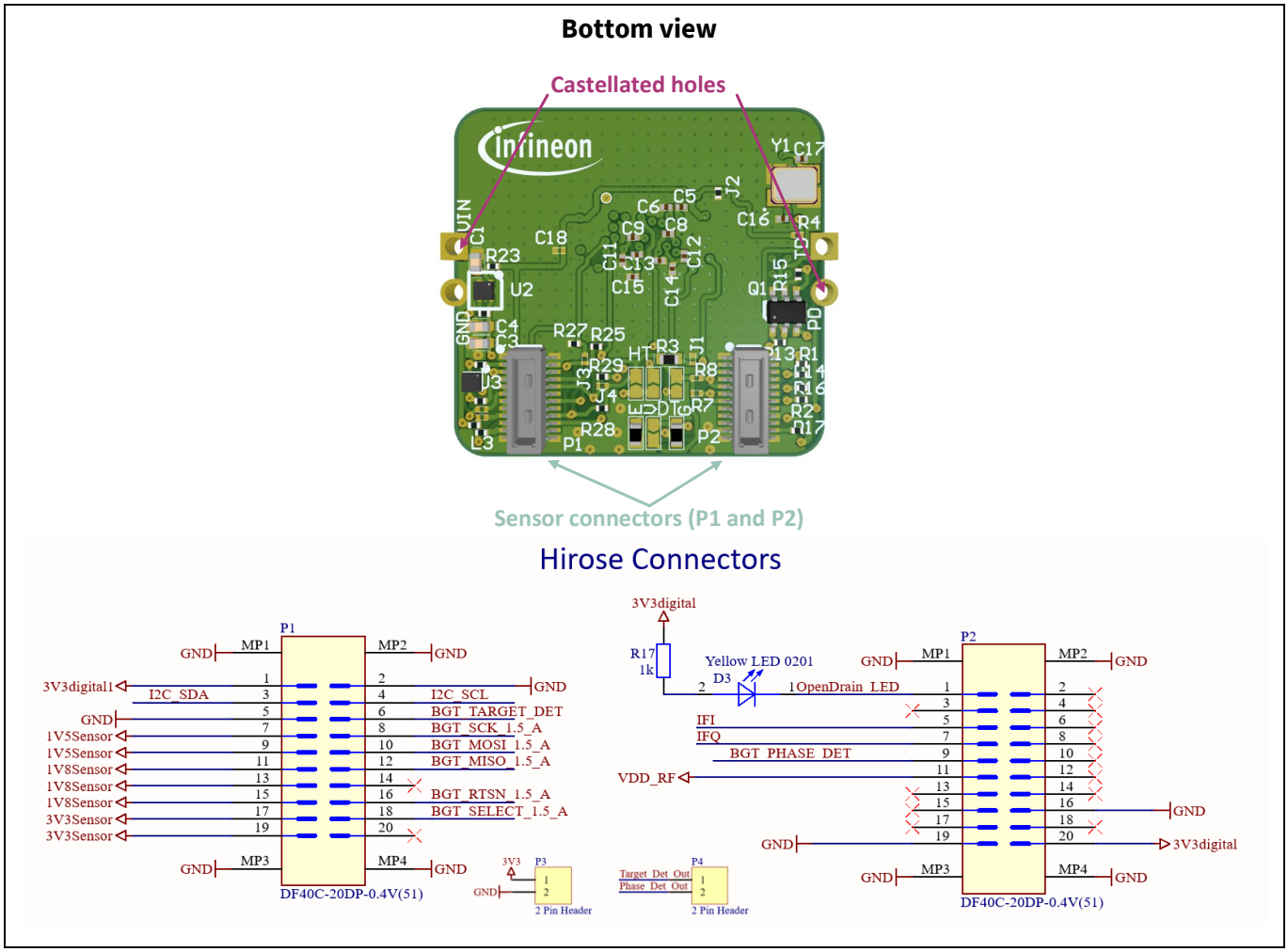


Figure 12 Connectors on the BGT60LTR11AIP EBG shield, and their pinouts

3.7 EEPROM

The BGT60LTR11AIP EBG shield contains an EEPROM (24CW1280T-I/CS0668) connected via an I²C interface to store data such as the board identifier; see Figure 13 for the connection details. This EEPROM contains a descriptor indicating the type of shield board and MMIC. This is used by the firmware (FW) to communicate properly with the shield.

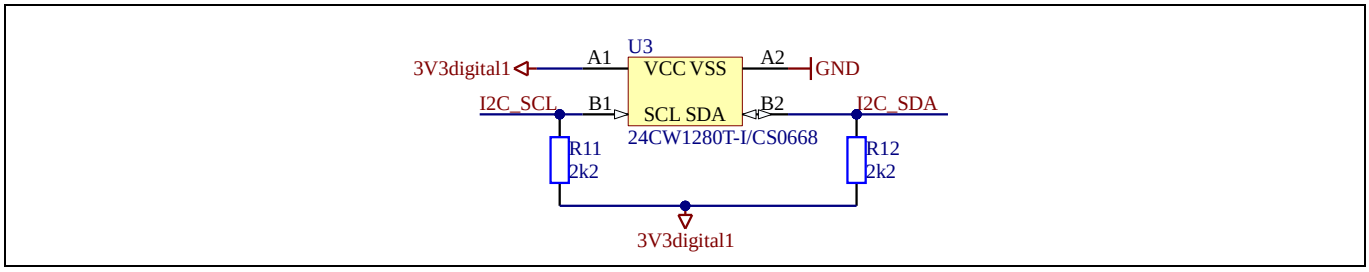


Figure 13 Schematics of the EEPROM

3.8 LEDs and level shifters

The shield has two LEDs to indicate the motion detection (green) and the target's direction of motion (red); see Figure 14. Note that R1 and R2 are limiting resistors. The digital block within the detector in the MMIC evaluates and sets the target detect/phase detect outputs of the BGT60LTR11AIP MMIC. The Target Detect (**TD**et) output is active LOW. The Phase Detect (**PD**et) output is used to indicate the direction of the detected target. It is set to HIGH for approaching targets; otherwise, it is LOW (default).

The outputs from the MMIC are at the voltage level of 1.5 V. They are level-shifted to the voltage level of V_{in} by using the circuit shown in Figure 14. In this circuit, BGT_TARGET_DET and BGT_PHASE_DET are outputs of the MMIC (1.5 V voltage level). V_{DD_RF} is 1.5 V and V_{in} is 3.3 V (when connected with Radar Baseboard MCU7).

- When BGT_TARGET_DET is HIGH (1.5 V), NMOS is off (Vgs = 0 V), and Target_Det_Out is 3.3 V through the R14 pull-up resistor
- When BGT_TARGET_DET is LOW (0 V), NMOS is on (Vgs = 1.5 V), and Target_Det_Out is pulled down to 0 V

The same applies to the BGT_PHASE_DET signal.

Table 4 LED detection

LED	Mode	Comments
Green	On – target detected Off – target not detected	Target_Det_Out is an active LOW signal
Red	On – target departing Off – target approaching	Phase_Det_Out is an active LOW signal

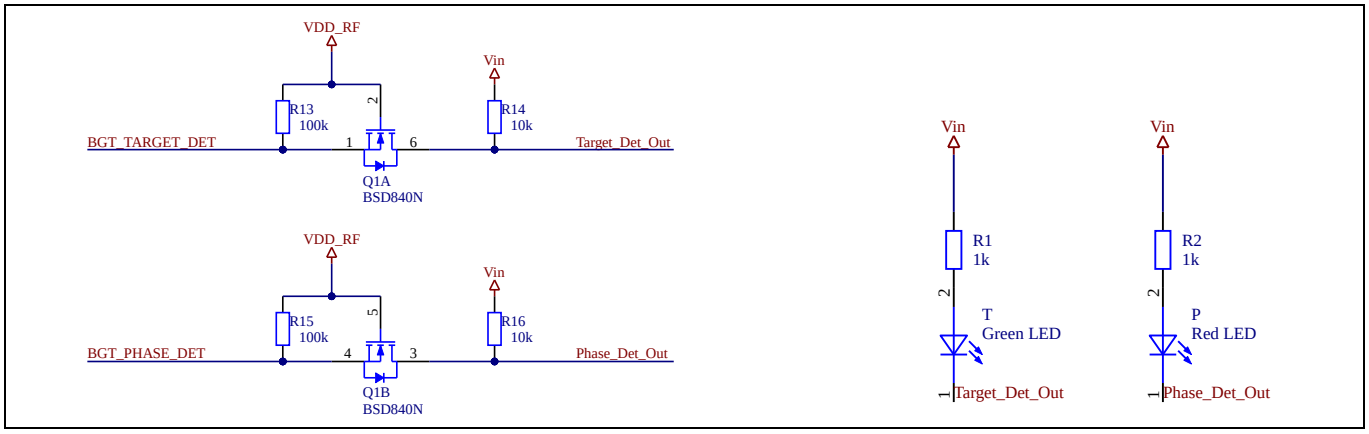


Figure 14 Connections of the LEDs and level shifter

3.9 MMIC quad-state inputs

The BGT60LTR11AIP MMIC has four quad-state inputs QS1 to 4, used in autonomous mode to set the device configuration. Figure 15 shows the default settings of these QS pins on the BGT60LTR11AIP EBG shield.

To offer more flexibility in autonomous mode, an “Advance mode” is enabled when the BGT_PLL_TRIG pin is kept as “1” during chip boot and QS1 is either GND or open. In this ode, BGT_MOSI and BGT_SCK pins are also sampled to determine the pulse repetition time (PRT). In addition, pins QS2 and QS3 are evaluated by the ADC and converted into 4-bit values before each “mean window”.

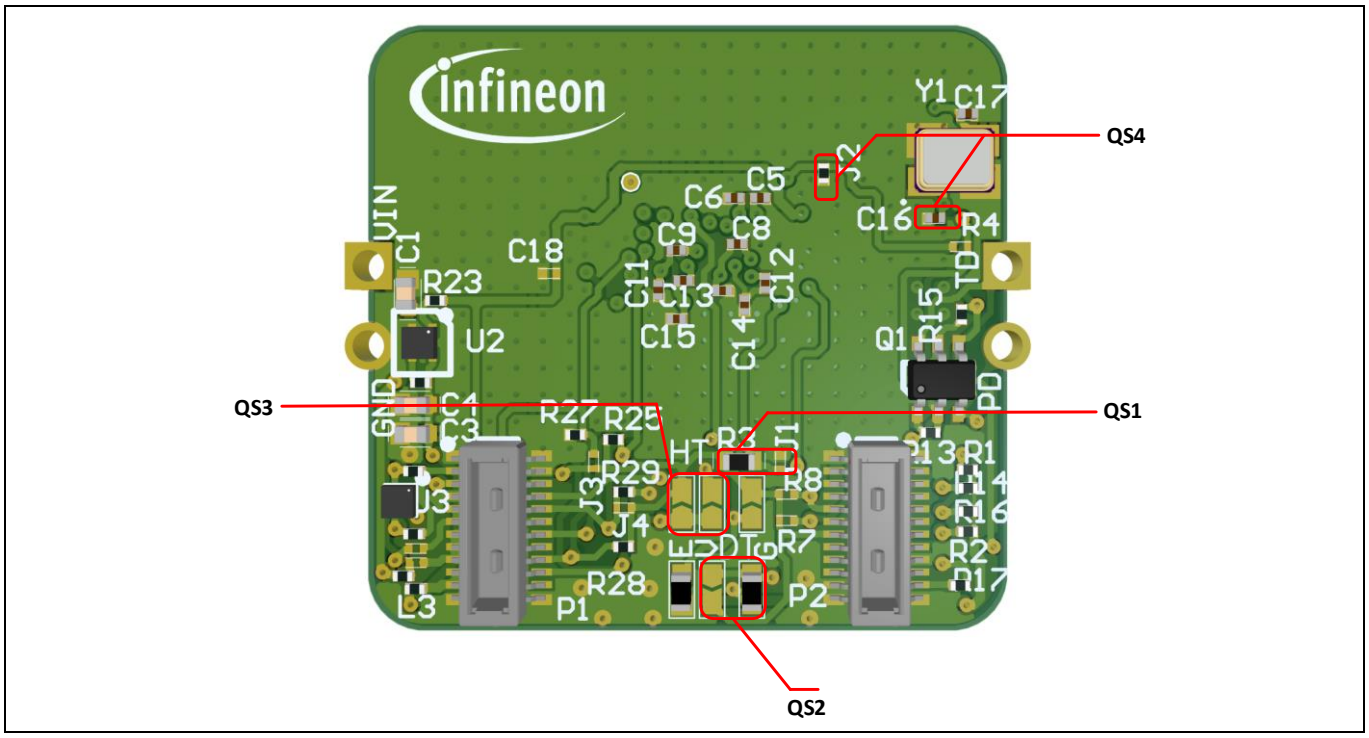


Figure 15 MMIC QS1 to QS4 quad-state inputs (PCB bottom side)

For more details on the BGT60LTR11AIP MMIC quad-state inputs, see UG124434: User guide to BGT60LTR11AIP [2].

3.10 Electromagnetic band gap structure

XENSIV™ BGT60LTR11AIP achieves an excellent antenna performance in a small size and at a low cost. If there is additional space on the PCB, the performance can even be improved through the use of electromagnetic band gap (EBG) structures.

Usually, a part of the RF signal couples onto the PCB through the solder balls and via radiation or coupling. Those electromagnetic signals will then be reflected at metallic surfaces on the PCB or can travel as surface waves on the PCB. These result in radiation from various PCB structures and the PCB edges. The reflected or re-radiated RF signal portions from the PCB will superimpose with the initial RF signal radiated by the sensor antennas. Depending on the phases, this can lead to constructive or destructive interference and will cause deviations of the resulting radiation pattern from the radiation pattern of the sensor antennas. As a result, the PCB design and size can have a noticeable impact on the resulting radiation pattern of the system.

Using an EBG structure placed on the PCB around the sensor package overcomes this challenge and reduces the sensitivity of the resulting radiation pattern from the PCB design.

The EBG structure has two important effects; both effects result in fewer deviations of the initial radiation pattern by the PCB.

- Reflections of an electromagnetic wave traveling perpendicular to the surface of the EBG structure behave in a similar way to reflections from a regular metal plane, but without the 180-degree phase shift.
- The EBG structure strongly reduces the propagation of surface waves on the PCB, leading to lower radiation from PCB structures and PCB edges.

EBG structures in general consist of multiple identical elements placed in a uniform grid. The literature provides various EBG element designs that use different geometries. The geometry of the EBG element defines the inductance and capacitance between neighboring elements and, if present, further PCB layers, which will result in a specific operating frequency band of the individual EBG design.

Figure 16 shows the EBG element design used for the BGT60LTR11AIP RF shield. The EBG consists of a rectangular patch with a centered via connection to the internal PCB GND layer.

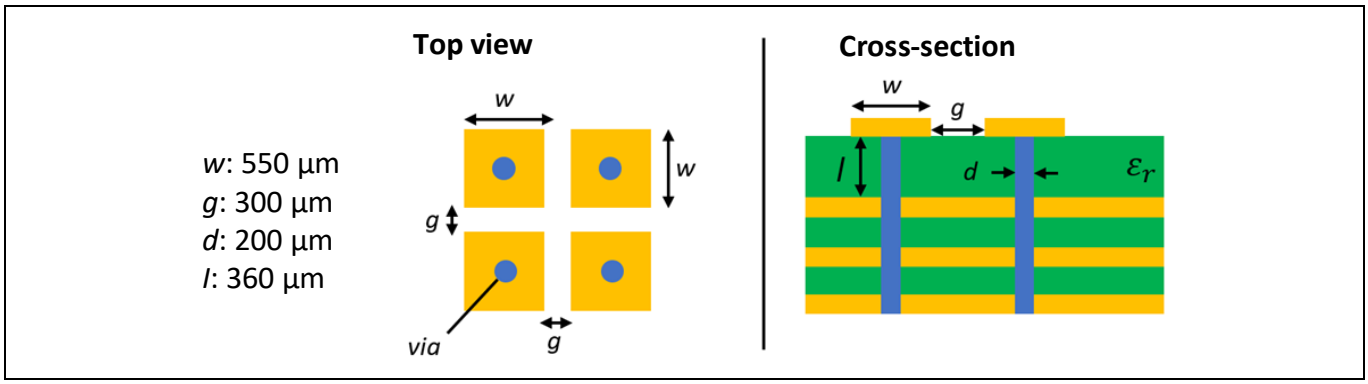


Figure 16 EBG geometry designed for 61 GHz radar on FR4

The size of the patch ($w = 0.55\ mm$) and the periodicity ($w + g = 0.85\ mm$) are designed for an operation frequency around 61 GHz on a FR4 substrate with a thickness of the first laminate layer of ($l = 0.36\ mm$) and a via diameter ($d = 0.2\ mm$). It is important to highlight that this specific EBG design is only valid for the chosen substrate thickness, substrate material, and via diameter. Any changes to these values might require a redesign of the EBG structure to adjust the operating frequency.

The first inner metal layer forms a continuous GND plane underneath the EBG structure. Therefore, only the thickness of the first laminate layer is relevant for this EBG design; the thickness of the other layers can be customized. Blind vias can be used to simplify the routing underneath the EBG area.

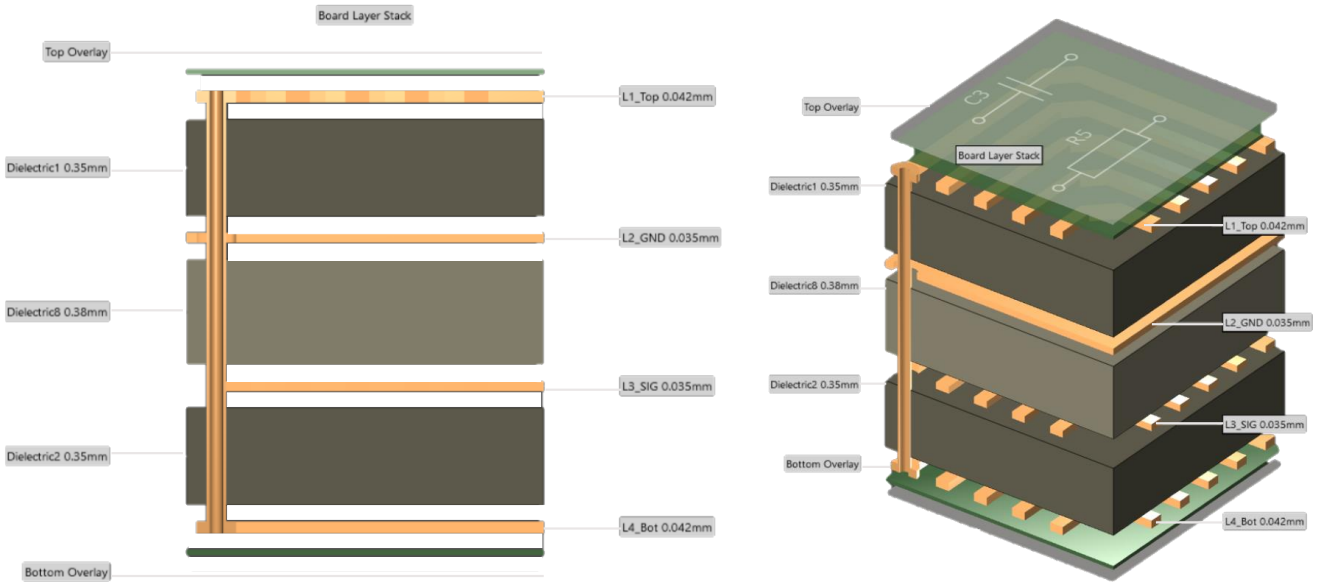
At least three rows of EBG elements in every direction around the sensor are recommended for a significant effect. Additional rows of EBG elements will further decrease the sensitivity of the radiation pattern toward the remaining PCB layout. This results in a trade-off between the area occupied by the EBG elements and radiation performance.

The EBG structure does not necessarily have to be part of every design. For many applications, reasonable performance has been demonstrated without an EBG structure. It is also worth mentioning that the use of the EBG concept will not inherently improve every existing design. However, when the PCB design has a strong impact on the radiation pattern, EBG structures can improve the situation.

Nevertheless, applying the EBG structure around the sensor with sufficient elements provides consistent radiation performance on custom PCB layouts without the need for EM simulations or multiple optimization steps.

3.11 Layer stackup and routing

The PCB is designed with a four-layer stackup with standard FR4 material. Figure 17 shows the different layers and their thicknesses.



#	Name	Material	Type	Weight	Thickness	Dk
	Top Overlay		Overlay			
	Top Solder	Solder Resist	Solder Mask		0.02mm	3.5
1	L1_Top		Signal	1oz	0.042mm	
	Dielectric1	FR-4	Core		0.35mm	4.2
2	L2_GND		Plane	1oz	0.035mm	
	Dielectric8	FR-4	Prepreg		0.38mm	4.2
3	L3_SIG		Signal	1oz	0.035mm	
	Dielectric2	FR-4	Core		0.35mm	4.3
4	L4_Bot		Signal	1oz	0.042mm	
	Bottom Solder	Solder Resist	Solder Mask		0.02mm	3.5
	Bottom Overlay		Overlay			

Figure 17 PCB layer stackup in 2D and 3D views

In the routing on the PCB, the VTUNE pin on the BGT60LTR11AIP MMIC should be left floating. Any components added to the line, or a long wire being connected, can result in spurs.

4 Radar MMIC configuration

The radar MMIC can be configured in two different operation modes. In autonomous mode, the sensor configuration parameters are set via QS pins and external resistors. In SPI mode, the connection to a microcontroller allows setting the sensor configuration parameters by writing in the internal registers through SPI.

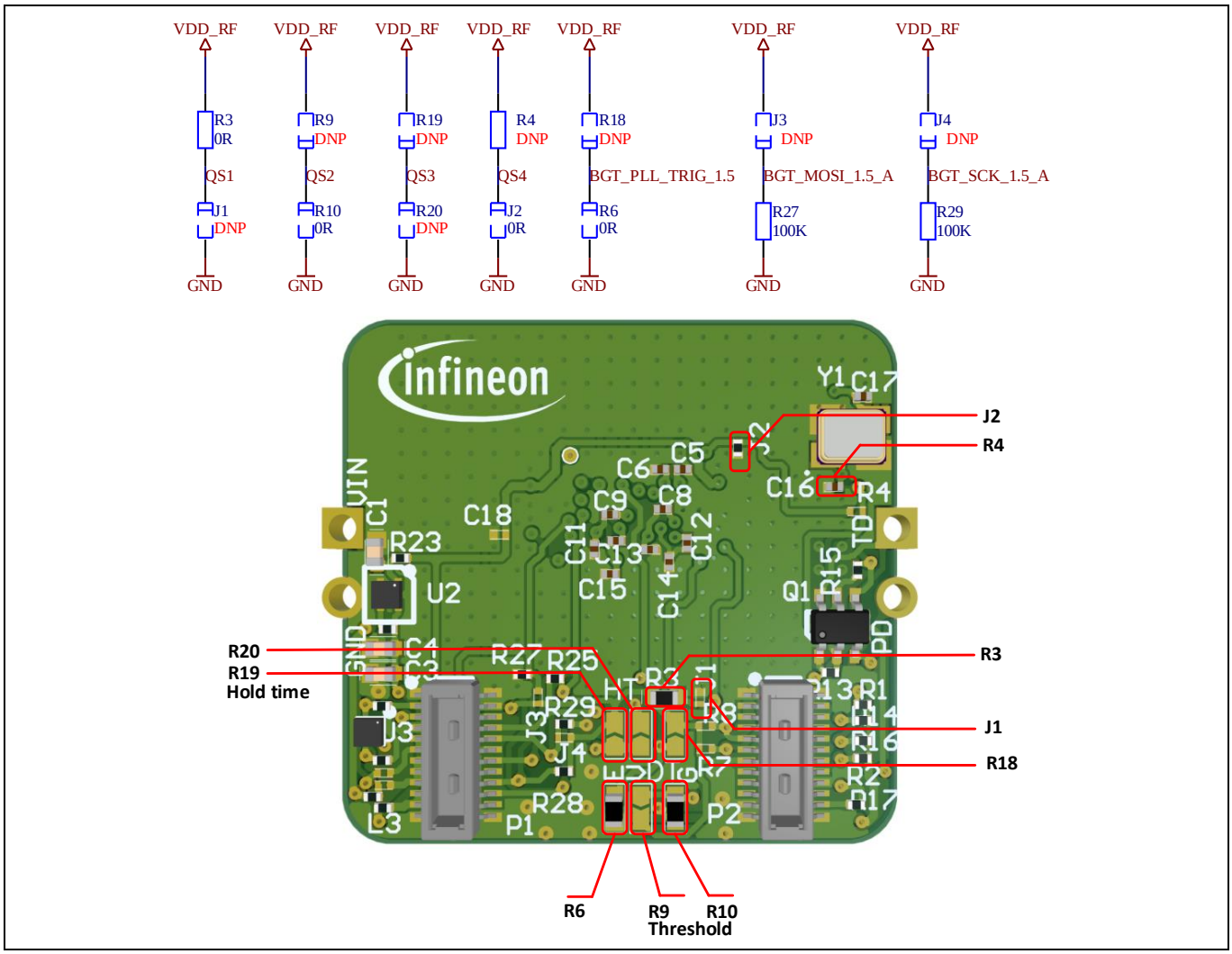


Figure 18 **QS1 to QS4 schematic and layout connections**

4.1 Operation mode

The QS1 pin allows choosing the operation mode of the radar MMIC as shown in Table 5.

Table 5 **QS1 settings**

QS1	Operation mode of the MMIC	PCB configuration	
Ground	Autonomous continuous wave (CW) mode	J1 = 0 Ω	R3 = DNP*
Open	Autonomous pulsed mode	J1 = DNP*	R3 = DNP*
100 kΩ to V_{DD}	SPI mode with external 9.6 MHz clock enabled	J1 = DNP*	R3 = 100 kΩ
V_{DD} (default)	SPI mode	J1 = DNP*	R3 = 0 Ω

*DNP = Do Not Populate/Do Not Place

By default, the BGT60LTR11AIP EBG shield is configured in SPI mode to enable radar MMIC configuration via the FW running on the Radar Baseboard MCU7 microcontroller.

To make the shield work in autonomous mode, you need to remove resistor R3, as shown in Figure 19.

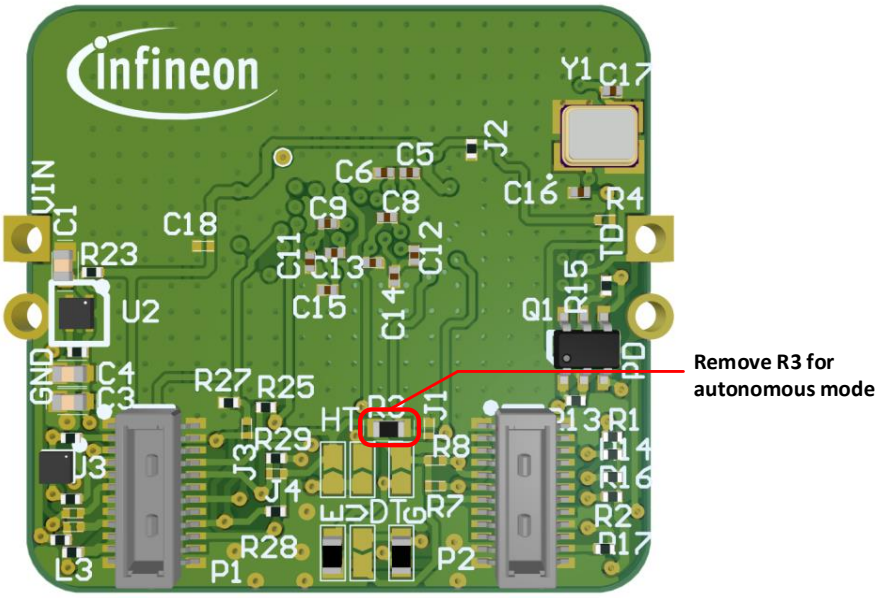


Figure 19 Converting the shield to autonomous mode

Note: Once a BGT60LTR11AIP EBG shield is converted to autonomous mode, it should NOT be connected to a Radar Baseboard MCU7 to change the settings via the GUI. Solder only resistors with values mentioned in Table 5 and Table 6 onto the shield to achieve the desired settings.

4.2 Detector threshold

The internal detector threshold is the minimum signal strength that must be reached to trigger a detection event. The lower the threshold set, the higher the sensitivity and therefore the higher the detection range.

Note: To avoid triggering a false detection, increase the detector threshold, which reduces the sensor sensitivity, especially in "noisy" environments.

Autonomous mode

QS2 is used to select the detector threshold value for autonomous mode. To have up to 16 threshold values, connect PLL_TRIG to V_{DD} by removing R6 and placing R18 = 0 Ω. This will put the MMIC into "Advance mode". The default QS2 setting on the shield is for threshold 80.

See Table 6 for recommended resistor values for changing the QS2 on the autonomous shield.

Table 6 QS2 settings

Resistor settings		Detector threshold (Radar Fusion GUI setting)
R9	**R10**	
10 kΩ	330 Ω	61
10 kΩ	1 kΩ	66
10 kΩ	1.8 kΩ	80 (default)
10 kΩ	2.7 kΩ	90
10 kΩ	3.9 kΩ	112 (Figure 28)
10 kΩ	5.6 kΩ	136
10 kΩ	6.8 kΩ	192
10 kΩ	8.2 kΩ	248
10 kΩ	12 kΩ	320
10 kΩ	15 kΩ	284
10 kΩ	18 kΩ	480
10 kΩ	27 kΩ	640
10 kΩ	39 kΩ	896
10 kΩ	56 kΩ	1344
10 kΩ	100 kΩ	1920
10 kΩ	220 kΩ	2560

SPI mode

In SPI operation mode, you can set the internal detector threshold by writing to the *thrs* (Reg2[12:0]) bit fields of the MMIC SPI registers.

4.3 Detector hold time

The internal detector hold time is the time for which the internal detector outputs remain active after target detection.

Autonomous mode

QS3 is used to select the detector hold time value for autonomous mode. To have up to 16 hold time values, set "Advance mode", as explained in 4.2. The default QS3 setting on the shield for the hold time is 1 s. See Table 7 for recommended resistor values for changing the QS3 on the autonomous shield.

Table 7 QS3 settings

Resistor settings		Detector hold time
R19	**R20**	
10 kΩ	330 Ω	Minimum (16 ms, 32 ms, 64 ms, or 128 ms) depending on the PRT
10 kΩ	1 kΩ	500 ms (default)
10 kΩ	1.8 kΩ	1 s
10 kΩ	2.7 kΩ	2 s
10 kΩ	3.9 kΩ	3 s
10 kΩ	5.6 kΩ	5 s
10 kΩ	6.8 kΩ	10 s
10 kΩ	8.2 kΩ	30 s
10 kΩ	12 kΩ	45 s
10 kΩ	15 kΩ	1 min.
10 kΩ	18 kΩ	90 s
10 kΩ	27 kΩ	2 min.
10 kΩ	39 kΩ	5 min.
10 kΩ	56 kΩ	10 min.
10 kΩ	100 kΩ	15 min.
10 kΩ	220 kΩ	30 min.

SPI mode

In SPI operation mode, you can set the internal detector hold time by writing to the *hold* (Reg10[15:0]) bit fields of the MMIC SPI registers.

4.4 Operating frequency

Autonomous mode

QS4 is used to set the operating frequency for the MMIC in the 60 GHz ISM band, which is important to meet worldwide regulation requirements. See Table 8 for possible settings.

Table 8 QS4 settings

QS4	Device operating frequency	PCB configuration	
Ground (default)	61.1 GHz	J2 = 0 Ω	R4 = DNP*
Open	61.2 GHz	J2 = DNP*	R4 = DNP*
100 kΩ to V_{DD}	61.3 GHz	J2 = DNP*	R4 = 100 kΩ
V_{DD}	61.4 GHz	J2 = DNP*	R4 = 0 Ω

*DNP = Do Not Populate/Do Not Place

SPI mode

In SPI operation mode, you can set the device operation frequency by writing to the *pll_fcw* (Reg5[11:0]) bitfields of the MMIC SPI registers. The BGT60LTR11AIP device operates in the 61 GHz to 61.5 GHz frequency band.

Note: Keep a 50 MHz guard band on each side of the band edge to avoid emissions outside the ISM band.

Note: Sensors operating close together at the same operating frequency can interfere with each other. To avoid this, set different operating frequencies for each device, with a difference of at least 12 MHz.

4.5 Pulse repetition time (PRT)

PRT is the duty cycle repetition rate, which means the time until the next pulsing sequence starts in pulsed mode.

Autonomous mode

The PRT can be configured in autonomous pulsed mode (QS1 is either GND or OPEN, as shown in Table 5) only if “Advance mode” is enabled by keeping the PLL_Trig pin to “1”. The SPI pins BGT_MOSI and BGT_SCK are sampled during chip boot-up and determine the PRT setting, as shown in Table 9.

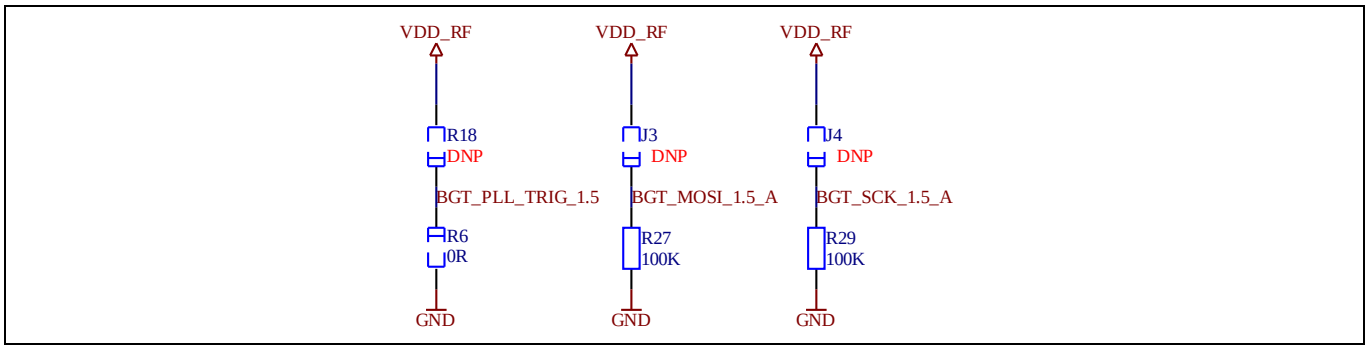


Figure 20 Configuring PRT

Table 9 PRT configuration in (pulsed) autonomous mode

BGT_PLL_TRIG*	BGT_MOSI	BGT_SCK	PRT	PCB components			
1	0	0	500 µs	J3 = DNP*	R27 = 100 kΩ	J4 = DNP*	R29 = 100 kΩ
1	0	1	2000 µs	J3 = DNP*	R27 = 100 kΩ	J4 = 100 kΩ	R29 = DNP*
1	1	0	250 µs	J3 = 100 kΩ	R27 = DNP*	J4 = DNP*	R29 = 100 kΩ
1	1	1	1000 µs	J3 = 100 kΩ	R27 = DNP*	J4 = 100 kΩ	R29 = DNP*

*R6 = DNP, R18 = 0 Ω, DNP = Do Not Populate/Do Not Place

SPI mode

In SPI pulsed operation mode, you can set the PRT value by writing to the *dc_rep_rate* (Reg7[11:10]) bitfields of the MMIC SPI registers.

You can also enable the adaptive pulse repetition time (APRT) by writing to the *aprt* (Reg2[6]) bitfield of the MMIC SPI registers. The PRT multiplier factor, of 2, 4, 8, or 16, is also set by writing to the *prt_mult* (Reg13[1:0]) bitfields.

5 Autonomous mode operation

In autonomous mode operation, the MMIC uses only internal detectors for motion and direction of motion indication. The BGT60LTR11AIP autonomous shield can be powered directly through the castellated holes on the sides of the shield or through a baseboard platform like Radar Baseboard MCU7.

5.1 Battery-powered operation

The BGT60LTR11AIP autonomous shield can operate independently with a battery that supplies to the VIN and GND pins of the castellated holes. The shield will generate internal detector outputs on TD (**TD**et) and PD (**PD**et) castellated holes depending on the movement of the target. As shown in Figure 21, the output signals **TD**et and **PD**et are connected to LEDs, which glow according to target movement (TD) and direction of movement (PD).

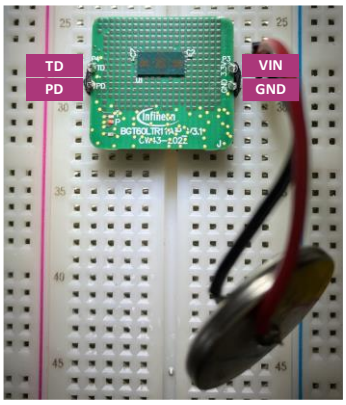


Figure 21 Radar shield working independently with a battery power supply

5.2 Arduino MKR operation

The shield has dimensions such that it can be mounted onto an Arduino MKR series board as a plug-in motion sensor, as shown in Figure 22.

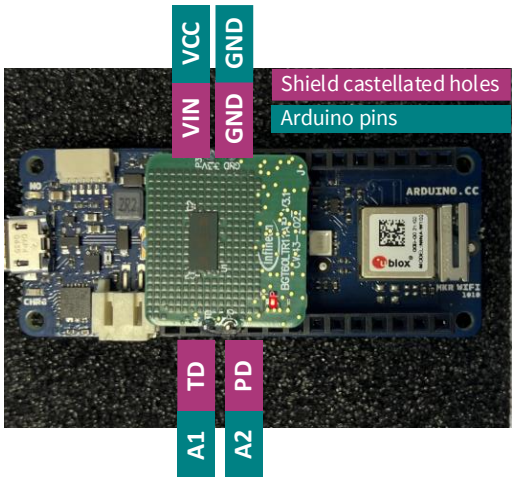


Figure 22 Radar shield mounted on an Arduino MKR Wifi1010 board

Find the BGT60LTR11 Radar Arduino Library and instructions to get started on Infineon's GitHub repository.

6 Firmware

6.1 Overview

Radar Baseboard MCU7 comes with a default FW that serves as a bridge between a host (typically a PC) and the BGT60LTR11AIP RF shield mounted on sensor connectors.

When the FW detects a BGT60LTR11AIP EBG shield, it automatically configures the driver layer for the BGT60LTR11AIP sensor. This includes configuring the chip, as well as setting up the MCU to initiate an SPI transfer when the sensor signals the availability of new data via the IRQ line. The FW will also configure the communication layer so that messages specific to the radar and BGT60LTR11AIP are understood.

For more details, see the UG091519: Radar Baseboard MCU7 user guide note [3].

6.2 SPI MISO arbitration

The BGT60LTR11AIP MMIC V3.0 implements a new internal digital detector using the internal ADC samples from I/Q signals. Thus, internal access to ADC values must be multiplexed with external SPI access (from Radar Baseboard MCU7), in a process known as “SPI MISO arbitration”.

The SPI MISO line arbitration is active in the following situations:

- The BGT60LTR11AIP device is active after a hard reset or soft reset, and after bootup time in any autonomous mode.
- After activation of SPI “Pulsed mode” (set *start_pm* (Reg15[14]) bit to “1”).
- After activation of SPI “CW mode” (set *start_pm* (Reg15[14]) bit and *start_cw* (Reg15[12]) bit to “1”).

By default, the SPI MISO line arbitration is in High-Z state after reset to avoid disturbance in a multi-client SPI setup. This line must be set explicitly into driving mode by setting the *miso_drv* (Reg15[6]) bit to “1” to be active outside SPI access.

This approach has the following consequences:

- If the BGT60LTR11AIP registers need to be set only once before “Pulsed mode” is activated, ignore MISO arbitration. Use the hard-reset pin instead of soft-reset via Reg15 to avoid SPI access.
- If the BGT60LTR11AIP registers need to be updated when the device is running, use MISO line arbitration.
- If a clear synchronization to the RF pulse is required, use MISO arbitration. Set up synchronization just before starting “Pulsed mode” (the rising edge of MISO indicates a good sampling point).
- If “div-out” RF-Pulse-sync is already used or implemented, it can still be used.

For more details on the BGT60LTR11AIP MMIC registers, see the BGT60LTR11AIP datasheet [1].

To implement MISO arbitration, you need a rising-edge and falling-edge IRQ on the GPIO line. You could consider multiplexing on the MISO pin. You should also consider implementing a guard timer to prevent access sometime before the next pulse is required. A guard timer is not required if only a **defined** sequence of SPI accesses is performed, and if arbitration timing is ensured.

Use the following procedure to synchronize access with pulsing:

After starting Pulsed/CW mode, register the rising-edge IRQ to synchronize with pulse, block SPI access.

1. Wait for a rising edge on the MISO line (via IRQ):

a) Deactivate the rising-edge IRQ.

b) Start the guard timer with “pulse repletion rate – guard time”.

c) Activate falling-edge IRQ.

2. After the falling edge on the MISO line:
a) Deactivate the falling-edge IRQ.
b) MCU SPI communication allowed.
c) Start the readout of internal ADC registers (Reg40 and Reg41) if required.
d) Perform other SPI register access operations.

3. When the guard timer expires:
a) Block SPI communication.
b) Activate the rising-edge IRQ.

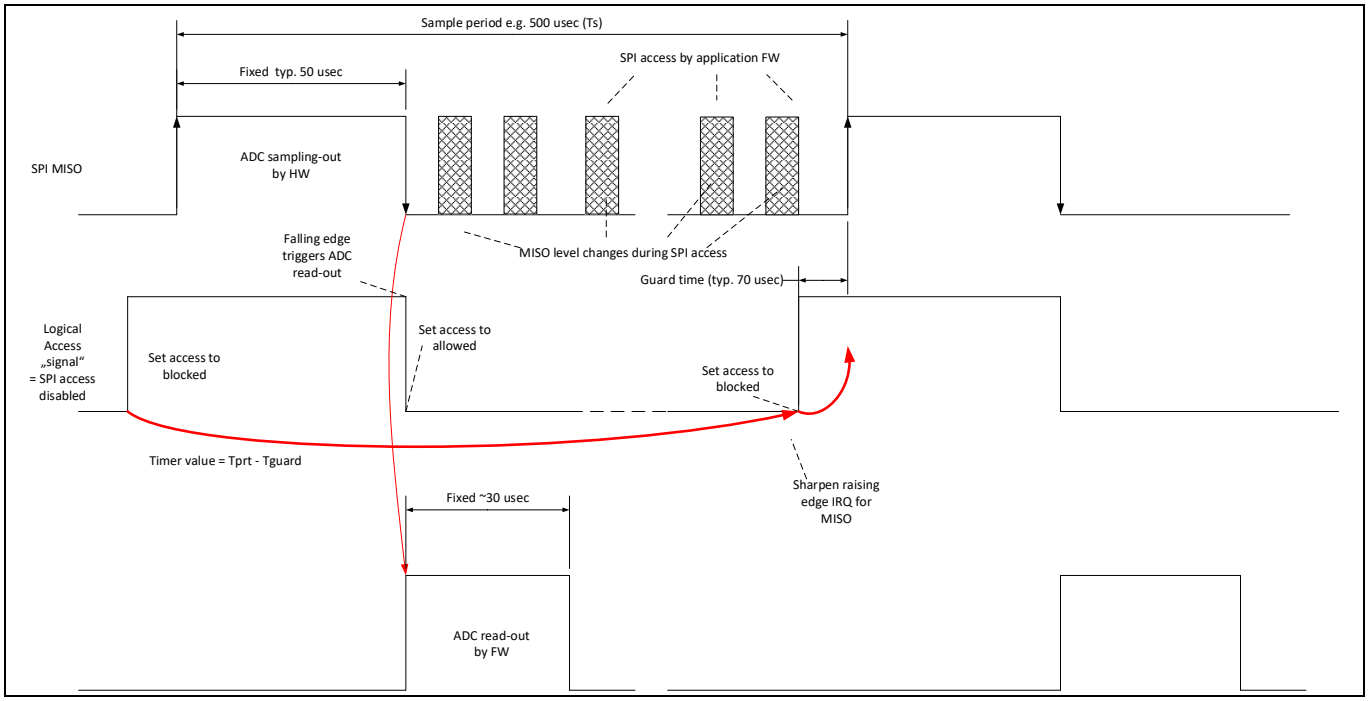


Figure 23 Synchronized SPI access time diagram

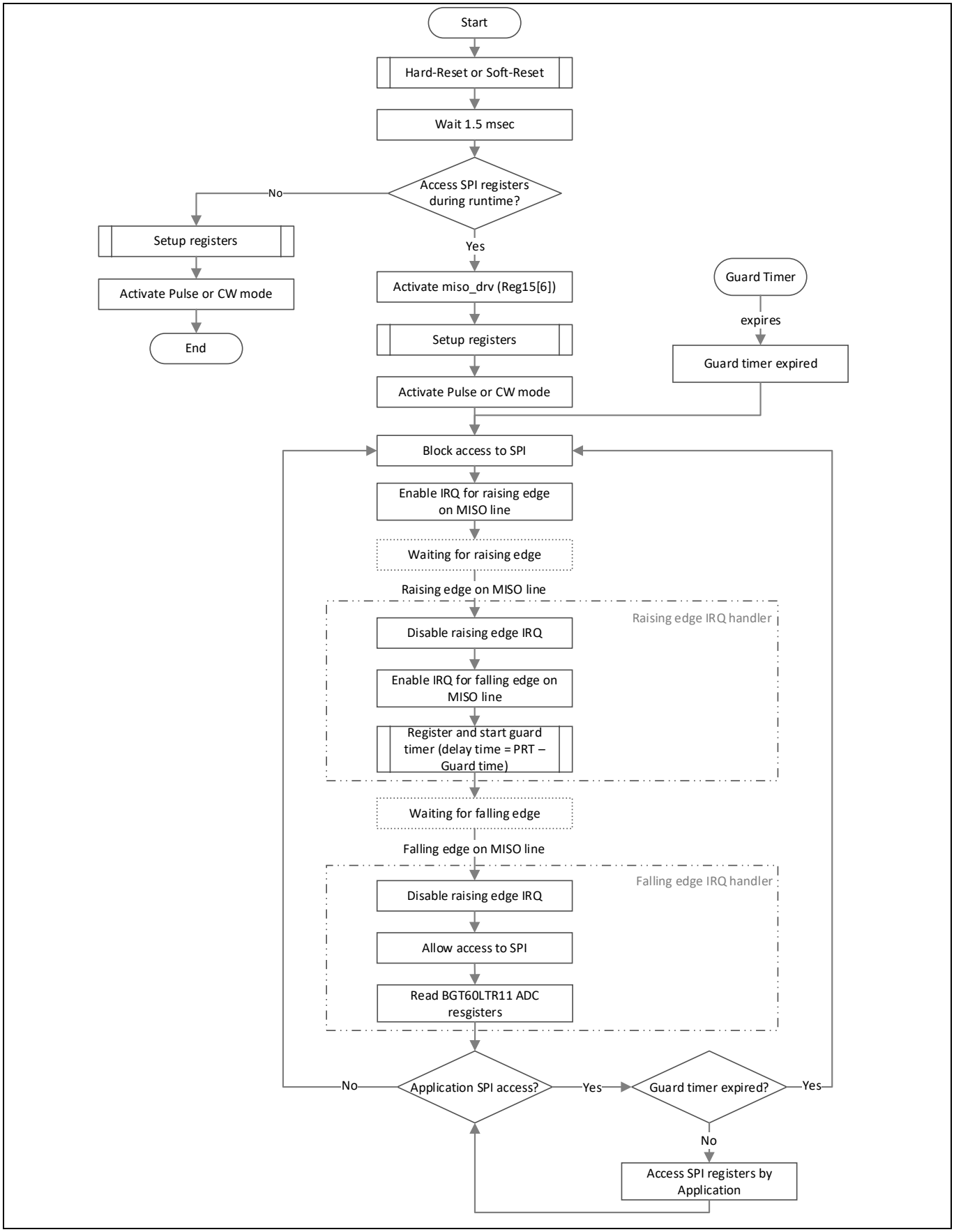


Figure 24 SPI arbitration flow diagram

Note the following:

- MISO line is High-Z if Chip Select (CS) is inactive (default).
- MISO arbitration can be enabled via the *miso_drv* (Reg15[6]) bit.
- Without respecting MISO arbitration, device functionality is NOT ensured.
- Only the I/Q channel (Reg40 and Reg41) is sampled via the internal state machine. For other ADC channels, explicit ADC conversion must be triggered manually.
- If an external ADC is used for sampling, the best time for S/H activation is at the rising edge of the MISO arbitration signal. Conversion could be done later.

Figure 25 shows a typical access:

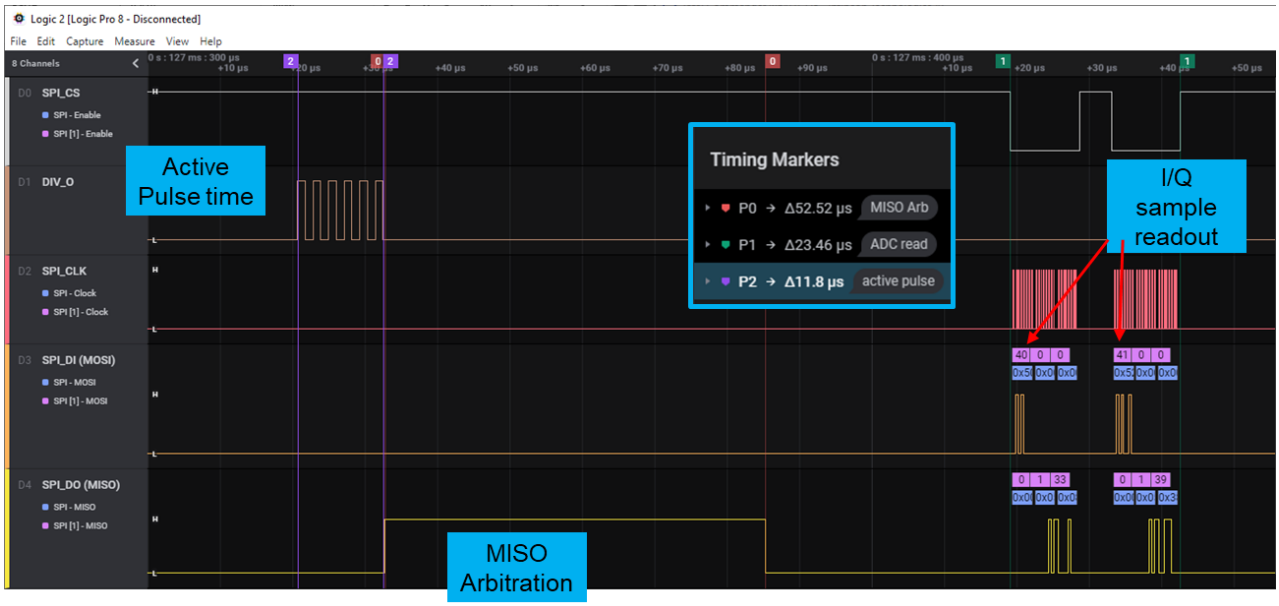


Figure 25 Typical SPI access

7 Measurement results

7.1 Radiation pattern simulation results

To analyze the sensor radiation characteristics, the radiation pattern of a BGT60LTR11AIP EBG shield configured in CW mode is simulated along the H-plane and E-plane of the sensor. Figure 26a shows the realized gain of the transmitting antenna in H-plane and E-plane at a frequency of 61 GHz. Figure 26b shows the antenna characteristics of the receiving antenna in H-plane and E-plane at a frequency of 61 GHz.

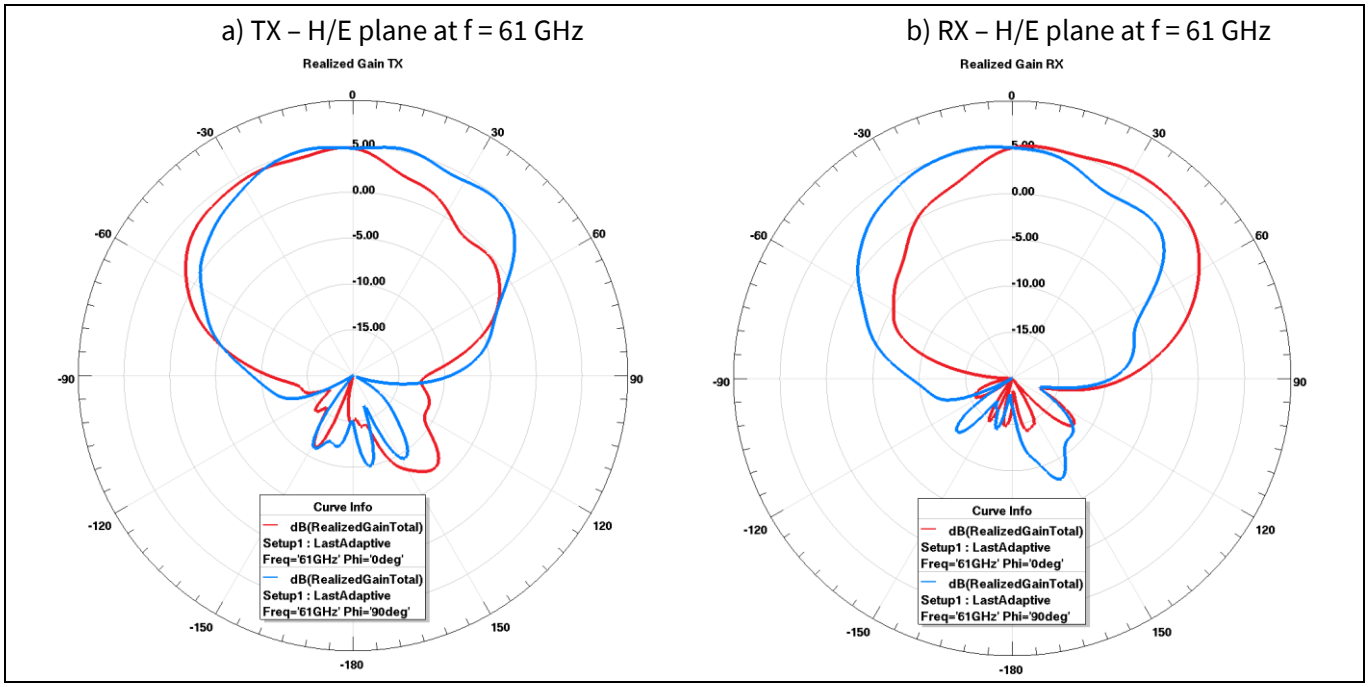


Figure 26 Radiation pattern simulations of the BGT60LTR11AIP EBG shield in CW mode

The equivalent isotropically radiated power (EIRP) of the transmitter path is measured along the H-plane and E-plane of the sensor in an anechoic chamber with a spectrum analyzer. Figure 27 shows the EIRP gain of the transmitting antenna in H-plane and E-plane at a frequency of 61 GHz.

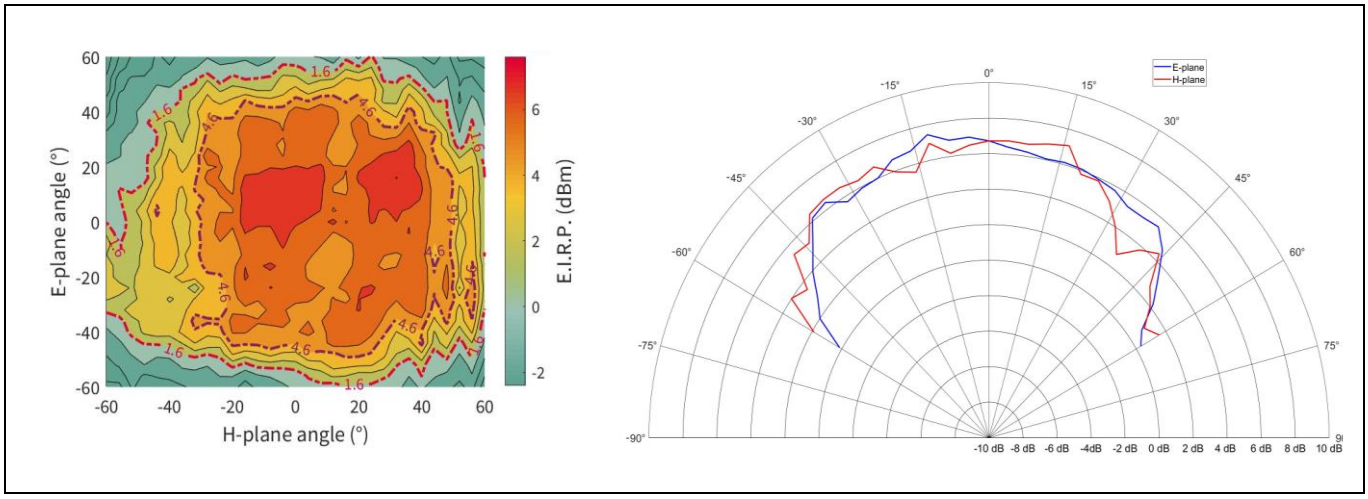


Figure 27 EIRP TX measurement result at carrier frequency of 61 GHz

7.2 Motion detection area

The measurements are conducted for different MMIC operation modes and settings. Figure 28 shows the possible operating modes, and how the detection status is driven.

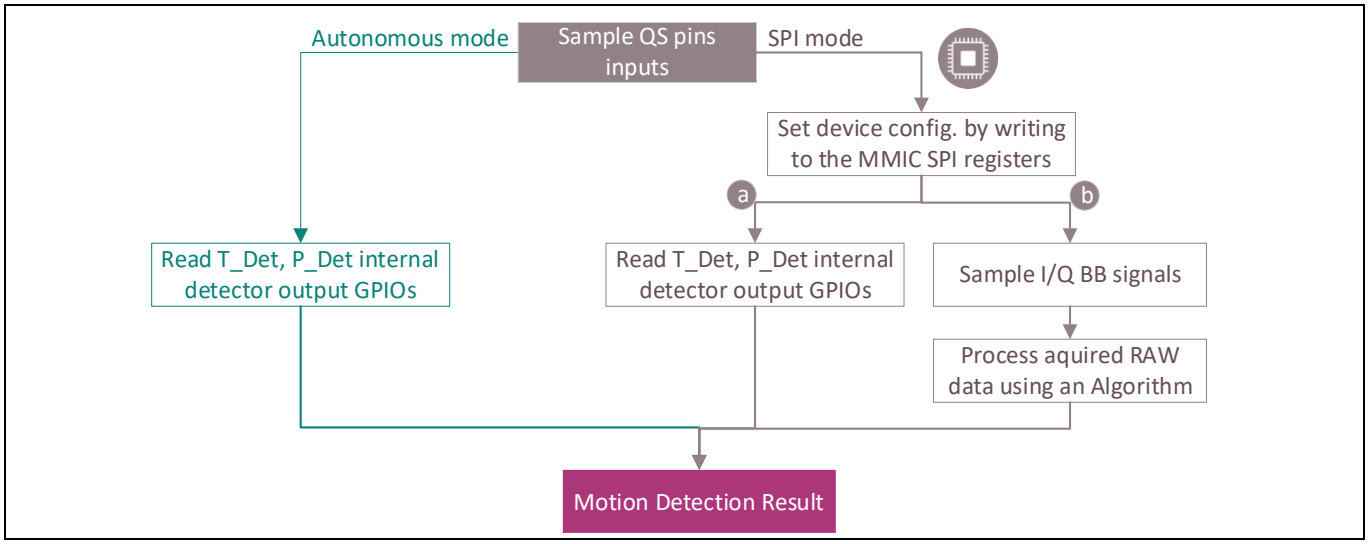


Figure 28 Shield operation modes and motion detection status

7.2.1 Autonomous mode

- **Hardware**
  BGT60LTR11AIP EBG shield (which is configured by default in autonomous pulsed mode). For more details, see Section 5.
- **Firmware**
  No FW is required for the autonomous shield.
- **Height**
  Board is placed at 1.2 m.
- **Scenario**
  Measure the maximum detection range of a human target along the H/E plane of the sensor for different angles.
- **Detection status**
  Driven from the internal detector output (**TD**et). Figure 29 shows the measurement results in the H-plane and E-plane and the correct shield orientation.

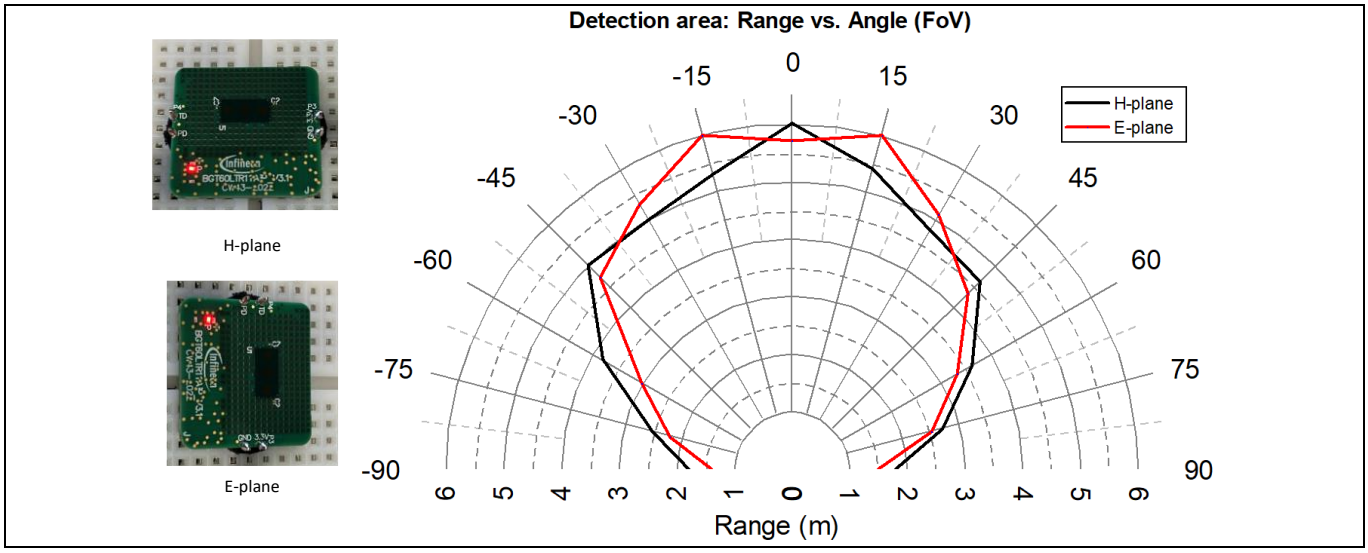


Figure 29 **H-plane and E-plane human target detection area for BGT60LTR11AIP autonomous shield**

7.2.2 SPI mode and MMIC internal detector

- **Hardware**
  Radar Baseboard MCU7 and BGT60LTR11AIP EBG shield (by default, configured in SPI pulsed mode).
- **Firmware**
  Used only to set the shield configuration by writing to the MMIC SPI registers Figure 28a shows. The "Radar Integrated Motion Sensing" application available from the Radar Fusion GUI is used.
- **Height**
  Board is placed at 1.2 m.
- **Scenario**
  Measure the maximum detection range of a human target along the H-plane and E-plane of the sensor for different threshold values (selected from the GUI) and different angles.
- **Detection status**
  Driven from the internal detector output (**TD**et). Figure 30 and Figure 31 show the measurement results in the H-plane and E-plane respectively, and the correct shield orientation.

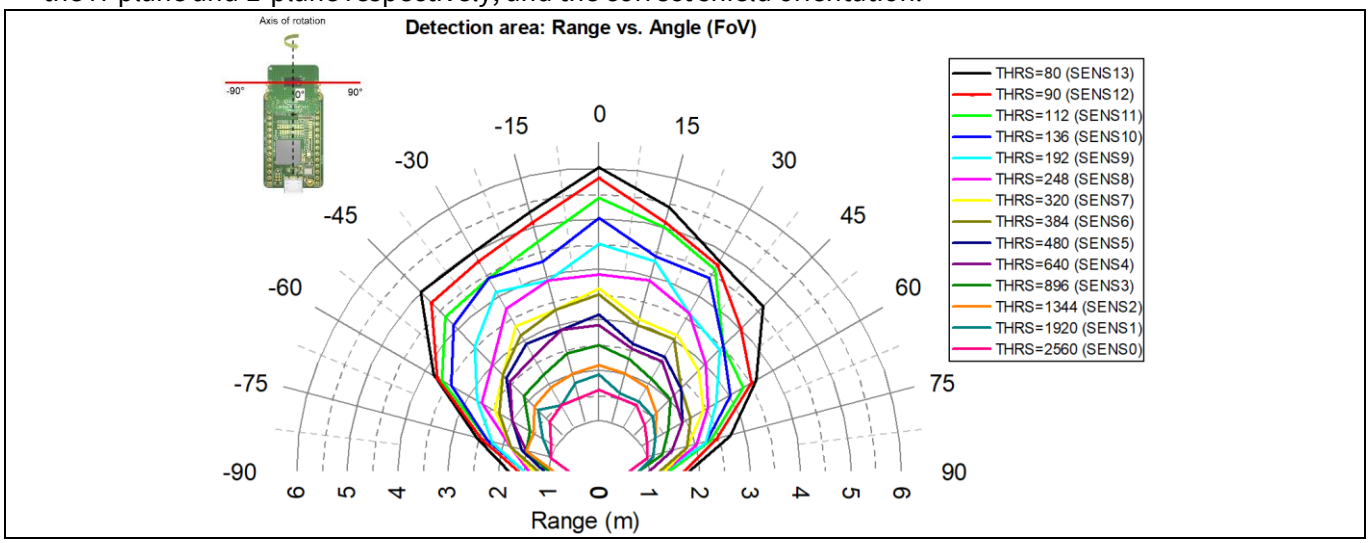


Figure 30 **H-plane human target detection area, in SPI mode, using MMIC internal detector**

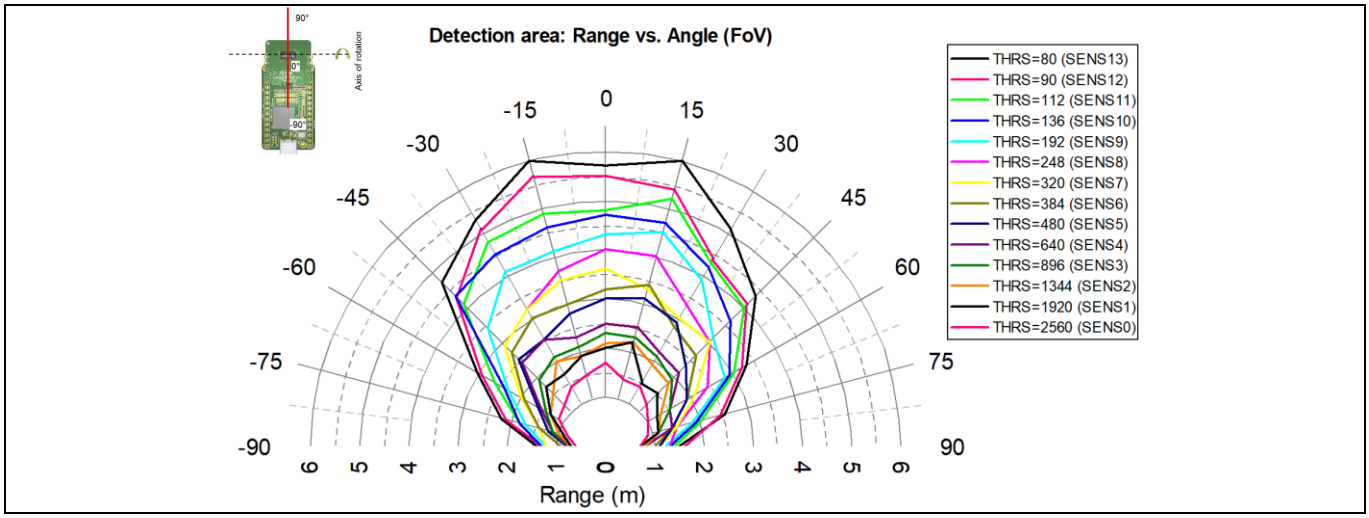


Figure 31 **E-plane human target detection area, in SPI mode, using MMIC internal detector**

7.2.3 SPI mode and motion detection algorithm

- **Hardware**
  Radar Baseboard MCU7 and BGT60LTR11AIP EBG shield (by default, configured in SPI pulsed mode).
- **Firmware**
  Used to set the shield configuration by writing to the MMIC SPI registers, sample the I&Q baseband signals, and process the acquired RAW data through a motion detection algorithm as Figure 28b shows. The “Radar Advanced Motion Sensing with SPI” application available from the Radar Fusion GUI is used.
- **Height**
  Board is placed at 1.2 m.
- **Scenario**
  Measure the maximum detection range of a human target along the H-plane and E-plane of the sensor for different angles, with the default configuration, and with an algorithm set threshold value of 15, which can be selected from the Radar Fusion GUI.
- **Detection status**
  Driven from the advanced motion detection algorithm output. Figure 32 shows the measurement results in the H-plane and E-plane and the correct shield orientation.

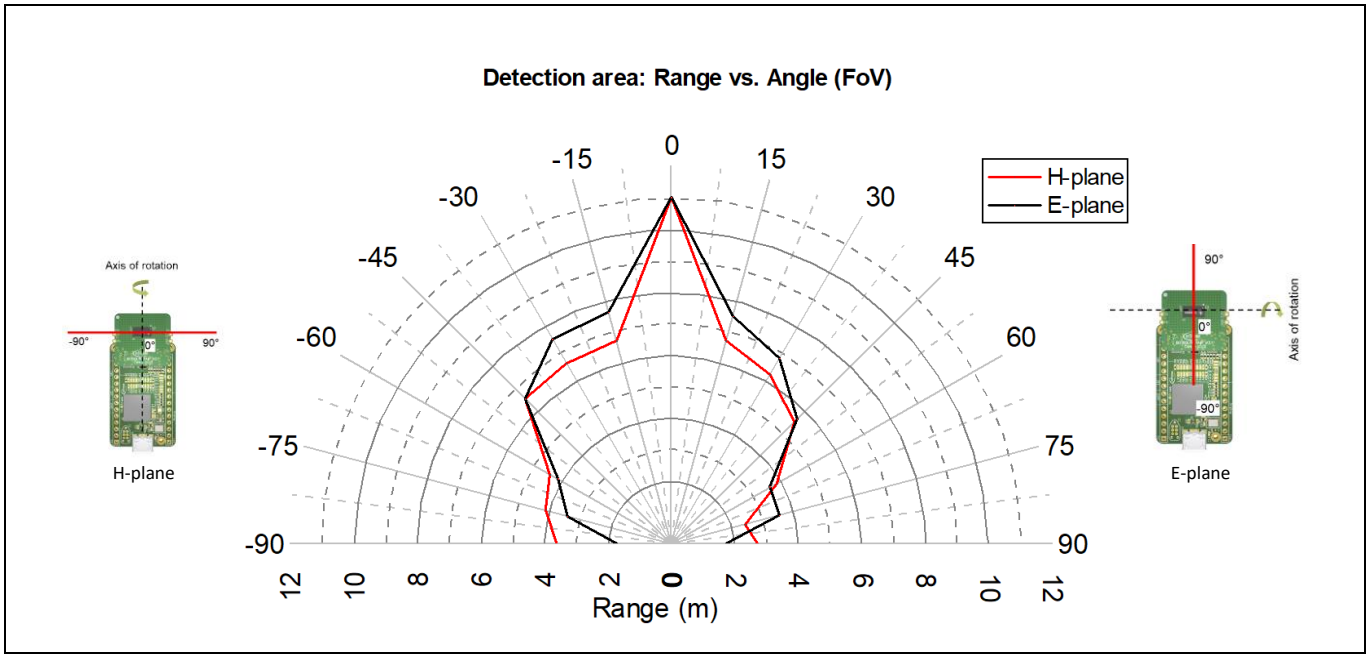


Figure 32 **H-plan and E-plane human target detection area, in SPI mode, using advanced motion sensing (AMS) algorithm**

7.2.4 On-ceiling measurements

- **Hardware**
  Radar Baseboard MCU7 and BGT60LTR11AIP EBG shield (by default, configured in SPI pulsed mode).
- **Firmware**
  Used to set the shield configuration by writing to the MMIC SPI registers, sample the I&Q baseband signals, and process the acquired RAW data through a motion detection algorithm as shown in Figure 28b.
- **Height**
  Board is placed at 3 m height, facing down.
- **Scenario**
  Measure the maximum detection range of a human target along different angles, with the default configuration, and with an algorithm, which can be selected from the Radar Fusion GUI.
- **Detection status**
  Measurement 1 is driven from the internal detector output (**TD**et). Figure 33 shows the measurement result in red and the correct shield orientation.

  Measurement 2 is driven from the output of the advanced motion detection algorithm. Figure 33 shows the measurement result in blue and the correct shield orientation.

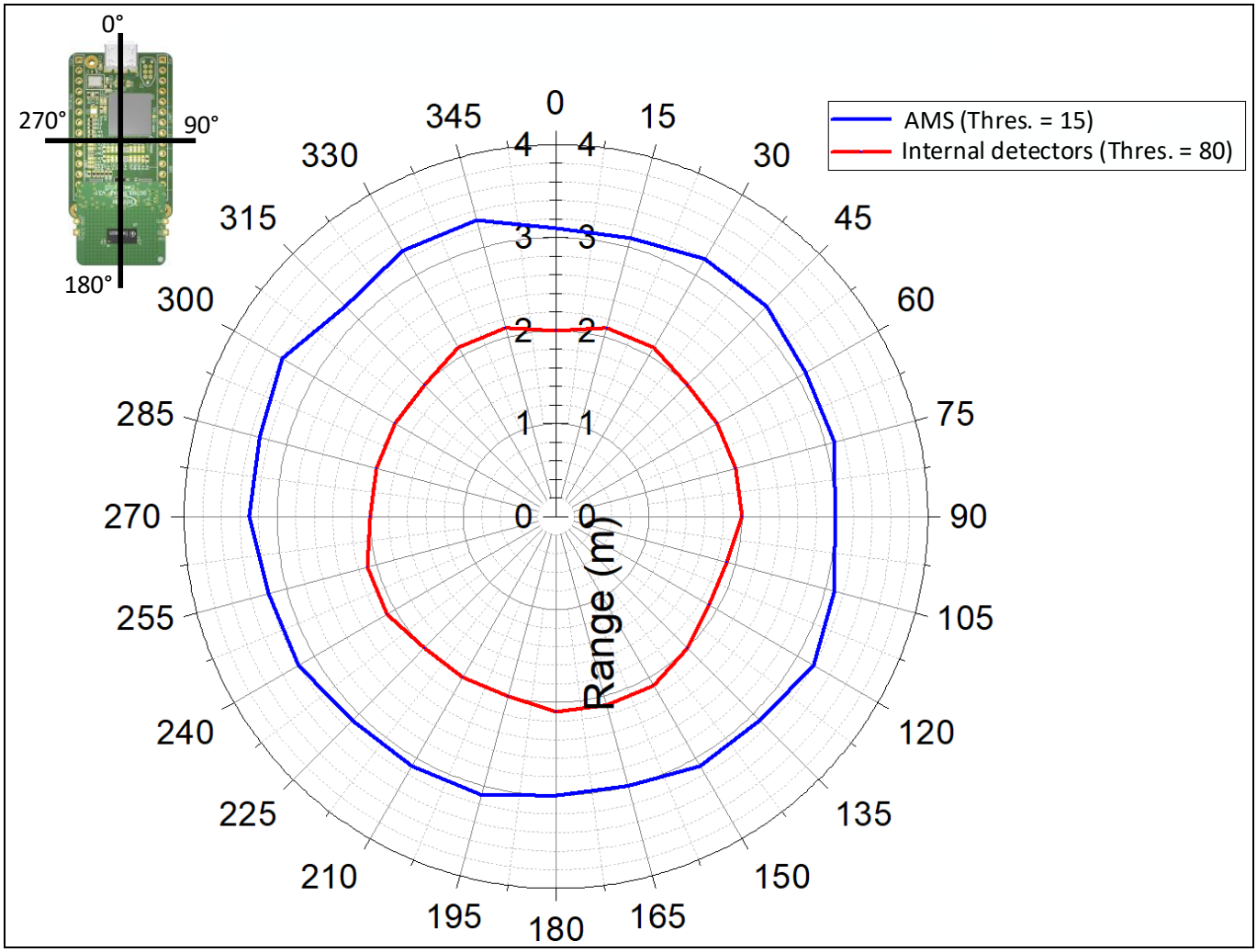


Figure 33 **On-ceiling measurement results in SPI mode using the radar internal detectors (in red) and the AMS algorithm (in blue)**

8 Power consumption analysis

8.1 Duty cycling

The current consumption of the BGT60LTR11AIP MMIC can be optimized by configuring the duty cycle pulse width (PW) and pulse repetition time (PRT). Table 10 lists the current consumption values of the MMIC with the default PW of 5 µs (the time MMIC is active during one pulsing event).

Table 10 Average current consumption of the BGT60LTR11AIP EBG shield in SPI pulsed mode

PW (µs)	PRT (µs)	Current consumption (mA)
5	250	6.752
5	500 (default)	3.776
5	1000	2.288
5	2000	1.544

Figure 34 shows the current consumption of the BGT60LTR11AIP EBG shield.

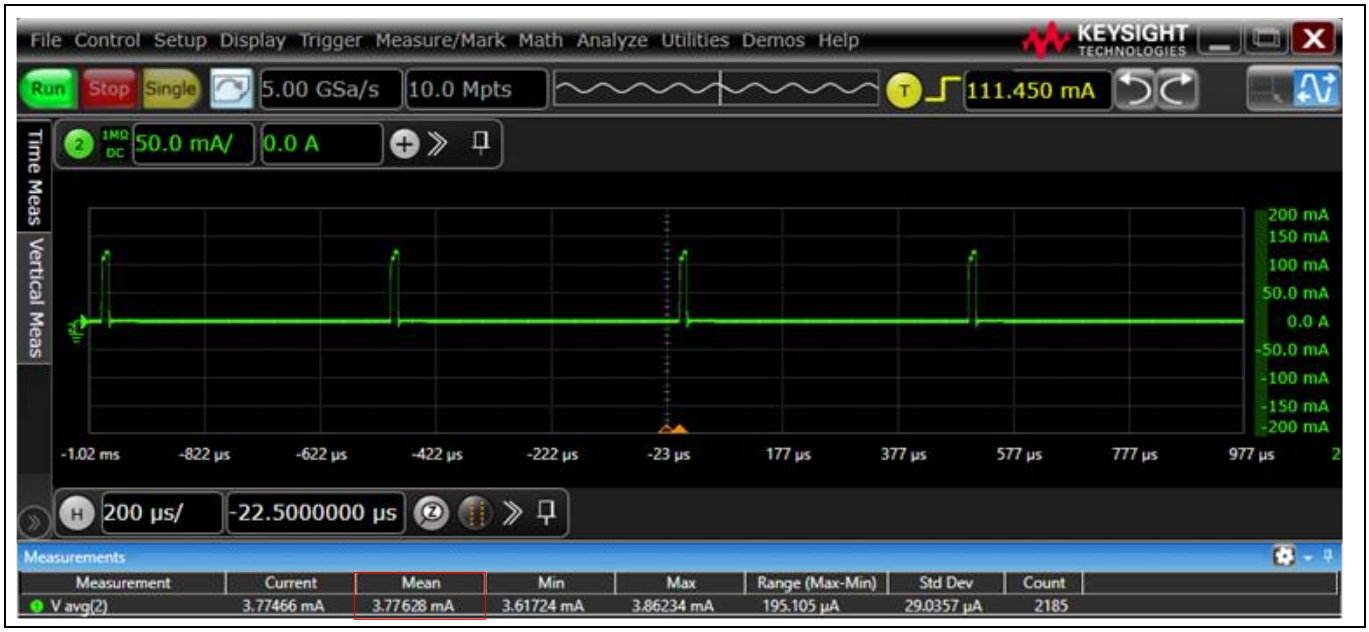


Figure 34 Current consumption of shield with PW = 5 µs and PRT = 500 µs

8.2 Adaptive pulse repetition time (APRT)

APRT is a power-saving option of the BGT60LTR11AIP MMIC. It consists of multiplying the PRT by a factor of 2, 4, 8, or 16 when no target is detected by the internal detector. When a target is detected, the PRT returns to the default value to ensure reliable detection.

Enabling the APRT feature as an additional power-saving option effectively reduces the on-time of the MMIC because the default PRT is only used when a target is detected. Depending on the use case and the multiplier value selected, the power consumption of the shield can be reduced significantly. The following figures show how the set PRT = 500 µs changes when APRT is enabled with different multiplication factors and when a target is detected.

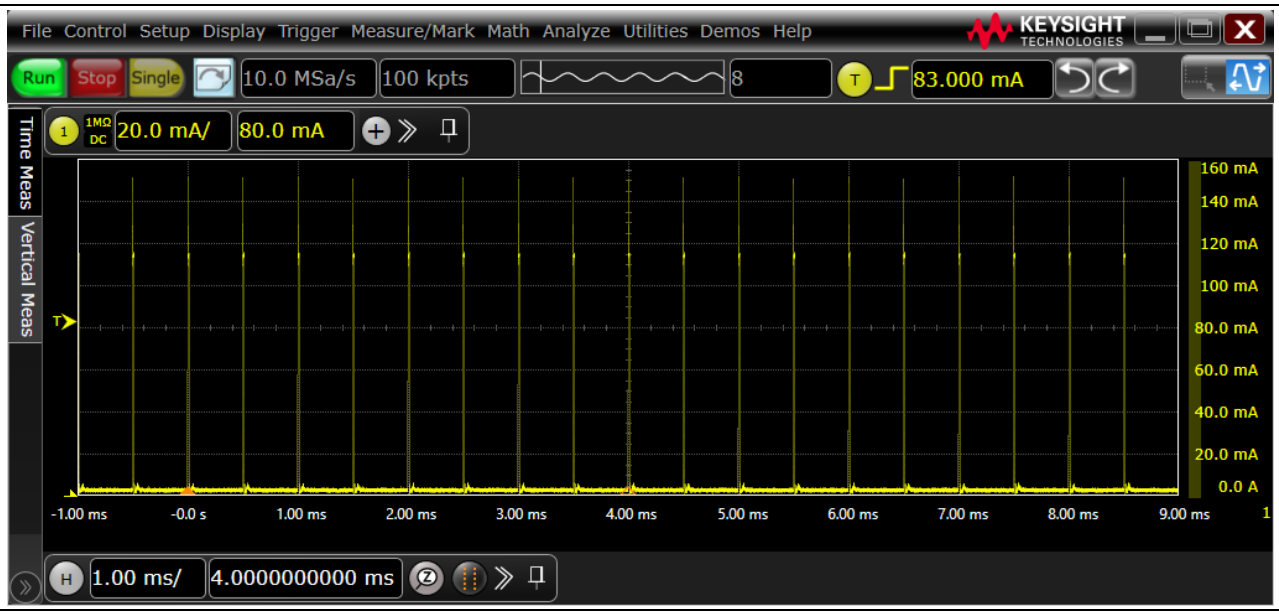


Figure 35 APRT disabled: Target detected/no target detected; PRT remains 500 µs

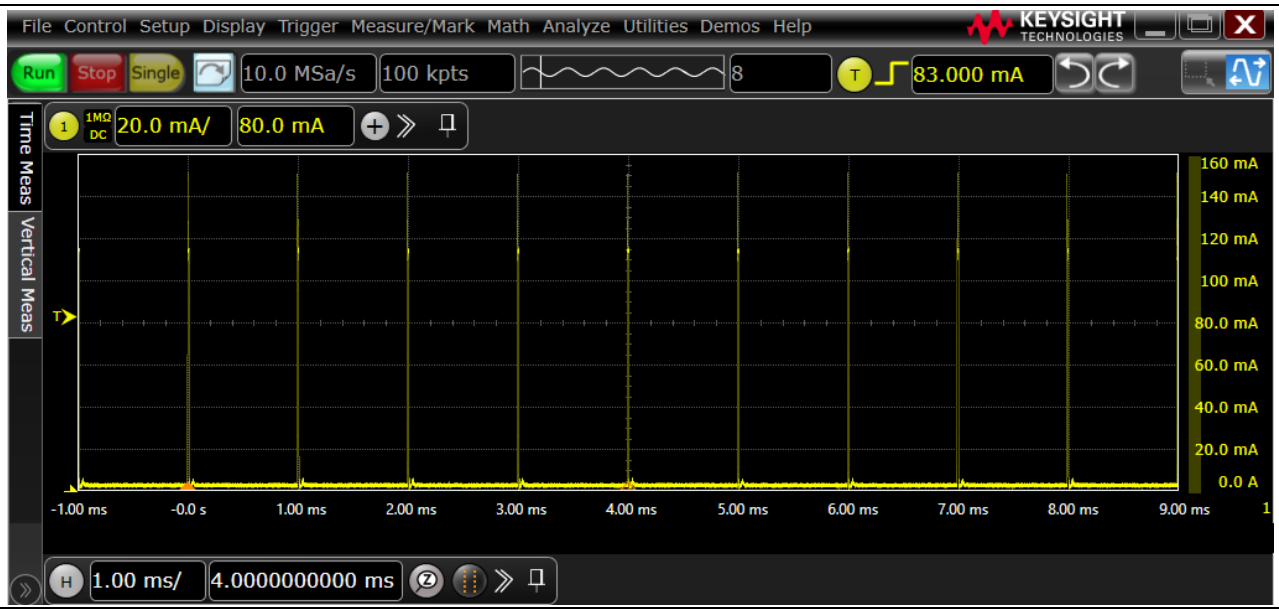


Figure 36 APRT enabled: Multiplier x2, no target detected; PRT switches to 1 ms

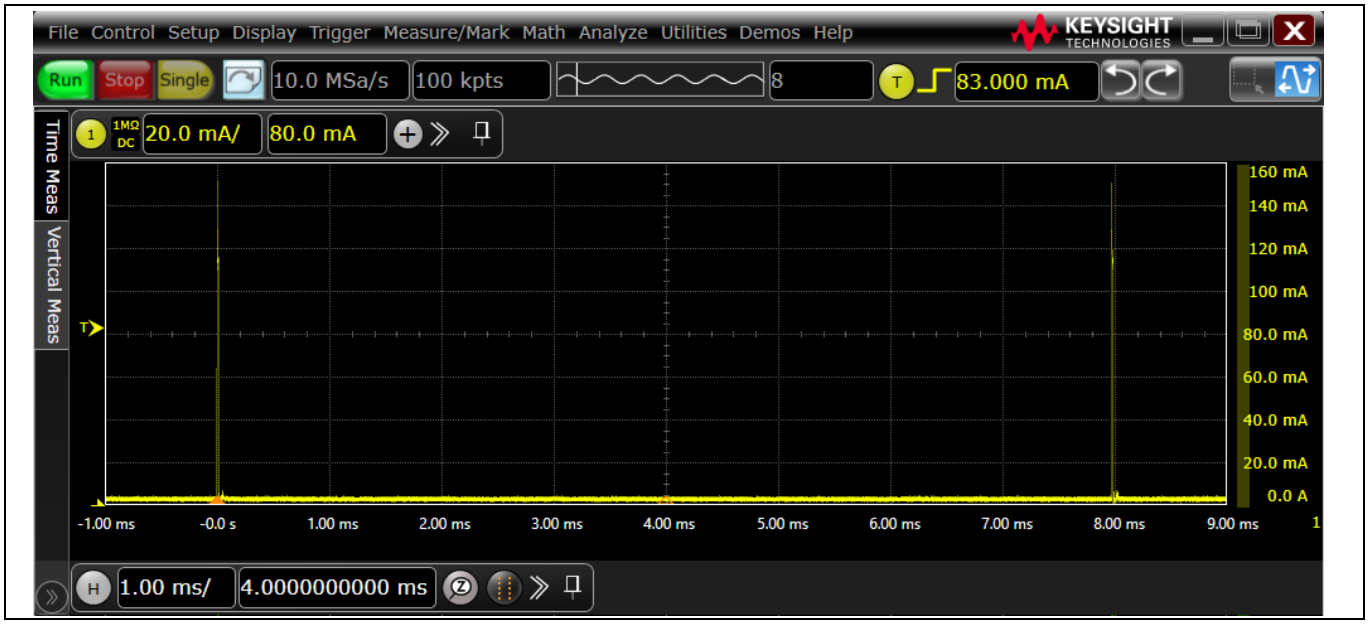


Figure 37 **APRT enabled: Multiplier x16, no target detected; PRT switches to 8 ms**

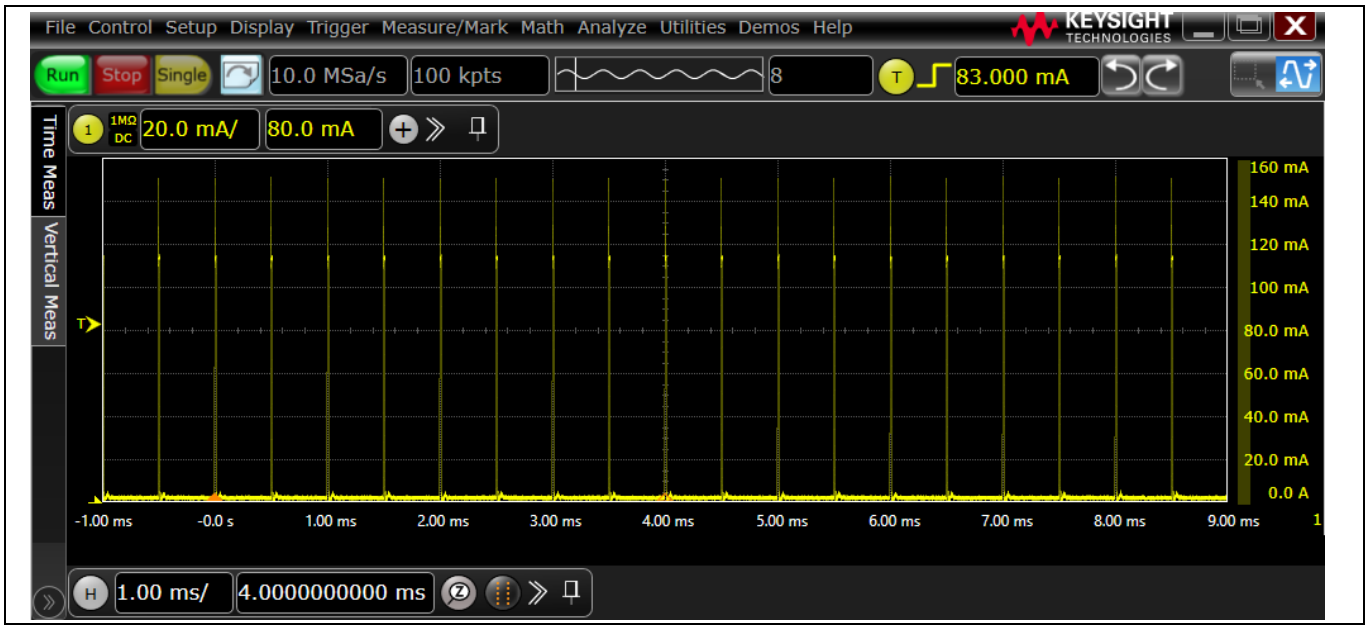


Figure 38 **APRT enabled: Multiplier x16, target detected; PRT switches back from 8 ms to 500 µs**

References

[1] Infineon Technologies AG: *BGT60LTR11AIP MMIC datasheet*; Available online

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[4] Infineon Technologies AG: *AN155336: Electronic band gap (EBG) structure for BGT60LTR11AIP application note*; Available online

Revision history

Document revision	Date	Description of changes
1.00	2023-02-14	Initial version
1.10	2024-05-20	Updated Figure 24. SPI arbitration flow diagram to fix miso_drv register number Updated Figures 15, 18, 19 with the shield v3.1 details instead of v2.0 Miscellaneous document cleanup updates
1.20	2024-10-21	Changed document ID

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