PSOC™ Control Low-voltage LLC Development Expansion Kit user guide

About this document

Scope and purpose

This document describes the hardware details of the Low-voltage LLC Development Expansion Board. It is designed to provide an evaluation platform for digital control applications using the PSOC™ Control, an Arm® Cortex®-M33 based MCU.

This board is part of Infineon's digital power evaluation platform kits.

Intended audience

This document is intended for KIT_PSC3_LLC1 users. This board is intended for use under laboratory conditions, together with the additional items listed in the Getting started section.

Safety precautions

***Note**: Please note the following warnings regarding the hazards associated with development systems.*

Table 1 Safety precautions

	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

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1 Introduction

The Low-voltage LLC Resonant Converter Development Expansion Kit provides a safe, highly integrated, and flexible platform for developing and testing digital power-conversion control using the PSOC™ Control MCU family. The expansion board features a high-frequency full-bridge LLC resonant converter with onboard analog primary and isolated secondary sensing networks, an independent auxillary supply input, and an independent hardware-driven protection system. A 120-pin connector links the board to the control card, providing access to all required analog, digital, and PWM signals for robust closed-loop software control of the Low-voltage LLC converter.

The board includes USB-UART, CAN, and mikroBUS interfaces for external communication and system expansion. It also features a network of dedicated test points to simplify waveform measurement, hardware debugging, and control-loop validation. This kit serves as an ideal hardware development accelerator for real-time digital control-loop prototyping and firmware validation using the ModusToolbox™ environment.

1.1 Key features

The Low-voltage LLC Evaluation board includes the following hardware elements and features:

- A full bridge LLC on the primary side with a center-tapped transformer with synchronous rectification
- Control Card connector for plugging the selected Control Card
- A master slave connection to allow the controllability of a second evaluation board (like a low-voltage Dual Buck board or low-voltage PFC) from the Control Card plugged into the LLC board
- Several accessible test points for measurements and detailed analysis of the LLC converter
- Multiple options for user machine interfaces:
  - General-purpose press button for user interaction
  - Multiple LEDs indicate the following:
    - Power ON condition
    - USER LED and Software FAULT to indicate control regulation and fault conditions
  - Communication ports, such as CAN interface, a dual-port serial interface, a mikroBUS header
- An independent 12 VDC auxiliary supply input to bias the IC and allow the generation of signals even without an input voltage
- Hardware protection circuits not controlled by the MCU to act as an ultimate barrier to protect the board from damage caused by incorrect PWM signal sequences

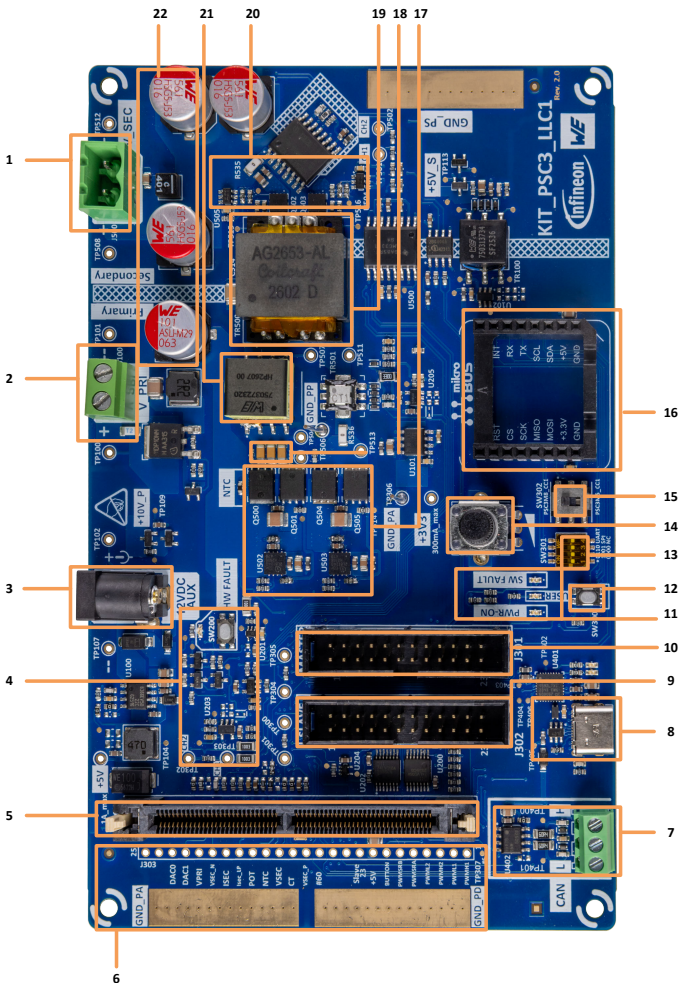
***Note**: Not all failure combinations are covered by this protection circuit.*

1.2 Kit contents

The following are the kit contents:

- Low-voltage LLC Evaluation board
- AC-DC auxiliary power adapter (230 VAC to 12 VDC)
- 24-pin ribbon cable
- QSG QR code

1 Introduction



1. J500 - DC Output connector (secondary)
2. J100 – DC Input connector (primary)
3. J102 – Auxiliary supply
4. HW Protection Logic
5. J303 – 120 pin connector for hosting KIT_PSC3xx_CC1
6. Analog and digital test point with dedicated ground planes
7. J401 – CAN communication interface
8. J400 – Dual serial port interface
9. J302 – Daisy chain slave connector
10. J301 – Daisy chain master connector
11. User LEDs
12. SW300 – Press button
13. Communication interface selection
14. Potentiometer
15. SW302 - SPI communication selection according to CC1 card.
16. mikroBUS connector
17. Primary side power stage (gate drivers + full bridge)
18. Resonant capacitors
19. Transformer (7:1)
20. Secondary side power stage (gate drivers + synchronous rectification mosfets)
21. Resonant inductor
22. Output capacitor

Figure 1 Low-voltage LLC Evaluation hardware description (1)

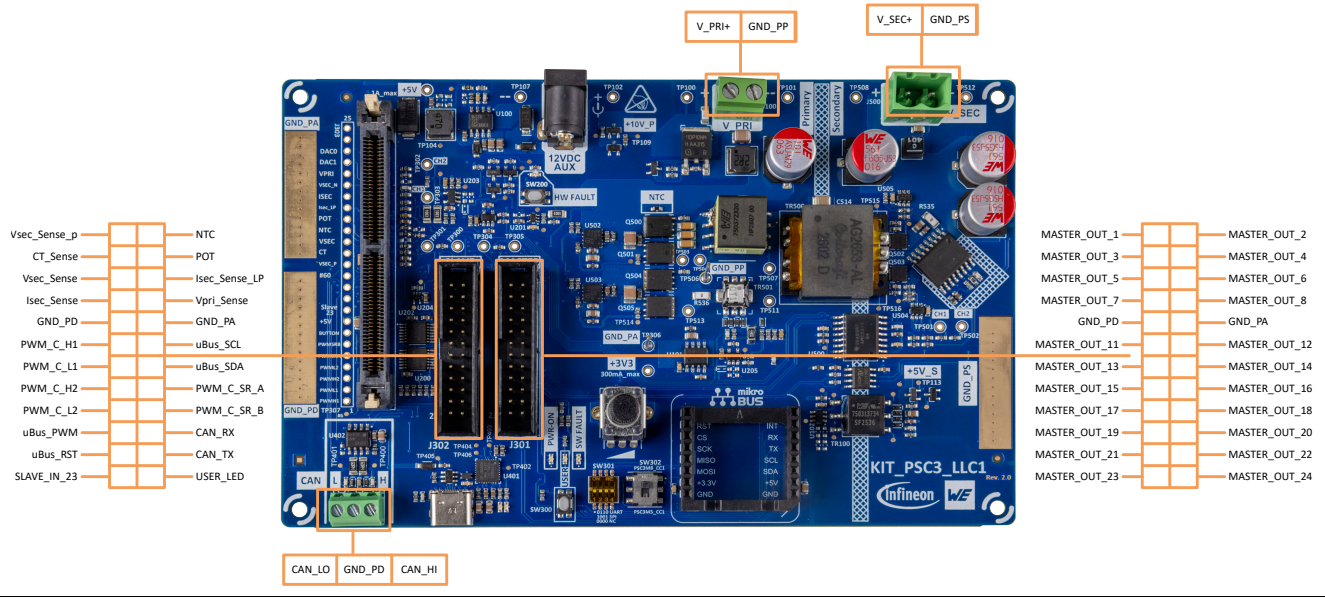


Figure 2 Low-voltage LLC Evaluation hardware description (2)

1.3 Evaluation kit setup

To operate the kit, the user must separately order additional items.

1.3.1 Minimal hardware setup (in standalone LV LLC testing)

A PSOC™ Control Card offering is described in Table 2.

Table 2 PSOC™ Control Card options

PSOC™ Control Card options		Remark
1	**KIT_PSC3M5_CC1**	Active and preferred
2	**KIT_PSC3M8_CC1**	KIT_PSC3M8_CC1 does not have supported application firmware. Such support is planned from the second half of 2026

- A **DC load** with a rating equal to or higher than the output electrical specifications listed in the Hardware specification (for example, KORAD KEL102)
- A **DC supply** with a rating equal to or higher than the output electrical specifications listed in the Hardware specification
- **Cables** to connect the output of the LLC board to the DC load

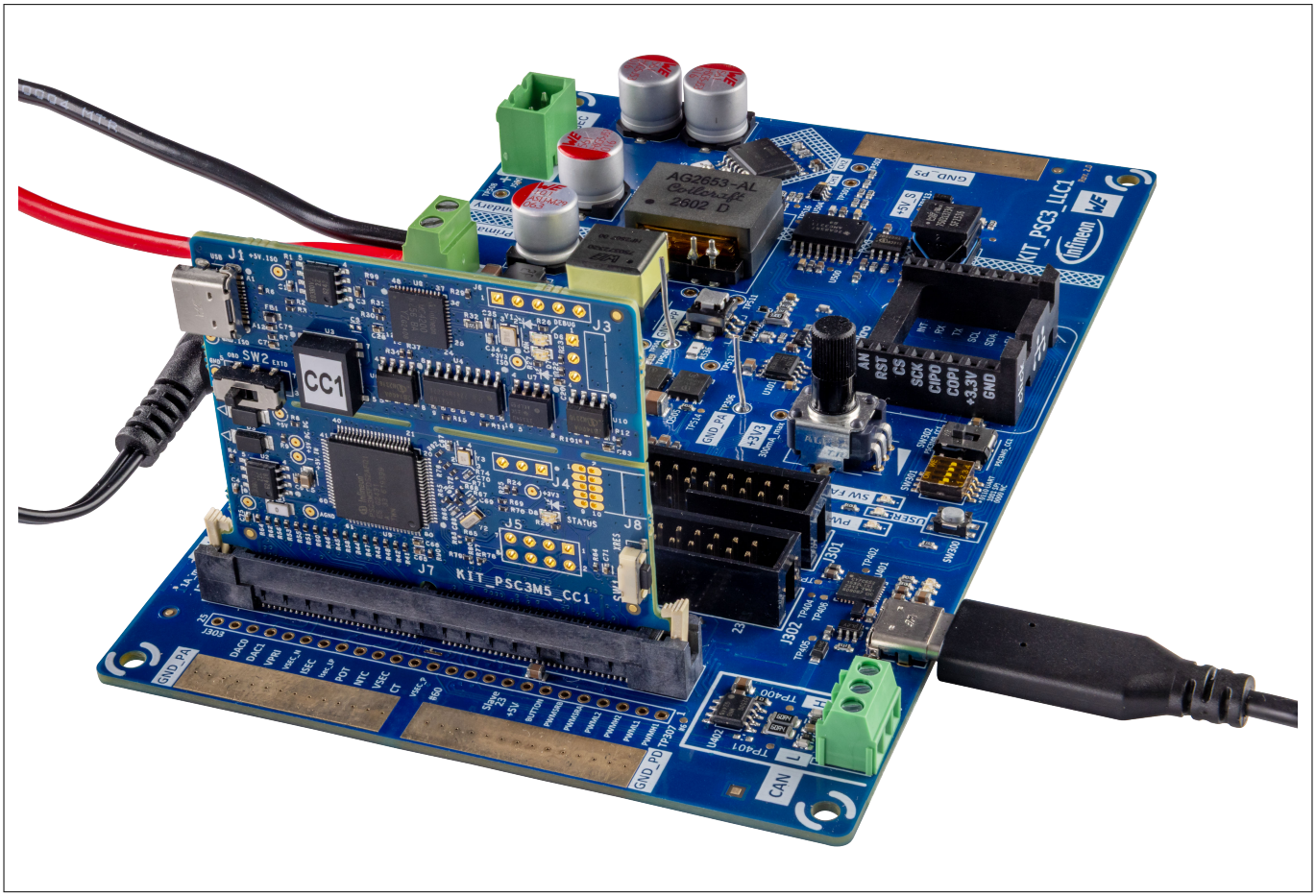


Figure 3 Overview of the minimal setup

1.3.2 Full hardware setup (in standalone LV LLC testing)

Optionally, the system functionality can be extended through a **PMBUS dongle** , such as USB0010, which enables the use of the graphical user interface available in the Power Suite package.

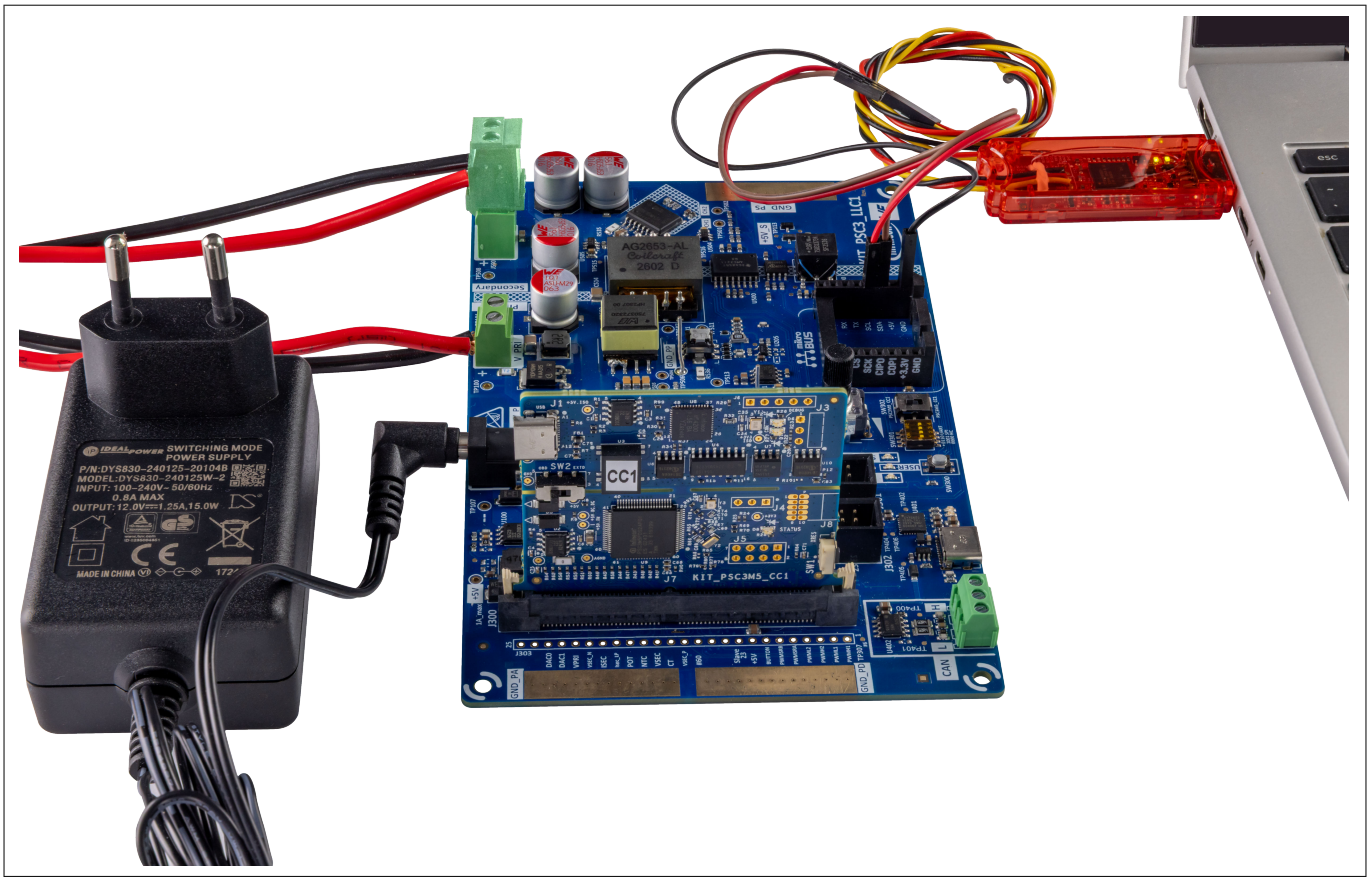


Figure 4 Overview of the full hardware setup

1.4 Hardware specification

The key specifications for the KIT_PSC3_LLC1 are described in Table 3.

Table 3 Hardware specification

Parameter	Unit	Min	Nom	Max	Remark
Input voltage	VDC	37	40	43	–
Input current	IDC	–	–	1.5	–
Output voltage	VDC	–	5	6.5	–
Output current	ADC	–	–	10	–
Output power	W	–	–	50	–
Switching frequency	kHz	350	–	1000	Expected frequency operating range

2 Kit operation

The **Low-voltage LLC Evaluation Board** is a **scaled-down** implementation of a real resonant converter, with operating parameters reduced by approximately a factor of **ten** compared to a high-voltage design.

- Its primary goal is to provide a **realistic and functional system prototype**, offering greater fidelity than a purely simulated “digital twin”. It closely resembles the high-voltage resonant architecture and behavior while operating in a **safe low-voltage environment**
- The board can be used directly **on a standard laboratory desk** without specialized high-voltage equipment
- By maintaining the input DC voltage **below 50 V**, the system remains within non-hazardous voltage levels as defined by safety standards
- The platform also provides a comprehensive environment for learning how to use the differentiating MCU peripherals of the **PSOC™ Control family** through direct interaction with a full-bridge LLC with a synchronous rectification system. In addition, system complexity can be extended by interconnecting additional expansion boards in a daisy chain configuration

2.1 Getting started

The Low-voltage LLC Development Expansion Kit shall be used with the PSOC™ Control C3M5 Digital Power Control Card, KIT_PSC3M5_CC1, which is supported by the ModusToolbox™ software.

Using ModusToolbox™ software, you can enable and configure PSOC™ Control C3M5 MCU resources and middleware libraries, develop control loop implementation code, program and debug the MCU.

A code example is available for evaluating the Low-voltage LLC Evaluation Board using the PSOC™ Control C3M5 Digital Power Control Card. This example helps users to become familiar with both the LLC Evaluation Board and PSOC™ Control C3M5 MCU and provides a foundation for developing a custom design. It can be accessed through the ModusToolbox™ new application, with the appropriate BSP selected in the tool. Alternatively, you can access it from Infineon’s code examples for ModusToolbox™ software page.

Similar support will also be extended to future products within the PSOC™ Control family.

2.2 Creating a project and program using ModusToolbox™ software

The PSOC™ Control C3M5 Control Card can be programmed and debugged using the onboard J-Link debugger. This onboard J-programmer/debugger supports USB-UART bridge functionality. An XMC4200 device is used to implement the J-Link functionality.

***Note**: To use J-Link, ensure you have downloaded and installed the latest J-Link drivers.*

The following steps briefly introduce project creation, programming, and debugging using ModusToolbox™ software. For detailed instructions, go to **Help > ModusToolbox™ General Documentation > ModusToolbox™ user guide**.

1. Keep the KIT_PSC3M5_CC1 unplugged from the KIT_PSC3_LLC1. Connect the KIT_PSC3M5_CC1 board to the PC using the provided USB cable through the J-Link USB connector, as shown in Figure 5. When connected for the first time, the board enumerates as a USB composite device.

   ***Note**: See the KIT_PSC3M5_CC1 quick start guide or User guide for more details*

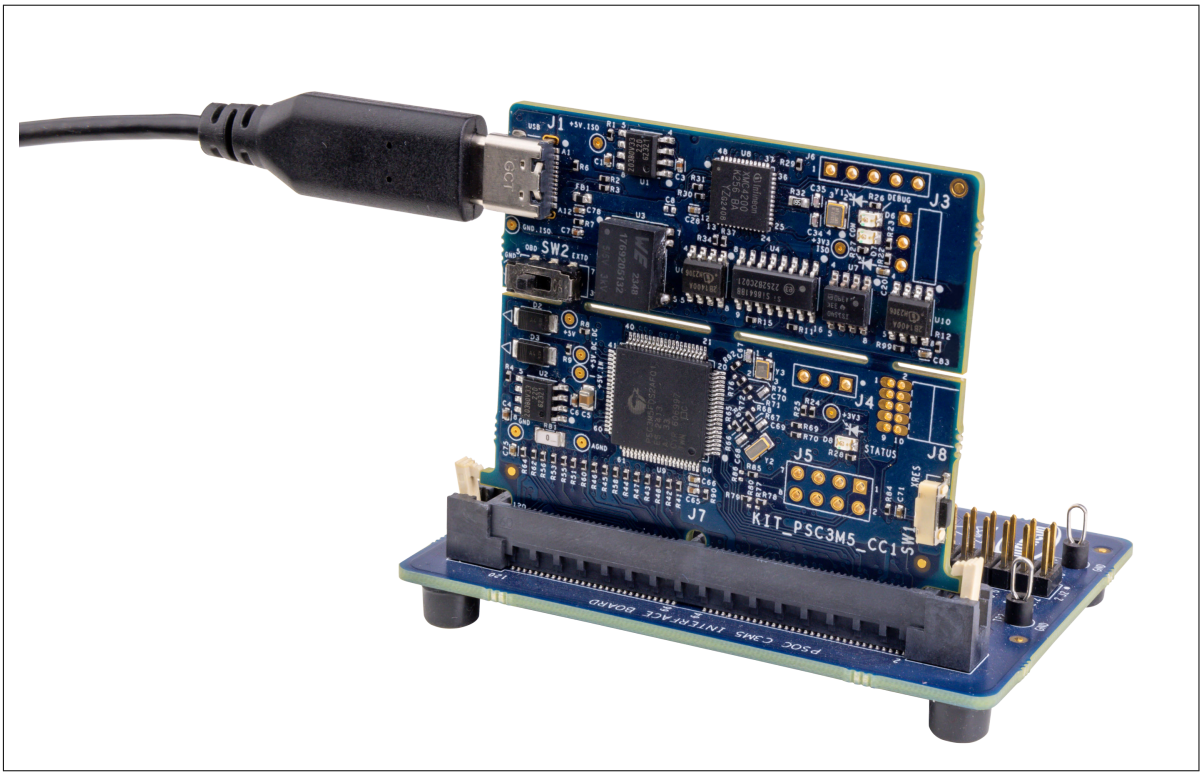


Figure 5 USB connection on CC1 card

2. The debugger on this kit is based on J-Link and one UART. The COM LED (green) is always ON if the USB is connected.

***Note**: Programming can be done either with the onboard J-Link debugger or by attaching an external debugger to the connector (J8) on the Control Card. However, it is recommended to use the onboard J-Link debugger*

3. In the Eclipse IDE within the ModusToolbox™ software, import the code example (application) into a new workspace

a. In the Quick Panel, click **New Application** from the Start section

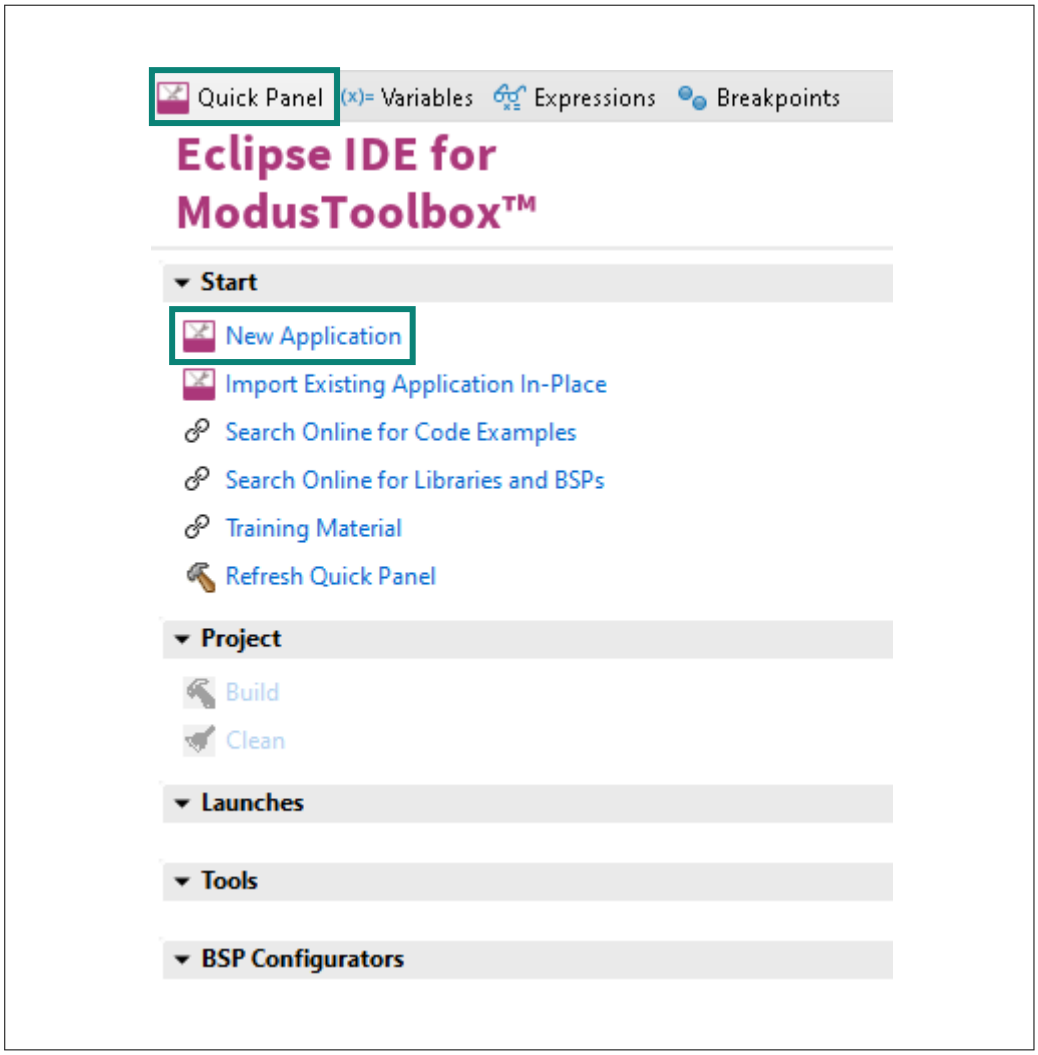


Figure 6 Create new application

b. Select the **BSP -KIT_PSC3M5_CC1** in the **Choose Board Support Package (BSP)** window and click **Next**

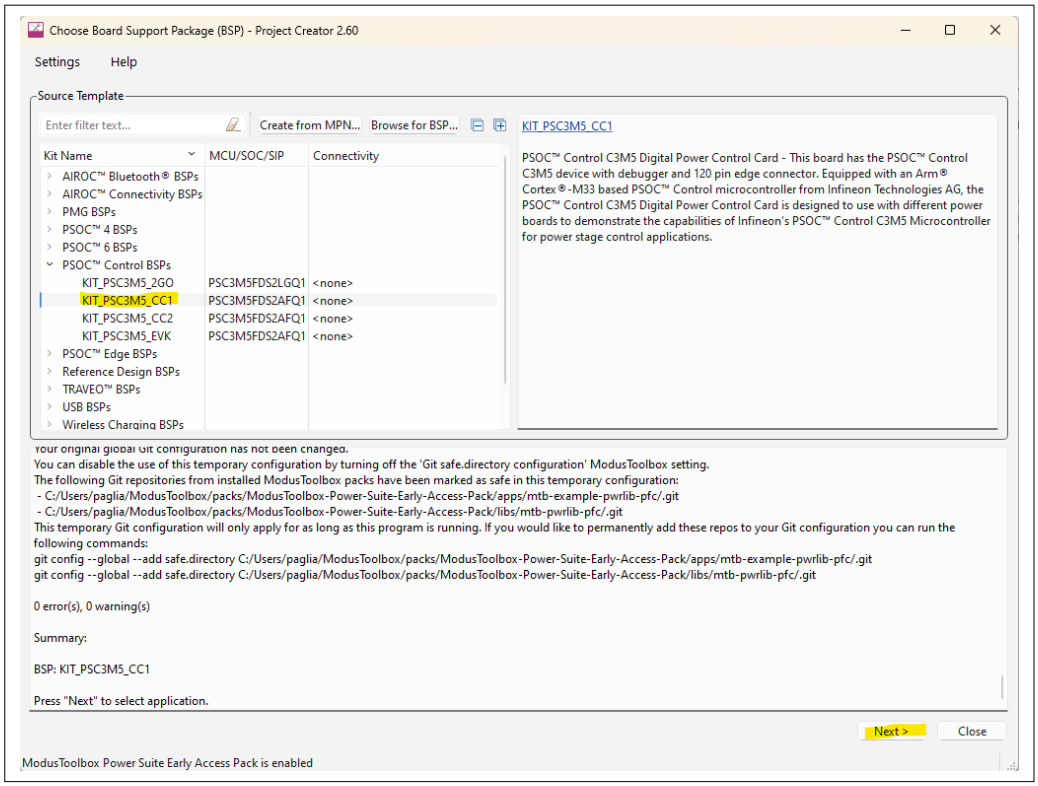


Figure 7 Choose BSP

c. Select the application in the Select Application window and click **Create**

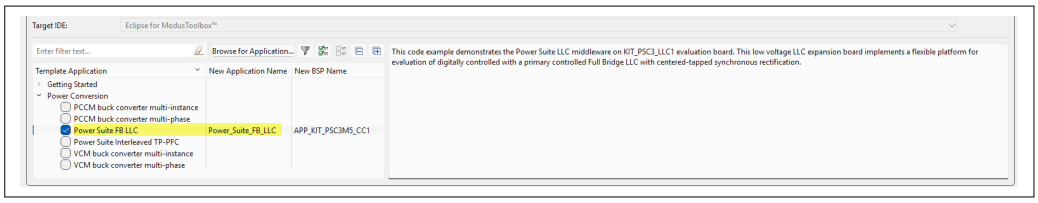


Figure 8 Select the application

4. To build and program a PSOC™ Control C3M5 MCU application, follow the steps:

a. In the **Project Explorer**, select **<App_Name>** project

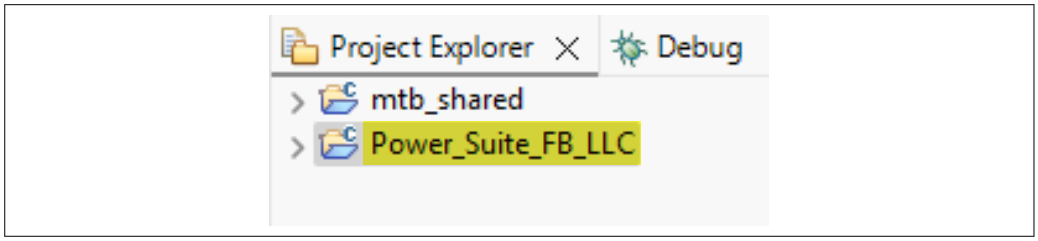


Figure 9 Programming in ModusToolbox™ Software (1)

b. In the **Quick Panel**, under the **Launches** section, click the **<App_Name> Program (J-Link)** configuration, as shown in Figure 10

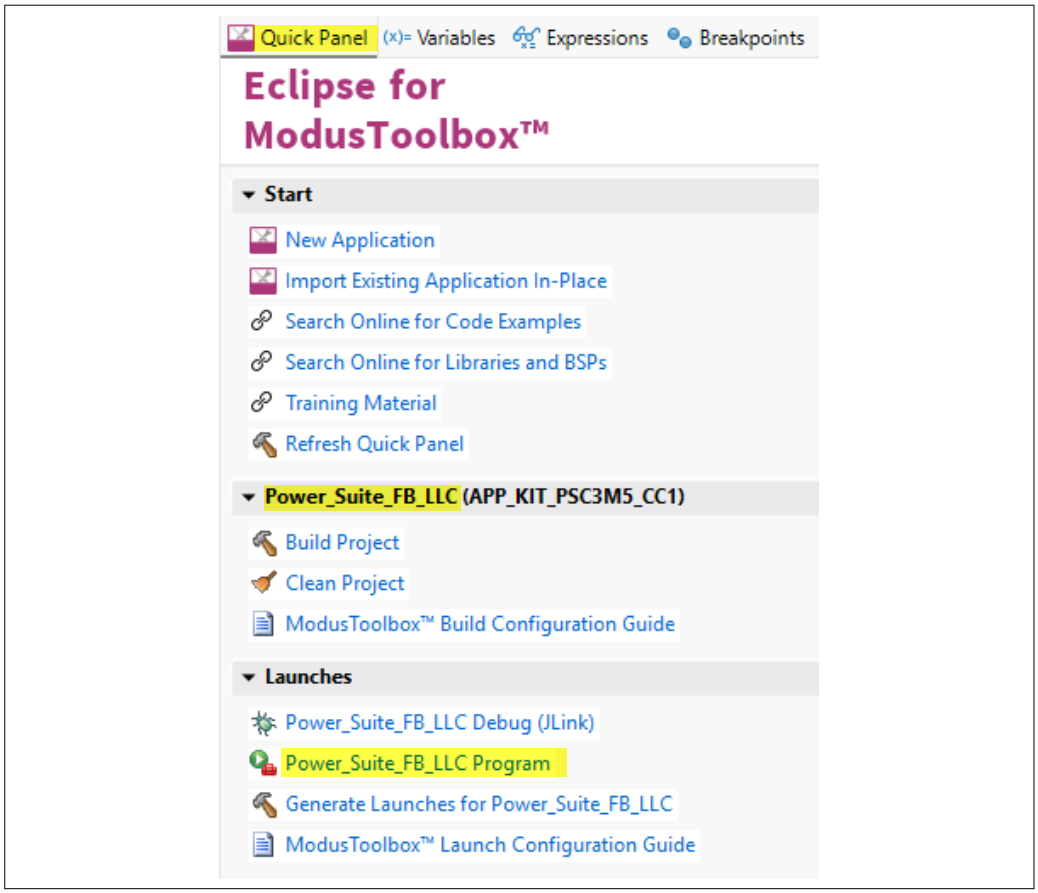


Figure 10 Programming in ModusToolbox™ software (2)

ModusToolbox™ software has an integrated debugger.

5. To debug a PSOC™ Control C3M5 MCU application, select the **<App_Name>Debug (J-Link)** configuration from the **Launches** section

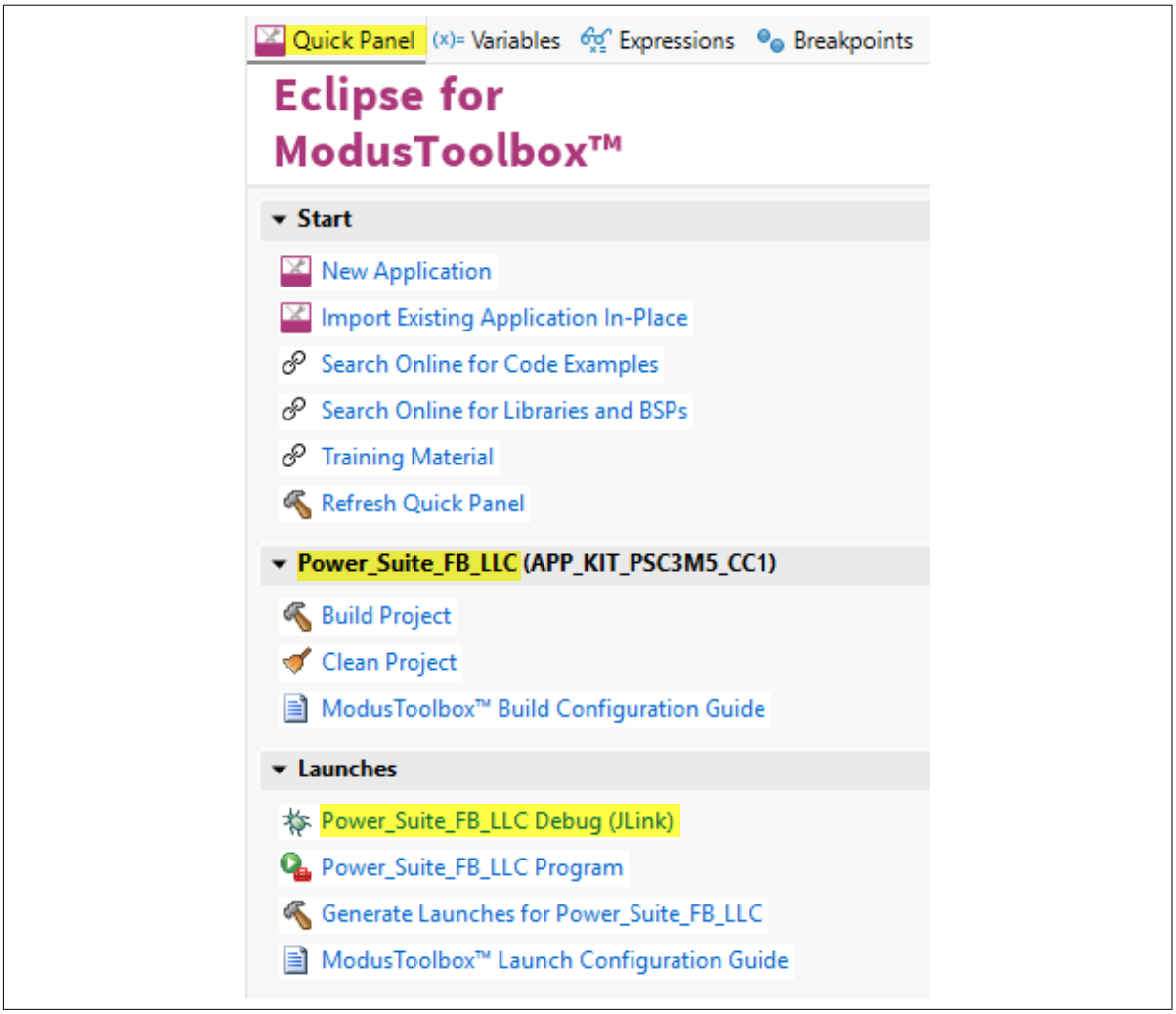


Figure 11 Debugging in ModusToolbox™ software

For more details, see the Program and debug section in the Eclipse IDE for ModusToolbox™ user guide.

3 Low-voltage LLC Evaluation Board hardware

The following section describes the hardware details of the KIT_PSC3_LLC1 Low-Voltage LLC Evaluation Board.

3.1 Block diagram

The Low-voltage (LLC) Evaluation board consists of a full bridge on the primary side and a synchronous rectification stage on the secondary side enabled through a center-tapped transformer. Primary side current is sensed with a current transformer, while secondary side current is sensed with a TLE4978 device. Primary and secondary side voltages are also sensed and routed to the 120-pin connector to complement the needed analog quantities for finalizing a software-based LLC algorithm.

The simplified block diagram is illustrated in Figure 12.

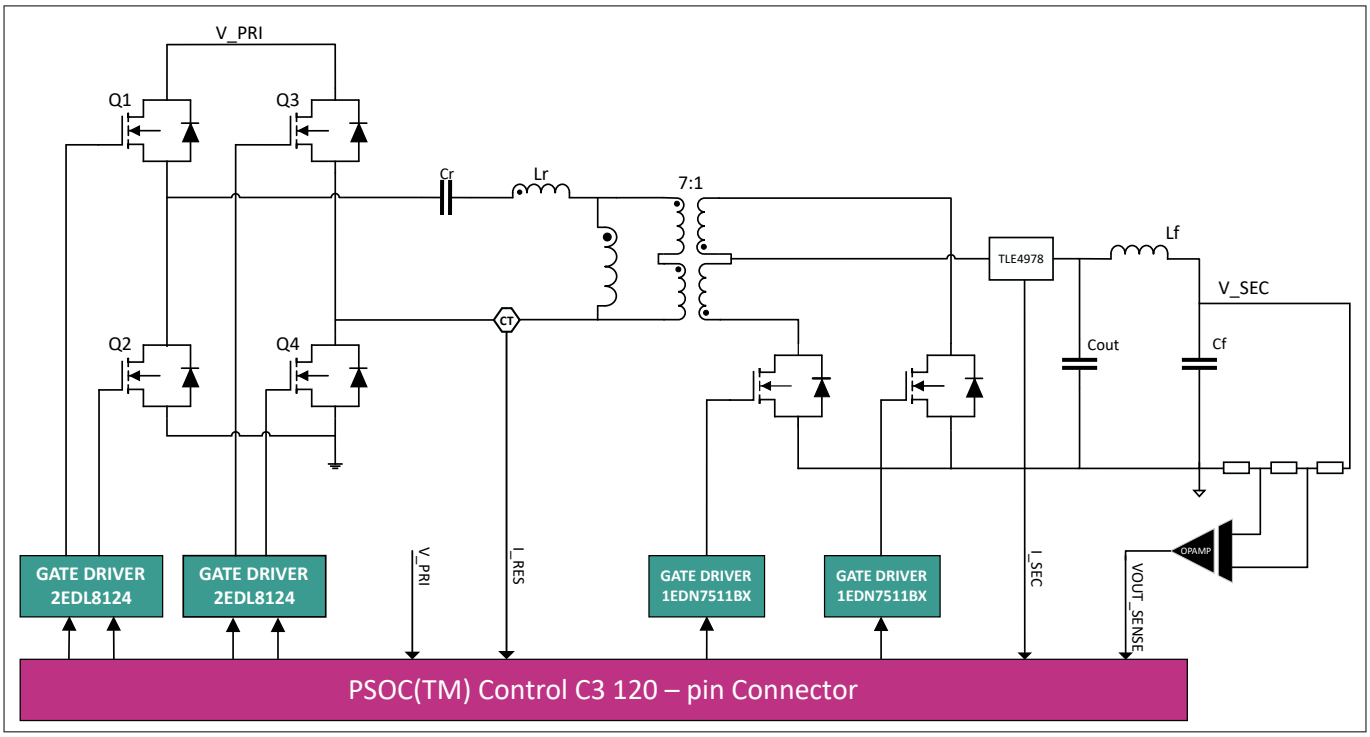


Figure 12 High-level LV (LLC) block diagram for topology and needed quantities for control development

The block diagram in Figure 13 provides a better understanding of the evaluation board sub-circuit organization.

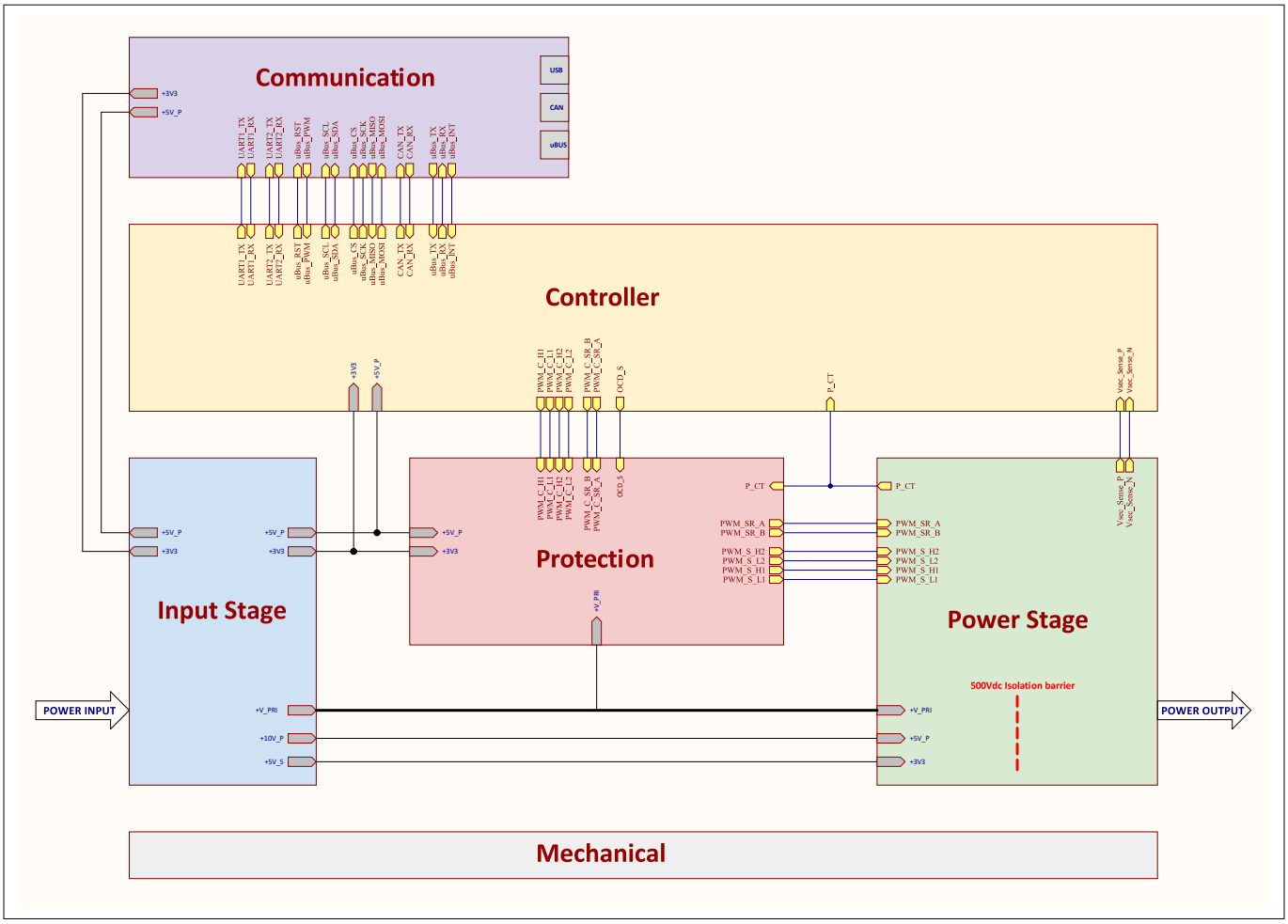


Figure 13 Functional blocks of the Low-voltage (LLC) Evaluation board hardware

The Low-voltage (LLC) Evaluation board consists of five main functional domains:

- **Input stage**: This portion deals with all voltage generation:
  - DC input
  - Auxiliary supply voltage concept for primary and secondary side
- **Protection**: This section provides an onboard active protection that operates in parallel as an ultimate safeguard to potential electrical overstress generated by improper use of PWM signals
- **Power stage**: This section describes the power stage topology, the gate driver circuitry, and sensing strategy
- **Controller**: This section covers the pin assignment with respect to the control card 120 -pin connector, additional connector pinout for daisy chain and for debugging, the signal conditioning circuits to translate what comes from the power stage to the analog inputs of the MCU, and some simple HMI (i.e., LEDs, push button, and potentiometer)
- **Communication**: This section address the different communication layers added on the board to interact with the algorithm, a dual serial port, a CAN port, and a standard mikroBUS interface for using external part click boards

3.1.1 Power flow and supply strategy

Figure 14 provides a high-level overview of the strategy taken in generating the different voltage rails to power up the system. In the next section, a more detailed description is provided.

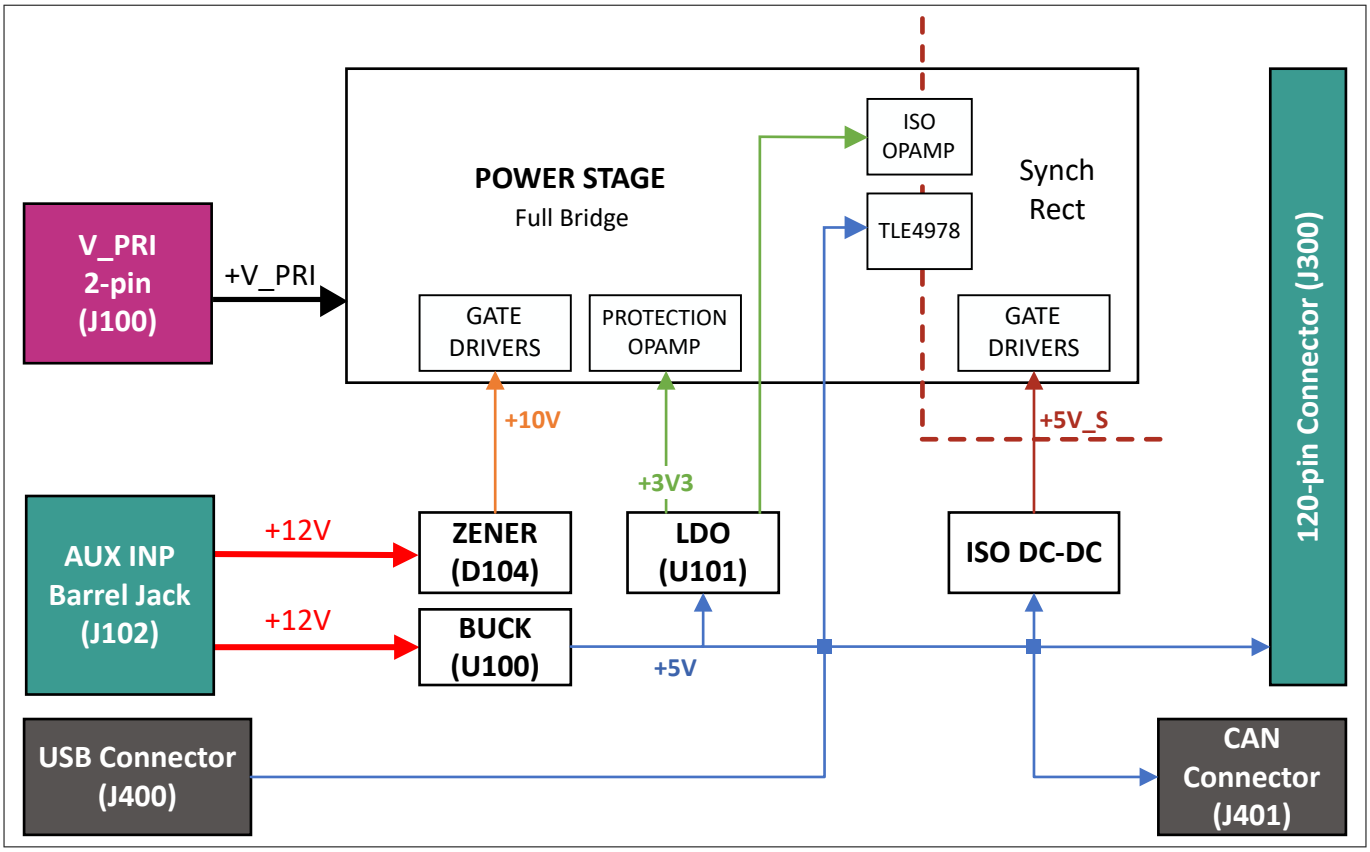


Figure 14 Power flow and supply strategy

3.1.2 Input stage

The Low-voltage (LLC) Evaluation Board is designed for safe low-voltage operation. Its main specifications are listed in Table 3. Operating the board at voltages above the rated limits will result in permanent hardware damage. When used with the LLC code example described in section Creating a project and program using ModusToolbox™ software, the default regulated output voltage depends on the position of the potentiometer, ranging from 0 V to 6 V. The maximum output power is set to 50 W when the target output voltage is 5 V. Although the sensing circuits can measure much higher currents, the output current must not exceed 10 A. To maintain a compact board size, the power stage is designed without a heatsink. Consequently, operating the board at above 10 A can cause both the primary- and secondary-side MOSFETs to reach dangerously high temperatures.

***Note**: A different output voltage can also be set by sending an appropriate PMBus command using the dongle and the GUI provided with Power Suite (full setup). See the Software manual for detailed instructions.*

Hardware limitations: Independent hardware protection is implemented and will be triggered if the input voltage exceeds 48 V, or if the resonant current exceeds ~8.5 A or if the secondary current exceeds 64 A.

The LLC application has the advantage that when switches are not operated, the output voltage remains LOW; it is inherently safe.

A schematic view of the input stage is shown in Figure 15.

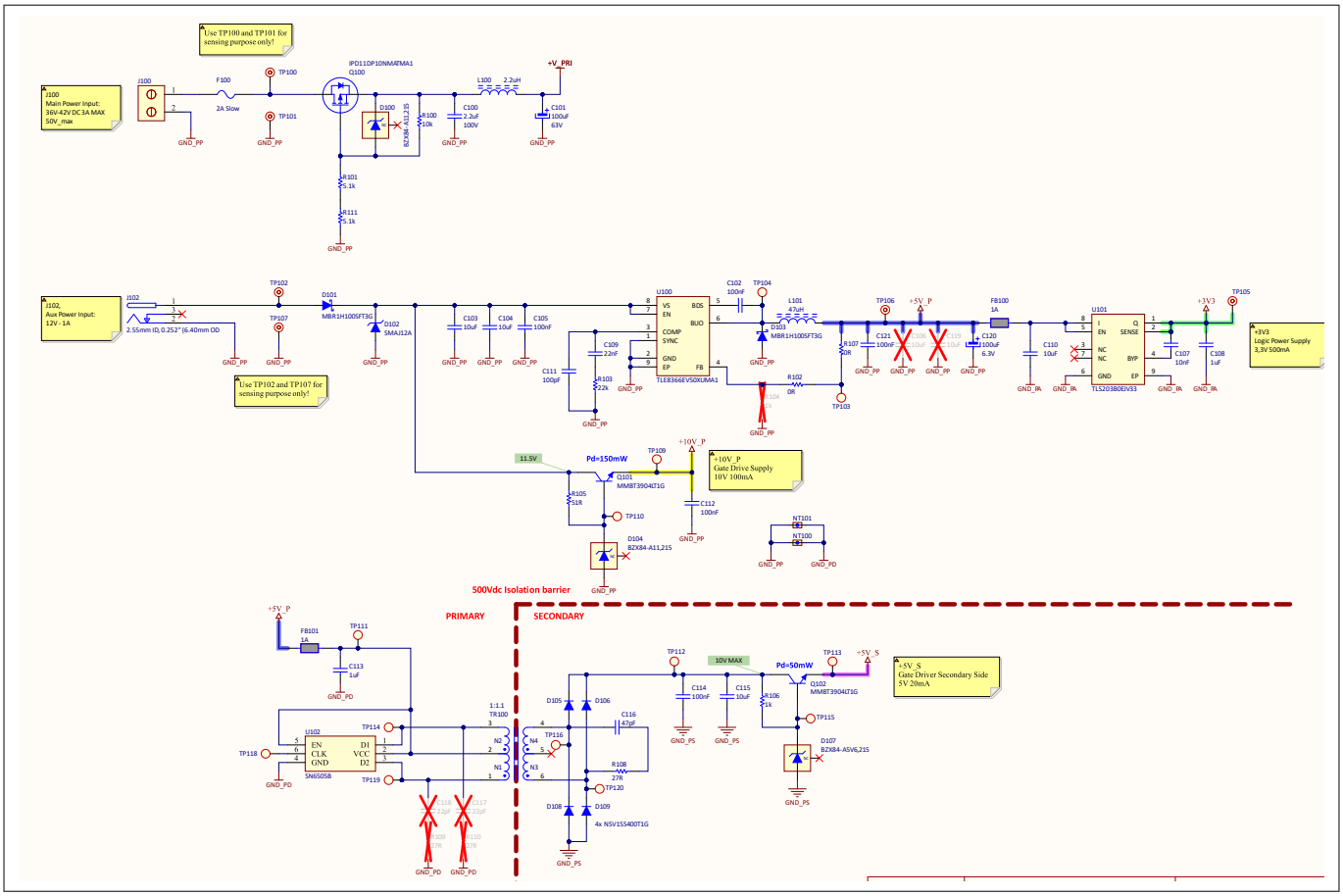


Figure 15 Input stage overview

The input stage manages the main DC power distribution and system biasing. It routes the primary DC input directly to the power stage switches while stepping down the incoming auxiliary voltage to generate the internal auxiliary rails. Specifically, it provides regulated 3.3 V, 5 V, and 10 V supplies to power the primary logic, protection circuits, and gate drivers across the board. The internal 5 V and 3.3 V rail are generated by a buck converter U100 (TLE8366EV50) and a linear regulator U101 (TLS203B0EJ V33) respectively. Additionally, input protection in the main power path is implemented by a 2 A surface-mount fuse (F100), a transient voltage suppression diode (D100), and bulk decoupling capacitors (C100, C101).

For gate drive biasing, the primary-side +10V_P supply is generated using a discrete linear regulator composed of pass transistor Q101 (MMBT3904LT1G) and zener diode D104 (BZX84-A11,215). To supply the isolated secondary side across the 500 V DC isolation barrier, a push-pull transformer driver, U102 (SN6505B), drives the primary side of a 1:1.1 pulse transformer (TR100). The secondary outputs of the transformer are rectified using a full-bridge diode array (D105–D109, NSVR05400T1G) and then regulated to an isolated +5 V_S supply by a secondary linear regulator stage consisting of transistor Q102 and zener diode D107 (BZX84-A5V6,215).

Two input connectors are available: **J100** and **J102**.

- **J100 is a DC input connection (green)**: Use a DC programmable power supply capable of delivering more than the rated output power.
- **J102 is the auxiliary supply connection (black)** : Connect the auxiliary power supply provided in the kit.

The test points **TP100, TP101,TP102**, and **TP107** are provided next to the input connectors for voltage sensing only. They must not be used as current supply terminals. When monitoring the DC input with an oscilloscope, the user can select either a differential probe or a single-ended probe depending on the measurement setup and whether the secondary-side voltage is being evaluated.

3.1.3 Power stage

The schematic view of the power stage is shown in Figure 16.

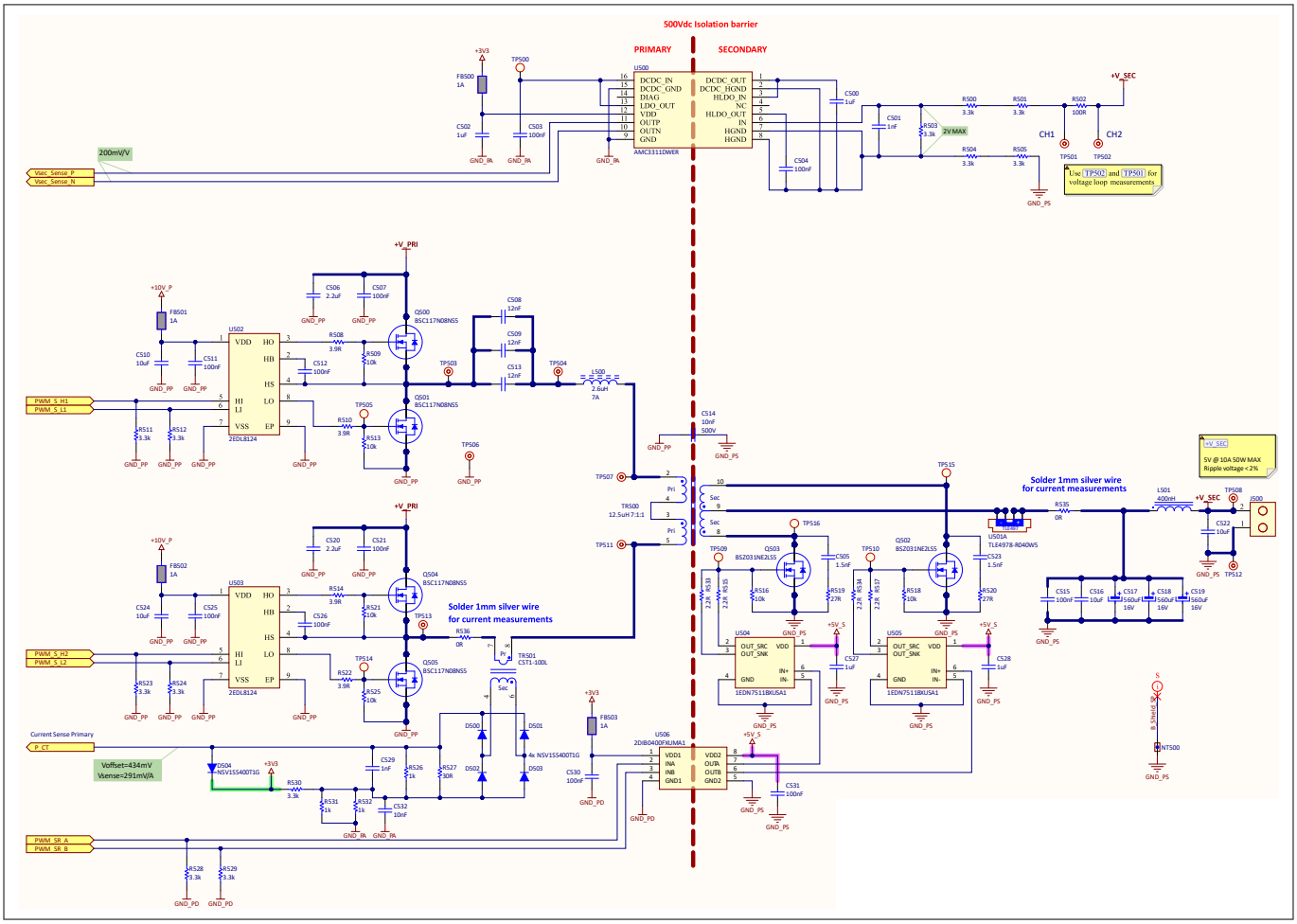


Figure 16 Power stage

The power stage performs the core DC-DC power conversion using a high-efficiency **Full-Bridge LLC resonant converter** topology with secondary-side synchronous rectification. A strict galvanic isolation barrier divides the primary-side high-voltage circuits from the secondary-side low-voltage output.

At the central to this stage is the high-frequency planar isolation transformer **TR500** (Coilcraft part number: AG2653-AL), which serves three key functions:

1. **Galvanic isolation**: Provides the required safety barrier separating the primary high-voltage domain from the secondary low-voltage output
2. **Voltage scaling (turns ratio)**: The transformer implements a precise primary-to-center-tapped-secondary turns ratio of (7:1:1) to step down the nominal primary DC link down to the target level for active rectification
3. **Resonant tank integration**: The transformer is wound with a controlled primary magnetizing inductance 12.5 µH. This integrated magnetizing inductance interacts directly with the external resonant inductor L500 (2.6 µH) and the parallel resonant capacitors C508, C509, and C513 (36 nF total) to form the LLC resonant tank network

Primary full-bridge resonant circuit

The primary side uses a full-bridge switching topology to convert the incoming primary DC input (+V_PRI) into a high-frequency AC wave that excites the LLC resonant tank

Key components are as follows:

- **Full-bridge inverter:** Four high-performance low $R_{ds(ON)}$ N-channel MOSFETs **OptiMOS™ 5** (BSC117N08NS5), where Q500 and Q501 comprise the first switching leg, and Q504 and Q505 comprise the second leg
- **LLC resonant tank:** Consists of a 2.6 µH series resonant inductor (L500) and a parallel capacitor bank containing three 12 nF capacitors (C508, C509, C513)
- **Resonant parameters:** The parallel capacitor configuration establishes a total resonant capacitance **Cr** of 36 nF, yielding a hardware resonant frequency **fr** of approximately 520 kHz
- **Gate driver ICs:** Two dual-channel gate driver (2EDL8124) ICs (U502 and U503) drive the inverter legs
- **Logic input interface:** The drivers receive high-side and low-side logic commands (PWM_S_H1/L1 and PWM_S_H2/L2) referenced to logic ground via 3.3 kΩ pull-down resistors (R511, R512, R523, R524).
- **Gate resistor networks:** Series 3.9 Ω resistors (R508, R510, R514, R522) control the switching *dV/dt*, while 10 kΩ gate-to-source resistors stabilize the MOSFETs during startup.
- **Driver power and biasing:** The ICs are powered from the +10V_P rail filtered through ferrite beads (FB501, FB502) and utilize external bootstrap capacitors (C512, C526) to bias the floating high-side gate outputs (HO)
- **Test points:** Dedicated evaluation points are provided to capture critical converter dynamics. These allow users to safely monitor the main switching nodes (TP503, TP513), the high-frequency resonant tank capacitor voltage (TP503, TP504), observe that the transformer primary winding voltage (TP507, TP511), and analyze the resonant inductor voltage (TP505, TP507) alongside the gate driver output (TP514)

Attention**: **It is strongly recommended to use high-bandwidth differential probes when monitoring these nodes to avoid introducing parasitic ground loops or corrupting high-frequency switching waveforms.

Secondary synchronous rectification (SR) stage

The secondary-side of the power stage actively rectifies the high-frequency AC output from the center-tapped isolation transformer **TR500** to deliver a stable DC voltage.

The key components are as follows:

- **Synchronous rectifier:** Two low $R_{ds(ON)}$ N-channel power MOSFETs Q502 and Q503, (**BSZ031NE2LS5**), operating as an efficient active center-tapped rectification network
- **Galvanic isolation boundary:** A dual-channel digital isolator U506 (2D1B040FXUMA1) safely transfers the high-speed logic control signals (**PWM_SR_A** and **PWM_SR_B**) across the primary-to-secondary ground boundary (GND_PD to GND_PS)
- **Gate driver ICs:** Two independent 1EDN7511BXUSA1 low-side gate drivers (U504, U505) command the synchronous switches and are biased locally by the isolated +5V_S rail and a 1 µF capacitor (C527, C528)
- **Gate turn-on/off optimization:** Split gate paths use 2.2 Ω resistors for managed turn-on (R515, R517) and fast turn-off (R533, R534), paired with 10 kΩ gate-to-source stabilization resistors (R516, R518)
- **Snubber networks:** Parallel RC snubber circuits consisting of 27 Ω resistors (R519, R520) and 1.5 nF high-voltage ceramic capacitors (C505, C523) damp high-frequency voltage spikes across the SR MOSFETs
- **Current measurement:** Current sensor U501A (TLE4978R040W5) is used for precise output current measurements
- **Output filtering:** The output stage features a multi-stage parallel capacitor bank comprising low-ESR ceramic decoupling capacitors (C515, C516, CS22) and bulk storage electrolytic capacitors (C517, C518, C519) to minimize voltage ripple. A 400 nH power inductor (L501) provides final high-frequency filtering before delivering a stable output

- **Output terminal:** Connector (J500) is provided to connect the output load. Use a resistive load (rheostat) or a DC electronic load (for example, KORAD KEL102)
- **Test points:** Dedicated evaluation points are provided to allow monitoring of the isolated auxiliary rail (TP511 for +5V_S), to verify the synchronous gate drive waveforms (TP509 and TP510), to check the transformer secondary voltage and the switch nodes (TP515, TP516 and TP508) and to measure the filtered DC output voltage profile (TP508, TP512)

3.1.4 Analog sensing and hardware protection

***Note**: Since this kit supports multiple CC1 control cards, verify that the required anti-aliasing capacitor is present on the analog connection to the MCU pin of the selected CC1 card. For the **KIT_PSC3M5_CC1**, **100 pF** capacitor **(C39, C40, C41 and C42)** shall be soldered from the analog pins and digital ground if they are not already installed. Additionally, the anti-aliasing filter value may be adjusted, if required, to match the specific signal bandwidth of the application.*

Primary current sensing (P_CT)

The hardware design for primary current sensing is shown in Figure 17.

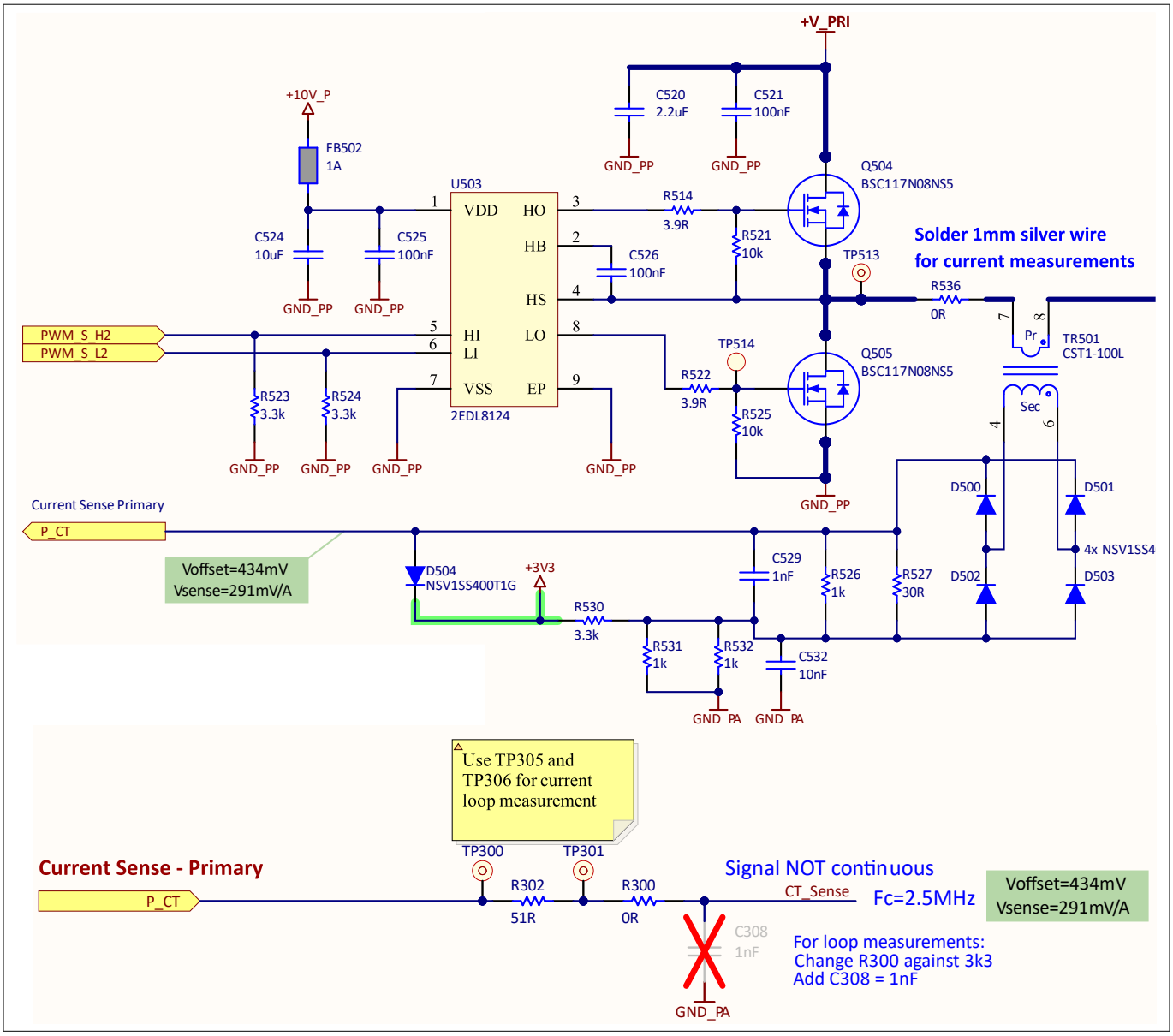


Figure 17 Primary current sensing (P_CT)

The high-frequency AC current flowing through the primary LLC resonant tank is monitored via a **1:100 Coilcraft CST1-100L current sense transformer (TR501)**. The transformer secondary AC output current is rectified into a pulsed DC waveform voltage using a high-speed full-bridge diode array (D500–D503, NSV1SS400T1G). A load resistor (R527) converts the current into a readable voltage signal. To ensure that zero-crossing current transitions do not clip negatively and can be cleanly processed within the controller's single-ended 3.3 V ADC dynamic range, a DC bias of 434 mV is injected via a resistor divider network formed by R530 and a parallel combination of R531 and R532. Combining this offset with the burden scaling yields a net output sensitivity of exactly **291 mV/A** with a high-bandwidth low-pass filter cutoff frequency **(2.5 MHz)**.

For advanced frequency response loop testing and stability analysis, dedicated test points (TP300, TP301) are placed in line with the signal path. Performing open-loop frequency response measurements requires on-board hardware modification: the default 0 Ω link resistor **R300** must be replaced with a 3.3kΩ resistor, and a 1 nF filter capacitor (C308) must be populated to form a stable injection node.

Primary DC input voltage sensing (Vpri_Sense)

The DC bus voltage (+V_PRI) is continuously monitored using a high-impedance voltage divider network and an integrated low-pass filter stage. Figure 18 represents the hardware implementation. The resistive divider is formed by a series path consisting of R303 (100 Ω), R304 (100 kΩ), and two series ground-return resistors, R305

(3.3 kΩ) and R306 (3.3 kΩ). This network drops the high-voltage input rail down to a safe, microcontroller-compatible analog range, yielding a net attenuation sensitivity of exactly 62mV/V.

To suppress high-frequency switching noise and voltage transients in the measurement path, an inline filtering capacitor C301 (10 nF) is connected in parallel, clamping the loop's corner frequency to a stable 2 kHz. Figure 18 shows the hardware design for primary DC input voltage sensing (Vpri_Sense).

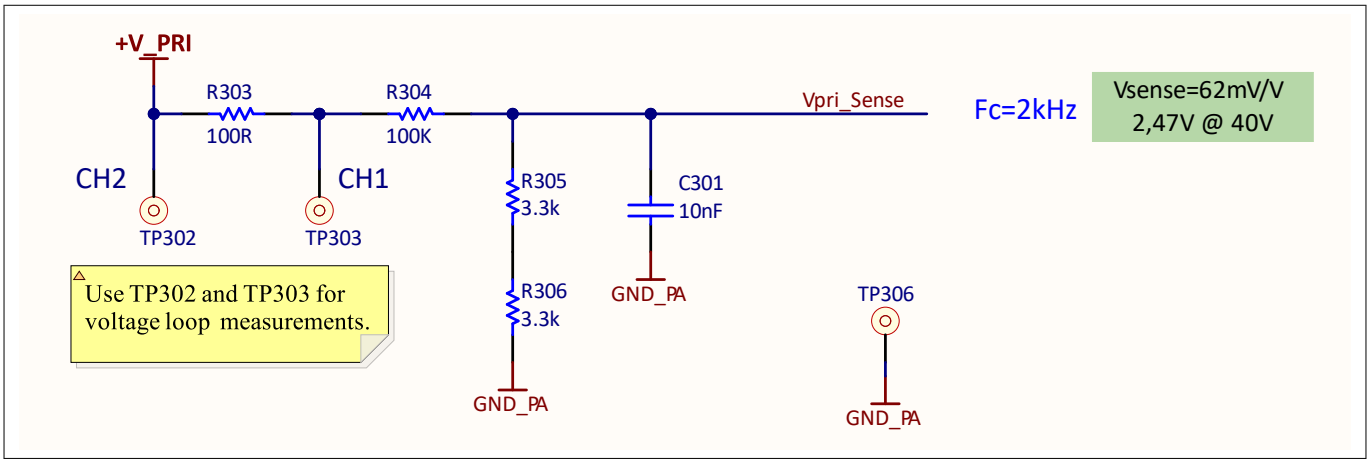


Figure 18 Primary DC input voltage sensing (Vpri_Sense)

For control loop stability verification and input voltage-loop calibrations, dedicated diagnostic evaluation points TP302 (CH2) and TP303 (CH1) are placed at the front edge of the sensing array. These test points provide a clean, non-invasive injection node for frequency response analysers to perform voltage loop response measurements without requiring trace slicing.

Secondary output current sensing (Isec_Sense)

Figure 19 shows the hardware design for secondary output current sensing (Isec_Sense)

The secondary-side output current is monitored using a high-speed coreless Hall-effect current sensor **U501 (TLE4978-R040W5)** powered by the +5V_P rail and filtered through a 1A ferrite bead (FB300). Because the sensor operates on a 5 V rail but interfaces with a 3.3 V microcontroller ADC, the raw analog output voltage from AOUT (pin 13) is scaled down through an onboard voltage divider network formed by R301 (261 Ω), R323 (1 kΩ), and R324 (1 kΩ). This resistive attenuation implements a 0.66 scaling factor (1.65 V/2.5 V), shifting the native (2.5 V) zero-current offset down to a controller-compatible (1.65 V) and setting the net output sensitivity to exactly **32 mV/A**. The overcurrent detection threshold (OCD_THR, pin 15) is locked at a stable reference voltage of **1.24 V** via a parallel R322 (3.3 kΩ) and C311 (1 nF) filter combination to govern hardware fault tripping. This corresponds to an OCD threshold of 64 A peak.

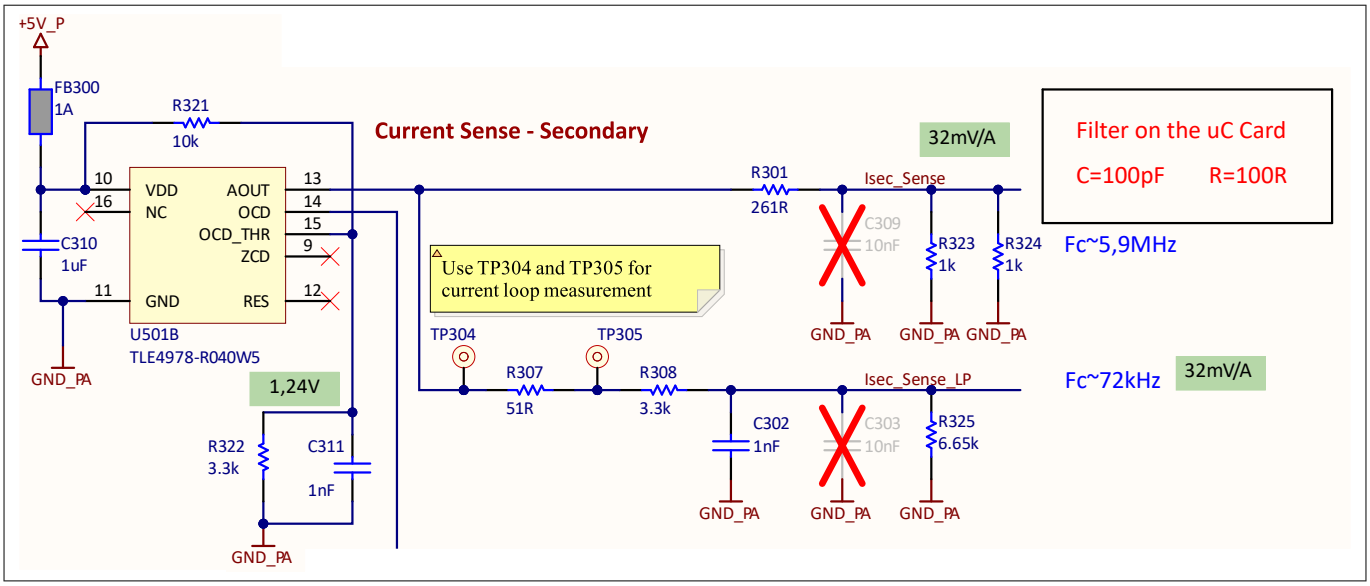


Figure 19 Secondary output current sensing (Isec_Sense)

The conditioned sensor output splits into two distinct diagnostic paths, each optimized for telemetry and filtering:

- **High-speed path (Isec_Sense):** Routed directly to the microcontroller card through a localized high-bandwidth RC low-pass filter (R = 100 Ω, C = 100 pF), establishing a transient corner frequency of approximately 5.9 MHz
- **Low-frequency path (Isec_Sense_LP):** Routed through an additional inline low-pass smoothing stage composed of R307 (51 Ω), R308 (3.3k Ω), C302 (1 nF), and a pull-down termination resistor R325 (6.65 kΩ). This stage provides a filtered average telemetry line with a corner frequency (Fc) of approximately **72 kHz**. Note that capacitors (C309, C303) are unpopulated placeholders by default

For frequency response analysis and stability evaluation of the secondary current feedback loop, dedicated instrumentation test points (TP304, TP305) are provided inline at the output of the sensor's main conditioning node.

Secondary output voltage sensing (Vsec_Sense)

The secondary DC output voltage (+V_SEC) is monitored across the galvanic isolation barrier using an **AMC3311DWER precision isolated amplifier (U500)**, paired with an **AZV831KTR-G1 operational amplifier (U300)** difference stage. This setup provides low-latency analog feedback to the primary-side controller. Figure 20 shows the hardware design for secondary output voltage sensing (Vsec_Sense).

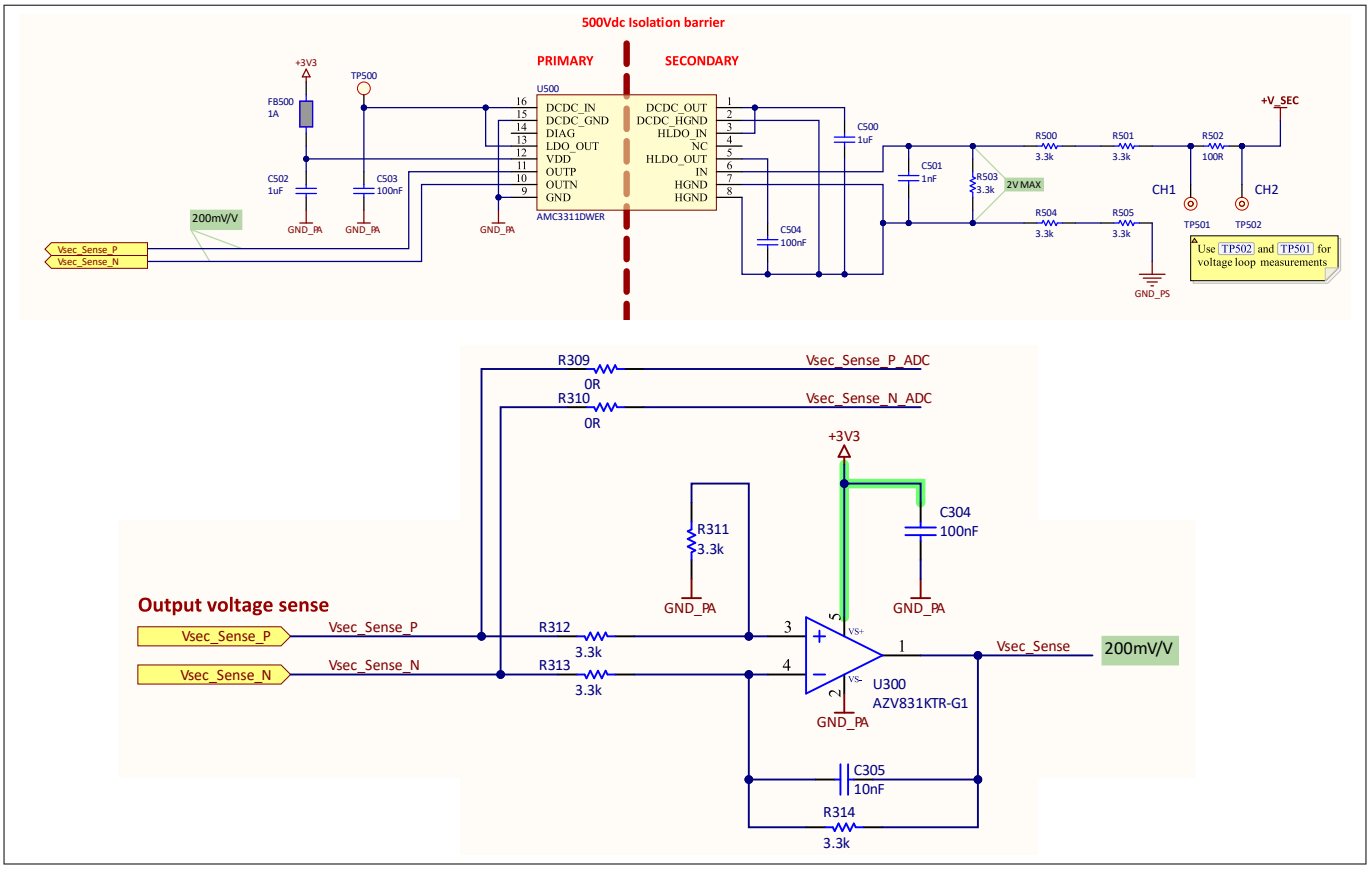


Figure 20 Secondary output voltage sensing (Vsec_Sense)

The key components are as follows:

- **Galvanic isolation barrier:** The precision isolated amplifier (U500) safely spans a **500 VDC isolation boundary**, separating the secondary ground domain (GND_PS) from the primary ground domain (GND_PA)
- **Secondary scaling:** A high-impedance (high-Z) resistive divider (R500–R504) on the secondary-side steps down the output rail to match the precise 1 V maximum linear input range of U500
- **Differential dual routing:** The isolated differential signals (Vsec_Sense_P/N) cross to the primary side and split. They can be routed directly to the MCU ADC pins via zero-ohm links (R309, R310) as Vsec_Sense_P_ADC and Vsec_Sense_N_ADC
- **Single-ended reconstruction:** Concurrently, the differential tracks feed the U300 op-amp stage. Configured as a difference amplifier with symmetrical 3.3 kΩ networks (R311–R314) and a 10 nF filter capacitor (C305), it generates a clean single-ended analog loop line (Vsec_Sense) with a net attenuation gain of exactly **200 mV/V**

Temperature sensing

A negative thermocouple (NTC) is added to the circuit and located between the output capacitor and the phase 1 half bridge. The operation of the NTC is simple: as the temperature increases, the resistance of the sensing element decreases, and the resulting input voltage to the MCU pin decreases.

Figure 21 shows the implementation of the circuit. The nominal resistance at 25°C is 10 kΩ.

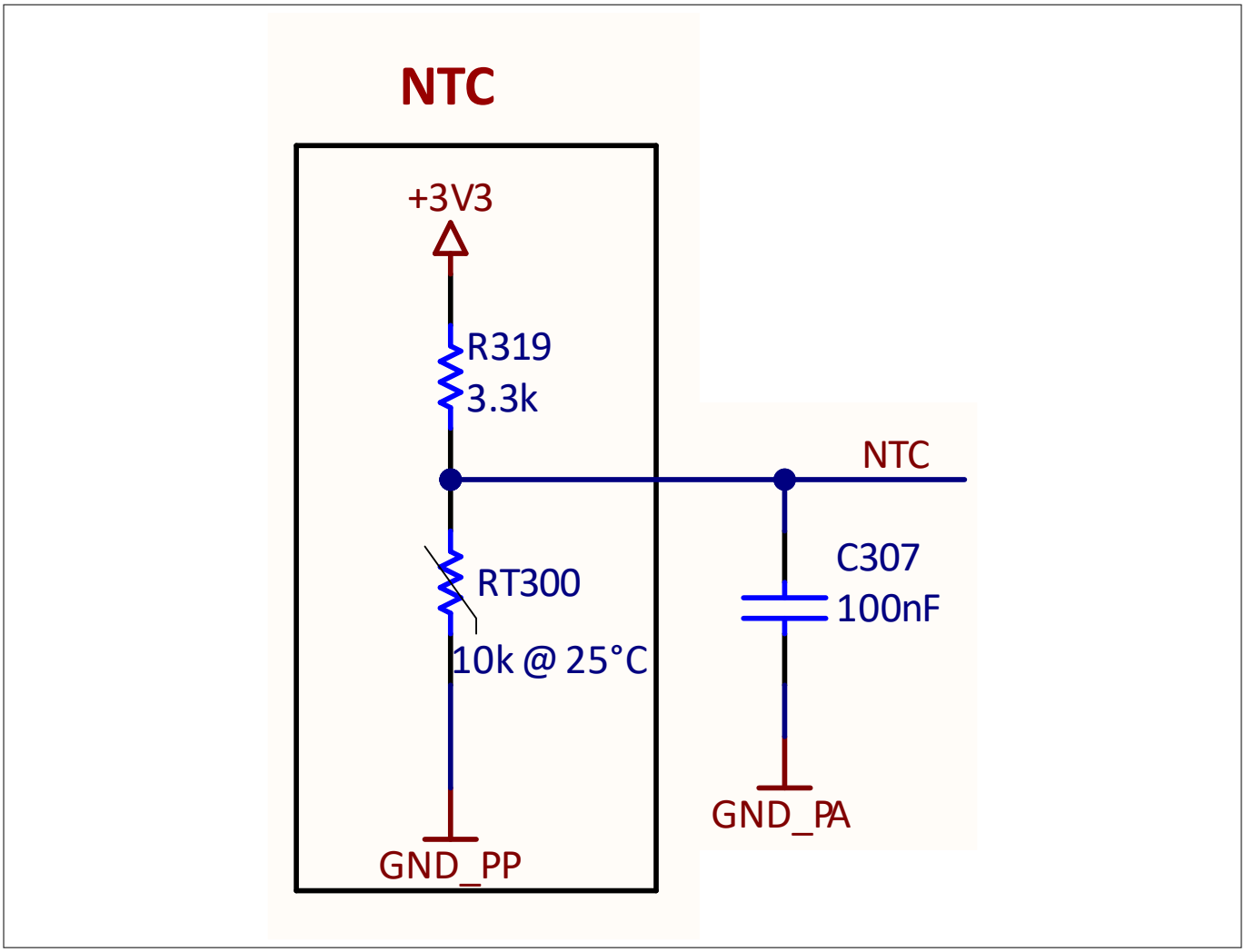


Figure 21 **Temperature sensor circuit**

Table 4 **Analog sensing gain**

Parameter	Transducer	Voltage offset	Gain	Test point	Expected input values		
					Min	Nominal	Max
Primary current sensing (**P_CT**)	Current transformer	434 mV	291 mV/A	J302.3, TP300, TP301	0	–	11 A
DC voltage sensing (**Vpri_Sense**)	Resistor divider	0 V	62 mV/V	J302.1	0 V	40 V	53.2 V
Secondary current sense (**Isec_Sense**)	TLE4973-R040W5	1.65 V	32 mV/A	J302.7, J302.6, TP304, TP305	0 V	10 A	51.56 A
Secondary voltage sensing (**Vsec_Sense**)	AZV831KTR-G1	1.65 V	200 mV/V	J302.5, J500(OUT), TP 306	0 V	–	6.5 V
Temperature sense	–	0 V	–	J303.18	–	2.48 V @ 25°C	0.2 V @ 120°C
Potentiometer (HMI)	–	0 V	Volt divider type	J303.17	0 V	1.65 V @ default	3.3 V

3.1.5 Hardware protection circuit

The board is equipped with an onboard hardware protection circuit that operates independently from the microcontroller unit (MCU). Its primary purpose is to provide a low-latency safety barrier that prevents permanent hardware damage if an incorrect or corrupted PWM switching sequence is generated due to firmware malfunctions or configuration errors.

Protection Functions

Three primary analog protection functions are implemented on the board to guard against voltage and current stress:

- **Primary overvoltage protection (OVP):** An analog comparator (U203, NCS2252) continuously monitors the main primary-side high-voltage DC link (+V_PRI). The bus voltage is stepped down through a resistive divider network (R208, R211 and R215) and compared against a fixed reference threshold of 3 V. The hardware is configured with an OVP threshold at exactly **48 V**. When the bus primary voltage violates this limit, the comparator output transitions LOW and instantly latches a fault condition into the hardware circuit
- **Primary resonant tank overcurrent detection (P_CT):** High-frequency primary tank current spikes are caught using the dedicated primary current transformer feedback line (P_CT). This signal feeds an ultra-fast analog comparator stage (U205, NCS2252) that triggers a low-latency shutdown if PT_CT exceeds 3 V, corresponding to a primary peak current of 8.6 A
- **Secondary output overcurrent detection (OCD_S):** The output current loop is monitored via the OCD_S input, which observes the secondary-side hall-effect current sensor's open-collector fault output flag. The overcurrent detection threshold (OCD_THR, pin 15) is locked at a stable reference voltage of 1.24 V via a parallel R322 (3.3 kΩ) and C311 (1nF) filter combination to govern hardware fault tripping. This corresponds to an OCD threshold of 64A peak. When a secondary current threshold violation occurs, this line pulls low to propagate the overcurrent fault across the combined hardware detection path

Latch and PWM disable

The core of the protection logic relies on an S-R latch circuit (U201, MIC841) to lock the system into a safe state immediately following any fault detection.

- **Hardware interception logic:** When any of the three protection loops (OVP, P_CT, or OCD_S) force a comparator output LOW, the latch transitions its output state and controls an active hardware pull-down network driven by transistors Q200, Q201 (MMBT3904LT1G), and Q202 (BSS840215F)
- **AND gate override:** The latch output is combined directly with the raw controller-side switching signals (PWM_C_L1, PWM_C_H1, PWM_C_L2, PWM_C_H2, PWM_C_SR_A, PWM_C_SR_B) through a series of quad high-speed logic **AND gates** (U200A, U202A, 74LVC08A)
- **Forced low state:** As long as the hardware fault latch remains active, the logic AND gates override the incoming controller commands and force all active gate-driver output lines (PWM_S_L1, PWM_S_H1, PWM_S_L2, PWM_S_H2, PWM_SR_A, PWM_SR_B) to a low state. This action shuts down the primary full-bridge and secondary synchronous rectification stages, protecting the board components regardless of the MCU's state

Fault indication and reset

The hardware protection block provides visual status tracking alongside manual reset mechanisms:

- **Visual status flags:** When a safety trip event is latched in hardware, the circuit illuminates a high-visibility red **HW FAULT LED** (D201) to indicate an active shutdown condition
- **Manual reset switch:** A physical, tactile reset switch (SW200) is integrated directly into the latch bias network. Pressing this button manually clears the active S-R latch status, extinguishing the red D201 warning indicator and re-enabling the PWM gate drive lines once the underlying overvoltage or overcurrent condition is resolved

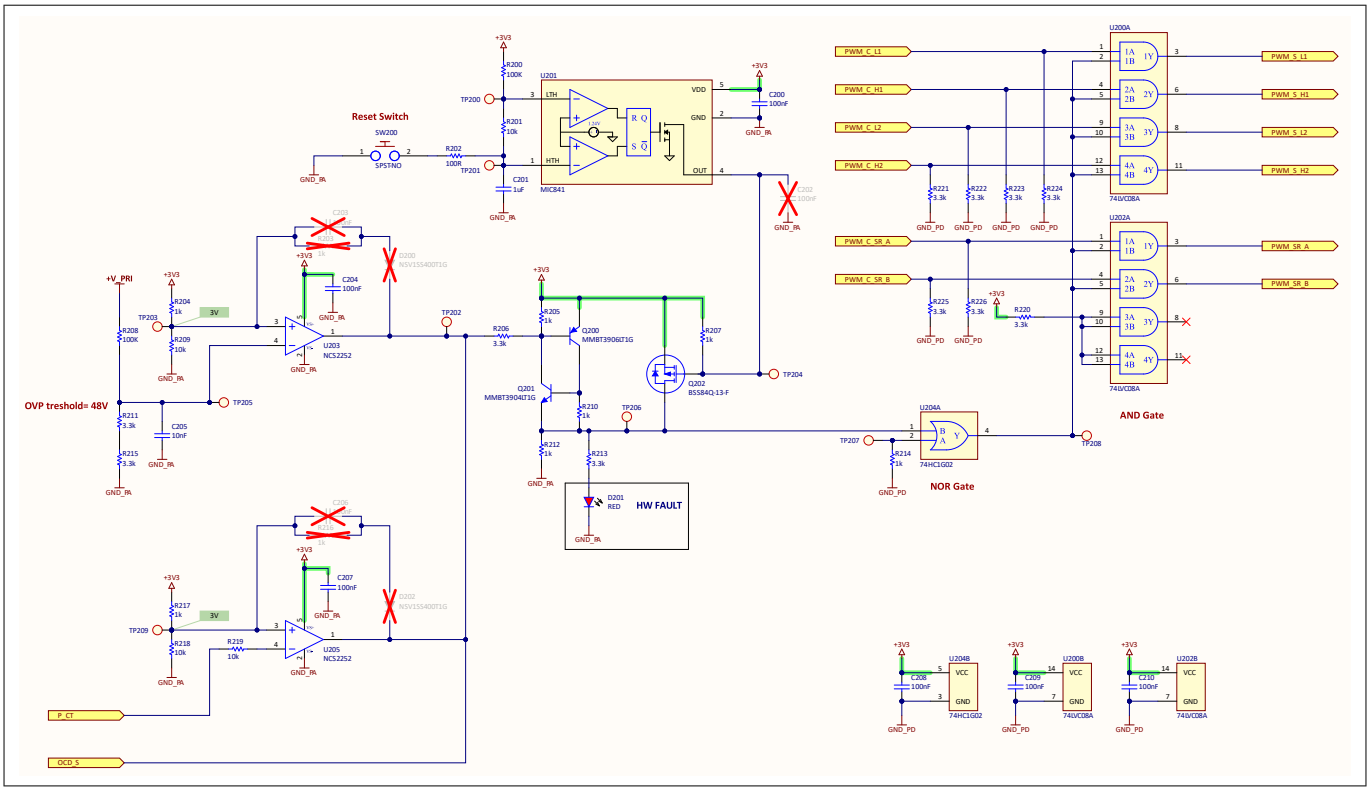


Figure 22 Protection: Detection and reset circuits

However, note that there is no direct connection from the hardware protection circuit to the MCU for signalling the onset of a hardware fault protection event. For this reason, the tripping thresholds have been intentionally selected at a high level compared to the nominal operating conditions, as shown in Table 4.

3.1.6 Controller

The MCU, as introduced in the Getting started section, is not part of the KIT_PSC3_LLC1 content. On the evaluation board, a **120-pin connector**, **(J300**, **HTEC8-160-01-L-DV-A-BL)** is added. The KIT_PSC3Mx_CC1 board can be easily plugged to get digital and analog lines connected.

In Table 5, the 120-pin connector pinout is presented; this table also includes control card pin assignment information. Although MCU is out of the scope of the evaluation board, the reason of adding a dedicated column for MCU is to explain where user can encounter limitations. It is possible to resolve such limitations by PCB rework concerning desoldering the 0 Ω resistor and soldering them back to establish right connection.

Table 5 120-pin connector pinout

Pin number	Low-voltage LLC board	KIT_PSC3M5_CC1	KIT_PSC3M5_CC1	Low-voltage LLC board	Pin number
1	–	+3V3	XRES	–	2
3	–	–	P3.0	FAULT_LED	4
5	PWM_C_H1	P4.4	P3.1	#6	6
7	PWM_C_L1	P4.5	P9.4	USER_BUTTON	8
9	GND_PD	GND	5V0_IN	+5V_P	10
11	PWM_C_H2	P4.6	–	–	12

(table continues...)

Table 5 (continued) 120-pin connector pinout

Pin number	Low-voltage LLC board	KIT_PSC3M5_CC1	KIT_PSC3M5_CC1	Low-voltage LLC board	Pin number
13	PWM_C_L2	P4.7	P9.0	MASTER_OUT_19	14
15	µBus_SCL	P7.0	P9.1	MASTER_OUT_21	16
17	µBus_SDA	P7.1	P9.2	MASTER_OUT_20	18
19	PWM_C_SR_A	P7.2	P9.3	MASTER_OUT_22	20
21	PWM_C_SR_B	P7.3	P9.5[1)]	–	22
23	GND_PD	GND	5V0_IN	+5V_P	24
25	MASTER_OUT_11	P4.0		–	26
27	MASTER_OUT_13	P4.1	P0.0/WCO_OUT[1)]	–	28
29	MASTER_OUT_15	P4.2	P0.1/WCO_IN[1)]	–	30
31	MASTER_OUT_17	P4.3	P1.0/ECO_IN[1)]	–	32
33	MASTER_OUT_12	P7.4	P1.1/ECO_OUT[1)]	–	34
35	MASTER_OUT_14	P7.5	–	–	36
37	GND_PD	GND	5V0_IN	+5V_P	38
39	MASTER_OUT_16	P7.6	–	–	40
41	MASTER_OUT_24	P7.7	P2.2	µBus_MOSI/CLK	42
43	–	–	P2.3	µBus_MISO/MOSI	44
45	µBus_PWM	P6.0	P5.0/SDA[1)]	–	46
47	µBus_RST	P6.1	P5.1/SCL[1)]	–	48
49	CAN_RX	P6.2	P3.2	UART2_TX	50
51	CAN_TX	P6.3	P3.3	UART2_RX	52
53	–	–	P5.2/UART_RX[1)]	µBus_TX	54
55	GND_PD	GND	P5.3/UART_TX[1)]	µBus_RX	56
57	SLAVE_IN_23	P8.0	P8.4	µBus_INT	58
59	USER_LED	P8.1	P8.5	#60	60
61	MASTER_OUT_23	P8.2	–	–	62
63	MASTER_OUT_18	P8.3	–	–	64
65	Vsec_Sense_P_ADC	AN_A0	VDDA_C	–	66
67	CT_Sense	AN_A1	AN_A7	NTC	68
69	Vsec_Sense	AN_A5	AN_A6	POT	70
71	Isec_Sense	AN_A3	AN_B4	Isec_Sense_LP	72
73	GND_PA	AGND	AGND	GND_PA	74
75	MASTER_OUT_7	AN_A4	AN_B5	Vpri_Sense	76

(table continues...)

Table 5 (continued) 120-pin connector pinout

Pin number	Low-voltage LLC board	KIT_PSC3M5_CC1	KIT_PSC3M5_CC1	Low-voltage LLC board	Pin number
77	–	VAREF_EXT_C	AN_B2	MASTER_OUT_2	78
79	MASTER_OUT_3	AN_A2	AN_B3	MASTER_OUT_4	80
81	MASTER_OUT_1	AN_B0	AN_B6	MASTER_OUT_6	82
83	MASTER_OUT_5	AN_B1	AN_B7	MASTER_OUT_8	84
85	–	–	–	–	86
87	GND_PA	AGND	AGND	GND_PA	88
89	–	–	–	–	90
91	–	–	–	–	92
93	Vsec_Sense_N_ADC	–	–	–	94
95	–	–	–	–	96
97	–	–	–	–	98
99	–	–	–	–	100
101	P8DAC0	–	–	P8DAC1	102
103	–	–	–	–	104
105	–	–	–	–	106
107	–	–	–	–	108
109	–	–	–	–	110
111	–	–	GND	GND_PA	112
113	GND_PA	GND	P2.0/TDI	µBus_CS	114
115	–	P1.2/TCK[1)]	P2.1/TDO	#116	116
117	–	P1.3/TMS[1)]	VBACKUP_C	–	118
119	–	+3V3	+3V3	–	120

1) MCU pin has a defined functionality on the control card; therefore, the pin is not exposed to the 120-pin connector by default. To enable them for usage on J300, a KIT_PSC3M5_CC1 PCB rework is required. See the Control Card user guide for more information.

3.1.7 LEDs

On the board, multiple LEDs are provided. Table 6 summarises their usage.

Table 6 LEDs

LED	Designator	Color	Function
HW FAULT	D201	RED	Normally OFF, it turns ON in case of a hardware failure, and protection is detected.
PWR ON	D303	GREEN	It turns ON when the +3V3 supply is generated, it will imply that the +5 V rail is also correctly generated.

(table continues...)

Table 6 (continued) LEDs

LED	Designator	Color	Function
USER LED	D301	GREEN	MCU-driven LED, the user is free to define when to turn it ON. It gets ON when the MCU pin is set HIGH. A viable usage of it can be, for example, to signal when the output voltage is inside its regulation limits, or to blink it when the power stage is actively modulating.
SW FAULT	D302	RED	MCU-driven LED, the user is free to define when to turn it ON. It gets ON when the MCU pin is set HIGH. A viable usage of this pin is to signal any abnormal condition detected by the firmware, for example, when reading a wrong sensor offset.
UART1 heart bit	D402	GREEN	Driven by U401 when UART1 communication is ongoing.
UART2 heart bit	D401	GREEN	Driven by U401 when UART2 communication is ongoing.

3.1.8 User button

The Low-voltage (LLC) Evaluation board has one user button **(SW300)**, which is connected to pin 8 of the connector (J300). This general-purpose button is provided to allow the user to interact with the hardware. By default, the signal is in the HIGH state. When the button is pressed, the signal transitions to a LOW state.

3.1.9 Master – Slave configuration

The Low-voltage (LLC) Evaluation Board can be connected to a second evaluation board with a 24-pin ribbon cable to complete a master-slave connection that can be controlled with a single digital power control card. To establish this setup, connect the MASTER connector (J302) from the LLC board (where the control card is plugged) to the SLAVE connector of the secondary evaluation board. The MASTER and SLAVE connectors carry only ADC, PWM, and GPIO signals. When two evaluation boards are connected in a daisy-chain configuration, a proper power interconnection must also be established in accordance with the requirements of the slave board. For example, the output voltage of a PFC board can be connected to the input voltage of the LLC board.

If the MASTER and SLAVE connections are not required, such connectors still offer valid help to provide an additional access point to the MCU pins on top of the test point connector (J303). Both the digital and analog signals can be probed.

3.1.10 Test point connector

The connector (J303) is provided on the board to allow users to probe all the relevant analog and digital signals used for driving the full-bridge LLC. By default, J303 is not populated with a connector, leaving the vias exposed. Oscilloscope probe tips can be directly inserted into these vias for an easy measurement. To simplify the grounding scheme, adjacent to J303, dedicated ground planes are provided that are compatible with crocodile clips. See the Test point overview section for more information.

3.1.11 Connection to network analyzer

It is possible to analyze the frequency response of the control loop by injecting on a small shunt resistor a frequency variable signal generated by an external network analyzer. This tool is used for determining the bandwidth and phase margin of the Low-voltage LLC converter. The evaluation board includes test points, **TP501** and **TP502** across resistor R303**,** for output voltage frequency response determination, **TP304** and **TP305** across resistor R302 for current frequency response determination.

3.1.12 Communication

Multiple interfaces are available to support the development of custom protocols with the MCU.

3.1.12.1 Serial communication interface (SCB)

The board includes a **USB-to-dual-UART bridge** (**CY7C65215**) to provide multiple communication interfaces between the MCU and an external host, such as a PC.

This device enumerates as **two virtual COM ports** when connected to a computer.

The purpose of offering two independent channels is to allow parallel implementation of different communication protocols. For example,

- **Low-frequency channel**: Intended for slow-rate monitoring protocols, such as exchanging configuration commands, reading fault/status registers, or retrieving low-frequency variables
- **High-frequency channel**: Suitable for streaming internal algorithm variables at high data rates, enabling a virtual oscilloscope functionality

These are example use cases only. Users are free to define and implement protocols according to their requirements.

Connection

Use a **USB cable** (Type-A to Type-C) to connect your PC to the connector (J400) on the board. When the USB cable is plugged in, 5 V will be provided to the board, the LDO will turn ON, generating the 3V3, and the LED D303 PWR_ON will glow. When serial communication is ongoing, the two green LEDs (D401, D402) will glow.

***Note**: The USB cable is not included in the box and must be purchased separately.*

See Figure 23 for the hardware implementation.

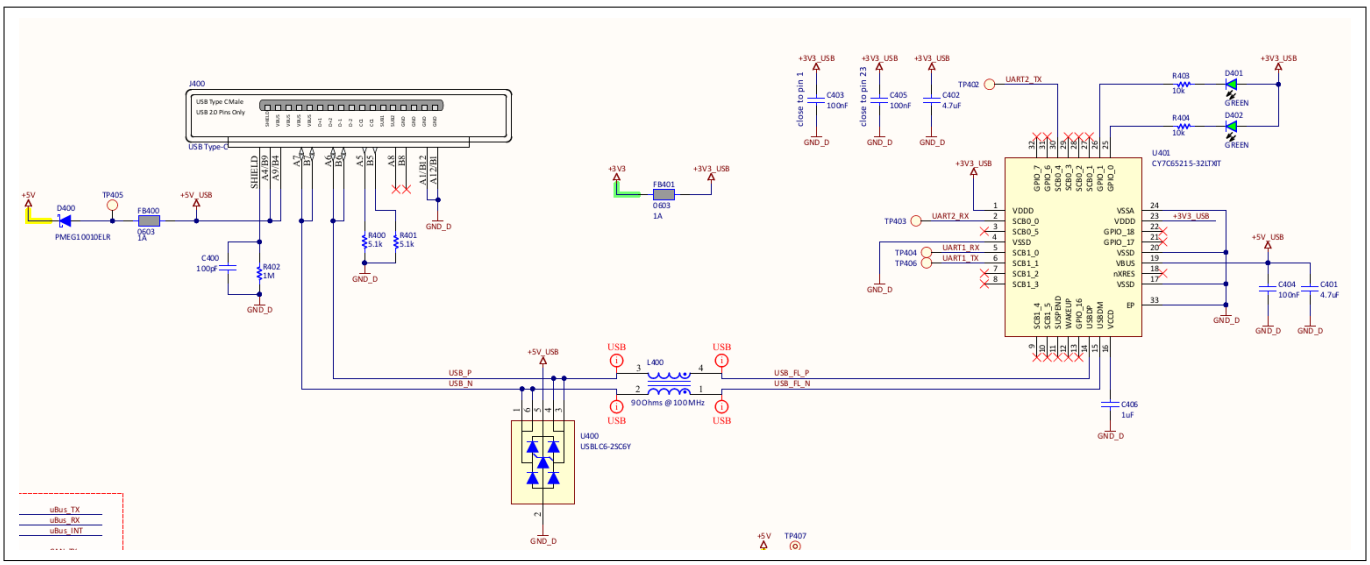


Figure 23 USB to double UART bridge

Dual USB–UART bridge configuration

The **U401** device, an Infineon **CY7C65215** dual-port USB bridge, converts the USB connection to two independent UART interfaces for the MCU

Custom baud rates can be configured through the associated **Serial Communication Block (SCB)** in the project's Device Configurator, under the **Baud Rate** property

Routing and port selection

- **UART2**
  - Routed directly to the 120-pin connector
- **UART1**
  - Routed through the **SW301** switch block. This configuration allows the same SCB instance to be re-purposed in one of the following ways:
    - As a **UART communication** is connected to the USB bridge or
    - As a **SPI interface** available on the **mikroBUS connector (SK400)**, which requires an additional configuration depending on the plugged control card

Table 7 show the SCB mapping configuration provided by SW301.

Table 7 SW301 options

Mapping configuration	Position			
	1	**2**	**3**	**4**
Not Connected	OFF	OFF	OFF	OFF
UART1	OFF	**ON**	**ON**	OFF
µBus_SPI	**ON**	OFF	OFF	**ON**

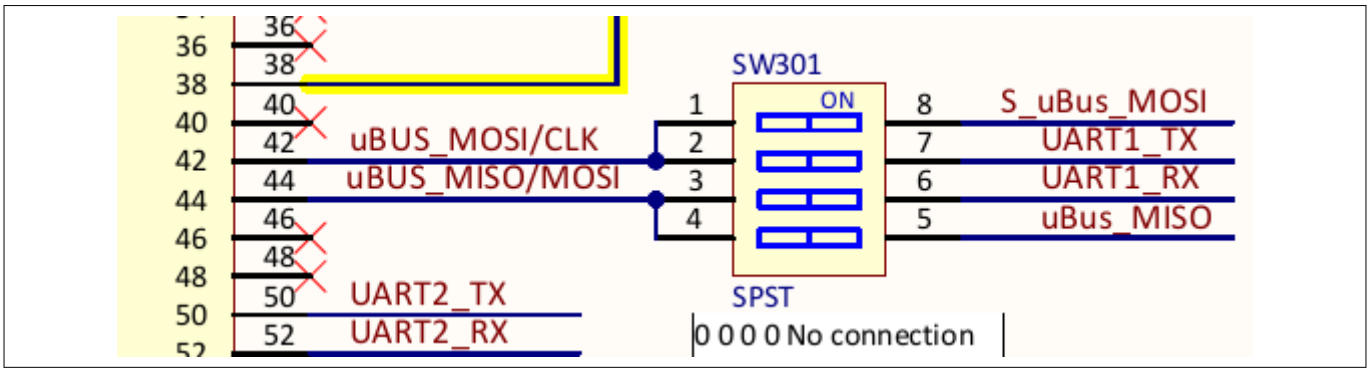


Figure 24 UART routing to 120-pin connector

3.1.12.2 CAN interface

In case you have an available CAN slave stack to port and test on PSOC™ Control MCU, the evaluation board supports a CAN interface by using the connector (J401).

Table 8 CAN interface functionality

J401	Functionality
1	CANH
2	GND
3	CANL

A straight connection to the 120-pin connection is provided using a dedicated CAN FD controller inside the MCU.

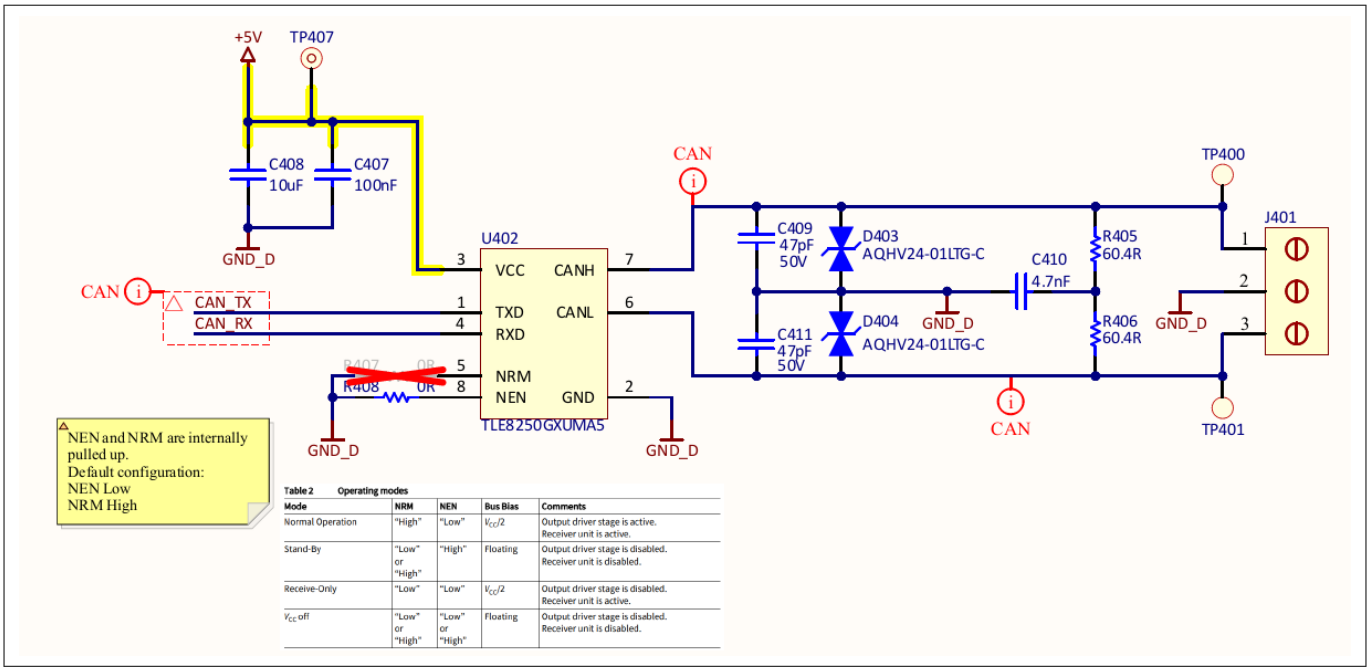


Figure 25 CAN schematic

3.1.12.3 mikroBUS expansion connector

The board is equipped with a **mikroBUS connector (SK400)** to extend the system's capabilities by adding third-party click boards. This widely used form factor allows easy integration of peripherals such as displays, communication modules, and sensors.

***Note**: No firmware example is provided for mikroBUS peripherals; users are expected to develop custom application code based on the requirement.*

See Figure 26 for the pinout of the mikroBUS interface.

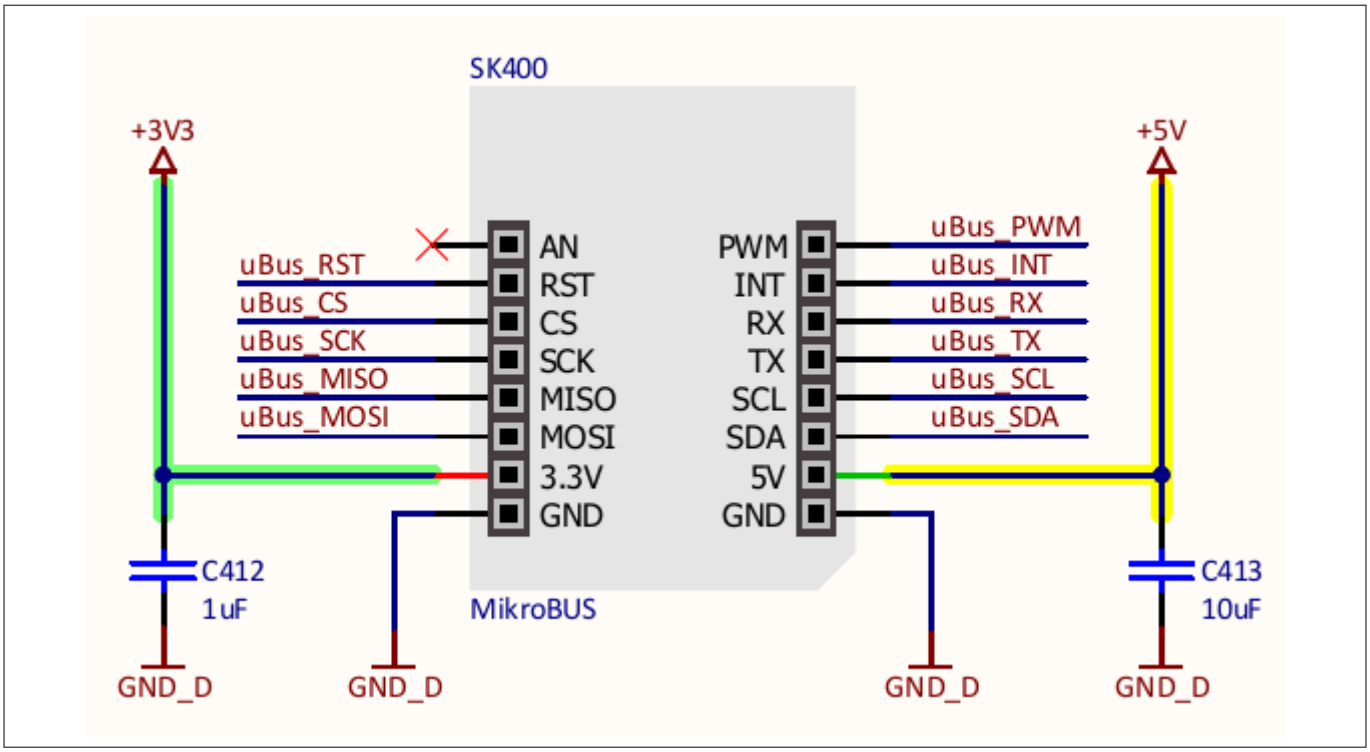


Figure 26 mikroBUS connector

SK400 exposes various resources (for example, **I²C**, **SPI**, and GPIOs). Some of them, although physically connected on the 120-pin connector, may not be connected on the control card side. Please refer to Table 5 to verify whether a PCB rework on the Control Card is required.

***Note**: Control Cards are designed to assign a local functionality to dedicated pins, hence not exposing the pin to the 120-pin connector. However, 0R resistors are added on the control card to repurpose the pin from local to external by a PCB rework. Refer to the control card schematic or user guide (both available at www.Infineon.com website) for more information.*

***Note**: To use I2C properly on SK400, it is mandatory to change the default initialization of the pin in "Device Configurator". When selecting I2C protocol, please change the SDA and SCK configuration from "Open Drain" to "Resistive pull-up".*

Users may connect jumper wires (not supplied) to these pins for development or test purposes. Most mikroBUS pins are directly connected to the 120-pin connector, with the exception of the SPI signals.

SPI / UART1 shared SCB

As described in the Serial communication interface (SCB) section, the mikroBUS **SPI interface** shares the same SCB instance as for **UART1** (USB-UART bridge).

Therefore, SPI and UART1 cannot operate simultaneously. The selection between these two functions is controlled through **SW301**.

Table 9 SW301 options

Parameter	Position			
	1	2	3	4
Not Connected	OFF	OFF	OFF	OFF

(table continues...)

Table 9 (continued) SW301 options

Parameter	Position			
	1	2	3	4
UART1	OFF	ON	ON	OFF
µBus_SPI	**ON**	OFF	OFF	**ON**

SW302 configuration

SW302 is a slider switch; its behavior is to connect one terminal to two possible terminations according to the slider position. It handles two terminals. The goal is to repurpose some 120-pin connections when replacing the suggested control card, **KIT_PSC3M5_CC1**, with future products.

Table 10 SW302 options

Control Card	Slider position	120-pin connector function
KIT_PSC3M8_CC1	1 – 2	J300.42 → µBUS_SCK
	4 – 5	J300.116 → µBUS_MOSI
KIT_PSC3M5_CC1	3 – 1	J300.42 → µBUS_MOSI
	6 – 5	J300.116 → µBUS_SCK

3.1.13 Test point overview

A comprehensive list of all test points on the board, is compiled into one summary table for easy reference. For compactness, the following abbreviations are used:

- TP = Test point
- DP: Differential probe
- SE: Single-ended probe
- GD: Gate driver
- PH: High-frequency leg
- LF: Low-frequency leg

Test point number	Circuit	Test point description	Remarks
GND_PP	–	Primary power ground plane	TP to be referred to the suggested ground plane for best accuracy.
GND_PA	–	Primary analog ground plane	
GND_PD	–	Primary digital ground plane	
GND_PS	–	Secondary power ground plane	Isolated secondary ground
TP100	Input stage	Main power input positive rail (+V_PRI)	SE at GND_PP Sense node
TP101	Input stage	Main power input negative return (GND_PP)	SE at GND_PP Sense node
TP102	Input stage	Auxiliary power input positive rail (+12 V)	SE at GND_PP; Sense node
TP103	Input stage	Buck regulator (U100) feedback node	SE at GND_PP

Test point number	Circuit	Test point description	Remarks
TP104	Input stage	Buck regulator switching node	SE at GND_PP
TP105	Input stage	Linear regulator (U101) output rail (+3V3)	SE at GND_PA;
TP106	Input stage	Buck regulator output rail (+5V_P)	SE at GND_PP;
TP107	Input stage	Auxiliary power input negative return (GND_PP)	SE
TP109	Input stage	Regulated gate drive auxiliary supply (+10V_P)	SE at GND_PP Primary gate drive rail
TP110	Input stage	Discrete regulator (Q101) reference node	Zener D104 clamp output
TP111	Input stage	Isolated driver input supply rail (+5V_P)	SE at GND_PD
TP112	Input stage	Transformer (TR100) secondary rectified output	Preregulator node
TP113	Input stage	Isolated secondary gate drive rail (`+5V_S`)	Secondary gate drive rail
TP114	Input stage	Pulse transformer primary input node 1	SE at GND_PD;
TP115	Input stage	Isolated secondary base reference voltage	SE at GND_PS; Bound by 5.6V Zener D107
TP116	Input stage	Pulse transformer secondary winding node 4	SE at GND_PS; AC input to rectification diode D105
TP118	Input stage	Isolated push-pull driver CLK	SE at GND_PD;
TP119	Input stage	Pulse transformer primary input node 3	SE at GND_PD; Driver output line D2 from U102
TP120	Input stage	Pulse transformer secondary winding node 6	SE at GND_PS; AC input to rectification diode D109
TP200	Protection stage	S-R latch (`U201`) LTH	SE at GND_PD
TP201	Protection stage	S-R latch (`U201`) HTH	SE at GND_PD
TP202	Protection stage	Primary input voltage (OVP) signal	SE at GND_PA
TP203	Protection stage	Primary input voltage (OVP) reference	SE at GND_PA
TP204	Protection stage	S-R latch (`U201`) OUT	SE at GND_PA
TP205	Protection stage	Primary input voltage (OVP) sensing node	SE at GND_PA; Scaled +V_PRI input to comparator U203
TP206	Protection stage	Hardware fault monitoring LED	SE at GND_PA
TP207	Protection stage	Hardwarelatch override debug	SE at GND_PD

Test point number	Circuit	Test point description	Remarks
TP208	Protection stage	Master hardware latch status monitoring	SE at GND_PD;
TP209	Protection stage	Primary current overcurrent threshold	SE at GND_PA
TP300	Analog sensing	Primary current (P_CT) loop measurement and injection point 1	SE at GND_PA;
TP301	Analog sensing	Primary current (P_CT) measurement	SE at GND_PA; Bode plot injection point 2
TP302	Analog sensing	Input DC voltage sense test Point (CH2)	SE at GND_PA; Voltage loop test node
TP303	Analog sensing	Input DC voltage sense test Point (CH1)	SE at GND_PA; Voltage loop test node
TP304	Analog sensing	Secondary current output (`Isec_Sense`)	SE at GND_PA
TP305	Analog sensing	Filtered secondary low-pass current output (`Isec_Sense_LP`)	SE at GND_PA
TP306	Analog sensing	GND_PA	SE
TP307	Analog sensing	J300.6 pin	SE at GND_PD
TP400	Peripherals	CAN high	SE at GND_PD
TP401	Peripherals	CAN low	SE at GND_PD
TP402	Peripherals	UART 2 transmit	SE at GND_PD
TP403	Peripherals	UART 2 receive	SE at GND_PD
TP404	Peripherals	UART 1 receive	SE at GND_PD
TP405	Peripherals	USB supply voltage	SE at GND_PD;
TP406	Peripherals	UART 1 transmit	SE at GND_PD;
TP503	Power stage	Primary H-Bridge leg 1 switch node	DP
TP504	Power stage	Resonant tank capacitor voltage array	DP at TP 503
TP505	Power stage	Primary H-Bridge leg 1 gate drive	DP / SE at GND_PP;
TP506	Power stage	GND_PP	-
TP507	Power stage	Transformer TR500 primary input pin 2	DP
TP508	Power stage	LLC secondary output	SE at GND_PS;
TP509	Power stage	Synchronous rectifier (Q503) gate control	DP / SE at GND_PS;

Test point number	Circuit	Test point description	Remarks
TP510	Power stage	Synchronous rectifier (Q502) Gate Control	SE at GND_PS;
TP511	Power stage	Transformer (TR500) primary input pin 5	DP
TP512	Power stage	GND_PS, J500.1	-
TP513	Power stage	Primary H-Bridge leg 2 switch node	DP
TP514	Power stage	Primary H-Bridge leg 2 gate drive	DP / SE at GND_PP;
TP515	Power stage	Transformer (TR500) secondary pin 10	DP / SE at GND_PS;
TP515	Power stage	Transformer (TR500) secondary pin 8	DP / SE at GND_PS;
J303 Pin 1	Interface connector	Controller PWM output leg 1 high-side (`PWM_C_H1`)	SE at GND_PD; Raw control command from MCU
J303 Pin 2	Interface connector	Controller PWM output leg 1 low-side (`PWM_C_L1`)	SE at GND_PD; Raw control command from MCU
J303 Pin 3	Interface connector	Controller PWM output leg 2 high-side (`PWM_C_H2`)	SE at GND_PD; Raw control command from MCU
J303 Pin 4	Interface connector	Controller PWM output leg 2 low-side (`PWM_C_L2`)	SE at GND_PD; Raw control command from MCU
J303 Pin 5	Interface connector	Synchronous rectifier control channel A (`PWM_C_SR_A`)	SE at GND_PD; Raw logic command before isolator `U506`
J303 Pin 6	Interface connector	Synchronous rectifier control channel B (`PWM_C_SR_B`)	SE at GND_PD; Raw logic command before isolator `U506`
J303 Pin 7	Interface connector	Manual user push-button status line (`USER_BUTTON`)	SE at GND_PD; Latches high/low based on `SW300` state
J303 Pin 8	Interface connector	Main Auxiliary Board power line (`+5V_P`)	SE at GND_PD; Primary auxiliary power rail verification point
J303 Pin 9	Interface connector	Slave controller communication line (`SLAVE_IN_23`)	SE at GND_PD
J303 Pin 13	Interface connector	Isolated output voltage (`Vsec_Sense_P`)	SE at GND_PD
J303 Pin 14	Interface connector	Primary tank transformer current sense (`CT_Sense`)	SE at GND_PA;

Test point number	Circuit	Test point description	Remarks
J303 Pin 15	Interface connector	Single-ended reconstructed output voltage (`Vsec_Sense`)	SE at GND_PA;
J303 Pin 16	Interface connector	Planar transformer NTC thermistor output (`NTC`)	SE at GND_PA;
J303 Pin 17	Interface connector	Manual on-board tuning dial voltage line (`POT`)	SE at GND_PA;
J303 Pin 18	Interface connector	Secondary low-pass filtered current (`Isec_Sense_LP`)	SE at GND_PA;
J303 Pin 19	Interface connector	Secondary high-speed transient current (`Isec_Sense`)	SE at GND_PA;
J303 Pin 20	Interface connector	Isolated output voltage (`Vsec_Sense_N`)	DP (with Pin 13);
J303 Pin 21	Interface connector	Input DC bus attenuated voltage telemetry (`Vpri_Sense`)	SE at GND_PA; Downscaled primary rail profile
J303 Pin 22	Interface connector	Auxiliary custom DAC output profile 1 (`P8DAC1`)	SE at GND_PD
J303 Pin 23	Interface connector	Auxiliary custom DAC output profile 0 (`P8DAC0`)	SE at GND_PD

4 Production data

The board has been designed using Altium Designer. The full PCB design data (schematics, layout, and BOM) of this board can be downloaded from the kit webpage.

Revision history

Document revision	Date	Description of changes
**	2026-07-08	Initial release

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Edition 2026-07-08

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference

IFX-xgl1779899517419

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The electrical installation must be completed in accordance with the appropriate safety requirements.