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32-Bit Microcontroller

FM0+ Family

Peripheral Manual Analog Macro Part

Doc. No. 002-05020 Rev. *C

Cypress Semiconductor
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San Jose, CA 95134-1709
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Preface

Thank you for your continued use of Cypress products.
Read this manual and "Data Sheet" thoroughly before using products in this family.

In addition, this manual is defined as separate volume which is extracted the Analog macro part from the peripheral manual.

Purpose of this manual and intended readers

This manual explains the functions and operations of this family and describes how it is used. The manual is intended for engineers engaged in the actual development of products using this family.

Note:

- *This manual explains the configuration and operation of the peripheral functions, but does not cover the specifics of each device in the series.Users should refer to the respective data sheets of devices for device-specific details.*
- *Whether a peripheral function is on board or not is dependent on product type. See data sheets for details.*

Sample programs and development environment

Cypress offers sample programs free of charge for using the peripheral functions of the FM0+ family. Cypress also makes available descriptions of the development environment required for this series. Feel free to use them to verify the operational specifications and usage of this Cypress microcontroller.

Microcontroller support information:

https://community.cypress.com/community/MCU

Note:

- *Note that the sample programs are subject to change without notice. Since they are offered as a way to demonstrate standard operations and usage, evaluate them sufficiently before running them on your system.*
  Cypress assumes no responsibility for any damage that may occur as a result of using a sample program.

Overall Organization of This Manual

Peripheral Manual Analog Part has 3 chapters and APPENDIXES as shown below.

CHAPTER 1-1 : A/D Converter
CHAPTER 1-2 : 12-bit A/D Converter
CHAPTER 1-3 : A/D Timer Trigger Selection
CHAPTER 2 : 10-bit D/A Converter
CHAPTER 3-1 : LCD Controller Overview
CHAPTER 3-2 : LCD Controller (TYPE1)
CHAPTER 3-3 : LCD Controller (TYPE2)
APPENDIXES

Related Manuals

The manuals related to this family are listed below. See the manual appropriate to the applicable conditions.

The contents of these manuals are subject to change without notice. Contact us to check the latest versions available.

Peripheral Manual

- FM0+ Family PERIPHERAL MANUAL
  (Called "PERIPHERAL MANUAL" hereafter)
- FM0+ Family PERIPHERAL MANUAL Timer Part
  (Called "Timer Part" hereafter)
- FM0+ Family PERIPHERAL MANUAL Analog Macro Part (this manual)
  (Called "Analog Macro Part" hereafter)
- FM0+ Family PERIPHERAL MANUAL Communication Macro Part
  (Called "Communication Macro Part" hereafter)
- FM0+ Family PERIPHERAL MANUAL Ethernet Part
  (Called "Ethernet Part" hereafter)

Data sheet

For details about device-specific, electrical characteristics, package dimensions, ordering information etc., see the following document.

- 32-bit Microcontroller FM0+ Family DATA SHEET

Note:

- *The data sheets for each series are provided.*
  See the appropriate data sheet for the series that you are using.

CPU Programming manual

For details about Arm Cortex-M0+ core, see the following documents that can be obtained from http://www.arm.com/.

- Cortex-M0+ Technical Reference Manual
- Armv6-M Architecture Application Level Reference Manual

Flash Programming manual

For details about the functions and operations of the built-in flash memory, see the following document.

- FM0+ Family FLASH PROGRAMMING MANUAL

Note:

- *The Flash Programming manuals for each series are provided.*
  See the appropriate Flash Programming manual for the series that you are using.

How to Use This Manual

Finding a function

The following methods can be used to search for the explanation of a desired function in this manual:

- Search from the table of the contents

  The table of the contents lists the manual contents in the order of description.

- Search from the register

  The address where each register is located is not described in the text. To verify the address of a register, see "A. Register Map" in "APPENDIXES".

About the chapters

Basically, this manual explains Analog macro Part.

Terminology

This manual uses the following terminology.

Term	Explanation
Word	Indicates access in units of 32 bits.
Half word	Indicates access in units of 16 bits.
Byte	Indicates access in units of 8 bits.

Notations

- The notations in bit configuration of the register explanation of this manual are written as follows.
  - bit : bit number
  - Field : bit field name
  - Attribute : Attributes for read and write of each bit
    - R : Read only
    - W : Write only
    - R/W : Readable/Writable
    - - : Undefined
  - Initial value : Initial value of the register after reset
    - 0 : Initial value is "0"
    - 1 : Initial value is "1"
    - X : Initial value is undefined

- The multiple bits are written as follows in this manual.
  Example : bit7:0 indicates the bits from bit7 to bit0

- The values such as for addresses are written as follows in this manual.
  - Hexadecimal number : "0x" is attached in the beginning of a value as a prefix (example : 0xFFFF)
  - Binary number : "0b" is attached in the beginning of a value as a prefix (example: 0b1111)
  - Decimal number : Written using numbers only (example : 1000)

The target products in this manual

■ In this manual, the products are classified into the following groups and are described as follows.
For the descriptions such as "TYPE1-M0+", “TYPE2-M0+” and “TYPE3-M0+”, see the relevant items of the target FM0+ product in the lists below.

Table 1 FM0+ family TYPE1 Product list

TYPE	Flash memory size	
	56 Kbytes	**88 Kbytes**
TYPE1-M0+	S6E1A11B S6E1A11C	S6E1A12B S6E1A12C

Table 2 FM0+ family TYPE2 Product list

TYPE	Flash memory size	
	304K bytes	**560K bytes**
TYPE2-M0+	S6E1B84E	S6E1B86E
	S6E1B84F	S6E1B86F
	S6E1B84G	S6E1B86G
	S6E1B34E	S6E1B36E
	S6E1B34F	S6E1B36F
	S6E1B34G	S6E1B36G

Table 3 FM0+ family TYPE3 Product list

TYPE	Flash memory size	
	64K bytes	**128K bytes**
TYPE3-M0+	S6E1C31B	S6E1C32B
	S6E1C31C	S6E1C32C
	S6E1C31D	S6E1C32D
	S6E1C11B	S6E1C12B
	S6E1C11C	S6E1C12C
	S6E1C11D	S6E1C12D

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CHAPTER 1-1: A/D Converter

This chapter explains the functions and operations of the A/D converter.

1. Configuration
2. Functions and Operations
3. Usage Precautions

CODE: 9BFADCTOP_FM0-E03.0

1. Configuration

The A/D converter converts analog input voltage from an external pin to a digital value.

A/D Converter Configuration

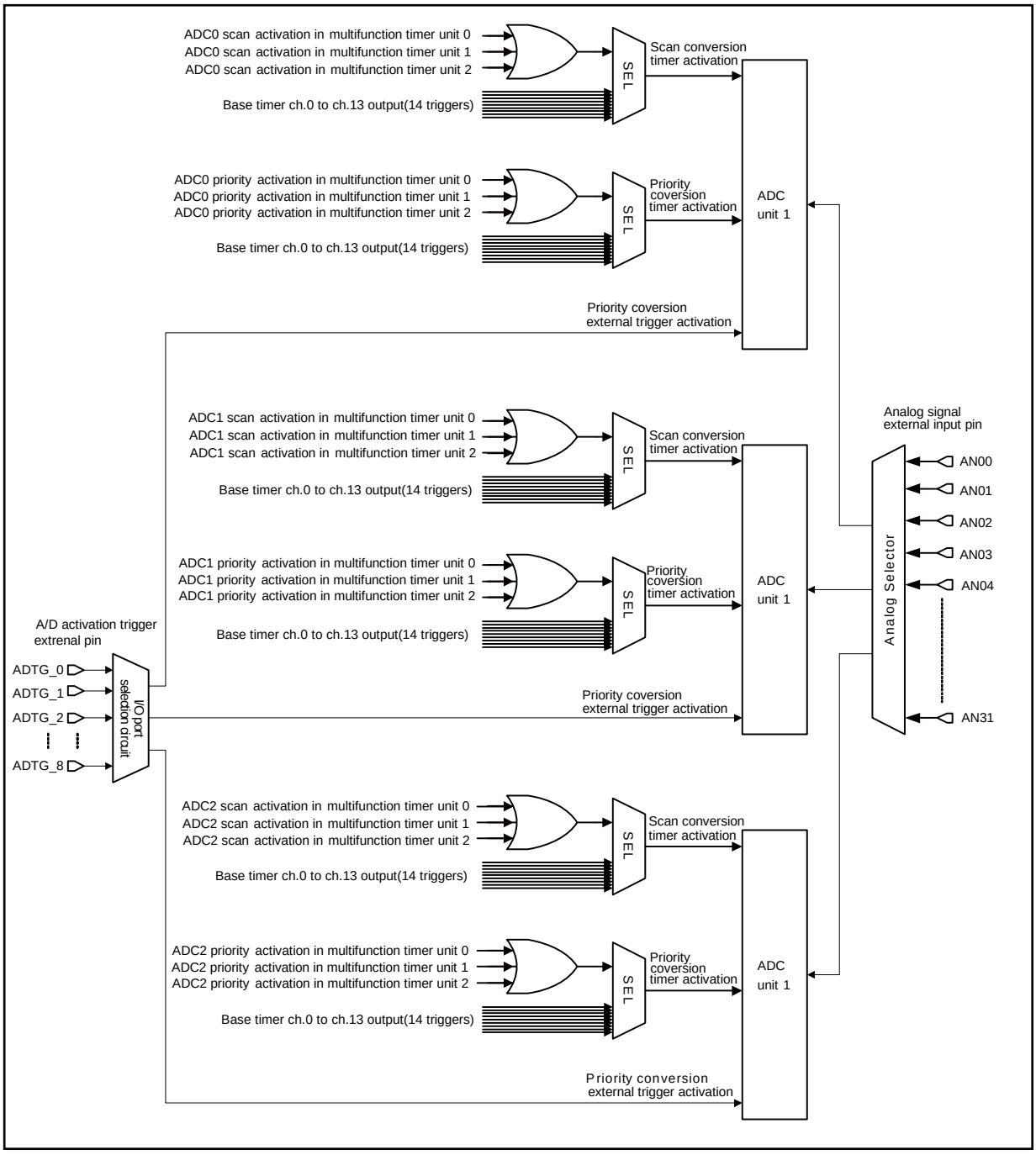
- The maximum 3 units of A/D converters with 12-bit resolution have been installed.
- Any channel can be selected to any unit from the maximum 32 channels of analog input.
- The following triggers can be selected as an activation trigger for A/D conversion.
  - Priority conversion activation trigger

    Trigger input from an external pin
    Timer trigger input (base timer or multifunction timer)
    Software activation
  - Scan conversion activation trigger

    Timer trigger input (base timer or multifunction timer)
    Software activation

Figure 1-1 shows a block diagram of the A/D converter with the related circuits.

Figure 1-1 Block Diagram of the A/D Converter with the Related Circuits



2. Functions and Operations

See descriptions of the following related chapters for functions and operations of the A/D converter.

12-bit A/D Converter Operation

See the chapter of 12-bit A/D Converter for conversion operations of 12-bit A/D converter.

12-bit A/D Timer Trigger Select Operation

See the chapter of A/D Timer Trigger Selection for operations of 12-bit A/D converter timer trigger selection.

3. Usage Precautions

This section shows the notes.

Notes on 12-bit A/D Converter

- Simultaneous A/D conversion of multiple channels is possible on the products that have multiple A/D converters.
  Do not select the same input channel with the multiple units.

- Some channels of an analog input cannot be used for certain products. Do not change the selection registers (SCIS0, SCIS1, SCIS2, and SCIS3) and the sampling time selection registers (ADSS0, ADSS1, ADSS2, and ADSS3) for the channels which cannot be used from their initial values.

- In this family, P1A[2:0] of the priority conversion input selection register (PCIS) should be selected for an analog input channel during priority conversion. Always write 0 to ESCE bit of the priority conversion control register (PCCR) of the 12-bit A/D converter.

- DMA transfer using the A/D interrupt request generation of this family supports only DMA transfer using generation of a scan conversion interrupt request. DMA transfer using a priority conversion interrupt request is not supported.

- Product specifications and Number of channels/units mounted

The number of analog inputs/units mounted and the number of base timer channels used for AD Startup trigger are different by products.
For details, see Product Configuration in Data Sheet of the product used.

CHAPTER 1-2: 12-bit A/D Converter

This chapter explains the functions and operations of the 12-bit A/D converter.

1. Overview
2. Configuration
3. Explanation of Operations
4. Setup procedure Examples
5. Registers

CODE: 9xFBAD12M3_FM0-E03.0

1. Overview

The 12-bit A/D converter is a function that converts analog input voltages into 12-bit digital values using a type of the RC Successive Approximation Register.

Features of the 12-bit A/D Converter

- 12-bit resolution
- Converter using a type of RC Successive Approximation Register with sample and hold circuits
- Two sampling times selectable for each input channel
- Scan conversion operation:
  - Multiple analog inputs can be selected from multiple channels.
  - Start factors are software and timers.
  - Repeat mode is available.
- Priority conversion operation:

  Even during scan operation, if a start factor of priority conversion occurs, it is possible to interrupt the ongoing scan conversion and perform conversion with high priority (There are two priority levels: 1 and 2. Priority level 1 is higher than priority level 2.).

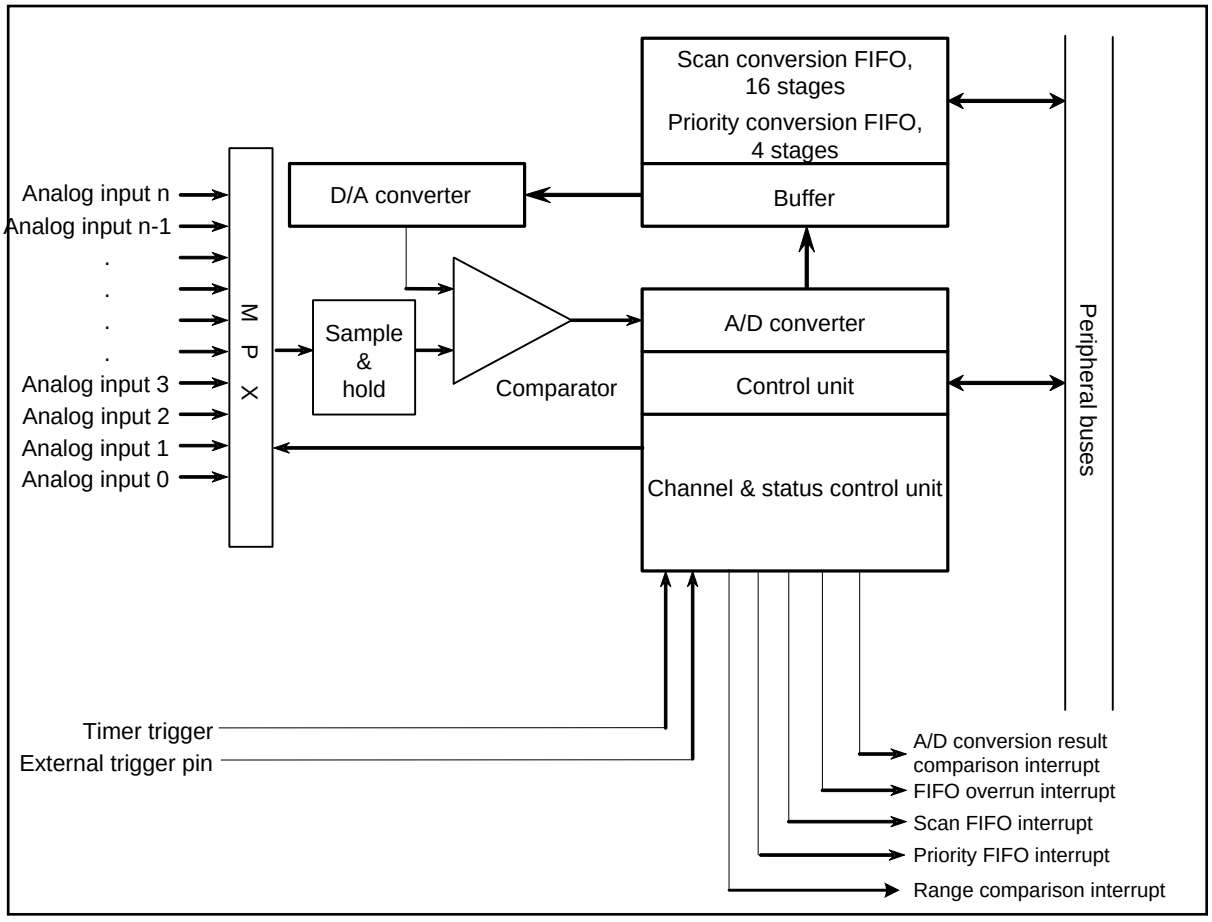
  Start factors are software and timers (priority level 2), and external triggers (priority level 1).
- FIFO function:
  - Sixteen FIFO stages for scan conversion and four FIFO stages for priority conversion are incorporated.
  - An interrupt is generated when data is written in the specified count of FIFO stages.
- Changeable A/D conversion data placement (selectable between shift to the MSB side and shift to LSB side)
- The A/D conversion result comparison function is available.
- Range comparison function
  - Upper and lower limits can be specified
  - Either detection of within the range or without the range can be set.
  - With the continuous detection, the noise can be removed. The continuous detection time can be specified from 1 to 7.
  - For the detection of without the range, over the upper limit or below the lower limit can be specified.
- There are five interrupt factors as follows:
  1. Scan conversion FIFO stage count interrupt
  2. Priority conversion FIFO stage count interrupt
  3. FIFO overrun interrupt (for both scan and priority conversion processes)
  4. A/D conversion result comparison interrupt
  5. Range comparison interrupt
- DMA transfer triggered by an interrupt request.

2. Configuration

This section provides the configuration of the 12-bit A/D converter.

12-bit A/D Converter Block Diagram

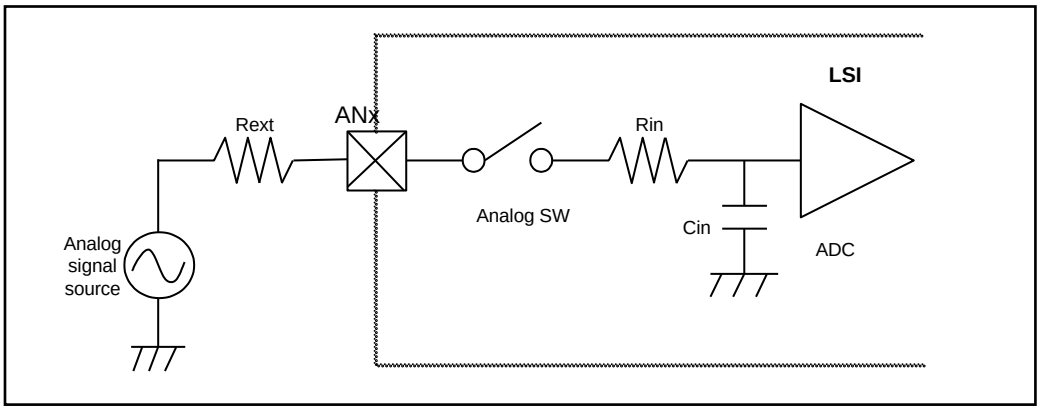
Figure 2-1 12-bit A/D Converter Block Diagram



Input Impedance

The sampling circuit of the A/D converter is shown as an equivalent circuit in Figure 2-2. See the "Electrical Characteristics" in "Data Sheet" to make sure that the external impedance, Rext should be selected not to exceed the sampling time.

Figure 2-2 Input Impedance Equivalent Circuit Diagram



3. Explanation of Operations

This section explains the operations of the 12-bit A/D converter.

3.1. Enabling Operations of the A/D Converter
3.2. A/D Conversion Operation
3.3. FIFO Operations
3.4. A/D Comparison Function
3.5. Range Comparison Function
3.6. Starting DMA

3.1 Enabling Operations of the A/D Converter

This section explains enabling operations of the A/D converter.

The A/D converter must be in the operation enable state prior to A/D conversion. Writing "1" to the ENBL bit of the A/D Operation Enable Setup Register (ADCEN) turns the A/D converter from the operation stop state to the operation enable state after the period of operation enable state transitions. On the other hand, writing "0" to the ENBL bit of the ADCEN register turns the A/D converter immediately to the operation stop state.

A/D conversion can be performed only in the operation enable state. An A/D conversion request in the operation stop state is ignored. If the A/D converter enters the operation stop state during A/D conversion, A/D conversion stops immediately.

Reading the READY bit of the ADCEN register allows you to check whether the A/D converter is in the operation enable state or not.

3.2 A/D Conversion Operation

The A/D converter can perform two types of conversion processes: scan conversion and priority conversion.

3.2.1. Scan Conversion Operation

3.2.2. Priority Conversion Operation

3.2.3. Priority Levels and State Transitions

3.2.1 Scan Conversion Operation

This section explains the scan conversion operation.

The input channels are selected in the Scan Conversion Input Selection Register (SCIS). By setting the corresponding bit in the SCIS to 1, any necessary channel can be selected from among multiple analog input channels.

The A/D converter can be started by software or a timer. To start the converter by software, set the SSTR bit in the Scan Conversion Control Register (SCCR) to 1. Then conversion starts. To start the converter by timers, set the SHEN bit in the SCCR register to 1 to enable timer start. Conversion starts when the timer's rising edge is detected. When conversion starts, the SCS bit in the ADSR register is set to 1. When the conversion is completed, the SCS bit is reset to 0.

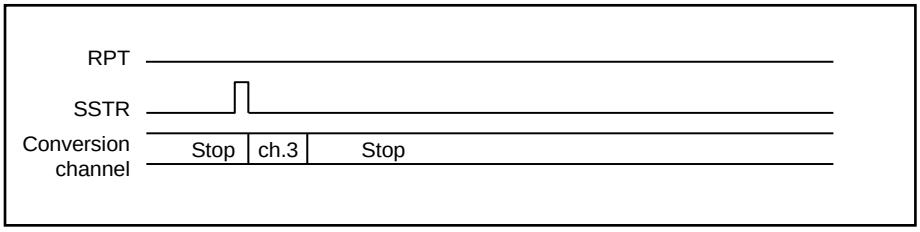
When the SSTR bit in the SCCR register is set to 1 again during A/D conversion or the timer's rising edge is detected again while timer start is enabled, the ongoing conversion operation is immediately stopped and initialized and the A/D conversion is performed again (the operation is restarted).

The available scan conversion modes are as follows:

1. **One-shot mode for a single channel**

   This mode is selected when only one analog priority conversion is specified for scan conversion and RPT = 0 in the SCCR register. When the selected priority conversion is completed, the operation stops.

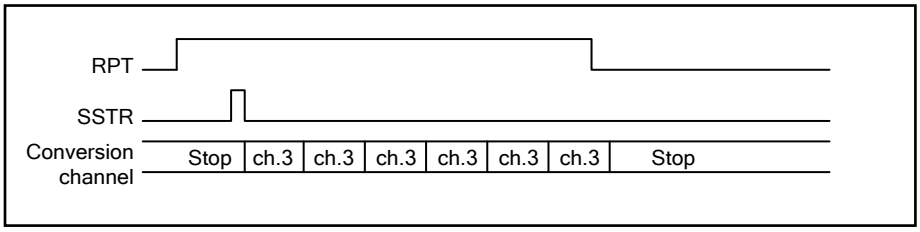
Figure 3-1 Stop of Operation in One-shot Mode for a Single Channel (SCIS3 = 0x00, SCIS2 = 0x00, SCIS1 = 0x00, SCIS0 = 0x08)



2. **Continuous mode for a single channel**

   This mode is selected when only one analog priority conversion process is specified for scan conversion and RPT = 1 in the SCCR register. When the selected priority conversion is completed, the same priority conversion is started again. To stop A/D conversion, set RPT bit to 0. The operation stops when the ongoing A/D conversion is completed.

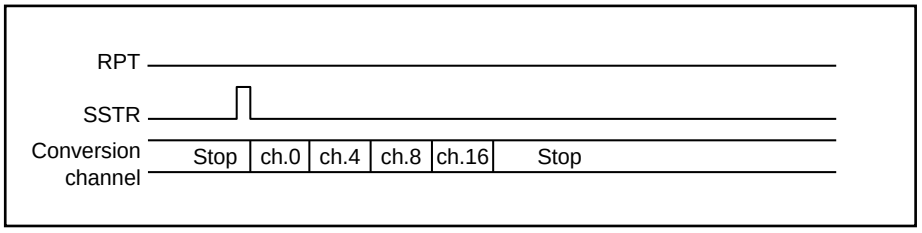
Figure 3-2 Stop of Operation in Continuous Mode for a Single Channel (SCIS3 = 0x00, SCIS2 = 0x00, SCIS1 = 0x00, SCIS0 = 0x08)



3. One-shot mode for multiple channels

This mode is selected when multiple analog channels are specified for scan conversion and RPT = 0 in the SCCR register. When the conversion starts, the existence of each channel is automatically checked. While the channels are switched from one to another, A/D conversion is started and the conversion result is written to FIFO when the conversion is completed. The conversion channels are selected in descending order of channel number (starting from ch.0). Channels not selected in the SCIS register are skipped and the conversion operation targets the next selected channel. When the A/D conversion of the last one of the selected channels is completed, the A/D conversion is stopped.

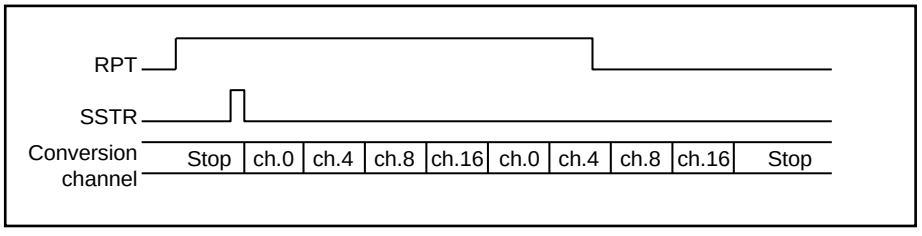
Figure 3-3 Stop of Operation in One-shot Mode for Multiple Channels (SCIS3 = 0x00, SCIS2 = 0x01, SCIS1 = 0x01, SCIS0 = 0x11)



4. Continuous mode for multiple channels

This mode is selected when multiple analog channels are specified for scan conversion and RPT = 1 in the SCCR register. When the conversion starts, the existence of each channel is automatically checked. While the channels are switched from one to another, A/D conversion is started and the conversion result is written to FIFO when the conversion is completed. The conversion channels are selected in descending order of channel number (starting from ch.0). Channels not selected in the SCIS register are skipped and the conversion operation targets the next selected channel. When the A/D conversion of the last one of the selected channels is completed, the conversion operation starts again from ch.0. To end A/D conversion, clear the RPT bit to 0. The operation stops when the A/D conversion of the last one of the selected channels is completed.

Figure 3-4 Stop of Operation in Continuous Mode for Multiple Channels (SCIS3 = 0x00, SCIS2 = 0x01, SCIS1 = 0x01, SCIS0 = 0x11)



3.2.2 Priority Conversion Operation

This section explains the priority conversion operation.

This mode is used to give priority to a specific conversion process. Even when scan conversion is in progress, if priority conversion is started, the scan conversion is interrupted immediately and the priority conversion is performed. When the priority conversion is completed, the scan operation restarts from the channel where it was interrupted. If conversion with higher priority (priority level 1) is started while the conversion with lower priority (priority level 2) is performed, the priority level 2 conversion is interrupted immediately and the priority level 1 conversion is performed. When the priority level 1 conversion is completed, the priority level 2 conversion is restarted.

Two levels of priority are given to priority conversion. Priority level 1 is the highest and priority level 2 is the second. Trigger start by an external pin is assigned as the start factor at priority level 1 and software/timer start is assigned as that at priority level 2.

- The input channels are selected in the Priority Conversion Input Selection register (PCIS).

  The procedure for selecting channels at priority level 1 differs depending on the ESCE bit in the Priority Conversion Control Register (PCCR).
  When ESCE = 0: The P1A[2:0] bits in the PCIS register are used. Only one of the eight channels, ch.0 to ch.7, can be selected.
  When ESCE = 1: The setting of the P1A[2:0] bits in the PCIS register is ignored. Only one of the eight channels, ch.0 to ch.7, can be selected with input from the external pin (ECS[2:0]).

  Example: ECS[2:0] = 000 -> ch.0
  = 010 -> ch.2
  = 111 -> ch.7

- The P2A[4:0] bits in the PCIS register are used for selecting the channel at priority level 2. Only one of the multiple input channels can be selected.

The start factor of A/D conversion differs depending on the priority level.

- Priority level 1 (highest priority) conversion can be started by a falling edge of external trigger input.

  To enable external trigger start, set the PEEN bit in the PCCR register to 1.

- Priority level 2 conversion can be started by software or a timer.

  To start conversion by software, set the PSTR bit in the PCCR register to 1. To start conversion by a timer, set the PHEN bit in the PCCR register to 1 to enable timer start. Conversion starts when the timer's rising edge is detected. When conversion starts, the PCS bit in the ADSR register is set to 1. When the conversion is completed, the PCS bit is reset to 0.

In priority conversion mode, the conversion cannot be restarted. In addition, start factors at the same priority level are ignored.
(A timer start factor is ignored during software-started operation.)

If a priority level 1 start factor (external trigger) occurs during conversion started by a priority level 2 start factor (software or timer), the PCNS bit in the A/D Status Register (ADSR) is set to 1 and the priority level 2 conversion is interrupted immediately. When the priority level 1 conversion is completed, PCNS is reset to 0 and the interrupted priority level 2 conversion is restarted. If a priority level 2 start factor occurs during priority level 1 conversion, the priority level 2 start factor is reserved (retained) and PCNS bit is set to 1. When the priority level 1 conversion is completed, PCNS bit is reset to 0 and the priority level 2 conversion is started.

Priority conversion can only be performed in one-shot mode for a single channel.

3.2.3 Priority Levels and State Transitions

This section explains priority levels and state transitions.

Priority Levels

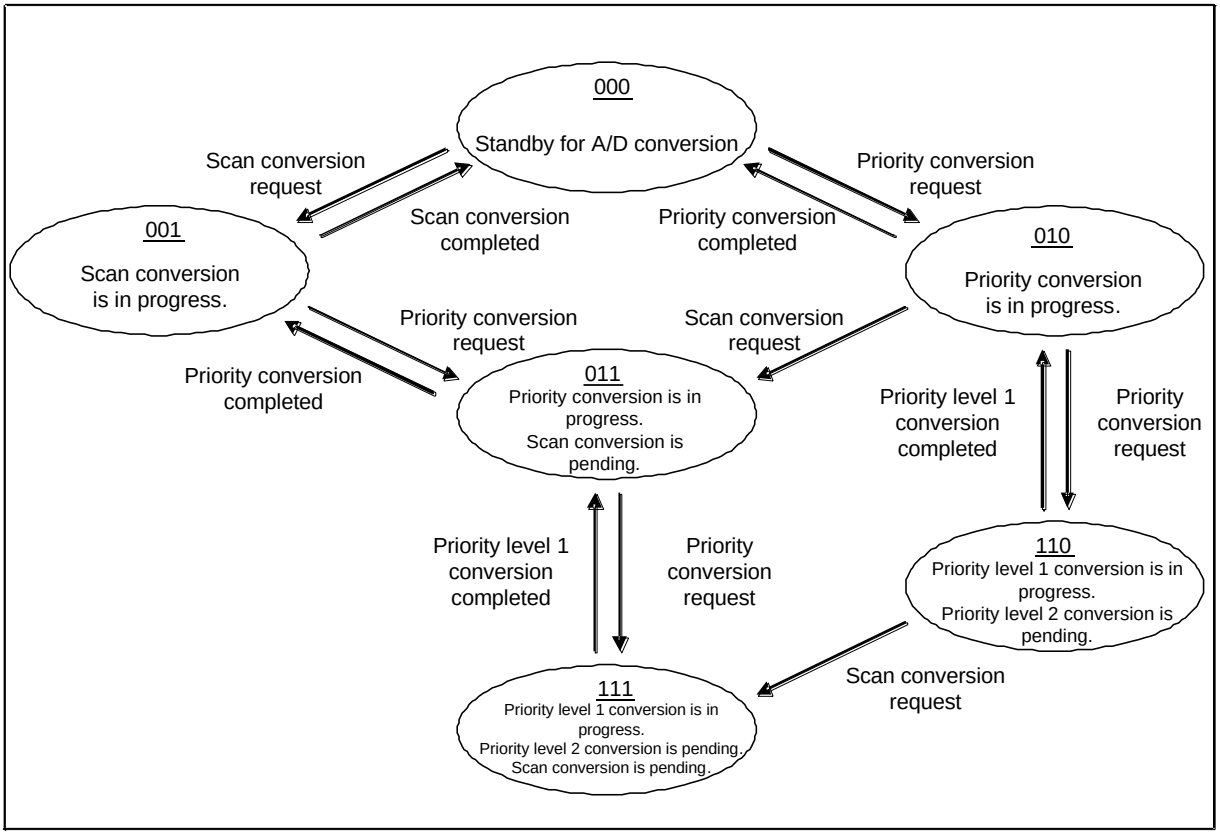
Table 3-1 Priority Levels for the A/D Converter

Priority level	Conversion type	Start factor
1	Priority level 1 conversion	- Input from external trigger pin (at falling edge)
2	Priority level 2 conversion	- Software (when the priority conversion start bit (PSTR) of priority conversion control register (PCCR) is set to 1) - Trigger input from timer (at rising edge)
3	Scan conversion	- Software (when the scan conversion start bit (SSTR) of scan conversion control register (SCCR)is set to 1) - Trigger input from timer (at rising edge)

- When a startup by priority conversion occurs during scan conversion
  The scan conversion operation is interrupted and priority conversion operation is performed. When the priority conversion operation is completed, the scan conversion is restarted from the channel where it was interrupted.
- When a startup at priority level 1 occurs during conversion at priority level 2
  The priority level 2 conversion is interrupted and the operation by the startup at priority level 1 is performed. When the priority level 1 operation is completed, the priority level 2 conversion is restarted automatically.
- When a startup at priority level 2 occurs during conversion at priority level 1
  The start factor at priority level 2 is retained. When the priority level 1 conversion is completed, the priority level 2 conversion is started automatically.
- When a startup of scan conversion occurs during priority level 1 conversion
  The start factor of the scan conversion is retained. When the priority level 1 conversion is completed, the scan conversion operation is started automatically.
- When a startup of scan conversion occurs during priority level 2 conversion
  The start factor of the scan conversion is retained. When the priority level 2 conversion is completed, the scan conversion operation is started automatically.
- While priority conversion is performed, start factor at the same priority level are masked (the operation is
  not restarted).

State Transitions

Figure 3-5 12-bit A/D Converter State Transitions



The operation states can be read from the PCNS, PCS, and SCS bits of the ADSR register.

Table 3-2 Correspondence between Bits and Operation States

PCNS	PCS	SCS	Explanation of states
0	0	0	Standby for A/D conversion.
0	0	1	Scan A/D conversion is in progress.
0	1	0	Priority A/D conversion (priority level 1 or 2) is in progress.
0	1	1	Priority A/D conversion (priority level 1 or 2) is in progress. Scan conversion is pending.
1	1	0	Priority A/D conversion (priority level 1) is in progress. Priority conversion (priority level 2) is pending.
1	1	1	Priority A/D conversion (priority level 1) is in progress. Scan conversion and priority conversion (priority level 2) are pending.

3.3 FIFO Operations

The A/D converter has 16 FIFO stages for scan conversion and 4 FIFO stages for priority conversion. When conversion data is written in the specified count of FIFO stages, an interrupt is generated to the CPU.

3.3.1. FIFO Operations in Scan Conversion

3.3.2. Interrupts in Scan Conversion

3.3.3. FIFO Operations in Priority Conversion

3.3.4. Interrupts in Priority Conversion

3.3.5. Validity of FIFO Data

3.3.6. Bit placement Selection for FIFO Data Registers

3.3.1 FIFO Operations in Scan Conversion

This section explains FIFO operations in scan conversion.

Sixteen FIFO stages are incorporated for writing scan conversion data. After reset, they are in empty state and the SEMP bit in the Scan Conversion Control Register (SCCR) is set to 1. When A/D conversion of one channel is completed, the conversion result, start factor, and conversion channel are written in the first FIFO stage. This resets SEMP bit to 0. The conversion result, start factor, and conversion channel for the next channel are written sequentially in the second FIFO stage.

When such data is written in all of the 16 stages, the SFUL bit is set to 1 to indicate that FIFO is in full state. If conversion is performed and an attempt is made to write data in FIFO when FIFO is in full state, the SOVR bit is set to 1 and the data is discarded (cannot overwrite the existing data).

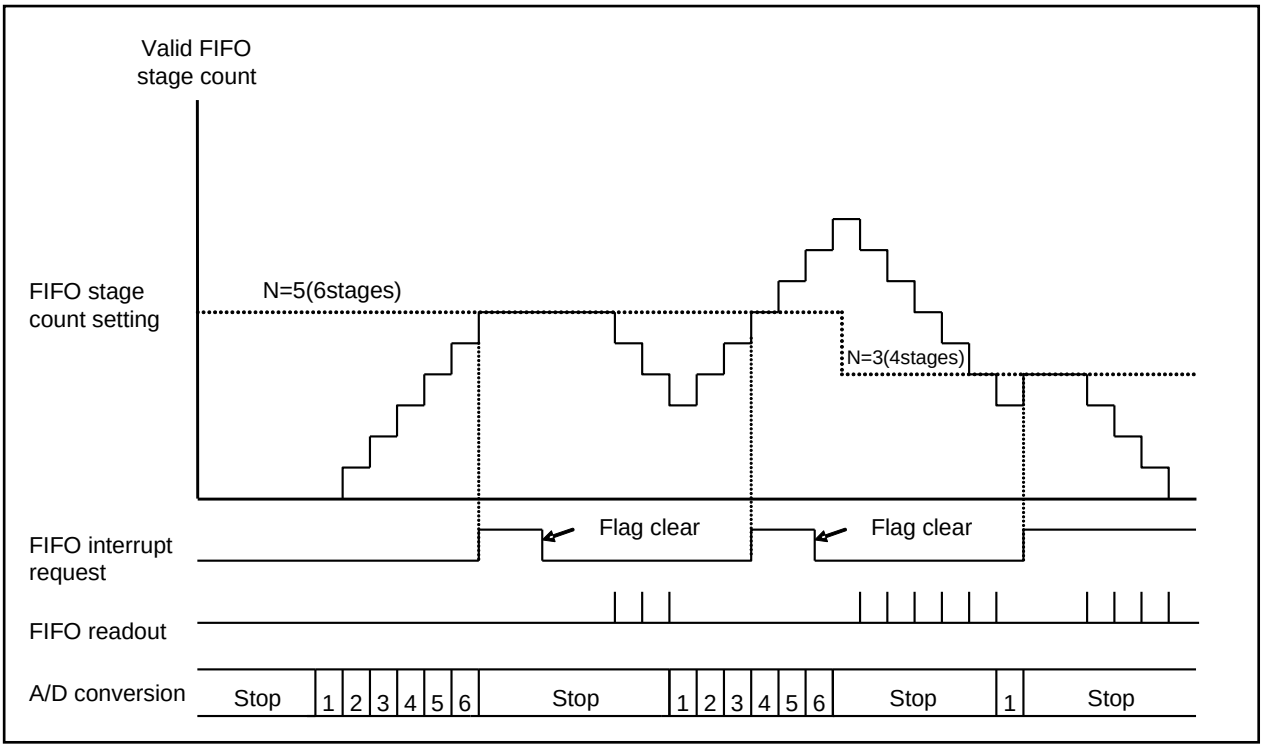
To clear the data in FIFO, set the SFCLR bit in the Scan Conversion Control register to 1. FIFO goes to the empty state and the SEMP bit is set to 1.

Data in FIFO can be read sequentially by reading the Scan Conversion FIFO Data Register (SCFD). To perform a byte (8 bits) access to this register, read the most significant byte (bit31:24) to shift FIFO (reading the other bytes (bit23:16, bit15:8, bit7:0) does not shift FIFO). To perform a half word (16 bits) access to this register, read the most significant half word (bit31:16) to shift FIFO (reading the other byte (bit15:0) does not shift FIFO). Performing a word (32 bits) access to this register shifts FIFO.

3.3.2 Interrupts in Scan Conversion

This section explains interrupts in scan conversion.

Figure 3-6 FIFO Interrupt Settings and FIFO Operations



When conversion data for the number of FIFO stages (N + 1) set in SFS[3:0] in the Scan Conversion FIFO Stage Count Setup Register (SFNS) is written in FIFO, the interrupt request bit (SCIF) in the A/D Control Register (ADCR) is set to 1. If the interrupt enable bit (SCIE) is set to 1, an interrupt request is generated to the CPU.

The following explains FIFO stage count interrupt methods for each scan conversion mode.

1. One-shot mode for a single channel

   To generate an interrupt after the completion of one conversion process for the specified channel, set SFS[3:0] = 0x0. When conversion data is written in the first FIFO stage, SCIF bit is set to 1.

Note:

- *If SFS[3:0] bits are set to 0x1 or more (two stages or more), interrupts are not generated until conversion data is written into FIFO by the specified stage count.*

2. Continuous mode for a single channel

   To generate an interrupt after the completion of one conversion process for the specified channel, set SFS[3:0] = 0x0. When conversion data is written in the first FIFO stage, SCIF bit is set to 1.

To generate an interrupt at the completion of a number of times of conversion of the specified channel, set SFS[3:0] bits to 0x1 or more (two stages or more). For example, set SFS[3:0] = 0x3 to generate an interrupt after four repeats.

3. One-shot mode for multiple channels

   To generate an interrupt after the completion of conversion of the multiple specified channels, set the FIFO stage count according to the number of channels. If eight channels are selected, set the FIFO stage count by setting SFS[3:0] = 0x7. When the conversion of the last one of the selected channels is completed, SCIF bit is set to 1.
   An interrupt can be generated at any timing before scan completion by setting SFS[3:0] bits to a value less than the number of selected channels.

4. Continuous mode for multiple channels

   To generate an interrupt after the completion of the first scan of the multiple specified channels, set the FIFO stage count according to the number of channels. If eight channels are selected, set the FIFO stage count by setting SFS[3:0] = 0x7. When the conversion of the last one of the selected channels is completed, SCIF bit is set to 1.
   To generate an interrupt after the completion of the second scan, set the FIFO stage count to twice the number of selected channels. For example, when four channels are selected, set the FIFO stage count to 8 (SFS[3:0] = 0x7). An interrupt is generated when the second scan is completed.
   Because the FIFO stage count can be set to any value, an interrupt can be generated at any desired timing.

3.3.3 FIFO Operations in Priority Conversion

This section explains FIFO operations in priority conversion.

Four FIFO stages are incorporated for writing priority conversion data. After reset, they are in empty state and the PEMP bit in the Priority Conversion Control Register is set to 1. When one A/D conversion process is completed, the conversion result, start factor, and conversion channels are written in the first FIFO stage. This resets SEMP bit to 0. The conversion result and conversion channels for the subsequent conversion processes are written in the corresponding FIFO stages.

When such data is written in all of the 4 stages, the PFUL bit is set to 1 to indicate that FIFO is in full state. If conversion is performed and an attempt is made to write data in FIFO when FIFO is in full state, the POVR bit is set to 1 and the data is discarded (cannot overwrite the existing data).

To clear the data in FIFO, set the PFCLR bit in the Priority Conversion Control Register (PCCR) to "1". FIFO goes to the empty state and the PEMP bit is set to 1.

Data in FIFO can be read sequentially by reading the Priority Conversion FIFO Data Register (PCFD). To perform byte (8 bits) access to this register, read the most significant byte (bit31:24) to shift FIFO (reading the other bytes (bit23:16, bit15:8, bit7:0) does not shift FIFO). To perform a half word (16 bits) access to this register, read the most significant half word (bit31:16) to shift FIFO (reading the other byte (bit15:0) does not shift FIFO). Performing a word (32 bits) access to this register shifts FIFO.

3.3.4 Interrupts in Priority Conversion

This section explains interrupts in priority conversion.

When conversion data for the number of FIFO stages (N + 1) set in PFS[1:0] in the Priority Conversion FIFO Stage Count Setup Register (PFNS) is written in FIFO, the interrupt request bit (PCIF) in the A/D Control Register (ADCR) is set to 1. If the interrupt enable bit (PCIE) is set to "1", an interrupt request is generated to the CPU.

The following explains FIFO stage count interrupt methods in priority conversion.

To generate an interrupt after the completion of one conversion process for the specified channel, set PFS[1:0] = 0x0. When conversion data is written in the first FIFO stage, PCIF bit is set to 1.

Note:

- *If PFS[1:0] bits are set to 0x1 or more (two stages or more), interrupts are not generated until conversion data is written into FIFO by the specified stage count.*

3.3.5 Validity of FIFO Data

This section explains a restriction on reading FIFO data registers.

The bit12 of the Scan Conversion FIFO Data Register (SCFD) and Priority Conversion FIFO Data Register (PCFD) comes with the INVL (A/D conversion result disable) bit which indicates data validity. During reading FIFO data registers, the INVL bit is cleared to 0 if data is valid while the INVL bit is set to 1 if data is invalid.

For word (32 bits) reading, data validity can be checked by the INVL bit.

For half word (16 bits) reading which does not use interrupts or empty bits (SEMP, PEMP), always start reading from the least significant 16 bits including the INVL bit. If the INVL bit is 1 at this time, reading the most significant 16 bits is prohibited. The most significant 16 bits must be read only when the INVL bit is 0.

For byte (8 bits) reading which does not use interrupts or empty bits (SEMP, PEMP), always start reading from bit15:8 including the INVL bit. If the INVL bit is 1 at this time, reading bit31:24, bit23:16, or bit7:0 is prohibited. They must be read only when the INVL bit is 0.

3.3.6 Bit placement Selection for FIFO Data Registers

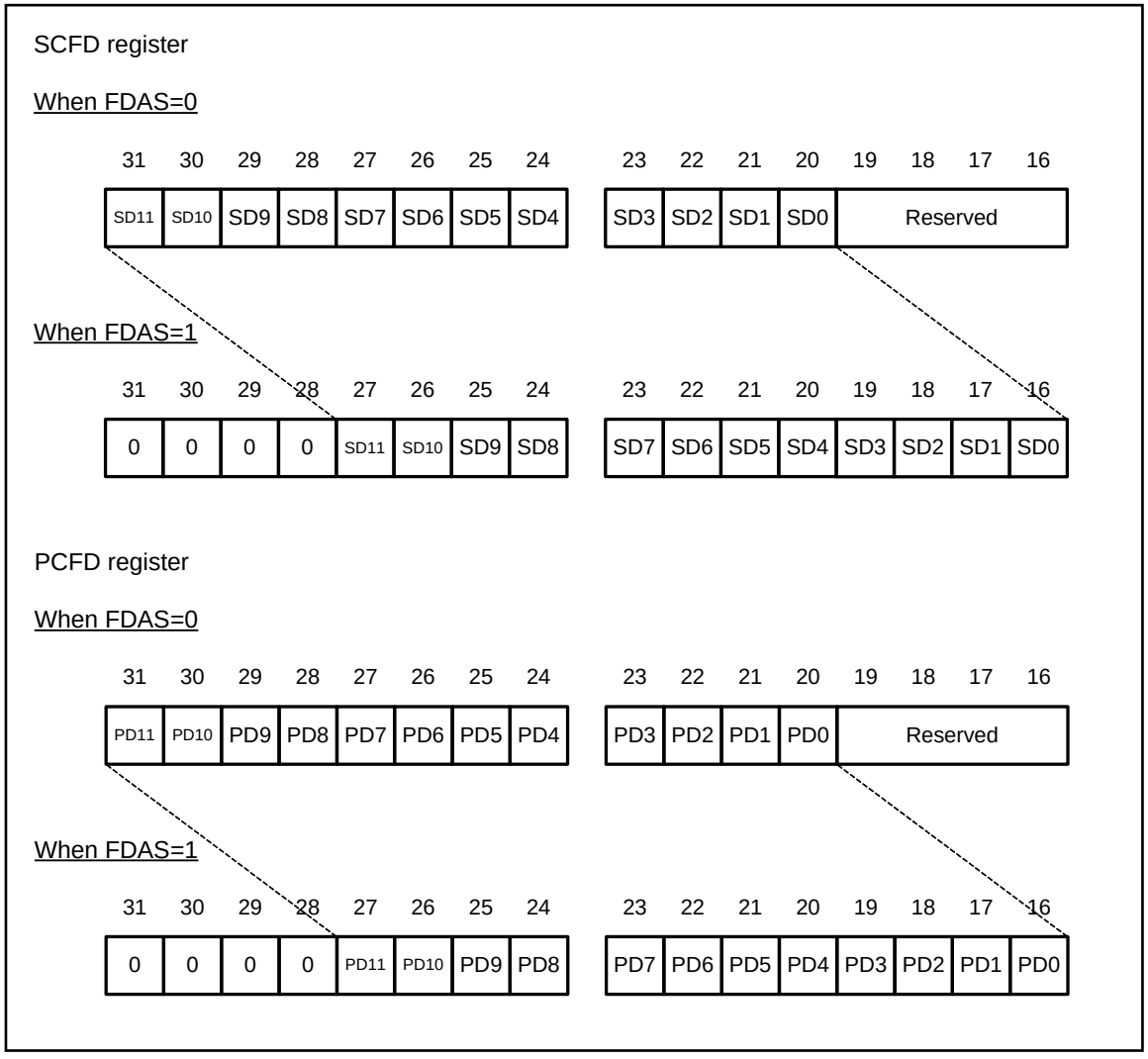
This section explains bit placement selection for FIFO data registers.

The A/D converter can change the bit placement for the conversion results in the Scan Conversion FIFO Data Register (SCFD) and Priority Conversion FIFO Data Register (PCFD) with the FDAS bit in the A/D Status Register (ADSR) (Figure 3-7).

Setting the FDAS bit to 1 places 12-bit A/D conversion results (SD11 to SD0, PD11 to PD0) on the LSB side (bit27:16) when a FIFO data register is read. Placement of the least significant 16 bits of a FIFO data register does not change.

FIFO is shifted, regardless of the set value of the FDAS bit, by reading bit31:24 (for a byte access), bit31:16 (for a half word access), or bit31:0 (for a word access) of a FIFO data register.

Figure 3-7 FIFO Data Register Bit Placement



3.4 A/D Comparison Function

The A/D comparison function compares A/D conversion results and generates interrupts.

To use the comparison function, set the CMPEN bit in the A/D Comparison Control Register (bit7 in the CMPCR register) to 1.

The values set in the A/D Comparison Value Setup Register (CMPD) are compared with the most significant 10 bits (bit11:2) of the A/D conversion result. If the comparison result satisfies the conditions set in the A/D Comparison Control Register (CMPCR), the A/D comparison interrupt bit (CMPIF) in the ADCR register is set to 1. If the interrupt enable bit (CMPIE) is 1, an interrupt is generated to the CPU.

Note:

- *Two bits (bit1:0) on the LSB side are not compared.*

Because the result of A/D conversion, regardless of scan or priority, is compared before it is written to FIFO, comparison is possible when FIFO is full.

If CMD1 bit is set to 1 (to generate an interrupt when the result is equal to or more than the CMPD set value), CMPIF is set to 1 when the conversion result is equal to the value in the A/D Comparison Value Setup Register (CMPD).

3.5 Range Comparison Function

The range comparison function is a function to determine whether the conversion result of the A/D converter is within or outside the specified range and generate an interrupt.

To start the range comparison function, write 1 to the range comparison enabling setting (RCOE) of Range Comparison Control Register (WCMPCR).

The upper 10 bits (bit11:2) of the A/D conversion result is compared with the upper threshold setting register (WCMPDH) and the lower threshold setting register (WCMPDL).

Note:

- *The comparison with two bits (bit1, bit0) on LSB side is not executed.*

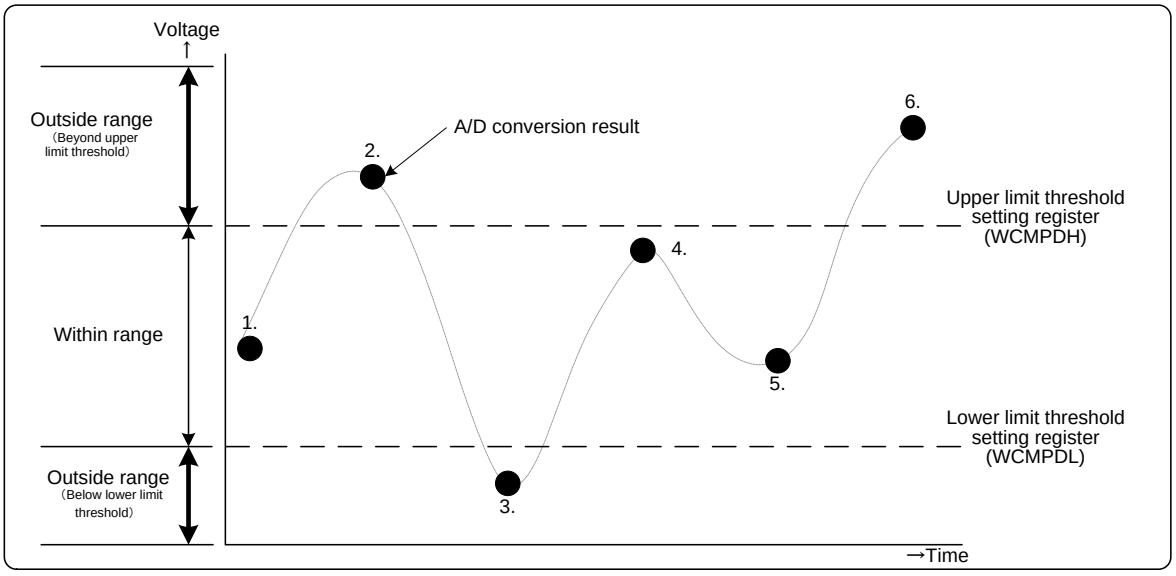
When the within-range /outside-range confirmation select (RCOIRS) of Range Comparison Control Register is 1, the A/D conversion result is confirmed to be outside of the specified range.

Table 3-3 shows the detection conditions of the range comparison and Figure 3-8 shows the operation of the range comparison.

Table 3-3 Range Comparison Conditions

Range Comparison Result	Outside-Range Confirmation (RCOIRS="0")	Within-Range Confirmation (RCOIRS="1")	Remarks
Outside range (beyond upper limit threshold) A/D data bit > upper limit threshold setting register	Detected	Not Undetected	Figure 3-8：2,6
Within Range A/D data bit ≥ lower limit threshold setting register And, A/D data bit ≤ upper limit threshold setting register	Not detected	Detected	Figure 3-8：1,4,5
Outside range (below lower limit threshold) A/D data bit < lower limit threshold setting register	Detected	Not detected	Figure 3-8：3

Figure 3-8 Range Comparison Operation



The Continuous detection function detects the range comparison continuously, and removes the noise etc. When the range comparison is continuously detected for the times specified in continuous detection count specification and state setting (RCOCD) of the range comparison control register (WCMPCR), the range comparison flag register (RCINT) is set to 1. When the range comparison interrupt enable bit (RCOIE) is set to "1", the interrupt is generated for CPU.

When the range comparison result is found to be undetected even one time in the continuous detection, the continuous detection measurement is cleared to 0 times, and restarts the measurement.

For the continuous detection conditions, see Table 3-4.

Table 3-4 Continuous Detection Conditions

Items	Descriptions
Continuous detection measurement operation	The detection is always operated whenever the continuous comparison execution enable setting (RCOE) is set to "1".
Continuous detection count	− With the continuous detection count specification (RCOCD), the detection count can be selected from 1 to 7 times. − With the continuous detection count status display (RCOCD), the state of the detection count can be confirmed.
Clear conditions	− When the range comparison execution enable setting (RCOE) is set to "0". − When the result is undetected with the range comparison result.
Increment condition	When the result is detected with the range comparison result. However, when the detection count reaches the continuous detection count specification (RCOCD), the detection is stopped at the continuous detection count specification value

Note:

- *When the confirmation of outside-range (WCMPCR.RCOIRS) is 0, the continuous detection measurement is not cleared to 0 times, and continues the continuous detection even if the range comparison result is changed from the state of the upper limit threshold excess to the state of below lower limit threshold.*

To initialize the state of the continuous detection count of the range comparison result, disable the range comparison while A/D conversion is not required, and then enable the range comparison again.

When the confirmation of outside-range of the range comparison (RCOIRS) is "0",the state of the upper limit threshold excess or the state of below lower limit threshold can be confirmed with the range comparison threshold excess flag bit (RCOOF).

For the judgment conditions of the Range Comparison Threshold Excess Flag, see Table 3-5.

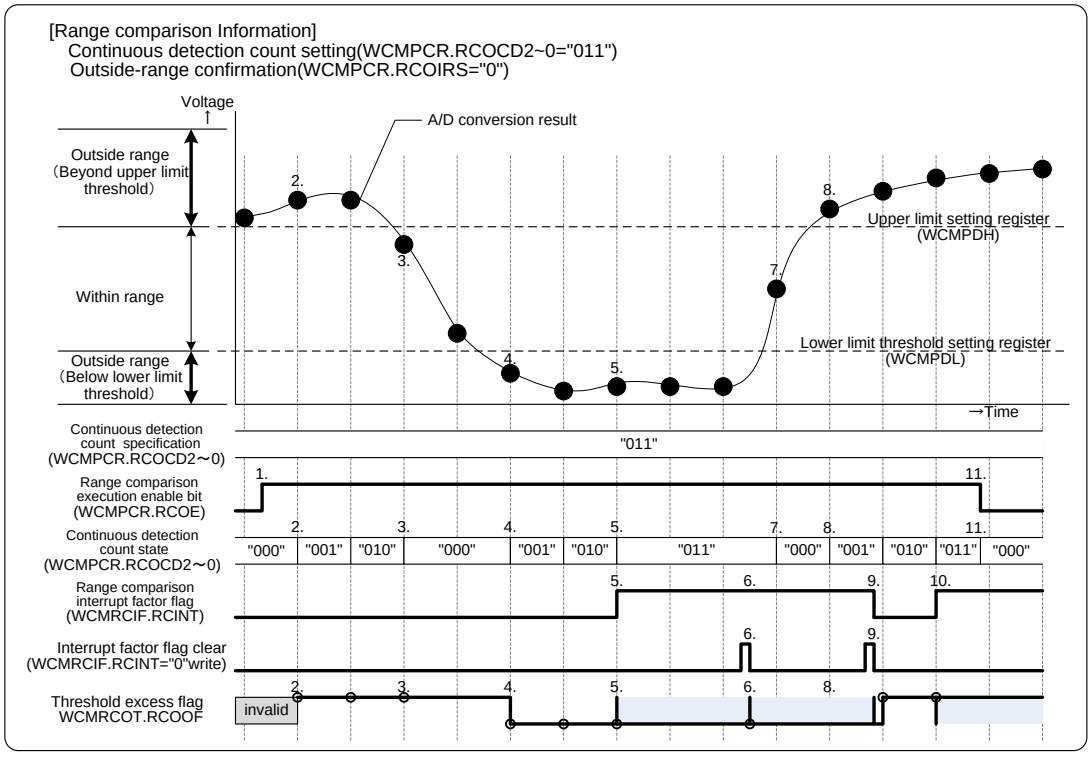
Table 3-5 Range Comparison Threshold Excess Flag, Judgment Conditions

Range Comparison Result	Range Comparison Threshold Excess Flag Bit(RCOOF)	
	Outside-range confirmed (RCOIRS="0")	**Within-range confirmed (RCOIRS="1")**
Outside range (beyond upper limit threshold) A/D data bit > upper limit threshold setting register	"1"	Prior value held
Within Range A/D data bit ≥ lower limit threshold setting register And, A/D data bit ≤ upper limit threshold setting register	Prior value held	Prior value held
Outside range (below lower limit threshold) A/D data bit < lower limit threshold setting register	"0"	Prior value held

Moreover, the range comparison threshold excess flag bit (RCOOF) holds the content set in itself while the comparison interrupt factor flag (RCINT) is set to 1.

For the operation example of the range comparison function, see Figure 3-9.

Figure 3-9 Range Comparison Function Operation Example



The explanation of range comparison function operation in Figure 3-9 is as follows:

1. When the range comparison execution disable setting (RCOE) is 0, the continuous detection count state (RCOCD) is initialized to 000.
   When the range comparison execution disable setting (RCOE) is set to 1, the range comparison operation is started.
2. When the range comparison result exceeds the upper limit threshold , the continuous count detection state (RCOCD) begins to increment.
   Moreover, the threshold excess flag notifies the upper limit threshold excess (RCOOF=1).
3. Before the continuous detection count specification value (RCOCD) becomes 011, the range comparison result is found to be within the range. So, the continuous detection count state (RCOCD) is initialized to be 000.
   Furthermore, the threshold excess flag (RCOOF) holds the prior value.
4. Because the range comparison result is below the lower limit threshold, the continuous count detection state (RCOCD) executes the increment.
   And, the threshold excess flag notifies that the result is below the lower limit threshold (RCOOF=0).
5. As the range comparison result reaches continuously the continuous detection count specification value (RCOCD =011), the range comparison interrupt factor flag (RCINT) is set to be 1.
   Moreover, the threshold excess flag (RCOOF) sets the threshold excess state where the range

comparison interrupt factor flag is set (RCINT=1) and holds the state until the range comparison interrupt factor flag is cleared (RCINT=0).

6. The set operation by the state of the continuous detection is given priority when the state of the range comparison interrupt factor flag clear (RCINT=0) and the state of the continuous detection compete. The range comparison interrupt factor flag is set (RCINT=1) and the threshold excess flag (RCOOF) set to the threshold excess state again.
7. When the range comparison result is within the range, even in the state of the range comparison interrupt factor flag set (RCINT=1), the state of the continuous detection frequency is initialized (RCOCD =000).
8. Even in the range comparison interrupt factor flag set state (RCINT=1), the range comparison result increments the continuous count detection (RCOCD2) by the upper limit threshold excess. However, in the range comparison interruption factor flag set state (RCINT=1), the threshold excess flag (RCOOF) holds the prior value.
9. The range comparison interrupt factor flag is cleared (RCINT=0) because of the range comparison interrupt factor flag clear (RCINT=0).
   Moreover, the hold state of the limit excess flag (RCOOF) is also released.
10. Because the range comparison result continuously reached the continuous detection count specification value (RCOCD =011), the range comparison interrupt factor flag (RCINT) is set to 1. Moreover, the threshold excess flag (RCOOF) is set to the threshold excess state when the range comparison interrupt factor flag is set (RCINT=1) and its state is held until the range comparison interrupt factor flag is cleared (RCINT=0).
11. When the range comparison operation is disabled (RCOE=0), the continuous detection count state (RCOCD) is initialized to 000.
    Moreover, neither the range comparison interrupt factor flag (RCINT) nor the threshold excess flag (RCOOF) are cleared because the range comparison operation is disabled (RCOE=0).

However, because the range comparisons of the A/D conversion results are implemented before A/D conversion result is written to FIFO regardless of the scanning conversion and the priority conversion, the range comparison can be executed even when FIFO is in the FULL state.

3.6 Starting DMA

This section explains the DMA transfer processing for FIFO data of A/D converter.

Data stored in FIFO of A/D converter can be transferred with the hardware activated DMA transfer using interrupt signals. The required settings and operations are as follows.

This product is compatible with DMA transfers of scan convert FIFO data by DMAC, and scan convert FIFO data and prior convert FIFO data by DSTC.

・The interrupt signal from the A/D converter is connected to the interrupt controller in the initial state. According to the select register setting for DMA transfer requests of interrupt controller and the DREQENB register setting of DSTC, connect the scan convert interrupt signal and prior convert interrupt signal to DMAC/DSTC. Enables interrupts from the A/D converter. (ADCR:SCIE=1, ADCR:PCIE=1)

・Set 0 for the FIFO stage count when the interrupts from the A/D converter are generated (the interrupt request will be generated when the conversion result is stored in the first FIFO stage).

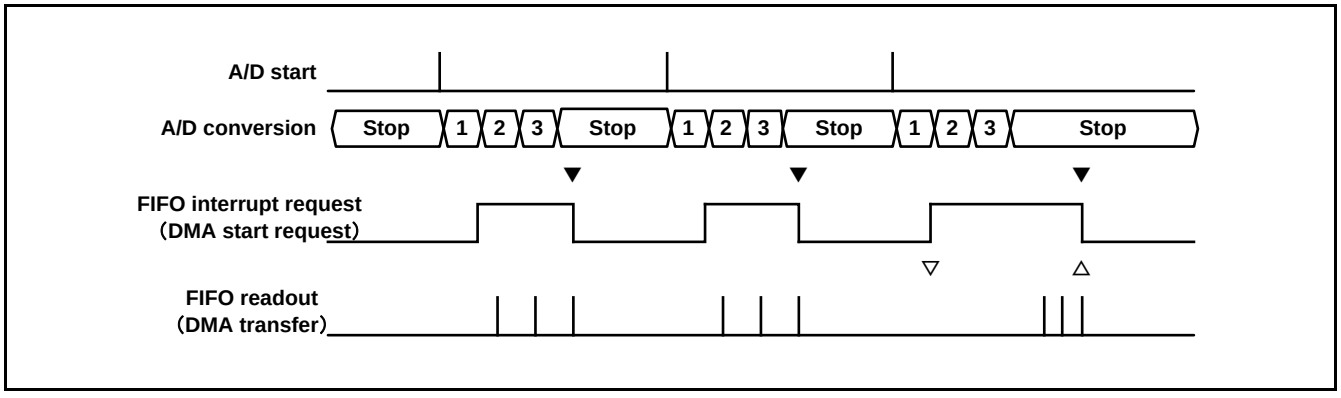
・For DMAC/DSTC side, specify the transfer source addresses for the scan convert FIFO data register (SCFD) and prior conversion FIFO data register (PCFD). In case of DMAC, select the hardware demand transfer for transfer mode. In case of DSTC, select DES0.MODE=1 for transfer mode. For number of transfer, specify the number of data stored in FIFO.

Figure 3-10 shows a timing chart of DMA transfer operations.

After A/D conversion is started, the converted data will be stored in FIFO. Interrupt requests from the A/D converter are generated. By DMAC/DSTC, reading the FIFO data register and writing to the destination are performed, and data transfer is performed. The generated interrupt signals are cleared from the DMAC/DSTC side. (▼mark in this figure) Clearing the interrupt flag (ADCR:SCIF, ADCR:PCIF) from CPU is not required. After transfer operation is completed for the times specified in DMAC/DSTC, the transfer completion notification from DMAC/DSTC can be received.

If DMAC/DSTC processes transfer requests other than those of the A/D converter, note that the start of DMA transfer may get delayed as shown from ▽ to △ in the figure.

Figure 3-10 DMA transfer Operation



4. Setup procedure Examples

This section provides examples of setup procedures for the 12-bit A/D converter.

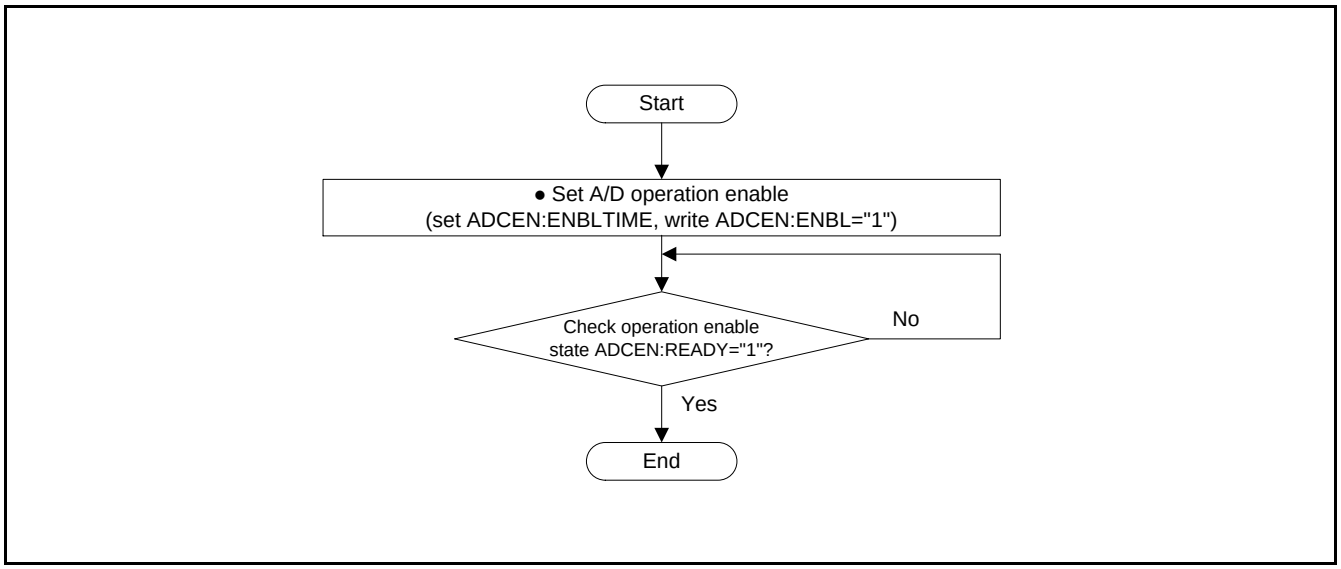
4.1. A/D Operation Enable Setup Procedure Example
4.2. Scan Conversion Setup Procedure Example
4.3. Priority Conversion Setup Procedure Example
4.4. Range Comparison Function Setting Example
4.5. Setting Conversion Time

4.1 A/D Operation Enable Setup Procedure Example

This section provides an A/D operation enable setup procedure example.

- Set the period of operation enable state transitions
- Poll the operation enable state

Figure 4-1 A/D Operation Enable Setup Procedure Example

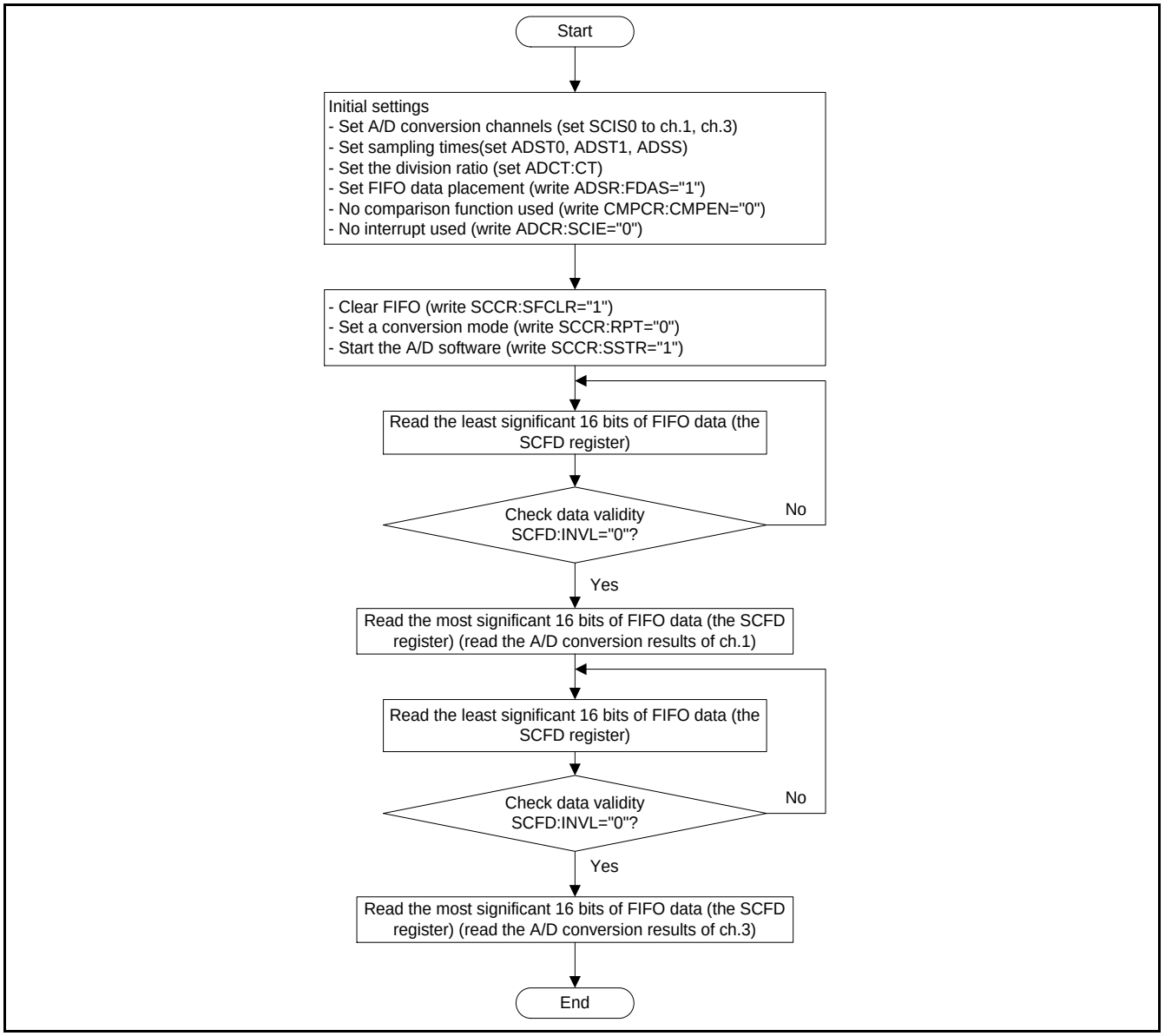


4.2 Scan Conversion Setup Procedure Example

This section provides a scan conversion setup procedure example.

- Scan conversion by software startup
- Set A/D conversion channels to ch.1 and ch.3
- Set different sampling times for ch.1 and ch.3
- Set the clock division ratio
- Read the least significant 16 bits of FIFO data and check data validity by the INVL bit
- After checking that data is valid, read the most significant 16 bits of FIFO data

Figure 4-2 Scan Conversion Setup Procedure Example

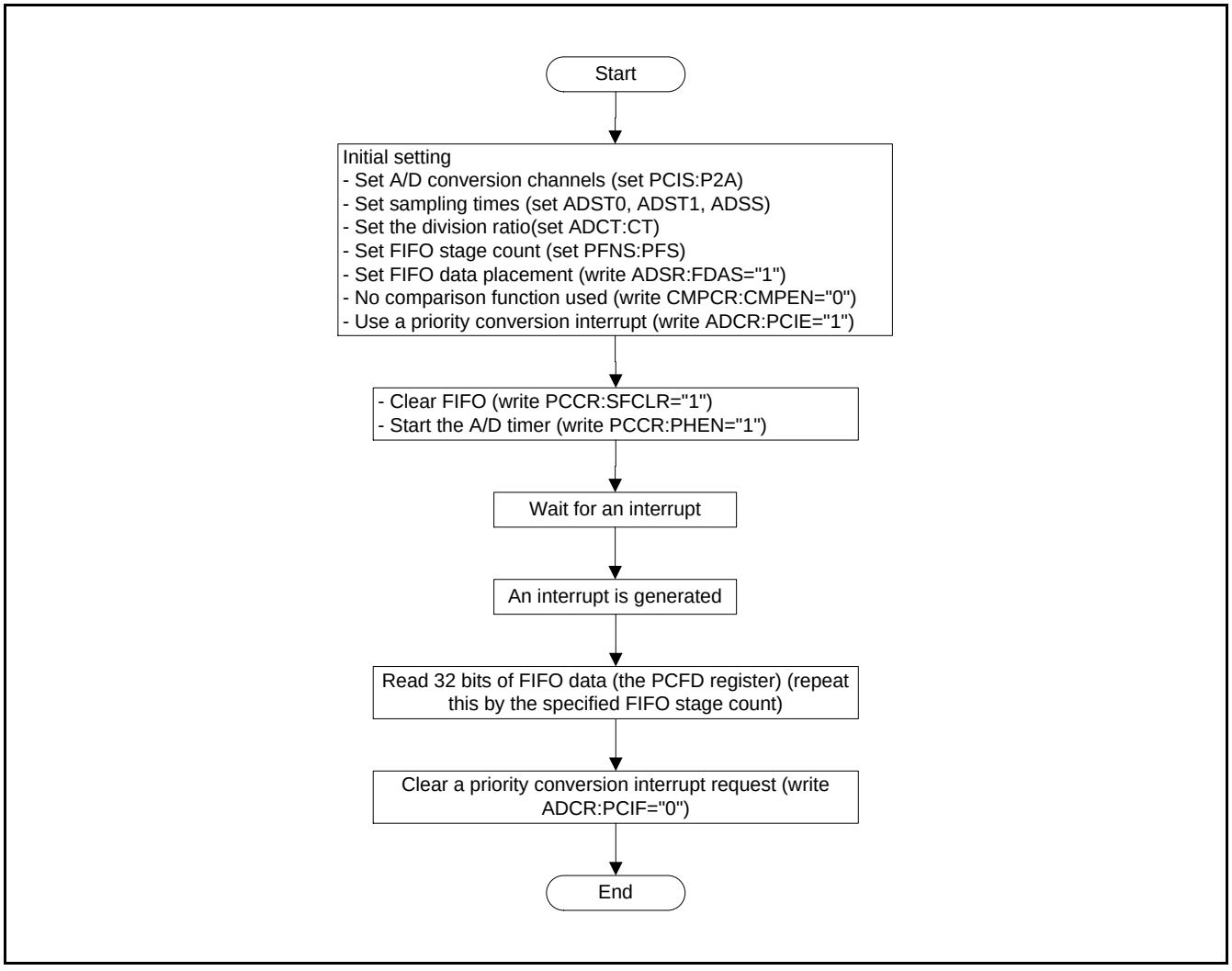


4.3 Priority Conversion Setup Procedure Example

This section provides a priority conversion setup procedure example.

- Priority conversion at priority level 2 by timer start
- Conversion channels are ch.1 and ch.3
- Set different sampling times for ch.1 and ch.3
- Set the clock division ratio
- Read 32 bits of FIFO data by using an interrupt
- Read FIFO by the specified stage count

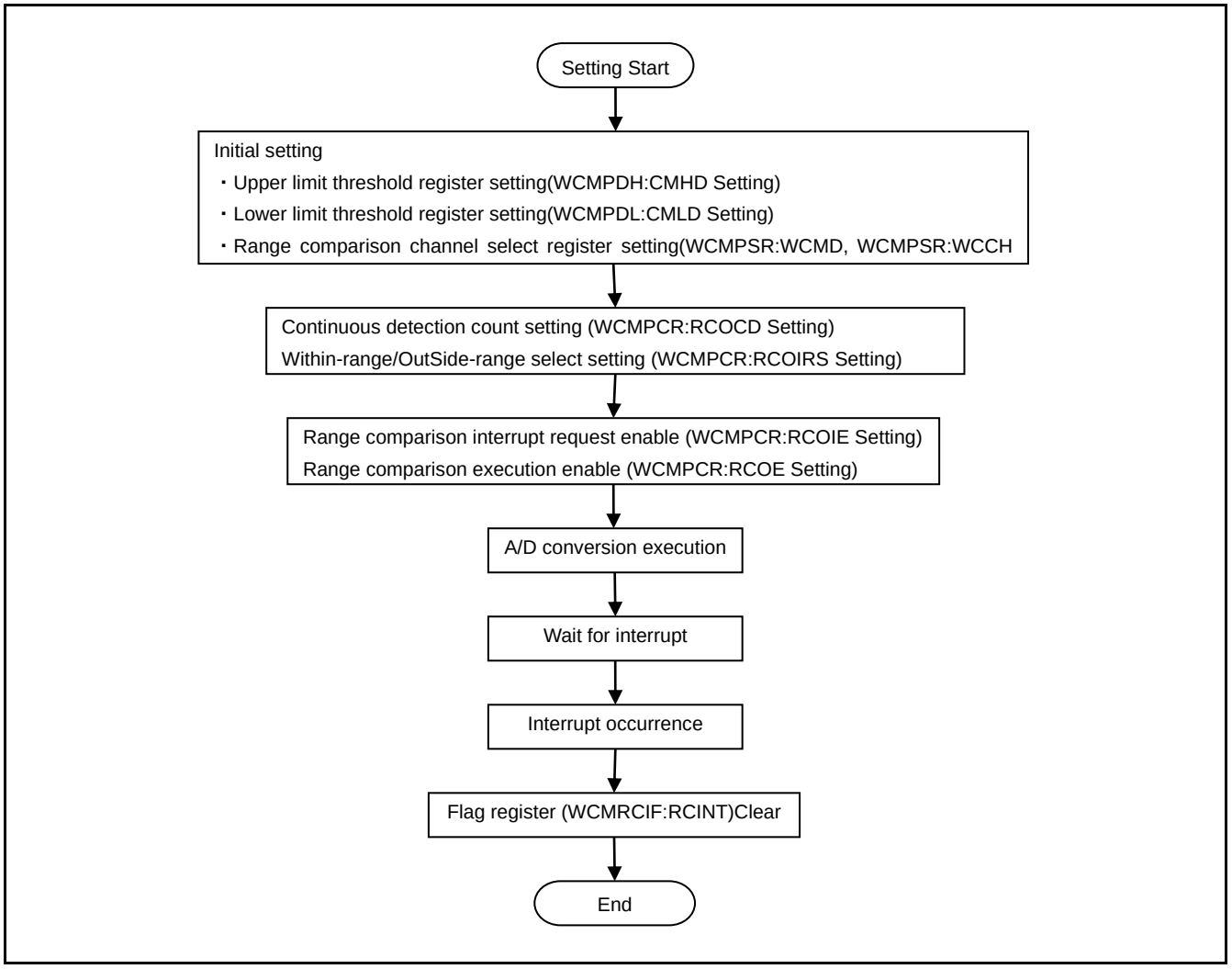
Figure 4-3 Priority Conversion Setup Procedure Example



4.4 Range Comparison Function Setting Example

This section shows the example of range comparison function setting procedures.

Figure 4-4 Example of Comparison Function Setting Procedures



4.5 Setting Conversion Time

The conversion time of the A/D converter is "sampling time" + "comparison time". Two sampling time settings can be applied to each channel. This section explains how to set and calculate the conversion time.

Example of Setting the Sampling Time

A sampling time is set in each of Sampling Time Setup Registers 0 and 1 (ADST0 and ADST1). Using Sampling Time Selection Registers (ADSS3 to ADSS0), whether Sampling Time Setup Registers 0 or 1 is used to provide the value can be selected for each channel. This allows you to set different sampling times for channels with different external impedances.

Sampling time = Base clock (HCLK) cycle× Clock division ratio × {(ST set value + 1) × STX setting multiplier + 3}

Notes:

- *For setting the sampling time, refer to the "Electrical Characteristics" in the "Data Sheet" to make sure that an appropriate time should be selected in accordance with an external impedance of an input channel, an analog power supply voltage (AVCC), and a base clock (HCLK) cycle.*
- *When STXx2, STXx1, and STXx0 = 000 (STx4 to STx0 set values multiplied by 1) are set, set STx4 to STx0 to "2" or more ("1" or less must not be set).*

Example of Setting the Comparison Time

The comparison time is set in the Comparison Time Setup Register (ADCT).

Comparison time = Compare clock cycle × 14
Compare clock cycle = Base clock (HCLK) cycle × Clock division ratio

Notes:

- *For setting the compare clock cycle, refer to the "Electrical Characteristics" in the "Data Sheet" to make sure that an appropriate time should be selected in accordance with an analog power supply voltage (AVCC) and a base clock (HCLK) cycle.*
- *If the sampling time or compare clock cycle fails to meet the electrical characteristics of the A/D converter, the A/D conversion accuracy may be degraded.*

Example of Conversion Time Calculation (when HCLK = 20 MHz (50 ns cycle))

(1) Sampling time

- When ST04 to ST00 = 2, STX02, STX01, and STX00 = 000 (multiplied by 1), and CT7 to CT0=0 (Compare clock division ratio: 2)
- Sampling time = 50 ns × 2 ×{(2+1) × 1 + 3} = 600 ns
  When ST14 to ST10 = 19, STX12, STX11, and STX10 = 001 (multiplied by 4), and CT7 to CT0=0 (Compare clock division ratio: 2)
  Sampling time = 50 ns × 2 ×{(19 + 1) × 4 + 3} = 8300 ns

(2) Comparison time

- When CT7 to CT0 = 0 (Clock division ratio: 2)
  Compare clock cycle = 50 ns × 2 = 100 ns
  Comparison time = 100 ns × 14 = 1400 ns

(3) Conversion time

- By adding (1) and (2) together:
  Conversion time for channels specified with the ADST0 register = 2000 ns
  Conversion time for channels specified with the ADST1 register = 9700 ns

5. Registers

This section explains the configuration and functions of the registers used for the 12-bit A/D converter.

Table 5-1 List of Registers for the 12-bit A/D Converter

Abbreviation	Register name	Reference
ADCR	A/D Control Register	5.1
ADSR	A/D Status Register	5.2
SCCR	Scan Conversion Control Register	5.3
SFNS	Scan Conversion FIFO Stage Count Setup Register	5.4
SCFD	Scan Conversion FIFO Data Register	5.5
SCIS	Scan Conversion Input Selection Register	5.6
PCCR	Priority Conversion Control Register	5.7
PFNS	Priority Conversion FIFO Stage Count Setup Register	5.8
PCFD	Priority Conversion FIFO Data Register	5.9
PCIS	Priority Conversion Input Selection Register	5.10
CMPD	A/D Comparison Value Setup Register	5.11
CMPCR	A/D Comparison Control Register	5.12
ADSS	Sampling Time Selection Register	5.13
ADST	Sampling Time Setup Register	5.14
ADCT	Comparison Time Setup Register	5.15
ADCEN	A/D Operation Enable Setup Register	5.16
WCMPDH	Upper Limit Threshold Setting Register	5.17
WCMPCR	Range Comparison Control Register	5.18
WCMPDL	Lower Limit Threshold Setting Register	5.19
WCMPSR	Range Comparison Channel Select Register	5.20
WCMRCOT	Range Comparison Threshold Excess Flag Register	5.21
WCMRCIF	Range Comparison Flag Register	5.22

5.1 A/D Control Register (ADCR)

The A/D Control Register (ADCR) performs interrupt flag display and interrupt enable control.

bit	15	14	13	12	11	10	9	8
Field	SCIF	PCIF	CMPIF	Reserved	SCIE	PCIE	CMPIE	OVRIE
Attribute	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
Initial value	0	0	0	X	0	0	0	0

[bit15] SCIF: Scan conversion interrupt request bit

When conversion values are written up to the stage count specified in the Scan Conversion FIFO Stage Count Setup Register (SFNS), this bit is set to 1. The read value of Read-Modify-Write operation is 1 regardless of the bit value.

bit	Description	
	Read	Write
0	Conversion result is not stored.	Clears this bit.
1	Conversion result is stored.	No effect.

[bit14] PCIF: Priority conversion interrupt request bit

When conversion values are written up to the stage specified in the Priority Conversion FIFO Stage Count Setup Register (PFNS), this bit is set to 1. The read value of Read-Modify-Write operation is 1 regardless of the bit value.

bit	Description	
	Read	Write
0	Conversion result is not stored.	Clears this bit.
1	Conversion result is stored.	No effect.

[bit13] CMPIF: Conversion result comparison interrupt request bit

When the condition set in the A/D Comparison Value Setup Register (CMPD) or A/D Comparison Control Register (CMPCR) is satisfied during the operation of the A/D conversion result comparison function, this bit is set to 1. The read value of Read-Modify-Write operation is 1 regardless of the bit value.

bit	Description	
	Read	Write
0	Specified condition is not satisfied.	Clears this bit.
1	Specified condition is satisfied.	No effect.

[bit12] Reserved: Reserved bit

Writing has no effect on operation.
The read value is undefined.

[bit11] SCIE: Scan conversion interrupt enable bit

This bit controls the interrupt request of SCIF. When the SCIE bit is enabled, and the SCIF bit is set, an interrupt request to the CPU is generated.

bit	Description
0	Interrupt request disable
1	Interrupt request enable

[bit10] PCIE: Priority conversion interrupt enable bit

This bit controls the interrupt request of PCIF. When the PCIE bit is enabled, and the PCIF bit is set, an interrupt request to the CPU is generated.

bit	Description
0	Interrupt request disable
1	Interrupt request enable

[bit9] CMPIE: Conversion result comparison interrupt enable bit

This bit controls the interrupt request of CMPIF. When the CMPIE bit is enabled, and the CMPIF bit is set, an interrupt request to the CPU is generated.

bit	Description
0	Interrupt request disable
1	Interrupt request enable

[bit8] OVRIE: FIFO overrun interrupt enable bit

This bit controls the interrupt request of the SOVR bit in the SCCR register or the POVR bit in the PCCR register. When the OVRIE bit is enabled, and the SOVR or POVR bit is set, an interrupt request to the CPU is generated.

bit	Description
0	Interrupt request disable
1	Interrupt request enable

5.2 A/D Status Register (ADSR)

The A/D Status Register (ADSR) displays scan and priority conversion statuses.

bit	7	6	5	4	3	2	1	0
Field	ADSTP	FDAS	Reserved			PCNS	PCS	SCS
Attribute	R/W	R/W	-			R	R	R
Initial value	0	0	XXX			0	0	0

[bit7] ADSTP: A/D conversion forced stop bit

Setting the ADSTP bit to 1 stops the A/D conversion operation forcibly (both scan and priority conversion operations are stopped). Forced stop of A/D conversion initializes the PCNS, PCS, and SCS bits in the ADSR register to 0. However, other register bits are not reset.

bit	Description	
	Read	Write
0	The value is always "0".	No effect.
1		Stops the conversion operation forcibly.

[bit6] FDAS: FIFO data placement selection bit

Setting the FDAS bit to 1 shifts the Scan Conversion FIFO Data Register (SCFD) and Priority Conversion FIFO Data Register (PCFD) conversion result values by 4 bits to the LSB side, placing them in bit27:16. The position of the lower 16-bit of the FIFO data register does not change.

bit	Description
0	Places conversion result on the MSB side.
1	Places conversion result on the LSB side.

[bit5:3] Reserved: Reserved bits

Writing has no effect on operation.
The read value is undefined.

[bit2] PCNS: Priority conversion pending flag

This flag indicates that conversion at priority level 2 (software/timer) is pending. This flag is set when priority conversion at priority level 2 (software/timer) is started while priority conversion at priority level 1 (external trigger start) is performed or when conversion at priority level 1 is started while priority conversion at priority level 2 is performed. Writing is ignored.

bit	Description
0	Priority level 2 conversion is not pending.
1	Priority level 2 conversion is pending.

[bit1] PCS: Priority conversion status flag

This flag indicates that priority A/D conversion is in progress. This flag is set while priority conversion at priority level 1 or 2 is performed. Writing is ignored.

bit	Description
0	Priority conversion is stopped.
1	Priority conversion is in progress.

[bit0] SCS: Scan conversion status flag

This flag indicates that scan A/D conversion is in progress. Writing is ignored.

bit	Description
0	Scan conversion is stopped.
1	Scan conversion is in progress.

5.3 Scan Conversion Control Register (SCCR)

The Scan Conversion Control Register (SCCR) controls the scan conversion mode.

bit	15	14	13	12	11	10	9	8
Field	SEMP	SFUL	SOVR	SFCLR	Reserved	RPT	SHEN	SSTR
Attribute	R	R	R/W	R/W	-	R/W	R/W	R/W
Initial value	1	0	0	0	X	0	0	0

[bit15] SEMP: Scan conversion FIFO empty bit

This bit is set when FIFO goes to the empty state. When conversion data is written in the Scan Conversion FIFO Data Register (SCFD), this bit is set to 0. Writing is ignored.

bit	Description
0	Data remains in FIFO.
1	FIFO is empty.

[bit14] SFUL: Scan conversion FIFO full bit

This bit is set when FIFO goes to full state. When SFCLR is set to 1 or the Scan Conversion FIFO Data Register (SCFD) is read, this bit is set to 0. Writing is ignored.

bit	Description
0	Data can be input to FIFO.
1	FIFO is full.

[bit13] SOVR: Scan conversion overrun flag

This bit is set when an attempt to write data to a full FIFO is made (conversion data in a full FIFO is not overwritten). The read value of Read-Modify-Write operation is 1 regardless of the bit value. When the OVRIE bit in the ADCR register is 1 and the SOVR bit is 1, an interrupt is generated to the CPU.

bit	Description	
	Read	Write
0	No overrun has occurred.	Clears this bit.
1	Overrun has occurred.	No effect.

[bit12] SFCLR: Scan conversion FIFO clear bit

Setting this bit to 1 clears the scan conversion FIFO. FIFO becomes empty and the SEMP bit is set to 1.

bit	Description	
	Read	Write
0	The value is always "0".	No effect.
1		Clears FIFO.

[bit11] Reserved: Reserved bit

Writing has no effect on operation.
The read value is undefined.

[bit10] RPT: Scan conversion repeat bit

Setting this bit to 1 places the converter in the repeat mode. When the conversion of all analog input channels selected in the Scan Conversion Input Selection Register (SCIS) is completed, the conversion is started again.

Setting the RPT bit to 0 ends the repeat conversion. The operation stops when the conversion of the analog input channels selected in the SCIS bit is completed.

Setting the RPT bit to 1 must be performed while scan conversion is stopped (ADSR: SCS= 0). (Setting the SSTR bit to 1 may be performed simultaneously with setting the RPT bit to 1.)

bit	Description
0	Single conversion mode
1	Repeat conversion mode

Note:

- *The repeat transfer cannot be stooped immediately even when PRT bit is set to 0.*
  Writing data to FIFO will be continued until the transfer is stopped.
  Note that FIFO data and Status bits (FIFO full bit etc.) continue to change until the transfer is stopped.

[bit9] SHEN: Scan conversion timer start enable bit

Set this bit to 1 to start scan conversion using a rising edge from a timer. Software startup (SSTR = 1) is valid even when this bit is set to 1.

bit	Description
0	Timer start disable
1	Timer start enable

[bit8] SSTR: Scan conversion start bit

Setting this bit to 1 starts A/D conversion. Setting this bit to 1 again during conversion stops the ongoing conversion immediately and restarts the conversion.

bit	Description	
	Read	Write
0	The value is always "0".	No effect.
1		Starts conversion or restarts the conversion (during conversion).

Note:

- *If a startup by a timer occurs simultaneously with the setting of the SSTR bit to 1, the setting of the SSTR bit to 1 takes preference and the startup by the timer is ignored.*

5.4 Scan Conversion FIFO Stage Count Setup Register (SFNS)

The Scan Conversion FIFO Stage Count Setup Register (SFNS) sets up the generation of interrupt requests in scan conversion. When the specified count of FIFO stages store A/D conversion data, the interrupt request bit (SCIF) is set.

bit	7	6	5	4	3	2	1	0
Field	Reserved				SFS[3:0]			
Attribute	-				R/W			
Initial value	XXXX				0000			

[bit7:4] Reserved: Reserved bits

Writing has no effect on operation.
The read value is undefined.

[bit3:0] SFS[3:0]: Scan conversion FIFO stage count setting bits

When A/D conversion data for the FIFO stage count (N + 1) set in SFS[3:0] bits are written, the interrupt request flag (SCIF) is set to 1.

bit3:0	Description
0000	Generates an interrupt request when conversion result is stored in the first FIFO stage.
0001	Generates an interrupt request when conversion result is stored in the second FIFO stage.
0010	Generates an interrupt request when conversion result is stored in the third FIFO stage.
...	...
1101	Generates an interrupt request when conversion result is stored in the 14th FIFO stage.
1110	Generates an interrupt request when conversion result is stored in the 15th FIFO stage.
1111	Generates an interrupt request when conversion result is stored in the 16th FIFO stage.

5.5 Scan Conversion FIFO Data Register (SCFD)

The Scan Conversion FIFO Data Register (SCFD) consists of 16 FIFO stages and stores analog conversion results. Data can be retrieved sequentially by reading the register.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Field	SD 11	SD 10	SD 9	SD 8	SD 7	SD 6	SD 5	SD 4	SD 3	SD 2	SD 1	SD 0	Reserved			
Attribute	R												R			
Initial value	0xXXX												XXXX			

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Reserved			INVL	Reserved		RS 1	RS 0	Reserved			SC 4	SC 3	SC 2	SC 1	SC 0
Attribute	R			R	R		R		R			R				
Initial value	XXX			1	XX		XX		XXX			XXXXX				

[bit31:20] SD11 to SD0: Scan conversion result

The result of 12-bit scan A/D conversion is written.

[bit19:13] Reserved: Reserved bits

The read value is undefined.

[bit12] INVL : A/D conversion result disable bit

This bit is set when this register value is invalid.

bit	Description
0	This register value is valid
1	This register value is invalid

[bit11:10] Reserved: Reserved bits

The read value is undefined.

[bit9:8] RS1, RS0: Scan conversion start factor

The start factor of the scan conversion corresponding to this register value is shown.

bit9:8	Description
01	Software start
10	Timer start

[bit7:5] Reserved: Reserved bits

The read value is undefined.

[bit4:0] SC4 to SC0: Conversion input channel bits

The analog input channels corresponding to the conversion result written in SD11 to SD0 are written. Settings for channels not defined in the product specifications are not written. See the specified number of the analog input channels in the Data Sheet of each product.

bit4:0	Description
00000	ch.0
00001	ch.1
00010	ch.2
...	...
11101	ch.29
11110	ch.30
11111	ch.31

Notes:

- *This register has different bit configurations depending on the FDAS bit setting in the A/D Status Register (ADSR). When the FDAS bit is 1, see 3.3.6 Bit placement Selection for FIFO Data Registers.*
- *To perform a byte access to this register, read the most significant byte (bit31:24) to shift the FIFO data. Reading the other bytes (bit23:16, bit15:8, bit7:0) does not shift FIFO. To perform a half byte access to this register, read the most significant half byte (bit 31:16) to shift the FIFO data. Reading the other byte (bit15:0) does not shift FIFO. Performing a word access to this register shifts FIFO.*
- *If software and a timer are started simultaneously, 0b11 may be read from the RS[1:0] bits.*

5.6 Scan Conversion Input Selection Register (SCIS)

The Scan Conversion Input Selection Register (SCIS) is used to select analog input channels for which scan conversion is performed. Any channels can be selected from multiple analog inputs. The selected channels are converted in ascending order of channel number.

SCIS3 (most significant byte: AN31 to AN24) and SCIS2 (least significant byte: AN23 to AN16)

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	AN 31	AN 30	AN 29	AN 28	AN 27	AN 26	AN 25	AN 24	AN 23	AN 22	AN 21	AN 20	AN 19	AN 18	AN 17	AN 16
Attribute	R/W															
Initial value	0x00															

[bit15:0] AN31 to AN16: Analog input selection bits

When these bits are set to 1, the corresponding channels are selected for analog conversion.

SCIS1 (most significant byte: AN15 to AN8) and SCIS0 (least significant byte: AN7 to AN0)

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	AN 15	AN 14	AN 13	AN 12	AN 11	AN 10	AN 9	AN 8	AN 7	AN 6	AN 5	AN 4	AN 3	AN 2	AN 1	AN 0
Attribute	R/W															
Initial value	0x00															

[bit15:0] AN15 to AN0: Analog input selection bits

When these bits are set to 1, the corresponding channels are selected for analog conversion.

Notes:

- *It is not allowed to change the channels during A/D conversion. Be sure to set SCIS3 to SCIS0 while the A/D conversion is stopped. A/D conversion is not period of waiting start factors. It is allowed to change the channel during no start factors period.*
- *It is not possible to set 1 in the bit corresponding to a channel that is not defined in the product specifications. See the specified number of the analog input channels in the Data Sheet of each product.*

Example of Scan Conversion Order

The selected channels are converted in ascending order of channel number.

Example : When the AN1, AN3, AN5, and AN23 bits are set to 1, the analog conversion proceeds from ch.1, ch.3, ch.5, and to ch.23.

5.7 Priority Conversion Control Register (PCCR)

The Priority Conversion Control Register (PCCR) controls the priority conversion mode.

Priority conversion can be performed even while scan conversion is being performed.

In addition, different priority levels (two levels) can be given to priority conversion processes.

bit	15	14	13	12	11	10	9	8
Field	PEMP	PFUL	POVR	PFCLR	ESCE	PEEN	PHEN	PSTR
Attribute	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	0	0	0	0	0	0	0

[bit15] PEMP: Priority conversion FIFO empty bit

This bit is set when FIFO goes to the empty state. When conversion data is written in the Priority Conversion FIFO Data Register (PCFD), this bit is set to "0". Writing is ignored.

bit	Description
0	Data remains in FIFO.
1	FIFO is empty.

[bit14] PFUL: Priority conversion FIFO full bit

This bit is set when FIFO goes to full state. When PFCLR bit is set to "1" or the Priority Conversion FIFO Data Register (PCFD) is read, this bit is set to 0. Writing is ignored.

bit	Description
0	Data can be input to FIFO.
1	FIFO is full.

[bit13] POVR: Priority conversion overrun flag

This bit is set when an attempt to write data to a full FIFO is made (conversion data in a full FIFO is not overwritten). The read value of Read-Modify-Write operation is 1 regardless of the bit value. When the OVRIE bit in the ADCR register is 1, an interrupt is generated to the CPU if the POVR bit is 1.

bit	Description	
	Read	Write
0	No overrun has occurred.	Clears this bit.
1	Overrun has occurred.	No effect on operation.

[bit12] PFCLR: Priority conversion FIFO clear bit

Setting this bit to 1 clears the priority conversion FIFO. FIFO becomes empty and the PEMP bit is set to 1.

bit	Description	
	Read	Write
0	The value is always "0".	No effect on operation
1		Clears FIFO.

[bit11] ESCE: External trigger analog input selection bit

This bit selects whether the external trigger analog input is selected with the P1A[2:0] bits in the Priority Conversion Input Selection Register (PCIS) or the external input pin ECS[2:0] bits.

bit	Description
0	The external trigger analog inputs are selected with P1A[2:0].
1	The external trigger analog inputs are selected with an external input.

Notes:

- *It is not allowed to change the setting of the ESCE bit during A/D conversion. To change the setting, make sure the A/D conversion is stopped. A/D conversion is not period of waiting start factors. It is allowed to change the setting of the ESCE bit during no start factors period.*
- *If channel selection with external pins ECS[2:0] cannot be used due to the product specifications, be sure to set the ESCE bit to 0.*

[bit10] PEEN: Priority conversion external start enable bit

Set this bit to 1 to start priority conversion using a falling edge of an external trigger pin input. Conversion started with an external trigger has priority level 1 (highest priority).

bit	Description
0	External trigger start disable
1	External trigger start enable

[bit9] PHEN: Priority conversion timer start enable bit

Set this bit to 1 to start priority conversion using a rising edge from a timer. Software startup (PSTR = 1) is valid even when this bit is set to 1. Conversion started with an external trigger has priority level 2 (lower priority than level 1).

bit	Description
0	Timer start disable
1	Timer start enable

[bit8] PSTR: Priority conversion start bit

Setting this bit to 1 starts A/D conversion. Conversion started with this bit has priority level 2 (lower than priority level 1). It is not possible to restart the conversion started with this bit.

bit	Description	
	Read	Write
0	The value is always "0".	No effect on operation
1		Starts priority conversion.

5.8 Priority Conversion FIFO Stage Count Setup Register (PFNS)

The Priority Conversion FIFO Stage Count Setup Register (PFNS) sets up the generation of interrupt requests in priority conversion. When the specified count of FIFO stages store A/D conversion data, the interrupt request bit (PCIF) is set.

bit	7	6	5	4	3	2	1	0
Field	Reserved		TEST[1:0]		Reserved		PFS[1:0]	
Attribute	-		R		-		R/W	
Initial value	XX		XX		XX		00	

[bit7:6] Reserved: Reserved bits

Writing has no effect on operation.
The read value is undefined.

[bit5:4] TEST[1:0]: Test bits

Write	Has no effect on operation.
Read	The value is undefined.

[bit3:2] Reserved: Reserved bits

Writing has no effect on operation.
The read value is undefined.

[bit1:0] PFS[1:0]: Priority conversion FIFO stage count setting bits

When A/D conversion data for the FIFO stage count (N + 1) set in PFS[1:0] is written, the interrupt request flag (PCIF) is set to 1.

bit1:0	Description
00	Generates an interrupt request when conversion result is stored in the first FIFO stage.
01	Generates an interrupt request when conversion result is stored in the second FIFO stage.
10	Generates an interrupt request when conversion result is stored in the third FIFO stage.
11	Generates an interrupt request when conversion result is stored in the fourth FIFO stage.

5.9 Priority Conversion FIFO Data Register (PCFD)

The Priority Conversion FIFO Data Register (PCFD) consists of four FIFO stages and stores analog conversion results. Data can be retrieved sequentially by reading the register.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Field	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	Reserved			
Attribute	R												R			
Initial value	0xXXX												XXXX			

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Reserved			INVL	Reserved	RS2	RS1	RS0	Reserved			PC4	PC3	PC2	PC1	PC0
Attribute	R			R	R	R			R			R				
Initial value	XXX			1	X	XXX			XXX			XXXXX				

[bit31:20] PD11 to PD0: Priority conversion result

The result of 12-bit priority A/D conversion is written.

[bit19:13] Reserved: Reserved bits

The read value is undefined.

[bit12] INVL: A/D conversion result disable bit

This bit is set when this register value is invalid.

bit	Description
0	This register value is valid
1	This register value is invalid

[bit11] Reserved: Reserved bit

The read value is undefined.

[bit10:8] RS2 to RS0: Scan conversion start factor

The start factor of the priority conversion corresponding to this register value is shown.

bit10:8	Description
001	Software start (priority level 2)
010	Timer start (priority level 2)
100	External trigger (priority level 1)

[bit7:5] Reserved: Reserved bits

The read value is undefined.

[bit4:0] PC4 to PC0: Conversion input channel bits

The analog input channels corresponding to the conversion result written in PD11 to PD0 are written. Settings for channels not defined in the product specifications are not written. See the specified number of the analog input channels in the "Data Sheet" of each product.

bit4:0	Description
00000	ch.0
00001	ch.1
00010	ch.2
...	...
11101	ch.29
11110	ch.30
11111	ch.31

Notes:

- *This register has different bit configurations depending on the FDAS bit setting in the A/D Status Register (ADSR). When the FDAS bit is 1, see 3.3.6 Bit placement Selection for FIFO Data Registers.*
- *To perform a byte access to this register, read the most significant byte (bit31:24) to shift the FIFO data. Reading the other bytes (bit23:16, bit15:8, bit7:0) does not shift FIFO. To perform a half word access to this register, read the most significant half word (bit31:16) to shift FIFO. Reading the other byte (bit15:0) does not shift FIFO. Performing a word access to this register shifts FIFO.*
- *If software and a timer are started simultaneously, 0b011 may be read from the RS[2:0] bits.*
- *Conversion started with an external trigger can be performed only when the analog input channel is between ch.0 to ch.7.*

5.10 Priority Conversion Input Selection Register (PCIS)

The Priority Conversion Input Selection Register (PCIS) is used to select the analog input channels for which priority conversion is performed. For software or timer start at priority level 2, only one channel can be selected from multiple analog input channels. For external trigger start at priority level 1, one channel can be selected from eight channels (ch.0 to ch.7).

bit	7	6	5	4	3	2	1	0
Field	P2A[4:0]					P1A[2:0]		
Attribute	R/W					R/W		
Initial value	00000					000		

[bit7:3] P2A[4:0]: Priority level 2 analog input selection

This bit specifies the analog input channel for a start at priority level 2 (software/timer). It can be selected from all channels. It is not possible to set the channel that is not defined in the product specifications. See the specified number of the analog input channels in the "Data Sheet" of each product.

bit7:3	Description
00000	ch.0
00001	ch.1
00010	ch.2
...	...
11101	ch.29
11110	ch.30
11111	ch.31

[bit2:0] P1A[2:0]: Priority level 1 analog input selection

This bit specifies the analog input channel for a start at priority level 1 (external trigger). It can be selected from eight channels (ch.0 to ch.7).

bit2:0	Description
000	ch.0
001	ch.1
010	ch.2
...	...
101	ch.5
110	ch.6
111	ch.7

Note:

- *It is not allowed to change the channel during A/D conversion. Be sure to write a value to P1A or P2A when the A/D conversion is stopped. A/D conversion is not period of waiting start factors. It is allowed to change the channel during no start factors period.*

5.11 A/D Comparison Value Setup Register (CMPD)

The A/D Comparison Value Setup Register (CMPD) sets the value to be compared with the A/D conversion result. When the conditions set in both this register and the A/D Comparison Control Register (CMPCR) are satisfied, the conversion result comparison interrupt request bit (CMPIF) in the A/D Control Register (ADCR) is set.

bit	31	30	29	28	27	26	25	24
Field	CMAD11	CMAD10	CMAD9	CMAD8	CMAD7	CMAD6	CMAD5	CMAD4
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

bit	23	22	21	20	19	18	17	16
Field	CMAD3	CMAD2	Reserved					
Attribute	R/W	R/W	-					
Initial value	0	0	XXXXXX					

[bit31:22] CMAD11 to CMAD2: A/D conversion compare value setting bits

These bits set the value to be compared with the A/D conversion result.

The most significant 10 bits (bit11:2) of the A/D conversion result are compared with the value in this register (CMAD11 to CMAD2). The least significant two bits (bit1:0) of the A/D conversion result are not compared.

[bit21:16] Reserved: Reserved bits

Writing has no effect on operation.
The read value is undefined.

5.12 A/D Comparison Control Register (CMPCR)

The A/D Comparison Control Register (CMPCR) controls the A/D comparison function. When the converted value is compared with the value in the A/D Comparison Value Setup Register (CMPD) and the comparison condition in this register is satisfied, the conversion result comparison interrupt request bit (CMPIF) in the A/D Control Register (ADCR) is set.

bit	7	6	5	4	3	2	1	0
Field	CMPEN	CMD1	CMD0	CCH[4:0]				
Attribute	R/W	R/W	R/W	R/W				
Initial value	0	0	0	00000				

[bit7] CMPEN: Conversion result comparison function operation enable bit

This bit enables the operation of the A/D comparison function.

bit	Description
0	Stops the comparison function operation.
1	Enables the comparison function operation.

[bit6] CMD1: Comparison mode 1

This bit sets the condition for generating a conversion interrupt request.

bit	Description
0	Generates an interrupt request when the most significant 10 bits (bit11:2) of the A/D conversion result is smaller than the CMPD set value.
1	Generates an interrupt request when the most significant 10 bits (bit11:2) of the A/D conversion result is equal to or greater than the CMPD set value.

[bit5] CMD0: Comparison mode 0

This bit selects the comparison target. When this bit is 1, the setting of CCH[4:0] is invalid.

bit	Description
0	Compares the conversion result of the channel set in CCH[4:0].
1	Compares the conversion results of all channels.

[bit4:0] CCH[4:0]: Comparison target analog input channel

This bit sets the analog channel to be compared. When the CMD0 bit is 1, setting of this bit is invalid. It is not possible to set the channel that is not defined in the product specifications. See the specified number of the analog input channels in the "Data Sheet" of each product.

bit4:0	Description
00000	ch.0
00001	ch.1
00010	ch.2
...	...
11101	ch.29
11110	ch.30

bit4:0	Description
11111	ch.31

5.13 Sampling Time Selection Register (ADSS)

The Sampling Time Selection Register (ADSS3 to ADSS0) allows you to set the sampling time for each bit. Which of the sampling times set in Sampling Time Setup Registers 0 and 1 (ADST0 and ADST1) is used is specified in this register.

ADSS3 (most significant byte: TS31 to TS24) and ADSS2 (least significant byte: TS23 to TS16)

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	TS31	TS30	TS29	TS28	TS27	TS26	TS25	TS24	TS23	TS22	TS21	TS20	TS19	TS18	TS17	TS16
Attribute	R/W															
Initial value	0x0000															

[bit15:0] TS31 to TS16: Sampling time selection bits

Set the sampling time specified in the Sampling Time Setup Register (ADST) for the corresponding channel. Setting 0 specifies the time set in ADST0 and setting 1 specifies the time set in ADST1. TS31 to TS16 correspond respectively to ch.31 to ch.16.

ADSS1 (most significant byte: TS15 to TS8) and ADSS0 (least significant byte: TS7 to TS0)

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	TS15	TS14	TS13	TS12	TS11	TS10	TS9	TS8	TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0
Attribute	R/W															
Initial value	0x0000															

[bit15:0] TS15 to TS0: Sampling time selection bits

Set the sampling time specified in the Sampling Time Setup Register (ADST) for the corresponding channel. Setting 0 specifies the time set in ADST0 and setting "1" specifies the time set in ADST1. TS15 to TS0 correspond respectively to ch.15 to ch.0.

Notes:

- *It is not allowed to write to the ADSS register during A/D conversion. A/D conversion is not period of waiting start factors. It is allowed to write to the ADSS register during no start factors period.*
- *It is not possible to set 1 in the bit corresponding to a channel that is not defined in the product specifications. See the specified number of the analog input channels in the "Data Sheet" of each product.*

5.14 Sampling Time Setup Register (ADST)

Sampling Time Setup Registers 0 and 1 (ADST0 and ADST1) set the sampling times for A/D conversion. ADST0 and ADST1 are provided for setting two sampling times, and which one is used is selected in the Sampling Time Selection Register (ADSS3 to ADSS0).

ADST0 (most significant byte)

bit	15	14	13	12	11	10	9	8
Field	STX02	STX01	STX00	ST04	ST03	ST02	ST01	ST00
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	1	0	0	0	0

[bit15:13] STX02 to STX00: Sampling time N times setting bits

These bits multiply the sampling time set values in the ST04 to ST00 bits by N.

bit15	bit14	bit13	Description
0	0	0	Set value × 1 (Initial value)
0	0	1	Set value × 4
0	1	0	Set value × 8
0	1	1	Set value × 16
1	0	0	Set value × 32
1	0	1	Set value × 64
1	1	0	Set value × 128
1	1	1	Set value × 256

[bit12:8] ST04 to ST00: Sampling time setting bits

These bit set the sampling time for A/D conversion.

Sampling time = HCLK cycle × Clock division ratio × {(ST set value + 1) × STX setting multiplier + 3}

Example : When ST04 to ST00 = 9, STX02, STX01, and STX00 = 001 (multiplied by 4),
CT7 to CT0=0x00 (Clock frequency division ratio: 2), and HCLK = 20 MHz (50 ns),
Sampling time = 50 ns × 2 ×{(9 + 1) × 4 + 3} = 4300ns

Notes:

- *It is not allowed to write to the ADST0 register during A/D conversion. A/D conversion is not period of waiting start factors. It is allowed to write to the ADST0 register during no start factors period.*
- *For setting the sampling time, refer to the "Electrical Characteristics" in the "Data Sheet" to make sure that an appropriate time should be selected in accordance with an external impedance of an input channel, an analog power supply voltage (AVCC), and a base clock (HCLK) cycle.*
- *When STX02, STX01, and STX00 = 000 (ST04 to ST00 set values multiplied by 1) are set, set ST04 to ST00 to 2 or more (1 or less must not be set).*

ADST1 (least significant byte)

bit	7	6	5	4	3	2	1	0
Field	STX12	STX11	STX10	ST14	ST13	ST12	ST11	ST10
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	1	0	0	0	0

[bit7:5] STX12 to STX10: Sampling time N times setting bits

These bits multiply the sampling time set values in the ST14 to ST10 bits by N.

bit7	bit6	bit5	Description
0	0	0	Set value × 1(initial value)
0	0	1	Set value × 4
0	1	0	Set value × 8
0	1	1	Set value × 16
1	0	0	Set value × 32
1	0	1	Set value × 64
1	1	0	Set value × 128
1	1	1	Set value × 256

[bit4:0] ST14 to ST10: Sampling time setting bits

These bit set the sampling time for A/D conversion.

Sampling time = HCLK cycle × Clock division ratio × {(ST set value + 1) × STX setting multiplier + 3}

Example : When ST14 to ST10 = 9, STX12, STX11, and STX10 = 001 (multiplied by 4),
CT7 to CT0=0x00 (Clock frequency division ratio: 2), and HCLK = 20 MHz (50 ns),
Sampling time = 50 ns × {(9 + 1) × 4 + 3} = 4300ns

Notes:

- *It is not allowed to write to the ADST1 register during A/D conversion. A/D conversion is not period of waiting start factors. It is allowed to write to the ADST1 register during no start factors period.*
- *For setting the sampling time, refer to the Electrical Characteristics in the Data Sheet to make sure that an appropriate time should be selected in accordance with an external impedance of an input channel, an analog power supply voltage (AVCC), and a base clock (HCLK) cycle.*
- *When STX12, STX11, and STX10 = 000 (ST14 to ST10 set values multiplied by 1) are set, set ST14 to ST10 to 2 or more (1 or less must not be set).*

5.15 Frequency Division Ratio Setup Register (ADCT)

The Frequency Division Ratio Setup Register (ADCT) sets the clock frequency division ratio, which is part of the A/D conversion time.

bit	7	6	5	4	3	2	1	0
Field	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	1	1	1

[bit7:0] CT7 to CT0: Frequency division ratio setting bits

These bits set the division ratio of the HCLK frequency for generating the clock of A/D conversion.

The frequency division ratio setting is common in Sampling Setup Registers 0 and 1 (ADST0/1).

bit7:0	Description
0x80	Frequency division ratio 1
0x00	Frequency division ratio 2
0x01	Frequency division ratio 3
0x02	Frequency division ratio 4
...	...
0X07	Frequency division ratio 9 (Initial value)
...	...
0x3C	Frequency division ratio 62
0x3D	Frequency division ratio 63
0x3E	Frequency division ratio 64
0x3F	Frequency division ratio 65

Compare clock cycle = Base clock (HCLK) cycle × Frequency division ratio
Comparison time = Compare clock cycle × 14

Example : When the CT[7:0] set value = 0 (Compare frequency division ratio: 2) and
HCLK = 20 MHz (50 ns),
Compare clock cycle = 50 ns × 2 = 100 ns
Comparison time = 100 ns × 14 = 1400 ns

Notes:

- *Setting 0x40 to 0x7F to bit7:0 is not allowed.*
- *It is not allowed to write to the clock division setting register (ADCT) during A/D conversion. A/D conversion is not period of waiting start factors. It is allowed to write to the clock division setting register (ADCT) during no start factors period.*
  Only when the base clock prescaler register (BSC_PSR) of clock generator is set to 0x0, A/D conversion can be performed in frequency division ratio at 1.
- *For setting the compare clock cycle, refer to the Electrical Characteristics in the Data Sheet to make sure that an appropriate time should be selected in accordance with an analog power supply voltage (AVCC) and a base clock (HCLK) cycle.*

5.16 A/D Operation Enable Setup Register (ADCEN)

The A/D Operation Enable Setup Register (ADCEN) is used to turn the 12-bit A/D converter to the operation enable state.

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	ENBLTIME[15:8]								Reserved						READY	ENBL
Attribute	R/W								R						R	R/W
Initial value	0xFF								000000						0	0

[bit15:8] ENBLTIME[15:8]: Operation enable state transition cycle selection bits

These bits select the cycle count of operation enable state transition period.

Operation enable state transition period= Base clock (HCLK) cycle × (ENBLTIME setting value × 4 + 1)

Example) When ENBLTIME[15:8] = 0xFF, and HCLK = 20MHz (50ns),
Operation enable state transition period = 50 ns × (255×4 + 1) = 51050 ns

[bit7:2] Reserved: Reserved bits

The read value is undefined.

[bit1] READY: A/D operation enable state bit

This bit indicates whether the A/D converter is in the operation enable state or in the operation stop state.

A/D conversion can be performed only in the operation enable state.
An A/D conversion request in the operation stop state is ignored.
If the A/D converter enters the operation stop state during A/D conversion, A/D conversion stops immediately.

bit	Description
0	Operation stop state
1	Operation enable state

[bit0] ENBL: A/D operation enable bit

This bit enables the operation of the A/D converter.

Writing 1 to the ENBL bit turns the A/D converter to the operation enable state after the period of operation enable state transitions. On the other hand, writing 0 to this bit turns the A/D converter to the operation stop state.

bit	Description
0	Stops operation
1	Enables operation

Note:

- *For setting the period of operation enable state transition, refer to the Electrical Characteristics in the Data Sheet to make sure that an appropriate time should be selected in accordance with an analog power supply voltage (AVCC) and a base clock (HCLK) cycle.*
  It is not allowed to rewrite ENBLTIME[15:8] during the period between writing 1 to ENBL bit and

setting READY bit to 1.
When setting the CPU to the timer mode, the stop mode, RTC mode, deep standby STOP mode, and deep standby RTC mode, set the ENBL bit to 0 and turn the A/D converter to the operation stop state.

5.17 Upper Limit Setup Register (WCMPDH)

The Upper Limit Setup Register (WCMPDH) is used to set the upper limit used for the range comparison.

bit	31	30	29	28	27	26	25	24
Field	CMHD11	CMHD10	CMHD9	CMHD8	CMHD7	CMHD6	CMHD5	CMHD4
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

bit	23	22	21	20	19	18	17	16
Field	CMHD3	CMHD2	Reserved					
Attribute	R/W	R/W	R					
Initial value	0	0	000000					

[bit31:22] CMHD11 to CMHD2: Upper limit bits

These bits specify the upper limit threshold used for range comparison.

bit31:22	Description
Upper limit	

[bit21:16] Reserved: Reserved bits

When writing, always write 0.
When reading, 0 is always read.

Note:

- *When the range comparison function enabled, the most significant 10 bits (bit11:2) of the A/D conversion result is compared with this register (CMHD). The comparison with the least significant 2 bits (bit1:0) of the A/D conversion result is not executed.*

5.18 Range Comparison Control Register (WCMPCR)

The range comparison control register (WCMPCR) is used for the confirmation of continuous detection specification count and its state, the selection of within-range or out-of-range confirmation, the confirmation of upper limit excess or lower limit excess in the out-of-range area, and enabling and disabling of range comparison interrupt.

bit	7	6	5	4	3	2	1	0
Field	RCOCD2	RCOCD1	RCOCD0	RCOIRS	RCOIE	RCOE	Reserved	
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R	
Initial value	0	0	1	0	0	0	00	

[bit7:5] RCOCD2 to RCOCD0: Continuous detection specification count/state indication bits

These bits indicate continuous detection specification count and continuous detection time state of range comparison result.

bit7:5	Description	
	At reading except in RMW accessing	At reading or at writing in RMW accessing
000	Continuous detection state: 0 times	Setting prohibited
001	Continuous detection state: 1 times	Specified continuous detection time: 1
010	Continuous detection state: 2 times	Specified continuous detection time: 2
011	Continuous detection state: 3 times	Specified continuous detection time: 3
100	Continuous detection state: 4 times	Specified continuous detection time: 4
101	Continuous detection state: 5 times	Specified continuous detection time: 5
110	Continuous detection state: 6 times	Specified continuous detection time: 6
111	Continuous detection state: 7 times	Specified continuous detection time: 7

- When the range comparison result count reaches the continuous detection specification count, the range comparison interrupt factor flag bit (RCINT) of the corresponding start channel is set to 1. And the continuous detection state is stopped at the continuous detection specification count.
- At reading other the read-modify-write (RMW) access, the continuous detection state is read out.
- At reading other the read-modify-write (RMW) access, the written value (the continuous detection specification count) is read out.

Notes:

- *Do not change the continuous detection specification count bit and state indication bit (RCOCD) while the range comparison operation is enabled (RCOE=1).*
- *Do not set 000 to the continuous detection specification count bit and state indication bit (RCOCD).*

[bit4] RCOIRS: Selection bit of within-range and out-of- range confirmation

bit	Description
0	Confirmation of out-of-range
1	Confirmation of within-range

- The A/D conversion result (scan conversion or priority conversion) selects the range comparison conditions of out-of- range or within-range for upper limit threshold bit (CMHD) and lower limit threshold bit (CMLD) selected by the upper/lower limit threshold selection bit (RCOTS).
- The range comparison condition at the out-of-range confirmation (RCOIRS=0) is as follows:
  A/D conversion result (scan conversion or priority conversion) > upper limit threshold bit (CMHD)
  Or, A/D conversion result (scan conversion or priority conversion) < lower limit threshold bit (CMLD)
- The range comparison condition at the within-range confirmation (RCOIRS=1) is as follows:
  A/D conversion result (scan conversion or priority conversion) ≤ upper limit threshold bit (CMHD)
  And, A/D conversion result (scan conversion or priority conversion) ≥ lower limit threshold bit (CMLD)
- At the range comparison detection for the out-of-range range confirmations (RCOIRS="0"), the upper limit threshold excess or below the lower limit threshold can be confirmed by threshold excess flag bit (RCOOF).

[bit3] RCOIE: Range comparison interrupt request enable bit

bit	Description
0	Range comparison interrupt disabled
1	Range comparison interrupt enabled

- When the range comparison interrupt factor flag bit (RCINT) of the corresponding startup channel is set to 1 and when the range comparison interrupt request is enabled (RCOIE=1), the interrupt request is generated.

[bit2] RCOE: Range comparison execution enable bit

Selects A/D comparison function and range comparison function.

bit	Description
0	Range comparison execution disabled
1	Range comparison execution enabled

- When the range comparison execution enable bit (RCOE) is 0, the range comparison execution is disabled. Moreover, the continuous detection count sate is initialized to 000.

When the range comparison execution enable bit (RCOE) is 1, the range comparison execution is enabled.

[bit1:0] Reserved: Reserved bits

When writing, always write 0.
When reading, 0 is always read.

5.19 Lower Limit Threshold Setup Register (WCMPDL)

The lower limit threshold setup register (WCMPDL) is used to set the lower limit threshold for the range comparison.

bit	15	14	13	12	11	10	9	8
Field	CMLD11	CMLD10	CMLD9	CMLD8	CMLD7	CMLD6	CMLD5	CMLD4
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Field	CMLD3	CMLD2	Reserved					
Attribute	R/W	R/W	R					
Initial value	0	0	000000					

[bit15:6] CMLD11 to CMLD2: Lower limit threshold bits

Set the lower limit threshold used for the range comparison.

Bit15:6	Description
Lower limit threshold	

[bit5:0] Reserved: Reserved bits

When writing, always write 0.

When reading, 0 is always read.

Note:

- *When the range comparison execution is enabled, the most significant 10 bits (bit11:2) of the A/D conversion result is compared with this register (CMLD). The comparison with the least significant 2 bits (bit1:0) of the A/D conversion result is not executed.*

5.20 Range Comparison Channel Select Register (WCMPSR)

The range comparison channel select register (WCMPSR) is used to set the channel for the range comparison.

bit	15	14	13	12	11	10	9	8
Field	Reserved		WCMD	WCCH[4:0]				
Attribute	R		R/W	R/W				
Initial value	00		0	00000				

[bit15:14] Reserved: Reserved bits

When writing, always write 0.

When reading, 0 is always read.

[bit13] WCMD: Comparison mode select bit

bit	Description
0	Compares the conversion result of the channel set with WCCH[4:0] bits.
1	Compares the conversion results of all channels.

Selects the target for the range comparison. When this bit is 1, the setting of WCCH[4:0] bits becomes invalid.

[bit12:8] WCCH[4:0]: Comparison target analog input channel

Bit12:8	Description
00000	Ch.0
00001	Ch.1
00010	Ch.2
- - -	- - -
11101	Ch.29
11110	Ch.30
11111	Ch.31

Selects the target analog input channel for comparison. When WCMD bit is 1, the setting of these bits is invalid. It is not possible to set the channel that is not defined in the product specifications. See the specified number of the analog input channels in the Data Sheet of the product used.

5.21 Range Comparison Threshold Excess Flag Register (WCMRCOT)

The range comparison threshold excess flag register (WCMCOT) is used to indicate that the comparison result is beyond the upper limit threshold or below the lower limit threshold in the out-of-range confirmation setting.

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	R							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	R							
Initial value	0x00							

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	R							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	Reserved							RCOOF
Attribute	R							R/W
Initial value	0000000							0

[bit31:1] Reserved: Reserved bits

When writing, always write 0.

When reading, 0 is always read.

[bit0] RCOOF: Threshold excess flag bit

bit	Description
0	Below the lower limit threshold (A/D data < Lower limit threshold bit)
1	Beyond the upper limit threshold (A/D data > Upper limit threshold bit)

- For the confirmation of outside-range (RCOIRS=0), this bit indicates that the range comparison result is greater than the upper limit threshold setting register (RCOOF=1), or the result is smaller than the lower limit threshold (RCOOF=0).
- For the confirmation of outside-range (RCOIRS=0), when the range comparison result is confirmed to be within the range, the threshold excess flag bit holds the prior value.
- When the range comparison interrupt factor flag bit (RCINT) of the corresponding startup channel is set to be 1, the threshold excess flag bit (RCOOF) is not updated and holds the prior value, even if the range comparison result is confirmed to be outside the range for the confirmation of outside-range (RCOIRS=0).
- For the confirmation of within-range (RCOIRS=1), the threshold excess flag bit has no meaning (the bit holds the prior value.)

5.22 Range Comparison Flag Register (WCMRCIF)

The range comparison flag register (WCMRCIF) indicates the interrupt factor due to the continuous detection of the range comparison result.

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	R							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	R							
Initial value	0x00							

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	R							
Initial value	0x00							

Bit	7	6	5	4	3	2	1	0
Field	Reserved							RCINT
Attribute	R							R/W
Initial value	0000000							0

[bit31:1] Reserved: Reserved bits

When writing, always write 0.

When reading, 0 is always read.

[bit0] RCINT: Range comparison interrupt factor flag bit

bit	Description	
	Read	**Write**
0	Range comparison interrupt factor clear state	Bit clear
1	State where the interrupt factor is generated due to the continuous detection of range comparison results	No change and no influence to others.

- The RCINT bit is set to 1 by the continuous detection of the range comparison results of the corresponding startup channel.
- When RCINT bit and range comparison interrupt request permission (RCOIE) of the corresponding startup channel are 1, the range comparison interrupt request is generated.
- At writing, the RCINT bit is cleared by 0, the bit is not changed by 1 and has no influence to others.

Notes:

- *At read-modify-write access (RMW), 1 is read.*

- *When the software clear (writing RCINT=0) and hardware set occurs simultaneously, the hardware set has a priority.*

CHAPTER 1-3: A/D Timer Trigger Selection

This chapter explains the functions and operations to select a timer trigger of the A/D converter.

1. Overview
2. Registers

CODE: 9BFBATSB_FM0-E03.0

1. Overview

This section explains the operations to select a timer trigger of the A/D converter.

Selecting a Timer Trigger of the A/D Converter

The A/D converter can be started by the factors shown in Table 1-1.

Table 1-1 A/D Converter Start Factor

Conversion type	Start factor
Priority level 1 conversion	– Input from an external trigger pin (at falling edge)
Priority level 2 conversion	– Software (when the Priority Conversion Start Bit(PSTR) of Priority Conversion Control Register (PCCR) is set to 1) – Trigger input from timer (at rising edge)
Scan conversion	– Software (when the Scan Conversion Start Bit (SSTR) of SCAN Conversion Control Register (SCCR) is set to 1) – Trigger input from timer (at rising edge)

The A/D converter can be started with two types of timers: base timer and multifunction timer.

A timer start factor can be selected using the Scan Conversion Timer Trigger Selection Register (SCTSL) or Priority Conversion Timer Trigger Selection Register (PRTSL). The A/D converter starts A/D conversion if a rising edge of the selected timer is detected while timer starting is enabled.

The multiple A/D converters can use same start factor.

For details on the operations of the 12-bit A/D converter, see “3. Explanation of operations” in the “12-bit A/D Converter”.

2. Registers

This section explains the configuration and functions of the registers used to select an A/D timer trigger.

List of Timer Trigger Selection Registers for A/D Converter

Abbreviation	Register name	Reference
SCTSL	Scan Conversion Timer Trigger Selection Register	2.1
PRTSL	Priority Conversion Timer Trigger Selection Register	2.2

2.1 Scan Conversion Timer Trigger Selection Register (SCTSL)

The Scan Conversion Timer Trigger Selection Register (SCTSL) is used to select a timer trigger when performing scan conversion.

bit	15	14	13	12	11	10	9	8
Field	Reserved				SCTSL[3:0]			
Attribute	R				R/W			
Initial value	XXXX				0000			

[bit15:12] Reserved: Reserved bits

The read values are undefined.

Writing has no effect in operation.

[bit11:8] SCTSL[3:0]: Scan conversion timer trigger selection bits

bit11:8	Description
0000	No selected trigger (Input is fixed to 0.)
0001	Starts scan conversion with the multifunction timer.
0010	Base timer ch.0
0011	Base timer ch.1
0100	Base timer ch.2
0101	Base timer ch.3
0110	Base timer ch.4
0111	Base timer ch.5
1000	Base timer ch.6
1001	Base timer ch.7
1010	Base timer ch.8
1011	Base timer ch.9
1100	Base timer ch.10
1101	Base timer ch.11
1110	Base timer ch.12
1111	Base timer ch.13

The number of channels in the base timer is differed for each product. For details, see “Data Sheet “of the product used. Do not make settings for a channel which is not mounted.

2.2 Priority Conversion Timer Trigger Selection Register (PRTSL)

The Priority Conversion Timer Trigger Selection Register (PRTSL) is used to select a timer trigger when performing priority conversion.

bit	7	6	5	4	3	2	1	0
Field	Reserved				PRTSL[3:0]			
Attribute	R				R/W			
Initial value	XXXX				0000			

[bit7:4] Reserved: Reserved bits

The read values are undefined.

Writing has no effect in operation.

[bit3:0] PRTSL[3:0]: Priority conversion timer trigger selection bits

bit3:0	Description
0000	No selected trigger (Input is fixed to 0.)
0001	Starts priority conversion with the multifunction timer.
0010	Base timer ch.0
0011	Base timer ch.1
0100	Base timer ch.2
0101	Base timer ch.3
0110	Base timer ch.4
0111	Base timer ch.5
1000	Base timer ch.6
1001	Base timer ch.7
1010	Base timer ch.8
1011	Base timer ch.9
1100	Base timer ch.10
1101	Base timer ch.11
1110	Base timer ch.12
1111	Base timer ch.13

The number of channels in the base timer is differed for each product. For details, see “Data Sheet “of the product used. Do not make settings for a channel which is not mounted.

CHAPTER2: 10-bit D/A Converter

This chapter explains the functions and operations of

10-bit D/A converter.

1. Overview
2. Configuration
3. Operations
4. Setting Procedure Example
5. Registers
6. Notes on Using 10-bit D/A Converter

CODE: 9xFBDA10M3-E01.0

1. Overview

The 10-bit D/A converter has a function to convert 10-bit digital values to analog output values.

Features of 10-bit D/A Converter

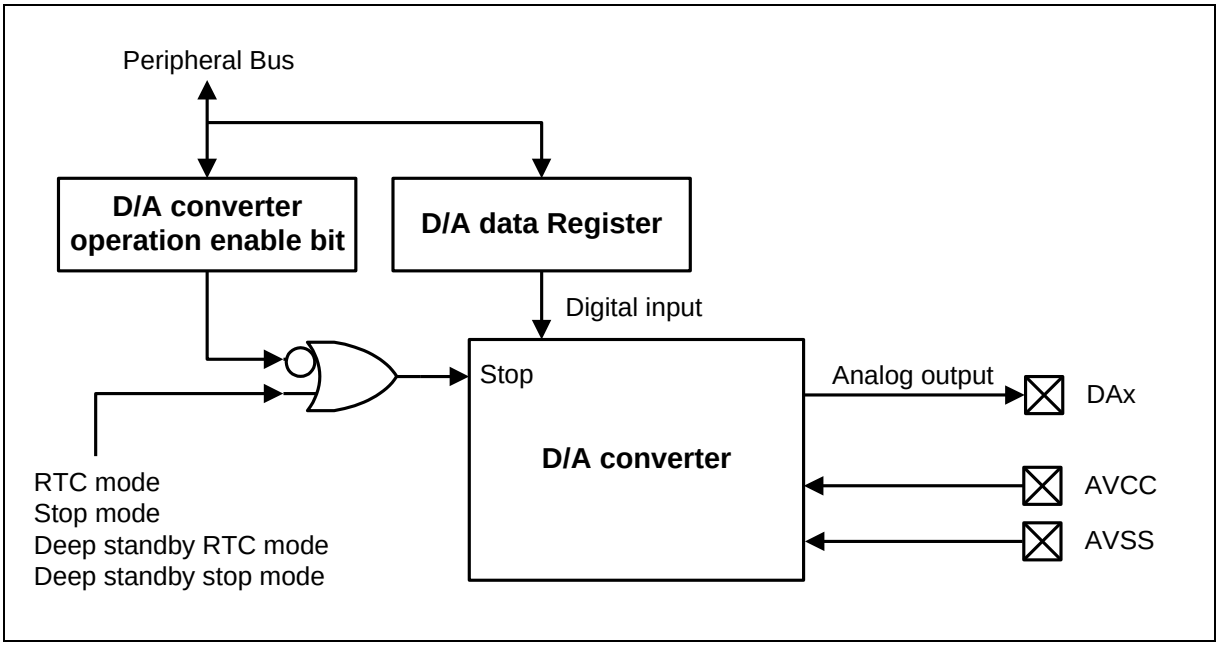
- 10-bits resolution
- R-2R method
- Stops operating in low power consumption modes below:
  - RTC mode
  - Stop mode
  - Deep standby RTC mode
  - Deep standby stop mode

2. Configuration

This section shows the configuration of the 10-bit D/A converter.

Block Diagram of 10-bit D/A Converter

Figure 2-1 Block Diagram of 10-bit D/A Converter



3. Operations

This section explains the operations of the 10-bit D/A converter.

When the operation of D/A converter is enabled with the DAE bit of D/A Control Register (DACR), the digital values written in the D/A Data Register (DADR) will be converted to analog values and output from DAx pins. In this case,

In some low power consumption modes, the operation of the D/A converter will be stopped independent of the DAE bit.

The operation states of the D/A converter are shown in the following Table 3-1.

Table 3-1 Operation States of D/A Converter and I/O Port State When DAE=1

Operating Mode	D/A Converter Operation	I/O Port
RTC mode Stop mode Deep standby RTC mode Deep standby stop mode	Stop	– Input shutdown – Input/output direction is defined by DDR setting. – Output level is defined by PDOR setting. – Pull-up is determined by PCR setting.
Modes other the above	Enable	– Input shutdown – Input direction – Pull-up shutdown

Voltages which can be output while D/A converter operation is enabled are from 0.0V to 1023/1024×AVCC (AVCC: Voltage at AVCC pins). D/A Data Register (DADR) bits and ideal values of output voltage are shown in Table 3-2.

Table 3-2 Relationship between DA[9:0] and Analog Output Values

DA[9:0]	Ideal Output Voltage
0000000000	0 / 1024 × AVCC
0000000001	1 / 1024 × AVCC
0000000010	2 / 1024 × AVCC
…	…
1111111101	1021 / 1024 × AVCC
1111111110	1022 / 1024 × AVCC
1111111111	1023 / 1024 × AVCC

While D/A converter operation is stopped, the outputs of the D/A converter are at Hi-Z.

4. Setting Procedure Example

This section provides an example of setting procedure for the 10-bit D/A converter.

Setting procedure to operate D/A converter and output to DAx pins are as follows.

1. Set a digital value to be converted in the D/A Data Register (DADR).
2. Set "1" to the DAE bit of D/A Control Register (DACR).

After the setting above is completed, analog values will be output from the DAx pins.

5. Registers

This section describes the registers of the 10-bit D/A converter.

List of Registers of 10-bit D/A Converter

Table 5-1 List of Registers of 10-bit D/A Converter

Abbreviation	Register Name	Reference
DACR	D/A Control Register	5.1
DADR	D/A Data Register	5.2

5.1 D/A Control Register (DACR)

The D/A Control Register (DACR) controls D/A converter operations.

Register Configuration

bit	23	22	21	20	19	18	17	16
Field	Reserved							DAE
Attribute	-							R/W
Initial Value	XXXXXXX							0

Register Functions

[bit23:17] Reserved: Reserved bits

The read values are undefined. Writing has no effect in operation.

[bit16] DAE: D/A converter operation enable bit

Bit	Description
0	D/A converter operation stop
1	D/A converter operation enable

5.2 D/A Data Register (DADR)

D/A Data Register (DADR) is a register which sets digital values to be converted to analog signals.

Register Configuration

bit	15	14	13	12	11	10	9	8
Field	Reserved						DA[9:8]	
Attribute	-						R/W	
Initial Value	XXXXXX						XX	

bit	7	6	5	4	3	2	1	0
Field	DA[7:0]							
Attribute	R/W							
Initial Value	0xXX							

Register Functions

[bit15:10] Reserved: Reserved bits

The read values are undefined. Writing has no effect in operation.

[bit9:0] DA[9:0]: D/A Data Register

See Table 3-2 for relationship between the setting values of this register and the output voltages.

6. Notes on Using 10-bit D/A Converter

This section provides notes on using the 10-bit D/A converter.

The D/A converter may output an unknown value immediately after DAR bit of D/A Control Register (DAXR) is changed from "0" to "1". See "Electrical Specification" in the datasheet for the duration of the unknown output.

At DAE=1, the external interrupt input select bit (EINTxxS) of the extended function pin setting register (EPFR06, 15) should be set to a pin other than a pin sharing analog output (DAx) and external interrupt input (INTxx).

CHAPTER3-1: LCD Controller Overview

This chapter describes the functions and operations of the LCD controller. Different chapter for different Type.

CODE: 9BLCDC-E01.0

■ The TYPEs of LCDC

There are 2 types of LCDC mounted in different product. For the details of each setting, refer to the each chapter as following Table 1-1.

Table 1-1 Correspondence Table for LCDC Chapter

Product TYPE	Reference
—	Chapter " LCDC_TYPE1"
TYPE2	Chapter " LCDC_TYPE2"

CHAPTER3-2: LCD Controller (TYPE1)

In FM0+ family product, LCD Controller(TYPE1) is not equipped.

This chapter is removed.

CODE: 9BLCDC-E01.0

CHAPTER3-3: LCD Controller (TYPE2)

This chapter describes the functions and operations of the LCD controller.

1. Overview
2. Configuration
3. Operations
4. Setting Procedure Examples
5. Registers
6. Notes on Using LCD Controller

CODE: 9BLCDC-E01.0

1. Overview

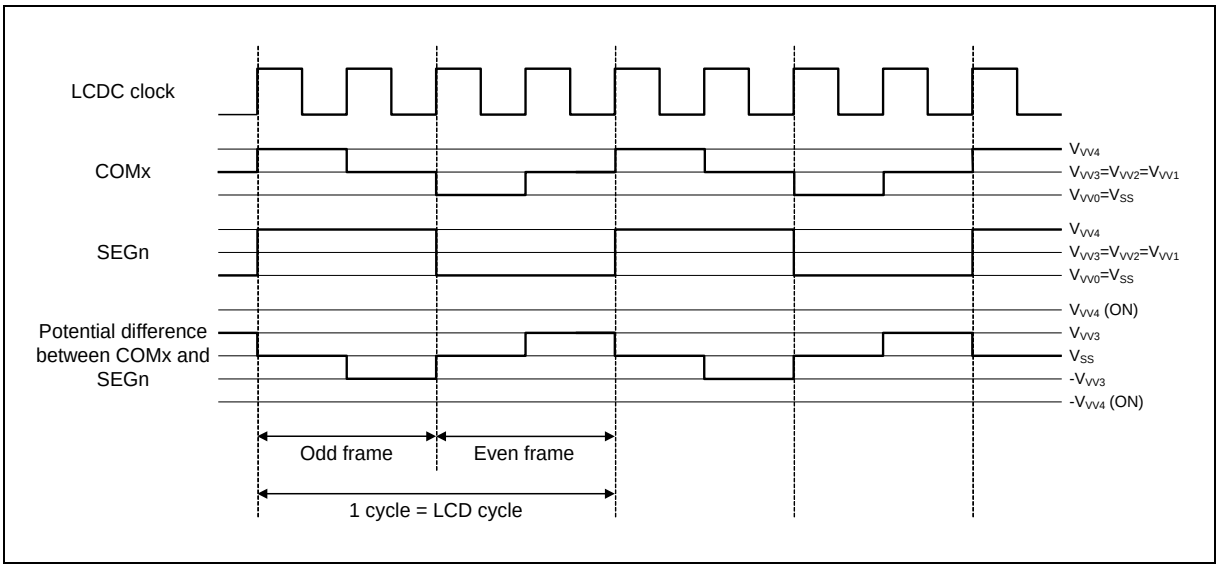
The LCD controller displays the contents of Display Data Memory (LCDRAM) directly to the LCD (Liquid Crystal Display) panel by using segment outputs and common outputs.

Functions of LCD Controller

- 8 COM mode or 4 COM mode is selectable for display mode
  - 8 COM mode
    - Up to 8 common outputs (COM0 to COM7) and up to 40 segment outputs (SEG00 to SEG39) are available
    - LCDRAM size is up to 40 bytes (40 × 8 bits)
    - Bias is selectable from 1/3 or 1/4.
  - 4 COM mode
    - Up to 4 common outputs (COM0 to COM3) and up to 44 segment outputs (SEG00 to SEG43) are available
    - LCDRAM size is up to 22 bytes (44 × 4 bits)
    - Bias is selectable from 1/2, 1/3 or 1/4
- Divider resistors for generating LCD drive power are incorporated allowing selecting 10kΩ or 100kΩ for the resistor values (the LCD drive power can be supplied from the external circuit)
- Sub-clock and PCLK are available for LCD controller operating clock (LCDC clock).
- Blinking (flashing) function is available
- Direct drive for LCD panel is available
- Voltage Booster configuration is available
- Interrupt request is allowed per frame

Terms Used for LCD Controller

Terms used for this chapter are defined as follows.



- LCDC clock

  Clock which drives the LCD controller.

- LCD cycle

  Cycle of AC waveform which drives LCD.

  By its nature, LCD causes deterioration to its LCD elements if DC driven because the LCD elements are affected by chemical changes. To avoid this situation, the LCD controller incorporates AC waveform generator to generate AC waveform consisting of 2 frames: an odd frame and an even frame (inverted odd frame), allowing driving the LCD.

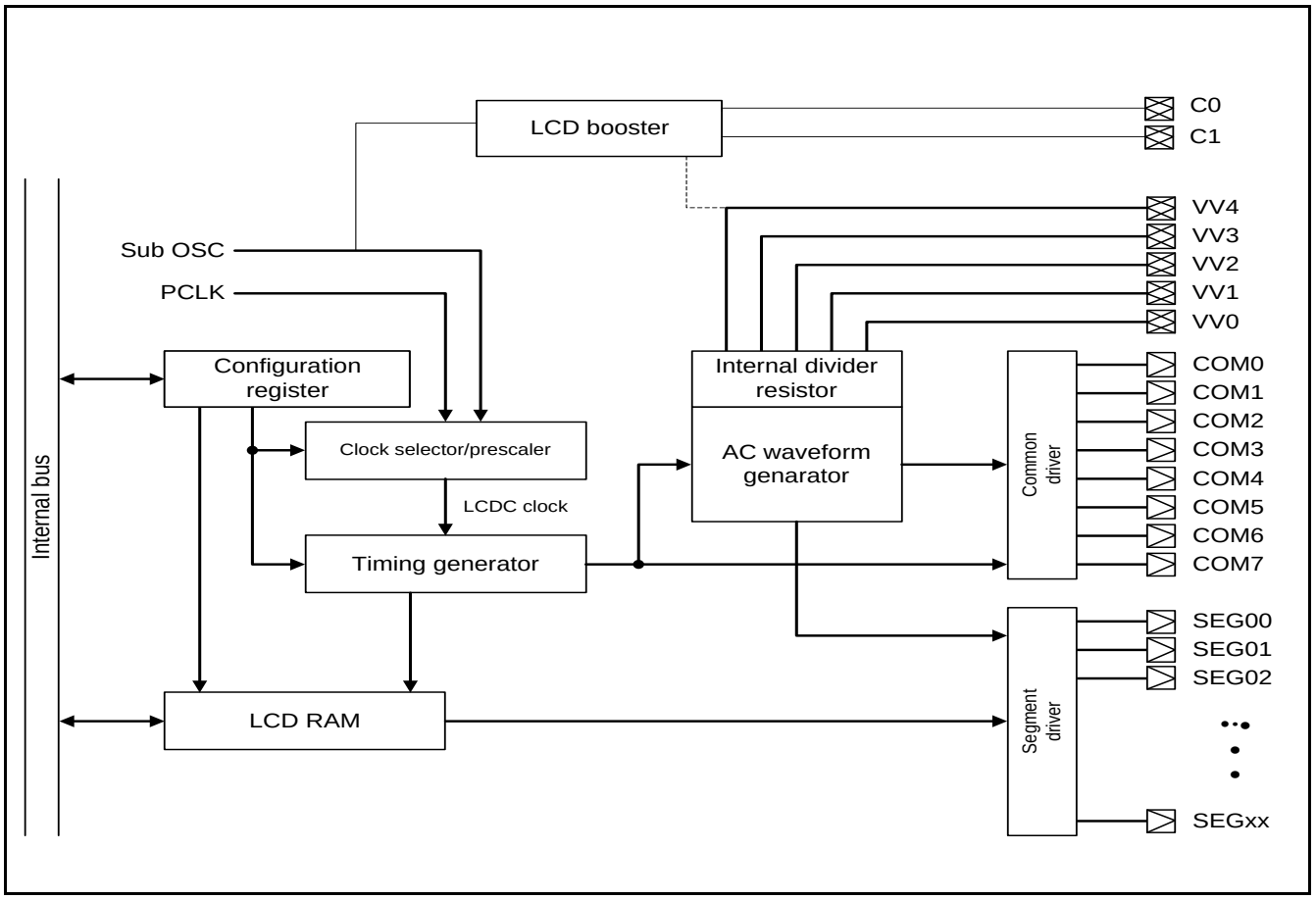
2. Configuration

This section describes the configuration of the LCD controller.

Block Diagram of LCD Controller

The block diagram of LCD controller is shown in Figure 2-1.

Figure 2-1 Block Diagram of LCD Controller



- Clock selector/prescaler

  Clock selector/prescaler is used to select clock from sub-clock and PCLK to generate LCDC clock.

- LCD booster

  LCD booster generates higher voltage than VCC to drive LCD common/segment output.

- Timing generator

  Timing generator is used to control common outputs and segment outputs based on LCDC clock and register setups.

- AC waveform generator

  AC waveform generator generates AC waveform which drives LCD based on the signals from Timing Generator.

- Common/segment driver

  Common/segment driver is a driver for LCD common/segment output pins.

- Configuration register

  This register controls LCD controller operations.

- LCD RAM

  LCD RAM is the Display Data Memory Register for segment output signal generation.
  The contents of the LCDRAM are automatically read in synchronization with the selection timing for common signals and output from the segment output pins.
  The contents of the LCDRAM are output from the segment output pins at the same time of rewrite to the LCDRAM.

- Internal divider resistor

  Internal divider resistors are used to generate LCD drive voltages. When the LCD drive power pins (VV0 to VV4) are acting as divider resistor pins, the divider resistors can be provided externally.

2.1 LCD Drive Voltage Generator

LCD panel drive voltage can be generated with the use of the internal divider resistors in the LCD controller or external divider resistors. If booster function is chosen, it is necessary to choose external divider resistors method.

Internal Divider Resistors

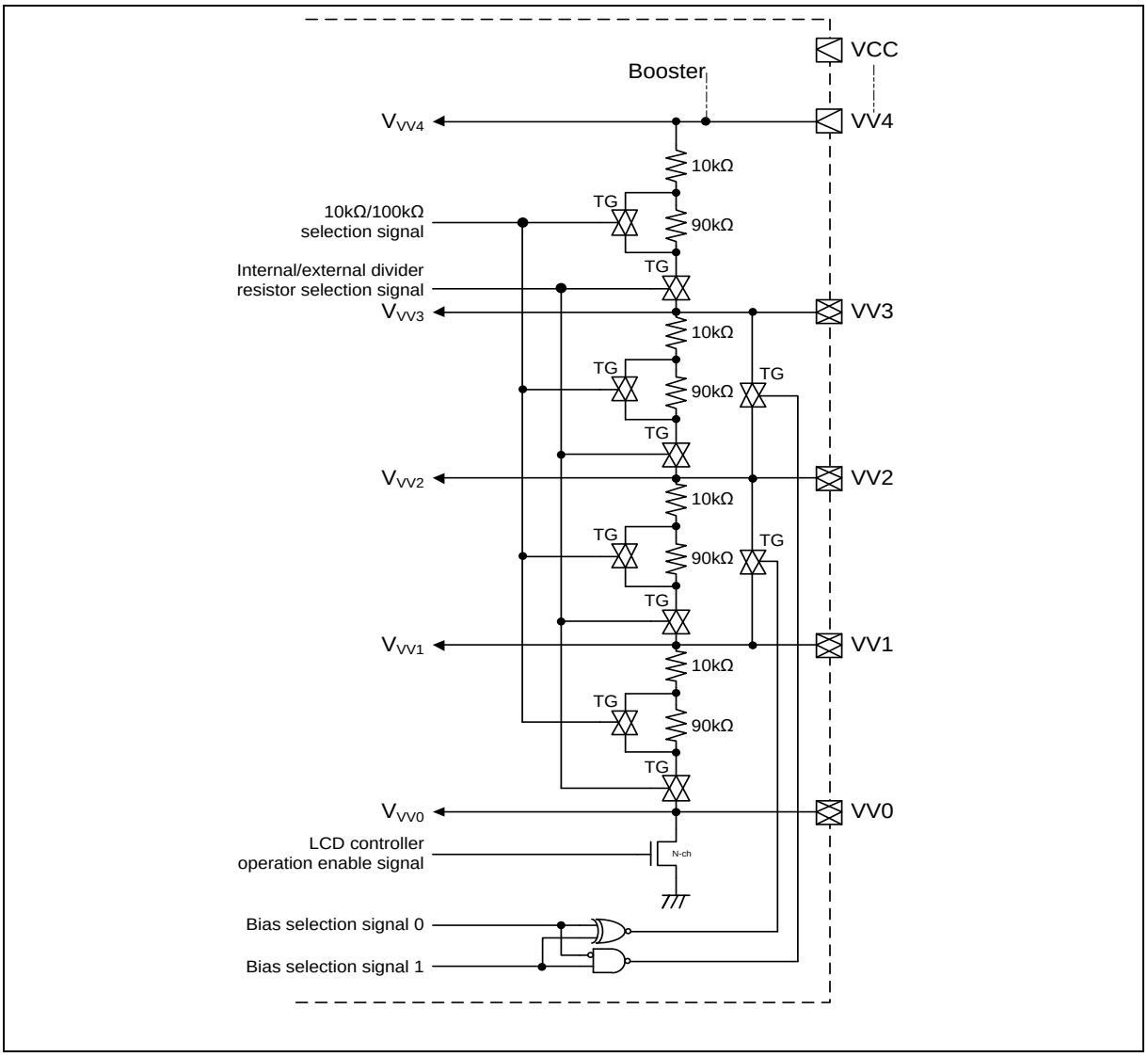
LCD controller incorporates internal divider resistors. External divider resistors can be connected to the LCD drive power pins (VV0 to VV4).
To select internal divider resistor or external divider resistor, use LCD drive power control bit (VSEL) of the LCDC Control Register 1 (LCDCC1). Setting the VSEL bit to "1" makes the internal divider resistors live. To use internal divider resistors only without any external divider resistor, set the VE4 bit of the LCDC Control Register 3 (LCDCC3) to "1" (if LCD Controller is used, VV4 pin is not allowed to be used as general purpose input/output pin).

There are two kinds of power source could provide power supply to VV4, one is internal booster, the other is external VCC,

In case of Booster is used, Since Booster could be provide power source for VV4, do not connect the VV4 to VCC by board. For details please refer to 5.4(LCDC_BOOSER register-PSF).

Figure 2-2 shows the equivalent circuit when internal divider resistors are used.

Figure 2-2 Equivalent Circuit of Internal Divider Resistors



Internal Divider Resistor Use and Brightness Adjustment by Connecting Resistor

The internal divider resistors consist of 10kΩ and 100kΩ resistors. Figure 2-3, Figure 2-4 and Figure 2-5 show the pictures of internal divider resistors. In the case where sufficient brightness cannot be obtained by using the internal divider resistors, connect (pins VCC and VV4) an external variable resistor (V_R) to adjust the voltage at pin VV4.

Figure 2-3 Internal Divider Resistors for 1/4 Bias Generation Bias

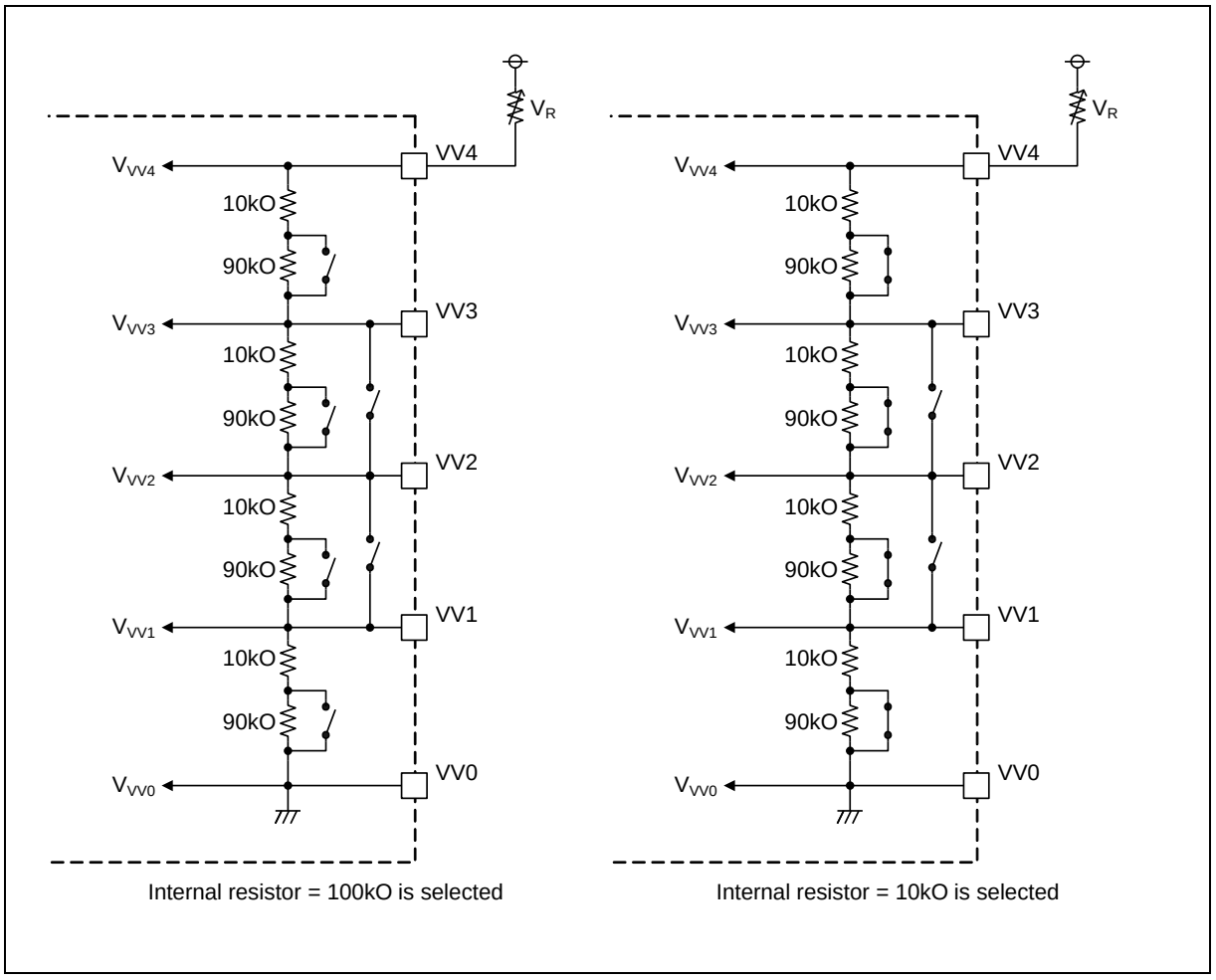


Figure 2-4 Internal Divider Resistors for 1/3 Bias Generation

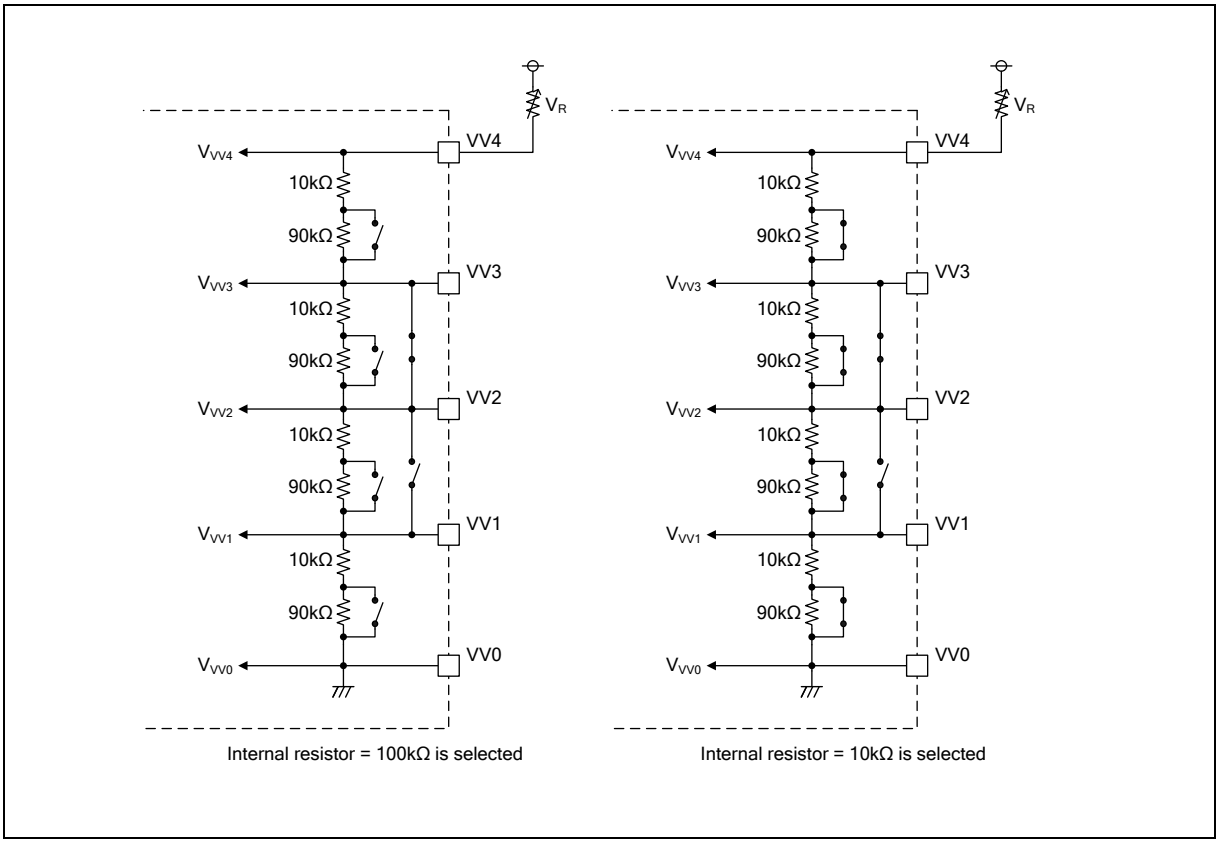
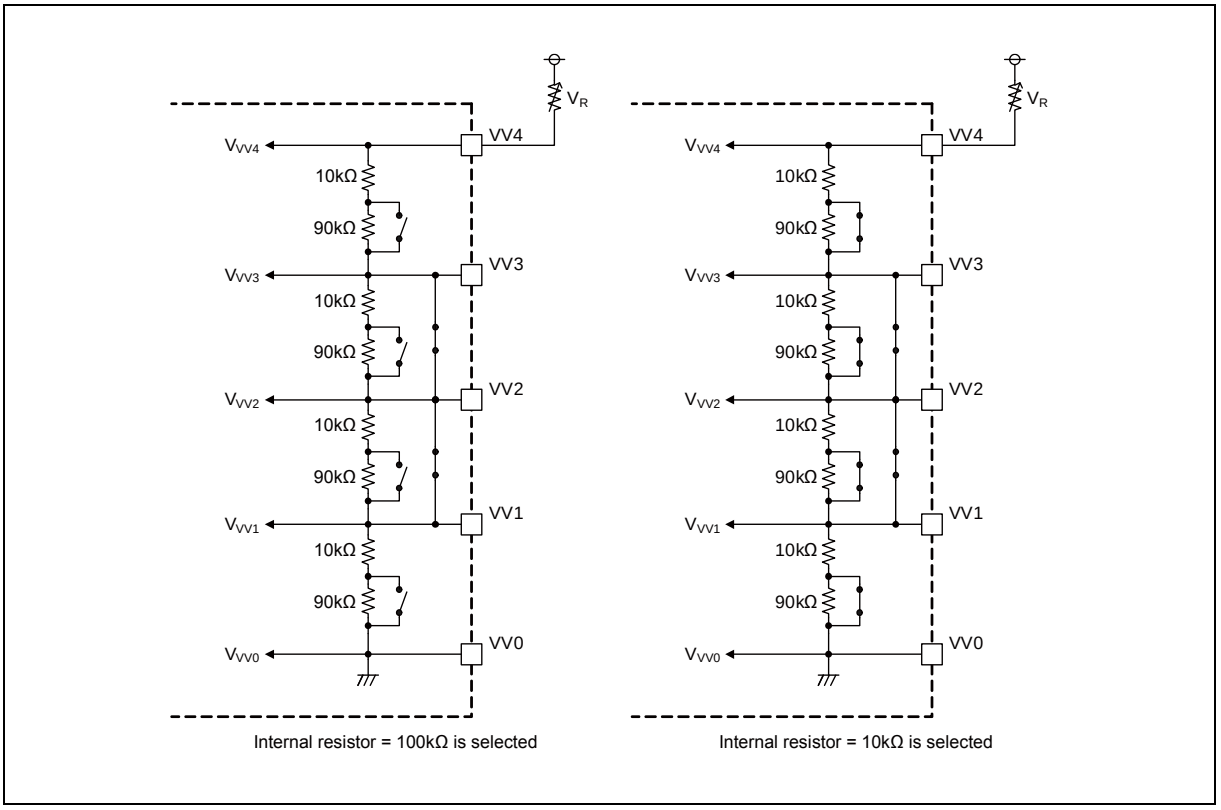


Figure 2-5 Internal Divider Resistors for 1/2 Bias Generation



2.2 External Divider Resistor for LCD Controller

This Family allows connecting external divider resistors to pins VV0 to VV4.
Connecting a variable resistor between pins VCC and VV4 allows brightness adjustment.

External Divider Resistor

External divider resistors can be connected to the LCD drive power pins (VV0 to VV4) without using the internal divider resistors. External divider resistor connection corresponding to bias system is shown in Figure 2-6, LCD drive voltage is shown in Table 2-1.

Figure 2-6 Examples of External Divider Resistor Connection

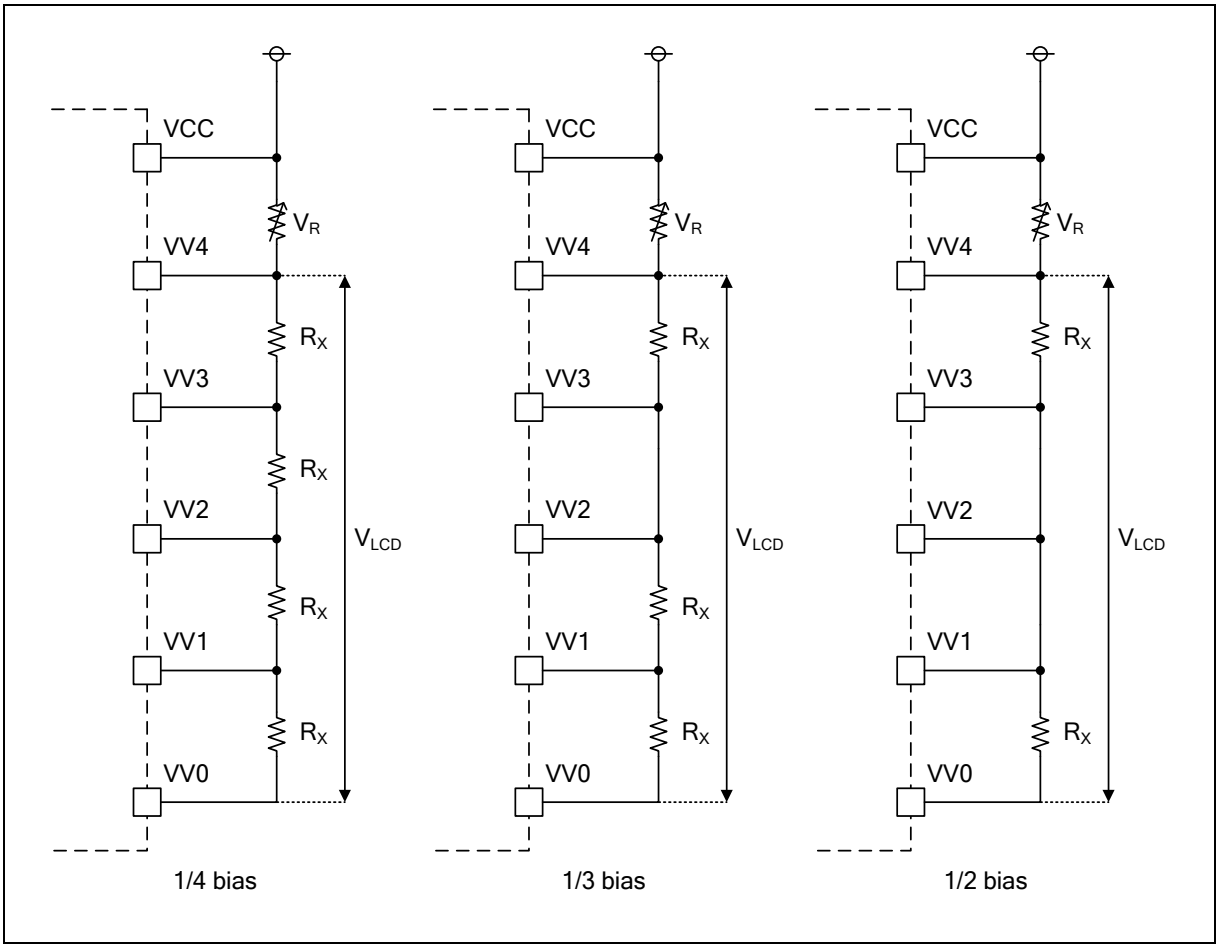


Table 2-1 LCD Drive Voltage Setting

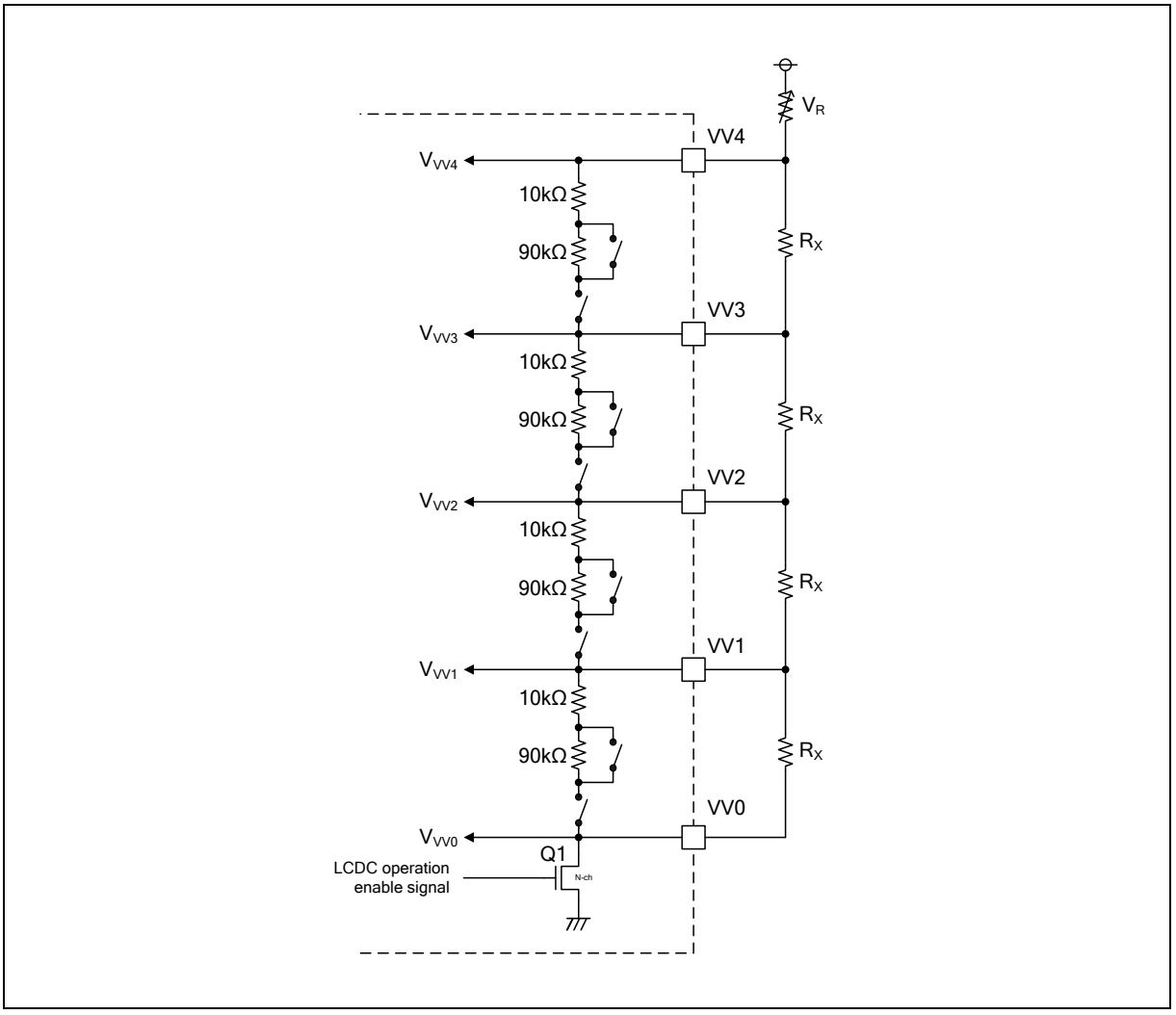
	V_{VV4}	V_{VV3}	V_{VV2}	V_{VV1}	V_{VV0}
1/2 bias	V_{LCD}	1/2 V_{LCD}	1/2 V_{LCD}	1/2 V_{LCD}	GND
1/3 bias	V_{LCD}	2/3 V_{LCD}	2/3 V_{LCD}	1/3 V_{LCD}	GND
1/4 bias	V_{LCD}	3/4 V_{LCD}	1/2 V_{LCD}	1/4 V_{LCD}	GND

V_{LCD}: LCD operating voltage

Using External Divider Resistor

Pin VV0 is internally connected to Vss (GND) through a transistor. When external divider resistors are used, connecting Vss side of the divider resistors to the pin VV0 allows cutting off the current through the resistors when LCD controller is stopped. Figure 2-7 shows the picture when external divider resistors are used.

Figure 2-7 External Divider Resistors Used



1. To connect external divider resistors without any effect from the internal divider resistor, "0" must be written to the LCD drive voltage control bit (LCDCC1:VSEL) of LCDC Control Register 1 to disconnect entire internal divider resistors. When you use the ports as LCD drive power pins, write "1" to the selection bits VV4 to VV0 (LCDCC3:VE4 to VE0) of LCDC Control Register 3.
2. When a value other than "000" is written to display mode selection bits (LCDCC1:MS[2:0]) of LCDCC1 Register, LCDC operation enable transistor (Q1) becomes "ON" allowing current through the external divider resistors.
3. When "000" is written to the display mode selection bits (MS[2:0]), the LCDC operation enable transistor (Q1) becomes "OFF" to cut off the current through the external divider resistors.

Note:

- *The most appropriate value of the external resistor R_X depends on your LCD panel. Choose a resistor value which suits your LCD panel.*

2.3 Pins

This section describes the pins of the LCD controller.

Pins of LCD Controller

Pins of LCD controller consist of 8 common output pins (COM0 to COM7), up to 44 segment output pins (SEG00 to SEG43) and 5 LCD drive power pins (VV0 to VV4), and all these pins are shared by general purpose input/output ports.

When you use these pins as LCD controller pins, set bits to "1" where they correspond to CDC Control Register 3(LCDCC3), LCDC COM Output Enable Register (LCDC_COMEN) or LCDC SEG Output Enable Register 1/2 (LCDC_SEGEN1/2).

When you use these pins as general purpose input/output ports, set bits to "0" where they correspond to LCDC Control Register 3(LCDCC3), LCDC COM Output Enable Register (LCDC_COMEN) or LCDC SEG Output Enable Register 1/2 (LCDC_SEGEN1/2) before setting the I/O port input control bit (PICTL) of LCDC Control Register 3 (LCDCC3) to "1".

- Pins COM0 to COM7

In 8 COM mode, pins COM0 to COM7 can be used as common output pins.

In 4 COM mode, pins COM0 to COM3 can be used as common output pins. Products with COM4 to COM7 pins shared with SEG pins allow using them as SEG output pins.

- Pins SEG00 to SEG43

In 8 COM mode, pins SEG00 to SEG39 can be used as segment output pins.

In 4 COM mode, pins SEG00 to SEG43 can be used as segment output pins.

- Pins VV0 to VV4

These pins are LCD drive power pins.

When you use internal divider resistors, pins VV0 to VV3 allow you to check the internal voltages.

The LCD drive power may be supplied from the external circuit.

- Pins C0/C1

These pins are LCD booster external capacitance pins.

When you use internal booster charge pump function, you should configure LCDC_BOOSTER :CENSEL to ‘1’ to enable booster external capacitance.

3. Operations

This section describes the operations of the LCD controller.

Modes of LCD Controller

Table 3-1 shows display modes and combinations of bias available for LCD controller.

Table 3-1 Combination of Display Mode and Bias

Display Mode LCDCC1:MS[2:0]	1/2 Bias	1/3 Bias	1/4 Bias
001 (4 COM mode, 1/2 duty)	○	×	×
010 (4 COM mode, 1/3 duty)	×	○	×
011 (4 COM mode, 1/4 duty)	×	○	×
100 (8 COM mode, 1/3 duty, LCDCC3:BLS8=0)	×	○	×
100 (8 COM mode, 1/4 duty, LCDCC3:BLS8=1)	×	×	○

○: Setting allowed

×: Setting prohibited

Operation States of LCD Controller

Operation states of CPU operation mode for LCD controller are shown in Table 3-2.

Table 3-2 Operation States of LCD Controller

CPU Operation Mode		Operation States
Run mode		Operable
Standby mode	Sleep mode	Operable
	Timer mode	Operable*
	RTC mode	Not operable
	Stop mode	
Deep standby mode	Deep standby RTC mode	Not operable
	Deep standby Stop mode	

*: LCDC interrupt request will not be generated.

Notes:

- *As PCLK stops in timer mode, when you run the LCD controller in timer mode, select sub-clock as LCDC source clock before moving to the timer mode.*
- *As LCD controller will not run in RTC/stop mode or deep standby mode, move to RTC/stop mode or deep standby mode after display for LCD controller is stopped (LCDCC1:MS[2:0]=000).*

3.1 LCD Drive Waveform

By its nature, LCD causes deterioration to its LCD elements if DC driven because the LCD elements are affected by chemical changes. To avoid this situation, the LCD controller incorporates AC waveform generator to generate AC waveform consisting of 2 frames allowing driving the LCD. Output waveform consists of the following 5 types.

8 COM mode:

- 1/3 bias, 1/8 duty output waveform
- 1/4 bias, 1/8 duty output waveform

4 COM mode:

- 1/2 bias, 1/2 duty output waveform
- 1/3 bias, 1/3 duty output waveform
- 1/3 bias, 1/4 duty output waveform

3.1.1 Output Waveform of LCD Controller in 8 COM Mode (1/3 Bias, 1/8 Duty)

In 8 COM mode with 1/3 bias and 1/8 duty, COM0 to COM7 are used for display.

Example of Output Waveform in 8 COM Mode with 1/3 Bias, 1/8 Duty

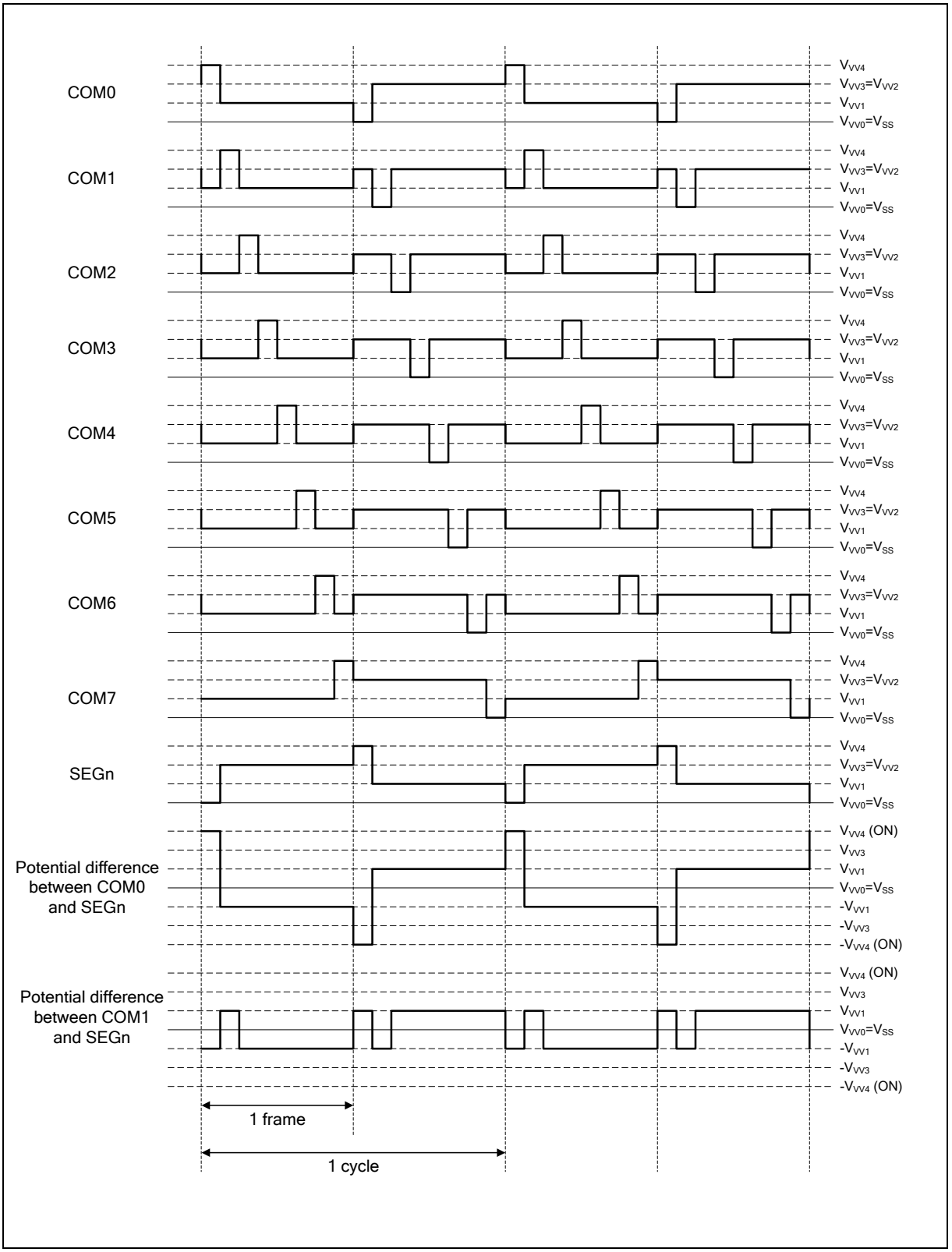
Liquid crystal elements of display with maximum potential difference between common outputs and segment outputs turn "ON".

Output waveforms when the contents of LCDRAM are Table 3-3 are shown in Figure 3-1.

Table 3-3 Example of LCDRAM Contents

Segment	LCDRAM Contents							
	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
SEGn	0	0	0	0	0	0	0	1

Figure 3-1 Example of Output Waveform in 8 COM Mode, 1/3 Bias, 1/8 Duty Ratio



3.1.2 Output Waveform of LCD Controller in 8 COM Mode (1/4 Bias, 1/8 Duty)

In 8 COM mode with 1/4 bias and 1/8 duty, COM0 to COM7 are used for display.

Example of Output Waveform in 8 COM Mode with 1/4 Bias, 1/8 Duty

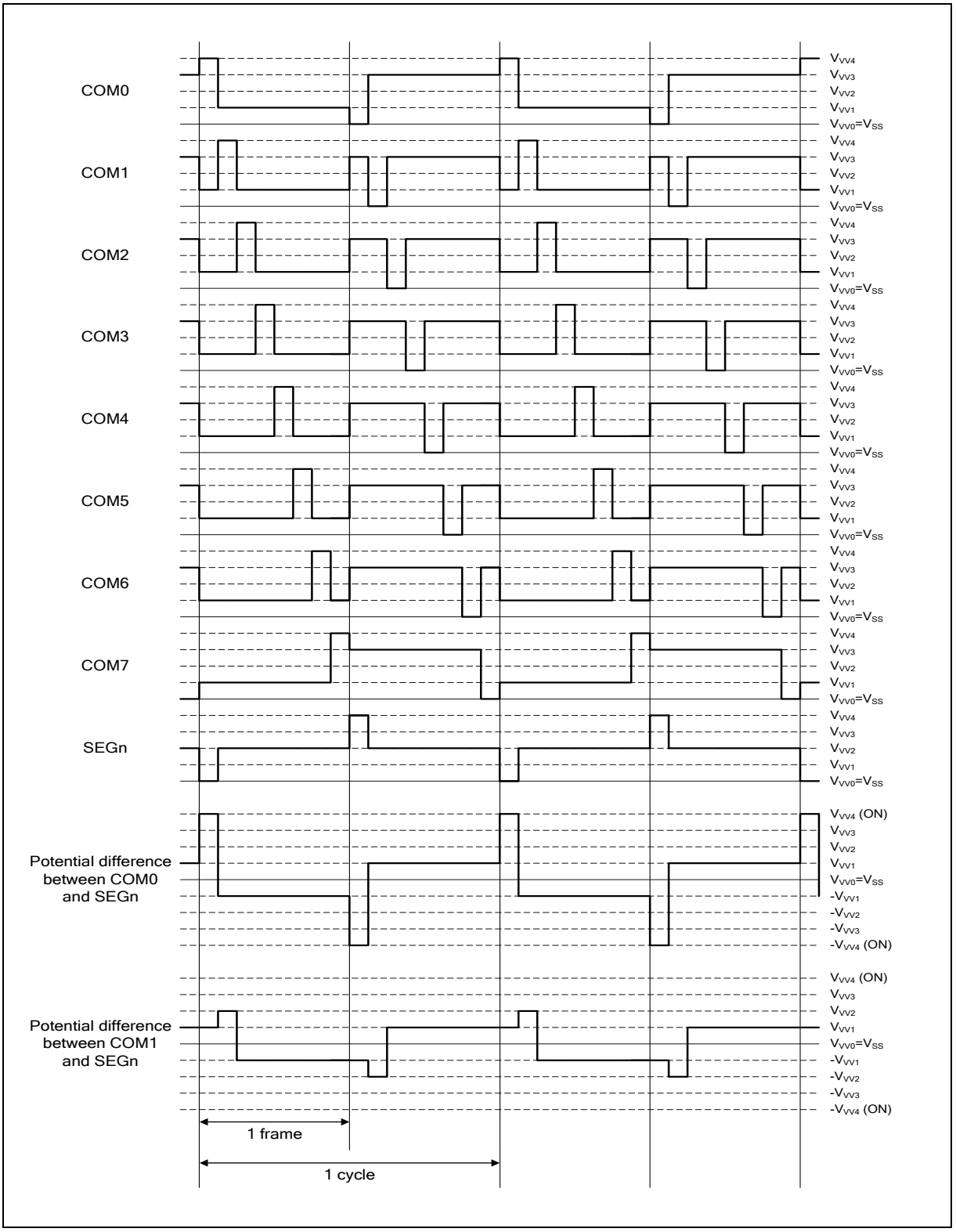
Liquid crystal elements of display with maximum potential difference between common outputs and segment outputs turn "ON".

Output waveforms when the contents of LCDRAM are Table 3-4 are shown in Figure 3-2.

Table 3-4 Example of LCDRAM Contents

Segment	LCDRAM Contents							
	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
SEGn	0	0	0	0	0	0	0	1

Figure 3-2 Example of Output Waveform in 8 COM Mode, 1/4 Bias, 1/8 Duty Ratio



3.1.3 Output Waveform of LCD Controller in 4 COM Mode (1/2 Bias, 1/2 Duty)

Display drive outputs consist of AC waveform of 2 separate drive type frames.
In 4 COM mode with 1/2 bias and 1/2 duty, COM0 and COM1 are used for display and COM2 and COM3 are not used.

Example of Output Waveform in 4 COM Mode with 1/2 Bias, 1/2 Duty

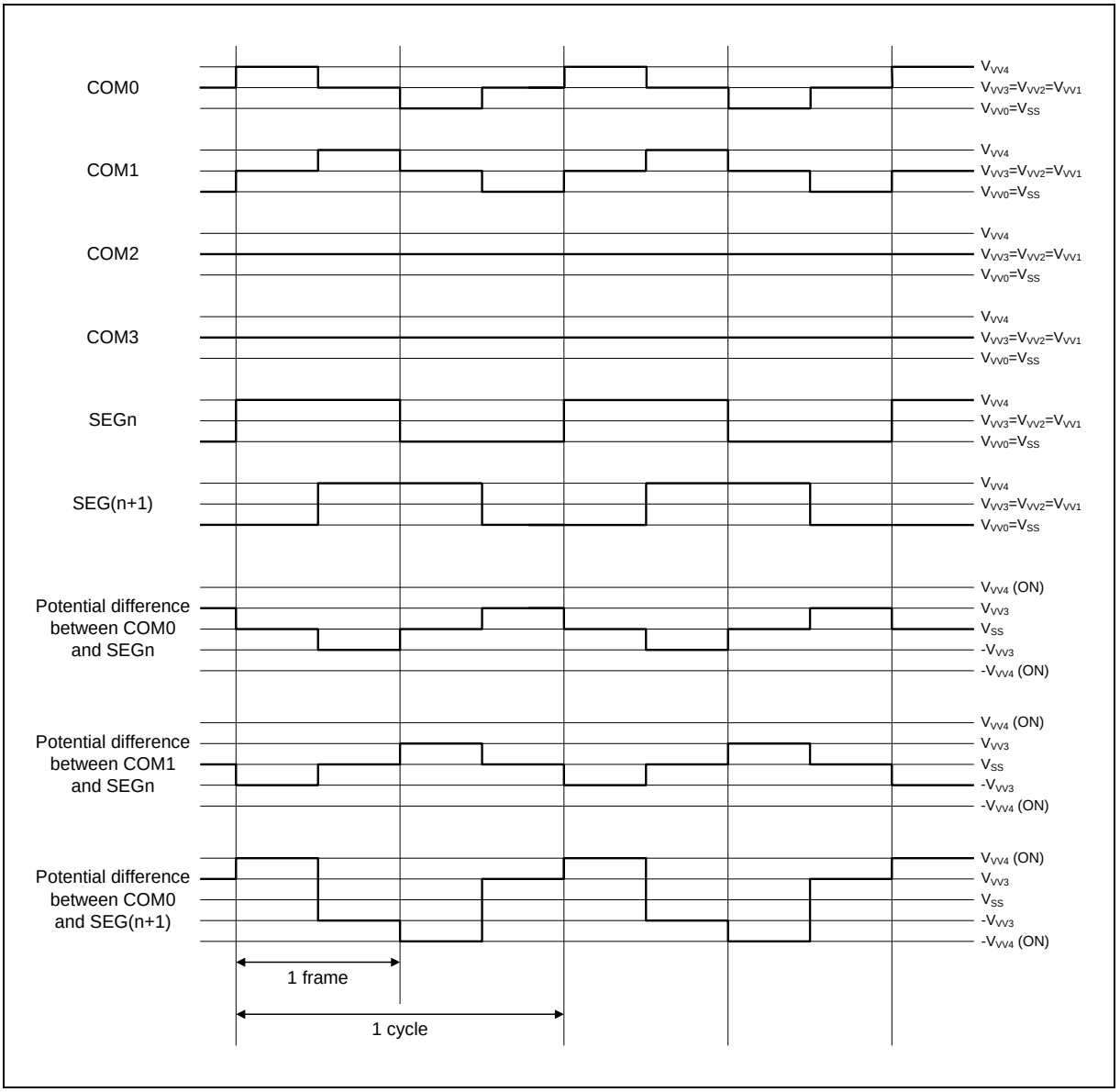
Liquid crystal elements of display with maximum potential difference between common outputs and segment outputs turn "ON".
Output waveforms when the contents of LCDRAM are Table 3-5 are shown in Figure 3-3.

Table 3-5 Example of LCDRAM Contents

Segment	LCDRAM Contents			
	COM3	COM2	COM1	COM0
SEGn	–	–	0	0
SEG(n+1)	–	–	0	1

–: Not used

Figure 3-3 Example of Output Waveform in 4 COM Mode, 1/2 Bias, 1/2 Duty Ratio



3.1.4 Output Waveform of LCD Controller in 4 COM Mode (1/3 Bias, 1/3 Duty)

In 4 COM mode with 1/3 bias and 1/3 duty, COM0, COM1 and COM2 are used for display and COM3 is not used.

Example of Output Waveform in 4 COM Mode with 1/3 Bias, 1/3 Duty

Liquid crystal elements of display with maximum potential difference between common outputs and segment outputs turn "ON".

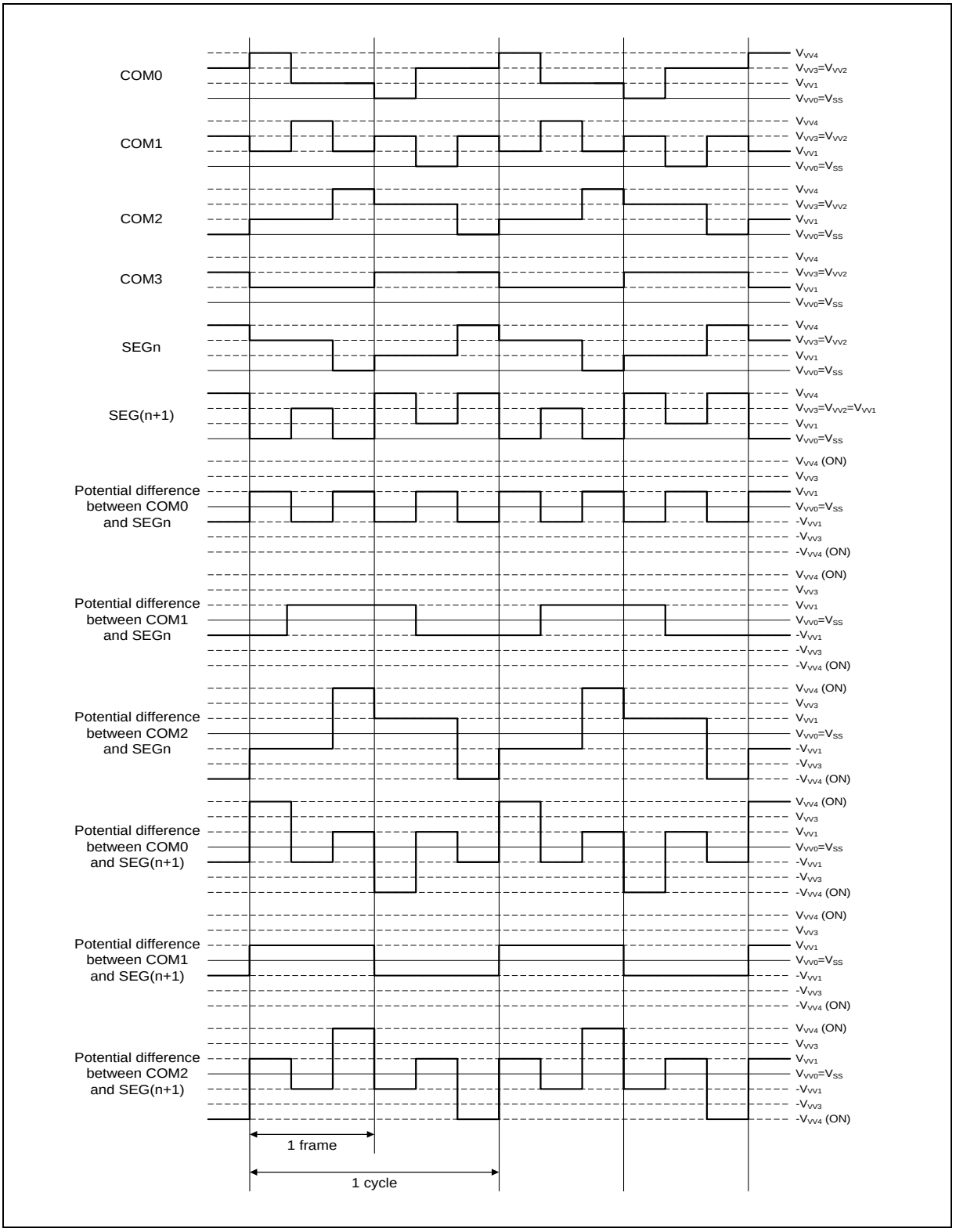
Output waveforms when the contents of LCDRAM are Table 3-6 are shown in Figure 3-4.

Table 3-6 Example of LCDRAM Contents

Segment	LCDRAM Contents			
	COM3	COM2	COM1	COM0
SEGn	–	1	0	0
SEG(n+1)	–	1	0	1

–: Not used

Figure 3-4 Example of Output Waveform in 4 COM Mode, 1/3 Bias, 1/3 Duty Ratio



3.1.5 Output Waveform of LCD Controller in 4 COM Mode (1/3 Bias, 1/4 Duty)

In 4 COM mode with 1/3 bias and 1/4 duty, COM0 to COM3 are used for display.

Example of Output Waveform in 4 COM Mode with 1/3 Bias, 1/4 Duty

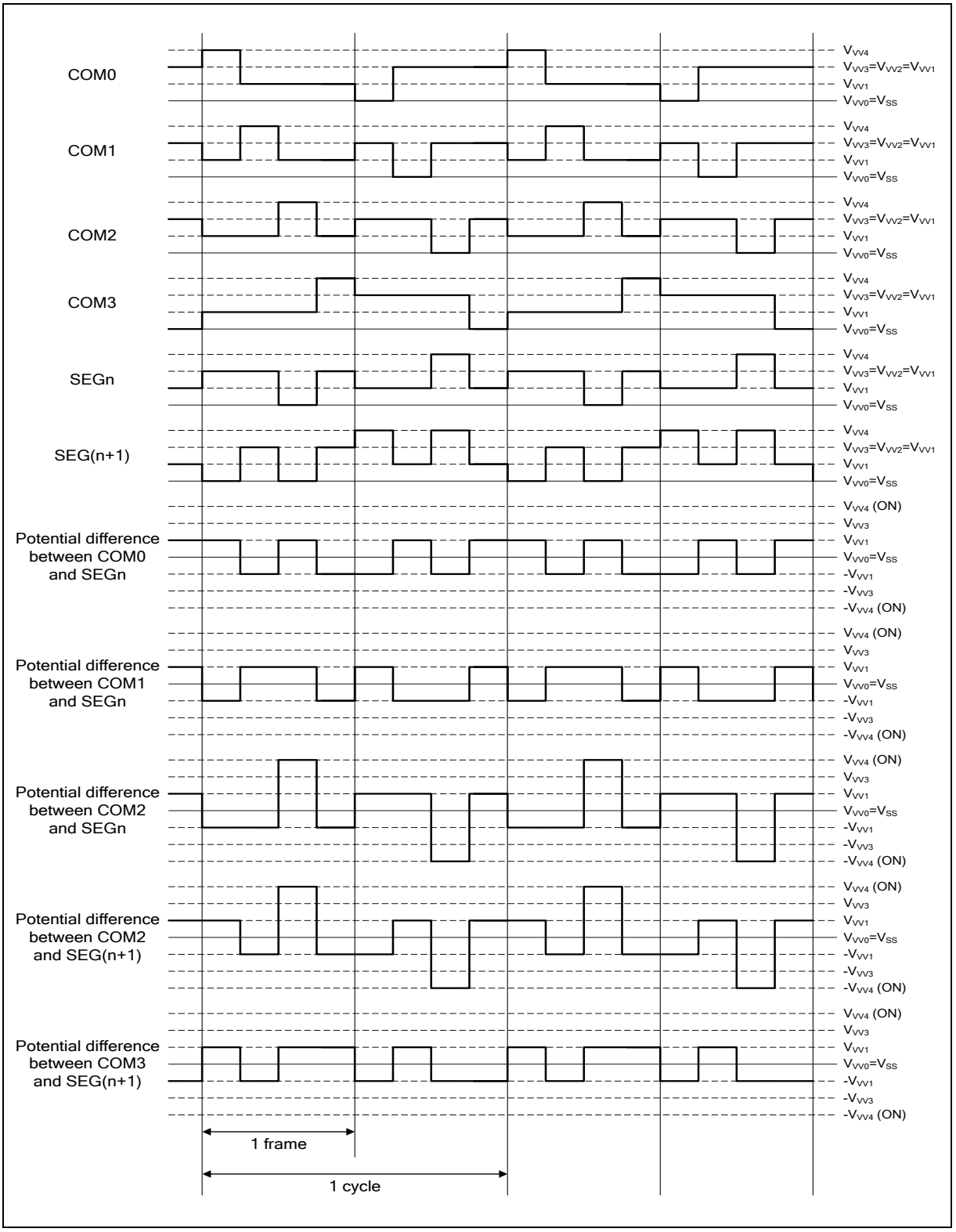
Liquid crystal elements of display with maximum potential difference between common outputs and segment outputs turn "ON".

Output waveforms when the contents of LCDRAM are Table 3-7 are shown in Figure 3-5.

Table 3-7 Example of LCDRAM Contents

Segment	LCDRAM Contents			
	COM3	COM2	COM1	COM0
SEGn	0	1	0	0
SEG(n+1)	0	1	0	1

Figure 3-5 Example of Output Waveform in 4 COM Mode, 1/3 Bias, 1/4 Duty Ratio



3.2 Interrupts of LCD Controller

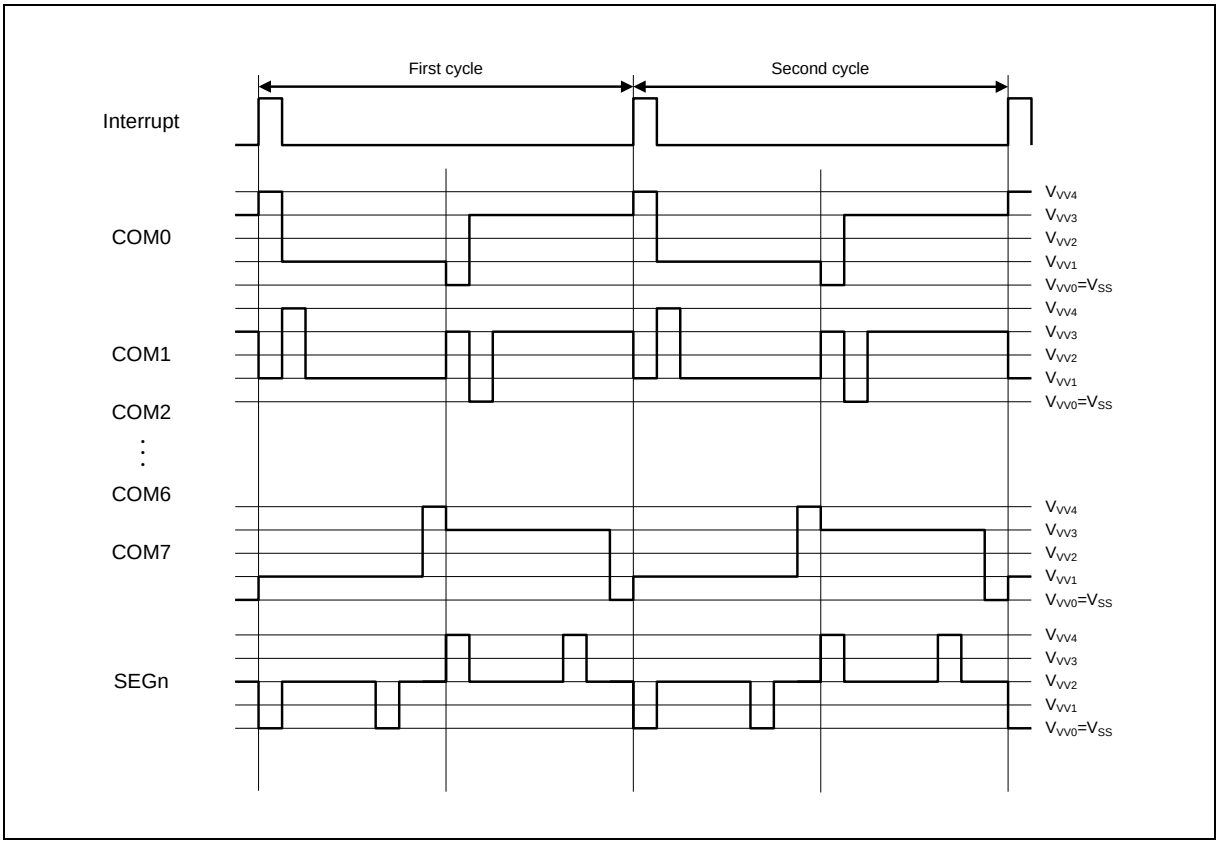
The LCD controller generates interrupts synchronized with LCD cycle.

Interrupts of LCD Controller

After 1 cycle process is completed, LCD controller sets LCDC interrupt request flag bit (LCDCC2:LCDIF) to "1". If interrupt request has already been enabled (LCDCC2:LCDIEN = 1) when the LCDIF bit is set to "1", LCD controller issues an interrupt request to the interrupt controller. To clear the interrupt request, write "0" to the LCDIF bit with interrupt routine.

LCD controller always sets the LCDIF bit to "1" after 1 cycle process is completed independent of the LCDIEN value. If both LCDIF and LCDIEN bits are still "1" after an LCDC interrupt request is issued, CPU is not able to recover from the interrupt process. Always clear the LCDIF bit to "0" after an LCDC interrupt request is issued so that CPU is able to recover from the interrupt process.

Figure 3-6 Interrupt Timing



3.3 Display Data Memory of LCD Controller

The sizes of display data memory (LCD RAM) in 8 COM mode and 4 COM mode are different from each other.
In 8 COM mode, LCD RAM holds up to 40 × 8 bits (40 bytes) for segment output signal generation.
In 4 COM mode, LCD RAM holds up to 44 × 4 bits (22 bytes) for segment output signal generation.

Display Data Memory and Output Pin

The contents of the display data memory (LCDRAM) are automatically read at common signal selection timing, synchronized and output to segment output pins.
Bits with "1" are converted to a selected voltage (LCD is displayed) and bits with "0" are converted to a non-selected voltage (LCD is not displayed) to output.
LCD display operation is asynchronous with CPU operation allowing write/read to/from LCDRAM at a random timing. Pins not specified as segment outputs can be used as input/output ports and corresponding LCDRAM can be used as usual general purpose registers. Table 3-8 shows the relation between duty, common outputs and LCRAM bits used.
Figure 3-7 and Figure 3-8 show LCDRAM address allocation for common outputs and segment output pins in 8 COM mode and 4 COM mode.

Figure 3-7 LCDRAM and Common/Segment Output Pin (8 COM Mode)

Base_Address(n) +Adress									
n	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	SEG00
n+1	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	SEG01
n+2	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	SEG02
n+3	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	SEG03
n+4	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	SEG04
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
n+36	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	SEG36
n+37	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	SEG37
n+38	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	SEG38
n+39	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	SEG39
	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0	

Range and COM pins used for 1/8 duty ratio

Figure 3-8 LCDRAM and Common/Segment Output Pin (4 COM Mode)

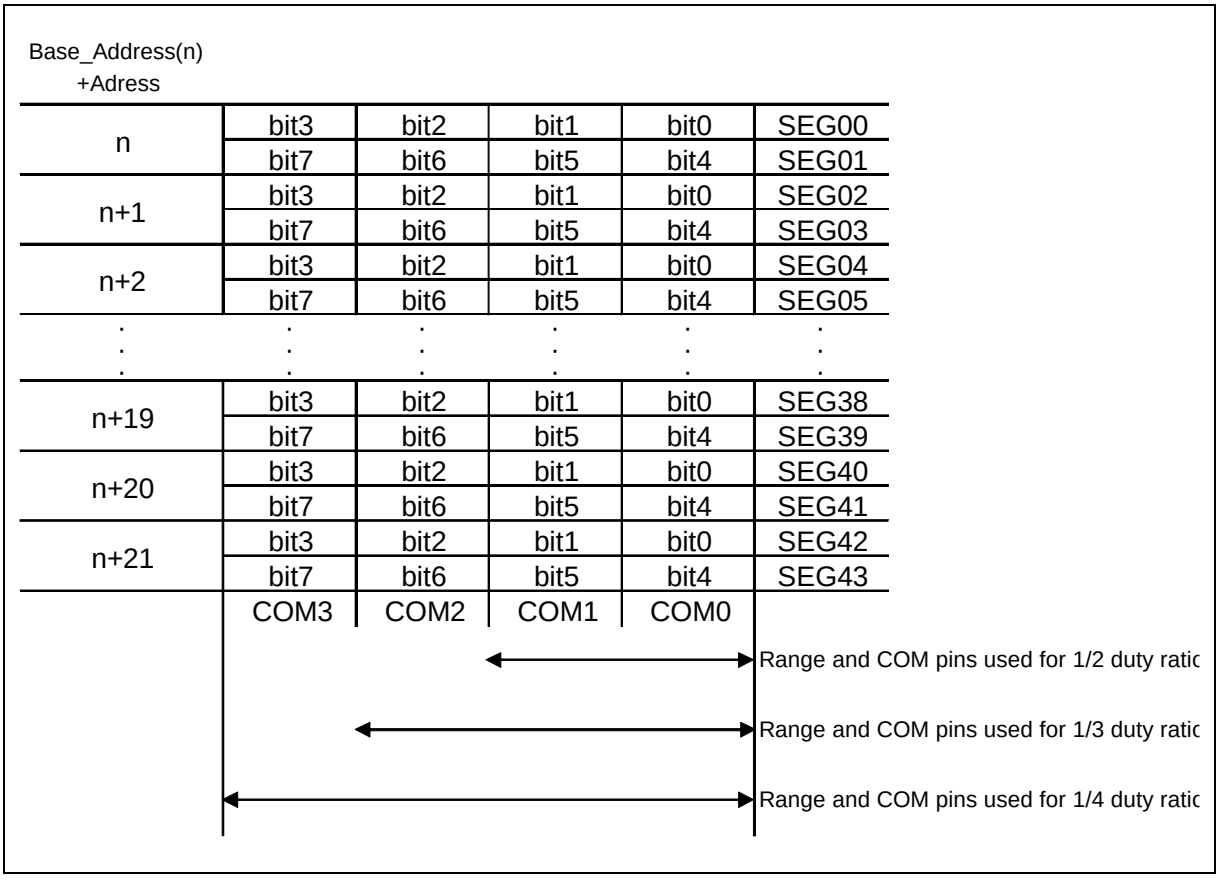


Table 3-8 Relation between Duty Ratio, Common Output and LCDRAM Bit Used

Duty Ratio	Common Output Used	Display Data Bits Used							
		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
1/2	COM0, COM1 (2)	–	–	○	○	–	–	○	○
1/3	COM0 to COM2 (3)	–	○	○	○	–	○	○	○
1/4	COM0 to COM3 (4)	○	○	○	○	○	○	○	○
1/8	COM0 to COM7 (8)	○	○	○	○	○	○	○	○

○ : Bit used

– : Bit not used

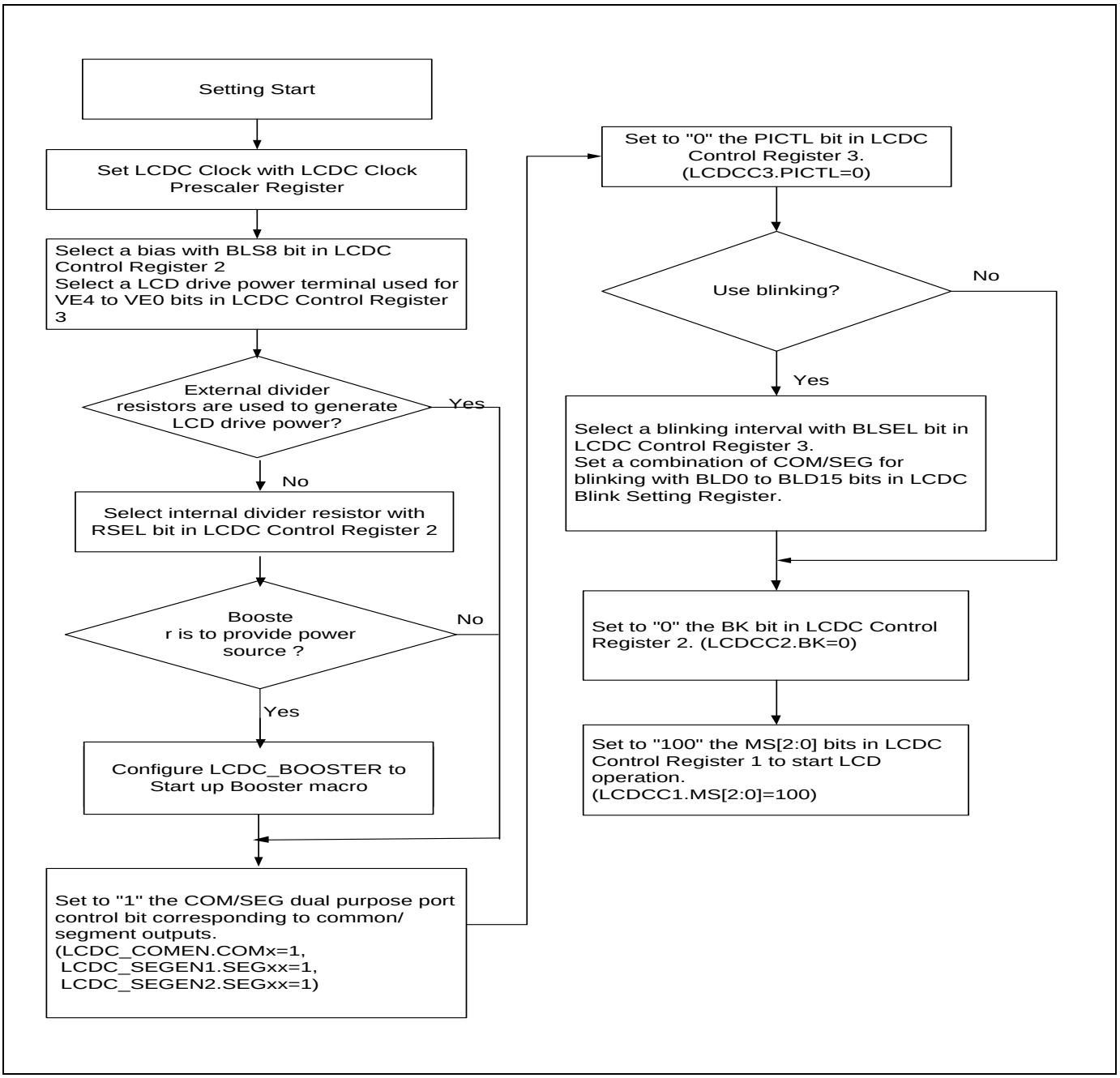
4. Setting Procedure Examples

This section provides examples of procedure for setting the LCD controller.

Setting Procedure in 8 COM Mode

Figure 4-1 shows setting procedure in 8COM mode.

Figure 4-1 LCD Controller Setting Procedure in 8 COM Mode

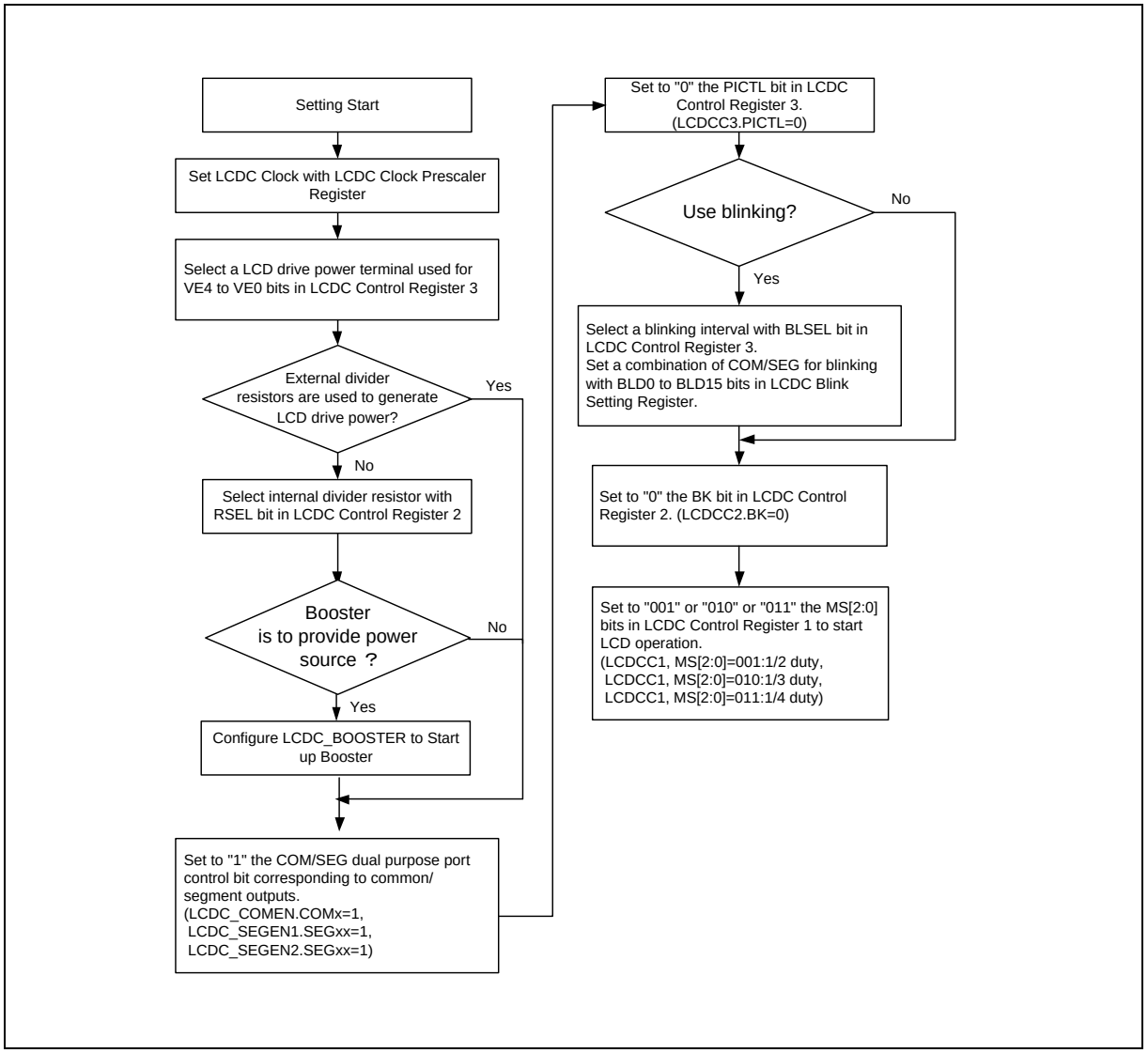


- After setting by Figure 4-1, drive waveform for LCD panel will be output to common/segment output pins according to the settings of LCDRAM and LCDC registers.
- Select output pins for LCD with LCDC Control Register 3 (LCDCC3), LCDC COM Output Enable Register (LCDC_COMEN) and LCDC SEG Output Enable Register 1/2 (LCDC_SEGEN1/2). Pins not selected as common/segment output pins can be used as general purpose input/output ports.
- LCDC clock can be switched even if LCD is being displayed.
  However, as flicker may be found in the LCD display, set BK bit of LCDC Control Register 2 to "1" (LCDCC2:BK=1) that shows a blank screen, and then switch the LCDC clock.
- Display drive outputs consist of AC waveform in 2 frames which are determined with bias and duty settings.
- When you use blink function, set bits to "1" where they correspond to LCDC Blink Setting Register (LCDC_BLINK). The blinking interval can be selected from 2 types with BLSEL bit of LCDC Control Register 3 (LCDCC3).

Setting Procedure in 4 COM Mode

Figure 4-2 shows setting procedure in 4 COM mode.

Figure 4-2 LCD Controller Setting Procedure in 4 COM Mode



- After setting by Figure 4-2, drive waveform for LCD panel will be output to common/segment output pins according to the settings of LCDRAM and LCDC registers.
- Select output pins for LCD with LCDC Control Register 3 (LCDCC3), LCDC COM Output Enable Register (LCDC_COMEN) and LCDC SEG Output Enable Register 1/2 (LCDC_SEGEN1/2). Pins not selected as common/segment output pins can be used as general purpose input/output ports.
- LCDC clock can be switched even if LCD is being displayed.
  However, as flicker may be found in the LCD display, set BK bit of LCDC Control Register 2 to "1" (LCDCC2:BK=1) that shows a blank screen, and then switch the LCDC clock.
- Display drive outputs consist of AC waveform in 2 frames which are determined with bias and duty settings.

- When you use blink function, set bits to "1" where they correspond to LCDC Blink Setting Register (LCDC_BLINK). The blinking interval can be selected from 2 types with BLSEL bit of LCDC Control Register 3 (LCDCC3).

5. Registers

This section describes the registers of the LCD controller.

List of Registers of LCD Controller

Table 5-1 List of Registers of LCD Controller

Abbreviation	Register Name	Reference
LCDCC1	LCDC Control Register 1	5.1
LCDCC2	LCDC Control Register 2	5.2
LCDCC3	LCDC Control Register 3	5.3
LCDC_BOOSTER	LCDC Booster Control Register	5.4
LCDC_PSR	LCDC Clock Prescaler Register	5.5
LCDC_COMEN	LCDC COM Output Enable Register	5.6
LCDC_SEGEN1	LCDC SEG Output Enable Register 1	5.7
LCDC_SEGEN2	LCDC SEG Output Enable Register 2	5.8
LCDC_BLINK	LCDC Blink Setting Register	5.9
LCDRAM00 to LCDRAM39	Display Data Memory Register 00 to 39	5.10

5.1 LCDC Control Register 1 (LCDCC1)

The LCDC Control Register 1 (LCDCC1) is used to set up LCD controller.

Register Configuration

bit	7	6	5	4	3	2	1	0
Field	Reserved	LCDEN	VSEL	MS[2:0]			Reserved	
Attribute	-	R/W	R/W	R/W			-	
Initial Value	0	0	0	000			00	

Register Functions

[bit7] Reserved: Reserved bits

"0" is always read. Write does not affect these bits.

[bit6] LCDEN: Timer mode operation enable bit

Bit	Description
0	LCD controller stops running in timer mode.
1	LCD controller runs in timer mode.

Note:

- *PCLK stops in timer mode. When you run the LCF controller in timer mode, select sub-clock as LCDC clock source (LCDC_PSR:CLKSEL=0) before transiting to timer mode.*

[bit5] VSEL: LCD drive power control bit

Bit	Description
0	External divider resistors are used to create LCD drive power.
1	Internal divider resistors are used to create LCD drive power.

[bit4:2] MS[2:0]: LCD controller display mode selection bits

bit4:2	Description
000	LCD controller stops display operations.
001	4 COM mode, 1/2 duty
010	4 COM mode, 1/3 duty
011	4 COM mode, 1/4 duty
1xx	8 COM mode, 1/8 duty

[bit1:0] Reserved: Reserved bits

"0" is always read. Write does not affect these bits.

5.2 LCDC Control Register 2 (LCDCC2)

The LCDC Control Register 2 (LCDCC2) is used to set up LCD controller.

Register Configuration

bit	15	14	13	12	11	10	9	8
Field	Reserved		RSEL	BLS8	INV	BK	LCDIEN	LCDIF
Attribute	-		R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	00		0	1	0	1	0	0

Register Functions

[bit15:14] Reserved: Reserved bits

"0" is always read. Write does not affect these bits.

[bit13] RSEL: Divider resistor value selection bit

This bit is used to select a value of divider resistor when internal divider resistor is selected (LCDCC1:VSEL="1").

Bit	Description
0	100 kΩ resistors are selected.
1	10 kΩ resistors are selected.

[bit12] BLS8: 8 COM mode bias selection bit

Bit	Description
0	1/3 bias is selected in 8 COM mode.
1	1/4 bias is selected in 8 COM mode.

Note:

- *In 4 COM mode, LCD controller operations will not be affected.*

[bit11] INV: Reverse display control bit

Bit	Description
0	Display is not reversed.
1	Display is reversed.

[bit10] BK: Blank display control bit

Bit	Description
0	Data stored in LCDRAM (LCDRAM00 to 43) is displayed.
1	Blank is displayed independent of data stored in LCDRAM (LCDRAM00 to 43).

[bit9] LCDIEN: Interrupt enable bit

Bit	Description
0	Disables interrupt request.
1	Enables interrupt request.

[bit8] LCDIF: Interrupt request detection bit

Bit	Description
0	No interrupt request is detected.
1	Interrupt request is detected.

5.3 LCDC Control Register 3 (LCDCC3)

The LCDC Control Register 3 (LCDCC3) is used to set up LCD controller.

Register Configuration

bit	23	22	21	20	19	18	17	16
Field	PICTL	BLSEL	VE4	VE3	VE2	VE1	VE0	Reserved
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-
Initial Value	0	0	1	1	1	1	1	0

Register Functions

[bit23] PICTL: I/O port input control bit

This bit controls I/O ports shared by COM and SEG.

Bit	Description
0	Input from I/O port is cut off. Suppresses short-circuit current when used as COM/SEG output pin.
1	Input from I/O port is not cut off.

Note:

- *As PICTL bit is initialized by a reset, set PICTL bit to "1" when you use I/O ports as input pins. However, the inputs from I/O ports which are set as COM/SEG pins with LCDC_COMEN, LCDC_SEG1 and LCDC_SEG2 registers will be cut off.*

[bit22] BLSEL: Blink interval selection bit

Bit	Description
0	$1/2^{14}$ of sub-clock is selected. If sub-clock is 32.768 [kHz], the interval becomes 0.5 [s].
1	$1/2^{15}$ of sub-clock is selected. If sub-clock is 32.768 [kHz], the interval becomes 1.0 [s].

[bit21] VE4: VV4 selection bit

Bit	Description
0	Functions as GPIO.
1	Functions as LCD drive power pin (VV4).

Note:

- *As VV4 pin cannot be used as GPIO when LCD controller is selected (LCDCC1:VSEL="1"), be sure to write "1" to VE4 bit.*

[bit20] VE3: VV3 selection bit

Bit	Description
0	Functions as GPIO.
1	Functions as LCD drive power pin (VV3).

[bit19] VE2: VV2 selection bit

Bit	Description
0	Functions as GPIO.
1	Functions as LCD drive power pin (VV2).

[bit18] VE1: VV1 selection bit

Bit	Description
0	Functions as GPIO.
1	Functions as LCD drive power pin (VV1).

[bit17] VE0: VV0 selection bit

Bit	Description
0	Functions as GPIO.
1	Functions as LCD drive power pin (VV0).

[bit16] Reserved: Reserved bit

"0" is always read. Write does not affect this bit.

Note:

- *When internal divider resistor is selected (LCDCC1:VSEL="1"), pins VV3 to VV0 can be used as GPIO.*

5.4 LCDC Booster Control Register (LCDC_BOOSTER)

The LCDC Booster Control Register (LCDC_BOOSTER) is used to configure LCD booster function.

Register Configuration

bit	15	14	13	12	11	10	9	8
Field	Reserved		BTRC[1:0]		BTRF[3:0]			
Attribute	-		R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0		0	0	1	1	1	0

Bit	7	6	5	4	3	2	1	0
Field	Reserved				CENSEL	PSF	BSTPD	BSTOPT
Attribute	-	-	-	-	R/W	R	R/W	R/W
Initial Value	0	0	0	0	0	0	1	1

Register Functions

[bit15:14] Reserved: Reserved bits

"0" is always read. Write does not affect these bits.

[bit13:12] BTRC: Booster coarse setting bits

[bit11:8] BTRF: Booster fine setting bits

The combination between BTRF and BTRC are list as following table:

Permitted Setting *1		Output VV1 Voltage (Unit-V)	Output VV2 Voltage (Unit-V)	Output VV3 Voltage (Unit-V)	Output VV4 Voltage (Unit-V)	Remark
BTRC[1:0]	BTRF[3:0]					
00	1010	1.00	2.00	3.00	4.00	It can be set in 1/4 BIAS. Other BIAS setting is inhibited.
00	1011	1.05	2.10	3.15	4.20	
00	1100	1.10	2.20	3.30	4.40	
00	1101	1.15	2.30	3.45	4.60	
00	1110	1.20	2.40	3.60	4.80	
01	0111	1.25	2.50	2.50	3.75	It can be set in 1/3 BIAS. Other BIAS setting is inhibited
01	1000	1.30	2.60	2.60	3.90	
01	1001	1.35	2.70	2.70	4.05	
01	1010	1.40	2.80	2.80	4.20	
01	1011	1.45	2.90	2.90	4.35	
01	1100	1.50	3.00	3.00	4.50	
01	1101	1.55	3.10	3.10	4.65	
01	1110	1.60	3.20	3.20	4.80	
10	0101	1.65	3.30	3.30	4.95	

Permitted Setting *1		Output VV1 Voltage (Unit-V)	Output VV2 Voltage (Unit-V)	Output VV3 Voltage (Unit-V)	Output VV4 Voltage (Unit-V)	Remark
BTRC[1:0]	BTRF[3:0]					
10	1100	2.00	2.00	2.00	4.00	It can be set in 1/2 BIAS. Other BIAS setting is inhibited
10	1101	2.05	2.05	2.05	4.10	
10	1110	2.10	2.10	2.10	4.20	
11	0010	2.15	2.15	2.15	4.30	
11	0011	2.20	2.20	2.20	4.40	
11	0100	2.25	2.25	2.25	4.50	
11	0101	2.30	2.30	2.30	4.60	
11	0110	2.35	2.35	2.35	4.70	
11	0111	2.40	2.40	2.40	4.80	
11	1000	2.45	2.45	2.45	4.90	

*1: Other setting combinations are inhibited.

[bit7:4] Reserved: Reserved bits

"0" is always read. Write does not affect these bits.

[bit3] CENSEL: Booster C1/C0 pin enable control

Bit	Description
0	Booster C0/C1 pin function is disable
1	Booster C0/C1 pin function is enable

[bit2] PSF: LCDC power source flag bit

Bit	Description
0	Indicated that VCC of MCU as LCDC power supply is selected
1	Indicated that internal VV4 output as LCDC power supply is selected

Note: This bit is automatically set if LCD booster function is power on.

And it is automatically cleared if LCD booster is power down.

[bit1] BSTPD: Booster Power down control bit

Bit	Description
0	Booster charge pump is power on
1	Booster charge pump is power down

[bit0] BSTOPT: Booster module option

Bit	Description
0	MCU does not have booster function
1	MCU has booster function

Note: Only if the MCU has booster function, the configuration of booster related register could be available.

5.5 LCDC Clock Prescaler Register (LCDC_PSR)

The LCDC Clock Prescaler Register (LCDC_PSR) is used to set up LCD clock.

Register Configuration

bit	31	23	22	21	0
Field	Reserved		CLKSEL	CLKDIV	
Attribute	-		R/W	R/W	
Initial Value	0_0000_0000		0	00_0000_0000_0000_0000_0000	

Register Functions

[bit31:23] Reserved: Reserved bits

"0" is always read. Write does not affect these bits.

[bit22] CLKSEL: Source clock selection bit

Bit	Description
0	Sub-clock is selected for LCDC source clock.
1	PCLK is selected for LCDC source clock.

[bit21:0] CLKDIV: LCDC clock division ratio setting bit

bit21:0	Description
00_0000_0000_0000_0000_0000	These bits set LCDC clock division ratio (1 to 2097153). Clock is divided by (CLKDIV setting value +1). e.g.: CLKDIV(=00_0000_0000_0000_0000_0000) + 1 ⇒ 1 division
00_0000_0000_0000_0000_0001	
•	
•	
11_1111_1111_1111_1111_1110	
11_1111_1111_1111_1111_1111	

5.6 LCDC COM Output Enable Register (LCDC_COMEN)

The LCDC COM Output Enable Register (LCDC_COMEN) controls outputs for COM output pins (COM0 to COM7).

Register Configuration

bit	31							8
Field	Reserved							
Attribute	-							
Initial Value	0x000000							

bit	7	6	5	4	3	2	1	0
Field	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Register Functions

[bit31:8] Reserved: Reserved bits

"0" is always read. Write does not affect these bits.

[bit7:4] COM7 to COM4: Dual purpose COM/SEG port control bits

These bits control I/O port status for COM4 to COM7 and analog switches for common outputs.
Products with COM4 to COM7 shared with segment output pins allow I/O port status control for SEGxx and analog switch control for segment outputs in 4 COM mode.
Writing to these bits in 4 COM mode from products not shared with SEGxx pins will not affect any operation.

bit7:4	Description
0	Target I/O ports are used as GPIO. Analog switches for COMx/SEGxx outputs turn off.
1	Target I/O ports are used as COMx/SEGxx output pins. Analog switches for COMx/SEGxx outputs turn on.

[bit3:0] COM3 to COM0: Dual purpose COM port control bit

These bits control I/O port status and analog switches for COM outputs.

bit3:0	Description
0	Target I/O ports are used as GPIO. Analog switches for COMx outputs turn off.
1	Target I/O ports are used as COMx output pins. Analog switches for COMx outputs turn on.

5.7 LCDC SEG Output Enable Register 1 (LCDC_SEGEN1)

The LCDC SEG Output Enable Register 1 (LCDC_SEGEN1) controls outputs for segment output pins (SEG00 to SEG31).

Register Configuration

bit	31	30	29	28	27	26	25	24
Field	SEG31	SEG30	SEG29	SEG28	SEG27	SEG26	SEG25	SEG24
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

bit	23	22	21	20	19	18	17	16
Field	SEG23	SEG22	SEG21	SEG20	SEG19	SEG18	SEG17	SEG16
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

bit	15	14	13	12	11	10	9	8
Field	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG09	SEG08
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Field	SEG07	SEG06	SEG05	SEG04	SEG03	SEG02	SEG01	SEG00
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Register Functions

[bit31:0] SEG31 to SEG00: Dual purpose SEG port control bits

These bits control I/O port status and analog switches for SEG outputs.

bit31:0	Description
0	Target I/O ports are used as GPIO. Analog switches for SEGxx outputs turn off.
1	Target I/O ports are used as SEGxx output pins. Analog switches for SEGxx outputs turn on.

5.8 LCDC SEG Output Enable Register 2 (LCDC_SEGEN2)

The LCDC SEG Output Enable Register 2 (LCDC_SEGEN2) controls outputs for segment output pins (SEG00 to SEG31).

Register Configuration

bit	31							8
Field	Reserved							
Attribute	-							
Initial Value	0x000000							

bit	7	6	5	4	3	2	1	0
Field	SEG39	SEG38	SEG37	SEG36	SEG35	SEG34	SEG33	SEG32
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Register Functions

[bit31:8] Reserved: Reserved bits

"0" is always read. Write does not affect these bits.

[bit7:0] SEG39 to SEG32: Dual purpose SEG port control bits

These bits control I/O port status and analog switches for SEG outputs.

bit7:0	Description
0	Target I/O ports are used as GPIO. Analog switches for SEGxx outputs turn off.
1	Target I/O ports are used as SEGxx output pins. Analog switches for SEGxx outputs turn on.

5.9 LCDC Blink Setting Register (LCDC_BLINK)

The LCDC Blink Setting Register (LCDC_BLINK) is used to control blinking.

8 COM mode: A combination of SEG00, SEG01 and COM0 to COM7 determines the dots to blink.

4 COM mode: A combination of SEG00 to SEG03 and COM0 to COM3 determines the dots to blink.

Register Configuration

bit	15	14	13	12	11	10	9	8
Field	BLD15	BLD14	BLD13	BLD12	BLD11	BLD10	BLD09	BLD08
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Field	BLD07	BLD06	BLD05	BLD04	BLD03	BLD02	BLD01	BLD00
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Register Functions

[bit15] BLD15: Blink operation control bit 15

Bit	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG03-COM3.
	8 COM mode	Blinking for SEG01-COM7.

[bit14] BLD14: Blink operation control bit 14

Bit	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG03-COM2.
	8 COM mode	Blinking for SEG01-COM6.

[bit13] BLD13: Blink operation control bit 13

Bit	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG03-COM1.
	8 COM mode	Blinking for SEG01-COM5.

[bit12] BLD12: Blink operation control bit 12

Bit	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG03-COM0.
	8 COM mode	Blinking for SEG01-COM4.

[bit11] BLD11: Blink operation control bit 11

Bit	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG02-COM3.
	8 COM mode	Blinking for SEG01-COM3.

[bit10] BLD10: Blink operation control bit 10

Bit	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG02-COM2.
	8 COM mode	Blinking for SEG01-COM2.

[bit9] BLD09: Blink operation control bit 9

Bit	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG02-COM1.
	8 COM mode	Blinking for SEG01-COM1.

[bit8] BLD08: Blink operation control bit 8

Bit	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG02-COM0.
	8 COM mode	Blinking for SEG01-COM0.

[bit7] BLD07: Blink operation control bit 7

Bit	Mode	Description
0	-	Blinking is disabled.
1	4COM mode	Blinking for SEG01-COM3.
	8COM mode	Blinking for SEG00-COM7.

[bit6] BLD06: Blink operation control bit 6

Bit	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG01-COM2.
	8 COM mode	Blinking for SEG00-COM6.

[bit5] BLD05: Blink operation control bit 5

Bit	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG01-COM1.
	8 COM mode	Blinking for SEG00-COM5.

[bit4] BLD04: Blink operation control bit 4

Bit	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG01-COM0.
	8 COM mode	Blinking for SEG00-COM4.

[bit3] BLD03: Blink operation control bit 3

Bit	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG00-COM3.
	8 COM mode	Blinking for SEG00-COM3.

[bit2] BLD02: Blink operation control bit 2

Bit	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG00-COM2.
	8 COM mode	Blinking for SEG00-COM2.

[bit1] BLD01: Blink operation control bit 1

Bit	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG00-COM1.
	8 COM mode	Blinking for SEG00-COM1.

[bit0] BLD00: Blink operation control bit 0

Bit	Mode	Description
0	-	Blinking is disabled.
1	4 COM mode	Blinking for SEG00-COM0.
	8 COM mode	Blinking for SEG00-COM0.

5.10 Display Data Memory Register 00 to 39 (LCDRAM00 to LCDRAM39)

The Display Data Memory Registers 00 to 39 (LCDRAM00 to LCDRAM39) are used to set data to be displayed on the LCD panel.

Register Configuration

bit	31 24	23 16	15 8	7 0
Field	LCDRAM03	LCDRAM02	LCDRAM01	LCDRAM00
Attribute	R/W	R/W	R/W	R/W
Initial Value	0x00	0x00	0x00	0x00

bit	31 24	23 16	15 8	7 0
Field	LCDRAM07	LCDRAM06	LCDRAM05	LCDRAM04
Attribute	R/W	R/W	R/W	R/W
Initial Value	0x00	0x00	0x00	0x00

bit	31 24	23 16	15 8	7 0
Field	LCDRAM11	LCDRAM10	LCDRAM09	LCDRAM08
Attribute	R/W	R/W	R/W	R/W
Initial Value	0x00	0x00	0x00	0x00

bit	31 24	23 16	15 8	7 0
Field	LCDRAM15	LCDRAM14	LCDRAM13	LCDRAM12
Attribute	R/W	R/W	R/W	R/W
Initial Value	0x00	0x00	0x00	0x00

bit	31 24	23 16	15 8	7 0
Field	LCDRAM19	LCDRAM18	LCDRAM17	LCDRAM16
Attribute	R/W	R/W	R/W	R/W
Initial Value	0x00	0x00	0x00	0x00

bit	31 24	23 16	15 8	7 0
Field	LCDRAM23	LCDRAM22	LCDRAM21	LCDRAM20
Attribute	R/W	R/W	R/W	R/W
Initial Value	0x00	0x00	0x00	0x00

bit	31 24	23 16	15 8	7 0
Field	LCDRAM27	LCDRAM26	LCDRAM25	LCDRAM24
Attribute	R/W	R/W	R/W	R/W
Initial Value	0x00	0x00	0x00	0x00

bit	31 24	23 16	15 8	7 0
Field	LCDRAM31	LCDRAM30	LCDRAM29	LCDRAM28
Attribute	R/W	R/W	R/W	R/W
Initial Value	0x00	0x00	0x00	0x00

bit	31 24	23 16	15 8	7 0
Field	LCDRAM35	LCDRAM34	LCDRAM33	LCDRAM32
Attribute	R/W	R/W	R/W	R/W
Initial Value	0x00	0x00	0x00	0x00

bit	31 24	23 16	15 8	7 0
Field	LCDRAM39	LCDRAM38	LCDRAM37	LCDRAM36
Attribute	R/W	R/W	R/W	R/W
Initial Value	0x00	0x00	0x00	0x00

6. Notes on Using LCD Controller

This section provides notes on using the LCD controller.

- When you use COM/SEG output pins as GPIO, set dual purpose COM/SEG port control bits to "0" where they correspond to LCDC COM Output Enable Register (LCDC_COMEN) and LCDC SEG Output Enable Register 1/2(LCDC_SEG1/2), and set the port input control bits (PICTL) of LCDC Control Register 3 (LCDCC3) to "1".
- If LCDC clock is stopped while LCD is displaying, the AC waveform generator also stops to cause applying DC voltage to the liquid crystal elements. To avoid this situation, stop the LCD display in advance.
  See chapters "Clocks" or "Low Power Consumption Mode" in "PERIPHERAL MANUAL" for the conditions to stop sub-clock or PCLK.
- The timing of operation to output LCDRAM data to LCD is different from the timing of access from CPU to LCDRAM. Flicker in screen may be found if write interval of LCDRAM is shorter than LCD cycle setup because the frame display patterns are different from each other.

APPENDIXES

This chapter shows the register map and list of notes.

A. Product Type

B. Register Map (TYPE1-M0+)

C. Register Map (TYPE2-M0+)

D. Register Map (TYPE3-M0+)

E. List of Notes

CODE: 9AFAPPENDIXES-E03.0

A. Product Type

This section describes the product TYPE.

1. Product TYPE List

CODE: xxxx

1. Product TYPE List

In this manual, the products are classified into the following groups and are described as follows.

For the descriptions such as "TYPE1-M0+","TYPE2-M0+" and “TYPE3-M0+”, see the relevant items of the target FM0+ product in the lists below.

Table 1-1 FM0+ family TYPE1-M0+ Product list

TYPE	Flash memory size	
	56 Kbytes	**88 Kbytes**
TYPE1-M0+	S6E1A11B S6E1A11C	S6E1A12B S6E1A12C

Table 1-2 FM0+ family TYPE2-M0+ Product list

TYPE	Flash memory size	
	304K bytes	**560K bytes**
TYPE2-M0+	S6E1B84E	S6E1B86E
	S6E1B84F	S6E1B86F
	S6E1B84G	S6E1B86G
	S6E1B34E	S6E1B36E
	S6E1B34F	S6E1B36F
	S6E1B34G	S6E1B36G

Table 1-3 FM0+ family TYPE3 Product list

TYPE	Flash memory size	
	64K bytes	**128K bytes**
TYPE3-M0+	S6E1C31B	S6E1C32B
	S6E1C31C	S6E1C32C
	S6E1C31D	S6E1C32D
	S6E1C11B	S6E1C12B
	S6E1C11C	S6E1C12C
	S6E1C11D	S6E1C12D

B. Register Map (TYPE1-M0+)

This chapter shows the register map.

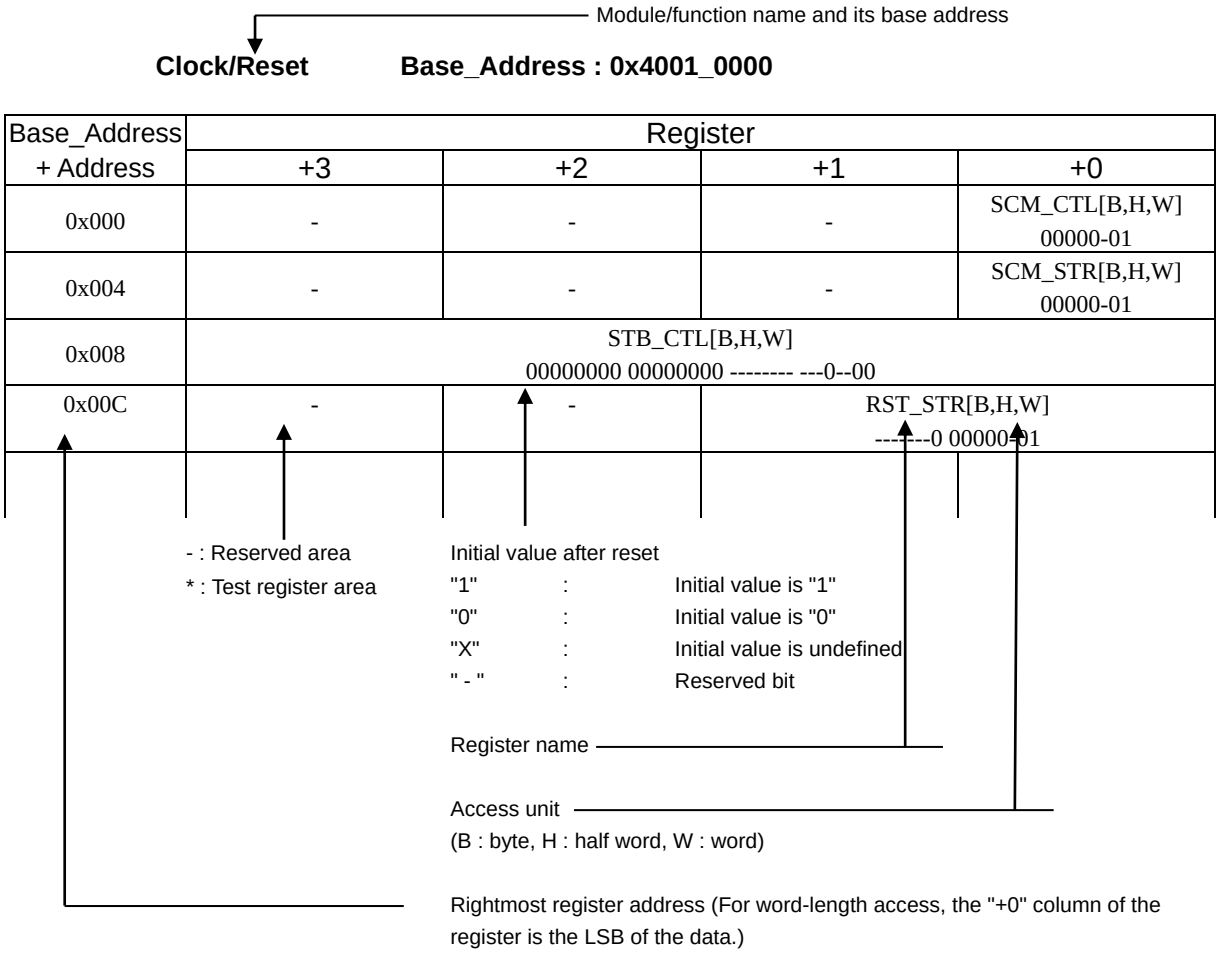
1. Register Map

CODE: 9AFREGMAP-E01.0

1. Register Map

Register map is shown on the table every module/function.

[How to Read the Each Table]



Notes:

- The register table is represented in the little-endian.
- When performing a data access, the addresses should be as below according to the access size.
  - Word access : Address should be multiples of 4 (least significant 2 bits should be "0x00")
  - Half word access : Address should be multiples of 2 (least significant bit should be "0x0")
  - Byte access : -
- Do not access the test register area.
- Do not access the area that is not written in the register table.
- When the register is accessed by larger unit than register size, for the reserved area to access at the same time, the read value is undefined, and writing is invalid.

1.1 Flash I/F

Flash I/F Base_Address : 0x4000_0000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	-
0x004	FRWTR[B,H,W]			
0x008	FSTR[B,H,W]			
0x00C				
0x010	FSYNDN[B,H,W]			
0x014 - 0x01C	-	-	-	-
0x020	FICR[B,H,W]			
0x024	FISR[B,H,W]			
0x028	FICLR[B,H,W]			
0x02C - 0x0FC	-	-	-	-
0x100	CRTRMM[B,H,W]			
0x104 - 0x1FC	-	-	-	-

Note:

- *For details of Flash I/F registers, refer to "FLASH PROGRAMMING MANUAL" of the product used.*

1.2 Unique ID

Unique ID Base_Address : 0x4000_0200

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	UIDR0[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXX----			
0x004	UIDR1[W]			
	-------- -------- ---XXXXX XXXXXXXX			
0x008 – 0xDFC	-	-	-	-

1.3 Clock/Reset

Clock/Reset Base_Address : 0x4001_0000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	SCM_CTL[W]
				00000-01
0x004	-	-	-	SCM_STR[W]
				00000-01
0x008	STB_CTL[W]			
	00000000 00000000 -------- ---0-000			
0x00C	-	-	RST_STR[W]	
			-------0 0000--01	
0x010	-	-	-	BSC_PSR[W]
				-----000
0x014	-	-	-	APBC0_PSR[W]
				------00
0x018	-	-	-	APBC1_PSR[W]
				1--0--00
0x01C	-	-	-	-
0x020	-	-	-	SWC_PSR[W]
				X-----00
0x024 - 0x02C	-	-	-	-
0x030	-	-	-	CSW_TMR[W]
				00000000
0x034	-	-	-	PSW_TMR[W]
				---0-000
0x038	-	-	-	PLL_CTL1[W]
				00000000
0x03C	-	-	-	PLL_CTL2[W]
				--000000
0x040	-	-	CSV_CTL[W]	
			-111--00 ------11	
0x044	-	-	-	CSV_STR[W]
				------00
0x048	-	-	FCSWH_CTL[W]	
			11111111 11111111	
0x04C	-	-	FCSWL_CTL[W]	
			00000000 00000000	
0x050	-	-	FCSWD_STR[W]	
			00000000 00000000	
0x054	-	-	-	DBWDT_CTL[W]
				0-0-----
0x058	-	-	-	*

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x05C	-	-	-	-
0x060	-	-	-	INT_ENR[W]
				--0--000
0x064	-	-	-	INT_STR[W]
				--0--000
0x068	-	-	-	INT_CLR[W]
				--0--000
0x06C - 0xFFC	-	-	-	-

1.4 HW WDT

HW WDT Base_Address : 0x4001_1000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	WDG_LDR[W]			
	00000000 00000000 11111111 11111111			
0x004	WDG_VLR[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x008	-	-	-	WDG_CTL[W]
				------11
0x00C	-	-	-	WDG_ICL[W]
				XXXXXXXX
0x010	-	-	-	WDG_RIS[W]
				-------0
0x014 - 0xBFC	-	-	-	-
0xC00	WDG_LCK[W]			
	00000000 00000000 00000000 00000001			
0xC04 - 0xFFC	-	-	-	-

1.5 SW WDT

SW WDT Base_Address : 0x4001_2000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	WdogLoad[W]			
	11111111 11111111 11111111 11111111			
0x004	WdogValue[W]			
	11111111 11111111 11111111 11111111			
0x008	-	-	-	WdogControl[W]
				---00000
0x00C	WdogIntClr[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x010	-	-	-	WdogRIS[W]
				-------0
0x014	*			
0x018	-	-	-	WdogSPMC[W]
				-------0
0x01C - 0xBFC	-	-	-	-
0xC00	WdogLock[W]			
	00000000 00000000 00000000 00000000			
0xC04 - 0xDFC	-	-	-	-
0xF00	*			
0xF08 - 0xFDF	-	-	-	-
0xFE0 - 0xFFC	*			

1.6 Dual Timer

Dual Timer Base_Address : 0x4001_5000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	Timer1Load[W]			
	00000000 00000000 00000000 00000000			
0x004	Timer1Value[W]			
	11111111 11111111 11111111 11111111			
0x008	Timer1Control[W]			
	-------- -------- -------- 00100000			
0x00C	Timer1IntClr[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x010	Timer1RIS[W]			
	-------- -------- -------- -------0			
0x014	Timer1MIS[W]			
	-------- -------- -------- -------0			
0x018	Timer1BGLoad[W]			
	00000000 00000000 00000000 00000000			
0x020	Timer2Load[W]			
	00000000 00000000 00000000 00000000			
0x024	Timer2Value[W]			
	11111111 11111111 11111111 11111111			
0x028	Timer2Control[W]			
	-------- -------- -------- 00100000			
0x02C	Timer2IntClr[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x030	Timer2RIS[W]			
	-------- -------- -------- -------0			
0x034	Timer2MIS[W]			
	-------- -------- -------- -------0			
0x038	Timer2BGLoad[W]			
	00000000 00000000 00000000 00000000			
0x040 - 0xFFC	-	-	-	-

1.7 MFT

MFT unit0 Base_Address : 0x4002_0000

MFT unit1 Base_Address : 0x4002_1000

MFT unit2 Base_Address : 0x4002_2000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x100	OCCP0[H,W]		-	-
	00000000 00000000			
0x104	OCCP1[H,W]		-	-
	00000000 00000000			
0x108	OCCP2[H,W]		-	-
	00000000 00000000			
0x10C	OCCP3[H,W]		-	-
	00000000 00000000			
0x110	OCCP4[H,W]		-	-
	00000000 00000000			
0x114	OCCP5[H,W]		-	-
	00000000 00000000			
0x118	-	OCSD10[B,H,W]	OCSB10[B,H,W]	OCSA10[B,H,W]
		00000000	00000000	00000000
0x11C	-	OCSD32[B,H,W]	OCSB32[B,H,W]	OCSA32[B,H,W]
		00000000	00000000	00000000
0x120	-	OCSD54[B,H,W]	OCSB54[B,H,W]	OCSA54[B,H,W]
		00000000	00000000	00000000
0x124	-	-	OCSC[B,H,W]	-
			--000000	
0x128	-	-	OCSE0[H,W]	
			00000000 00000000	
0x12C	OCSE1[H,W]			
	00000000 00000000 00000000 00000000			
0x130	-	-	OCSE2[H,W]	
			00000000 00000000	
0x134	OCSE3[H,W]			
	00000000 00000000 00000000 00000000			
0x138	-	-	OCSE4[H,W]	
			00000000 00000000	
0x13C	OCSE5[H,W]			
	00000000 00000000 00000000 00000000			
0x140	TCCP0[H,W]		-	-
	11111111 11111111			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x144	TCDT0[H,W]		-	-
	00000000 00000000			
0x148	TCSC0[B,H,W]		TCSA0[B,H,W]	
	00000000 00000000		000---00 01000000	
0x14C	TCCP1[H,W]		-	-
	11111111 11111111			
0x150	TCDT1[H,W]			
	00000000 00000000			
0x154	TCSC1[B,H,W]		TCSA1[B,H,W]	
	00000000 00000000		000---00 01000000	
0x158	TCCP2[H,W]		-	-
	11111111 11111111			
0x15C	TCDT2[H,W]		-	-
	00000000 00000000			
0x160	TCSC2[B,H,W]		TCSA2[B,H,W]	
	00000000 00000000		000---00 01000000	
0x164	TCAL[B,H,W] (only in unit 0)			
	00000000 00000000 11111111 11111111			
0x168	-	OCFS54[B,H,W]	OCFS32[B,H,W]	OCFS10[B,H,W]
		00000000	00000000	00000000
0x16C	-	-	ICFS32[B,H,W]	ICFS10[B,H,W]
			00000000	00000000
0x170	-	ACFS54[B,H,W]	ACFS32[B,H,W]	ACFS10[B,H,W]
		00000000	00000000	00000000
0x174	ICCP0[H,W]		-	-
	00000000 00000000			
0x178	ICCP1[H,W]		-	-
	00000000 00000000			
0x17C	ICCP2[H,W]		-	-
	00000000 00000000			
0x180	ICCP3[H,W]		-	-
	00000000 00000000			
0x184	-	-	ICSB10[B,H,W]	ICSA10[B,H,W]
			------00	00000000
0x188	-	-	ICSB32[B,H,W]	ICSA32[B,H,W]
			------00	00000000
0x18C	WFTF10[H,W]		-	-
	00000000 00000000			
0x190	WFTB10[H,W]		WFTA10[H,W]	
	00000000 00000000		00000000 00000000	
0x194	WFTF32[H,W]		-	-
	00000000 00000000			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x198	WFTB32[H,W]		WFTA32[H,W]	
	00000000 00000000		00000000 00000000	
0x19C	WFTF54[H,W]		-	-
	00000000 00000000			
0x1A0	WFTB54[H,W]		WFTA54[H,W]	
	00000000 00000000		00000000 00000000	
0x1A4	-	-	WFSA10[H,W]	
			---00000 000000	
0x1A8	-	-	WFSA32[H,W]	
			---00000 000000	
0x1AC	-	-	WFSA54[H,W]	
			---00000 000000	
0x1B0	-	-	WFIR[H,W]	
			00000000 00000000	
0x1B4	-	-	NZCL[H,W]	
			-000--00 ---00000	
0x1B8	ACMP0		-	-
	00000000 00000000			
0x1BC	ACMP1		-	-
	00000000 00000000			
0x1C0	ACMP2		-	-
	00000000 00000000			
0x1C4	ACMP3		-	-
	00000000 00000000			
0x1C8	ACMP4		-	-
	00000000 00000000			
0x1CC	ACMP5		-	-
	00000000 00000000			
0x1D0	-	-	ACSA[B,H,W]	
			--000000 --000000	
0x1D4	-	-	ACSD0[B,H,W]	ACSC0[B,H,W]
			00000000	00000000
0x1D8	-	-	ACSD1[B,H,W]	ACSC1[B,H,W]
			00000000	00000000
0x1DC	-	-	ACSD2[B,H,W]	ACSC2[B,H,W]
			00000000	00000000
0x1E0	-	-	ACSD3[B,H,W]	ACSC3[B,H,W]
			00000000	00000000
0x1E4	-	-	ACSD4[B,H,W]	ACSC4[B,H,W]
			00000000	00000000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x1E8	-	-	ACSD5[B,H,W]	ACSC5[B,H,W]
			00000000	00000000
0x1EC - 0xFFC	-	-	-	-

1.8 PPG

PPG Base_Address : 0x4002_4000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	TTCR0[B,H,W] 11110000	-
0x004	-	-	-	*
0x008	-	-	COMP0[B,H,W] 00000000	-
0x00C	-	-	-	COMP2[B,H,W] 00000000
0x010	-	-	COMP4[B,H,W] 00000000	-
0x014	-	-	-	COMP6[B,H,W] 00000000
0x018 - 0x01C	-	-	-	-
0x020	-	-	TTCR1[B,H,W] 11110000	-
0x024	-	-	-	*
0x028	-	-	COMP1[B,H,W] 00000000	-
0x02C	-	-	-	COMP3[B,H,W] 00000000
0x030	-	-	COMP5[B,H,W] 00000000	-
0x034	-	-	-	COMP7[B,H,W] 00000000
0x038 - 0x03C	-	-	-	-
0x040	-	-	TTCR2[B,H,W] 11110000	-
0x044	-	-	-	*
0x048	-	-	COMP8[B,H,W] 00000000	-
0x04C	-	-	-	COMP10[B,H,W] 00000000
0x050	-	-	COMP12[B,H,W] 00000000	-
0x054	-	-	-	COMP14[B,H,W] 00000000
0x058 - 0x0FC	-	-	-	-

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x100	-	-	TRG0[B,H,W]	
			00000000 00000000	
0x104	-	-	REVC0[B,H,W]	
			00000000 00000000	
0x108 - 0x13C	-	-	-	-
0x140	-	-	TRG1[B,H,W]	
			-------- 00000000	
0x144	-	-	REVC1[B,H,W]	
			-------- 00000000	
0x148 - 0x1FC	-	-	-	-
0x200	-	-	PPGC0[B,H,W]	PPGC1[B,H,W]
			00000000	00000000
0x204	-	-	PPGC2[B,H,W]	PPGC3[B,H,W]
			00000000	00000000
0x208	-	-	PRLH0[B,H,W]	PRLL0[B,H,W]
			XXXXXXXX	XXXXXXXX
0x20C	-	-	PRLH1[B,H,W]	PRLL1[B,H,W]
			XXXXXXXX	XXXXXXXX
0x210	-	-	PRLH2[B,H,W]	PRLL2[B,H,W]
			XXXXXXXX	XXXXXXXX
0x214	-	-	PRLH3[B,H,W]	PRLL3[B,H,W]
			XXXXXXXX	XXXXXXXX
0x218	-	-	-	GATEC0[B,H,W]
				--00---00
0x21C - 0x23C	-	-	-	-
0x240	-	-	PPGC4[B,H,W]	PPGC5[B,H,W]
			00000000	00000000
0x244	-	-	PPGC6[B,H,W]	PPGC7[B,H,W]
			00000000	00000000
0x248	-	-	PRLH4[B,H,W]	PRLL4[B.H.W]
			XXXXXXXX	XXXXXXXX
0x24C	-	-	PRLH5[B,H,W]	PRLL5[B,H,W]
			XXXXXXXX	XXXXXXXX
0x250	-	-	PRLH6[B,H,W]	PRLL6[B,H,W]
			XXXXXXXX	XXXXXXXX
0x254	-	-	PRLH7[B,H,W]	PRLL7[B,H,W]
			XXXXXXXX	XXXXXXXX
0x258	-	-	-	GATEC4[B,H,W]
				--00--00
0x25C - 0x27C	-	-	-	-
0x280	-	-	PPGC8[B,H,W]	PPGC9[B,H,W]
			00000000	00000000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x284	-	-	PPGC10[B,H,W]	PPGC11[B,H,W]
			00000000	00000000
0x288	-	-	PRLH8[B,H,W]	PRLL8[B,H,W]
			XXXXXXXX	XXXXXXXX
0x28C	-	-	PRLH9[B,H,W]	PRLL9[B,H,W]
			XXXXXXXX	XXXXXXXX
0x290	-	-	PRLH10[B,H,W]	PRLL10[B,H,W]
			XXXXXXXX	XXXXXXXX
0x294	-	-	PRLH11[B,H,W]	PRLL11[B,H,W]
			XXXXXXXX	XXXXXXXX
0x298	-	-	-	GATEC8[B,H,W]
				--00--00
0x29C - 0x2BC	-	-	-	-
0x2C0	-	-	PPGC12[B,H,W]	PPGC13[B,H,W]
			00000000	00000000
0x2C4	-	-	PPGC14[B,H,W]	PPGC15[B,H,W]
			00000000	00000000
0x2C8	-	-	PRLH12[B,H,W]	PRLL12[B,H,W]
			XXXXXXXX	XXXXXXXX
0x2CC	-	-	PRLH13[B,H,W]	PRLL13[B,H,W]
			XXXXXXXX	XXXXXXXX
0x2D0	-	-	PRLH14[B,H,W]	PRLL14[B,H,W]
			XXXXXXXX	XXXXXXXX
0x2D4	-	-	PRLH15[B,H,W]	PRLL15[B,H,W]
			XXXXXXXX	XXXXXXXX
0x2D8	-	-	-	GATEC12[B,H,W]
				--00--00
0x2DC - 0x2FC	-	-	-	-
0x300	-	-	PPGC16[B,H,W]	PPGC17[B,H,W]
			00000000	00000000
0x304	-	-	PPGC18[B,H,W]	PPGC19[B,H,W]
			00000000	00000000
0x308	-	-	PRLH16[B,H,W]	PRLL16[B,H,W]
			XXXXXXXX	XXXXXXXX
0x30C	-	-	PRLH17[B,H,W]	PRLL17[B,H,W]
			XXXXXXXX	XXXXXXXX
0x310	-	-	PRLH18[B,H,W]	PRLL18[B,H,W]
			XXXXXXXX	XXXXXXXX
0x314	-	-	PRLH19[B,H,W]	PRLL19[B,H,W]
			XXXXXXXX	XXXXXXXX
0x318	-	-	-	GATEC16[B,H,W]
				--00---00

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x31C - 0x33C	-	-	-	-
0x340			PPGC20[B,H,W]	PPGC21[B,H,W]
			00000000	00000000
0x344	-	-	PPGC22[B,H,W]	PPGC23[B,H,W]
			00000000	00000000
0x348	-	-	PRLH20[B,H,W]	PRLL20[B,H,W]
			XXXXXXXX	XXXXXXXX
0x34C	-	-	PRLH21[B,H,W]	PRLL21[B,H,W]
			XXXXXXXX	XXXXXXXX
0x350	-	-	PRLH22[B,H,W]	PRLL22[B,H,W]
			XXXXXXXX	XXXXXXXX
0x354	-	-	PRLH23[B,H,W]	PRLL23[B,H,W]
			XXXXXXXX	XXXXXXXX
0x358	-	-	-	GATEC20[B,H,W]
				--00--00
0x35C - 0x37C	-	-	-	-
0x380	-	-	-	IGBTC[B,H,W]
				00000000
0x384 - 0xFFC	-	-	-	-

1.9 Base Timer

Base Timer ch.0 Base Address : 0x4002_5000

Base Timer ch.1 Base Address : 0x4002_5040

Base Timer ch.2 Base Address : 0x4002_5080

Base Timer ch.3 Base Address : 0x4002_50C0

Base Timer ch.4 Base Address : 0x4002_5200

Base Timer ch.5 Base Address : 0x4002_5240

Base Timer ch.6 Base Address : 0x4002_5280

Base Timer ch.7 Base Address : 0x4002_52C0

Base Timer ch.8 Base Address : 0x4002_5400

Base Timer ch.9 Base Address : 0x4002_5440

Base Timer ch.10 Base Address : 0x4002_5480

Base Timer ch.11 Base Address : 0x4002_54C0

Base Timer ch.12 Base Address : 0x4002_5600

Base Timer ch.13 Base Address : 0x4002_5640

Base Timer ch.14 Base Address : 0x4002_5680

Base Timer ch.15 Base Address : 0x4002_56C0

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	PCSR/PRLL[H,W]	
			XXXXXXXX XXXXXXXX	
0x004	-	-	PDUT/PRLH/DTBF[H,W]	
			XXXXXXXX XXXXXXXX	
0x008	-	-	TMR[H,W]	
			00000000 00000000	
0x00C	-	-	TMCR[B,H,W]	
			-0000000 00000000	
0x010	-	-	TMCR2[B,H,W]	STC[B,H,W]
			-------0	0000-000
0x014 - 0x03C	-	-	-	-

1.10 IO Selector for Base Timer

IO Selector for ch.0-ch.3 (Base Timer) **Base Address : 0x4002_5100**

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	BTSEL0123[B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

IO Selector for ch.4-ch.7 (Base Timer) **Base Address : 0x4002_5300**

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	BTSEL4567[B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

IO Selector for ch.8-ch.11 (Base Timer) **Base Address : 0x4002_5500**

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	BTSEL89AB[B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

IO Selector for ch.12-ch.15 (Base Timer) **Base Address : 0x4002_5700**

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	BTSELCDEF[B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

Software-based Simultaneous Startup (Base Timer) **Base Address : 0x4002_5F00**

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000 - 0x0FB	-	-	-	-
0x0FC	-	-	BTSSSR[B,H,W] XXXXXXXX XXXXXXXX	

1.11 QPRC

QPRC ch.0 **Base Address : 0x4002_6000**

QPRC ch.1 **Base Address : 0x4002_6040**

QPRC ch.2 **Base Address : 0x4002_6080**

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x0000	-	-	QPCR[H,W]	
			00000000 00000000	
0x0004	-	-	QRCR[H,W]	
			00000000 00000000	
0x0008	-	-	QPCCR[H,W]	
			00000000 00000000	
0x000C	-	-	QPRCR[H,W]	
			00000000 00000000	
0x0010	-	-	QMPR[H,W]	
			11111111 11111111	
0x0014	-	-	QICRH[B,H,W]	QICRL[B,H,W]
			--000000	00000000
0x0018	-	-	QCRH[B,H,W]	QCRL[B,H,W]
			00000000	00000000
0x001C	-	-	QECR[B,H,W]	
			-------- -----000	
0x0020 - 0x0038	-	-	-	-
0x003C	QPCRR[B,H,W]		QRCRR[B,H,W]	
	00000000 00000000		00000000 00000000	

1.12 QPRC NF

QPRC ch.0 NF **Base Address : 0x4002_6100**

QPRC ch.1 NF **Base Address : 0x4002_6110**

QPRC ch.2 NF **Base Address : 0x4002_6120**

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x0000	NFCTLA[B,H,W]			
	-------- -------- -------- --00-000			
0x0004	NFCTLB[B,H,W]			
	-------- -------- -------- --00-000			
0x0008	NFCTLC[B,H,W]			
	-------- -------- -------- --00-000			
0x000C	-	-	-	-

1.13 A/DC

12-bit A/DC unit0 Base_Address : 0x4002_7000

12-bit A/DC unit1 Base_Address : 0x4002_7100

12-bit A/DC unit2 Base_Address : 0x4002_7200

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	ADCR[B,H,W]	ADSR[B,H,W]
			000-0000	00---000
0x004	-	-	-	*
0x008	-	-	SCCR[B,H,W]	SFNS[B,H,W]
			1000-000	----0000
0x00C	SCFD[B,H,W]			
	XXXXXXXX XXXX---- ---X--XX ---XXXXX			
0x010	-	-	SCIS3[B,H,W]	SCIS2[B,H,W]
			00000000	00000000
0x014	-	-	SCIS1[B,H,W]	SCIS0[B,H,W]
			00000000	00000000
0x018	-	-	PCCR[B,H,W]	PFNS[B,H,W]
			1000-000	--XX--00
0x01C	PCFD[B,H,W]			
	XXXXXXXX XXXX---- ---X-XXX ---XXXXX			
0x020	-	-	-	PCIS[B,H,W]
				00000000
0x024	CMPD[B,H,W]		-	CMPCR[B,H,W]
	00000000 00------			00000000
0x028	-	-	ADSS3[B,H,W]	ADSS2[B,H,W]
			00000000	00000000
0x02C	-	-	ADSS1[B,H,W]	ADSS0[B,H,W]
			00000000	00000000
0x030	-	-	ADST0[B,H,W]	ADST1[B,H,W]
			00010000	00010000
0x034	-	-	-	ADCT[B,H,W]
				00000111
0x038	-	-	SCTSL[B,H,W]	PRTSL[B,H,W]
			----0000	----0000
0x03C	-	-	ADCEN[B,H,W]	
			11111111 ------00	
0x040	*			
0x044	WCMRCIF[B,H,W]			
	-------- -------- -------- -------0			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x048	WCMRCOT[B,H,W]			
	-------- -------- -------- -------0			
0x04C	-	-	WCMPSR[B,H,W]	WCMPCR[B,H,W]
			--000000	001000--
0x050	WCMPDH[B,H,W]		WCMPDL[B,H,W]	
	00000000 00------		00000000 00------	
0x054 - 0x0FC	-	-	-	-

1.14 D/AC

10-bit D/AC Base_Address : 0x4002_8000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x00	-	DACR0[B,H,W]	DADR0[B,H,W]	
		-------0	------XX XXXXXXXX	
0x04	-	DACR1[B,H,W]	DADR1[B,H,W]	
		-------0	------XX XXXXXXXX	
0x08 - 0xFC	-	-	-	-

1.15 CR Trim

CR Trim Base_Address : 0x4002_E000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	MCR_PSR[B,H,W]
				------001
0x004	-	-	MCR_FTRM[B,H,W]	
			------01 11101111	
0x008	-	-	-	MCR_TTRM[B,H,W]
				---10000
0x00C	MCR_RLR[B,H,W]			
	00000000 00000000 00000000 00000001			
0x010 - 0x0FC	-	-	-	-

1.16 EXTI

EXTI Base_Address : 0x4003_0000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	ENIR[B,H,W]			
	00000000 00000000 00000000 00000000			
0x004	EIRR[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x008	EICL[B,H,W]			
	11111111 11111111 11111111 11111111			
0x00C	ELVR[B,H,W]			
	00000000 00000000 00000000 00000000			
0x010	ELVR1[B,H,W]			
	00000000 00000000 00000000 00000000			
0x014	-	-	NMIRR[B,H,W]	
			-------- -------0	
0x018	-	-	NMICL[B,H,W]	
			-------- -------1	
0x01C - 0x0FC	-	-	-	-

1.17 INT-Req. READ

INT-Req. READ Base_Address : 0x4003_1000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	DRQSEL[B,H,W]			
	00000000 00000000 00000000 00000000			
0x004	*			
0x008 - 0x00B	-	-	-	-
0x00C	-	-	-	IRQCMODE[B,H,W]
				-------0
0x010	EXC02MON[B,H,W]			
	-------- -------- -------- ------00			
0x014	IRQ00MON[B,H,W]			
	-------- -------- -------- -------0			
0x018	IRQ01MON[B,H,W]			
	-------- -------- -------- -------0			
0x01C	IRQ02MON[B,H,W]			
	-------- -------- -------- -------0			
0x020	IRQ03MON[B,H,W]			
	-------- -------- ----0000 00000000			
0x024	IRQ04MON[B,H,W]			
	-------- -------- -------- 00000000			
0x028	IRQ05MON[B,H,W]			
	-------- 00000000 00000000 00000000			
0x02C	IRQ06MON[B,H,W]			
	-------- ----0000 00000000 00000000			
0x030	IRQ07MON[B,H,W]			
	-------- -------- -------- ------00			
0x034	IRQ08MON[B,H,W]			
	-------- -------- -------- ----0000			
0x038	IRQ09MON[B,H,W]			
	-------- -------- -------- ------00			
0x03C	IRQ10MON[B,H,W]			
	-------- -------- -------- ----0000			
0x040	IRQ11MON[B,H,W]			
	-------- -------- -------- ------00			
0x044	IRQ12MON[B,H,W]			
	-------- -------- -------- ----0000			
0x048	IRQ13MON[B,H,W]			
	-------- -------- -------- ------00			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x04C	IRQ14MON[B,H,W]			
	-------- -------- -------- ----0000			
0x050	IRQ15MON[B,H,W]			
	-------- -------- -------- ------00			
0x054	IRQ16MON[B,H,W]			
	-------- -------- -------- ----0000			
0x058	IRQ17MON[B,H,W]			
	-------- -------- -------- ------00			
0x05C	IRQ18MON[B,H,W]			
	-------- -------- -------- ----0000			
0x060	IRQ19MON[B,H,W]			
	-------- -------- -------- ---0--00			
0x064	IRQ20MON[B,H,W]			
	-------- -------- -------- ---00000			
0x068	IRQ21MON[B,H,W]			
	-------- -------- -------- ---0--00			
0x06C	IRQ22MON[B,H,W]			
	-------- -------- -------- ---00000			
0x070	IRQ23MON[B,H,W]			
	-------- -------- -------0 00000000			
0x074	IRQ24MON[B,H,W]			
	-------- -------- -------- --00-000			
0x078	IRQ25MON[B,H,W]			
	-------- -------- -------- ---00000			
0x07C	IRQ26MON[B,H,W]			
	-------- -------- -------- ---00000			
0x080	IRQ27MON[B,H,W]			
	-------- -------- -------- --000000			
0x084	IRQ28MON[B,H,W]			
	-------- ------00 00000000 00000000			
0x088	IRQ29MON[B,H,W]			
	-------- -------- ----0000 00000000			
0x08C	IRQ30MON[B,H,W]			
	-------- ------00 00000000 00000000			
0x090	IRQ31MON[B,H,W]			
	----0--- -------- 00000000 00000000			
0x094 - 0x20C	-	-	-	-
0x210	RCINTSEL0[B,H,W] 00000000 00000000 00000000 00000000			
0x214	RCINTSEL1[B,H,W] 00000000 00000000 00000000 00000000			
0x218 - 0xFFC	-	-	-	-

1.18 GPIO

GPIO Base_Address : 0x4003_3000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	PFR0[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 1010			
0x004	PFR1[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x008	PFR2[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x00C	PFR3[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x010	PFR4[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x014	PFR5[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x018	PFR6[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x01C	PFR7[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x020	PFR8[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x024	PFR9[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x028	PFRA[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x02C	PFRB[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x030	PFRC[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x034	PFRD[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x038	PFRE[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x03C	PFRF[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x040 - 0x0FC	-	-	-	-
0x100	PCR0[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 1010			
0x104	PCR1[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x108	PCR2[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x10C	PCR3[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x110	PCR4[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x114	PCR5[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x118	PCR6[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x11C	PCR7[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x120	-	-	-	-
0x124	PCR9[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x128	PCRA[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x12C	PCRB[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x130	PCRC[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x134	PCRD[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x138	PCRE[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x13C	PCRF[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x140 - 0x1FC	-	-	-	-
0x200	DDR0[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x204	DDR1[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x208	DDR2[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x20C	DDR3[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x210	DDR4[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x214	DDR5[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x218	DDR6[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x21C	DDR7[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x220	DDR8[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x224	DDR9[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x228	DDRA[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x22C	DDRB[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x230	DDRC[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x234	DDRD[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x238	DDRE[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x23C	DDRF[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x240 - 0x2FC	-	-	-	-
0x300	PDIR0[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x304	PDIR1[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x308	PDIR2[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x30C	PDIR3[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x310	PDIR4[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x314	PDIR5[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x318	PDIR6[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x31C	PDIR7[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x320	PDIR8[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x324	PDIR9[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x328	PDIRA[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x32C	PDIRB[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x330	PDIRC[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x334	PDIRD[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x338	PDIRE[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x33C	PDIRF[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x340 - 0x3FC	-	-	-	-
0x400	PDOR0[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x404	PDOR1[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x408	PDOR2[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x40C	PDOR3[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x410	PDOR4[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x414	PDOR5[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x418	PDOR6[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x41C	PDOR7[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x420	PDOR8[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x424	PDOR9[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x428	PDORA[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x42C	PDORB[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x430	PDORC[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x434	PDORD[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x438	PDORE[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x43C	PDORF[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x440 - 0x4FC	-	-	-	-
0x500	ADE[B,H,W]			
	1111 1111 1111 1111 1111 1111 1111 1111			
0x504 - 0x57C	-	-	-	-
0x580	SPSR[B,H,W]			
	---- ---- ---- ---- ---- ---- ---- 0101			
0x584 - 0x5FC	-	-	-	-
0x600	EPFR00[B,H,W]			
	---- ---- ---- ---1 ---- ---- 0000 -000			
0x604	EPFR01[B,H,W]			
	0000 0000 0000 0000 --00 0000 0000 0000			
0x608	EPFR02[B,H,W]			
	0000 0000 0000 0000 ---0 0000 0000 0000			
0x60C	EPFR03[B,H,W]			
	0000 0000 0000 0000 ---0 0000 0000 0000			
0x610	EPFR04[B,H,W]			
	--00 0000 --00 00-- --00 0000 -000 00--			
0x614	EPFR05[B,H,W]			
	--00 0000 --00 00-- --00 0000 --00 00--			
0x618	EPFR06[B,H,W]			
	0000 0000 0000 0000 0000 0000 0000 0000			
0x61C	EPFR07[B,H,W]			
	---- 0000 0000 0000 0000 0000 0000 ----			
0x620	EPFR08[B,H,W]			
	---- 0000 0000 0000 0000 0000 0000 0000			
0x624	EPFR09[B,H,W]			
	0000 0000 0000 0000 0000 0000 0000 0000			
0x628 - 0x62C	-	-	-	-
0x630	EPFR12[B,H,W]			
	--00 0000 --00 00-- --00 0000 --00 00--			
0x634	EPFR13[B,H,W]			
	--00 0000 --00 00-- --00 0000 --00 00--			
0x638	EPFR14[B,H,W]			
	---- ---- ---- ---- ---- ---- --00 0000			
0x63C	EPFR15[B,H,W]			
	0000 0000 0000 0000 0000 0000 0000 0000			
0x640	EPFR16[B,H,W]			
	---- 0000 0000 0000 0000 0000 0000 ----			
0x644	EPFR17[B,H,W]			
	---- 0000 0000 0000 0000 0000 0000 ----			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x648	EPFR18[B,H,W]			
	---- ---- ---- ---- ---- ---- ---- 0000			
0x64C - 0x650	-	-	-	-
0x654	EPFR21[B,H,W]			
	---- ---- ---- ---- ---- ---- ---- -000			
0x658	EPFR22[B,H,W]			
	---- ---- ---- ---- 0000 ---- 0000 ----			
0x65C - 0x6FC	-	-	-	-
0x700	PZR0[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x704	PZR1[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x708	PZR2[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x70C	PZR3[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x710	PZR4[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x714	PZR5[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x718	PZR6[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x71C	PZR7[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x720	PZR8[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x724	PZR9[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x728	PZRA[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x72C	PZRB[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x730	PZRC[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x734	PZRD[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x738	PZRE[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x73C	PZRF[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x740 - 0x7FC	-	-	-	-
0x800	*			
0x804	*			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x808 - 0x8FC	-	-	-	-
0x900	FPOER0[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x904	FPOER1[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x908	FPOER2[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x90C	FPOER3[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x910	FPOER4[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x914	FPOER5[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x918	FPOER6[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x91C	FPOER7[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x920	FPOER8[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x924	FPOER9[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x928	FPOERA[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x92C	FPOERB[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x930	FPOERC[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x934	FPOERD[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x938	FPOERE[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x93C	FPOERF[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x940 - 0xFFC	-	-	-	-

1.19 HDMI-CEC

HDMI-CEC/Remote Control Receiver ch.0 Base_Address : 0x4003_4000

HDMI-CEC/Remote Control Receiver ch.1 Base_Address : 0x4003_4100

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x00	-	-	-	TXCTRL[B,H,W]
				--0000-0
0x04	-	-	-	TXDATA[B,H,W]
				00000000
0x08	-	-	-	TXSTS[B,H,W]
				--00---0
0x0C	-	-	-	SFREE[B,H,W]
				----0000
0x10 - 0x3F	-	-	-	-
0x40	-	-	RCCR[B,H,W]	RCST[B,H,W]
			0---0000	00000000
0x44	-	-	RCSHW[B,H,W]	RCDAHW[B,H,W]
			00000000	00000000
0x48	-	-	RCDBHW[B,H,W]	-
			00000000	
0x4C	-	-	RCADR1[B,H,W]	RCADR2[B,H,W]
			---00000	---00000
0x50	-	-	RCDTHH[B,H,W]	RCDTHL[B,H,W]
			00000000	00000000
0x54	-	-	RCDTLH[B,H,W]	RCDTLL[B,H,W]
			00000000	00000000
0x58	-	-	RCCKD[H,W]	
			---00000 00000000	
0x5C	-	-	RCRC[B,H,W]	RCRHW[B,H,W]
			---0---0	00000000
0x60	-	-	RCLE[B,H,W]	-
			00000-00	
0x64	-	-	RCLELW[B,H,W]	RCLESW[B,H,W]
			00000000	00000000
0x68 - 0xFC	-	-	-	-

1.20 LVD

LVD Base_Address : 0x4003_5000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	LVD_CTL[B,H,W]	
			100000-- 000011--	
0x004	-	-	-	LVD_STR[B,H,W]
				0-------
0x008	-	-	-	LVD_CLR[B,H,W]
				1-------
0x00C	LVD_RLR[W]			
	00000000 00000000 00000000 00000001			
0x010	-	-	-	LVD_STR2
				01------
0x014 - 0x0FC	-	-	-	-

1.21 DS Mode

DS Mode Base_Address : 0x4003_5100

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	REG_CTL[B,H,W]
				-------0
0x004	-	-	-	RCK_CTL[B,H,W]
				------01
0x008 - 0x6FC	-	-	-	-
0x700	-	-	-	PMD_CTL[B,H,W]
				-------0
0x704	-	-	-	WRFSR[B,H,W]
				------00
0x708	-	-	WIFSR[B,H,W]	
			------00 00000000	
0x70C	-	-	WIER[B,H,W]	
			------00 00000-00	
0x710	-	-	-	WILVR[B,H,W]
				-----000
0x714	-	-	-	DSRAMR[B,H,W]
				------00
0x718 - 0x7FC	-	-	-	-
0x800	BUR04[B,H,W]	BUR03[B,H,W]	BUR02[B,H,W]	BUR01[B,H,W]
	00000000	00000000	00000000	00000000
0x804	BUR08[B,H,W]	BUR07[B,H,W]	BUR06[B,H,W]	BUR05[B,H,W]
	00000000	00000000	00000000	00000000
0x808	BUR012[B,H,W]	BUR11[B,H,W]	BUR10[B,H,W]	BUR09[B,H,W]
	00000000	00000000	00000000	00000000
0x80C	BUR16[B,H,W]	BUR15[B,H,W]	BUR14[B,H,W]	BUR13[B,H,W]
	00000000	00000000	00000000	00000000
0x810 - 0xEFC	-	-	-	-

1.22 MFS

MFS ch.0 Base_Address : 0x4003_8000

MFS ch.1 Base_Address : 0x4003_8100

MFS ch.2 Base_Address : 0x4003_8200

MFS ch.3 Base_Address : 0x4003_8300

MFS ch.4 Base_Address : 0x4003_8400

MFS ch.5 Base_Address : 0x4003_8500

MFS ch.6 Base_Address : 0x4003_8600

MFS ch.7 Base_Address : 0x4003_8700

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	SCR/IBCR[B,H,W]	SMR[B,H,W]
			0--00000	000-00-0
0x004	-	-	SSR[B,H,W]	ESCR/IBSR[B,H,W]
			0-000011	00000000
0x008	-	-	RDR/TDR[H,W]	
			00000000 00000000	
0x00C	-	-	BGR1[B,H,W]	BGR0[B,H,W]
			00000000	00000000
0x010	-	-	ISMK[B,H,W]	ISBA[B,H,W]
			--------	--------
0x014	-	-	FCR1[B,H,W]	FCR0[B,H,W]
			---00100	-0000000
0x018	-	-	FBYTE2[B,H,W]	FBYTE1[B,H,W]
			00000000	00000000
0x01C	-	-	SCSTR1/ EIBCR[B,H,W]	SCSTR0 [B,H,W]
			00000000	00000000
0x020	-	-	SCSTR3[B,H,W]	SCSTR2[B,H,W]
			00000000	00000000
0x024	-	-	SACSR[B,H,W]	
			--000--0 00-00000	
0x028	-	-	STMR[B,H,W]	
			00000000 00000000	
0x02C	-	-	STMCR[B,H,W]	
			00000000 00000000	

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x030	-	-	SCSCR[B,H,W]	
			00000000 00100000	
0x034	-	-	SCSFR1[B,H,W] 10000000	SCSFR0[B,H,W] 10000000
0x038	-	-	-	SCSFR2[B,H,W] 10000000
0x03C	-	-	TBYTE1[B,H,W]	TBYTE0[B,H,W]
			00000000	00000000
0x040	-	-	TBYTE3[B,H,W] 00000000	TBYTE2[B,H,W] 00000000
0x044 - 0x0FC	-	-	-	-

1.23 CRC

CRC Base_Address : 0x4003_9000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	CRCCR[B,H,W]
				-0000000
0x004	CRCINIT[B,H,W]			
	11111111 11111111 11111111 11111111			
0x008	CRCIN[B,H,W]			
	00000000 00000000 00000000 00000000			
0x00C	CRCR[B,H,W]			
	11111111 11111111 11111111 11111111			

1.24 Watch Counter

Watch Counter Base_Address : 0x4003_A000

Base_Address	Register			
+ Address	**+3**	**+2**	**+1**	**+0**
0x000	-	WCCR[B,H,W]	WCRL[B,H,W]	WCRD[B,H,W]
		00--0000	--000000	--000000
0x004 - 0x00C	-	-	-	-
0x010	-	-	CLK_SEL[B,H,W]	
			-----000 ------00	
0x014	-	-	-	CLK_EN[B,H,W]
				------00
0x018 - 0xFFC	-	-	-	-

1.25 RTC

RTC Base_Address : 0x4003_B000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	WTCR1[B,H,W]			
	00000000 00000000 ---00000 -00000-0			
0x004	WTCR2[B,H,W]			
	-------- -------- -----000 -------0			
0x008	WTBR[B,H,W]			
	-------- 00000000 00000000 00000000			
0x00C	WTDR[B,H,W]	WTHR[B,H,W]	WTMIR[B,H,W]	WTSR[B,H,W]
	--000000	--000000	-0000000	-0000000
0x010	-	WTYR[B,H,W]	WTMOR[B,H,W]	WTDW[B,H,W]
		00000000	---00000	-----000
0x014	ALDR[B,H,W]	ALHR[B,H,W]	ALMIR[B,H,W]	-
	--000000	--000000	-0000000	
0x018	-	ALYR[B,H,W]	ALMOR[B,H,W]	-
		00000000	---00000	
0x01C	WTTR[B,H,W]			
	-------- ------00 00000000 00000000			
0x020	-	-	WTCLKM[B,H,W]	WTCLKS[B,H,W]
			------00	-------0
0x024	-	WTCALEN[B,H,W]	WTCAL[B,H,W]	
		-------0	------00 00000000	
0x028	-	-	WTDIVEN[B,H,W]	WTDIV[B,H,W]
			------00	----0000
0x02C	-	-	-	WTCALPRD[B,H,W]
				--010011
0x030	-	-	-	WTCOSEL[B,H,W]
				-------0
0x034 - 0xFFC	-	-	-	-

1.26 Low-speed CR Prescaler

Low-speed CR Prescaler Base_Address : 0x4003_C000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	LCR_PRSLD[B,H,W]
				--000000
0x000 - 0x0FC	-	-	-	-

1.27 Peripheral Clock Gating

Peripheral Clock Gating Base_Address : 0x4003_C100

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	CKEN0[B,H,W]			
	---1---1 ----1111 11111111 11111111			
0x004	MRST0[B,H,W]			
	-------0 ----0000 00000000 00000000			
0x008 - 0x00C	-	-	-	-
0x010	CKEN1[B,H,W]			
	-------- ----1111 ----1111 ----1111			
0x014	MRST1[B,H,W]			
	-------- ----0000 ----0000 ----0000			
0x018 - 0x01C	-	-	-	-
0x020	CKEN2[B,H,W]			
	-------- -------- -------- --00----			
0x024	MRST2[B,H,W]			
	-------- -------- -------- --00----			
0x028 - 0x0FC	-	-	-	-

1.28 DMAC

DMAC Base_Address : 0x4006_0000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x0000	DMACR[B,H,W]			
	00-00000 -------- -------- --------			
0x0010	DMACA0[B,H,W]			
	00000000 0---0000 00000000 00000000			
0x0014	DMACB0[B,H,W]			
	--000000 00000000 00000000 -------0			
0x0018	DMACSA0[B,H,W]			
	00000000 00000000 00000000 00000000			
0x001C	DMACDA0[B,H,W]			
	00000000 00000000 00000000 00000000			
0x0020	DMACA1[B,H,W]			
	00000000 0---0000 00000000 00000000			
0x0024	DMACB1[B,H,W]			
	--000000 00000000 00000000 -------0			
0x0028	DMACSA1[B,H,W]			
	00000000 00000000 00000000 00000000			
0x002C	DMACDA1[B,H,W]			
	00000000 00000000 00000000 00000000			
0x0030	DMACA2[B,H,W]			
	00000000 0---0000 00000000 00000000			
0x0034	DMACB2[B,H,W]			
	--000000 00000000 00000000 -------0			
0x0038	DMACSA2[B,H,W]			
	00000000 00000000 00000000 00000000			
0x003C	DMACDA2[B,H,W]			
	00000000 00000000 00000000 00000000			
0x0040	DMACA3[B,H,W]			
	00000000 0---0000 00000000 00000000			
0x0044	DMACB3[B,H,W]			
	--000000 00000000 00000000 -------0			
0x0048	DMACSA3[B,H,W]			
	00000000 00000000 00000000 00000000			
0x004C	DMACDA3[B,H,W]			
	00000000 00000000 00000000 00000000			
0x0050	DMACA4[B,H,W]			
	00000000 0---0000 00000000 00000000			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x0054	DMACB4[B,H,W]			
	--000000 00000000 00000000 -------0			
0x0058	DMACSA4[B,H,W]			
	00000000 00000000 00000000 00000000			
0x005C	DMACDA4[B,H,W]			
	00000000 00000000 00000000 00000000			
0x0060	DMACA5[B,H,W]			
	00000000 00000000 00000000 00000000			
0x0064	DMACB5[B,H,W]			
	--000000 00000000 00000000 -------0			
0x0068	DMACSA5[B,H,W]			
	00000000 00000000 00000000 00000000			
0x006C	DMACDA5[B,H,W]			
	00000000 00000000 00000000 00000000			
0x0070	DMACA6[B,H,W]			
	00000000 0---0000 00000000 00000000			
0x0074	DMACB6[B,H,W]			
	--000000 00000000 00000000 -------0			
0x0078	DMACSA6[B,H,W]			
	00000000 00000000 00000000 00000000			
0x007C	DMACDA6[B,H,W]			
	00000000 00000000 00000000 00000000			
0x0080	DMACA7[B,H,W]			
	00000000 0---0000 00000000 00000000			
0x0084	DMACB7[B,H,W]			
	--000000 00000000 00000000 -------0			
0x0088	DMACSA7[B,H,W]			
	00000000 00000000 00000000 00000000			
0x008C	DMACDA7[B,H,W]			
	00000000 00000000 00000000 00000000			
0x0090 - 0x00FC	-	-	-	-

1.29 MTB_DWT

MTB_DWT Base_Address : 0xF000_1000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	CMP_ADDR_START[B,H,W]			
	00000000 00000000 00000000 00000000			
0x004	CMP_DATA_START[B,H,W]			
	00000000 00000000 00000000 00000000			
0x008	CMP_MASK_START[B,H,W]			
	00000000 00000000 00000000 00000000			
0x00C	-	-	-	-
0x010	CMP_ADDR_STOP[B,H,W]			
	00000000 00000000 00000000 00000000			
0x014	CMP_DATA_STOP[B,H,W]			
	00000000 00000000 00000000 00000000			
0x018	CMP_MASK_STOP[B,H,W]			
	00000000 00000000 00000000 00000000			
0x01C	-	-	-	-
0x020	-	-	-	FCT[B,H,W]
				00000000
0x024 - 0xFCC	-	-	-	-
0xFD0	PID4[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFD4	PID5[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFD8	PID6[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFDC	PID7[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFE0	PID0[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFE4	PID1[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFE8	PID2[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFEC	PID3[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFF0	CID0[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFF4	CID1[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFF8	CID2[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0xFFC	CID3[B,H,W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			

1.30 Fast GPIO

Fast GPIO **Base_Address : 0xF800_0000**

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	FPDIR0[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x004	-	-	FPDIR1[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x008	-	-	FPDIR2[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x00C	-	-	FPDIR3[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x010	-	-	FPDIR4[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x014	-	-	FPDIR5[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x018	-	-	FPDIR6[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x01C	-	-	FPDIR7[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x020	-	-	FPDIR8[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x024	-	-	FPDIR9[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x028	-	-	FPDIRA[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x02C	-	-	FPDIRB[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x030	-	-	FPDIRC[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x034	-	-	FPDIRD[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x038	-	-	FPDIRE[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x03C	-	-	FPDIRF[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x040	-	-	FPDOR0[B,H,W]	
			00000000 00000000	
0x044	-	-	FPDOR1[B,H,W]	
			00000000 00000000	

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x048	-	-	FPDOR2[B,H,W]	
			00000000 00000000	
0x04C	-	-	FPDOR3[B,H,W]	
			00000000 00000000	
0x050	-	-	FPDOR4[B,H,W]	
			00000000 00000000	
0x054	-	-	FPDOR5[B,H,W]	
			00000000 00000000	
0x058	-	-	FPDOR6[B,H,W]	
			00000000 00000000	
0x05C	-	-	FPDOR7[B,H,W]	
			00000000 00000000	
0x060	-	-	FPDOR8[B,H,W]	
			00000000 00000000	
0x064	-	-	FPDOR9[B,H,W]	
			00000000 00000000	
0x068	-	-	FPDORA[B,H,W]	
			00000000 00000000	
0x06C	-	-	FPDORB[B,H,W]	
			00000000 00000000	
0x070	-	-	FPDORC[B,H,W]	
			00000000 00000000	
0x074	-	-	FPDORD[B,H,W]	
			00000000 00000000	
0x078	-	-	FPDORE[B,H,W]	
			00000000 00000000	
0x07C	-	-	FPDORF[B,H,W]	
			00000000 00000000	
0x080	-	-	-	M_FPDIR0[B,H,W]
				XXXXXXXX
0x084	-	-	-	M_FPDIR1[B,H,W]
				XXXXXXXX
0x088	-	-	-	M_FPDIR2[B,H,W]
				XXXXXXXX
0x08C	-	-	-	M_FPDIR3[B,H,W]
				XXXXXXXX
0x090	-	-	-	M_FPDIR4[B,H,W]
				XXXXXXXX
0x094	-	-	-	M_FPDIR5[B,H,W]
				XXXXXXXX

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x098	-	-	-	M_FPDIR6[B,H,W]
				XXXXXXXX
0x09C	-	-	-	M_FPDIR7[B,H,W]
				XXXXXXXX
0x0A0	-	-	-	M_FPDIR8[B,H,W]
				XXXXXXXX
0x0A4	-	-	-	M_FPDIR9[B,H,W]
				XXXXXXXX
0x0A8	-	-	-	M_FPDIRA[B,H,W]
				XXXXXXXX
0x0AC	-	-	-	M_FPDIRB[B,H,W]
				XXXXXXXX
0x0B0	-	-	-	M_FPDIRC[B,H,W]
				XXXXXXXX
0x0B4	-	-	-	M_FPDIRD[B,H,W]
				XXXXXXXX
0x0B8	-	-	-	M_FPDIRE[B,H,W]
				XXXXXXXX
0x0BC	-	-	-	M_FPDIRF[B,H,W]
				XXXXXXXX
0x0C0	-	-	-	M_FPDOR0[B,H,W]
				00000000
0x0C4	-	-	-	M_FPDOR1[B,H,W]
				00000000
0x0C8	-	-	-	M_FPDOR2[B,H,W]
				00000000
0x0CC	-	-	-	M_FPDOR3[B,H,W]
				00000000
0x0D0	-	-	-	M_FPDOR4[B,H,W]
				00000000
0x0D4	-	-	-	M_FPDOR5[B,H,W]
				00000000
0x0D8	-	-	-	M_FPDOR6[B,H,W]
				00000000
0x0DC	-	-	-	M_FPDOR7[B,H,W]
				00000000
0x0E0	-	-	-	M_FPDOR8[B,H,W]
				00000000
0x0E4	-	-	-	M_FPDOR9[B,H,W]
				00000000
0x0E8	-	-	-	M_FPDORA[B,H,W]
				00000000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x0EC	-	-	-	M_FPDORB[B,H,W]
				00000000
0x0F0	-	-	-	M_FPDORC[B,H,W]
				00000000
0x0F4	-	-	-	M_FPDORD[B,H,W]
				00000000
0x0F8	-	-	-	M_FPDORE[B,H,W]
				00000000
0x0FC	-	-	-	M_FPDORF[B,H,W]
				00000000
0x100 - 0xFFC	-	-	-	-

C. Register Map (TYPE2-M0+)

This chapter shows the register map.

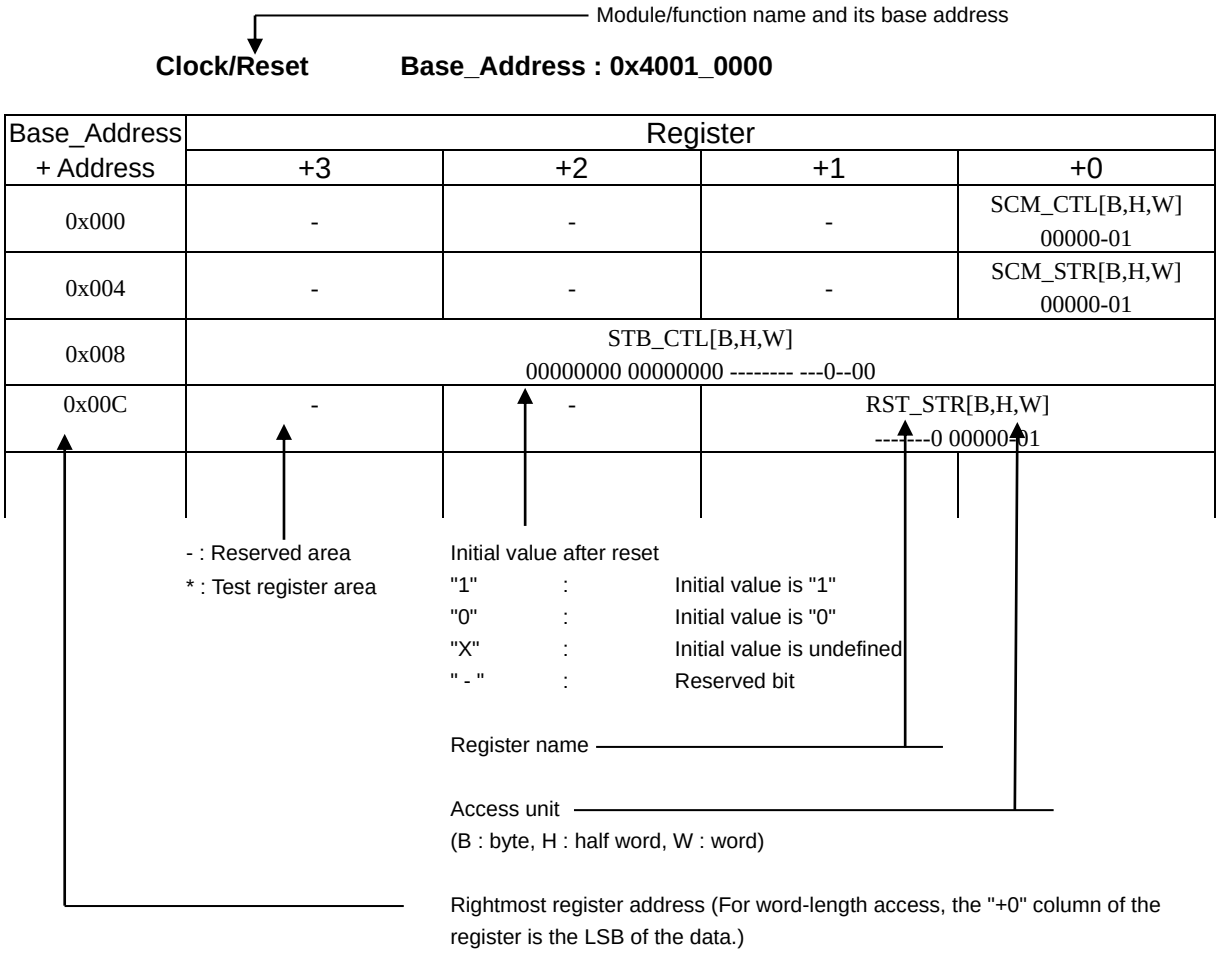
1. Register Map

CODE: 9AFREGMAP-E01.0

1. Register Map

Register map is shown on the table every module/function.

[How to Read the Each Table]



Notes:

- The register table is represented in the little-endian.
- When performing a data access, the addresses should be as below according to the access size.
  - Word access : Address should be multiples of 4 (least significant 2 bits should be "0x00")
  - Half word access : Address should be multiples of 2 (least significant bit should be "0x0")
  - Byte access : -
- Do not access the test register area.
- Do not access the area that is not written in the register table.
- When the register is accessed by larger unit than register size, for the reserved area to access at the same time, the read value is undefined, and writing is invalid.

1.1 Flash I/F

Flash I/F Base_Address : 0x4000_0000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	-
0x004	FRWTR[B,H,W]			
0x008	FSTR[B,H,W]			
0x00C	FRVRC[B,H,W]			
0x010	FSYNDN[B,H,W]			
0x014 - 0x01C	-	-	-	-
0x020	FICR[B,H,W]			
0x024	FISR[B,H,W]			
0x028	FICLR[B,H,W]			
0x02C - 0x0FC	-	-	-	-
0x100	CRTRMM[B,H,W]			
0x104 - 0x1FC	-	-	-	-

Note:

- *For details of Flash I/F registers, refer to "FLASH PROGRAMMING MANUAL" of the product used.*

1.2 Unique ID

Unique ID Base_Address : 0x4000_0200

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	UIDR0[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXX----			
0x004	UIDR1[W]			
	-------- -------- ---XXXXX XXXXXXXX			
0x008 – 0xDFC	-	-	-	-

1.3 Clock/Reset

Clock/Reset Base_Address : 0x4001_0000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	SCM_CTL[W]
				00000-01
0x004	-	-	-	SCM_STR[W]
				00000-01
0x008	STB_CTL[W]			
	00000000 00000000 -------- ---0-000			
0x00C	-	-	RST_STR[W]	
			-------0 0000--01	
0x010	-	-	-	BSC_PSR[W]
				-----000
0x014	-	-	-	APBC0_PSR[W]
				------00
0x018	-	-	-	APBC1_PSR[W]
				1--0--00
0x01C	-	-	-	-
0x020	-	-	-	SWC_PSR[W]
				X-----00
0x024 - 0x02C	-	-	-	-
0x030	-	-	-	CSW_TMR[W]
				00000000
0x034	-	-	-	PSW_TMR[W]
				---0-000
0x038	-	-	-	PLL_CTL1[W]
				00000000
0x03C	-	-	-	PLL_CTL2[W]
				--000000
0x040	-	-	CSV_CTL[W]	
			-111--00 ------11	
0x044	-	-	-	CSV_STR[W]
				------00
0x048	-	-	FCSWH_CTL[W]	
			11111111 11111111	
0x04C	-	-	FCSWL_CTL[W]	
			00000000 00000000	
0x050	-	-	FCSWD_STR[W]	
			00000000 00000000	

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x054	-	-	-	DBWDT_CTL[W]
				0-0-----
0x058	-	-	-	*
0x05C	-	-	-	-
0x060	-	-	-	INT_ENR[W]
				--0--000
0x064	-	-	-	INT_STR[W]
				--0--000
0x068	-	-	-	INT_CLR[W]
				--0--000
0x06C - 0xFFC	-	-	-	-

1.4 HW WDT

HW WDT Base_Address : 0x4001_1000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	WDG_LDR[W]			
	00000000 00000000 11111111 11111111			
0x004	WDG_VLR[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x008	-	-	-	WDG_CTL[W]
				------11
0x00C	-	-	-	WDG_ICL[W]
				XXXXXXXX
0x010	-	-	-	WDG_RIS[R]
				-------0
0x014 - 0xBFC	-	-	-	-
0xC00	WDG_LCK[W]			
	00000000 00000000 00000000 00000001			
0xC04 - 0xFFC	-	-	-	-

1.5 SW_WDT

SW WDT Base_Address : 0x4001_2000

Base_Address	Register			
+ Address	**+3**	**+2**	**+1**	**+0**
0x000	WdogLoad[W]			
	11111111 11111111 11111111 11111111			
0x004	WdogValue[W]			
	11111111 11111111 11111111 11111111			
0x008	-	-	-	WdogControl[W]
				---00000
0x00C	WdogIntClr[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x010	-	-	-	WdogRIS[R]
				-------0
0x014	*			
0x018	-	-	-	WdogSPMC[W]
				-------0
0x01C - 0xBFC	-	-	-	-
0xC00	WdogLock[W]			
	00000000 00000000 00000000 00000000			
0xC04 - 0xDFC	-	-	-	-
0xF00	*			
0xF08 - 0xFDF	-	-	-	-
0xFE0 - 0xFFC	*			

1.6 Dual Timer

Dual Timer Base_Address : 0x4001_5000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	Timer1Load[W]			
	00000000 00000000 00000000 00000000			
0x004	Timer1Value[W]			
	11111111 11111111 11111111 11111111			
0x008	Timer1Control[W]			
	-------- -------- -------- 00100000			
0x00C	Timer1IntClr[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x010	Timer1RIS[W]			
	-------- -------- -------- -------0			
0x014	Timer1MIS[W]			
	-------- -------- -------- -------0			
0x018	Timer1BGLoad[W]			
	00000000 00000000 00000000 00000000			
0x020	Timer2Load[W]			
	00000000 00000000 00000000 00000000			
0x024	Timer2Value[W]			
	11111111 11111111 11111111 11111111			
0x028	Timer2Control[W]			
	-------- -------- -------- 00100000			
0x02C	Timer2IntClr[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x030	Timer2RIS[W]			
	-------- -------- -------- -------0			
0x034	Timer2MIS[W]			
	-------- -------- -------- -------0			
0x038	Timer2BGLoad[W]			
	00000000 00000000 00000000 00000000			
0x040 - 0xFFC	-	-	-	-

1.7 MFT

MFT unit0 Base_Address : 0x4002_0000

MFT unit1 Base_Address : 0x4002_1000

MFT unit2 Base_Address : 0x4002_2000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x100	OCCP0[H,W] 00000000 00000000		-	-
0x104	OCCP1[H,W] 00000000 00000000		-	-
0x108	OCCP2[H,W] 00000000 00000000		-	-
0x10C	OCCP3[H,W] 00000000 00000000		-	-
0x110	OCCP4[H,W] 00000000 00000000		-	-
0x114	OCCP5[H,W] 00000000 00000000		-	-
0x118	OCSD10[B,H,W] --000000 00000000		OCSB10[B,H,W] 00000000	OCSA10[B,H,W] 00000000
0x11C	OCSD32[B,H,W] --000000 00000000		OCSB32[B,H,W] 00000000	OCSA32[B,H,W] 00000000
0x120	OCSD54[B,H,W] --000000 00000000		OCSB54[B,H,W] 00000000	OCSA54[B,H,W] 00000000
0x124	-	-	OCSC[B,H,W] --000000	-
0x128	-	-	OCSE0[B,H,W] 00000000 00000000	
0x12C	OCSE1[B,H,W] 00000000 00000000 00000000 00000000			
0x130	-	-	OCSE2[B,H,W] 00000000 00000000	
0x134	OCSE3[B,H,W] 00000000 00000000 00000000 00000000			
0x138	-	-	OCSE4[B,H,W] 00000000 00000000	
0x13C	OCSE5[B,H,W] 00000000 00000000 00000000 00000000			
0x140	TCCP0[H,W] 11111111 11111111		-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x144	TCDT0[H,W] 00000000 00000000		-	-
0x148	TCSC0[H,W] 00000000 00000000		TCSA0[B,H,W] 00000000 01000000	
0x14C	TCCP1[H,W] 11111111 11111111		-	-
0x150	TCDT1[H,W] 00000000 00000000		-	-
0x154	TCSC1[H,W] 00000000 00000000		TCSA1[B,H,W] 00000000 01000000	
0x158	TCCP2[H,W] 11111111 11111111		-	-
0x15C	TCDT2[H,W] 00000000 00000000		-	-
0x160	TCSC2[H,W] 00000000 00000000		TCSA2[B,H,W] 00000000 01000000	
0x164	TCAL[W] 00000000 00000000 11111111 11111111 *1			
	-	-	-	- *2
	*1 MFT unit0 *2 MFT unit1,unit2			
0x168	-	OCFS54[B,H,W] 00000000	OCFS32[B,H,W] 00000000	OCFS10[B,H,W] 00000000
0x16C	-	-	ICFS32[B,H,W] 00000000	ICFS10[B,H,W] 00000000
0x170	-	ACFS54[B,H,W] 00000000	ACFS32[B,H,W] 00000000	ACFS10[B,H,W] 00000000
0x174	ICCP0[H,W] 00000000 00000000		-	-
0x178	ICCP1[H,W] 00000000 00000000		-	-
0x17C	ICCP2[H,W] 00000000 00000000		-	-
0x180	ICCP3[H,W] 00000000 00000000		-	-
0x184	-	-	ICSB10[B,H,W] ------00	ICSA10[B,H,W] 00000000
0x188			ICSB32[B,H,W] ------00	ICSA32[B,H,W] 00000000
0x18C	WFTF10[H,W] 00000000 00000000		-	-
0x190	WFTB10[H,W] 00000000 00000000		WFTA10[H,W] 00000000 00000000	

Base_Address + Address	Register			
	+3	+2	+1	+0
0x194	WFTF32[H,W] 00000000 00000000		-	-
0x198	WFTB32[H,W] 00000000 00000000		WFTA32[H,W] 00000000 00000000	
0x19C	WFTF54[H,W] 00000000 00000000		-	-
0x1A0	WFTB54[H,W] 00000000 00000000		WFTA54[H,W] 00000000 00000000	
0x1A4	-	-	WFSA10[B,H,W] --000000 000000	
0x1A8	-	-	WFSA32[B,H,W] --000000 000000	
0x1AC	-	-	WFSA54[B,H,W] --000000 000000	
0x1B0	-	-	WFIR[H,W] 00000000 00000000	
0x1B4	-	-	NZCL[H,W] 00000000 00000000	
0x1B8	ACMP0[H,W] 00000000 00000000		-	-
0x1BC	ACMP1[H,W] 00000000 00000000		-	-
0x1C0	ACMP2[H,W] 00000000 00000000		-	-
0x1C4	ACMP3[H,W] 00000000 00000000		-	-
0x1C8	ACMP4[H,W] 00000000 00000000		-	-
0x1CC	ACMP5[H,W] 00000000 00000000		-	-
0x1D0	-	-	ACSA[B,H,W] 00000000 00000000	
0x1D4	-	ACMC0[B,H,W] 00--0000	ACSD0[B,H,W] 00000000	ACSC0[B,H,W] 00000000
0x1D8	-	ACMC1[B,H,W] 00--0000	ACSD1[B,H,W] 00000000	ACSC1[B,H,W] 00000000
0x1DC	-	ACMC2[B,H,W] 00--0000	ACSD2[B,H,W] 00000000	ACSC2[B,H,W] 00000000
0x1E0	-	ACMC3[B,H,W] 00--0000	ACSD3[B,H,W] 00000000	ACSC3[B,H,W] 00000000
0x1E4	-	ACMC4[B,H,W] 00--0000	ACSD4[B,H,W] 00000000	ACSC4[B,H,W] 00000000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x1E8	-	ACMC5[B,H,W] 00--0000	ACSD5[B,H,W] 00000000	ACSC5[B,H,W] 00000000
0x1EC	-	-	-	TCSD[B,H,W] ------00
0x1F0-0xFFC	-	-	-	-

1.8 PPG

PPG Base_Address : 0x4002_4000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	TTCR0[B,H,W] 11110000	-
0x004	-	-	-	*
0x008	-	-	COMP0[B,H,W] 00000000	-
0x00C	-	-	-	COMP2[B,H,W] 00000000
0x010	-	-	COMP4[B,H,W] 00000000	-
0x014	-	-	-	COMP6[B,H,W] 00000000
0x018 - 0x01C	-	-	-	-
0x020	-	-	TTCR1[B,H,W] 11110000	-
0x024	-	-	-	*
0x028	-	-	COMP1[B,H,W] 00000000	-
0x02C	-	-	-	COMP3[B,H,W] 00000000
0x030	-	-	COMP5[B,H,W] 00000000	-
0x034	-	-	-	COMP7[B,H,W] 00000000
0x038 - 0x03C	-	-	-	-
0x040	-	-	TTCR2[B,H,W] 11110000	-
0x044	-	-	-	*
0x048	-	-	COMP8[B,H,W] 00000000	-
0x04C	-	-	-	COMP10[B,H,W] 00000000
0x050	-	-	COMP12[B,H,W] 00000000	-
0x054	-	-	-	COMP14[B,H,W] 00000000
0x058 - 0x0FC	-	-	-	-

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x100	-	-	TRG0[B,H,W]	
			00000000 00000000	
0x104	-	-	REVC0[B,H,W]	
			00000000 00000000	
0x108 - 0x13C	-	-	-	-
0x140	-	-	TRG1[B,H,W]	
			-------- 00000000	
0x144	-	-	REVC1[B,H,W]	
			-------- 00000000	
0x148 - 0x1FC	-	-	-	-
0x200	-	-	PPGC0[B,H,W]	PPGC1[B,H,W]
			00000000	00000000
0x204	-	-	PPGC2[B,H,W]	PPGC3[B,H,W]
			00000000	00000000
0x208	-	-	PRLH0[B,H,W]	PRLL0[B,H,W]
			XXXXXXXX	XXXXXXXX
0x20C	-	-	PRLH1[B,H,W]	PRLL1[B,H,W]
			XXXXXXXX	XXXXXXXX
0x210	-	-	PRLH2[B,H,W]	PRLL2[B,H,W]
			XXXXXXXX	XXXXXXXX
0x214	-	-	PRLH3[B,H,W]	PRLL3[B,H,W]
			XXXXXXXX	XXXXXXXX
0x218	-	-	-	GATEC0[B,H,W]
				--00---00
0x21C - 0x23C	-	-	-	-
0x240	-	-	PPGC4[B,H,W]	PPGC5[B,H,W]
			00000000	00000000
0x244	-	-	PPGC6[B,H,W]	PPGC7[B,H,W]
			00000000	00000000
0x248	-	-	PRLH4[B,H,W]	PRLL4[B.H.W]
			XXXXXXXX	XXXXXXXX
0x24C	-	-	PRLH5[B,H,W]	PRLL5[B,H,W]
			XXXXXXXX	XXXXXXXX
0x250	-	-	PRLH6[B,H,W]	PRLL6[B,H,W]
			XXXXXXXX	XXXXXXXX
0x254	-	-	PRLH7[B,H,W]	PRLL7[B,H,W]
			XXXXXXXX	XXXXXXXX
0x258	-	-	-	GATEC4[B,H,W]
				--00--00
0x25C - 0x27C	-	-	-	-
0x280	-	-	PPGC8[B,H,W]	PPGC9[B,H,W]
			00000000	00000000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x284	-	-	PPGC10[B,H,W]	PPGC11[B,H,W]
			00000000	00000000
0x288	-	-	PRLH8[B,H,W]	PRLL8[B,H,W]
			XXXXXXXX	XXXXXXXX
0x28C	-	-	PRLH9[B,H,W]	PRLL9[B,H,W]
			XXXXXXXX	XXXXXXXX
0x290	-	-	PRLH10[B,H,W]	PRLL10[B,H,W]
			XXXXXXXX	XXXXXXXX
0x294	-	-	PRLH11[B,H,W]	PRLL11[B,H,W]
			XXXXXXXX	XXXXXXXX
0x298	-	-	-	GATEC8[B,H,W]
				--00--00
0x29C - 0x2BC	-	-	-	-
0x2C0	-	-	PPGC12[B,H,W]	PPGC13[B,H,W]
			00000000	00000000
0x2C4	-	-	PPGC14[B,H,W]	PPGC15[B,H,W]
			00000000	00000000
0x2C8	-	-	PRLH12[B,H,W]	PRLL12[B,H,W]
			XXXXXXXX	XXXXXXXX
0x2CC	-	-	PRLH13[B,H,W]	PRLL13[B,H,W]
			XXXXXXXX	XXXXXXXX
0x2D0	-	-	PRLH14[B,H,W]	PRLL14[B,H,W]
			XXXXXXXX	XXXXXXXX
0x2D4	-	-	PRLH15[B,H,W]	PRLL15[B,H,W]
			XXXXXXXX	XXXXXXXX
0x2D8	-	-	-	GATEC12[B,H,W]
				--00--00
0x2DC - 0x2FC	-	-	-	-
0x300	-	-	PPGC16[B,H,W]	PPGC17[B,H,W]
			00000000	00000000
0x304	-	-	PPGC18[B,H,W]	PPGC19[B,H,W]
			00000000	00000000
0x308	-	-	PRLH16[B,H,W]	PRLL16[B,H,W]
			XXXXXXXX	XXXXXXXX
0x30C	-	-	PRLH17[B,H,W]	PRLL17[B,H,W]
			XXXXXXXX	XXXXXXXX
0x310	-	-	PRLH18[B,H,W]	PRLL18[B,H,W]
			XXXXXXXX	XXXXXXXX
0x314	-	-	PRLH19[B,H,W]	PRLL19[B,H,W]
			XXXXXXXX	XXXXXXXX
0x318	-	-	-	GATEC16[B,H,W]
				--00---00
0x31C - 0x33C	-	-	-	-
0x340	-	-	PPGC20[B,H,W]	PPGC21[B,H,W]

Base_Address	Register			
+ Address	+3	+2	+1	+0
			00000000	00000000
0x344	-	-	PPGC22[B,H,W]	PPGC23[B,H,W]
			00000000	00000000
0x348	-	-	PRLH20[B,H,W]	PRLL20[B,H,W]
			XXXXXXXX	XXXXXXXX
0x34C	-	-	PRLH21[B,H,W]	PRLL21[B,H,W]
			XXXXXXXX	XXXXXXXX
0x350	-	-	PRLH22[B,H,W]	PRLL22[B,H,W]
			XXXXXXXX	XXXXXXXX
0x354	-	-	PRLH23[B,H,W]	PRLL23[B,H,W]
			XXXXXXXX	XXXXXXXX
0x358	-	-	-	GATEC20[B,H,W]
				--00--00
0x35C - 0x37C	-	-	-	-
0x380	-	-	-	IGBTC[B,H,W]
				00000000
0x384 - 0xFFC	-	-	-	-

1.9 Base Timer

Base Timer ch.0 Base Address : 0x4002_5000

Base Timer ch.1 Base Address : 0x4002_5040

Base Timer ch.2 Base Address : 0x4002_5080

Base Timer ch.3 Base Address : 0x4002_50C0

Base Timer ch.4 Base Address : 0x4002_5200

Base Timer ch.5 Base Address : 0x4002_5240

Base Timer ch.6 Base Address : 0x4002_5280

Base Timer ch.7 Base Address : 0x4002_52C0

Base Timer ch.8 Base Address : 0x4002_5400

Base Timer ch.9 Base Address : 0x4002_5440

Base Timer ch.10 Base Address : 0x4002_5480

Base Timer ch.11 Base Address : 0x4002_54C0

Base Timer ch.12 Base Address : 0x4002_5600

Base Timer ch.13 Base Address : 0x4002_5640

Base Timer ch.14 Base Address : 0x4002_5680

Base Timer ch.15 Base Address : 0x4002_56C0

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	PCSR/PRLL[H,W]	
			XXXXXXXX XXXXXXXX	
0x004	-	-	PDUT/PRLH/DTBF[H,W]	
			XXXXXXXX XXXXXXXX	
0x008	-	-	TMR[H,W]	
			00000000 00000000	
0x00C	-	-	TMCR[B,H,W]	
			-0000000 00000000	
0x010	-	-	TMCR2[B,H,W]	STC[B,H,W]
			-------0	0000-000
0x014 - 0x03C	-	-	-	-

1.10 IO Selector for Base Timer

IO Selector for ch.0-ch.3 (Base Timer) Base Address : 0x4002_5100

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	BTSEL0123[B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

IO Selector for ch.4-ch.7 (Base Timer) Base Address : 0x4002_5300

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	BTSEL4567[B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

IO Selector for ch.8-ch.11 (Base Timer) Base Address : 0x4002_5500

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	BTSEL89AB[B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

IO Selector for ch.12-ch.15 (Base Timer) Base Address : 0x4002_5700

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	BTSELCDEF[B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

Software-based Simultaneous Startup (Base Timer) Base Address : 0x4002_5F00

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000 - 0x0FB	-	-	-	-
0x0FC	-	-	BTSSSR[B,H,W] XXXXXXXX XXXXXXXX	

1.11 QPRC

QPRC ch.0 **Base Address : 0x4002_6000**

QPRC ch.1 **Base Address : 0x4002_6040**

QPRC ch.2 **Base Address : 0x4002_6080**

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x0000	-	-	QPCR[H,W]	
			00000000 00000000	
0x0004	-	-	QRCR[H,W]	
			00000000 00000000	
0x0008	-	-	QPCCR[H,W]	
			00000000 00000000	
0x000C	-	-	QPRCR[H,W]	
			00000000 00000000	
0x0010	-	-	QMPR[H,W]	
			11111111 11111111	
0x0014	-	-	QICRH[B,H,W]	QICRL[B,H,W]
			--000000	00000000
0x0018	-	-	QCRH[B,H,W]	QCRL[B,H,W]
			00000000	00000000
0x001C	-	-	QECR[B,H,W]	
			-------- -----000	
0x0020 - 0x0038	-	-	-	-
0x003C	QPCRR[B,H,W]		QRCRR[B,H,W]	
	00000000 00000000		00000000 00000000	

1.12 QPRC NF

QPRC ch.0 NF **Base Address : 0x4002_6100**

QPRC ch.1 NF **Base Address : 0x4002_6110**

QPRC ch.2 NF **Base Address : 0x4002_6120**

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x0000	NFCTLA[B,H,W]			
	-------- -------- -------- --00-000			
0x0004	NFCTLB[B,H,W]			
	-------- -------- -------- --00-000			
0x0008	NFCTLC[B,H,W]			
	-------- -------- -------- --00-000			
0x000C	-	-	-	-

1.13 A/DC

12-bit A/DC unit0 Base_Address : 0x4002_7000

12-bit A/DC unit1 Base_Address : 0x4002_7100

12-bit A/DC unit2 Base_Address : 0x4002_7200

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	ADCR[B,H,W]	ADSR[B,H,W]
			000-0000	00---000
0x004	-	-	-	*
0x008	-	-	SCCR[B,H,W]	SFNS[B,H,W]
			1000-000	----0000
0x00C	SCFD[B,H,W]			
	XXXXXXXX XXXX---- ---X--XX ---XXXXX			
0x010	-	-	SCIS3[B,H,W]	SCIS2[B,H,W]
			00000000	00000000
0x014	-	-	SCIS1[B,H,W]	SCIS0[B,H,W]
			00000000	00000000
0x018	-	-	PCCR[B,H,W]	PFNS[B,H,W]
			1000-000	--XX--00
0x01C	PCFD[B,H,W]			
	XXXXXXXX XXXX---- ---X-XXX ---XXXXX			
0x020	-	-	-	PCIS[B,H,W]
				00000000
0x024	CMPD[B,H,W]		-	CMPCR[B,H,W]
	00000000 00------			00000000
0x028	-	-	ADSS3[B,H,W]	ADSS2[B,H,W]
			00000000	00000000
0x02C	-	-	ADSS1[B,H,W]	ADSS0[B,H,W]
			00000000	00000000
0x030	-	-	ADST0[B,H,W]	ADST1[B,H,W]
			00010000	00010000
0x034	-	-	-	ADCT[B,H,W]
				00000111
0x038	-	-	SCTSL[B,H,W]	PRTSL[B,H,W]
			----0000	----0000
0x03C	-	-	ADCEN[B,H,W]	
			11111111 ------00	
0x040	*			
0x044	WCMRCIF[B,H,W]			
	-------- -------- -------- -------0			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x048	WCMRCOT[B,H,W]			
	-------- -------- -------- -------0			
0x04C	-	-	WCMPSR[B,H,W]	WCMPCR[B,H,W]
			--000000	001000--
0x050	WCMPDH[B,H,W]		WCMPDL[B,H,W]	
	00000000 00------		00000000 00------	
0x054 - 0x0FC	-	-	-	-

1.14 D/AC

10-bit D/AC Base_Address : 0x4002_8000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x00	-	DACR0[B,H,W]	DADR0[B,H,W]	
		-------0	------XX XXXXXXXX	
0x04	-	DACR1[B,H,W]	DADR1[B,H,W]	
		-------0	------XX XXXXXXXX	
0x08 - 0xFC	-	-	-	-

1.15 CR Trim

CR Trim Base_Address : 0x4002_E000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	MCR_PSR[B,H,W]
				------001
0x004	-	-	MCR_FTRM[B,H,W]	
			------01 11101111	
0x008	-	-	-	MCR_TTRM[B,H,W]
				-0111111
0x00C	MCR_RLR[B,H,W]			
	00000000 00000000 00000000 00000001			
0x010 - 0x0FC	-	-	-	-

1.16 EXTI

EXTI Base_Address : 0x4003_0000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	ENIR[B,H,W]			
	00000000 00000000 00000000 00000000			
0x004	EIRR[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x008	EICL[B,H,W]			
	11111111 11111111 11111111 11111111			
0x00C	ELVR[B,H,W]			
	00000000 00000000 00000000 00000000			
0x010	ELVR1[B,H,W]			
	00000000 00000000 00000000 00000000			
0x014	-	-	NMIRR[B,H,W]	
			-------- -------0	
0x018	-	-	NMICL[B,H,W]	
			-------- -------1	
0x01C – 0x0FC	-	-	-	-

1.17 INT-Req. READ

INT-Req. READ Base_Address : 0x4003_1000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	-
0x004	*			
0x008 – 0x00B	-	-	-	-
0x00C	-	-	-	IRQCMODE[B,H,W]
				-------0
0x010	EXC02MON[B,H,W]			
	-------- -------- -------- ------00			
0x014	IRQ00MON[B,H,W]			
	-------- -------- -------- -------0			
0x018	IRQ01MON[B,H,W]			
	-------- -------- -------- -------0			
0x01C	IRQ02MON[B,H,W]			
	-------- -------- -------- -------0			
0x020	IRQ03MON[B,H,W]			
	-------- -------- -------- ----0000			
0x024	IRQ04MON[B,H,W]			
	-------- -------- -------- 00000000			
0x028	IRQ05MON[B,H,W]			
	-------- -------- 00000000 00000000			
0x02C	IRQ06MON[B,H,W]			
	-------- -------- -------- ------00			
0x030	IRQ07MON[B,H,W]			
	-------- -------- -------- -------0			
0x034	IRQ08MON[B,H,W]			
	-------- -------- -------- ------00			
0x038	IRQ09MON[B,H,W]			
	-------- -------- -------- -------0			
0x03C	IRQ10MON[B,H,W]			
	-------- -------- -------- ------00			
0x040	IRQ11MON[B,H,W]			
	-------- -------- -------- -------0			
0x044	IRQ12MON[B,H,W]			
	-------- -------- -------- ------00			
0x048	IRQ13MON[B,H,W]			
	-------- -------- -------- -------0			
0x04C	IRQ14MON[B,H,W]			
	-------- -------- -------- ------00			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x050	IRQ15MON[B,H,W]			
	-------- -------- -------- -------0			
0x054	IRQ16MON[B,H,W]			
	-------- -------- -------- ------00			
0x058	IRQ17MON[B,H,W]			
	-------- -------- -------- -------0			
0x05C	IRQ18MON[B,H,W]			
	-------- -------- -------- ------00			
0x060	IRQ19MON[B,H,W]			
	-------- -------- -------- -------0			
0x064	IRQ20MON[B,H,W]			
	-------- -------- -------- ------00			
0x068	IRQ21MON[B,H,W]			
	-------- -------- -------- -------0			
0x06C	IRQ22MON[B,H,W]			
	-------- -------- -------- ------00			
0x070	IRQ23MON[B,H,W]			
	-------- -------- ---0000- -----000			
0x074	IRQ24MON[B,H,W]			
	-------- -------- -----00- --000000			
0x078	IRQ25MON[B,H,W]			
	-------- -------- -------- ---00000			
0x07C	IRQ26MON[B,H,W]			
	-------- -------- -------- --000000			
0x080	IRQ27MON[B,H,W]			
	-------- -------- -------- --0-----			
0x084	IRQ28MON[B,H,W]			
	-------- -------- -------- --000000			
0x088	IRQ29MON[B,H,W]			
	-------- -------- -------0 00000000			
0x08C	IRQ30MON[B,H,W]			
	-------- -------- -------- --000000			
0x090	IRQ31MON[B,H,W]			
	----0--- -------- 00000000 00000000			
0x094 – 0x20C	-	-	-	-
0x210	RCINTSEL0[B,H,W]			
	00000000 00000000 00000000 00000000			
0x214	RCINTSEL1[B,H,W]			
	00000000 00000000 00000000 00000000			
0x218 – 0xFFC	-	-	-	-

1.18 LCDC

LCDC Base_Address : 0x4003_2000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x00	-	LCDCC3[B,H,W]	LCDCC2[B,H,W]	LCDCC1[B,H,W]
		0011111-	--010100	-00000--
0x04	LCDC_PSR[B,H,W]			
	-------- -0000000 00000000 00000000			
0x08	LCDC_COMEN[B,H,W]			
	-------- -------- -------- 00000000			
0x0C	LCDC_SEGEN1[B,H,W]			
	00000000 00000000 00000000 00000000			
0x10	LCDC_SEGEN2[B,H,W]			
	-------- -------- -------- 00000000			
0x14	-	-	LCDC_BLINK[B,H,W]	
			00000000 00000000	
0x18	-	-	LCDC_BOOSTER[B,H,W]	
			--001110	----0011
0x1C	LCDRAM03[B,H,W]	LCDRAM02[B,H,W]	LCDRAM01[B,H,W]	LCDRAM00[B,H,W]
	00000000	00000000	00000000	00000000
0x20	LCDRAM07[B,H,W]	LCDRAM06[B,H,W]	LCDRAM05[B,H,W]	LCDRAM04[B,H,W]
	00000000	00000000	00000000	00000000
0x24	LCDRAM11[B,H,W]	LCDRAM10[B,H,W]	LCDRAM09[B,H,W]	LCDRAM08[B,H,W]
	00000000	00000000	00000000	00000000
0x28	LCDRAM15[B,H,W]	LCDRAM14[B,H,W]	LCDRAM13[B,H,W]	LCDRAM12[B,H,W]
	00000000	00000000	00000000	00000000
0x2C	LCDRAM19[B,H,W]	LCDRAM18[B,H,W]	LCDRAM17[B,H,W]	LCDRAM16[B,H,W]
	00000000	00000000	00000000	00000000
0x30	LCDRAM23[B,H,W]	LCDRAM22[B,H,W]	LCDRAM21[B,H,W]	LCDRAM20[B,H,W]
	00000000	00000000	00000000	00000000
0x34	LCDRAM27[B,H,W]	LCDRAM26[B,H,W]	LCDRAM25[B,H,W]	LCDRAM24[B,H,W]
	00000000	00000000	00000000	00000000
0x38	LCDRAM31[B,H,W]	LCDRAM30[B,H,W]	LCDRAM29[B,H,W]	LCDRAM28[B,H,W]
	00000000	00000000	00000000	00000000
0x3C	LCDRAM35[B,H,W]	LCDRAM34[B,H,W]	LCDRAM33[B,H,W]	LCDRAM32[B,H,W]
	00000000	00000000	00000000	00000000
0x40	LCDRAM39[B,H,W]	LCDRAM38[B,H,W]	LCDRAM37[B,H,W]	LCDRAM36[B,H,W]
	00000000	00000000	00000000	00000000
0x44 – 0xFC	-	-	-	-

1.19 GPIO

GPIO Base_Address : 0x4003_3000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	PFR0[B,H,W]			
	---- ---- ---- ---- 0000 0000 0001 1111			
0x004	PFR1[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x008	PFR2[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x00C	PFR3[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x010	PFR4[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x014	PFR5[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x018	PFR6[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x01C	PFR7[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x020	PFR8[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x024	PFR9[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x028	PFRA[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x02C	PFRB[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x030	PFRC[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x034	PFRD[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x038	PFRE[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x03C	PFRF[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x040 – 0x0FC	-	-	-	-
0x100	PCR0[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 1010			
0x104	PCR1[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x108	PCR2[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x10C	PCR3[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x110	PCR4[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x114	PCR5[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x118	PCR6[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x11C	PCR7[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x120	-	-	-	-
0x124	PCR9[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x128	PCRA[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x12C	PCRB[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x130	PCRC[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x134	PCRD[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x138	PCRE[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x13C	PCRF[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x140 – 0x1FC	-	-	-	-
0x200	DDR0[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x204	DDR1[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x208	DDR2[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x20C	DDR3[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x210	DDR4[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x214	DDR5[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x218	DDR6[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x21C	DDR7[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x220	DDR8[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x224	DDR9[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x228	DDRA[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x22C	DDRB[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x230	DDRC[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x234	DDRD[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x238	DDRE[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x23C	DDRF[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x240 – 0x2FC	-	-	-	-
0x300	PDIR0[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x304	PDIR1[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x308	PDIR2[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x30C	PDIR3[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x310	PDIR4[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x314	PDIR5[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x318	PDIR6[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x31C	PDIR7[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x320	PDIR8[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x324	PDIR9[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x328	PDIRA[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x32C	PDIRB[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x330	PDIRC[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x334	PDIRD[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x338	PDIRE[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x33C	PDIRF[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x340 – 0x3FC	-	-	-	-
0x400	PDOR0[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x404	PDOR1[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x408	PDOR2[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x40C	PDOR3[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x410	PDOR4[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x414	PDOR5[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x418	PDOR6[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x41C	PDOR7[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x420	PDOR8[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x424	PDOR9[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x428	PDORA[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x42C	PDORB[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x430	PDORC[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x434	PDORD[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x438	PDORE[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x43C	PDORF[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x440 – 0x4FC	-	-	-	-
0x500	ADE[B,H,W]			
	---- ---- 1111 1111 1111 1111 1111 1111			
0x504 – 0x57C	-	-	-	-
0x580	SPSR[B,H,W]			
	---- ---- ---- ---- ---- ---- ---- 0101			
0x584 – 0x5FC	-	-	-	-
0x600	EPFR00[B,H,W]			
	---- ---- ---- ---1 ---- ---- 0000 -000			
0x604	EPFR01[B,H,W]			
	0000 0000 0000 0000 –00 0000 0000 0000			
0x608	EPFR02[B,H,W]			
	0000 0000 0000 0000 ---0 0000 0000 0000			
0x60C	EPFR03[B,H,W]			
	0000 0000 0000 0000 ---0 0000 0000 0000			
0x610	EPFR04[B,H,W]			
	--00 0000 –00 00-- --00 0000 -000 00--			
0x614	EPFR05[B,H,W]			
	--00 0000 –00 00-- --00 0000 –00 00--			
0x618	EPFR06[B,H,W]			
	0000 0000 0000 0000 0000 0000 0000 0000			
0x61C	EPFR07[B,H,W]			
	---- 0000 0000 0000 0000 0000 0000 ----			
0x620	EPFR08[B,H,W]			
	---- 0000 0000 0000 0000 0000 0000 0000			
0x624	EPFR09[B,H,W]			
	---- ---- ---- ---- 0000 ---- ---- ----			
0x628 – 0x638	-	-	-	-
0x63C	EPFR15[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x640	EPFR16[B,H,W]			
	---- 0000 0000 0000 0000 0000 0000 0000			
0x644	-			
	-	-	-	-
0x648	EPFR18[B,H,W]			
	--00 0000 0000 0000 0000 0000 0000 0000			
0x64C – 0x658	-	-	-	-
0x65C	EPFR23[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x660 – 0x680	-	-	-	-

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x684	EPFR33[B,H,W]			
	---- 0000 0000 0000 ---- 0000 0000 0000			
0x688	EPFR34[B,H,W]			
	---- ---- ---- ---- ---- ---- 0000 ----			
0x68C – 0x690	-	-	-	-
0x694	EPFR37[B,H,W]			
	---- 0000 0000 0000 ---- ---- ---- ----			
0x698	EPFR38[B,H,W]			
	---- ---- ---- ---- ---- 0000 0000 0000			
0x69C – 0x6FC	-	-	-	-
0x700	PZR0[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x704	PZR1[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x708	PZR2[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x70C	PZR3[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x710	PZR4[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x714	PZR5[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x718	PZR6[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x71C	PZR7[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x720	PZR8[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x724	PZR9[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x728	PZRA[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x72C	PZRB[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x730	PZRC[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x734	PZRD[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x738	PZRE[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x73C	PZRF[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x740	LVDIE[B,H,W]			
	---- ---- ---- ---- ---- ---- ---- ---0			
0x744 – 0x7FC	-	-	-	-
0x800	*			
0x804	*			
0x808 – 0x8FC	-	-	-	-
0x900	FPOER0[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x904	FPOER1[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x908	FPOER2[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x90C	FPOER3[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x910	FPOER4[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x914	FPOER5[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x918	FPOER6[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x91C	FPOER7[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x920	FPOER8[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x924	FPOER9[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x928	FPOERA[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x92C	FPOERB[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x930	FPOERC[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x934	FPOERD[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x938	FPOERE[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x93C	FPOERF[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x940 – 0xFFC	-	-	-	-

1.20 HDMI-CEC

HDMI-CEC/Remote Control Receiver ch.0 Base_Address : 0x4003_4000

HDMI-CEC/Remote Control Receiver ch.1 Base_Address : 0x4003_4100

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x00	-	-	-	TXCTRL[B,H,W]
				000000-0
0x04	-	-	-	TXDATA[B,H,W]
				00000000
0x08	-	-	-	TXSTS[B,H,W]
				0-00---0
0x0C	-	-	-	SFREE[B,H,W]
				----0000
0x10 – 0x3F	-	-	-	-
0x40	-	-	RCCR[B,H,W]	RCST[B,H,W]
			0---0000	00000000
0x44	-	-	RCSHW[B,H,W]	RCDAHW[B,H,W]
			00000000	00000000
0x48	-	-	RCDBHW[B,H,W]	-
			00000000	
0x4C	-	-	RCADR1[B,H,W]	RCADR2[B,H,W]
			---00000	---00000
0x50	-	-	RCDTHH[B,H,W]	RCDTHL[B,H,W]
			00000000	00000000
0x54	-	-	RCDTLH[B,H,W]	RCDTLL[B,H,W]
			00000000	00000000
0x58	-	-	RCCKD[H,W]	
			---00000 00000000	
0x5C	-	-	RCRC[B,H,W]	RCRHW[B,H,W]
			---0---0	00000000
0x60	-	-	RCLE[B,H,W]	-
			00000-00	
0x64	-	-	RCLELW[B,H,W]	RCLESW[B,H,W]
			00000000	00000000
0x68 – 0xFC	-	-	-	-

1.21 LVD

LVD Base_Address : 0x4003_5000

Base_Address	Register			
+ Address	**+3**	**+2**	**+1**	**+0**
0x000	-	-	LVD_CTL [B,H,W]	
			100000–000011--	
0x004	-	-	LVD_STR [B,H,W]	
			0------1 0------1	
0x008	-	-	LVD_CLR [B,H,W]	
			1------- 1-------	
0x00C	LVD_RLR [W]			
	---------- 00000000 00000001			
0x010	-	-	LVD_STR2 [B,H,W]	
			0------- 01------	
0x014	-	-	LVD_CTL2 [B,H,W]	
			-------0 000011--	
0x018	-	-	-	LVD2_CTL [B,H,W]
				000011--
0x01C	-	-	LVD2_CTL2 [B,H,W]	
			0------0 000011--	
0x020 – 0x0FC	-	-	-	-

1.22 DS Mode

DS Mode Base_Address : 0x4003_5100

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	REG_CTL [B,H,W]
				---- -10-
0x004	-	-	-	RCK_CTL [B,H,W]
				---- --01
0x008	-	-	-	REG_CTL2 [B,H,W]
				---- -011
0x00C	-	-	-	-
0x010	-	-	-	MOSC_CTL [B,H,W]
				---- -10-
0x014 – 0x0FC	-	-	-	-
0x100	-	-	-	CAL_CTL [B,H,W]
				---- 0000
0x104	-	-	-	CAL_SET [B,H,W]
				---1 0001
0x108	CAL_KEY [W]			
	00000000 00000000 00000000 00000001			
0x10C – 0x1FC	-	-	-	-
0x200 – 0x6FC	-	-	-	-
0x700	-	-	-	PMD_CTL [B,H,W]
				---- ---0
0x704	-	-	-	WRFSR [B,H,W]
				---- --00
0x708	-	-	WIFSR [B,H,W]	
			00000000 00000000	
0x70C	-	-	WIER [B,H,W]	
			00000000 00000-00	
0x710	-	-	WILVR [B,H,W]	
			-----000 00000000	
0x714	-	-	-	DSRAMR [B,H,W]
				---- --00
0x718 – 0x71C	-	-	-	-
0x720	-	-	-	STBFLASHPDX [B,H,W]
				---- ---0
0x724	RST_MSK [W]			
	00000000 00000000 -------- -------0			
0x728 – 0x7FC	-	-	-	-

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x800	BUR04 [B,H,W]	BUR03 [B,H,W]	BUR02 [B,H,W]	BUR01 [B,H,W]
	00000000	00000000	00000000	00000000
0x804	BUR08 [B,H,W]	BUR07 [B,H,W]	BUR06 [B,H,W]	BUR05 [B,H,W]
	00000000	00000000	00000000	00000000
0x808	BUR012 [B,H,W]	BUR11 [B,H,W]	BUR10 [B,H,W]	BUR09 [B,H,W]
	00000000	00000000	00000000	00000000
0x80C	BUR16 [B,H,W]	BUR15 [B,H,W]	BUR14 [B,H,W]	BUR13 [B,H,W]
	00000000	00000000	00000000	00000000
0x810 – 0xEFC	-	-	-	-

1.23 USB Clock

USB Clock Base_Address : 0x4003_6000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	UCCR [B,H,W]
				-000 0000
0x004	-	-	-	UPCR [B,H,W]
				---- --00
0x008	-	-	-	UPCR2 [B,H,W]
				---- -000
0x00C	-	-	-	UPCR3 [B,H,W]
				---0 0000
0x010	-	-	-	UPCR4 [B,H,W]
				-011 1011
0x014	-	-	-	UP_STR [B,H,W]
				---- ---0
0x018	-	-	-	UPINT_ENR [B,H,W]
				---- ---0
0x01C	-	-	-	UPINT_CLR [B,H,W]
				---- ---0
0x020	-	-	-	UPINT_STR [B,H,W]
				---- ---0
0x024	-	-	-	UPCR5 [B,H,W]
				---- 0001
0x028	-	-	-	UPCR6 [B,H,W]
				---- 0010
0x02C	-	-	-	UP_CR7 [B,H,W]
				---- ---0
0x030	-	-	-	USBEN0 [B,H,W]
				---- -100
0x034	-	-	-	USBEN1 [B,H,W]
				---- -100
0x038 – 0xFFC	-	-	-	-

1.24 MFS

MFS ch.0 Base_Address : 0x4003_8000

MFS ch.1 Base_Address : 0x4003_8100

MFS ch.2 Base_Address : 0x4003_8200

MFS ch.3 Base_Address : 0x4003_8300

MFS ch.4 Base_Address : 0x4003_8400

MFS ch.5 Base_Address : 0x4003_8500

MFS ch.6 Base_Address : 0x4003_8600

MFS ch.7 Base_Address : 0x4003_8700

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	SCR/IBCR[B,H,W]	SMR[B,H,W]
			0–00000	000-00-0
0x004	-	-	SSR[B,H,W]	ESCR/IBSR[B,H,W]
			0-000011	00000000
0x008	RDR/TDR[H,W]			
	00000000 00000000 00000000 00000000			
0x00C	-	-	BGR1[B,H,W]	BGR0[B,H,W]
			00000000	00000000
0x010	-	-	ISMK[B,H,W]	ISBA[B,H,W]
			--------	--------
0x014	-	-	FCR1[B,H,W]	FCR0[B,H,W]
			---00100	-0000000
0x018	-	-	FBYTE2[B,H,W]	FBYTE1[B,H,W]
			00000000	00000000
0x01C	-	-	SCSTR1/ EIBCR[B,H,W]	SCSTR0[B,H,W]
			00000000	00000000
0x020	-	-	SCSTR3[B,H,W]	SCSTR2[B,H,W]
			00000000	00000000
0x024	-	-	SACSR[B,H,W]	
			--000–0 00-00000	
0x028	-	-	STMR[B,H,W]	
			00000000 00000000	
0x02C	-	-	STMCR[B,H,W]	
			00000000 00000000	

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x030	-	-	SCSCR[B,H,W]	
			00000000 00100000	
0x034	-	-	SCSFR1[B,H,W] 10000000	SCSFR0[B,H,W] 10000000
0x038	-	-	-	SCSFR2[B,H,W] 10000000
0x03C	-	-	TBYTE1[B,H,W]	TBYTE0[B,H,W]
			00000000	00000000
0x040	-	-	TBYTE3[B,H,W] 00000000	TBYTE2[B,H,W] 00000000
0x044	-	-	FTICR2[B,H,W] 00000000	FTICR1[B,H,W] 00000000
0x048 – 0x0FC	-	-	-	-

Note:

- *RDR/TDR register's higher 16 bits can be accessed by word operation in MFS-I^{2}S mode.*

1.25 CRC

CRC Base_Address : 0x4003_9000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	CRCCR[B,H,W]
				-0000000
0x004	CRCINIT[B,H,W]			
	11111111 11111111 11111111 11111111			
0x008	CRCIN[B,H,W]			
	00000000 00000000 00000000 00000000			
0x00C	CRCR[B,H,W]			
	11111111 11111111 11111111 11111111			

1.26 Watch Counter

Watch Counter Base_Address : 0x4003_A000

Base_Address	Register			
+ Address	**+3**	**+2**	**+1**	**+0**
0x000	-	WCCR[B,H,W]	WCRL[B,H,W]	WCRD[B,H,W]
		00–0000	--000000	--000000
0x004 – 0x00C	-	-	-	-
0x010	-	-	CLK_SEL[B,H,W]	
			-----000 ------00	
0x014	-	-	-	CLK_EN[B,H,W]
				------00
0x018 – 0xFFC	-	-	-	-

1.27 RTC

RTC Base_Address : 0x4003_B000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x100	-	-	-	WTCR10[B,H,W] 00000000
0x104	-	-	-	WTCR11[B,H,W] ---00000
0x108	-	-	-	WTCR12[B,H,W] 00000000
0x10C	-	-	-	WTCR13[B,H,W] 00000000
0x110	-	-	-	WTCR20[B,H,W] --000000
0x114	-	-	-	WTCR21[B,H,W] -----000
0x118	-	-	-	*
0x11C	-	-	-	WTSR[B,H,W] -0000000
0x120	-	-	-	WTMIR[B,H,W] -0000000
0x124	-	-	-	WTHR[B,H,W] --000000
0x128	-	-	-	WTDR[B,H,W] --000000
0x12C	-	-	-	WTDW[B,H,W] -----000
0x130	-	-	-	WTMOR[B,H,W] ---00000
0x134	-	-	-	WTYR[B,H,W] 00000000
0x138	-	-	-	ALMIR[B,H,W] -0000000
0x13C	-	-	-	ALHR[B,H,W] --000000
0x140	-	-	-	ALDR[B,H,W] --000000
0x144	-	-	-	ALMOR[B,H,W] ---00000
0x148	-	-	-	ALYR[B,H,W] 00000000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x14C	-	-	-	WTTR0[B,H,W] 00000000
0x150	-	-	-	WTTR1[B,H,W] 00000000
0x154	-	-	-	WTTR2[B,H,W] ------00
0x158	-	-	-	WTCAL0[B,H,W] 00000000
0x15C	-	-	-	WTCAL1[B,H,W] ------00
0x160	-	-	-	WTCALEN[B,H,W] -------0
0x164	-	-	-	WTDIV[B,H,W] ----0000
0x168	-	-	-	WTDIVEN[B,H,W] ------00
0x16C	-	-	-	WTCALPRD[B,H,W] --010011
0x170	-	-	-	WTCOSEL[B,H,W] -------0
0x174	-	-	-	VB_CLKDIV[B,H,W] 00000111
0x178	-	-	-	WTOSCCNT[B,H,W] ------01
0x17C	-	-	-	CCS[B,H,W] 11001110
0x180	-	-	-	CCB[B,H,W] 11001110
0x184	-	-	-	*
0x188	-	-	-	BOOST[B,H,W] ------11
0x18C	-	-	-	EWKUP[B,H,W] -------0
0x190	-	-	-	VDET[B,H,W] 00------
0x194	-	-	-	*
0x198	-	-	-	HIBRST[B,H,W] -------0
0x19C	-	-	-	VBPFR[B,H,W] --011100
0x1A0	-	-	-	VBPCR[B,H,W] ----0000
0x1A4	-	-	-	VBDDR[B,H,W] ----XXXX

Base_Address + Address	Register			
	+3	+2	+1	+0
0x1A8	-	-	-	VBDIR[B,H,W] ----0000
0x1AC	-	-	-	VBDOR[B,H,W] ----1111
0x0B0	-	-	-	VBPZR[B,H,W] ------11
0x1B4-1FF	-	-	-	-
0x200	BREG03[B,H,W] 00000000	BREG02[B,H,W] 00000000	BREG01[B,H,W] 00000000	BREG00[B,H,W] 00000000
0x204	BREG07[B,H,W] 00000000	BREG06[B,H,W] 00000000	BREG05[B,H,W] 00000000	BREG04[B,H,W] 00000000
0x208	BREG0B[B,H,W] 00000000	BREG0A[B,H,W] 00000000	BREG09[B,H,W] 00000000	BREG08[B,H,W] 00000000
0x20C	BREG0F[B,H,W] 00000000	BREG0E[B,H,W] 00000000	BREG0D[B,H,W] 00000000	BREG0C[B,H,W] 00000000
0x210	BREG13[B,H,W] 00000000	BREG12[B,H,W] 00000000	BREG11[B,H,W] 00000000	BREG10[B,H,W] 00000000
0x214	BREG17[B,H,W] 00000000	BREG16[B,H,W] 00000000	BREG15[B,H,W] 00000000	BREG14[B,H,W] 00000000
0x218	BREG1B[B,H,W] 00000000	BREG1A[B,H,W] 00000000	BREG19[B,H,W] 00000000	BREG18[B,H,W] 00000000
0x21C	BREG1F[B,H,W] 00000000	BREG1E[B,H,W] 00000000	BREG1D[B,H,W] 00000000	BREG1C[B,H,W] 00000000
0x220	BREG23[B,H,W] 00000000	BREG22[B,H,W] 00000000	BREG21[B,H,W] 00000000	BREG20[B,H,W] 00000000
0x224	BREG27[B,H,W] 00000000	BREG26[B,H,W] 00000000	BREG25[B,H,W] 00000000	BREG24[B,H,W] 00000000
0x228	BREG2B[B,H,W] 00000000	BREG2A[B,H,W] 00000000	BREG29[B,H,W] 00000000	BREG28[B,H,W] 00000000
0x22C	BREG2F[B,H,W] 00000000	BREG2E[B,H,W] 00000000	BREG2D[B,H,W] 00000000	BREG2C[B,H,W] 00000000
0x230	BREG33[B,H,W] 00000000	BREG32[B,H,W] 00000000	BREG31[B,H,W] 00000000	BREG30[B,H,W] 00000000
0x234	BREG37[B,H,W] 00000000	BREG36[B,H,W] 00000000	BREG35[B,H,W] 00000000	BREG34[B,H,W] 00000000
0x238	BREG3B[B,H,W] 00000000	BREG3A[B,H,W] 00000000	BREG39[B,H,W] 00000000	BREG38[B,H,W] 00000000
0x23C	BREG3F[B,H,W] 00000000	BREG3E[B,H,W] 00000000	BREG3D[B,H,W] 00000000	BREG3C[B,H,W] 00000000
0x240	BREG43[B,H,W] 00000000	BREG42[B,H,W] 00000000	BREG41[B,H,W] 00000000	BREG40[B,H,W] 00000000
0x244	BREG47[B,H,W] 00000000	BREG46[B,H,W] 00000000	BREG45[B,H,W] 00000000	BREG44[B,H,W] 00000000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x248	BREG4B[B,H,W] 00000000	BREG4A[B,H,W] 00000000	BREG49[B,H,W] 00000000	BREG48[B,H,W] 00000000
0x24C	BREG4F[B,H,W] 00000000	BREG4E[B,H,W] 00000000	BREG4D[B,H,W] 00000000	BREG4C[B,H,W] 00000000
0x250	BREG53[B,H,W] 00000000	BREG52[B,H,W] 00000000	BREG51[B,H,W] 00000000	BREG50[B,H,W] 00000000
0x254	BREG57[B,H,W] 00000000	BREG56[B,H,W] 00000000	BREG55[B,H,W] 00000000	BREG54[B,H,W] 00000000
0x258	BREG5B[B,H,W] 00000000	BREG5A[B,H,W] 00000000	BREG59[B,H,W] 00000000	BREG58[B,H,W] 00000000
0x25C	BREG5F[B,H,W] 00000000	BREG5E[B,H,W] 00000000	BREG5D[B,H,W] 00000000	BREG5C[B,H,W] 00000000
0x260	BREG63[B,H,W] 00000000	BREG62[B,H,W] 00000000	BREG61[B,H,W] 00000000	BREG60[B,H,W] 00000000
0x264	BREG67[B,H,W] 00000000	BREG66[B,H,W] 00000000	BREG65[B,H,W] 00000000	BREG64[B,H,W] 00000000
0x268	BREG6B[B,H,W] 00000000	BREG6A[B,H,W] 00000000	BREG69[B,H,W] 00000000	BREG68[B,H,W] 00000000
0x26C	BREG6F[B,H,W] 00000000	BREG6E[B,H,W] 00000000	BREG6D[B,H,W] 00000000	BREG6C[B,H,W] 00000000
0x270	BREG73[B,H,W] 00000000	BREG72[B,H,W] 00000000	BREG71[B,H,W] 00000000	BREG70[B,H,W] 00000000
0x274	BREG77[B,H,W] 00000000	BREG76[B,H,W] 00000000	BREG75[B,H,W] 00000000	BREG74[B,H,W] 00000000
0x278	BREG7B[B,H,W] 00000000	BREG7A[B,H,W] 00000000	BREG79[B,H,W] 00000000	BREG78[B,H,W] 00000000
0x27C	BREG7F[B,H,W] 00000000	BREG7E[B,H,W] 00000000	BREG7D[B,H,W] 00000000	BREG7C[B,H,W] 00000000
0x280-0xFFC	-	-	-	-

1.28 Low-speed CR Prescaler

Low-speed CR Prescaler Base_Address : 0x4003_C000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	LCR_PRSLD[B,H,W]
				--000000
0x000 – 0x0FC	-	-	-	-

1.29 Peripheral Clock Gating

Peripheral Clock Gating Base_Address : 0x4003_C100

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	CKEN0[B,H,W]			
	---1–11 ----1111 11111111 11111111			
0x004	MRST0[B,H,W]			
	------00 ----0000 00000000 00000000			
0x008 – 0x00C	-	-	-	-
0x010	CKEN1[B,H,W]			
	-------- ----1111 ----1111 ----1111			
0x014	MRST1[B,H,W]			
	-------- ----0000 ----0000 ----0000			
0x018 – 0x01C	-	-	-	-
0x020	CKEN2[B,H,W]			
	-------- ---1-1-1 1111-1-- --00–00			
0x024	MRST2[B,H,W]			
	-------- ---0-0-0 0000-0-- --00–00			
0x028 – 0x0FC	-	-	-	-

1.30 Smart Card I/F

Smart Card I/F ch.0Base_Address : 0x4003_C900

Smart Card I/F ch.1Base_Address : 0x4003_C980

Base_Address + Address	Register			
	+3	+2	+1	+0
0x00	-	-	GLOBALCONTROL1[H,W] -0001000 00000000	
0x04	-	-	STATUS[H,W] --000000 00000001	
0x08	-	-	PORTCONTROL[H,W] 0000–00 00-0-0-0	
0x0C	-	-	DATA[H,W] -------0 00000000	
0x10	-	-	CARDCLOCK [H,W] 00000000 00101000	
0x14	-	-	BAUDRATE[H,W] 0000001 01110100	
0x18	-	-	GUARDTIMER[H,W] -------- 00000000	
0x1C	-	-	IDLETIMER[H,W] 00000000 00000000	
0x20	-	-	GLOBALCONTROL2[H,W] -------- ----1-00	
0x24	-	-	DATA_FIFO[H,W] -------0 00000000	
0x28	-	-	FIFO_LEVEL_READ[H,W] 00000000 00000000	
0x2C	-	-	FIFO_LEVEL_WRITE[H,W] 00000000 00000000	
0x30	-	-	FIFO_MODE[H,W] 00000000 ----0000	
0x34	-	-	FIFO_CLEAR_MSB_WRITE[H,W] -------- -------0	
0x38	-	-	FIFO_CLEAR_MSB_ READ[H,W] -------- -------0	
0x3C	-	-	-	-
0x40	-	-	IRQ_STATUS[H,W] -------- 00000000	
0x44- 0x7C	-	-	-	-

1.31 MFSI2S

MFSI2S ch.5 Base_Address : 0x4003_CA00

MFSI2S ch.6 Base_Address : 0x4003_CA80

Base_Address	Register			
+Address	+3	+2	+1	+0
0x00	-		CNTLREG [H,W] -------- -------- -----000 00000001	
0x04	-		I2SCLK [H,W] -------- -------- 000----- 00000000	
0x08	-		I2SST [B] ------00	I2SRST[B] 00000000

1.32 High Resilience

High Resilience Base_Address : 0x4003_E000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	RTR_CTL3 [B,H,W]	RTR_CTL2 [B,H,W]	RTR_CTL1 [B,H,W]	RTR_CTL0 [B,H,W]
	000- 000-	000- ----	---- ----	1111 1111
0x004	RTR_RTS3 [B,H,W]	RTR_RTS2 [B,H,W]	RTR_RTS1 [B,H,W]	RTR_RTS0 [B,H,W]
	1111 1111	1111 1111	1111 1111	1111 1111
0x008	RTR_TGS3 [B,H,W]	RTR_TGS2 [B,H,W]	RTR_TGS1 [B,H,W]	RTR_TGS0 [B,H,W]
	1111 1111	1111 1111	1111 1111	1111 1111
0x00C	RTR_STR3 [B,H,W]	RTR_STR2 [B,H,W]	RTR_STR1 [B,H,W]	RTR_STR0 [B,H,W]
	00-- ----	---- ----	00-- ----	---- ----
0x010	RTR_RLR [W]			
	00000000 00000000 00000000 00000000			
0x014	RTR_CT23 [B,H,W]	RTR_CT22 [B,H,W]	RTR_CT21 [B,H,W]	RTR_CT20 [B,H,W]
	0000 0000	0000 0000	0000 0000	---0 ---0
0x018	RTR_REV [B,H,W]			
	00000000 00010101 00000001 00000000			
0x01C – 0xFFC	-	-	-	-

1.33 USB

USB ch.0 Base_Address : 0x4004_0000

USB ch.1 Base_Address : 0x4005_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x2100	-	-	HCNT1[B,H,W] -----001	HCNT0[B,H,W] 00000000
0x2104	-	-	HERR[B,H,W] 00000011	HIRQ[B,H,W] 0-000000
0x2108	-	-	HFCOMP[B,H,W] 00000000	HSTATE[B,H,W] --010010
0x210C	-	-	HRTIMER(1/0)[B,H,W] 00000000 00000000	
0x2110	-	-	HADR[B,H,W] -0000000	HRTIMER(2)[B,H,W] ------00
0x2114	-	-	HEOF(1/0)[B,H,W] --000000 00000000	
0x2118	-	-	HFRAME(1/0)[B,H,W] -----000 00000000	
0x211C	-	-	-	HTOKEN[B,H,W] 00000000
0x2120	-	-	UDCC[B,H,W] -------- 10100-00	
0x2124	-	-	EP0C[H,W] ------0- -1000000	
0x2128	-	-	EP1C[H,W] 01100001 00000000	
0x212C	-	-	EP2C[H,W] 0110000- -1000000	
0x2130	-	-	EP3C[H,W] 0110000- -1000000	
0x2134	-	-	EP4C[H,W] 0110000- -1000000	
0x2138	-	-	EP5C[H,W] 0110000- -1000000	
0x213C	-	-	TMSP[H,W] -----000 00000000	
0x2140	-	-	UDCIE[B,H,W] --000000	UDCS[B,H,W] --000000
0x2144	-	-	EP0IS[H,W] 10---1-- --------	
0x2148	-	-	EP0OS[H,W] 100–00- -XXXXXXX	

Base_Address + Address	Register			
	+3	+2	+1	+0
0x214C	-	-	EP1S[H,W] 100-000X XXXXXXXX	
0x2150	-	-	EP2S[H,W] 100-000- -XXXXXXX	
0x2154	-	-	EP3S[H,W] 100-000- -XXXXXXX	
0x2158	-	-	EP4S[H,W] 100-000- -XXXXXXX	
0x215C	-	-	EP5S[H,W] 100-000- -XXXXXXX	
0x2160	-	-	EP0DTH[B,H,W] XXXXXXXX	EP0DTL[B,H,W] XXXXXXXX
0x2164	-	-	EP1DTH[B,H,W] XXXXXXXX	EP1DTL[B,H,W] XXXXXXXX
0x2168	-	-	EP2DTH[B,H,W] XXXXXXXX	EP2DTL[B,H,W] XXXXXXXX
0x216C	-	-	EP3DTH[B,H,W] XXXXXXXX	EP3DTL[B,H,W] XXXXXXXX
0x2170	-	-	EP4DTH[B,H,W] XXXXXXXX	EP4DTL[B,H,W] XXXXXXXX
0x2174	-	-	EP5DTH[B,H,W] XXXXXXXX	EP5DTL[B,H,W] XXXXXXXX
0x2178 – 0x217C	-	-	-	-

1.34 DSTC

DSTC Base_Address : 0x4006_1000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	DESTP[B,H,W] 00000000 00000000 00000000 00000000			
0x004	HWDESP[B,H,W] 00XXXXXX XXXXXX00 00000000 00000000			
0x008	SWTR[H] 00000000 00000000		CFG[B] 01000000	CMD[B] 00000001
0x00C	MONERS[B,H,W] 00XXXXXX XXXXXX00 XXXXXXXX XXX00000			
0x010	DREQENB[31:0] [B,H,W] 00000000 00000000 00000000 00000000			
0x014	DREQENB[63:32] [B,H,W] 00000000 00000000 00000000 00000000			
0x018-0x02C	-			
0x030	HWINT[31:0] [B,H,W] 00000000 00000000 00000000 00000000			
0x034	HWINT[63:32] [B,H,W] 00000000 00000000 00000000 00000000			
0x038-0x04C	-			
0x050	HWINTCLR[31:0] [B,H,W] 00000000 00000000 00000000 00000000			
0x054	HWINTCLR[63:32] [B,H,W] 00000000 00000000 00000000 00000000			
0x058-0x06C	-			
0x070	DQMSK[31:0] [B,H,W] 00000000 00000000 00000000 00000000			
0x074	DQMSK[63:32] [B,H,W] 00000000 00000000 00000000 00000000			
0x078-0x08C	-			
0x090	DQMSKCLR[31:0] [B,H,W] 00000000 00000000 00000000 00000000			
0x094	DQMSKCLR[63:32] [B,H,W] 00000000 00000000 00000000 00000000			
0x098-0xFFC	-			

1.35 MTB_DWT

MTB_DWT Base_Address : 0xF000_1000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	CMP_ADDR_START[B,H,W]			
	00000000 00000000 00000000 00000000			
0x004	CMP_DATA_START[B,H,W]			
	00000000 00000000 00000000 00000000			
0x008	CMP_MASK_START[B,H,W]			
	00000000 00000000 00000000 00000000			
0x00C	-	-	-	-
0x010	CMP_ADDR_STOP[B,H,W]			
	00000000 00000000 00000000 00000000			
0x014	CMP_DATA_STOP[B,H,W]			
	00000000 00000000 00000000 00000000			
0x018	CMP_MASK_STOP[B,H,W]			
	00000000 00000000 00000000 00000000			
0x01C	-	-	-	-
0x020	-	-	-	FCT[B,H,W]
				00000000
0x024 – 0xFCC	-	-	-	-
0xFD0	PID4[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFD4	PID5[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFD8	PID6[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFDC	PID7[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFE0	PID0[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFE4	PID1[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFE8	PID2[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFEC	PID3[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFF0	CID0[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFF4	CID1[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFF8	CID2[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0xFFC	CID3[B,H,W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			

1.36 Fast GPIO

Fast GPIO Base_Address : 0xF800_0000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	FPDIR0[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x004	-	-	FPDIR1[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x008	-	-	FPDIR2[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x00C	-	-	FPDIR3[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x010	-	-	FPDIR4[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x014	-	-	FPDIR5[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x018	-	-	FPDIR6[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x01C	-	-	FPDIR7[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x020	-	-	FPDIR8[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x024	-	-	FPDIR9[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x028	-	-	FPDIRA[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x02C	-	-	FPDIRB[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x030	-	-	FPDIRC[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x034	-	-	FPDIRD[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x038	-	-	FPDIRE[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x03C	-	-	FPDIRF[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x040	-	-	FPDOR0[B,H,W]	
			00000000 00000000	
0x044	-	-	FPDOR1[B,H,W]	
			00000000 00000000	

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x048	-	-	FPDOR2[B,H,W]	
			00000000 00000000	
0x04C	-	-	FPDOR3[B,H,W]	
			00000000 00000000	
0x050	-	-	FPDOR4[B,H,W]	
			00000000 00000000	
0x054	-	-	FPDOR5[B,H,W]	
			00000000 00000000	
0x058	-	-	FPDOR6[B,H,W]	
			00000000 00000000	
0x05C	-	-	FPDOR7[B,H,W]	
			00000000 00000000	
0x060	-	-	FPDOR8[B,H,W]	
			00000000 00000000	
0x064	-	-	FPDOR9[B,H,W]	
			00000000 00000000	
0x068	-	-	FPDORA[B,H,W]	
			00000000 00000000	
0x06C	-	-	FPDORB[B,H,W]	
			00000000 00000000	
0x070	-	-	FPDORC[B,H,W]	
			00000000 00000000	
0x074	-	-	FPDORD[B,H,W]	
			00000000 00000000	
0x078	-	-	FPDORE[B,H,W]	
			00000000 00000000	
0x07C	-	-	FPDORF[B,H,W]	
			00000000 00000000	
0x080	-	-	-	M_FPDIR0[B,H,W]
				XXXXXXXX
0x084	-	-	-	M_FPDIR1[B,H,W]
				XXXXXXXX
0x088	-	-	-	M_FPDIR2[B,H,W]
				XXXXXXXX
0x08C	-	-	-	M_FPDIR3[B,H,W]
				XXXXXXXX
0x090	-	-	-	M_FPDIR4[B,H,W]
				XXXXXXXX
0x094	-	-	-	M_FPDIR5[B,H,W]
				XXXXXXXX

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x098	-	-	-	M_FPDIR6[B,H,W]
				XXXXXXXX
0x09C	-	-	-	M_FPDIR7[B,H,W]
				XXXXXXXX
0x0A0	-	-	-	M_FPDIR8[B,H,W]
				XXXXXXXX
0x0A4	-	-	-	M_FPDIR9[B,H,W]
				XXXXXXXX
0x0A8	-	-	-	M_FPDIRA[B,H,W]
				XXXXXXXX
0x0AC	-	-	-	M_FPDIRB[B,H,W]
				XXXXXXXX
0x0B0	-	-	-	M_FPDIRC[B,H,W]
				XXXXXXXX
0x0B4	-	-	-	M_FPDIRD[B,H,W]
				XXXXXXXX
0x0B8	-	-	-	M_FPDIRE[B,H,W]
				XXXXXXXX
0x0BC	-	-	-	M_FPDIRF[B,H,W]
				XXXXXXXX
0x0C0	-	-	-	M_FPDOR0[B,H,W]
				00000000
0x0C4	-	-	-	M_FPDOR1[B,H,W]
				00000000
0x0C8	-	-	-	M_FPDOR2[B,H,W]
				00000000
0x0CC	-	-	-	M_FPDOR3[B,H,W]
				00000000
0x0D0	-	-	-	M_FPDOR4[B,H,W]
				00000000
0x0D4	-	-	-	M_FPDOR5[B,H,W]
				00000000
0x0D8	-	-	-	M_FPDOR6[B,H,W]
				00000000
0x0DC	-	-	-	M_FPDOR7[B,H,W]
				00000000
0x0E0	-	-	-	M_FPDOR8[B,H,W]
				00000000
0x0E4	-	-	-	M_FPDOR9[B,H,W]
				00000000
0x0E8	-	-	-	M_FPDORA[B,H,W]
				00000000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x0EC	-	-	-	M_FPDORB[B,H,W]
				00000000
0x0F0	-	-	-	M_FPDORC[B,H,W]
				00000000
0x0F4	-	-	-	M_FPDORD[B,H,W]
				00000000
0x0F8	-	-	-	M_FPDORE[B,H,W]
				00000000
0x0FC	-	-	-	M_FPDORF[B,H,W]
				00000000
0x100 – 0xFFC	-	-	-	-

D. Register Map (TYPE3-M0+)

This chapter shows the register map.

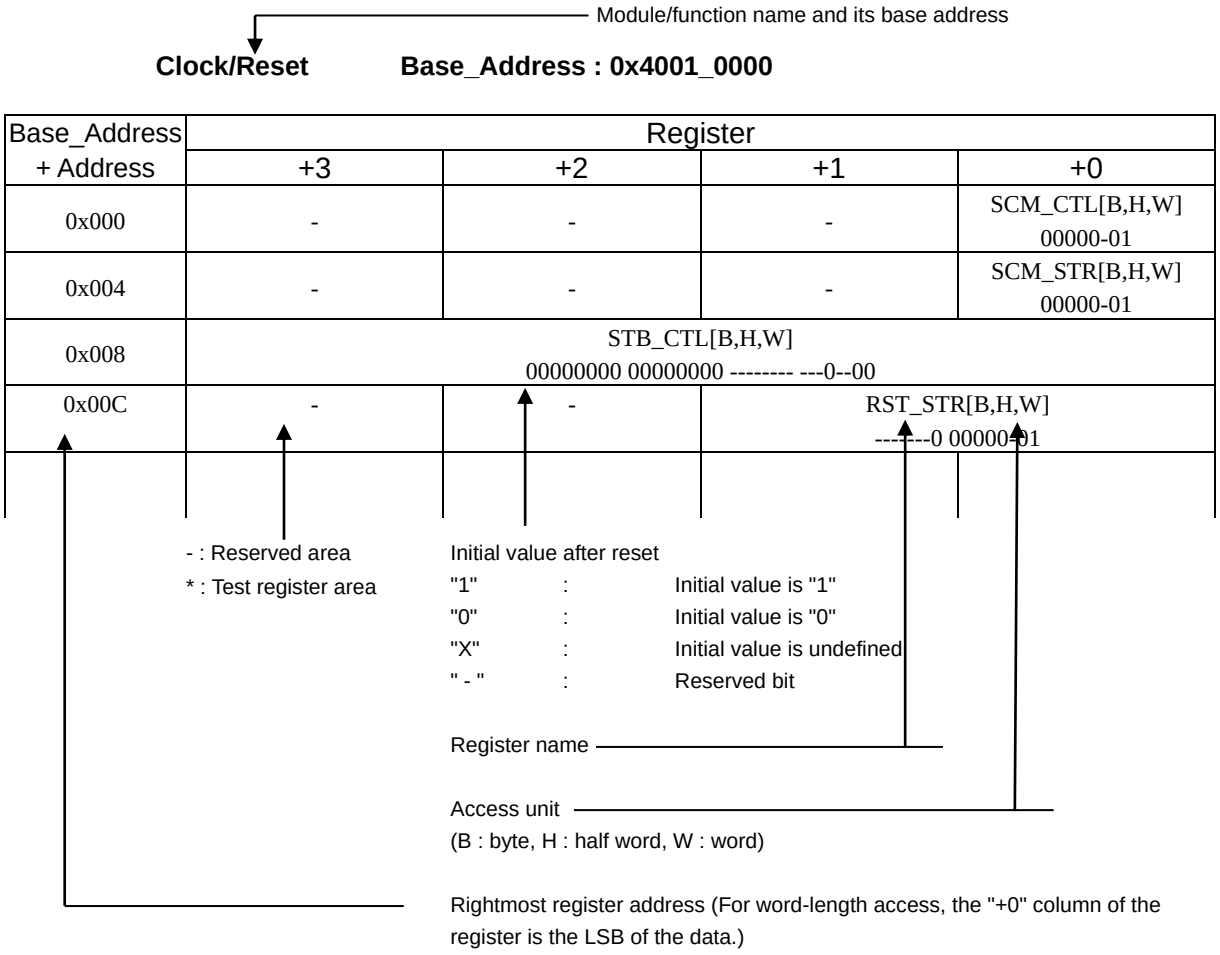
1. Register Map

CODE: 9AFREGMAP-E03.0

1. Register Map

Register map is shown on the table every module/function.

[How to Read the Each Table]



Notes:

- The register table is represented in the little-endian.
- When performing a data access, the addresses should be as below according to the access size.
  - Word access : Address should be multiples of 4 (least significant 2 bits should be "0x00")
  - Half word access : Address should be multiples of 2 (least significant bit should be "0x0")
  - Byte access : -
- Do not access the test register area.
- Do not access the area that is not written in the register table.
- When the register is accessed by larger unit than register size, for the reserved area to access at the same time, the read value is undefined, and writing is invalid.

1.1 Flash I/F

Flash I/F Base_Address : 0x4000_0000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	-
0x004	FRWTR[B,H,W]			
	-------- -------- -------- -----011			
0x008	FSTR[B,H,W]			
	-------- -------- -------- --00000X			
0x00C	-	-	-	-
0x010	FSYNDN[B,H,W]			
	-------- -------- -------- ----0001			
0x014 - 0x01C	-	-	-	-
0x020	FICR[B,H,W]			
	-------- -------- -------- ------00			
0x024	FISR[B,H,W]			
	-------- -------- -------- ------00			
0x028	FICLR[B,H,W]			
	-------- -------- -------- ------00			
0x02C - 0x0FC	-	-	-	-
0x100	CRTRMM[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x104 - 0x1FC	-	-	-	-

Note:

- *For details of Flash I/F registers, refer to "FLASH PROGRAMMING MANUAL" of the product used.*

1.2 Unique ID

Unique ID Base_Address : 0x4000_0200

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	UIDR0[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXX----			
0x004	UIDR1[W]			
	-------- -------- ---XXXXX XXXXXXXX			
0x008 – 0xDFC	-	-	-	-

1.3 Clock/Reset

Clock/Reset Base_Address : 0x4001_0000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	SCM_CTL[W]
				00000-01
0x004	-	-	-	SCM_STR[W]
				00000-01
0x008	STB_CTL[W]			
	00000000 00000000 -------- ---0-000			
0x00C	-	-	RST_STR[W]	
			-------0 00000-01	
0x010	-	-	-	BSC_PSR[W]
				-----000
0x014	-	-	-	APBC0_PSR[W]
				------00
0x018	-	-	-	APBC1_PSR[W]
				1--0--00
0x01C	-	-	-	-
0x020	-	-	-	SWC_PSR[W]
				X-----00
0x024 - 0x02C	-	-	-	-
0x030	-	-	-	CSW_TMR[W]
				00000000
0x034	-	-	-	PSW_TMR[W]
				---0-000
0x038	-	-	-	PLL_CTL1[W]
				00000000
0x03C	-	-	-	PLL_CTL2[W]
				--000000
0x040	-	-	CSV_CTL[W]	
			-111--00 ------11	
0x044	-	-	-	CSV_STR[W]
				------00
0x048	-	-	FCSWH_CTL[W]	
			11111111 11111111	
0x04C	-	-	FCSWL_CTL[W]	
			00000000 00000000	
0x050	-	-	FCSWD_STR[W]	
			00000000 00000000	
0x054	-	-	-	DBWDT_CTL[W]
				0-0-----

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x058	-	-	-	*
0x05C	-	-	-	-
0x060	-	-	-	INT_ENR[W]
				--0--000
0x064	-	-	-	INT_STR[W]
				--0--000
0x068	-	-	-	INT_CLR[W]
				--0--000
0x06C - 0xFFC	-	-	-	-

1.4 HW WDT

HW WDT Base_Address : 0x4001_1000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	WDG_LDR[W]			
	00000000 00000000 11111111 11111111			
0x004	WDG_VLR[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x008	-	-	-	WDG_CTL[W]
				------11
0x00C	-	-	-	WDG_ICL[W]
				XXXXXXXX
0x010	-	-	-	WDG_RIS[W]
				-------0
0x014 - 0xBFC	-	-	-	-
0xC00	WDG_LCK[W]			
	00000000 00000000 00000000 00000001			
0xC04 - 0xFFC	-	-	-	-

1.5 SW WDT

SW WDT Base_Address : 0x4001_2000

Base_Address	Register			
+ Address	**+3**	**+2**	**+1**	**+0**
0x000	WdogLoad[W]			
	11111111 11111111 11111111 11111111			
0x004	WdogValue[W]			
	11111111 11111111 11111111 11111111			
0x008	-	-	-	WdogControl[W]
				---00000
0x00C	WdogIntClr[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x010	-	-	-	WdogRIS[W]
				-------0
0x014	*			
0x018	-	-	-	WdogSPMC[W]
				-------0
0x01C - 0xBFC	-	-	-	-
0xC00	WdogLock[W]			
	00000000 00000000 00000000 00000000			
0xC04 - 0xDFC	-	-	-	-
0xF00	*			
0xF08 - 0xFDF	-	-	-	-
0xFE0 - 0xFFC	*			

1.6 Dual Timer

Dual Timer Base_Address : 0x4001_5000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	Timer1Load[W]			
	00000000 00000000 00000000 00000000			
0x004	Timer1Value[W]			
	11111111 11111111 11111111 11111111			
0x008	Timer1Control[W]			
	-------- -------- -------- 00100000			
0x00C	Timer1IntClr[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x010	Timer1RIS[W]			
	-------- -------- -------- -------0			
0x014	Timer1MIS[W]			
	-------- -------- -------- -------0			
0x018	Timer1BGLoad[W]			
	00000000 00000000 00000000 00000000			
0x020	Timer2Load[W]			
	00000000 00000000 00000000 00000000			
0x024	Timer2Value[W]			
	11111111 11111111 11111111 11111111			
0x028	Timer2Control[W]			
	-------- -------- -------- 00100000			
0x02C	Timer2IntClr[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x030	Timer2RIS[W]			
	-------- -------- -------- -------0			
0x034	Timer2MIS[W]			
	-------- -------- -------- -------0			
0x038	Timer2BGLoad[W]			
	00000000 00000000 00000000 00000000			
0x040 - 0xFFC	-	-	-	-

1.7 Base Timer

Base Timer ch.0 Base Address : 0x4002_5000

Base Timer ch.1 Base Address : 0x4002_5040

Base Timer ch.2 Base Address : 0x4002_5080

Base Timer ch.3 Base Address : 0x4002_50C0

Base Timer ch.4 Base Address : 0x4002_5200

Base Timer ch.5 Base Address : 0x4002_5240

Base Timer ch.6 Base Address : 0x4002_5280

Base Timer ch.7 Base Address : 0x4002_52C0

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	PCSR/PRLL[H,W]	
			XXXXXXXX XXXXXXXX	
0x004	-	-	PDUT/PRLH/DTBF[H,W]	
			XXXXXXXX XXXXXXXX	
0x008	-	-	TMR[H,W]	
			00000000 00000000	
0x00C	-	-	TMCR[B,H,W]	
			-0000000 00000000	
0x010	-	-	TMCR2[B,H,W]	STC[B,H,W]
			0-------0	0000-000
0x014 - 0x03C	-	-	-	-

1.8 IO Selector for Base Timer

IO Selector for ch.0-ch.3 (Base Timer) Base Address : 0x4002_5100

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	BTSEL0123[B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

IO Selector for ch.4-ch.7 (Base Timer) Base Address : 0x4002_5300

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	BTSEL4567[B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

Software-based Simultaneous Startup (Base Timer) Base Address : 0x4002_5F00

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000 - 0x0FB	-	-	-	-
0x0FC	-	-	BTSSSR [B,H,W] -------- XXXXXXXX	

1.9 A/DC

12-bit A/DC unit0 Base_Address : 0x4002_7000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	ADCR[B,H,W]	ADSR[B,H,W]
			000-0000	00---000
0x004	-	-	-	*
0x008	-	-	SCCR[B,H,W]	SFNS[B,H,W]
			1000-000	----0000
0x00C	SCFD[B,H,W]			
	XXXXXXXX XXXX---- ---X--XX ---XXXXX			
0x010	-	-	SCIS3[B,H,W]	SCIS2[B,H,W]
			00000000	00000000
0x014	-	-	SCIS1[B,H,W]	SCIS0[B,H,W]
			00000000	00000000
0x018	-	-	PCCR[B,H,W]	PFNS[B,H,W]
			10000000	--XX--00
0x01C	PCFD[B,H,W]			
	XXXXXXXX XXXX---- ---X-XXX ---XXXXX			
0x020	-	-	-	PCIS[B,H,W]
				00000000
0x024	CMPD[B,H,W]		-	CMPCR[B,H,W]
	00000000 00------			00000000
0x028	-	-	ADSS3[B,H,W]	ADSS2[B,H,W]
			00000000	00000000
0x02C	-	-	ADSS1[B,H,W]	ADSS0[B,H,W]
			00000000	00000000
0x030	-	-	ADST0[B,H,W]	ADST1[B,H,W]
			00010000	00010000
0x034	-	-	-	ADCT[B,H,W]
				00000111
0x038	-	-	SCTSL[B,H,W]	PRTSL[B,H,W]
			----0000	----0000
0x03C	-	-	ADCEN[B,H,W]	
			11111111 ------00	
0x040	*			
0x044	WCMRCIF[B,H,W]			
	-------- -------- -------- -------0			
0x048	WCMRCOT[B,H,W]			
	-------- -------- -------- -------0			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x04C	-	-	WCMPSR[B,H,W]	WCMPCR[B,H,W]
			00000000	001000--
0x050	WCMPDH[B,H,W]		WCMPDL[B,H,W]	
	00000000 00------		00000000 00------	
0x054 - 0x0FC	-	-	-	-

1.10 CR Trim

CR Trim Base_Address : 0x4002_E000

Base_Address	Register			
+ Address	**+3**	**+2**	**+1**	**+0**
0x000	-	-	-	MCR_PSR[B,H,W]
				-----001
0x004	-	-	MCR_FTRM[B,H,W]	
			------10 00000110	
0x008	-	-	-	MCR_TTRM[B,H,W]
				-1111111
0x00C	MCR_RLR[B,H,W]			
	00000000 00000000 00000000 00000001			
0x010 - 0x0FC	-	-	-	-

1.11 EXTI

EXTI Base_Address : 0x4003_0000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	ENIR[B,H,W]			
	00000000 00000000 00000000 00000000			
0x004	EIRR[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x008	EICL[B,H,W]			
	11111111 11111111 11111111 11111111			
0x00C	ELVR[B,H,W]			
	00000000 00000000 00000000 00000000			
0x010	ELVR1[B,H,W]			
	00000000 00000000 00000000 00000000			
0x014	-	-	NMIRR[B,H,W]	
			-------- -------0	
0x018	-	-	NMICL[B,H,W]	
			-------- -------1	
0x01C	ELVR2[B,H,W]			
	00000000 00000000 00000000 00000000			
0x020	-	-	-	NMIENR[B,H,W]
	-	-	-	-------0
0x024 – 0x0FC	-	-	-	-

1.12 INT-Req. READ

INT-Req. READ Base_Address : 0x4003_1000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000 – 0x004	-	-	-	-
0x008	VIR_OFFSET[B,H,W]			
	00000000 00000000 00000000 00000000			
0x010	-	-	-	ODDPKS[B,H,W]
				---00000
0x014 – 0x1FC	-	-	-	-
0x200	EXC02MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x204	IRQ00MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x208	IRQ01MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x20C	IRQ02MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x210	IRQ03MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x214	IRQ04MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x218	IRQ05MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x21C	IRQ06MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x220	IRQ07MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x224	IRQ08MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x228	IRQ09MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x22C	IRQ10MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x230	IRQ11MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x234	IRQ12MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x238	IRQ13MON[B,H,W]			
	00000000 00000000 00000000 00000000			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x23C	IRQ14MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x240	IRQ15MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x244	IRQ16MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x248	IRQ17MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x24C	IRQ18MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x250	IRQ19MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x254	IRQ20MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x258	IRQ21MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x25C	IRQ22MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x260	IRQ23MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x264	IRQ24MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x268	IRQ25MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x26C	IRQ26MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x270	IRQ27MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x274	IRQ28MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x278	IRQ29MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x27C	IRQ30MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x280	IRQ31MON[B,H,W]			
	00000000 00000000 00000000 00000000			
0x284 – 0xFFC	-	-	-	-

1.13 GPIO

GPIO Base_Address : 0x4003_3000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	PFR0[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 1010			
0x004	PFR1[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x008	PFR2[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x00C	PFR3[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x010	PFR4[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x014	PFR5[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x018	PFR6[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x01C	-	-	-	-
0x020	PFR8[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x024 – 0x034	-	-	-	-
0x038	PFRE[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x03C – 0x0FC	-	-	-	-
0x100	PCR0[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 1010			
0x104	PCR1[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x108	PCR2[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x10C	PCR3[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x110	PCR4[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x114	PCR5[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x118	PCR6[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x11C – 0x134	-	-	-	-

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x138	PCRE[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x13C – 0x1FC	-	-	-	-
0x200	DDR0[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x204	DDR1[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x208	DDR2[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x20C	DDR3[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x210	DDR4[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x214	DDR5[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x218	DDR6[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x21C	-	-	-	-
0x220	DDR8[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x224 – 0x234	-	-	-	-
0x238	DDRE[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x23C – 0x2FC	-	-	-	-
0x300	PDIR0[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x304	PDIR1[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x308	PDIR2[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x30C	PDIR3[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x310	PDIR4[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x314	PDIR5[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x318	PDIR6[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x31C	-	-	-	-
0x320	PDIR8[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x324 – 0x334	-	-	-	-

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x338	PDIRE[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x33C – 0x3FC	-	-	-	-
0x400	PDOR0[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x404	PDOR1[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x408	PDOR2[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x40C	PDOR3[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x410	PDOR4[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x414	PDOR5[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x418	PDOR6[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x41C	-	-	-	-
0x420	PDOR8[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x424 – 0x434	-	-	-	-
0x438	PDORE[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x43C – 0x4FC	-	-	-	-
0x500	ADE[B,H,W]			
	1111 1111 1111 1111 1111 1111 1111 1111			
0x504 – 0x57C	-	-	-	-
0x580	SPSR[B,H,W]			
	---- ---- ---- ---- ---- ---- ---0 0101			
0x584 – 0x5FC	-	-	-	-
0x600	EPFR00[B,H,W]			
	---- --00 ---- --01 ---- --0- ---- --00			
0x604 – 0x60C	-	-	-	-
0x610	EPFR04[B,H,W]			
	0000 0000 0000 0000 0000 0000 0000 0000			
0x614	EPFR05[B,H,W]			
	0000 0000 0000 0000 0000 0000 0000 0000			
0x618	EPFR06[B,H,W]			
	0000 0000 0000 0000 0000 0000 0000 0000			
0x61C	EPFR07[B,H,W]			
	0000 0000 0000 0000 0000 0000 0000 0000			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x620	EPFR08[B,H,W]			
	0000 0000 0000 0000 0000 0000 0000 0000			
0x624	EPFR09[B,H,W]			
	0000 0000 0000 0000 0000 0000 0000 0000			
0x628 – 0x654	-	-	-	-
0x658	EPFR22[B,H,W]			
	0000 0000 0000 0000 0000 0000 0000 0000			
0x65C	EPFR23[B,H,W]			
	0000 0000 0000 0000 0000 0000 0000 0000			
0x660 – 0x678	-	-	-	-
0x67C	EPFR31[B,H,W]			
	0000 0000 0000 0000 0000 0000 0000 0000			
0x680	-	-	-	-
0x684	EPFR33[B,H,W]			
	0000 0000 0000 0000 0000 0000 0000 0000			
0x688 – 0x690	-	-	-	-
0x694	EPFR37[B,H,W]			
	0000 0000 0000 0000 0000 0000 0000 0000			
0x698	EPFR38[B,H,W]			
	0000 0000 0000 0000 0000 0000 0000 0000			
0x69C – 0x6FC	-	-	-	-
0x700	-	-	-	-
0x704	PZR1[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x708	-	-	-	-
0x70C	PZR3[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x710 – 0x714	-	-	-	-
0x718	PZR6[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x71C – 0x7FC	-	-	-	-
0x800 – 0x8FC	-	-	-	-
0x900	FPOER0[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x904	FPOER1[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x908	FPOER2[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x90C	FPOER3[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x910	FPOER4[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x914	FPOER5[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x918	FPOER6[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x91C	-	-	-	-
0x920	FPOER8[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x924 – 0x934	-	-	-	-
0x938	FPOERE[B,H,W]			
	---- ---- ---- ---- 0000 0000 0000 0000			
0x93C – 0xFFC	-	-	-	-

1.14 HDMI-CEC

HDMI-CEC/Remote Control Receiver ch.0 Base_Address : 0x4003_4000

HDMI-CEC/Remote Control Receiver ch.1 Base_Address : 0x4003_4100

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x00	-	-	-	TXCTRL[B,H,W]
				000000-0
0x04	-	-	-	TXDATA[B,H,W]
				00000000
0x08	-	-	-	TXSTS[B,H,W]
				0-00---0
0x0C	-	-	-	SFREE[B,H,W]
				----0000
0x10 – 0x3F	-	-	-	-
0x40	-	-	RCCR[B,H,W]	RCST[B,H,W]
			0---0000	00000000
0x44	-	-	RCSHW[B,H,W]	RCDAHW[B,H,W]
			00000000	00000000
0x48	-	-	RCDBHW[B,H,W]	-
			00000000	
0x4C	-	-	RCADR1[B,H,W]	RCADR2[B,H,W]
			---00000	---00000
0x50	-	-	RCDTHH[B,H,W]	RCDTHL[B,H,W]
			00000000	00000000
0x54	-	-	RCDTLH[B,H,W]	RCDTLL[B,H,W]
			00000000	00000000
0x58	-	-	RCCKD[H,W]	
			---00000 00000000	
0x5C	-	-	RCRC[B,H,W]	RCRHW[B,H,W]
			---0---0	00000000
0x60	-	-	RCLE[B,H,W]	-
			00000-00	
0x64	-	-	RCLELW[B,H,W]	RCLESW[B,H,W]
			00000000	00000000
0x68 – 0xFC	-	-	-	-

1.15 LVD

LVD Base_Address : 0x4003_5000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	LVD_CTL [B,H,W]	
			10000000 00001100	
0x004	-	-	LVD_STR [B,H,W]	
			00000000 0000000-	
0x008	-	-	LVD_CLR [B,H,W]	
			00000000 10000000	
0x00C	LVD_RLR [W]			
	00000000 00000000 00000000 00000001			
0x010	-	-	LVD_STR2 [B,H,W]	
			00000000 01000000	
0x014 – 0x0FC	-	-	-	-

1.16 DS Mode

DS Mode Base_Address : 0x4003_5100

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	REG_CTL [B,H,W]
				---- -10-
0x004	-	-	-	RCK_CTL [B,H,W]
				---- --01
0x008 – 0x00C	-	-	-	-
0x010	-	-	-	MOSC_CTL [B,H,W]
				---- -10-
0x014 – 0x0FC	-	-	-	-
0x100	-	-	-	CAL_CTL [B,H,W]
				---- 0000
0x104	-	-	-	-
0x108	CAL_KEY [W]			
	00000000 00000000 00000000 00000001			
0x10C – 0x6FC	-	-	-	-
0x700	-	-	-	PMD_CTL [B,H,W]
				---- ---0
0x704	-	-	-	WRFSR [B,H,W]
				---- --00
0x708	-	-	WIFSR [B,H,W]	
			00000000 00000000	
0x70C	-	-	WIER [B,H,W]	
			00000000 00000-00	
0x710	-	-	WILVR [B,H,W]	
			-----000 00000000	
0x714	-	-	-	DSRAMR [B,H,W]
				---- --00
0x718 – 0x7FC	-	-	-	-
0x800	BUR04 [B,H,W]	BUR03 [B,H,W]	BUR02 [B,H,W]	BUR01 [B,H,W]
	00000000	00000000	00000000	00000000
0x804	BUR08 [B,H,W]	BUR07 [B,H,W]	BUR06 [B,H,W]	BUR05 [B,H,W]
	00000000	00000000	00000000	00000000
0x808	BUR012 [B,H,W]	BUR11 [B,H,W]	BUR10 [B,H,W]	BUR09 [B,H,W]
	00000000	00000000	00000000	00000000
0x80C	BUR16 [B,H,W]	BUR15 [B,H,W]	BUR14 [B,H,W]	BUR13 [B,H,W]
	00000000	00000000	00000000	00000000
0x810 – 0x8FC	-	-	-	-

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x900	WIOLC_CTL [B,H,W]			
	-------0 -------1 -------0 -------0			
0x904	-	-	-	SUBOSC_CTL[B,H,W]
				------01
0x908	-	-	-	CEC_CTL [B,H,W]
				----0000
0x90C	-	-	-	DEBUG_SW_CTL[B,H,W]
				-------1
0x910 – 0xEFC	-	-	-	-

1.17 USB Clock

USB Clock Base_Address : 0x4003_6000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	UCCR [B,H,W]
				-----000
0x004 – 0x024	-	-	-	-
0x028	-	-	-	UPCR6[B,H,W]
				----0010
0x02C	-	-	-	-
0x030	-	-	-	USBEN0[B,H,W]
				-------0
0x038 – 0x0FC	-	-	-	-

1.18 I2CSLAVE

I2CSLAVE ch.6 Base_Address : 0x4003_7980

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x00	IBSCR[B,H,W]		IBSSR[B,H,W]	
	------00 0-000000		-----001 00000000	
0x04	-	IBSDSTUPR[B,H,W]	IBSMSKR[B,H,W]	IBSADR[B,H,W]
	-	11111111	01111111	00000000
0x08	-	-	-	IBSTDR[B,H,W]
	-	-	-	11111111
0x0C	-	-	-	IBSRDR[B,H,W]
	-	-	-	11111111
0x10	-	-	IBSSCR[B,H,W]	
	-	-	-----0-- -----00-	
0x14	-	-	IBSSSR[B,H,W]	
	-	-	-------0 --------	
0x18 – 0x3F	-	-	-	-

1.19 MFS

MFS ch.0 Base_Address : 0x4003_8000

MFS ch.1 Base_Address : 0x4003_8100

MFS ch.3 Base_Address : 0x4003_8300

MFS ch.4 Base_Address : 0x4003_8400

MFS ch.6 Base_Address : 0x4003_8600

MFS ch.7 Base_Address : 0x4003_8700

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	SCR/IBCR[B,H,W]	SMR[B,H,W]
			0–00000	000-00-0
0x004	-	-	SSR[B,H,W]	ESCR/IBSR[B,H,W]
			0-000011	00000000
0x008	RDR/TDR[H,W]			
	00000000 00000000 00000000 00000000			
0x00C	-	-	BGR1[B,H,W]	BGR0[B,H,W]
			00000000	00000000
0x010	-	-	ISMK[B,H,W]	ISBA[B,H,W]
			--------	--------
0x014	-	-	FCR1[B,H,W]	FCR0[B,H,W]
			---00100	-0000000
0x018	-	-	FBYTE2[B,H,W]	FBYTE1[B,H,W]
			00000000	00000000
0x01C	-	-	SCSTR1/ EIBCR[B,H,W]	SCSTR0[B,H,W]
			00000000	00000000
0x020	-	-	SCSTR3[B,H,W]	SCSTR2[B,H,W]
			00000000	00000000
0x024	-	-	SACSR[B,H,W]	
			--000–0 00-00000	
0x028	-	-	STMR[B,H,W]	
			00000000 00000000	
0x02C	-	-	STMCR[B,H,W]	
			00000000 00000000	
0x030	-	-	SCSCR[B,H,W]	
			00000000 00100000	
0x034	-	-	SCSFR1[B,H,W] 10000000	SCSFR0[B,H,W] 10000000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x038	-	-	-	SCSFR2[B,H,W] 10000000
0x03C	-	-	TBYTE1[B,H,W] 00000000	TBYTE0[B,H,W] 00000000
0x040	-	-	TBYTE3[B,H,W] 00000000	TBYTE2[B,H,W] 00000000
0x044 – 0x0FC	-	-	-	-

Note:

- *RDR/TDR register's higher 16 bits can be accessed by word operation in I^2S mode.*

1.20 CRC

CRC Base_Address : 0x4003_9000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	CRCCR[B,H,W]
				-0000000
0x004	CRCINIT[B,H,W]			
	11111111 11111111 11111111 11111111			
0x008	CRCIN[B,H,W]			
	00000000 00000000 00000000 00000000			
0x00C	CRCR[B,H,W]			
	11111111 11111111 11111111 11111111			

1.21 Watch Counter

Watch Counter Base_Address : 0x4003_A000

Base_Address	Register			
+ Address	**+3**	**+2**	**+1**	**+0**
0x000	-	WCCR[B,H,W]	WCRL[B,H,W]	WCRD[B,H,W]
		00–0000	--000000	--000000
0x004 – 0x00C	-	-	-	-
0x010	-	-	CLK_SEL[B,H,W]	
			-----000 ------00	
0x014	-	-	-	CLK_EN[B,H,W]
				------00
0x018 – 0xFFC	-	-	-	-

1.22 RTC

RTC Base_Address : 0x4003_B000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	WTCR1[B,H,W]			
	00000000 00000000 ---00000 -00000-0			
0x004	WTCR2[B,H,W]			
	-------- -------- -----000 -------0			
0x008	WTBR[B,H,W]			
	-------- 00000000 00000000 00000000			
0x00C	WTDR[B,H,W]	WTHR[B,H,W]	WTMIR[B,H,W]	WTSR[B,H,W]
	--000000	--000000	-0000000	-0000000
0x010	-	WTYR[B,H,W]	WTMOR[B,H,W]	WTDW[B,H,W]
		00000000	---00000	-----000
0x014	ALDR[B,H,W]	ALHR[B,H,W]	ALMIR[B,H,W]	-
	--000000	--000000	-0000000	
0x018	-	ALYR[B,H,W]	ALMOR[B,H,W]	-
		00000000	---00000	
0x01C	WTTR[B,H,W]			
	-------- ------00 00000000 00000000			
0x020	-	-	WTCLKM[B,H,W]	WTCLKS[B,H,W]
			------00	-------0
0x024	-	WTCALEN[B,H,W]	WTCAL[B,H,W]	
		-------0	------00 00000000	
0x028	-	-	WTDIVEN[B,H,W]	WTDIV[B,H,W]
			------00	----0000
0x02C	-	-	-	WTCALPRD[B,H,W]
				--010011
0x030	-	-	-	WTCOSEL[B,H,W]
				-------0
0x034 – 0xFFC	-	-	-	-

1.23 Low-speed CR Prescaler

Low-speed CR Prescaler Base_Address : 0x4003_C000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	LCR_PRSLD[B,H,W]
				--000000
0x000 – 0x0FC	-	-	-	-

1.24 Peripheral Clock Gating

Peripheral Clock Gating Base_Address : 0x4003_C100

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	CKEN0[B,H,W]			
	---1---- -------1 -------- 11-11-11			
0x004	MRST0[B,H,W]			
	-------- -------0 -------- 00-00-00			
0x008 – 0x00C	-	-	-	-
0x010	CKEN1[B,H,W]			
	-------- -------- -------- ------11			
0x014	MRST1[B,H,W]			
	-------- -------- -------- ------00			
0x018 – 0x01C	-	-	-	-
0x020	CKEN2[B,H,W]			
	-------- -----1–111----- -------0			
0x024	MRST2[B,H,W]			
	-------- -----0–000----- -------0			
0x028 – 0x0FC	-	-	-	-

1.25 Smart Card I/F

Smart Card I/F ch.1 Base_Address : 0x4003_C980

Base_Address + Address	Register			
	+3	+2	+1	+0
0x00	-	-	GLOBALCONTROL1[H,W] -0001000 00000000	
0x04	-	-	STATUS[H,W] --000000 00000001	
0x08	-	-	PORTCONTROL[H,W] 0000–00 00-0-0-0	
0x0C	-	-	DATA[H,W] -------0 00000000	
0x10	-	-	CARDCLOCK [H,W] 00000000 00101000	
0x14	-	-	BAUDRATE[H,W] 0000001 01110100	
0x18	-	-	GUARDTIMER[H,W] -------- 00000000	
0x1C	-	-	IDLETIMER[H,W] 00000000 00000000	
0x20	-	-	GLOBALCONTROL2[H,W] -------- ----1-00	
0x24	-	-	DATA_FIFO[H,W] -------0 00000000	
0x28	-	-	FIFO_LEVEL_READ[H,W] 00000000 00000000	
0x2C	-	-	FIFO_LEVEL_WRITE[H,W] 00000000 00000000	
0x30	-	-	FIFO_MODE[H,W] 00000000 ----0000	
0x34	-	-	FIFO_CLEAR_MSB_WRITE[H,W] -------- -------0	
0x38	-	-	FIFO_CLEAR_MSB_ READ[H,W] -------- -------0	
0x3C	-	-	-	-
0x40	-	-	IRQ_STATUS[H,W] -------- 00000000	
0x44- 0x7C	-	-	-	-

1.26 MFSI2S

MFSI2S ch.4 Base_Address : 0x4003_CA00

MFSI2S ch.6 Base_Address : 0x4003_CA80

Base_Address + Address	Register			
	+3	+2	+1	+0
0x00	-	-	CNTLREG[B, H,W] -----0-0 -0000-01	
0x04	-	-	I2SCLK[B, H,W] 00------ 00000000	
0x08	-	-	I2SST[B,H,W] ------00	I2SRST[B,H,W] 00000000
0x0C- 0x3C	-	-	-	-

1.27 USB

USB ch.0 Base_Address : 0x4004_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x2100	-	-	HCNT1[B,H,W] -----001	HCNT0[B,H,W] 00000000
0x2104	-	-	HERR[B,H,W] 00000011	HIRQ[B,H,W] 0-000000
0x2108	-	-	HFCOMP[B,H,W] 00000000	HSTATE[B,H,W] --010010
0x210C	-	-	HRTIMER(1/0)[B,H,W] 00000000 00000000	
0x2110	-	-	HADR[B,H,W] -0000000	HRTIMER(2)[B,H,W] ------00
0x2114	-	-	HEOF(1/0)[B,H,W] --000000 00000000	
0x2118	-	-	HFRAME(1/0)[B,H,W] -----000 00000000	
0x211C	-	-	-	HTOKEN[B,H,W] 00000000
0x2120	-	-	UDCC[B,H,W] -------- 10100-00	
0x2124	-	-	EP0C[H,W] ------0- -1000000	
0x2128	-	-	EP1C[H,W] 01100001 00000000	
0x212C	-	-	EP2C[H,W] 0110000- -1000000	
0x2130	-	-	EP3C[H,W] 0110000- -1000000	
0x2134	-	-	EP4C[H,W] 0110000- -1000000	
0x2138	-	-	EP5C[H,W] 0110000- -1000000	
0x213C	-	-	TMSP[H,W] -----000 00000000	
0x2140	-	-	UDCIE[B,H,W] --000000	UDCS[B,H,W] --000000
0x2144	-	-	EP0IS[H,W] 10---1-- --------	
0x2148	-	-	EP0OS[H,W] 100–00- -XXXXXXX	

Base_Address + Address	Register			
	+3	+2	+1	+0
0x214C	-	-	EP1S[H,W] 100-000X XXXXXXXX	
0x2150	-	-	EP2S[H,W] 100-000- -XXXXXXX	
0x2154	-	-	EP3S[H,W] 100-000- -XXXXXXX	
0x2158	-	-	EP4S[H,W] 100-000- -XXXXXXX	
0x215C	-	-	EP5S[H,W] 100-000- -XXXXXXX	
0x2160	-	-	EP0DTH[B,H,W] XXXXXXXX	EP0DTL[B,H,W] XXXXXXXX
0x2164	-	-	EP1DTH[B,H,W] XXXXXXXX	EP1DTL[B,H,W] XXXXXXXX
0x2168	-	-	EP2DTH[B,H,W] XXXXXXXX	EP2DTL[B,H,W] XXXXXXXX
0x216C	-	-	EP3DTH[B,H,W] XXXXXXXX	EP3DTL[B,H,W] XXXXXXXX
0x2170	-	-	EP4DTH[B,H,W] XXXXXXXX	EP4DTL[B,H,W] XXXXXXXX
0x2174	-	-	EP5DTH[B,H,W] XXXXXXXX	EP5DTL[B,H,W] XXXXXXXX
0x2178 – 0x217C	-	-	-	-

1.28 DSTC

DSTC Base_Address : 0x4006_1000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	DESTP[B,H,W] 00000000 00000000 00000000 00000000			
0x004	HWDESP[B,H,W] 00XXXXXX XXXXXX00 00000000 00000000			
0x008	SWTR[H] 00000000 00000000		CFG[B] 01000000	CMD[B] 00000001
0x00C	MONERS[B,H,W] 00XXXXXX XXXXXX00 XXXXXXXX XXX00000			
0x010	DREQENB[31:0] [B,H,W] 00000000 00000000 00000000 00000000			
0x014	DREQENB[63:32] [B,H,W] 00000000 00000000 00000000 00000000			
0x018-0x02C				
0x030	HWINT[31:0] [B,H,W] 00000000 00000000 00000000 00000000			
0x034	HWINT[63:32] [B,H,W] 00000000 00000000 00000000 00000000			
0x038-0x04C				
0x050	HWINTCLR[31:0] [B,H,W] 00000000 00000000 00000000 00000000			
0x054	HWINTCLR[63:32] [B,H,W] 00000000 00000000 00000000 00000000			
0x058-0x06C				
0x070	DQMSK[31:0] [B,H,W] 00000000 00000000 00000000 00000000			
0x074	DQMSK[63:32] [B,H,W] 00000000 00000000 00000000 00000000			
0x078-0x08C				
0x090	DQMSKCLR[31:0] [B,H,W] 00000000 00000000 00000000 00000000			
0x094	DQMSKCLR[63:32] [B,H,W] 00000000 00000000 00000000 00000000			
0x098 – 0xFFC	-	-	-	-

1.29 MTB_DWT

MTB_DWT Base_Address : 0xF000_1000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	CMP_ADDR_START[B,H,W]			
	00000000 00000000 00000000 00000000			
0x004	CMP_DATA_START[B,H,W]			
	00000000 00000000 00000000 00000000			
0x008	CMP_MASK_START[B,H,W]			
	00000000 00000000 00000000 00000000			
0x00C	-	-	-	-
0x010	CMP_ADDR_STOP[B,H,W]			
	00000000 00000000 00000000 00000000			
0x014	CMP_DATA_STOP[B,H,W]			
	00000000 00000000 00000000 00000000			
0x018	CMP_MASK_STOP[B,H,W]			
	00000000 00000000 00000000 00000000			
0x01C	-	-	-	-
0x020	-	-	-	FCT[B,H,W]
				00000000
0x024 – 0xFCC	-	-	-	-
0xFD0	PID4[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFD4	PID5[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFD8	PID6[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFDC	PID7[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFE0	PID0[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFE4	PID1[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFE8	PID2[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFEC	PID3[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFF0	CID0[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFF4	CID1[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xFF8	CID2[B,H,W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0xFFC	CID3[B,H,W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			

1.30 Fast GPIO

Fast GPIO Base_Address : 0xF800_0000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	FPDIR0[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x004	-	-	FPDIR1[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x008	-	-	FPDIR2[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x00C	-	-	FPDIR3[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x010	-	-	FPDIR4[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x014	-	-	FPDIR5[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x018	-	-	FPDIR6[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x01C	-	-	-	-
0x020	-	-	FPDIR8[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x024 – 0x034	-	-	-	-
0x038	-	-	FPDIRE[B,H,W]	
			XXXXXXXX XXXXXXXX	
0x03C	-	-	-	-
0x040	-	-	FPDOR0[B,H,W]	
			00000000 00000000	
0x044	-	-	FPDOR1[B,H,W]	
			00000000 00000000	
0x048	-	-	FPDOR2[B,H,W]	
			00000000 00000000	
0x04C	-	-	FPDOR3[B,H,W]	
			00000000 00000000	
0x050	-	-	FPDOR4[B,H,W]	
			00000000 00000000	
0x054	-	-	FPDOR5[B,H,W]	
			00000000 00000000	
0x058	-	-	FPDOR6[B,H,W]	
			00000000 00000000	
0x05C	-	-	-	-

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x060	-	-	FPDOR8[B,H,W]	
			00000000 00000000	
0x064 – 0x074	-	-	-	-
0x078	-	-	FPDORE[B,H,W]	
			00000000 00000000	
0x07C	-	-	-	-
0x080				M_FPDIR0[B,H,W]
				XXXXXXXX
0x084	-	-	-	M_FPDIR1[B,H,W]
				XXXXXXXX
0x088 – 0x0BF	-			
0x0C0	-	-	-	M_FPDOR0[B,H,W]
				00000000
0x0C4	-	-	-	M_FPDOR1[B,H,W]
				00000000
0x0C8 – 0x0FC	-	-	-	-

1.31 VIR

VIR Base_Address : 0xF800_0100

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	VIR00[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x004	VIR01[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x008	VIR02[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x00C	VIR03[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x010	VIR04[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x014	VIR05[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x018	VIR06[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x01C	VIR07[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x020	VIR08[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x024	VIR09[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x028	VIR10[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x02C	VIR11[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x030	VIR12[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x034	VIR13[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x038	VIR14[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x03C	VIR15[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x040	VIR16[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x044	VIR17[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x048	VIR18[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x04C	VIR19[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x050	VIR20[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x054	VIR21[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x058	VIR22[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x05C	VIR23[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x060	VIR24[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x064	VIR25[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x068	VIR26[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x06C	VIR27[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x070	VIR28[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x074	VIR29[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x078	VIR30[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x07C	VIR31[W]			
	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			

E. List of Notes

This section explains notes for each function.

1. Notes when High-speed CR Is Used for Master Clock

CODE: 9APRECAUTION-FM0-E03.0

1. Notes when High-speed CR Is Used for Master Clock

This section explains notes when the high-speed CR is used for the master clock.

The frequency of the high-speed CR varies depending on the temperature and/or the power supply voltage. The following table shows notes on each function macro when the high-speed CR is used for the master clock.

Furthermore, pay attention to notes when the high-speed CR is used as an input clock of the PLL and the master clock is selected for PLL.

Notes on each macro

Macro	Function/Mode	Notes
Internal Bus Clock	HCLK/FCLK/PCLK0/PCLK1	The maximum frequency of the high-speed CR shall not exceed the upper limit of the internal operation clock frequency specified in the "Data Sheet" of the product used.
Timer	Multi-function Timer Base Timer Watch Timer Dual Timer Watch Dog Timer Quadrature	The frequency variation of the high-speed CR should be considered for the timer count value of each macro.
A/D Converter	Sampling Time Compare Tim	Considering the frequency variation of the high-speed CR, the sampling time and the compare time of the A/D converter shall satisfy the specification specified in the "Data Sheet" of the product used.
USB	-	As the frequency accuracy does not meet the required specification, these macros cannot be used when the high-speed CR is used for the master clock.
Multi Function Serial Interface	UART	Because of the frequency change of the High-Speed CR, the Board rate set may turn worse more. In case of over range of board rate error, this Function/Mode cannot be used.
	CSIO, I2C, MFS-I2S	The frequency variation of the high-speed CR should be considered for the communication of each macro.
	LIN	As the required frequency accuracy cannot be met, this function cannot be used as master. As slave, this function can be used. As a slave, the specified baud rate has more error at the maximum/minimum frequency of high-speed clock. So, if the error limit of the baud rate is exceeded, this function cannot be used.
Smart-card interface	-	Because of the frequency change of the High-Speed CR, the Board rate set may turn worse more. In case of over range of board rate error, this Function/Mode cannot be used.

F. Major Changes

Spansion Publication Number: MN710-00003

Page	Section	Changes
Revision 1.0		
-	-	Initial release
Revision 2.0		
5	The target products in this manual	Added TYPE2-M0+ products.
39	CHAPTER1-2:12bit A/D Converter 3.6 Starting DMA	Revised the description of the explanation
57	CHAPTER1-2:12bit A/D Converter 5.6 Scan Conversion input selection	Added Note
66	CHAPTER1-2:12bit A/D Converter 5.13 Sampling Time Selection	Added Note
67	CHAPTER1-2:12bit A/D Converter 5.14 Sampling Time Setup	Added Note
69	CHAPTER1-2:12bit A/D Converter 5.15 Frequency Division Ratio	Added Note
Revision 3.0		
5	The target products in this manual	Added TYPE3-M0+ products.
17	CHAPTER 1-2: 12-bit A/D Converter	Revised Figure 3-8, 3-9, 3-10,4-1
82	CHAPTER1-3: A/D Timer Trigger Selection 1. Overview	Added "The multiple A/D converters can use same start factor."
285	D. Register Map(TYPE3-M0+)	Added this chapter newly.

NOTE: Please see “Revision History” about later revised information.

Revision History

Document Revision History

Document Title:	32-Bit Microcontroller FM0+ Family Peripheral Manual Analog Macro Part		
Document Number:	002-05020		
Revision	**ECN No.**	**Origin of Change**	**Description of Change**
**	-	TOYO	New Specification
*A	5336124	KEMU	Updated to Cypress format. Updated Table 2 of Cover Page (How to use this manual) on page 6. Updated description of CHAPTER 1-2: 12-bit A/D Converter 4.4 Range Comparison Function Setting Example 4.5 Setting Conversion Time on page 50. Typo fixed of CHAPTER 1-2: 12-bit A/D Converter 5. Registers on page 52. Updated Table 1-1 of CHAPTER 3-1: LCD Controller Overview on page 101. Removed Contents of CHAPTER 3-2: LCD Controller (TYPE1) on page 103. Updated description of CHAPTER 3-3: LCD controller (TYPE2) on page 105. Updated Table 1-2 of APPENDIX Product Type List on page 159. Updated description of APPENDIX B Register Map (TYPE1-M0+) on page 161. Updated description of APPENDIX C Register Map (TYPE2-M0+) on page 215. Updated description of APPENDIX D Register Map (TYPE3-M0+) on page 279.
*B	5747733	AESATMP8	Updated logo and Copyright.
*C	6020845	KTOM	P.20 CHAPTER 1-2: Modified "Range comparison function" from "0 to 7" to "1 to 7". P.326 APPENDIX E: Removed the CAN from table of "Notes on each macro". P.7 Modified the item names of Table 1, 2, 3 from 10 digits to 8 digits. P.160 CHAPTER1: Modified the item names of "1. Product TYPE List" from 10 digits to 8 digits. P.3 Added the URL for "Microcontroller support information"