EZ-PD™ PAG2S-2P 65 W high-frequency quasi-resonant zero voltage switching flyback (QR-ZVS) charger and adapter solution user guide

REF_65W_ZVS_PAG2

About this document

Scope and purpose

This document provides instructions and a quick start guide for the EZ-PD™ PAG2S-2P controller-based Type-C charger and adapter solution (REF_65W_ZVS_PAG2).

Intended audience

This document is primarily intended for EZ-PD™ PAG2S-2P high-frequency quasi-resonant zero voltage switching flyback (QR-ZVS) charger and adapter solution developers.

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1 Introduction

EZ-PD™ PAG2P CYPAP212A1-14SXI (Power Adapter Generation 2 Primary) is Infineon's second-generation integrated primary-side start-up controller for AC/DC applications targeting the mobile power adapter segment. PAG2P interfaces with the AC mains rectified output on the primary side and receives the necessary PWM signal from the secondary side to provide a regulated output voltage. PAG2P is designed to complement a secondary controlled AC/DC flyback converter topology. In this topology, voltage and current regulation are performed by the secondary controller (PAG2S). PAG2P is responsible for providing the start-up function, driving the primary side FET as well as responding to fault conditions.

EZ-PD™ PAG2S CYPAS211A1-32LQXQ is an integrated secondary-side PWM controller and USB Power Delivery (USB PD) controller. PAG2S integrates a secondary side synchronous rectifier (SR), pulse-width modulator (PWM), and zero voltage switching (ZVS) control. PAG2S is targeted towards USB-C power adapters; it fits well into high-efficiency AC-DC flyback designs with USB PD and other standard charging protocols. PAG2S also supports USB PD Extended Power Range (EPR) mode.

Figure 1 shows the application diagram for a power adapter implementing a secondary side controlled synchronous flyback converter topology. PAG2S modulates the pulse width of the primary MOSFET in voltage control mode. PAG2S engages the internal error amplifier (EA) and a programmable ramp generator to determine the pulse width of PWM. The PWM signal is transferred from the secondary to the primary side through a pulse-edge transformer. In this topology, PAG2S integrates three key features: secondary-side PWM control, charging protocol control, and fault protection. This approach of integrating the ZVS on the secondary side has the following advantage over the traditional primary side control:

- Programmable high side ON time to reach true ZVS operation to achieve optimized efficiency

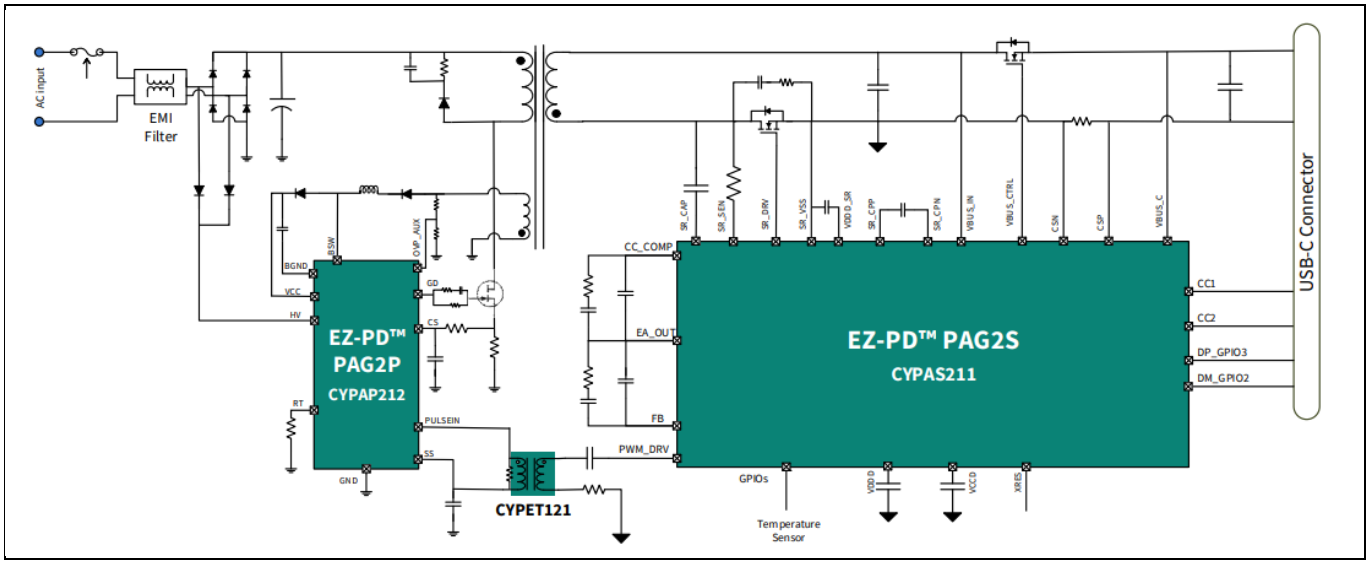

Figure 1 High-level block diagram of EZ-PD™ PAG2S-2P REF_65W_ZVS_PAG2 solution

Table 1 Critical components bill of materials (BOM)

Designator	Description	Part number	Manufacturer
U2	PAG2P primary side startup controller	CYPAP212A1-14SXQ	Infineon Technologies
U3	PAG2S USB PD power adapter secondary side controller	CYPAS211A1-32LQXQ	Infineon Technologies
Q1	OptiMOS™ N-channel 30 V 19 A	BSZ0902NS	Infineon Technologies
Q4	OptiMOS™ 6 N-channel 120 V 3.04 mΩ	ISC030N12NM6	Infineon Technologies
Q3	700 V 150 mΩ E-mode GaN transistor	GS-065-009-6S-L	Infineon Technologies
T1	118 µH ATQ23.7 power transformer	EF-239002	Better Magnetics Corp
T2	Pulse-edge transformer	ALTWR-C33TF	Infineon Technologies
C2, C3, C4, C5	Capacitor ALUM 33 µF 400 V 8x25 Radial	KCX 33 µF 400 V 8X25	Sh-ymin
C9, C48	Aluminum organic polymer capacitors 560 µF 25 V (6.3x10)	NPX 560 µF 25 V 6.3x10	Sh-ymin

2 Specifications

Table 2 Test specifications

Parameter	Value
Input voltage and frequency	100 V to 240 V AC, 47 Hz to 63 Hz
Max output power	65 W, 20 V to 3.25 A max
Output voltage	Fixed PDOs: 5.0 V / 3.0 A, 9.0 V / 3.0 A, 15.0 V / 3.0 A, 20.0 V / 3.25 A PPS: 5 V to 11 V, 3.0 A; 5 V to 16 V, 3.0 A; 5 V to 21.0 V, 3.25 A with PPS power limit
Peak efficiency	> 94%
Protections	1. Input overvoltage protection 2. Input undervoltage protection 3. V_{BUS_C} overvoltage protection (OVP) 4. V_{BUS_C} undervoltage protection (UVP) 5. Overcurrent protection (OCP) 6. Short-circuit protection (SCP) 7. Overtemperature protection (OTP) 8. V_{BUS_C} to CC short protection
Charging standards supported	1. USB-C PD v3.1 including programmable power supply (PPS) mode 2. Apple Charging 2.4 A 3. Qualcomm QC 2.0, 3.0, 4.0, 5.0 4. Samsung AFC 5. USB BC 1.2
EMI/EMC	1. Conducted emissions, CISPR32 CLASS B, 4 dB margin at 115/220 V AC 2. ESD, IEC61000-4-2, ±8 kV contact, ±16 kV air, Criteria A 3. Surge, IEC61000-4-5, ±1 kV DM and ±2 kV CM, Criteria B

3 Board overview

The EZ-PD™ PAG2S-2P-based 65 W QR-ZVS flyback USB PD charger and adapter solution (REF_65W_ZVS_PAG2) are shown in Figure 2. Solution board is designed to meet the specifications shown in Table 2.

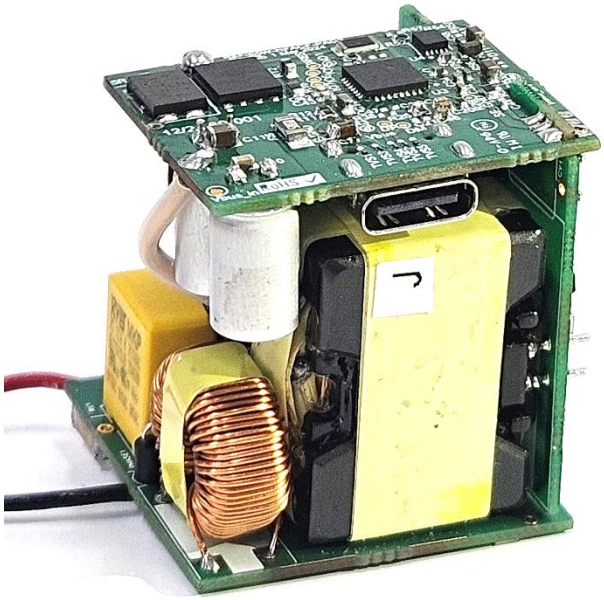

Figure 2 REF_65W_ZVS_PAG2 solution board

In this solution, the EZ-PD™ PAG2x operates with an optimal frequency of 150 kHz and functions as a secondary-side flyback and SR controller. This solution board consists of three boards:

- Baseboard being primary board with PAG2P and other power components
- EMI board with filters and bulk capacitors
- Secondary board with PAG2S, SR MOSFET, and Type-C connector

Figure 3 shows the schematic of PAG2S-2P-based 65 W high frequency QR-ZVS flyback charger and adapter solution.

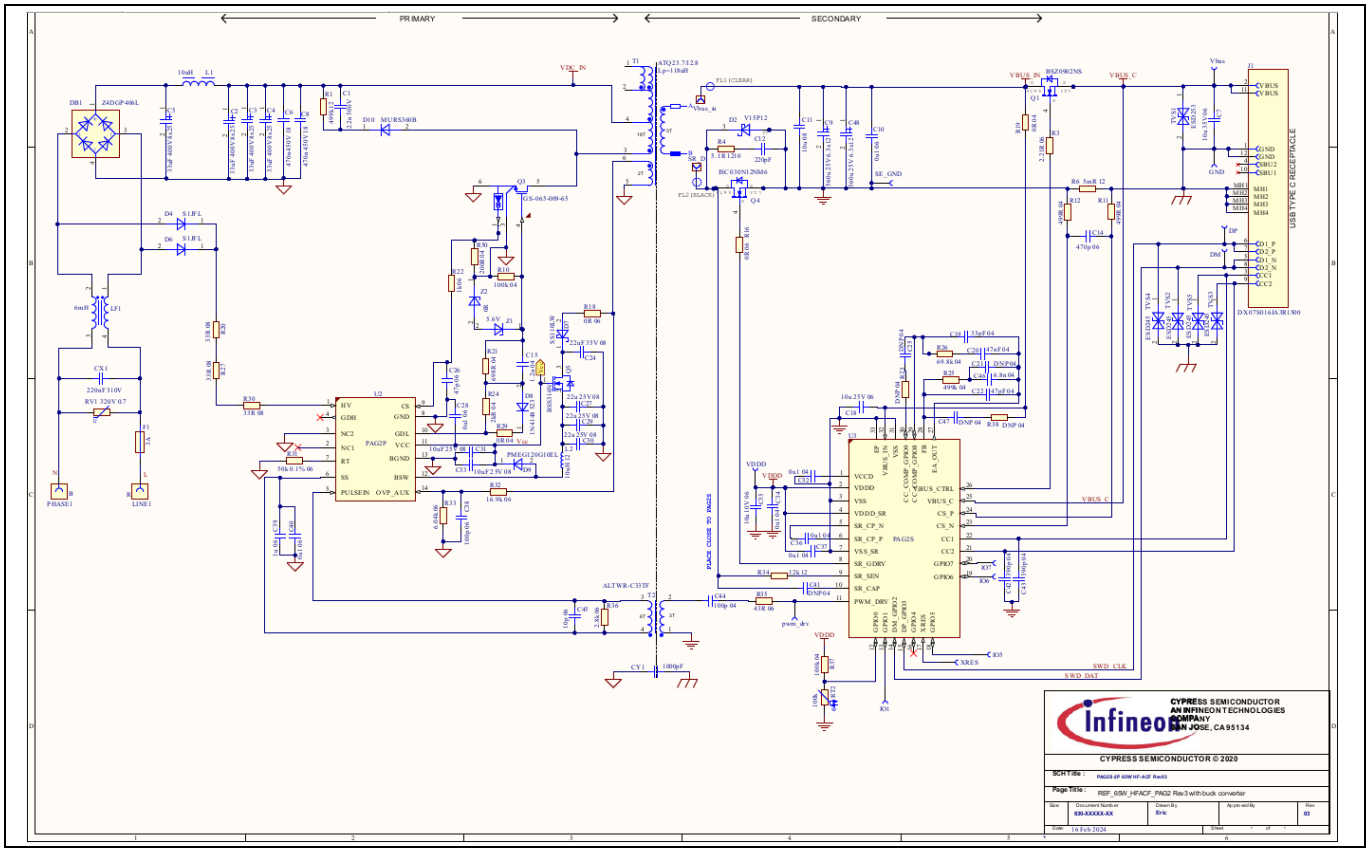

Figure 3 REF_65W_ZVS_PAG2 schematic

PAG2S uses PSoC™ MiniProg4 Program and Debug Kit (CY8CKIT-005-A) is an all-in-one development programmer and debugger for PSoC™ 4, PSoC™ 5LP, and PSoC™ 6 MCU devices to program the EZ-PD™ controllers. The PAG2S-based board uses a PSoC™ MiniProg4 five-pin connection and a JTAG to Type-C connector board. In this way, one can simply program the PAG2S-2P-based 65 W QR-ZVS flyback charger and adapter board using a Type-C connector.



Figure 4 MiniProg4 Program and Debug Kit (CY8CKIT-005-A)

3.1 Programming interface and settings

The PSoC™ Programmer software is used as a programming interface to program the firmware (*.hex* file) in an PAG2S-based board. For programming, select the “CCGx” platform and update the settings as shown in Figure 5.

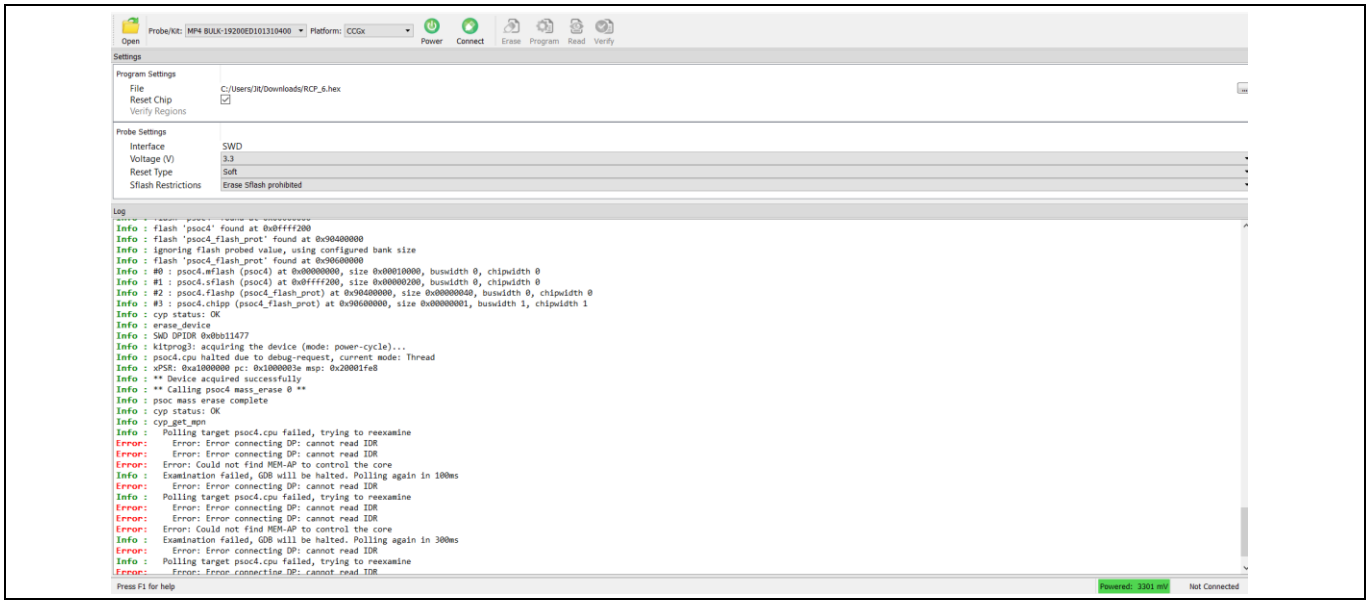

Figure 5 Programming interface to program the PAG2S board

4 Test setup

Figure 6 shows the test setup to capture the electrical data of the DUT. The following is the optimal setup to capture the efficiency:

- Input power using a power meter
- Output power using high-resolution output multimeters

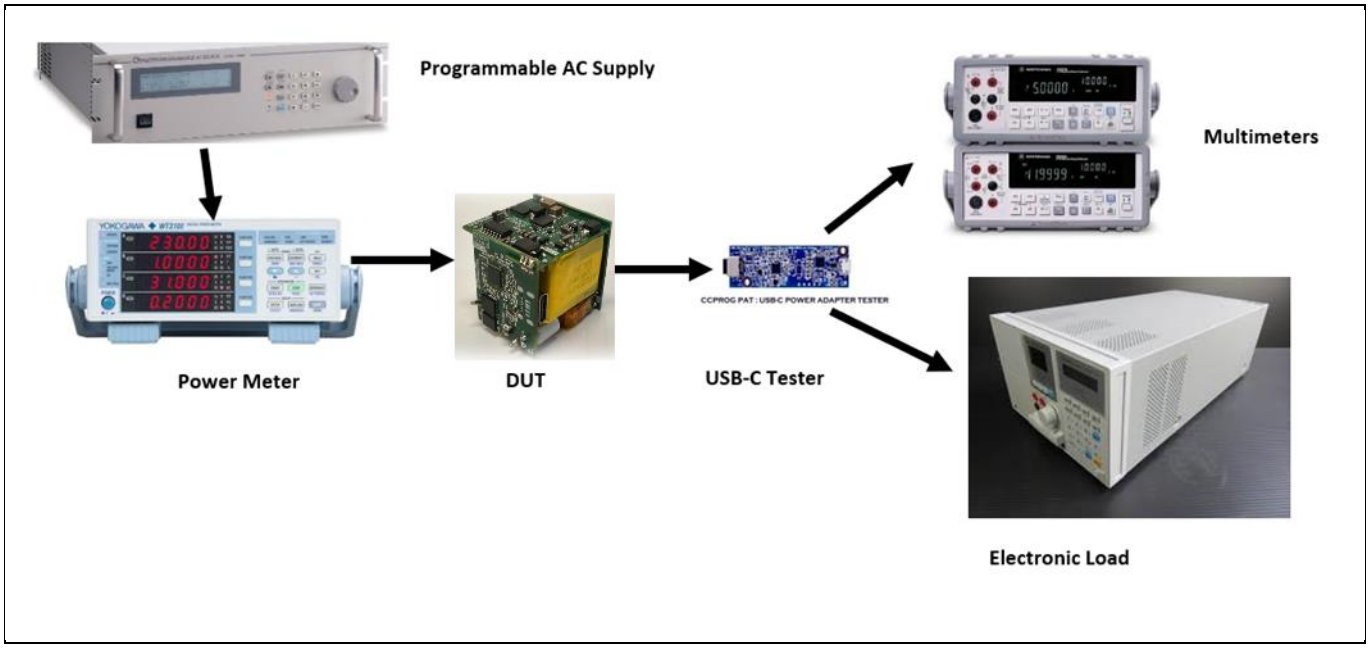

Figure 6 Test equipment connected to the standalone REF_65W_ZVS_PAG2 board

4.1 Test equipment

Table 3 shows the test equipment to measure performance parameters such as efficiency, ripple, regulation, and transient response.

Table 3 Test equipment details

Test setup	Description
Programmable AC source	Chroma 61501
AC power meter	Yokogawa WT310E
PAT tester	USBCEE PAT
Electronic load	Chroma 63102A
Multimeters	Keysight 34465A

4.2 Power adapter tester (PAT)

Connect the DUT to a USB-C PAT using a USB-C cable. After the connection is established, the PAT UI does a PDO discovery and displays the results.

The PAG2S-2P based 65 W QR-ZVS flyback charger and adapter solution is pre-configured with seven PDOs:

- **Fixed PDOs**: 5.0 V / 3.0 A; 9.0 V / 3.0 A; 15.0 V / 3.0 A; 20.0 V / 3.25 A
- **PPS**: 5 V to 11 V, 3.0 A; 5 V to 15.0 V, 3.0 A; 5 V to 21.0 V, 3.25 A (PPS power limited)

Choose a suitable pre-configured PDO or configure a new one using the EZ-PD™ Configuration Utility. Tests in the following sections use pre-configured PDOs.

To know more about the PAT tester, see USBCEE.

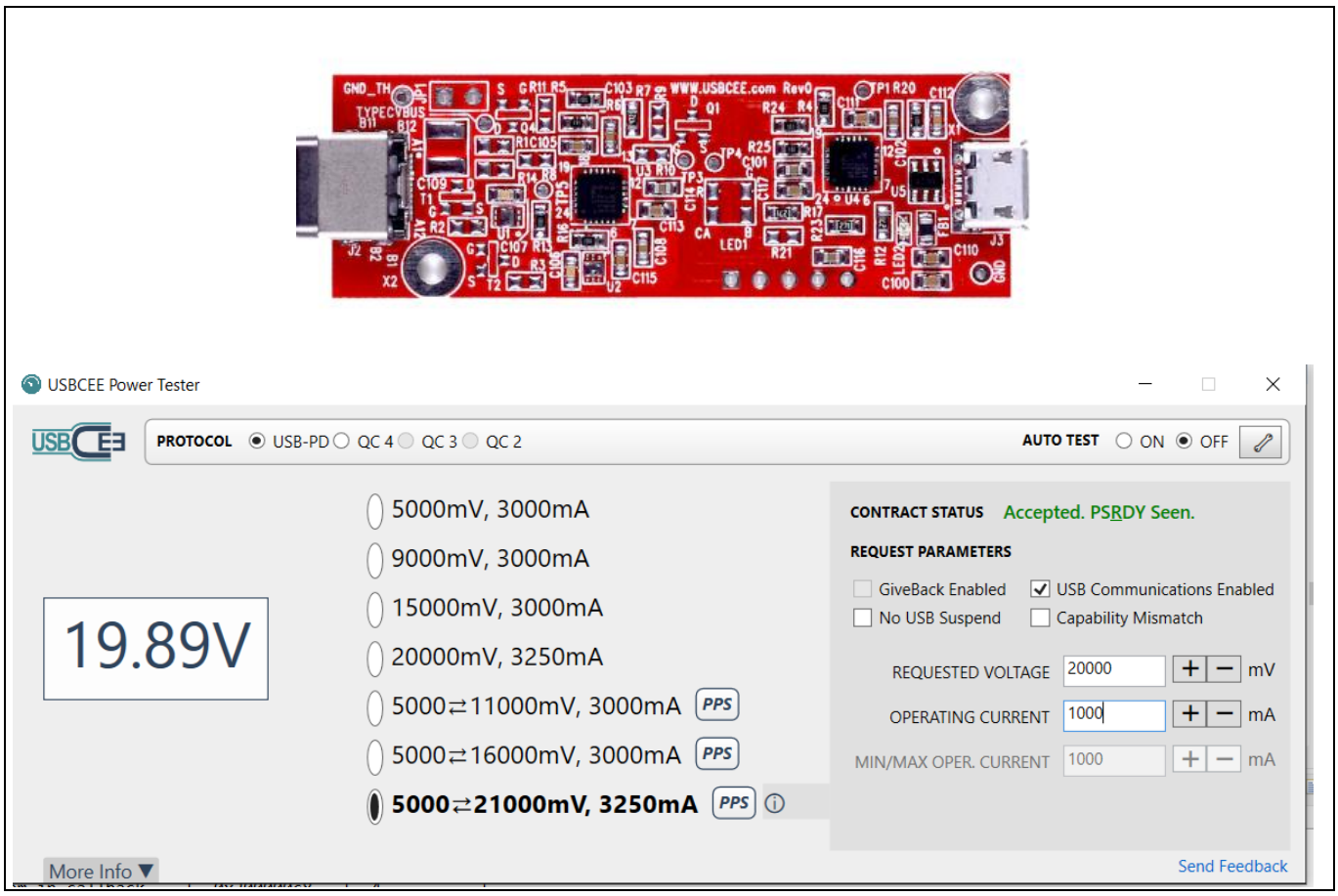

Figure 7 PAT tester and user interface

5 Quick steps for demo

1. Connect the 65-W solution board to the power meter AC terminal (that is already connected to the programmable AC supply) as shown in Figure 6.
2. Connect a USB PD tester or a power adapter tester (PAT) to the port and ensure that the USB PD tester gets a successful Power Delivery contract as shown in Figure 7.
3. Connect the electronic load at the PAT tester load terminal as shown in Figure 6.
4. Select the desired voltage on PAT UI and ramp up the load on the electronic load.

References

Datasheets

[1] 002-34772: CYPAP211/ CYPAP212 EZ-PD™ PAG2P primary-side startup controller

[2] 002-37216: CYPAS211 EZ-PD™ PAG2S-QZ integrated USB PD and secondary-side QR-ZVS controller

Revision history

Document revision	Date	Description of changes
**	2024-07-29	Initial release

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