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32-Bit Microcontroller FM4 Family Peripheral Manual Timer Part

Doc. No. 002-04858 Rev.*C

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Preface

Thank you for your continued use of Cypress products.
Read this manual and the data sheet thoroughly before using products in this family.

Purpose of This Manual / Intended Readers

This manual explains the functions and operations of this family and describes how they are used. The manual is intended for engineers engaged in the actual development of products using this family.
For the descriptions of the Analog macro, Timer, and Communication Macro, see the respective separate peripheral manuals.

Note:

- *This manual explains the configuration and operation of the peripheral functions, but does not cover the specifics of each device in the series.*
  Users should refer to the respective data sheets of devices for device-specific details.
- *Whether a peripheral function is on board or not is dependent on product type. See data sheets for details.*

Sample Programs and Development Environment

Cypress offers sample programs free of charge for using the peripheral functions of the FM4 family. Cypress also makes available descriptions of the development environment required for this family. Feel free to use them to verify the operational specifications and usage of this Cypress microcontroller.

Microcontroller support information:

https://community.cypress.com/community/MCU

Note:

- *Note that the sample programs are subject to change without notice. Since they are offered as a way to demonstrate standard operations and usage, evaluate them sufficiently before running them on your system.*
  Cypress assumes no responsibility for any damage that may occur as a result of using a sample program.

Overall Organization of This Manual

Peripheral Manual Timer part has 8 chapters and Appendixes as shown below.

CHAPTER 1: Watchdog Timer
CHAPTER 2: Dual Timer
CHAPTER 3-1: Watch Counter Prescaler
CHAPTER 3-2: Watch Counter
CHAPTER 4-1: Real-time Clock
CHAPTER 4-2: RTC Count Block (A)
CHAPTER 4-3: RTC Count Block (B)
CHAPTER 4-4: RTC Count Block (C)
CHAPTER 4-5: RTC Clock Control Block (A)
CHAPTER 4-6: RTC Clock Control Block (B)
CHAPTER 4-7: RTC Clock Control Block (C)
CHAPTER 5-1: Base Timer I/O Select Function
CHAPTER 5-2: Base Timer
CHAPTER 6: Multifunction Timer

CHAPTER 7-1: PPG Configuration
CHAPTER 7-2: PPG
CHAPTER 8-1: Quadrature Position/Revolution Counter
CHAPTER 8-2: Quad Counter Position Rotation Count Display Function
Appendixes

Related Manuals

The manuals related to this family are listed below. See the manual appropriate to the applicable conditions.

The contents of these manuals are subject to change without notice. Contact us to check the latest versions available.

Peripheral Manual

■ FM4 Family Peripheral Manual (002-04856)
Called Peripheral Manual hereafter

■ FM4 Family Peripheral Manual Timer Part (this manual)
Called Timer Part hereafter

■ FM4 Family Peripheral Manual Analog Macro Part (002-04860)
Called Analog Macro Part hereafter

■ FM4 Family Peripheral Manual Communication Macro Part (002-04862)
Called Communication Macro Part hereafter

■ FM4 Family Peripheral Manual GDC Part (002-04917)
Called GDC Part hereafter

Data Sheet

For details about device-specific, electrical characteristics, package dimensions, ordering information etc., see the following document.

■ 32-bit Microcontroller FM4 Family Data Sheet

Note:

- *The data sheets for each series are provided.*
  See the appropriate data sheet for the series that you are using.

CPU Programming Manual

For details about Arm Cortex-M4F core, see the following documents that can be obtained from http://www.arm.com/.

■ Cortex-M4 Technical Reference Manual
■ Arm v7-M Architecture Application Level Reference Manual

Flash Programming Manual

For details about the functions and operations of the built-in flash memory, see the following document.

■ FM4 Family Flash Programming Manual

Note:

- *Flash programming manuals for each series are provided.*
  See the appropriate flash programming manual for the series that you are using.

How to Use This Manual

Finding a Function

The following methods can be used to search for the explanation of a desired function in this manual:

■ Search from the table of the contents

The table of the contents lists the manual contents in the order of description.

■ Search from the register

The address where each register is located is not described in the text. To verify the address of a register, see A. Register Map in Appendixes.

About the Chapters

Basically, this manual explains 1 peripheral function per chapter.

Terminology

This manual uses the following terminology.

Term	Explanation
Word	Indicates access in units of 32 bits.
Half word	Indicates access in units of 16 bits.
Byte	Indicates access in units of 8 bits.

Notations

■ The notations in bit configuration of the register explanation of this manual are written as follows.

- bit: bit number
- Field: bit field name
- Attribute: Attributes for read and write of each bit
  - R: Read only
  - W: Write only
  - R/W: Readable/Writable
  - -: Undefined
- Initial value: Initial value of the register after reset
  - 0: Initial value is 0
  - 1: Initial value is 1
  - X: Initial value is undefined

■ The multiple bits are written as follows in this manual.

- Example: bit7:0 indicates the bits from bit7 to bit0

■ The values such as for addresses are written as follows in this manual.

- Hexadecimal number: 0x is attached in the beginning of a value as a prefix (example: 0xFFFF)
- Binary number: 0b is attached in the beginning of a value as a prefix (example: 0b1111)
- Decimal number : Written using numbers only (example: 1000)

The Target Products in This Manual

- In this manual, the products are classified into the following groups and are described follows.
  For the descriptions such as "TYPE1-M4", see the relevant items of the target product in the list below.

Table 1 TYPE1-M4 Product List

Description in this manual	Flash memory size		
	1024 Kbytes	768 Kbytes	512 Kbytes
TYPE1-M4	CY9BF568M CY9BF568N CY9BF568R CY9BF568RF MB9BF568M MB9BF568N MB9BF568R MB9BF568RF	CY9BF567M CY9BF567N CY9BF567R MB9BF567M MB9BF567N MB9BF567R	CY9BF566M CY9BF566N CY9BF566R MB9BF566M MB9BF566N MB9BF566R
	CY9BF468M CY9BF468N CY9BF468R MB9BF468M MB9BF468N MB9BF468R	CY9BF467M CY9BF467N CY9BF467R MB9BF467M MB9BF467N MB9BF467R	CY9BF466M CY9BF466N CY9BF466R MB9BF466M MB9BF466N MB9BF466R
	CY9BF368M CY9BF368N CY9BF368R MB9BF368M MB9BF368N MB9BF368R	CY9BF367M CY9BF367N CY9BF367R MB9BF367M MB9BF367N MB9BF367R	CY9BF366M CY9BF366N CY9BF366R MB9BF366M MB9BF366N MB9BF366R
	CY9BF168M CY9BF168N CY9BF168R MB9BF168M MB9BF168N MB9BF168R	CY9BF167M CY9BF167N CY9BF167R MB9BF167M MB9BF167N MB9BF167R	CY9BF166M CY9BF166N CY9BF166R MB9BF166M MB9BF166N MB9BF166R

Table 2 TYPE2-M4 Product List

Description in this manual	Flash memory size		
	512 Kbytes	384 Kbytes	256 Kbytes
TYPE2-M4	CY9BF566K CY9BF566L MB9BF566K MB9BF566L	CY9BF565K CY9BF565L MB9BF565K MB9BF565L	CY9BF564K CY9BF564L MB9BF564K MB9BF564L
	CY9BF466K CY9BF466L MB9BF466K MB9BF466L	CY9BF465K CY9BF465L MB9BF465K MB9BF465L	CY9BF464K CY9BF464L MB9BF464K MB9BF464L
	CY9BF366K CY9BF366L MB9BF366K MB9BF366L	CY9BF365K CY9BF365L MB9BF365K MB9BF365L	CY9BF364K CY9BF364L MB9BF364K MB9BF364L
	CY9BF166K CY9BF166L MB9BF166K MB9BF166L	CY9BF165K CY9BF165L MB9BF165K MB9BF165L	CY9BF164K CY9BF164L MB9BF164K MB9BF164L

Table 3 TYPE3-M4 Product List

Description in this manual	Flash memory size			No-Flash
	2 Mbytes	1.5 Mbytes	1 Mbytes	SRAM size 256 Kbytes
TYPE3-M4	S6E2CCAL S6E2CCAJ S6E2CCAH	S6E2CC9L S6E2CC9J S6E2CC9H	S6E2CC8L S6E2CC8J S6E2CC8H	-
	S6E2C5AL S6E2C5AJ S6E2C5AH	S6E2C59L S6E2C59J S6E2C59H	S6E2C58L S6E2C58J S6E2C58H	-
	S6E2C4AL S6E2C4AJ S6E2C4AH	S6E2C49L S6E2C49J S6E2C49H	S6E2C48L S6E2C48J S6E2C48H	-
	S6E2C3AL S6E2C3AJ S6E2C3AH	S6E2C39L S6E2C39J S6E2C39H	S6E2C38L S6E2C38J S6E2C38H	-
	S6E2C2AL S6E2C2AJ S6E2C2AH	S6E2C29L S6E2C29J S6E2C29H	S6E2C28L S6E2C28J S6E2C28H	-
	S6E2C1AL S6E2C1AJ S6E2C1AH	S6E2C19L S6E2C19J S6E2C19H	S6E2C18L S6E2C18J S6E2C18H	S6E2C10L S6E2C10J S6E2C10H

Table 4 TYPE4-M4 Product List

Description in this manual	Flash memory size 384 Kbytes	
	VRAM 512 Kbytes	VRAM 512 Kbytes + VFLASH 2 Mbytes
TYPE4-M4	S6E2D35G0 S6E2D35J0	S6E2D35GJ
	S6E2D55G0 S6E2D55J0	S6E2D55GJ
	S6E2DF5G0 S6E2DF5J0	S6E2DF5GJ
	S6E2DH5G0 S6E2DH5J0	S6E2DH5GJ

Table 5 TYPE5-M4 Product List

Description in this manual	Flash memory size	
	1 Mbytes	512 Kbytes
TYPE5-M4	S6E2GM8J S6E2GM8H	S6E2GM6J S6E2GM6H
	S6E2GK8J S6E2GK8H	S6E2GK6J S6E2GK6H
	S6E2GH8J S6E2GH8H	S6E2GH6J S6E2GH6H
	S6E2G28J S6E2G28H	S6E2G26J S6E2G26H
	S6E2G38J S6E2G38H	S6E2G36J S6E2G36H

Table 6 TYPE6-M4 Product List

Description in this manual	Flash memory size	
	512 Kbytes	**256 Kbytes**
TYPE6-M4	S6E2HG6G S6E2HG6F S6E2HG6E	S6E2HG4G S6E2HG4F S6E2HG4E
	S6E2HE6G S6E2HE6F S6E2HE6E	S6E2HE4G S6E2HE4F S6E2HE4E
	S6E2H46G S6E2H46F S6E2H46E	S6E2H44G S6E2H44F S6E2H44E
	S6E2H16G S6E2H16F S6E2H16E	S6E2H14G S6E2H14F S6E2H14E

Contents

CHAPTER 1: Watchdog Timer 23
1. Overview 24
2. Configuration and Block Diagram 25
3. Operations 27
4. Setting Procedure Example 33
5. Operation Example 37
6. Registers 40
   - 6.1 Software Watchdog Timer Load Register (WdogLoad) 41
   - 6.2 Software Watchdog Timer Value Register (WdogValue) 42
   - 6.3 Software Watchdog Timer Control Register (WdogControl) 43
   - 6.4 Software Watchdog Timer Clear Register (WdogIntClr) 45
   - 6.5 Software Watchdog Timer Interrupt Status Register (WdogRIS) 46
   - 6.6 Software Watchdog Timer Window Watchdog Mode Control Register (WdogSPMC) 47
   - 6.7 Software Watchdog Timer Lock Register (WdogLock) 48
   - 6.8 Hardware Watchdog Timer Load Register (WDG_LDR) 49
   - 6.9 Hardware Watchdog Timer Value Register (WDG_VLR) 50
   - 6.10 Hardware Watchdog Timer Control Register (WDG_CTL) 51
   - 6.11 Hardware Watchdog Timer Clear Register (WDG_ICL) 52
   - 6.12 Hardware Watchdog Timer Interrupt Status Register (WDG_RIS) 53
   - 6.13 Hardware Watchdog Timer Lock Register (WDG_LCK) 54
7. Usage Precautions 55

CHAPTER 2: Dual Timer 57
1. Overview 58
2. Configuration 59
3. Operations 60
   - 3.1 Timer Operating Mode 61
   - 3.2 Initial State 65
   - 3.3 Interrupt Operation 66
4. Setting Procedure Example 67
5. Registers 69
   - 5.1 Load Register (TimerXLoad) X=1 or 2 70
   - 5.2 Value Register (TimerXValue) X=1 or 2 71
   - 5.3 Control Register (TimerXControl) X=1 or 2 72
   - 5.4 Interrupt Clear Register (TimerXIntClr) X=1 or 2 74
   - 5.5 Interrupt Status Register (TimerXRIS) X=1 or 2 75
   - 5.6 Masked Interrupt Status Register (TimerXMIS) X=1 or 2 76
   - 5.7 Background Load Register (TimerXBGLoad) X=1 or 2 77

CHAPTER 3-1: Watch Counter Prescaler 79
1. Overview of Watch Counter Prescaler 80
2. Configuration of Watch Counter Prescaler 81

3. Explanation of Operations and Setting Procedures of the Watch Counter Prescaler 82
4. Registers of Watch Counter Prescaler 85
4.1 Clock Selection Register (CLK_SEL) 86
4.2 Division Clock Enable Register (CLK_EN) 87
CHAPTER 3-2: Watch Counter 89
1. Overview of the Watch Counter 90
2. Configuration of the Watch Counter 91
3. Interrupts of the Watch Counter 92
4. Explanation of Operations and Setting Procedure Examples of the Watch Counter 93
5. Registers of Watch Counter 95
5.1 Watch Counter Read Register (WCRD) 96
5.2 Watch Counter Reload Register (WCRL) 97
5.3 Watch Counter Control Register (WCCR) 98
CHAPTER 4-1: Real-time Clock 101
1. Configuration of Real-time Clock 102
2. Real-time Clock Acronym 104
3. Resetting RTC 105
CHAPTER 4-2: RTC Count Block(A) 107
1. Overview of RTC Count Block 108
2. Block Diagram of RTC Count Block 109
3. Operations of RTC Count Block and Setting Procedures 111
4. RTC Control Block Reset Operation 124
5. Leap Year Compliance of RTC Count Block 127
6. Time Rewrite Error 129
7. Registers in RTC Control Block 130
7.1 Control Register 10 (WTCR 10) 131
7.2 Control Register 11 (WTCR 11) 132
7.3 Control Register 12 (WTCR 12) 135
7.4 Control Register 13 (WTCR 13) 136
7.5 Control Register 20 (WTCR 20) 139
7.6 Control Register 21 (WTCR 21) 141
7.7 Second Register (WTSR) 142
7.8 Minute Register (WRMIR) 143
7.9 Hour Register (WTHR) 144
7.10 Day Register (WTDR) 145
7.11 Day of the Week Register (WTDW) 146
7.12 Month Register (WTMOR) 147
7.13 Year Register (WTYR) 148
7.14 Alarm Minute Register (ALMIR) 149
7.15 Alarm Hour Register (ALHR) 150
7.16 Alarm Day Register (ALDR) 151
7.17 Alarm Month Register (ALMOR) 152
7.18 Alarm Year Register (ALYR) 153
7.19 Time Setting Register 0 (WTTR0) 154
7.20 Time Setting Register 1 (WTTR1) 155
7.21 Time Setting Register 2 (WTTR2) 156
8. Usage Precautions 157
CHAPTER 4-3: RTC Count Block (B) 159
1. Overview of RTC Count Block 160

2. Block Diagram of RTC Count Block 161
3. Operations of RTC Count Block and Setting Procedures 163
4. RTC Control Block Reset Operation 175
5. Leap Year Compliance of RTC Count Block 178
6. Time Rewrite Error 180
7. Registers in RTC Control Block 181
7.1 Control Register 10 (WTCR 10) 182
7.2 Control Register 11 (WTCR 11) 184
7.3 Control Register 12 (WTCR 12) 186
7.4 Control Register 13 (WTCR 13) 188
7.5 Control Register 20 (WTCR 20) 190
7.6 Control Register 21 (WTCR 21) 192
7.7 Second Register (WTSR) 193
7.8 Minute Register (WRMIR) 194
7.9 Hour Register (WTHR) 195
7.10 Day Register (WTDR) 196
7.11 Day of the Week Register (WTDW) 197
7.12 Month Register (WTMOR) 198
7.13 Year Register (WTYR) 199
7.14 Alarm Minute Register (ALMIR) 200
7.15 Alarm Hour Register (ALHR) 201
7.16 Alarm Day Register (ALDR) 202
7.17 Alarm Month Register (ALMOR) 203
7.18 Alarm Year Register (ALYR) 204
7.19 Time Setting Register 0 (WTTR0) 205
7.20 Time Setting Register 1 (WTTR1) 206
7.21 Time Setting Register 2 (WTTR2) 207
8. Usage Precautions 208
CHAPTER 4-4: RTC Count Block(C) 209
1. Overview of RTC Count Block 210
2. Block Diagram of RTC Count Block 211
3. Operations of RTC Count Block and Setting Procedures 213
4. RTC Count Block Reset Operation 224
5. Leap Year Compliance of the RTC Count Block 227
6. Time Rewrite Error 229
7. Registers in RTC Control Block 231
7.1 Control Register 1 (WTCR 1) 232
7.2 Control Register 2 (WTCR 2) 238
7.3 Counter Cycle Setting Register (WTBR) 240
7.4 Day Register (WTDR) 240
7.5 Hour Register (WTHR) 242
7.6 Minute Register (WTMIR) 243
7.7 Second Register (WTSR) 244
7.8 Year Register (WTYR) 245
7.9 Month Register (WTMOR) 246
7.10 Day of the Week Register (WTDW) 247
7.11 Alarm Day Register (ALDR) 248
7.12 Alarm Hour Register (ALHR) 249
7.13 Alarm Minute Register (ALMIR) 250

7.14 Alarm Year Register (ALYR) ... 251
7.15 Alarm Month Register (ALMOR) ... 252
7.16 Time Setting Register (WTTR) ... 253
8. Usage Precautions ... 254
CHAPTER 4-5: RTC Clock Control Block (A) ... 255
1. Overview of the RTC Clock Control Block ... 256
2. Configuration of the RTC Clock Control Block ... 257
3. Operations of the RTC Clock Control Block ... 258
4. Setting Procedures of the RTC Clock Control Block ... 262
5. Registers of the RTC Clock Control Block ... 265
5.1 Frequency Correction Value Setting Register 0 (WTCAL0) ... 266
5.2 Frequency Correction Value Setting Register 1 (WTCAL1) ... 267
5.3 Frequency Correction Enable Register (WTCALEN) ... 268
5.4 Division Ratio Setting Register (WTDIV) ... 269
5.5 Divider Output Enable Register (WTDIVEN) ... 270
5.6 Frequency Correction Period Setting Register (WTCALPRD) ... 271
5.7 RTCCO Output Selection Register (WTCOSEL) ... 272
CHAPTER 4-6: RTC Clock Control Block(B) ... 273
1. Overview of the RTC Clock Control Block ... 274
2. Configuration of the RTC Clock Control Block ... 275
3. Operations of the RTC Clock Control Block ... 276
4. Setting Procedures of the RTC Clock Control Block ... 280
5. Registers of the RTC Clock Control Block ... 281
5.1 Frequency Correction Value Setting Register 0 (WTCAL0) ... 282
5.2 Frequency Correction Value Setting Register 1 (WTCAL1) ... 283
5.3 Frequency Correction Enable Register (WTCALEN) ... 284
5.4 Division Ratio Setting Register (WTDIV) ... 285
5.5 Divider Output Enable Register (WTDIVEN) ... 286
5.6 Frequency Correction Period Setting Register (WTCALPRD) ... 287
5.7 RTCCO Output Selection Register (WTCOSEL) ... 288
CHAPTER 4-7: RTC Clock Control Block (C) ... 289
1. Overview of the RTC Clock Control Block ... 290
2. Configuration of the RTC Clock Control Block ... 291
3. Operations of the RTC Clock Control Block ... 292
4. Setting Procedures of the RTC Clock Control Block ... 297
5. Registers of the RTC Clock Control Block ... 298
5.1 Clock Selection Register (WTCLKS) ... 299
5.2 Selection Clock Status Register (WTCLKM) ... 300
5.3 Frequency Correction Value Setting Register (WTCAL) ... 301
5.4 Frequency Correction Enable Register (WTCALEN) ... 302
5.5 Division Ratio Setting Register (WTDIV) ... 303
5.6 Divider Output Enable Register (WTDIVEN) ... 304
5.7 Frequency Correction Period Setting Register (WTCALPRD) ... 305
5.8 RTCCO Output Selection Register (WTCOSEL) ... 306
CHAPTER 5-1: Base Timer I/O Select Function ... 307
1. Overview ... 308
2. Configuration ... 309
3. I/O Mode ... 310
3.1 Pins 311

3.2 I/O Mode 313
4. Registers 331
4.1 I/O Select Register (BTSEL0123) 332
4.2 I/O Select Register (BTSEL4567) 334
4.3 I/O Select Register (BTSEL89AB) 336
4.4 I/O Select Register (BTSELCDEF) 338
4.5 Software-based Simultaneous Startup Register (BTSSSR) 340
CHAPTER 5-2: Base Timer 341
1. Overview of the Base Timer 342
2. Block Diagram of the Base Timer 344
3. Operations of the Base Timer 348
4. 32-bit Mode Operations 349
5. Base Timer Interrupt 351
6. Starting the DMA Controller (DMAC) 352
7. Registers of the Base Timer 353
8. Notes on using the Base Timer 354
9. Descriptions of Base Timer Functions 355
9.1 PWM Timer Function 356
9.1.1 16-bit PWM Timer Operations 357
9.1.2 One-shot Operation 358
9.1.3 Interrupt Factors and Timing Chart 359
9.1.4 Output Waveforms 360
9.1.5 PWM Timer Operation Flowchart 361
9.1.6 Timer Control Registers (TMCR and TMCR2) and Status Control Register (STC) used when the PWM Timer is selected 362
9.1.7 PWM Cycle Set Register (PCSR) 369
9.1.8 PWM Duty Set Register (PDUT) 370
9.1.9 Timer Register (TMR) 371
9.2 PPG Timer Function 372
9.2.1 16-bit PPG Timer Operations 373
9.2.2 Continuous Operation 374
9.2.3 One-shot Operation 375
9.2.4 Interrupt Factors and Timing Chart 377
9.2.5 PPG Timer Operation Flowchart 378
9.2.6 Timer Control Registers (TMCR and TMCR2) and Status Control Register (STC) used when the PPG Timer is selected 379
9.2.7 LOW Width Reload Register (PRLL) 386
9.2.8 HIGH Width Reload Register (PRLH) 387
9.2.9 Timer Register (TMR) 388
9.3 Reload Timer Function 389
9.3.1 Operations of the 16-bit Reload Timer 390
9.3.2 Reload Timer Operation Flowchart 394
9.3.3 Timer Control Registers (TMCR and TMCR2) and Status Control Register (STC) used when the Reload Timer is selected 395
9.3.4 Cycle Set Register (PCSR) 402
9.3.5 Timer Register (TMR) 403
9.4 PWC Timer Function 404
9.4.1 Operations of the PWC Timer 405
9.4.2 Timer Control Registers (TMCR and TMCR2) and Status Control Register

(STC) used when the PWC Timer is selected 413
9.4.3 Data Buffer Register (DTBF) 420
CHAPTER 6: Multifunction Timer 421
1. Overview of the Multifunction Timer 422
2. Configuration of the Multifunction Timer 423
2.1 Block Diagram of the Multifunction Timer 424
2.1.1 Block Diagram 424
2.1.2 Outline of Function Blocks 426
2.2 Description of Each Function Block 427
2.2.1 FRT: 3 Channels 427
2.2.2 OCU: 6 Channels (2 Channels × 3 Units) 431
2.2.3 WFG: 3 Channels 434
2.2.4 NZCL 438
2.2.5 ICU: 4 Channels (2 Channels × 2 Units) 440
2.2.6 ADCMP: 6 Channels 442
2.3 I/O Pins of the Multifunction Timer Unit 446
2.3.1 Correspondence with External I/O Pins 446
2.3.2 Interrupt Signal Outputs 447
2.3.3 Other I/O Signals 448
2.4 Function Differences by Product Type 449
3. Registers of the Multifunction Timer 450
3.1 Individual Notations and Common Notations of Channel Numbers in Descriptions of Functions 451
3.2 List of Multifunction Timer Registers 454
3.3 Details of Register Functions 457
3.3.1 FRT Control Register A (TCSA) 458
3.3.2 FRT Control Register C (TCSC) 464
3.3.3 FRT Control Register D (TCSD) (Products after TYPE3-M4) 466
3.3.4 FRT Cycle Setting Register (TCCP) 467
3.3.5 FRT Count Value Register (TCDT) 468
3.3.6 FRT Simultaneous Start Control Register (TCAL) 469
3.3.7 OCU Connecting FRT Select Register (OCFS) 471
3.3.8 OCU Control Register A (OCSA) 472
3.3.9 OCU Control Register B (OCSB) 475
3.3.10 OCU Control Register C (OCSC) 478
3.3.11 OCU Control Register D (OCSD) (TYPE1-M4, TYPE2-M4 products) 479
3.3.12 OCU Control Register D (OCSD) (Products after TYPE3-M4) 482
3.3.13 OCU Control Register E (OCSE) 485
3.3.14 OCU Compare Value Store Register (OCCP) 491
3.3.15 WFG Control Register A (WFSA) 492
3.3.16 WFG Timer Value Register (WFTA/WFTB) 497
3.3.17 Pulse Counter Value Register (WFTF) 498
3.3.18 NZCL Control Register (NZCL) 499
3.3.19 WFG Interrupt Control Register (WFIR) 505
3.3.20 ICU Connecting FRT Select Register (ICFS) 509
3.3.21 ICU Control Register A (ICSA) 510
3.3.22 ICU Control Register B (ICSB) 513
3.3.23 ICU Capture Value Store Register (ICCP) 514
3.3.24 ADCMP Connecting FRT Select Register (ACFS) 515

3.3.25 ADCMP Control Register A (ACSA) 516
3.3.26 ADCMP Control Register C (ACSC) 518
3.3.27 ADCMP Control Register D (ACSD) 520
3.3.28 ADCMP Compare Value Store Register (ACMP) 523
3.3.29 ADCMP Mask Compare Value Storage Register (ACMC) 524
4. Operations of the Multifunction Timer 527
4.1 Descriptions of FRT Operation 528
4.1.1 FRT Control Register 528
4.1.2 FRT Count Operation 530
4.1.3 TCCP Register Function 543
4.1.4 FRT Interrupt Operation 549
4.2 Description of OCU Operation 553
4.2.1 OCU Control Register 553
4.2.2 Independent Channel Operation 554
4.2.3 Channel-linked Operation 564
4.2.4 OCU Buffer Data Transfer 570
4.2.5 OCSE Buffer Function 572
4.3 OCU FM3 Family Product-compatible Operation 573
4.3.1 OCU FM3 Family Product-compatible Operation 573
4.4 Description of WFG Operation 574
4.4.1 WFG Control Register 574
4.4.2 List of CH_GATE Signal Output Details 575
4.4.3 List of RTO0 to RTO5 Signal Output Details 576
4.4.4 Through Mode 577
4.4.5 RT-PPG Mode 578
4.4.6 Timer-PPG Mode 579
4.4.7 RT-dead Timer Mode 582
4.4.8 RT-dead Timer Filter Mode 584
4.4.9 PPG-Dead Timer Mode 586
4.4.10 PPG-Dead Timer Filter Mode 588
4.4.11 Supplemental Explanation on Filtering Operation of Pulse Counter 590
4.4.12 Output Polarity Revered by WESA.DMOD 592
4.5 WFG FM3 Family Product-compatible Operation 596
4.5.1 WFG Operation Compatible with FM3 Family Products 596
4.6 Description of ADCMP Operation 597
4.6.1 ADCMP Control Register 597
4.6.2 Normal Mode Operation 598
4.6.3 Offset Mode Operation 603
4.6.4 ADCMP Buffer Transfer 607
4.6.5 ADC Start Linked with FRT Interrupt Mask Counter 609
4.7 ADCMP FM3 Family Product-compatible Operation 611
4.8 FRT Selection of OCU, ICU, and ADCMP 612
4.8.1 Product Mounting Two MFT's 612
4.8.2 Product Mounting Three MFT’s (other than TYPE6-M4) 614
4.8.3 Product Mounting Three MFT’s (TYPE6-M4 product) 618
4.9 PPG Timer Unit Connected to WFG 621
4.9.1 MFT unit1 621
4.9.2 MFT unit2 622
4.10 Treatment of Event Detect Register and Interrupt 623

4.10.1 List of Event Detection Registers and Interrupt Enable Registers 623
4.10.2 Configuration of Circuit 623
4.10.3 Notes When Event Detect Register of Class 1 is Cleared 626
4.10.4 Read Value Mask Function at RMW (Read Modify Write) Access 627
4.10.5 Clearing Event Detect Register in Class 2 627
5. Multifunction Timer Control Examples 628
5.1 Multifunction Timer Control Example 1 629
5.1.1 Timechart 629
5.1.2 FRT and OCU Settings and Operation 630
5.1.3 WFG Settings and Operation 631
5.1.4 ICU Settings and Operation 631
5.1.5 Completion of Process 631
5.1.6 Other Channel Processes 631
5.1.7 Details of Register Setting Values 632
5.2 Multifunction Timer Control Example 2 637
5.2.1 Timechart 637
5.2.2 FRT, OCU, and ADCMP Settings and Operation 638
5.2.3 WFG Settings and Operation 639
5.2.4 Completion of Process 639
5.2.5 Details of Register Setting Values 640
6. Detailed Timing of the Multifunction Timer Input/Output Signals 645
6.1 FRT Operation Detailed Timing When Using External Input Clock 646
6.2 OCU and WFG Operation Detailed Timing 646
6.3 ADCMP Operation Detailed Timing 648
6.4 ICU Operation Detailed Timing 649
6.5 DTTIX Input Detailed Timing 650
CHAPTER 7-1: PPG Configuration 651
1. Configuration 652
CHAPTER 7-2: PPG 655
1. Overview 656
2. Configuration and Block Diagrams of the PPG 657
2.1 PPG Circuit Block Diagram 657
3. Operations of the PPG 659
3.1 PPG Circuit Operations 660
3.1.1 PPG Operations 660
3.1.2 PPG Operation Modes 662
3.1.3 Selecting the PPG Operation Mode 665
3.1.4 Selecting the PPG Start Method 667
3.1.5 Selecting the Count Clock 668
3.1.6 Specifying the Reload Register and Pulse Width 668
3.1.7 Buffer Function of High Width Setting Reload Register 669
3.1.8 Interrupts 670
3.1.9 Polarity Reversal by REVn Register 671
3.1.10 8-bit PPG Operation Mode Example 672
3.1.11 8+8-bit PPG Operation Mode Example 673
3.1.12 16-bit PPG Operation Mode Example 675
3.1.13 16+16-bit PPG Operation Mode Example 677
3.1.14 Example of PPG Operation by GATE Signals from Multifunction Timer 680
3.2 Timing Generator Circuit Operations 681

3.2.1 Timing Generator Configuration 681
3.2.2 Timing Generator Operation Example 684
4. PPG Setup Procedure 687
4.1 Example of PPG Start by Writing to PPG Start Register 687
4.2 Example of PPG Start by GATE Signal from Multifunction Timer 688
4.3 Example of PPG Start by Timing Generator 689
5. PPG Registers 690
5.1 Timing Generator PPG Start Trigger Control Register 0 (TTCR0) 693
5.2 Timing Generator PPG Start Trigger Control Register 1 (TTCR1) 694
5.3 Timing Generator PPG Start Trigger Control Register 2 (TTCR2) 695
5.4 Timing Generator PPG Compare Register "n" (COMPn, where n=0 to 14) 696
5.5 PPG Start Register 0 (TRG0) 697
5.6 PPG Start Register 1 (TRG1) 698
5.7 Output Reverse Register 0 (REVC0) 699
5.8 Output Reverse Register 1 (REVC1) 700
5.9 PPG Operation Mode Control Register n (PPGCn n=0 to 23) 701
5.10 PPG Reload Registers n (PRLHn, PRLLn n=0 to 23) 704
5.11 Gate Function Control Registers n (GATEC0/GATEC4/GATEC8/GATEC12/GATEC16/ GATEC20) 707
6. Notes on using PPG 708
CHAPTER 8-1: Quadrature Position/Revolution Counter 709
1. Overview 710
2. Configuration 711
3. Operations 712
4. Registers 730
4.1 QPRC Position Count Register (QPCR) 731
4.2 QPRC Revolution Count Register (QRCR) 732
4.3 QPRC Position Counter Compare Register (QPCCR) 733
4.4 QPRC Position and Revolution Counter Compare Register (QPRCR) 734
4.5 QPRC Control Register (QCR) 735
4.6 QPRC Extension Control Register (QECR) 740
4.7 Low-Order Bytes of the QPRC Interrupt Control Register (QICRL) 742
4.8 High-Order Bytes of QPRC Interrupt Control Register (QICRH) 746
4.9 QPRC Maximum Position Register (QMPR) 750
4.10 AIN Noise Control Register (NFCTLA) 751
4.11 BIN Noise Control Register (NFCTLB) 752
4.12 ZIN Noise Control Register (NFRCTLZ) 753
CHAPTER 8-2: Quad Counter Position Rotation Count Display Function 755
1. Overview and Configuration 756
2. Register 757
2.1 Quad Counter Position Rotation Count Register (QPRCRR) 758
Appendixes 759
A. Register Map 760
1. Register Map 762
1.1 FLASH_IF 763
1.1.1 TYPE1-M4, TYPE2-M4 Products 763
1.1.2 TYPE3-M4 Product 764
1.1.3 TYPE4-M4, TYPE5-M4, TYPE6-M4 Products 765
1.2 Unique ID 766

1.3 ECC Capture Address 766
1.4 Clock/Reset 767
1.4.1 TYPE1-M4, TYPE2-M4 Products 767
1.4.2 TYPE3-M4, TYPE4-M4, TYPE5-M4, TYPE6-M4 Products 769
1.5 HW WDT 771
1.6 SW WDT 771
1.7 Dual_Timer 772
1.8 MFT 773
1.8.1 TYPE1-M4, TYPE2-M4 Products 773
1.8.2 TYPE3-M4, TYPE4-M4, TYPE5-M4, TYPE6-M4 Products 776
1.9 PPG 779
1.10 Base Timer 782
1.11 IO Selector for Base Timer 783
1.12 QPRC 784
1.12.1 TYPE1-M4, TYPE2-M4, TYPE6-M4 Products 784
1.12.2 TYPE3-M4, TYPE4-M4, TYPE5-M4 Products 785
1.13 QPRC NF 786
1.14 A/DC 787
1.15 CR Trim 788
1.16 EXTI 789
1.16.1 TYPE1-M4, TYPE2-M4, TYPE3-M4, TYPE4-M4 Products 789
1.16.2 TYPE5-M4, TYPE6-M4 Products 789
1.17 INT-Req. READ 790
1.17.1 TYPE1-M4, TYPE2-M4, TYPE6-M4 Products 790
1.17.2 TYPE3-M4, TYPE5-M4 Product 796
1.17.3 TYPE4-M4 Product 803
1.18 D/AC 810
1.19 HDMI-CEC 811
1.20 GPIO 812
1.20.1 TYPE1-M4, TYPE2-M4, TYPE6-M4 Products 812
1.20.2 TYPE3-M4 Product 819
1.20.3 TYPE4-M4 Product 828
1.20.4 TYPE5-M4 Product 836
1.21 LVD 845
1.22 DS_Mode 845
1.23 USB Clock 846
1.24 CAN_Prescaler 847
1.25 MFS 847
1.26 CRC 849
1.27 Watch Counter 849
1.28 RTC 850
1.28.1 TYPE1-M4, TYPE2-M4, TYPE3-M4, TYPE6-M4 Products 850
1.28.2 TYPE4-M4 Product 853
1.28.3 TYPE5-M4 Product 857
1.29 Low-speed CR Prescaler 858
1.30 Peripheral Clock Gating 859
1.30.1 TYPE1-M1, TYPE2-M4 Products 859
1.30.2 TYPE3-M4, TYPE4-M4 Products 859
1.30.3 TYPE5-M4, TYPE6-M4 Products 860

1.31 Smart Card Interface 861
1.32 MFSI2S 862
1.33 I2S Prescaler 863
1.33.1 TYPE1-M4, TYPE2-M4, TYPE3-M4 Products 863
1.33.2 TYPE4-M4 Product 864
1.34 GDC_Prescaler 865
1.35 EXT-Bus I/F 866
1.35.1 TYPE1-M4 Product 866
1.35.2 TYPE3-M4, TYPE4-M4, TYPE5-M4, TYPE6-M4 Products 869
1.36 USB 872
1.37 DMAC 874
1.38 DSTC 876
1.39 CAN 878
1.40 Ethernet-MAC 880
1.41 Ethernet-Control 880
1.42 I2S 881
1.43 SD-Card 881
1.44 CAN FD 882
1.45 Programmable-CRC 885
1.46 WorkFlash_IF 885
1.47 High-Speed Quad SPI Controller 886
1.47.1 TYPE1-M4, TYPE2-M4, TYPE3-M4 Products 886
1.47.2 TYPE4-M4 Product 889
1.48 HyperBus Interface 892
1.49 GDC Sub System Controller 893
1.50 GDC Sub System SDRAM Controller 896
B. List of Notes 897
1. Notes when High-speed CR is Used for the Master Clock 898
C. Major Changes 900
Revision History 903

CHAPTER 1: Watchdog Timer

This chapter explains the watchdog timer.

1. Overview
2. Configuration and Block Diagram
3. Operations
4. Setting Procedure Example
5. Operation Example
6. Registers
7. Usage Precautions

1. Overview

This section gives an overview of the watchdog timer.

The watchdog timer is a function to detect runaway of user programs.

If the watchdog timer is not cleared within the specified interval time, it judges that a user program is out of control, and outputs a system reset request or an interrupt request to the CPU.

This interrupt request is called a watchdog interrupt request. A reset request is called a watchdog reset request.

During watchdog timer operation, the timer must clear continually and periodically before the specified interval time has elapsed. If an abnormal operation of user program such as hanging up prevents it from being periodically cleared, it continues down counting, underflows, and outputs a watchdog interrupt request or a watchdog reset request.

This MCU has two kinds of watchdog timers as follows.

Software Watchdog Timer

- The software watchdog timer is activated by user program.
- A divided clock of the APB bus clock is used for a count clock.
- It counts cycles while the CPU program is operating and it stops counting while the APB clock is stopped in the standby mode (timer mode, stop mode, and during oscillation stabilization wait time of the source clock). The count value is retained so that it continues counting after returning from the standby mode.
- The software watchdog timer is stopped by all the resets.
- The window watchdog mode is provided.

Hardware Watchdog Timer

- The hardware watchdog timer is activated by turning on the device, and after releasing all the resets except software resets without an intervention of software.
- The hardware watchdog timer can be stopped by accessing a register with software.
- The low-speed CR clock (CLKLC) is used for a count clock.
- It counts cycles while CLKLC operats, and it stops counting while CLKLC is stopped in the standby mode (stop mode). The count value is retained so that it continues counting after returning from the standby mode.

Software/hardware Watchdog Timer

- Each watchdog timer has a lock register, accessing all the registers of watchdog timers cannot be done unless accessing and releasing a lock with a certain procedure.
- The watchdog timers can be reloaded by accessing the watchdog clear register.
- When the first underflow of the watchdog counter is generated, an interrupt request is generated. When the second underflow is generated without clearing the interrupt request, a reset request is generated. This function can be set by the register.

2. Configuration and Block Diagram

This section shows the block diagram of the watchdog timer.

Figure 2-1 Block Diagram of Software Watchdog Timer

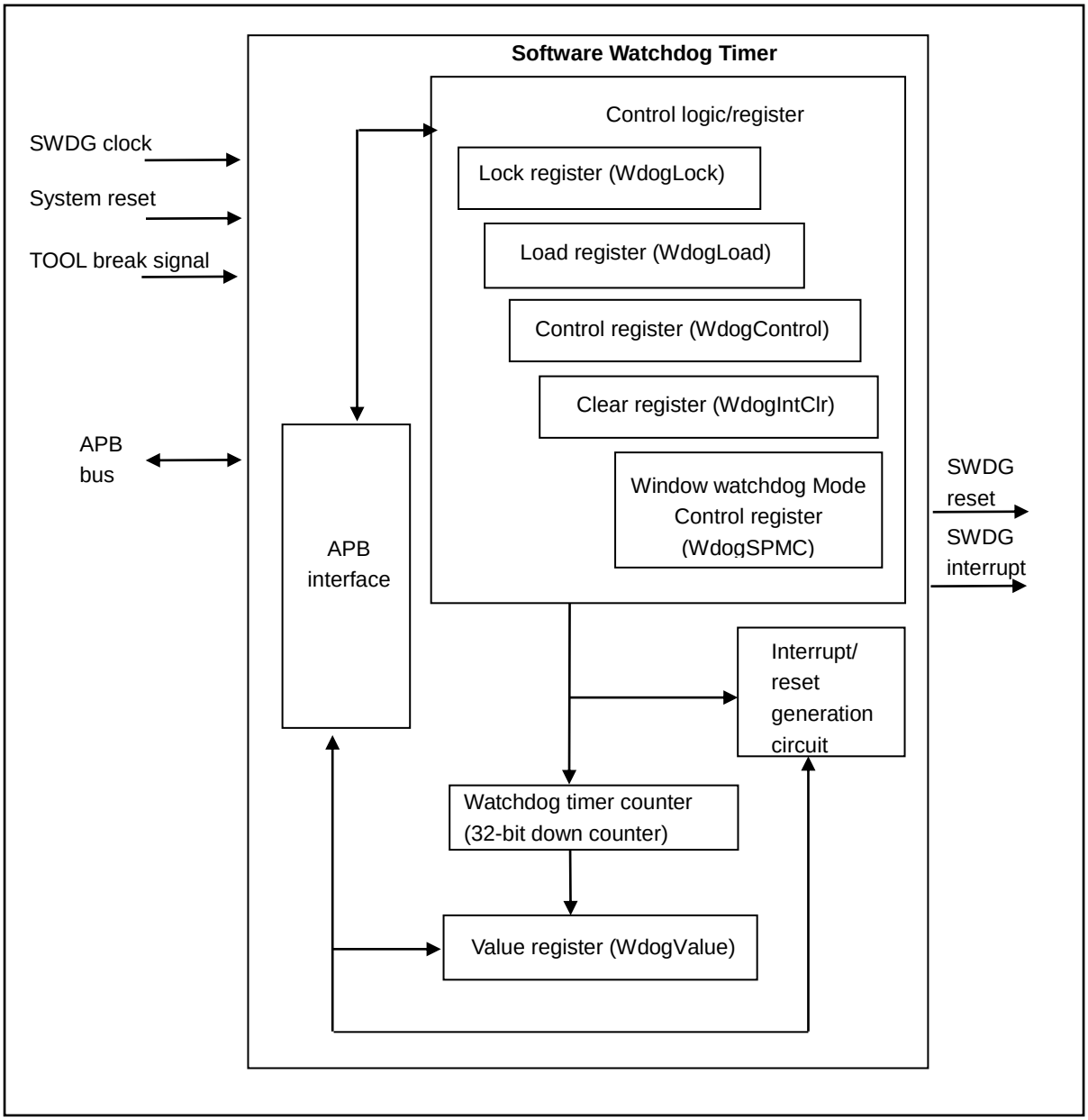
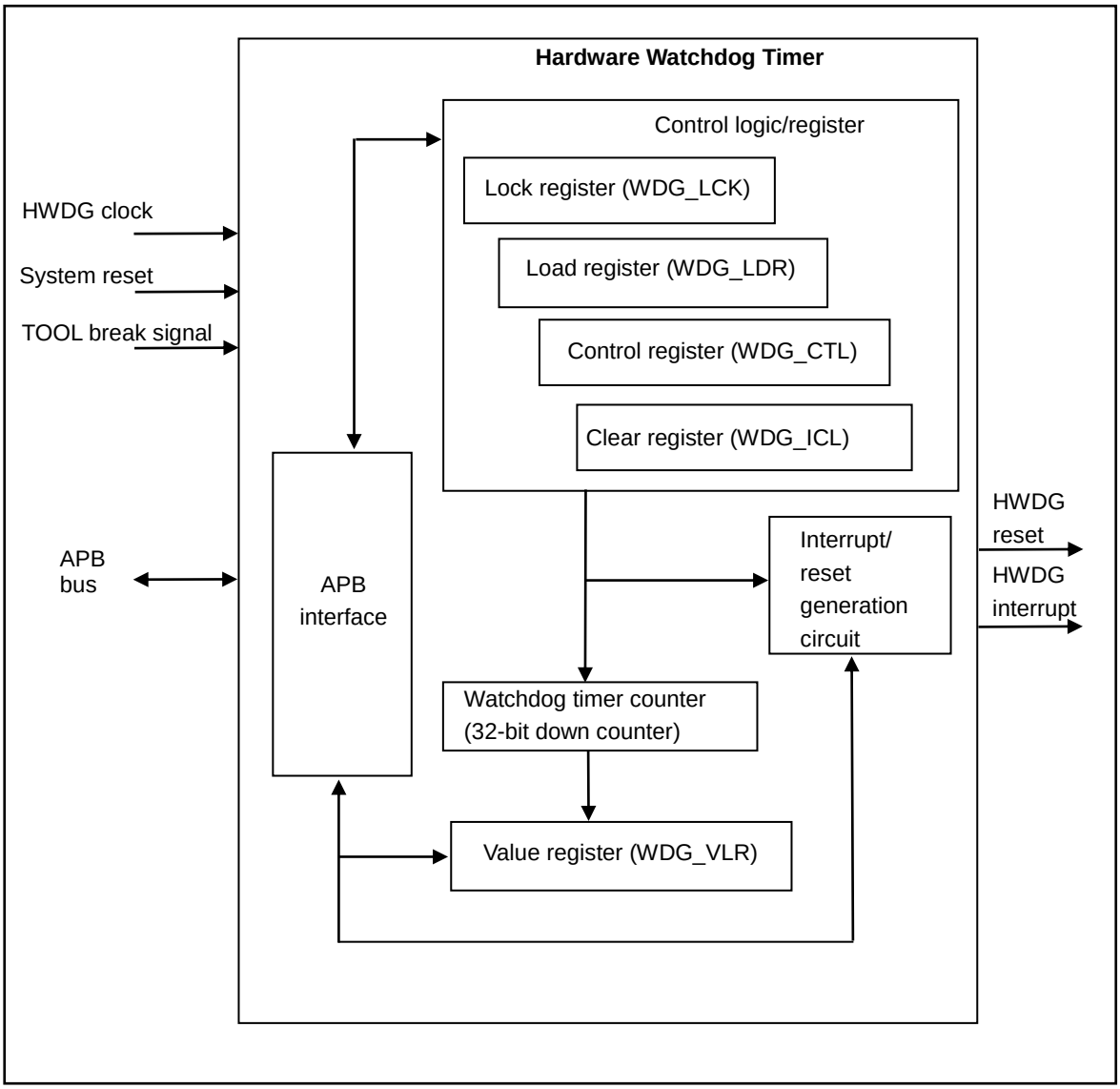


Figure 2-2 Block Diagram of Hardware Watchdog Timer



3. Operations

This section shows the configuration of the watchdog timer.

The watchdog timer consists of the following blocks.

Software Watchdog Timer

- Control register / logic

This circuit controls the software watchdog timer.
It consists of the load register, the lock register, the control register, and the clear register.

- Load register (WdogLoad)

  This register is a 32-bit register used to set count interval cycles of the software watchdog timer.
  The initial value is 0xFFFFFFFF. Table 3-1 shows the examples of interval time setting.

Table 3-1 Examples of Interval Time Setting of Software Watchdog Timer

Count Frequency	Interval Set Value	Interval Time
40 MHz	0xFFFFFFFF [initial value]	Approx. 107 s
20 MHz	0xFFFFFFFF [initial value]	Approx. 214 s
40 MHz	0x0000FFFF	Approx. 1.6 ms
20 MHz	0x0000FFFF	Approx. 3.2 ms

- Lock register (WdogLock)

  This register controls accesses to all the registers of the software watchdog timer.
  Writing a value of 0x1ACCE551 to this register enables write access to all the other registers of the software watchdog timer.

- Control register (WdogControl)

  This register sets an interrupt enable of the software watchdog, a reset enable of the software watchdog, and .a window watchdog mode enable.

- Clear register (WdogIntClr)

  This is a clear register of the software watchdog timer.
  Writing any value to the clear register reloads the value set in the load register to the counter.
  After the reloading completes, the counting is continues.

- Window Watchdog Mode Control register (WdogSPMC)

  This register sets a trigger to Window Watchdog Mode of the software watchdog timer.

■ Watchdog Timer Counter (32-bit Down Counter)

This is a 32-bit down counter. The count value is reloaded to the set value of the load register (WdogLoad) by accessing the clear register (WdogIntClr) before the counter value becomes 0 by decrementing.

Table 3-2 shows the down counter reload condition.

Table 3-2 Down Counter Reload Condition of Software Watchdog Timer

Reload Conditions
Accessing the clear register (WdogIntClr)
When the 32-bit down counter reaches 0
When the load register (WdogLoad) is modified
When the watchdog is stopped by writing INTEN=0 to the control register (WdogControl), and reactivated by writing INTEN=1

■ Value register (WdogValue)

This register can read the current counter value of the watchdog timer.

■ Interrupt and reset generation circuit

When an underflow of the watchdog timer counter is detected, a watchdog interrupt and a watchdog reset are generated due to the register setting.

- Interrupt status register (WdogRIS)

  This register shows the status of a software watchdog interrupt.

■ Activation of software watchdog timer

- Access to the control register (WdogControl), and enable the watchdog interrupt and watchdog reset.
- Table 3-3 shows the combination of watchdog interrupt and watchdog reset settings.

Table 3-3 Combination of Software Watchdog Interrupt and Reset

Interrupt	Reset	Operation
Disable	Disable	The watchdog timer is not operated
Enable	Disable	An interrupt is generated at underflow
Disable	Enable	The watchdog timer is not operated
Enable	Enable	An interrupt is generated at the first underflow A reset is generated at the second underflow [Initial setting]

Enabling an interrupt of the control register (WdogControl) becomes an activation trigger of the watchdog timer.

■ Reload and lock the software watchdog timer register

- The register has not been locked with initial condition after reset. To enable locking, write any values other than 0x1ACCE551 to the WdogLock register with software.
- When you access the clear register, write 0x1ACCE551 to the WdogLock register to release the lock.
- The value set to the load register (WdogLoad) is reloaded by writing an arbitrary value to the clear register (WdogIntClr).
- After the clear register has been accessed, it will not be automatically locked. Lock it again with software.

- Halting the software watchdog timer
  - The software watchdog timer is stopped by accessing the control register (WdogControl), and writing 0 to the watchdog interrupt enable bit.
  - The software watchdog timer is stopped by generating a reset.
- Window Watchdog Mode
  - The software watchdog timer has the Window Watchdog Mode.
  - The Window Watchdog Mode detects whether counter reload by software is implemented at the right timing.

    In the following cases, the specified event (an interrupt or reset) is issued:

  - When a counter underflow occurs.
  - When the WdogIntClr register is accessed at timing outside the timing window and the counter is cleared
  - When the WdogLoad register is accessed at a time outside the timing window and the counter is reloaded.

Hardware Watchdog Timer

- Control register / logic

This is a circuit to control the hardware watchdog timer.
It consists of the load register, the lock register, the control register, and the clear register.

- Load register (WDG_LDR)

  This register is a 32-bit register used to set count interval cycles of the hardware watchdog timer. The initial value is 0x0000FFFF (down counter for 16 bits=> approx. 655 ms @ 100 kHz (TYP)). For the frequency of CLKLC which is a count clock, see the data sheet for the product used.

- Lock register (WDG_LCK)

  This register controls the accesses of all the registers of the hardware watchdog timer. Writing a value of "0x1ACCE551" to this register enables write access to all the registers except the control register (WDG_CTL).

- Control register (WDG_CTL)

  This register sets watchdog interrupt enable and watchdog reset enable. To access this register, write 0x1ACCE551 to the lock register, and also write 0xE5331AAE to the lock register. If you don’t write the correct value after writing 0x1ACCE551, repeat the process from the beginning.

- Clear register (WDG_ICL)

  This is a clear register of the hardware watchdog timer.
  By writing an arbitrary 8-bit value and its reversed value in series, the timer counter is reloaded with the value stored in the load register and its counting is continues.

- Watchdog Timer Counter (32-bit down counter)

This is a 32-bit down counter. The count value is reloaded with the set value of the load register (WDG_LDR) by accessing the clear register (WDG_ICL) before the counter value decrements to "0".

Table 3-4 shows the down counter reload condition.

Table 3-4 Down Counter Reload Condition of Hardware Watchdog Timer

Reload Conditions
Accessing the clear register (WDG_ICL)
When the 32-bit down counter reaches "0"
When the load register (WDG_LDR) is modified
When the watchdog is stopped by writing INTEN=0 to the control register (WDG_CTL), and reactivated by writing INTEN=1

- Value register (WDG_VLR)

This register can read the current counter value of the watchdog timer. However, during tool break, a correct value can be read when the watchdog timer stopps. Except during a tool break, an inaccurate value may be read due to asynchronous reading. In this case, you must read the value twice and then compare the two.

- Interrupt and reset generation circuit

When an underflow of the watchdog timer counter is detected, a watchdog interrupt and a watchdog reset are generated according to the register setting.

- Interrupt status register (WDG_RIS)

  This register shows the status of a hardware watchdog interrupt.

- Activation of hardware watchdog timer

- Writing 0x1ACCE551 to the lock register (WDG_LCK) and then writing a reversal value "0xE5331AAE" to it enables access to the control register (WDG_CTL).
- Access the control register (WDG_CTL) and enable the watchdog interrupt and the watchdog reset.

Table 3-5 shows the combination of watchdog interrupt and watchdog reset settings.

Table 3-5 Combination of Hardware Watchdog Interrupt and Reset

Interrupt	Reset	Operation
Disable	Disable	The watchdog timer is disabled
Enable	Disable	An interrupt is generated at underflow
Disable	Enable	The watchdog timer is disabled
Enable	Enable	An interrupt is generated at the first underflow A reset is generated at the second underflow [Initial setting]

Enabling an interrupt of the control register (WDG_CTL) is an activation trigger of the hardware watchdog timer.

- Reload and lock the hardware watchdog timer register

  The set value is reloaded from the load register to the 32-bit down counter by writing a value to the clear register (WDG_ICL). After reloading, the register is locked again.
  Unlock is required to access the clear register each time hereafter.

- Stopping the hardware watchdog timer
  - Writing 0x1ACCE551 to the lock register (WDG_LCK) and then writing a reversal value 0xE5331AAE to it enables access to the control register (WDG_CTL).
  - The hardware watchdog timer is stopped by accessing the control register (WDG_CTL) and writing 0 to the watchdog interrupt enable bit.

Differences between Software Watchdog Timer and Hardware Watchdog Timer

Table 3-6 shows the major differences between software watchdog timer and hardware watchdog timer.

Table 3-6 Differences between Software Watchdog Timer and Hardware Watchdog Timer

	Software Watchdog	Hardware Watchdog
Count clock	Divided clock of APB	CLKLC
Read value of the value register	Synchronous reading Reading possible	Asynchronous reading Only during a tool break can a correct value be read. Otherwise during a tool break, an inaccurate value may be read.
Initial value of watchdog interrupt setting and reset setting Initial value	Disable (No watchdog operation)	Enable (Watchdog operation)
Register lock function initial state	No lock (Software locks after activation)	Lock (Hardware locks from the activation)
Releasing lock	Writing 0x1ACCE551 to lock register to release all locks for the registers	Writing 0x1ACCE551 to lock register to release all locks for the registers except WDG_CTL
WdogControl/ WDG_CTL register Releasing separate locks	None	Writing 0xE5331AAE to lock register to release the locks of the WDG_CTL register
Relock conditions	Writing a value other than "0x1ACCE551" to the lock register locks all the registers again.	After releasing lock for the registers except WDG_CTL, the lock is resumed under any of the following conditions: – Writing a value other than "0x1ACCE551" or "0xE5331AAE" to WDG_LCK – Writing to WDG_LDR – Writing to WDG_CTL – Writing to WDG_ICL again
		After releasing lock for the registers including WDG_CTL, lock is resumed under any of the following conditions: – Writing a value other than "0x1ACCE551" to WDG_LCK – Writing to WDG_LDR – Writing to WDG_ICL – Writing to WDG_CTL
Initial value of load register	0xFFFFFFFF	0x0000FFFF
Bit number of clear register	32 bits	8 bits
Clear register access	Clear by writing an arbitrary value	Clear by writing an arbitrary value, and then writing a reversed value of the arbitrary value
Window Watchdog Mode	Available	None

4. Setting Procedure Example

This section shows how to set the watchdog timer.

Software Watchdog Timer

Figure 4-1 Software Watchdog Timer Setting Procedure (1)

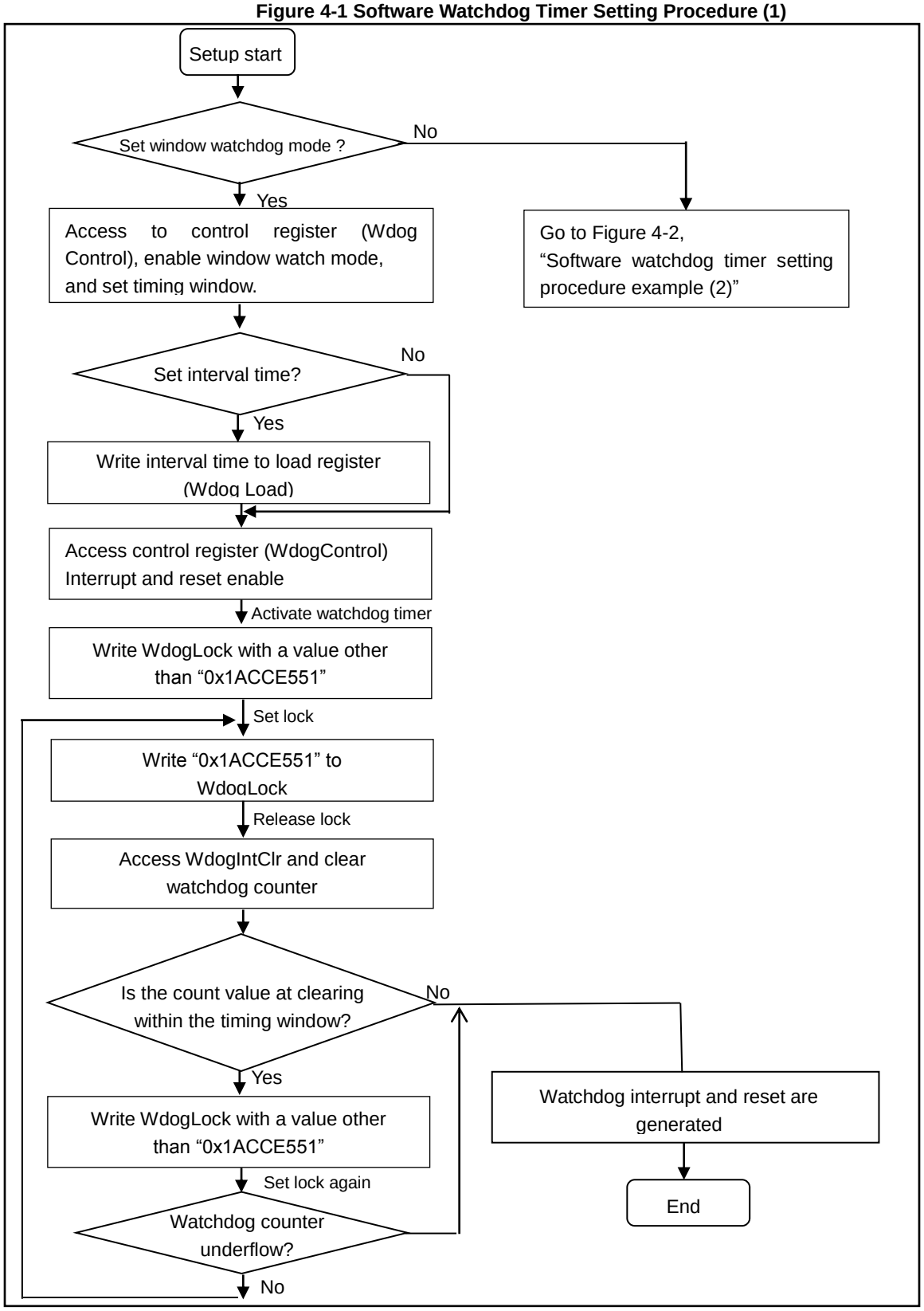
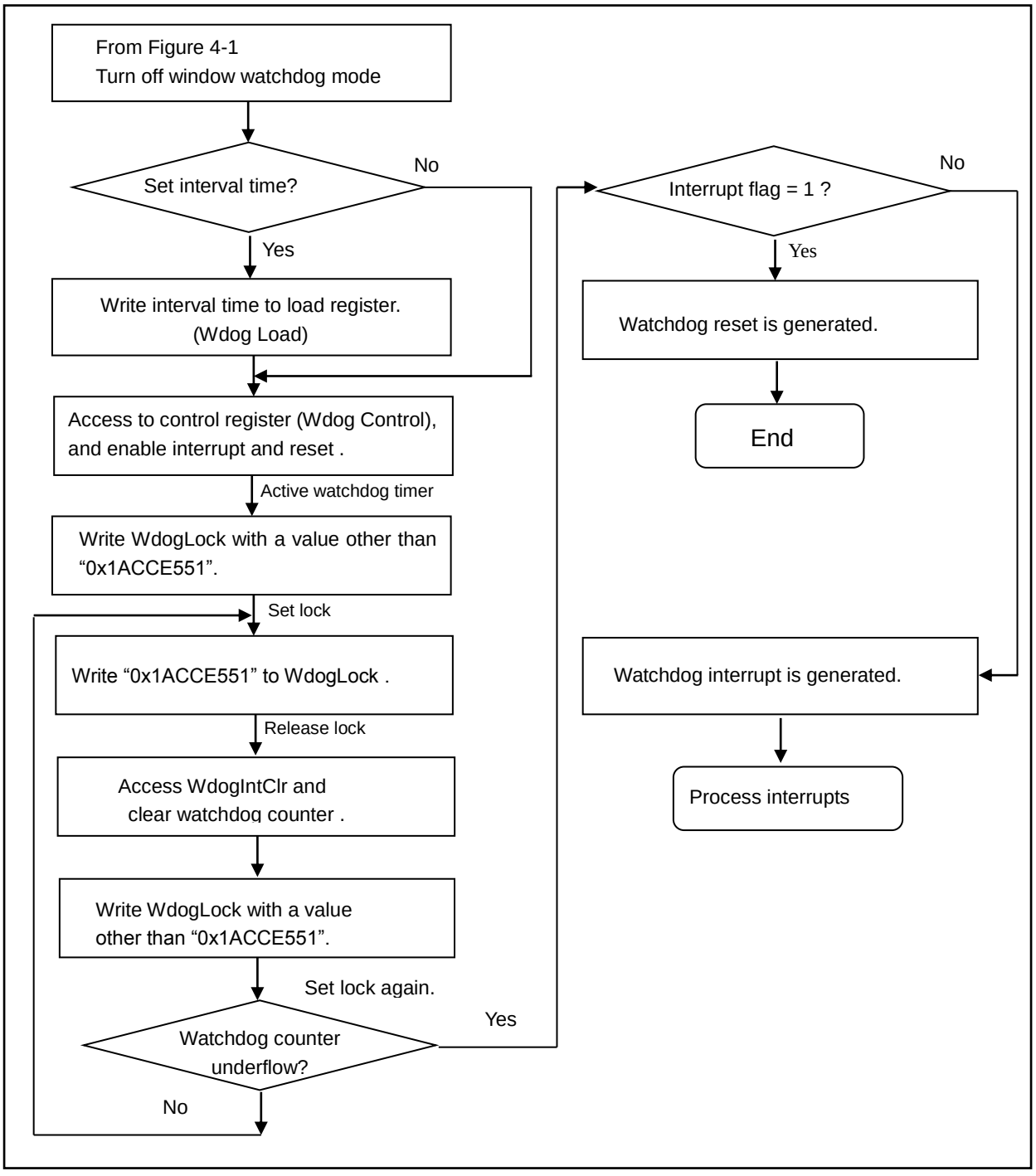
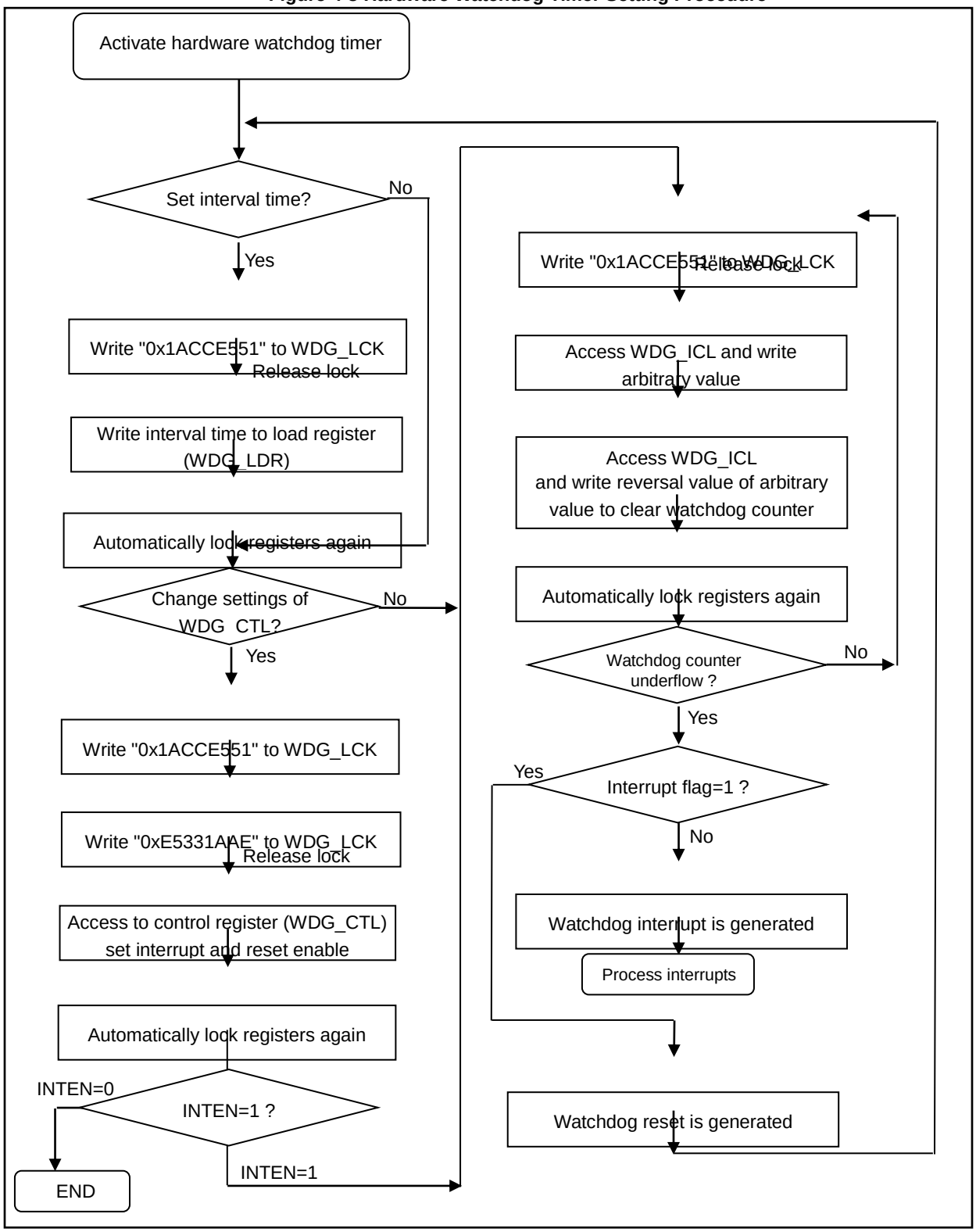


Figure 4-2 Software Watchdog Timer Setting Procedure (2)



Hardware Watchdog Timer

Figure 4-3 Hardware Watchdog Timer Setting Procedure

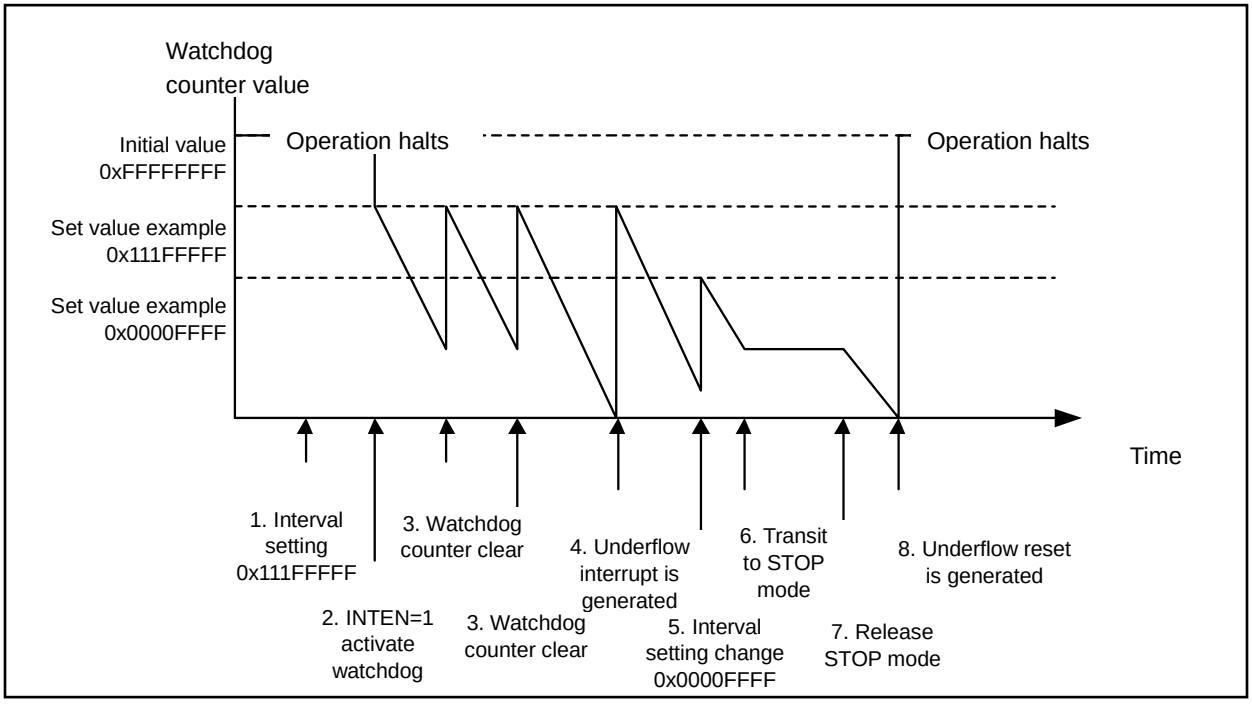


5. Operation Example

This section shows the operation of the watchdog timers.

Software Watchdog Timer

Figure 5-1 Operation Example of the Software Watchdog Timer

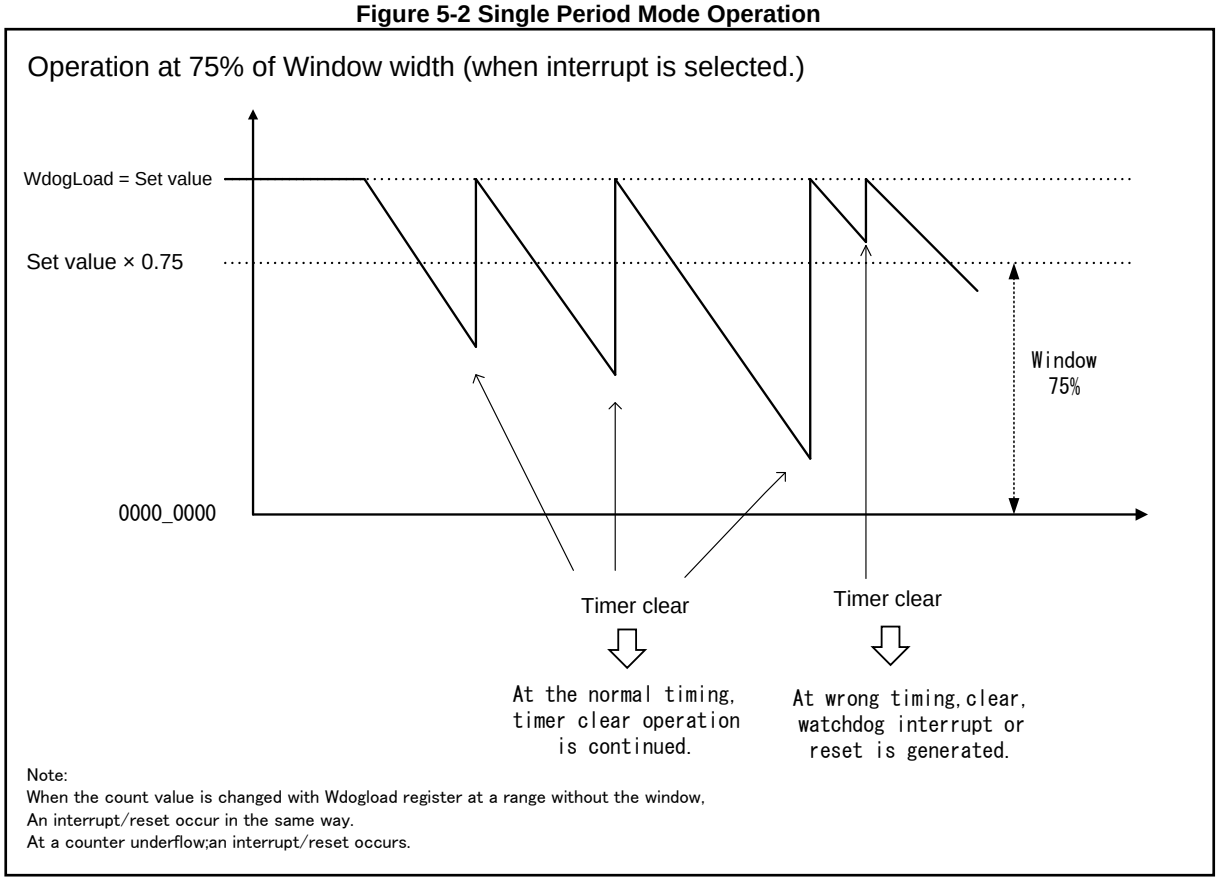


Note:

- *Before accessing each register, unlock the lock register as the above example shows. This operation is omitted. Also, this operation is not in window watchdog mode.*

1. Set SWC_PSR and WdogControl registers before activation.
   Write the set value to WdogLoad register to set the interval time.
   The interval time is not reflected because the watchdog is not activated. The count value is the initial value.
2. Access the WdogControl register and write 1 to the INTEN bit to activate the watchdog.
   At this time, the interval time is reflected and decrementing will be started from the value set in 1.
3. Write an arbitrary value to WdogIntClr register to clear the watchdog counter.
   At this time, the set value is the value set in 2.
4. When the counter is not cleared this time, an interrupt is generated at an underflow.
   At this time, the down counter set value is the value set in 2.
5. Access the WdogLoad register to change the interval time.
   At this time the down counter value is cleared to be to the set value.
6. Transfers to STOP mode. Thus, the software watchdog stops.
7. Clears STOP mode. The down counter is restarted. But, the counter value is not cleared.
   Note: After the oscillation stabilization wait is completes and the base clock operation is starts, the down count is restarts.
8. When WdogIntClr register is not accessed and the interrupt flag is not cleared, a software watchdog reset is generated if the second underflow occurs.
   Due to the reset occurrence, the software watchdog timer operation is stopped.

Figure 5-2 Single Period Mode Operation



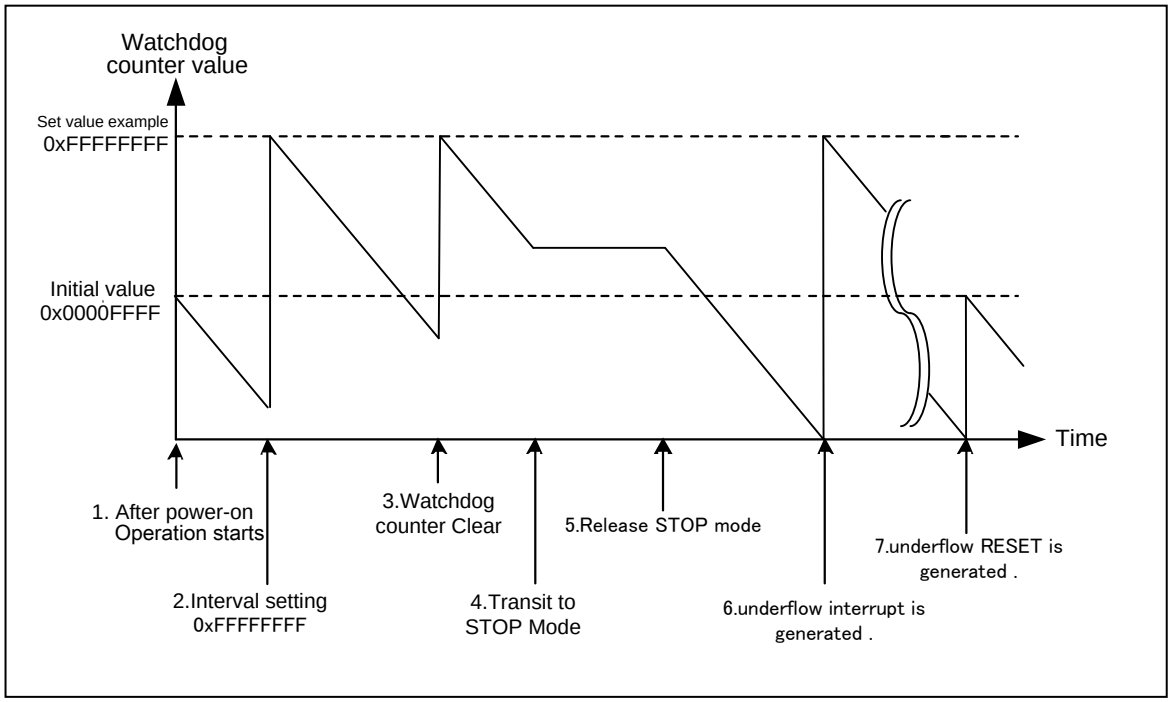
1. Before power-on, set SWC_PSR and WdogControl registers.
   Write the setting value to WdogLoad register and set an interval.
   Set the SPM and TWD bits of WdogControl. At this time, INTEN must be 0.
   Because of the power-on, the interval time is not reflected. The count value becomes the initial value.
   Set WdogSPMC register and set the trigger type in window watchdog mode.
2. Write 1 to INTEN bit of the WdogControl register to start the watchdog.
   Then, the interval time is reflected and the count down begins from the value set in 1.
3. Write an arbitrarily value to the WdogClr register to execute the watchdog counter clear.
   When the cleared timer value is within the set window value (in the above operation example, 75% or less): the clear is executed at the normal timing and the counter value becomes the value set in 1. To continue the operation.
4. Access to WdogClr to write an arbitrary value and execute watchdog counter clear.
   When the cleared timer value is without the set window value (in the above operation example, more than 75%):
   The clear is executed at the anomalous timing and the watchdog timer generates the interrupt/reset set in 1.
5. When an interrupt occurs, the watchdog timer continues its operation (in the above example).
   When a reset occurs, the watchdog timer stops its operation.

Note:

- *Release of the lock register is required to access each register. It is omitted in the operation example.*

Hardware Watchdog Timer

Figure 5-3 Hardware Watchdog Timer Operation



1. After power-on, the hardware watchdog timer is started.
   The count value is the initial value (0x0000FFFF).
2. Access to WDG_LDR register to change the interval time.
   At this time, the down count value will be cleared to the set value.
3. Write an arbitrary value to WDG_ICL register, and the write the reversal value of the arbitrary value to clear the watchdog counter.
   At this time, the set value will be the value set in 2.
4. Transit to Stop mode. The hardware watchdog will be stopped by this.
5. Release Stop mode. The down counter restarts. The count value is not cleared.
   (Note) Decrementing will be restarted after CLKLC oscillation is starts, and HWDG clock is input to restart the down count.
6. Without clearing the counter, an interrupt will be generated at underflow.
   At this time, the set value of the down counter will be the value set in 2.
7. A hardware watchdog reset will be generated when the second underflow is generated without clearing the interrupt flag by accessing the WDG_ICL register.
   The count value is returned to the initial value and decrementing is restarted.

Note:

- *Release of the lock register is required to access each register. It is omitted in the operation example.*

6. Registers

This section explains the clock generation registers.

Table 6-1 List of Registers for the Watchdog Timer

Abbreviated Register Name	Register Name	Reference
WdogLoad	Software watchdog timer load register	6.1
WdogValue	Software watchdog timer value register	6.2
WdogControl	Software watchdog timer control register	6.3
WdogIntClr	Software watchdog timer clear register	6.4
WdogRIS	Software watchdog timer interrupt status register	6.5
WdogSPMC	Software watchdog timer window watchdog mode control register	6.6
WdogLock	Software watchdog timer lock register	6.7
WDG_LDR	Hardware watchdog timer load register	6.8
WDG_VLR	Hardware watchdog timer value register	6.9
WDG_CTL	Hardware watchdog timer control register	6.10
WDG_ICL	Hardware watchdog timer clear register	6.11
WDG_RIS	Hardware watchdog timer interrupt status register	6.12
WDG_LCK	Hardware watchdog timer lock register	6.13

6.1 Software Watchdog Timer Load Register (WdogLoad)

The WdogLoad register sets the cycle of the software watchdog timer.

Register configuration

bit	31	0
Field	WdogLoad	
Attribute	R/W	
Initial value	0xFFFFFFFF	

Register function

[bit31:0] WdogLoad: Interval cycle setting bits

bit31:0	Explanation
In case of writing	Sets the cycle of the software watchdog. The initial value is 0xFFFFFFFF. The minimum value for writing is "0x00000001". When "0x00000000" is written, an interrupt will be generated. (A reset may be generated immediately depending on setting.)
In case of reading	A set value can be read. The initial value 0xFFFFFFFF is read.

Notes:

- *During watchdog timer operation, if the value of WdogLoad is modified, the value of WdogLoad will be reflected to the timer counter, and counting is continued.*
- *While the watchdog timer stops, if the value of WdogLoad is modified, the value of WdogLoad will be reflected to the timer counter at activation of the watchdog timer.*

6.2 Software Watchdog Timer Value Register (WdogValue)

The WdogValue register can read the current counter value of the software watchdog timer.

Register configuration

bit	31	0
Field	WdogValue	
Attribute	R	
Initial value	0xFFFFFFFF	

Register function

[bit31:0] WdogValue: Counter value bits

bit31:0	Explanation
In case of writing	No effect on the operation. .
In case of reading	The count value of the current watchdog counter is read. The initial value 0xFFFFFFFF is read if reading before activation.

Note:

- *See "5.13 Debug Break Watchdog Timer Control Register (DBWDT_CTL)" in the Clock chapter of the peripheral manual for the setting of watchdog timer at tool break.*

6.3 Software Watchdog Timer Control Register (WdogControl)

The WdogControl register sets enable/disable of the software watchdog timer.

Register configuration

bit	7	6	5	4	3	2	1	0
Field	Reserved			SPM	TWD		RESEN	INTEN
Attribute	-			R/W	R/W		R/W	R/W
Initial value	-			0	00		0	0

Register function

[bit7:5] Reserved: Reserved bits

"0b000" is read from these bits.

Write only “0b000”.

[bit4]SPM: Software Watchdog window watchdog mode enable bit

Bit		Explanation
Read		Register value is read.
Write	0	A window watchdog mode is disabled.
Write	1	A window watchdog mode is enabled.

Notes:

- *When INTEN=1, writing to this bit is disabled.During INTEN=0, write to this bit.*
- *At INTEN=1, writing to the INTEN bit and this bit at the same time is valid*
  At INTEN=0, writing to the INTEN bit and this bit at the same time is invalid.

[bit3:2] TWD: Software watchdog timing window setting bit

Bit		Explanation
Read		Register value is read.
Write	00	At the period of WdogLoad or less, reload is enabled.
Write	01	At the period of 75% or less of WdogLoad, reload is enabled.
Write	10	At the period of 50% or less of WdogLoad, reload is enabled.
Write	11	At the period of 25% or less of WdogLoad, reload is enabled.

Notes:

- *Only when SPM=1, this bit is effective.*
- *When INTEN=1, writing to this bit is disabled.During INTEN=0, write to this bit.*
- *At INTEN=1, writing to the INTEN bit and this bit at the same time is valid*
  At INTEN=0, writing to the INTEN bit and this bit at the same time is invalid.

[bit1] RESEN : Software watchdog reset enable bit

bit		Description
Read		Register value is read.
Write	0	A watchdog reset is disabled.
Write	1	A watchdog reset is enabled.

Note:

- *At SPM=1, the setting of this bit is invalid.*

[bit0] INTEN : Interrupt and counter enable bit of the software watchdog

bit		Description
Read		Register value is read.
Write	0	A watchdog interrupt is disabled. A watchdog counter is disabled.
Write	1	A watchdog interrupt is enabled. A watchdog counter is enabled.

Notes:

- *By writing 1 to the INTEN bit, the watchdog counter loads the interval cycle value from WdogLoad and the software watchdog timer is activated.*
- *Writing 0 to the INTEN bit stops the watchdog counter. The watchdog counter reloads the cycle value from WdogLoad when 1 is written again and reactivated.*
- *The watchdog timer can be activated by enabling INTEN bit only. The watchdog timer is not activated by enabling the RESEN bit only. To activate the watchdog timer, the INTEN bit should be enabled. See "3. Operations" for details.*
- *Writing 0 to the INTEN bit clears the interrupt flag in the software watchdog timer interrupt status register (WdogRIS).*

6.4 Software Watchdog Timer Clear Register (WdogIntClr)

The WdogIntClr register clears the software watchdog timer.

Register configuration

bit	31	0
Field	WdogIntClr	
Attribute	R/W	
Initial value	0xXXXXXXXX	

Register function

[bit31:0] WdogIntClr : clear bits

bit31:0	Description
Read	An undefined value is read.
Write	Writing an arbitrary value Clears an interrupt of the watchdog timer, if an interrupt of the watchdog timer is generated. Reloads the set value from the WdogLoad register to the watchdog timer counter.

6.5 Software Watchdog Timer Interrupt Status Register (WdogRIS)

The WdogRIS register shows the interrupt status of the software watchdog timer.

Register configuration

bit	7	1	0
Field	Reserved		RIS
Attribute	-		R
Initial value	-		0

Register function

[bit7:1] Reserved: Reserved bits

0b0000000 is read from these bits.

Write only “0b0000000”.

[bit0] RIS: Software watchdog interrupt status bit

bit		Description
Write		No effect on the operation.
Read	0	A watchdog interrupt has not generated.
Read	1	A watchdog interrupt has generated.

6.6 Software Watchdog Timer Window Watchdog Mode Control Register (WdogSPMC)

WdogSPMC register controls the software watchdog timer window watchdog mode.

Register configuration

Bit	7	1	0
Field	Reserved		TGR
Attribute	-		R/W
Initial value	-		0

Register function

[bit7:1] Reserved : Reserved bits

0b0000000 is read from these bits.

Write only “0b0000000”.

[bit0] TGR : Software watchdog trigger type bit

bit		Description
Read		Register value is read.
Write	0	In the following conditions, an interrupt is generated: When an counter underflow is generated When a counter clear (WdogIntClr write) is generated outside the timing window When a counter reload (WdogLoad write) is generated outside the timing window
Write	1	In the following conditions, a reset is generated: When a counter underflow is generated When a counter clear (WdogIntClr write) is generated outside the timing window When a counter reload (WdogLoad write) is generated outside the timing window

Note:

- *Only when SPM=1 is this bit effective.*
  When setting TGR=1, a reset is generated as an event regardless of the setting of RESEN bit of WdogControl.

6.7 Software Watchdog Timer Lock Register (WdogLock)

The WdogLock register controls accesses of all the registers of software watchdog timer.

Register configuration

bit	31	0
Field	WdogLock	
Attribute	R/W	
Initial value	0x00000000	

Register function

[bit31:0] WdogLock : Software watchdog lock register

bit31:0	Explanation
Write	Writing 0x1ACCE551: Releases locks of all the registers of software watchdog timer. Writing other than 0x1ACCE551: Lock function for all of the software watchdog timer registers will be enabled.
Read	0x00000000 : The locks are released. 0x00000001 : The locks are not released.

Notes:

- *Lock for initial values are not enabled. Enable lock function after the software watchdog timer is started.*
- *After lock is released, the software watchdog timer clear register (WdogIntClr) will become accessible.*
- *After accessing the clear register (WdogIntClr), the lock will not be automatically enabled. Incorporate "lock release -> clear -> lock enable" for any clear sequence.*
- *When accessing each register of the hardware watchdog while the locks are not released, reading is enabled and the values of each register can be read. Writing is ignored.*

6.8 Hardware Watchdog Timer Load Register (WDG_LDR)

The WDG_LDR register sets the cycle of hardware watchdog timer.

Register configuration

bit	31	0
Field	WDG_LDR	
Attribute	R/W	
Initial value	0x0000FFFF	

Register function

[bit31:0] WDG_LDR : Interval cycle setting bits

bit31:0	Explanation
Write	Sets the cycle of the hardware watchdog. The initial value is 0x0000FFFF. The minimum value of writing is 0x00000001. An interrupt is generated when 0x00000000 is written.
Read	A set value can be read. The initial value 0x0000FFFF is read.

Notes:

- *During watchdog timer operation, if the value of WDG_LDR is modified, the value of WDG_LDR is reflected to the timer counter and counting continues.*
- *During a watchdog timer halt, if the value of WDG_LDR is modified, the value of WDG_LDR is reflected to the timer counter at activation of the watchdog timer.*
- *If the WDG_LDR register is modified while the watchdog timer interrupt generates, the watchdog timer interrupt is cleared.*
- *This register cannot be cleared by a software reset or a software watchdog reset.*

6.9 Hardware Watchdog Timer Value Register (WDG_VLR)

The WDG_VLR register can read the current counter value of the hardware watchdog timer.

Register configuration

bit	31	0
Field	WDG_VLR	
Attribute	R	
Initial value	0xXXXXXXXX	

Register function

[bit31:0] WDG_VLR : Counter value bits

bit31:0	Explanation
Read	The count value of the current watchdog counter can be read. By turning on the power, the hardware watchdog automatically activates, therefore decrementing starts at the time of reading. The value after power on or the value decremented from the initial value 0x0000FFFF is read.
Write	No effect on the operation.

Notes:

- *This register cannot be cleared by software reset or software watchdog reset.*
- *Reading a correct value of this register is possible only if the watchdog timer stops at a tool break. See "5.13 Debug Break Watchdog Timer Control Register (DBWDT_CTL)" in the chapter of Clock in the peripheral manual for the setting of the watchdog timer at tool break. Except during a tool break, an inaccurate value may be read due to asynchronous reading. In this case, you must read the value twice and then compare the two.*

6.10 Hardware Watchdog Timer Control Register (WDG_CTL)

The WDG_CTL register sets enable/disable of the hardware watchdog timer.

Register configuration

bit	7	2	1	0
Field	Reserved		RESEN	INTEN
Attribute	-		R/W	R/W
Initial value	-		1	1

Register function

[bit7:2] Reserved : Reserved bits

0b000000 is read from these bits.

Write only “0b000000” to these bits.

[bit1] RESEN: Hardware watchdog reset enable bit

bit		Explanation
Read		The value of register is read.
Write	0	A watchdog reset is disabled.
Write	1	A watchdog reset is enabled.

[bit0] INTEN: Hardware watchdog interrupt and counter enable bit

bit		Explanation
Read		The value of the register is read.
Write	0	A watchdog interrupt is disabled. A watchdog counter is disabled.
Write	1	A watchdog interrupt is enabled. A watchdog counter is enabled.

Notes:

- *Writing 0 to the INTEN bit stops the watchdog counter. When writing 1 again, the watchdog counter reloads the cycle value from WDG_LDR register to activate the counter.*
- *The watchdog timer can be activated by enabling the INTEN bit only. The watchdog timer is not activated by enabling RESEN bit only. To activate the watchdog timer, INTEN bit must be enabled.*
- *To access this register, write 0x1ACCE551 to the hardware watchdog timer lock register (WDG_LCK), and also write the reversal value 0xE5331AAE to release lock.*
- *This register cannot be cleared by a software reset or a software watchdog reset*
- *Writing 0 to the INTEN bit clears the interrupt flag in hardware watchdog timer interrupt status register (WDG_RIS).*

6.11 Hardware Watchdog Timer Clear Register (WDG_ICL)

The WDG_ICL register clears the hardware watchdog timer.

Register configuration

bit	7	0
Field	WDG_ICL	
Attribute	R/W	
Initial value	0xXX	

Register function

[bit7:0] WDG_ICL: clear bits

bit7:0	Explanation
Read	Undefined value is read.
Write	Writing an arbitrary 8-bit value, and then write a reversal value of the arbitrary value, Clears a watchdog timer interrupt if an interrupt of watchdog timer was generated. Reloads the set value from the WDG_LDR register to the watchdog timer counter.

Note:

- *This register cannot be cleared by a software reset or a software watchdog reset.*

6.12 Hardware Watchdog Timer Interrupt Status Register (WDG_RIS)

The WDG_RIS register shows the interrupt status of the hardware watchdog timer.

Register configuration

bit	7	1	0
Field	Reserved		RIS
Attribute	-		R
Initial value	-		0

Register function

[bit7:1] Reserved: Reserved bits

0b0000000 is read from these bits.

In case of writing, set 0b0000000.

[bit0] RIS: Hardware watchdog interrupt status bit

bit		Explanation
Write		No effect on the operation.
Read	0	Hardware watchdog interrupt is not generated.
Read	1	Hardware watchdog interrupt is generated.

Note:

- *This register cannot be cleared by a software reset or a software watchdog reset.*

6.13 Hardware Watchdog Timer Lock Register (WDG_LCK)

The WDG_LCK register controls accesses of all the registers of the hardware watchdog timer.

Register configuration

bit	31	0
Field	WDG_LCK	
Attribute	R/W	
Initial value	0x00000001	

Register function

[bit31:0] WDG_LCK : Hardware watchdog lock register

bit31:0	Explanation
Write	Writing 0x1ACCE551: The locks of all the registers other than the control register are released. Later, in case of writing the reversal value, 0xE5331AAE: The locks of all the registers are released. In case another procedure is performed or writing any value other than the above0x1ACCE551: The locks of all the registers will be enabled.
Read	0x00000000: The locks are released. 0x00000001: The locks are not released.

Notes:

- *This register cannot be cleared by a software reset or a software watchdog reset.*
- *In case of accessing to each register of the hardware watchdog when the locks are not released, reading is enabled and the values of each register can be read. Writing is ignored.*

7. Usage Precautions

The section explains the precautions when using the watchdog timer.

- Hardware watchdog timer clear register

To clear the hardware watchdog, write an arbitrary 8-bit value, and then write a reversal value of the arbitrary value. Clearing cannot be performed unless the correct reversal value is written. Even if clearing is not performed, the register locks again.

- Cooperation with a debug tool

When a tool break is applied by a debug tool, continuing or stopping the watchdog timer counter can be controlled by the register setting. See the chapter Clock in the peripheral manual for details about the behavior of the watchdog timers during debugging.

- Operation at standby mode

Writing to a key register is required at the setting of the standby mode. Not stopping the watchdog timer for transition to standby mode may cause an unintended program operation.
See the chapter Low Power Consumption Mode in the peripheral manual for more details.

Generation of a watchdog reset can be confirmed by the reset source register. See the section 4.1 Reset Cause Register (RST_STR: ReSeT Status Register) in the chapter Reset in Peripheral Manual for more details.

- For an interrupt factor, see the section 3.3 EXC02 Batch Read Register (EXC02MON) and 3.5 IRQ001 Batch Read Register (IRQ001MON) in the chapter Interrupts in the peripheral manual.

- Use a divided clock of APB clock for the count clock of the software watchdog.

See the chapter Clock in the peripheral manual for divided clock setting of the count clock.

- Hardware watchdog and interrupt handler

Before releasing the Lock for WDG_CTL (after releasing the Lock for the register other than WDG_CTL), if another interrupt becomes effective by the hardware watchdog and the interrupt handler begins its processing, the Lock releasing count can not be detected by hardware.
So, at the beginning of the interrupt handler, write values in the WDG_LCK register to lock the register.

CHAPTER 2: Dual Timer

This chapter explains the Dual Timer functions and operations.

1. Overview
2. Configuration
3. Operations
4. Setting Procedure Example
5. Registers

1. Overview

The Dual Timer consists of two programmable 32-/16-bit down counters. An interrupt is generated when the counter reaches zero.

Dual Timer Overview

The Dual Timer consists of two programmable Free Run Counters. Each timer block operates identically. The Free Run Counters can be programmed for 32-bit or 16-bit counter size by the Control register. Also, any one of the following three timer modes can be selected:

- Free-running mode
  The counter operates continuously and wraps around to its maximum value each time that it reaches zero.
- Periodic mode
  The counter is reloaded from the Load register and operates continuously each time that it reaches zero.
- One-shot mode
  Writing to the Load register (TimerXLoad) loads the counter with a new value. The counter halts until it is reprogrammed when the counter reaches zero.

Two Free Run Counters operate in the common timer clock (TIMCLK). The APB bus clock (PCLK) is used as the timer clock. Also, each Free Run Counter has a prescaler that can divide by 1, 16, or 256. Therefore, the count rate of each Free Run Counter can be controlled by each prescaler.

Writing to the Load register (TimerXLoad) loads the counter with the timer count value. If the timer counter is enabled, the timer decrements at the rate determined in the timer clock and in the prescaler setting. When the timer counter has been running, writing to the Load register restarts the counter immediately with a new value.

An alternative way of loading the timer count is to write to the Background Load register (TimerXBGLoad). In this way, the current count value is not affected immediately after the writing, and the counter continues to decrement. Then, in the case where the counter reaches zero, the timer counter is reloaded with a new load value if it is in Periodic mode.

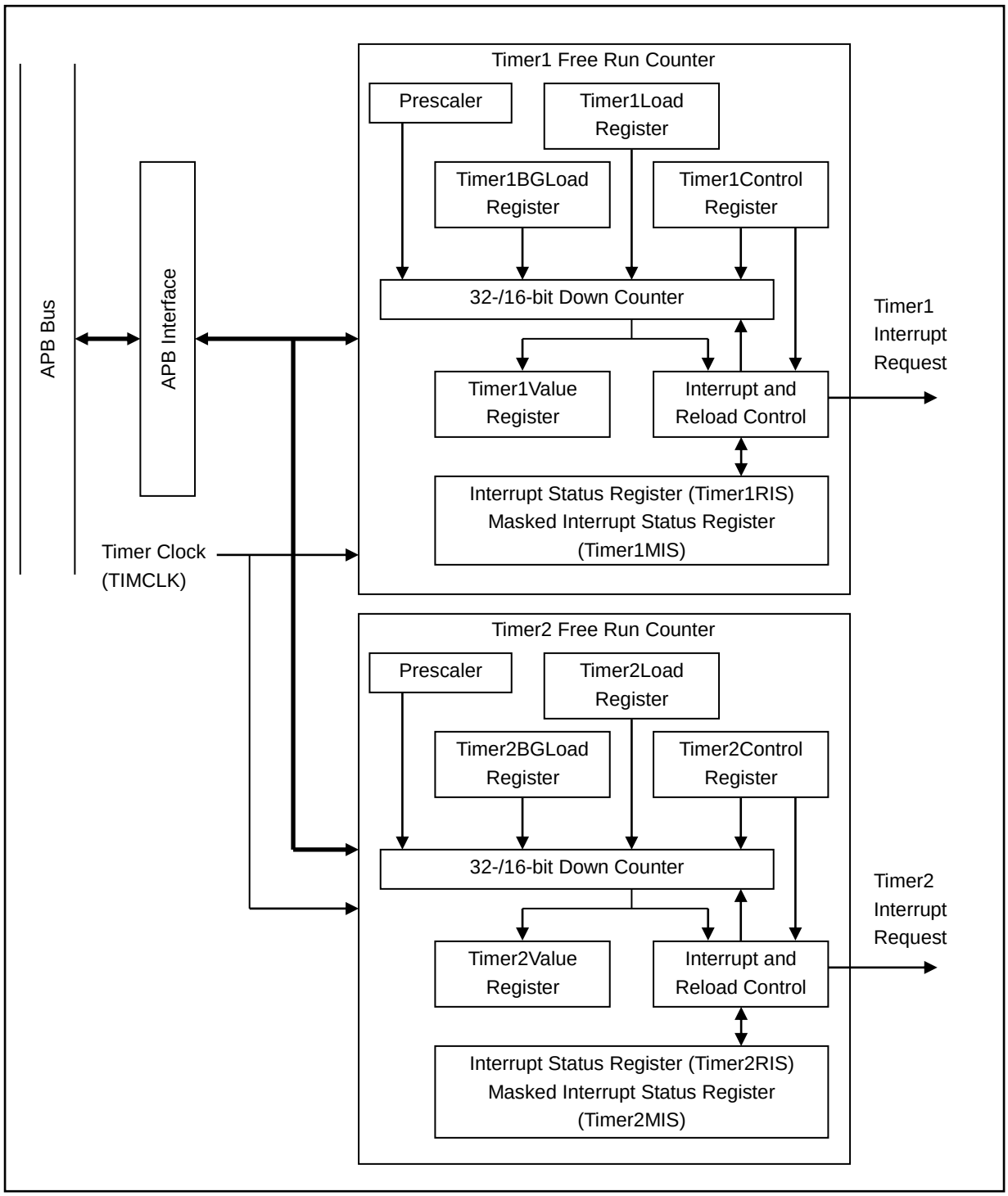
When the timer count reaches zero, an interrupt is generated. Writing to the Interrupt Clear register (TimerXIntClr) clears the interrupt. Also, the interrupt output signal can be masked by the Interrupt Mask register.

The current count value can be read from Value register at any time.

2. Configuration

This section illustrates the Dual Timer configuration.

Figure 2-1 Dual Timer Block Diagram



3. Operations

This section explains Dual Timer operations.

3.1. Timer Operating Mode
3.2. Initial State
3.3. Interrupt Operation

3.1 Timer Operating Mode

Operating modes are selected from three timer modes based on the settings of the Control register (TimerXControl)'s mode bit (TimerMode) and one-shot mode bit (OneShot).

Table 3-1 Mode Selection Table

TimerMode	OneShot	Selective Mode
0	0	Free-running mode
1	0	Periodic mode
-	1	One-shot mode

Timer size bit (TimerSize) of the Control register is used to appropriately configure 32-bit or 16-bit counter operation.

Note:

- *The character X in a register name in this chapter indicates either register of Free Run Counter 1 or 2.*

Free-running Mode

When a reset is performed, the timer value is initialized to 0xFFFFFFFF. Then, if the counter is enabled, the count decrements by one at the timer clock (TIMCLK) rising edge. Alternatively, writing to the Load register (TimerXLoad) loads a new initial counter value. Then, if the counter is enabled, the counter starts to decrement from this loaded value.

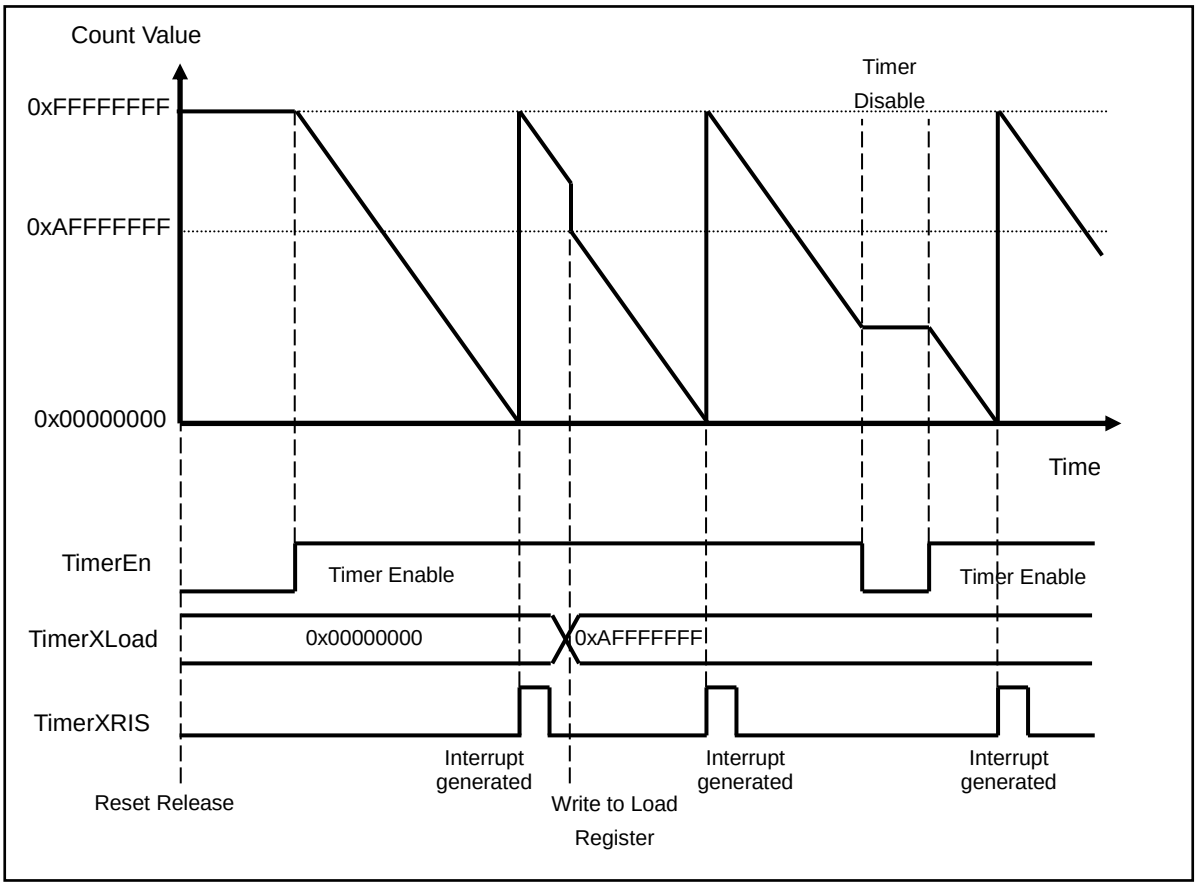
In 32-bit mode, when the count reaches zero (0x00000000), an interrupt is generated. Then, regardless of the Load register's value, the counter wraps around to 0xFFFFFFFF. The counter starts to decrement again, and as long as the counter is enabled, this whole cycle is repeated.

In 16-bit mode, only the lower 16 bits of the counter are decremented. When the count reaches 0x0000, an interrupt is generated. Then, regardless of the Load register's value, the counter wraps around to 0xFFFF.

If the Enable bit (TimerEn) of the Control register (TimerXControl) is cleared and the counter is disabled, the counter halts and holds the current value. If the counter is enabled again, the counter continues to decrement from the current value.

The counter value can be read from the Value register (TimerXValue) at any time.

Figure 3-1 Free-running Mode Operation (32-bit Mode)



Periodic Mode

Writing to the Load register (TimerXLoad) loads an initial counter value. Then, the counter starts to decrement from this value if the counter is enabled.

In 32-bit mode, all 32 bits of the counter are decremented. Then, when the count reaches zero (0x00000000), an interrupt is generated. The counter reloads the Load register value. The counter starts to decrement again. As long as the counter is enabled, this whole cycle is repeated.

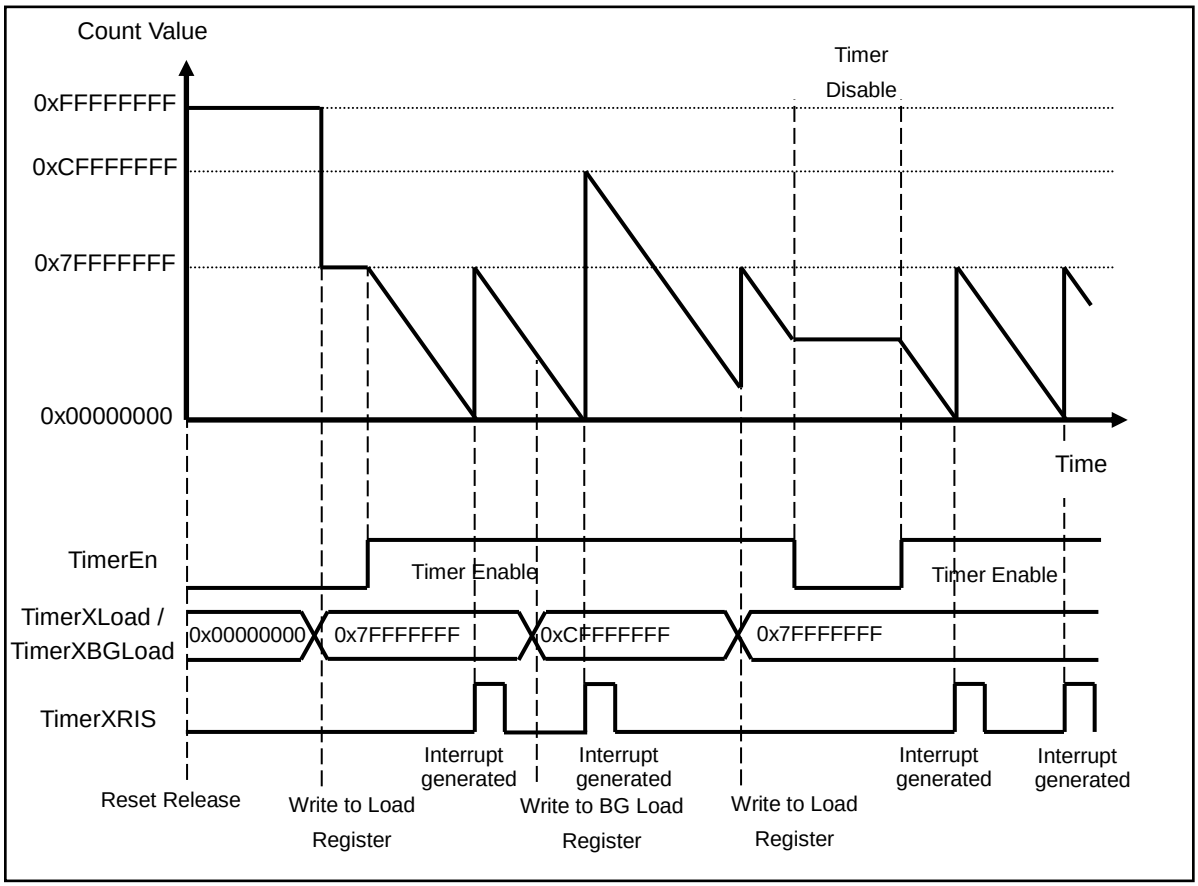
In 16-bit mode, only the lower 16 bits of the counter are decremented. When the count reaches 0x0000, an interrupt is generated. Then, the counter reloads the Load register value. The counter starts to decrement again. As long as the counter is enabled, this whole cycle is repeated.

When a new value is written to the Background Load register (TimerXBGLoad) while the counter is running, the value of the Load register is also updated to the same value. However, the counter continues to decrement to zero. When the counter reaches zero, it reloads the new value. As long as the Timer is set to Periodic Mode, this new load value is used for each subsequent reload.

When a new value is written to the Load register for loading the value to the counter while the counter is running, the counter value is changed to the new load value at the next timer clock.

If the Enable bit (TimerEn) of the Control register (TimerXControl) is cleared and the counter is disabled, the counter halts and holds the current value. If the counter is enabled again, the counter continues to decrement from the current value.

Figure 3-2 Periodic Mode Operation (32-bit Mode)



One-shot Mode

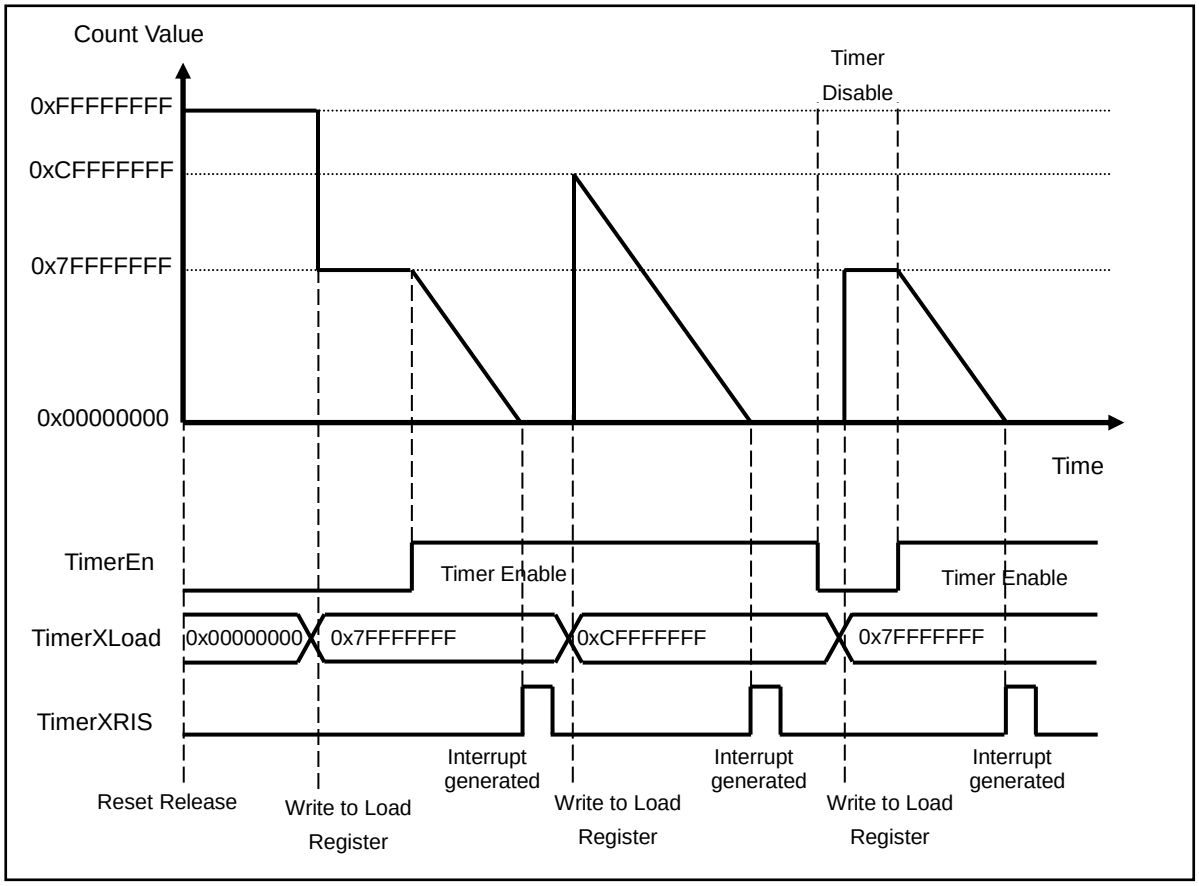
To start the count down sequence in One-shot Mode, a new load value is written to the Load register (TimerXLoad). If the counter is enabled, it starts to decrement from this value.

In 32-bit mode, all 32 bits of the counter are decremented. Then, when the count reaches zero (0x00000000), an interrupt is generated. Then, the counter halts.

In 16-bit mode, only the lower 16 bits of the counter are decremented. When the count reaches 0x0000, an interrupt is generated. Then, the counter halts.

In One-shot mode, writing a new value to the Load register starts the counter again. Then, the counter value is changed to the new load value at the next timer clock.

Figure 3-3 One-shot Mode Operation (32-bit Mode)



3.2 Initial State

After the reset, the timer is initialized as shown below:

- Timer counter disabled
- Free-running mode selected
- 16-bit counter mode selected
- Prescaler in the setting of dividing by 1
- Interrupt clear and interrupt enable states
- Load register set to zero
- Counter value set to 0xFFFFFFFF

3.3 Interrupt Operation

This section explains interrupt operation.

An interrupt is generated when the counter reaches 0x00000000 (in 32-bit mode) or 0xXXXX0000 (in 16-bit mode) in the setting of interrupt enable (IntEnable=1). In 16-bit mode, the upper 16 bits of the counter are ignored.

Writing to Interrupt Clear register (TimerXIntClr) clears an interrupt.

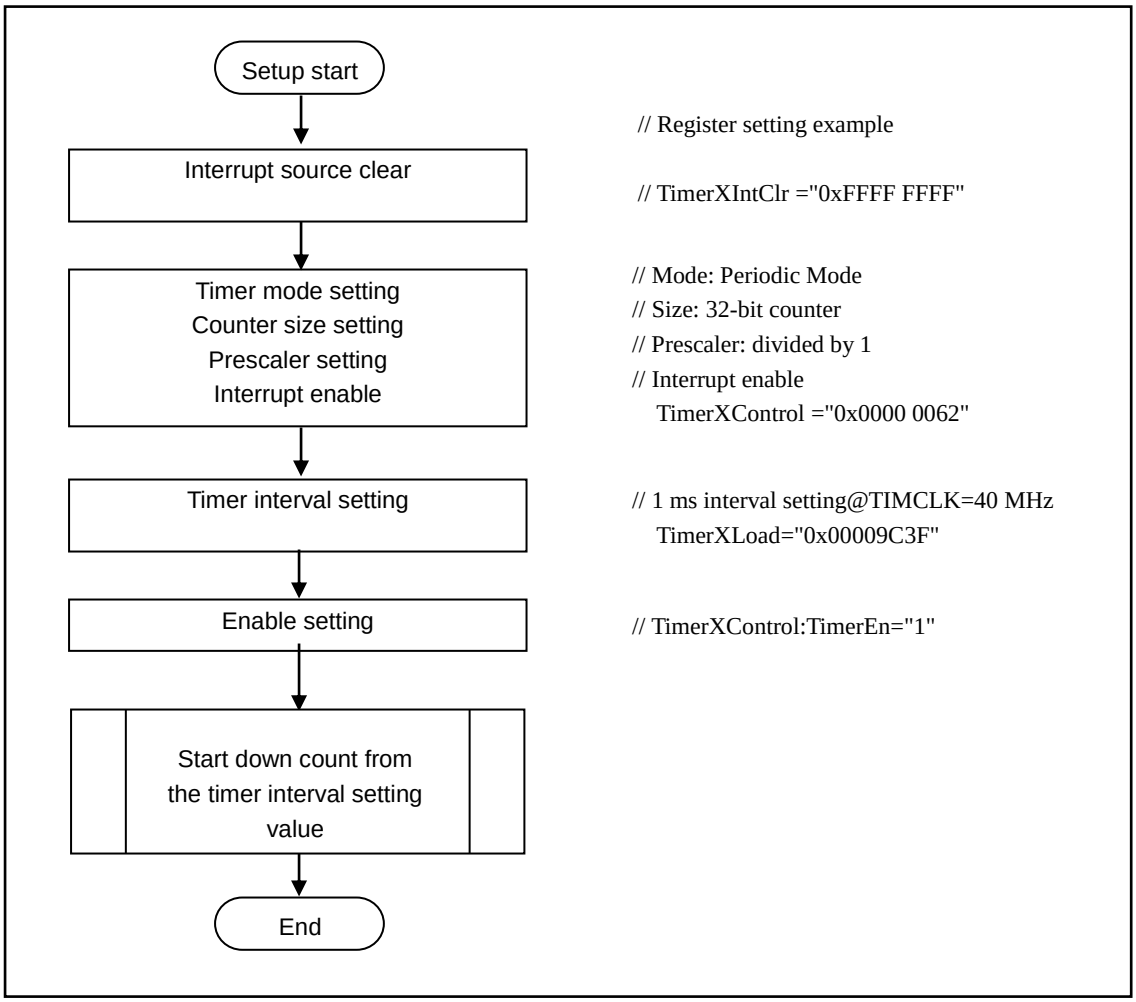
The interrupt signals generated in the Timer module can be masked when the Interrupt Enable bit (IntEnable) of the Control register (TimerXControl) is set to "0". The raw interrupt state before being masked can be read from the Interrupt Status register (TimerXRIS). Also, the masked interrupt state can be read from Masked Interrupt Status register (TimerXMIS).

4. Setting Procedure Example

This section describes an example of the Dual Timer setting procedure.

Dual Timer Setting Procedure Flow

Figure 4-1 Periodic Mode Setting Procedure



Timer Interval Setting

Expressions of the timer interval calculations in respective modes are shown in Table 4-1:

Table 4-1 Expression for Timer Interval Calculation

Mode	Timer Interval
32-bit Free-running	$(PRESCALE_{DIV} / TIMCLK_{FREQ}) \times 2^{32}$
16-bit Free-running	$(PRESCALE_{DIV} / TIMCLK_{FREQ}) \times 2^{16}$
Periodic & One-shot	$(PRESCALE_{DIV} / TIMCLK_{FREQ}) \times$ (TimerXLoad + 1)

- $TIMCLK_{FREQ}$ is the timer clock (TIMCLK) frequency.
- $PRESCALE_{DIV}$ is the prescaler division factor of 1, 16, or 256 configured by bit3:2 of the Control register (TimerXControl).
- TimerXLoad is the value of the Load register (TimerXLoad).

For example, in the case of $TIMCLK_{FREQ}$=40 MHz and $PRESCALE_{DIV}$=1, the value of the Load register (TimerXLoad) to configure a 1ms timer interval can be calculated as follows:

$$\begin{aligned} \text{TimerXLoad} &= \text{Timer interval} \times TIMCLK_{FREQ} / PRESCALE_{DIV} - 1 \\ &= 1\ \text{ms} \times 40\ \text{MHz} / 1 - 1 = 4 \times 10^4 - 1 = 0\text{x}00009\text{C}3\text{F} \end{aligned}$$

Note:

- *The minimum valid value of the Load register (TimerXLoad) is 0x00000001. If the Load register is set to 0x00000000, an interrupt will be immediately generated.*

5. Registers

This section explains the structures and functions of the registers used in Dual Timer.

Dual Timer Register List

Abbreviation	Register Name	Reference
Timer1Load	Timer1 Load register	5.1
Timer1Value	Timer1 Value register	5.2
Timer1Control	Timer1 Control register	5.3
Timer1IntClr	Timer1 Interrupt Clear register	5.4
Timer1RIS	Timer1 Interrupt Status register	5.5
Timer1MIS	Timer1 Masked Interrupt Status register	5.6
Timer1BGLoad	Timer1 Background Load register	5.7
Timer2Load	Timer2 Load register	5.1
Timer2Value	Timer2 Value register	5.2
Timer2Control	Timer2 Control register	5.3
Timer2IntClr	Timer2 Interrupt Clear register	5.4
Timer2RIS	Timer2 Interrupt Status register	5.5
Timer2MIS	Timer2 Masked Interrupt Status register	5.6
Timer2BGLoad	Timer2 Background Load register	5.7

5.1 Load Register (TimerXLoad) X=1 or 2

The Load register (TimerXLoad) set a start value to decrement the counter in 32-bit register.

bit	31															16
Field	TimerXLoad[31:16]															
Attribute	R/W															
Initial value	0x0000															

bit	15															0
Field	TimerXLoad[15:0]															
Attribute	R/W															
Initial value	0x0000															

[bit31:0] TimerXLoad: Timer X Load bits

When a value is directly written to this register, the current count is immediately set to a new value at the next timer clock. Also, in Periodic mode setting, this value is used for reloading the counter when the current count reaches zero.

In addition, the value in this register is also overwritten when the Background Load register (TimerXBGLoad) is written. However, in this case, the current count is not immediately affected.

After either the Load register (TimerXLoad) or the Background Load register (TimerXBGLoad) is written, the register value written last is returned at any reading. In other words, the same value is read from both of the Load register and the Background Load register, and the value is always reloaded after the counter reaches zero in Periodic Mode.

Note:

- *The minimum valid value of the Load register (TimerXLoad) is "0x00000001". If the Load register is set to "0x00000000", an interrupt will be immediately generated.*

5.2 Value Register (TimerXValue) X=1 or 2

The Value register (TimerXValue) indicates the current value of the decrement counter in 32-bit Read Only register.

bit	31															16
Field	TimerXValue[31:16]															
Attribute	R															
Initial value	0xFFFF															

bit	15															0
Field	TimerXValue[15:0]															
Attribute	R															
Initial value	0xFFFF															

[bit31:0] TimerXValue: Timer X Value bits

After a load operation in which a new load value is written to the Load register (TimerXLoad), the new load value is reflected immediately to this Value register (TimerXValue).

Note:

- *In 16-bit timer mode, the upper 16 bits of the 32-bit Value register (TimerXValue) are not automatically set to "0x0000". For example, when no writing to the Load register (TimerXLoad) has occurred yet since the change in the Timer from 32-bit mode to 16-bit mode, the upper 16 bits of the Value register have non-zero values.*

5.3 Control Register (TimerXControl) X=1 or 2

The Control register (TimerXControl) controls the Timer.

bit	31															16
Field	Reserved															
Attribute	-															
Initial value	0xXXXX															

bit	15	8	7	6	5	4	3	2	1	0
Field	Reserved		Timer En	Timer Mode	Int Enable	Reserved	TimerPre		Timer Size	One Shot
Attribute	-		R/W							
Initial value	0xXX		0	0	1	0	00		0	0

[bit31:8] Reserved: Reserved bits

These bits have no effect in write mode.
The read value is undefined.

[bit7] TimerEn: Enable bit

Bit	Description
0	Timer disabled [Initial value]
1	Timer enabled

[bit6] TimerMode: Mode bit

bit	Description
0	Free-running Mode [Initial value]
1	Periodic Mode

[bit5] IntEnable: Interrupt enable bit

Bit	Description
0	Interrupt disabled
1	Interrupt enabled [Initial value]

[bit4] Reserved: Reserved bit

This bit has no effect in write mode.
The read value is undefined.

[bit3:2] TimerPre: Prescale bits

bit3	bit2	Description
0	0	Clock divided by 1 [Initial value]
0	1	Clock divided by 16
1	0	Clock divided by 256
1	1	Setting is prohibited

[bit1] TimerSize: Counter size bit

Select 16/32-bit counter operation.

bit	Description
0	16-bit counter [Initial value]
1	32-bit counter

[bit0] OneShot: One-shot mode bit

Select One-shot Mode or Counter Wrapping Mode (Free-running Mode/Periodic Mode). Based on Mode bit (TimerMode) settings, Free-running Mode or Periodic Mode is selected.

Bit	Description
0	Wrapping Mode (Free-running Mode/Periodic Mode) [Initial value]
1	One-shot Mode

Note:

- *The counter mode, size, or prescale settings must not be changed while the Timer is running. To configure a new setting, the Timer must be disabled first and then a new setting value needs to be written to respective registers. Then, after the setting is changed, the Timer must be enabled again. Failure to follow this setting procedure can result in unpredictable behaviors of the device.*

5.4 Interrupt Clear Register (TimerXIntClr) X=1 or 2

The Interrupt Clear register (TimerXIntClr) clears an interrupt.

bit	31															16
Field	TimerXIntClr[31:16]															
Attribute	W															
Initial value	0xXXXX															

bit	15															0
Field	TimerXIntClr[15:0]															
Attribute	W															
Initial value	0xXXXX															

[bit31:0] TimerXIntClr : Interrupt clear bits

Writing any value to this register clears an interrupt output from the counter.

5.5 Interrupt Status Register (TimerXRIS) X=1 or 2

The Interrupt Status register (TimerXRIS) indicates an unmasked and raw interrupt status.

bit	31															16
Field	Reserved															
Attribute	-															
Initial value	0xXXXX															

bit	15														1	0
Field	Reserved															Timer XRIS
Attribute	-															R
Initial value	XXXXXXXXXXXXXX															0

[bit31:1] Reserved: Reserved bits

These bits have no effect in write mode.

The read value is undefined.

[bit0] TimerXRIS: Interrupt Status Register bit

bit	Description
0	No interrupt generated from the counter [Initial value]
1	Interrupt generated from the counter

5.6 Masked Interrupt Status Register (TimerXMIS) X=1 or 2

The Masked Interrupt Status register (TimerXMIS) indicates the masked interrupt status.

bit	31															16
Field	Reserved															
Attribute	-															
Initial value	0xXXXX															

bit	15														1	0
Field	Reserved															Timer XMIS
Attribute	-															R
Initial value	XXXXXXXXXXXXXXX															0

[bit31:1] Reserved: Reserved bits

These bits have no effect in write mode.
The read value is undefined.

[bit0] TimerXMIS: Masked Interrupt Status bit

This bit is a logical AND value of the Raw Interrupt Status and the Timer Interrupt Enable bit (IntEnable) of the Control register (TimerXControl). The same value as this bit is connected to the interrupt output signal.

bit	Description
0	No interrupt generated from the counter [Initial value]
1	Interrupt generated from the counter

5.7 Background Load Register (TimerXBGLoad) X=1 or 2

The Background Load register (TimerXBGLoad) is a 32-bit register having a value which the counter starts to decrement.

bit	31															16
Field	TimerXBGLoad[31:16]															
Attribute	R/W															
Initial value	0x0000															

bit	15															0
Field	TimerXBGLoad[15:0]															
Attribute	R/W															
Initial value	0x0000															

[bit31:0] TimerXBGLoad : Background Load bits

This register is used to reload the counter when the current count reaches zero in Periodic Mode setting. This is not used in Free-running Mode or One-shot Mode.

Writing to this register reloads the counter differently from the writing to the Load register (TimerXLoad). The difference is as follows. Writing to the Load register immediately starts the counter with the new value; however, writing to this register does not immediately restart the counter with the new value.

After a value is written to either the Load register or the Background Load register (TimerXBGLoad), the register value written last is returned at any reading. In other words, the same value is read from the Load register (TimerXLoad) and the Background Load register (TimerXBGLoad), and the value is always reloaded after the counter reaches zero in Periodic Mode.

CHAPTER 3-1: Watch Counter Prescaler

This chapter explains the functions and operations of the watch counter prescaler.

1. Overview of Watch Counter Prescaler
2. Configuration of Watch Counter Prescaler
3. Explanation of Operations and Setting Procedures of the Watch Counter Prescaler
4. Registers of Watch Counter Prescaler

1. Overview of Watch Counter Prescaler

The watch counter prescaler is a prescaler that generates a counter clock used for a watch counter.

Watch Counter Prescaler

This is a prescaler that generates a count clock of the watch counter.

The watch counter prescaler can select a main clock, a sub clock, high-speed CR, or CLKLC as an input clock (F_{CL}). The watch counter prescaler outputs the division clocks (WCCK0 to WCCK3) shown in Table 1-1 by setting the output clock selection bit (SEL_OUT[2:0]) of the clock selection register (CLK_SEL).

Table 1-1 Division Clocks Generated by the Watch Counter Prescaler

SEL_OUT[2:0]	WCCK3	WCCK2	WCCK1	WCCK0
000	$2^{15}/F_{CL}$	$2^{14}/F_{CL}$	$2^{13}/F_{CL}$	$2^{12}/F_{CL}$
001	$2^{25}/F_{CL}$	$2^{24}/F_{CL}$	$2^{23}/F_{CL}$	$2^{22}/F_{CL}$
010	$2^{4}/F_{CL}$	$2^{3}/F_{CL}$	$2^{2}/F_{CL}$	$2/F_{CL}$
011	$2^{8}/F_{CL}$	$2^{7}/F_{CL}$	$2^{6}/F_{CL}$	$2^{5}/F_{CL}$
100	$2^{12}/F_{CL}$	$2^{11}/F_{CL}$	$2^{10}/F_{CL}$	$2^{9}/F_{CL}$
101	$2^{19}/F_{CL}$	$2^{18}/F_{CL}$	$2^{17}/F_{CL}$	$2^{16}/F_{CL}$
110	$2^{23}/F_{CL}$	$2^{22}/F_{CL}$	$2^{21}/F_{CL}$	$2^{20}/F_{CL}$

SEL_OUT[2:0]: Output clock selection bit of clock selection register (CLK_SEL)
F_{CL}: Frequency of input clock

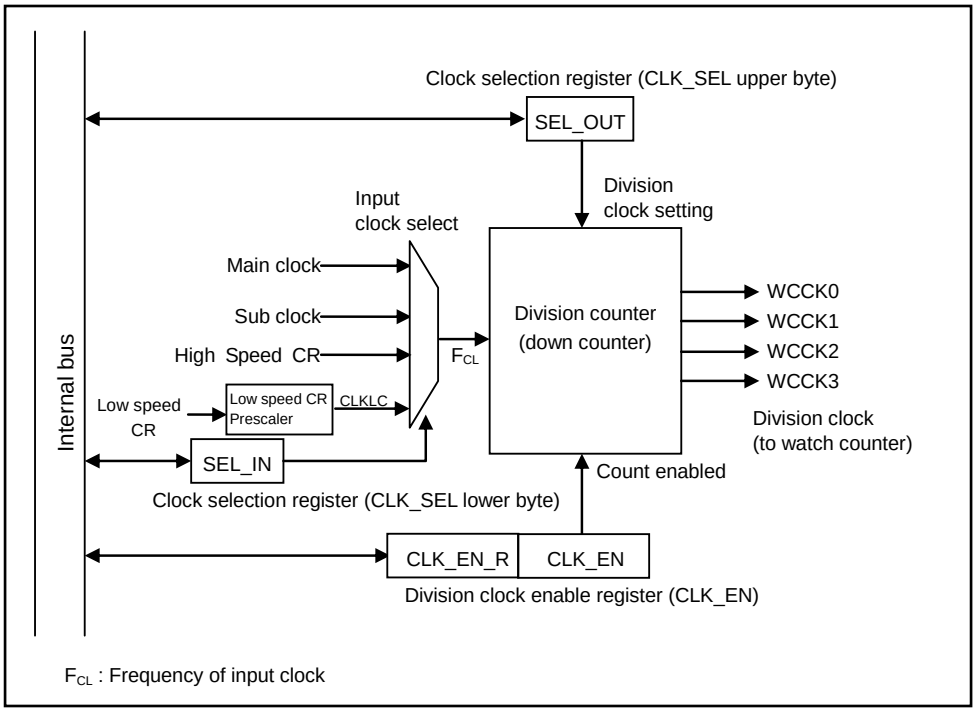
Note:

- *CLKLC is a clock that is obtained by dividing low-speed CR by CR prescaler.*

2. Configuration of Watch Counter Prescaler

This section shows the block diagram of the watch counter prescaler.

Figure 2-1 Block Diagram of Watch Counter Prescaler



- Clock selection register (CLK_SEL)

  This register selects the input clock (F_{CL}) that inputs the division counter, and sets the division clocks (WCCK0 to WCCK3) that output.

- Division clock enable register (CLK_EN)

  This register enables counting down of the division counter.
  There is a delay for 2 cycles of the clock selected by the Input selection bit (SEL_IN[1:0]) of the clock selection register (CLK_SEL) during a period of time from when a value is written to this register until the division counter starts to operate.

- Division counter

  This is a down counter that generates the division clocks (WCCK0 to WCCK3) of the input clock (F_{CL}).

3. Explanation of Operations and Setting Procedures of the Watch Counter Prescaler

This section explains the operations of the watch counter prescaler. Also, procedures for setting the operating state are shown.

Procedures for Setting the Watch Counter Prescaler

The procedures for setting the watch counter prescaler are shown below.

- To start output of the division clock
  1. Select the input clock (F_{CL}) of the division counter with the Input Clock Selection Bit (SEL_IN[1:0]) of the clock selection register (CLK_SEL). Also, set the division clock that outputs with the Output Clock Selection Bit(SEL_OUT[2:0]) of the clock selection register (CLK_SEL).
     At this time, the division clock to be output is fixed to L because the division counter is not operating.
  2. Set 1 to the division clock enable bit (CLK_EN) of the division clock enable register (CLK_EN) to enable output of the division clock.
- To stop output of the division clock

  Set 0 to the division clock enable bit (CLK_EN) of the division clock enable register (CLK_EN) to disable output of the division clock.
- To restart after stopping output of the division clock
  1. Set 1 to the division clock enable bit (CLK_EN) of the division clock enable register (CLK_EN) to enable output of the division clock.
  2. Write 0 to the watch counter operation enable bit (WCEN) of the watch counter control register (WCCR) of the watch counter, and clear the value of the 6-bit down counter in the watch counter to 0b000000.
  3. Write 1 to the watch counter operation enable bit (WCEN) of the watch counter control register (WCCR) of the watch counter to restart the operation of the watch counter.
- To switch while the division clock is operating
  1. Set 0 to the division clock enable bit (CLK_EN) of the division clock enable register (CLK_EN) to disable output of the division clock.
  2. Read the CLK_EN_R bit of the division clock enable register (CLK_EN), and confirm whether output of the division clock is stopped (CLK_EN_R=0).
  3. Select the input clock (F_{CL}) of the division counter by the SEL_IN [1:0] bits of the clock selection register (CLK_SEL). Also, set the division clock to be output with the Output Clock Selection Bit(SEL_OUT[2:0]) of the clock selection register (CLK_SEL).
  4. Set 1 to the division clock enable bit (CLK_EN) of the division clock enable register (CLK_EN) to enable output of the division clock.

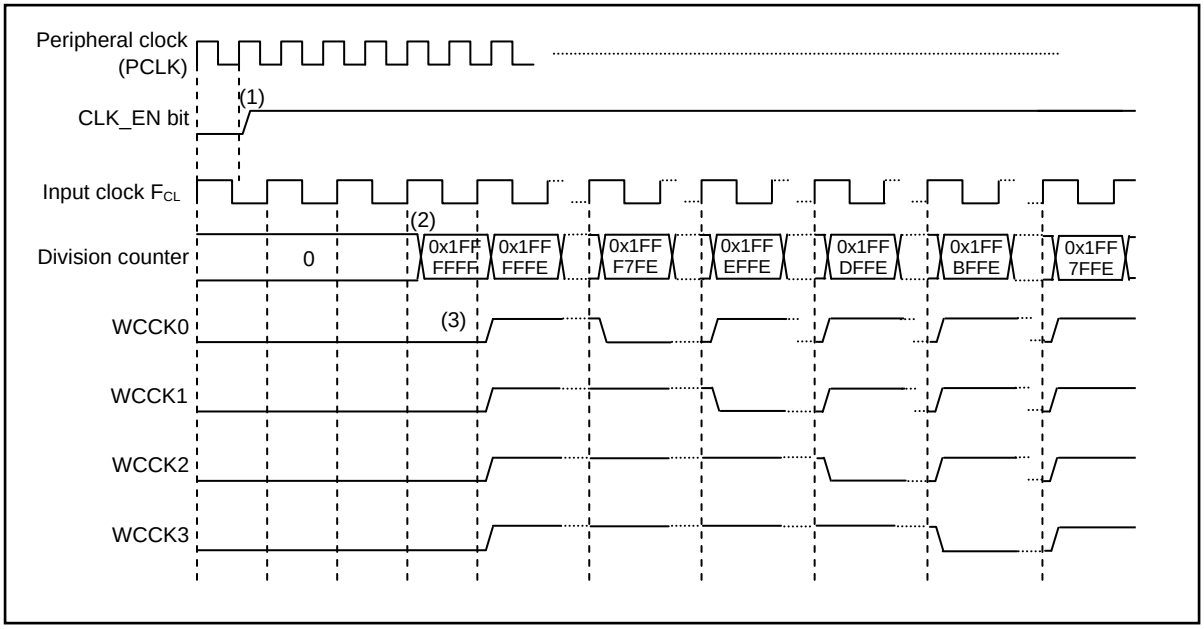
Notes:

- *The peripheral clock (PCLK) is used to set each register of the watch counter prescaler. The input clock (F_{CL}) of the division clock and the peripheral clock (PCLK) are not synchronized. Because the input clock (F_{CL}) of the division counter and peripheral clock (PCLK) are not synchronized, a delay for 3 clocks of the input clock (F_{CL}) is occurred to WCCK0 to WCCK3 after a value is set to each register.*
- *Regarding 2. of To switch while the division clock is operating, a glitch may occur when the division clock is switched while the division counter is operating. Confirm whether output of the division counter is stopped.*
- *The watch counter uses the output of the watch counter prescaler as a count clock. Therefore, the settings of the watch counter prescaler should not be changed while the watch counter is operating.*

Operation of the Watch Counter Prescaler

Figure 3-1 shows an operation of the watch counter prescaler when SEL_OUT [2:0] bit is set to 0 as an example.

Figure 3-1 Operation Explanation Diagram of the Watch Counter Prescaler



(1) Set the CLK_EN bit at rising of the peripheral clock (PCLK).

(2) The division counter is operated synchronizing with the input clock (F_{CL}).

(3) The clocks are output to WCCK0 to WCCK3 from the counter according to the settings of the SEL_OUT [2:0] bit.

Note:

- *The peripheral clock (PCLK) is used for the settings of each register of the watch counter prescaler. Because the input clock (F_{CL}) of the division counter and peripheral clock (PCLK) are not synchronized, a delay for 4 clocks of the input clock (F_{CL}) occurs to WCCK0 to WCCK3 after a value is set for each register.*

Relationship between the Frequency of the Input Clock (F_{CL}) and the Cycle of the Division Clock

Table 3-1 shows the setting example of the frequency of the input clock (F_{CL}) and the cycle of the division clock.

Table 3-1 Setting Example of the Watch Counter Prescaler

SEL_IN[1:0]	SEL_OUT[2:0]	Input Clock Frequency(F_{CL})	Cycle of Division Clock			
			WCCK3	WCCK2	WCCK1	WCCK0
00 (sub clock)	000	32.768 kHz	1 s	500 ms	250 ms	125 ms
01 (main clock)	001	33.554 MHz	1 s	500 ms	250 ms	125 ms
10 (High Speed CR)	110	4 MHz	2.097 s	1.049 s	524 ms	262 ms
11 (CLKLC)	100	100 kHz	41 ms	20 ms	10 ms	5 ms

4. Registers of Watch Counter Prescaler

This section explains the registers for the watch counter prescaler.

Table 4-1 List of Registers for the Watch Counter Prescaler

Abbreviated Register Name	Register Name	Reference
CLK_SEL	Clock selection register	4.1
CLK_EN	Division clock enable register	4.2

4.1 Clock Selection Register (CLK_SEL)

The clock selection register (CLK_SEL) selects the input clock (F_{CL}) and sets the division clocks (WCCK0 to WCCK3) to be output.

bit	15 to 11	10	9	8
Field	Reserved	SEL_OUT[2:0]		
Attribute	-	R/W		
Initial value	00000	000		

bit	7 to 2	1	0
Field	Reserved	SEL_IN[1:0]	
Attribute	-	R/W	
Initial value	000000	00	

[bit15:11, bit7:2] Reserved: Reserved bits

0 is always read.

Writing is ignored.

[bit10:8] SEL_OUT: Output clock selection bit

This bit selects the division clocks (WCCK0 to WCCK3) to be output from the division counter.

bit	Explanation			
	WCCK3	WCCK2	WCCK1	WCCK0
000	$2^{15}/F_{CL}$	$2^{14}/F_{CL}$	$2^{13}/F_{CL}$	$2^{12}/F_{CL}$
001	$2^{25}/F_{CL}$	$2^{24}/F_{CL}$	$2^{23}/F_{CL}$	$2^{22}/F_{CL}$
010	$2^{4}/F_{CL}$	$2^{3}/F_{CL}$	$2^{2}/F_{CL}$	$2/F_{CL}$
011	$2^{8}/F_{CL}$	$2^{7}/F_{CL}$	$2^{6}/F_{CL}$	$2^{5}/F_{CL}$
100	$2^{12}/F_{CL}$	$2^{11}/F_{CL}$	$2^{10}/F_{CL}$	$2^{9}/F_{CL}$
101	$2^{19}/F_{CL}$	$2^{18}/F_{CL}$	$2^{17}/F_{CL}$	$2^{16}/F_{CL}$
110	$2^{23}/F_{CL}$	$2^{22}/F_{CL}$	$2^{21}/F_{CL}$	$2^{20}/F_{CL}$

[bit1:0] SEL_IN: Input clock selection bit

This bit selects the input clock (F_{CL}) to be used.

bit	Explanation
00	Generates a division clock using the sub clock.
01	Generates a division clock using the main clock.
10	Generates a division clock using the high-speed CR
11	Generates a division clock using CLKLC.

4.2 Division Clock Enable Register (CLK_EN)

The division clock enable register (CLK_EN) is a register to enable a count down of the division counter.

bit	7	2	1	0
Field	Reserved		CLK_EN_R	CLK_EN
Attribute	-		R/W	R/W
Initial value	000000		0	0

[bit7:2] Reserved: Reserved bits

0 is always read.
Writing is ignored.

[bit1] CLK_EN_R: Division clock enable read bit

This bit can read the value of CLK_EN bit used for controlling the division. Writing to this bit does not affect operation or the reading value.

bit	Explanation
0	The counter for the clock division stops counting, and oscillation of the division clock is not performed.
1	The counter for the clock division starts counting, and oscillation of the division clock is performed.

[bit0] CLK_EN: Division clock enable bit

There is a delay for 2 cycles in the clock selected by the CLK_SEL register during a period of time from when a value is written to the CLK_EN bit until the value is reflected.

bit	Explanation
0	The division counter stops counting, and disables oscillation of the division clock. Clears the value of the division counter to 0.
1	The division counter starts counting, and enables oscillation of the division clock.

CHAPTER 3-2: Watch Counter

This chapter explains the functions and operations of the watch counter.

1. Overview of the Watch Counter
2. Configuration of the Watch Counter
3. Interrupts of the Watch Counter
4. Explanation of Operations and Setting Procedure Examples of the Watch Counter
5. Registers of Watch Counter

1. Overview of the Watch Counter

The watch counter is a timer that counts down starting from the specified value, and it generates an interrupt request at the time that the 6-bit down counter enters an underflow condition.

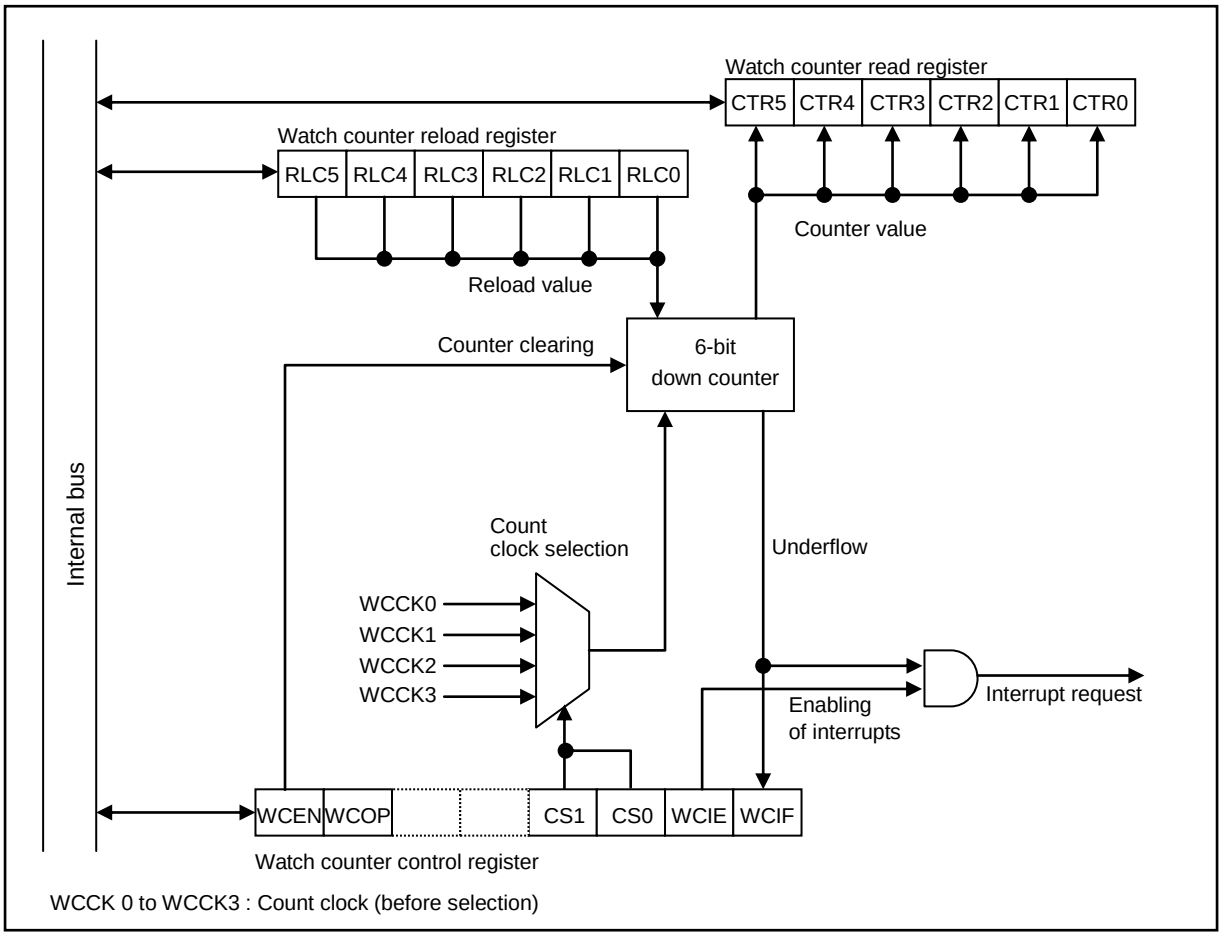
Watch Counter

- For the watch counter, one of the four types of clock (WCCK0, WCCK1, WCCK2, and WCCK3) selected by the count clock select bits (CS[1:0]) of the watch counter control register (WCCR) is used as a count clock of the 6-bit down counter.
- A number between 0 and 63 can be set as the value used for counting by the 6-bit down counter. If "60" is the count value used for a counting period of 1 second, an interrupt request is generated at an interval of 1 minute. If 0 is the count value used for a counting period of 1 second, an interrupt request is generated at an interval of 64 seconds
- An interrupt request can be generated at the time that the 6-bit down counter enters an underflow condition.

2. Configuration of the Watch Counter

This section shows the block diagram of the watch counter.

Figure 2-1 Block Diagram of the Watch Counter



- 6-bit down counter

  This is the 6-bit down counter of the watch counter. It reloads the value set in the watch counter reload register (WCRL) and starts counting down.

- Watch counter reload register (WCRL)

  This register specifies the value used by the watch counter to start counting. The 6-bit down counter counts down starting from the value set in this register.

- Watch counter read register (WCRD)

  This register reads the value in the 6-bit down counter. Also, the register can be read to check the count value.

- Watch counter control register (WCCR)

  This register controls the operation of the watch counter.

3. Interrupts of the Watch Counter

The 6-bit down counter enters an underflow condition when the value in the 6-bit down counter becomes 0b000001, and an underflow interrupt request is then generated.

Table 3-1 Interrupts of the Watch Counter

Interrupt Request	Interrupt Request Flag	Interrupt Request Enabled	Clearing an Interrupt Request
Underflow interrupt request	WCCR:WCIF=1	WCCR:WCIE=1	Write 0 to the WCIF bit for WCCR

WCCR: Watch counter control register

Note:

If generation of interrupt requests is enabled while the interrupt request flag is 1, an interrupt request is generated at the same time. To enable generation of the interrupt request, do either of the following.

- *Enable interrupt requests before enabling the generation of interrupt requests.*
- *Clear interrupt requests simultaneously with interrupts enabled.*

4. Explanation of Operations and Setting Procedure Examples of the Watch Counter

This section explains operations of the watch counter. Also, examples of procedures for setting the operating state are shown.

Setting Procedures of the Watch Counter

To operate the watch counter, follow the procedure below.

Select a count clock by using the count clock select bits (CS[1:0]) of the watch counter control register (WCCR).

Set a count value to the counter reload value setting bits (RLC[5:0]) in the watch counter reload register (WCRL).

Enable the operation of the watch counter by using the watch counter operation enable bit (WCEN) (WCEN = 1) of the watch counter control register (WCCR).
Start a countdown. Counting is performed at the rising edge of the count clock.

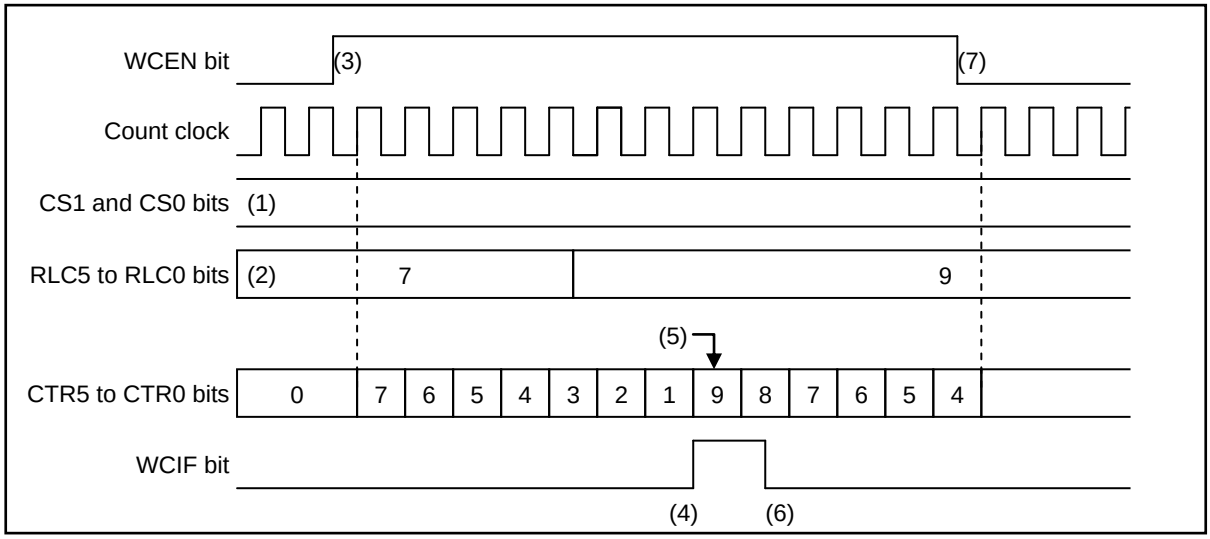
If the 6 -bit down counter enters an underflow condition, the value of the interrupt request flag bit (WCIF in the watch counter control register (WCCR) is changed to 1.
At this time, if generation of underflow interrupt requests has been enabled by the WCIE bit (WCIE = 1) in the watch counter control register (WCCR), an underflow interrupt request is generated.
Also, the value that is set in the counter reload value setting bits (RLC[5:0]) in the watch counter reload register (WCRL) is reloaded in the 6-bit down counter and the countdown is restarted.

If the value of the counter reload value setting bits (RLC[5:0]) in the watch counter reload register (WCRL) is changed to another value while the watch counter is active, the watch counter is updated with the new value at the next reload time.

The underflow interrupt request is cleared when 0 is written to the interrupt request flag bit (WCIF) in the watch counter control register (WCCR).

The 6-bit down counter is cleared to 0b000000 and the counting operation is stopped when "0" is written to the watch counter operation enable bit (WCEN) in the watch counter control register (WCCR).

Figure 4-1 Operation of the Watch Counter



Notes:

- *The peripheral clock (PCLK) is used for the setting of each register of the watch counter. Because the count clock and peripheral clock (PCLK) are not synchronized, an error of up to 1T (T: Count clock period) may occur at the count start time, depending on the time at which 1 is written to the WCEN bit in the watch counter control register (WCCR).*
- *Even at transition of the timer mode, the watch counter continues operating as long as the main clock or sub clock is operating. The timer mode can be canceled with the watch counter interrupt processing routine.*
- *Under the following condition, verify that the watch counter is stopped by checking the watch counter operating state flag (WCOP) (WCOP=0) in the watch counter control register (WCCR) before reactivating the watch counter.*
  Condition: In case of reactivating the watch counter after the watch counter is stopped by writing 0 to the WCEN in the watch counter control register (WCCR) by using the WCEN bit (WCEN = 1).

5. Registers of Watch Counter

This section explains the registers for the watch counter.

Table 5-1 List of Registers for the Watch Counter

Abbreviated Register Name	Register Name	Reference
WCRD	Watch counter read register	5.1
WCRL	Watch counter reload register	5.2
WCCR	Watch counter control register	5.3

5.1 Watch Counter Read Register (WCRD)

This register reads the value in the 6-bit down counter.

bit	7	6	5	4	3	2	1	0
Field	Reserved		CTR[5:0]					
Attribute	-		R					
Initial value	00		000000					

[bit7:6] Reserved: Reserved bits

"0" is always read.
Writing is ignored.

[bit5:0] CTR[5:0]: Counter read bits

These bits can read the counter value.
Writing is ignored.

Note:

- *If the 6-bit down counter is operating when its value is read, the register value must be read twice and verified to be the same value.*

5.2 Watch Counter Reload Register (WCRL)

This register specifies the value used by the watch counter to start counting. The 6-bit down counter counts down starting from the value set in the register.

The register specifies the reload value for the 6-bit down counter. If the 6-bit down counter enters an underflow condition, the value in this register is reloaded in the 6-bit down counter, and the countdown is restarted.

bit	15	14	13	12	11	10	9	8
Field	Reserved		RLC[5:0]					
Attribute	-		R/W					
Initial value	00		000000					

[bit15:14] Reserved: Reserved bits

"0" is always read.
Writing is ignored.

[bit13:8] RLC[5:0]: Counter reload value setting bits

These bits set the reload value for the 6-bit down counter.

The 6-bit counter counts downwards from the reload value and enters an underflow condition when its value reaches "1". If "0b000000" is set in these bits, it performs 64 countdowns from "63" to "0".
If this bit is modified during counting, the modified value is valid at reloading after underflow.

Notes:

- *If the value of RLC[5:0] bits is changed to another value while the 6-bit down counter is active, an underflow occurs and the new value is then reloaded.*
- *If the value of RLC[5:0] bits is changed to another value at the same time that an underflow interrupt request is generated, the correct value is not reloaded. Be sure to rewrite the value of RLC[5:0] bits either when the watch counter is stopped or in the interrupt processing routine before an interrupt request is generated.*
- *To verify whether the reload value is correctly set, read this register.*

5.3 Watch Counter Control Register (WCCR)

This register selects a count clock for the watch counter or enables/disables generation of interrupt requests. The register also enables/disables the operation of the watch counter.

bit	23	22	21	20	19	18	17	16
Field	WCEN	WCOP	Reserved		CS1	CS0	WCIE	WCIF
Attribute	R/W	R	-		R/W	R/W	R/W	R/W
Initial value	0	0	00		0	0	0	0

[bit23] WCEN: Watch counter operation enable bit

This bit enables the operation of the watch counter.

The peripheral clock (PCLK) is used for the settings of each register of the watch counter. Because the count clock and the peripheral clock (PCLK) are not synchronized, an error of up to 1T (T: count clock period) may occur at the count start time, depending on the time at which "1" is written to the WCEN bit of watch counter control register (WCCR).

Before writing "1" to this bit to start the operation of the watch counter, verify that the watch counter is stopped by checking the WCOP bit (WCOP=0).

bit	Explanation
0	The watch counter is disabled/stopped. The value in the 6-bit down counter is cleared to "0b000000".
1	The watch counter is enabled/started.

[bit22] WCOP: Watch counter operating state flag

This bit indicates the operating state of the watch counter.

Bit	Explanation
0	The watch counter is stopped.
1	The watch counter is active.

[bit21:20] Reserved: Reserved bits

"0" is always read.
Writing is ignored.

[bit19:18] CS1, CS0: Count clock select bits

These bits select a clock for the watch counter.

Change these bits when WCCR:WCEN=0 (watch counter operation disabled) and WCOP=0 (watch counter stopped).

bit19	bit18	Explanation
0	0	Selects WCCK0 as a count clock.
0	1	Selects WCCK1 as a count clock.
1	0	Selects WCCK2 as a count clock.
1	1	Selects WCCK3 as a count clock.

[bit17] WCIE: Interrupt request enable bit

This bit specifies whether to generate an underflow interrupt request when the 6-bit down counter underflows (WCIF=1).

Bit	Explanation
0	Disables generation of underflow interrupt requests.
1	Enables generation of underflow interrupt requests.

[bit16] WCIF: Interrupt request flag bit

This bit becomes "1" when the counter underflows.

When this bit and the WCIE bit are "1", a watch counter interrupt is generated.

"1" can be read when reading by the read modify write access.

bit		Explanation
Write	0	Clear this bit.
	1	No effect on operation.
Read	0	Indicate that an underflow does not occur.
	1	Indicate that an underflow occurs.

CHAPTER 4-1: Real-time Clock

The real-time clock is composed of the RTC clock control block and the RTC count block.

1. Configuration of Real-time Clock
2. Real-time Clock Acronym
3. Resetting RTC

1. Configuration of Real-time Clock

This section shows the configuration of the real-time clock.

Reference Chapters for the Real-Time Clock

Table 1-1 Correspondence Table for Real-time Clock

Product TYPE	Reference
TYPE1-M4, TYPE2-M4, TYPE6-M4	Chapter "RTC Count Block (A)" Chapter "RTC Clock Control Block (A)"
TYPE3-M4, TYPE4-M4	Chapter "RTC Count Block (B)" Chapter "RTC Clock Control Block (B)"
TYPE5-M4	Chapter "RTC Count Block (C)" Chapter "RTC Clock Control Block (C)"

Configuration of the Real-time Clock

Figure 1-1 Configuration of RTC Clock Control Block (A) and RTC Count Block (A)

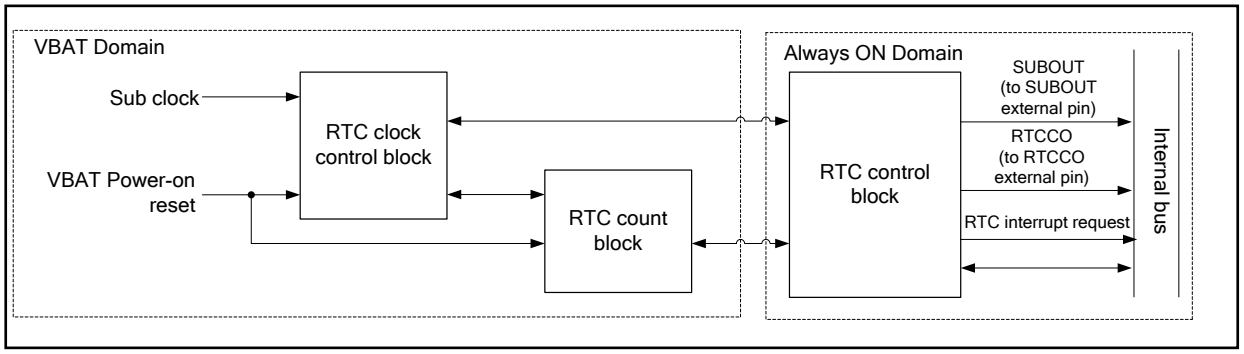


Figure 1-2 Configuration of RTC Clock Control Block (B) and RTC Count Block (B)

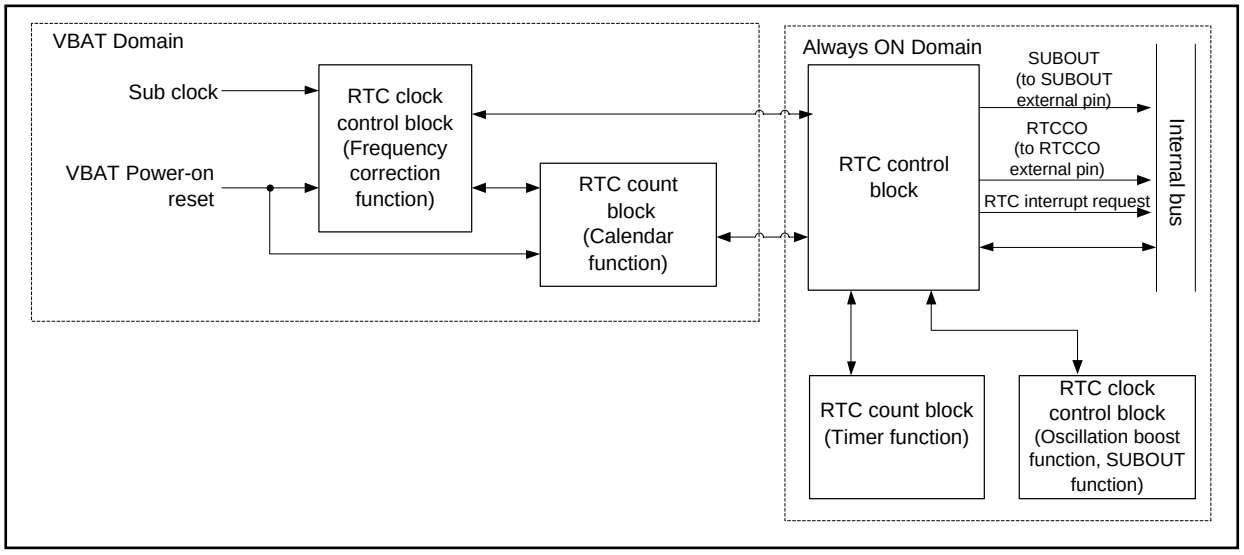
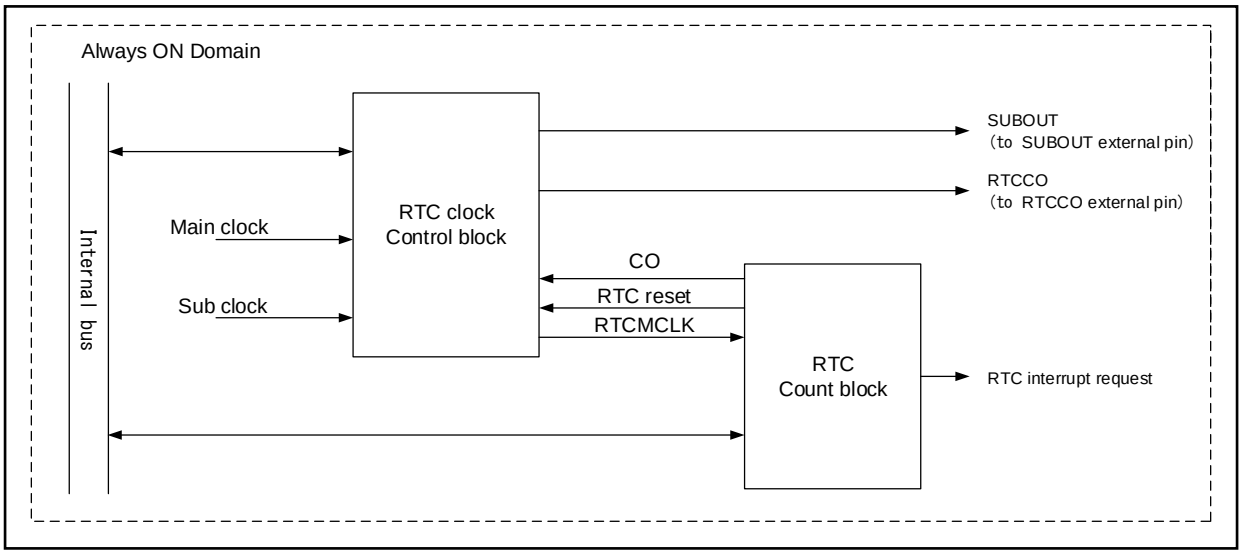


Figure 1-3 Configuration of RTC Clock Control Block (C) and RTC Count Block (C)



Notes:

- *In case of configuration of the RTC clock control block (A) and RTC count block (A), All of the RTC clock control block and RTC count block are placed in VBAT domain.*
- *In case of configuration of the RTC clock control block (B) and RTC count block (B), frequency correction function of the RTC clock control block and the calendar function of the RTC count block are placed in VBAT domain.*
  See Chapter VBAT Domain for details of the RTC control block.

2. Real-time Clock Acronym

This section explains the acronym of the real-time clock.

Acronym

- RTC: Real-time clock

  The RTC is composed of the RTC clock control block and the RTC count block.

3. Resetting RTC

This section explains the resetting of the RTC.

Resetting RTC (TYPE1-M4, TYPE2-M4, TYPE3-M4, TYPE4-M4, TYPE6-M4)

The RTC is reset by the VBAT power-on reset, but cannot be reset by the reset of the Always ON Domain.
Table 3-1 shows the reset sources of the VBAT Domain and Always ON Domain.

Table 3-1 Reset sources of the VBAT Domain and Always ON Domain

	VBAT Domain	Always ON Domain
VBAT power-on reset	○	×
Power-on reset	×	○
Low voltage detection reset	×	○
System reset	×	○
RTC reset	×	○
"○" shows the reset sources.		

The system reset consists of the following reset sources.

- INITX pin input
- Software watchdog reset
- Hardware watchdog reset
- Clock failure detection reset
- Anomalous frequency detection reset

An RTC reset is generated by writing 1 to the WTCR10:SRST bit.

Note:

- *See Chapter RTC Count Block for buffers to be initialized in the reset signals of the Always ON Domain.*

Resetting RTC (TYPE5-M4)

Four types of resets are available to the real-time clock, and they are each initialized with a different register.

■ Low-voltage Detection Reset/Power-on Reset

All the registers of the real-time clock are initialized.

■ System Reset

A system reset occurs with a reset factor (i.e., INITX pin input, a software watchdog reset, a hardware watchdog reset, a clock failure detection reset, or an abnormal frequency detection reset).
All the registers of the RTC clock control block are initialized.
For the registers that are initialized in the RTC count block, see 4. Resetting of the RTC Count Block in Chapter RTC Count Block.

■ RTC Reset

An RTC reset occurs by writing "1" to the SRST (RTC reset bit) in the RTC count block.
For the initialization of the registers in the RTC clock control block, see the precautions for the respective resisters in 7. Registers of the RTC Clock Control Block in Chapter RTC Clock Control Block.
For the registers that are initialized in the RTC count block, see "4. Resetting of the RTC Count Block" in Chapter RTC Count Block.

CHAPTER 4-2: RTC Count Block(A)

This chapter explains the functions and operations of the RTC count block(A).

1. Overview of RTC Count Block
2. Block Diagram of RTC Count Block
3. Operations of RTC Count Block and Setting Procedures
4. RTC Control Block Reset Operation
5. Leap Year Compliance of RTC Count Block
6. Time Rewrite Error
7. Registers in RTC Control Block
8. Usage Precautions

1. Overview of RTC Count Block

The RTC count block counts date and time (year, month, day, hour, minute, second and day of the week) from 00 year to 99 year, and also sets an alarm and a timer. The block can set an alarm for a specific time (year, month, day, hour, minute) or for a specific year/month/day/hour/minute. It can also set the timer to a future time (in hours, minutes and seconds) or to an interval (in hours, minutes and seconds) within a day. An overview of the RTC count block is shown below.

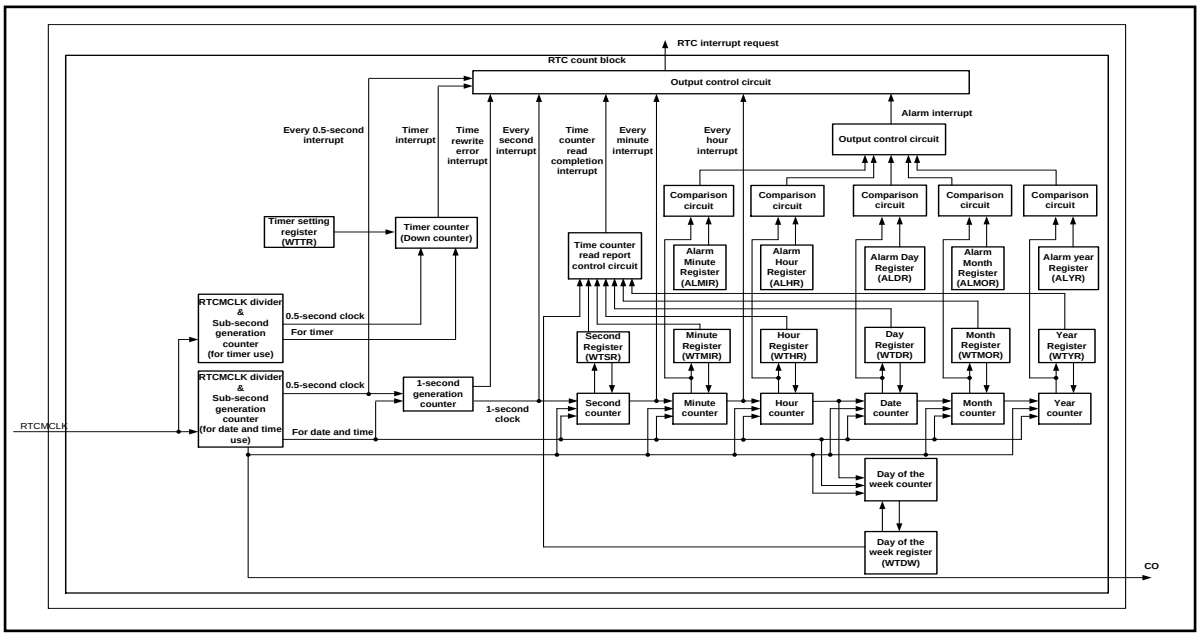
Overview of Functions of RTC Count Block

- Setting date and time (year, month, date, hour, minute, second, day of the week)
- Counting date and time (year (00 to 99), month, day, hour, minute, second and day of the week)
- Leap year compliance (00 year is operated as leap year)
- Alarm for a specific time (year, month, day, hour, minute)
- Alarm for a specific year/month/day/hour/minute
- Timer for a future time (in hours, minutes or seconds) or to an interval (in hours, minutes or seconds) within a day
- The RTC count block can reset the watch count of the RTC count block and modify the time for setting the time by the time signal.
- For changing time zone, the RTC count block can rewrite the time while keeping the watch count of the RTC count block running.(If the rewriting of the time is completed within 1 second, the RTC count block can keep counting the time without being interrupted.)
- The RTC count block can output the following interrupts:
  - Alarm (an interrupt to be generated at a designated date and time)
  - Every hour
  - Every minute
  - Every second
  - Every 0.5second
  - Timer
  - Time rewrite error
  - Time counter read completion
  - Pulse output every 0.5 second

2. Block Diagram of RTC Count Block

Figure 2-1 shows the block diagram of the RTC count block.

Figure 2-1 Block Diagram of RTC Count Block



RTCMCLK Divider and Sub-second Generation Counter (for Timer)

The RTCMCLK divider generates a timer clock. The sub-second generation counter (for timer) operates using the clock generated by the RTCMCLK divider and counts the time by the sub-second (0.5 second).

RTCMCLK Divider and Sub-second Generation Counter (for Date and Time)

The RTCMCLK divider generates a date and clock. The sub-second generation counter (for date and time) operates using the clock generated by the RTCMCLK divider and counts the time by the sub-second (0.5 second).

Timer Setting Register (WTTR)

This register stores the future time (in hours, minutes and seconds) and the interval (in hours, minutes and seconds) for the timer.

Timer Counter (Down Counter)

The timer counter counts down the value set in the Timer Setting Register with 0.5 second pulse that is output by the sub-second generation counter (for timer).

1 second Generation Counter

The timer counter generates 1 second pulses by counting 0.5 second pulses that the sub-second generation counter (for date and time) outputs.

Second Counter, Minute Counter, Hour Counter, Day Counter, Month Counter, Year Counter, and Day of the Week Counter

These counters count seconds, minutes, hours, days, months, years and days of the week respectively.

Second Register (WTSR), Minute Register (WTMIR), Hour Register (WTHR), Day Register (WTDR), Month Register (WTMOR) and Year Register (WTYR)

These registers indicate the following data of the RTC count block respectively: second, minute, hour, day, month and year.

Time Counter Read Report Control Circuit

This circuit reports the completion of the reading of the time counter.

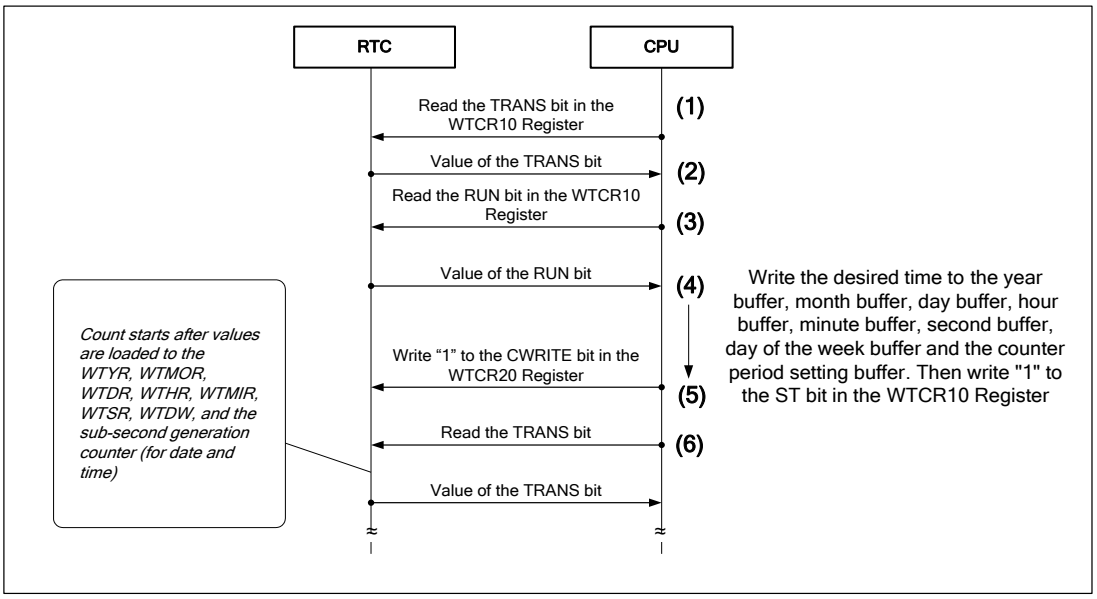
Alarm Minute Register (ALMIR), Alarm Hour Register (ALHR), Alarm Day Register (ALDR), Alarm Month Register (ALMOR) and Alarm Year Register (ALYR)

These registers store the minute, hour, day, month and year settings of the alarm respectively. If an alarm is set, a comparison circuit compares the value stored in one of the above registers with its corresponding counter value (minute counter, hour counter, day counter, month counter and year counter). If the two values are the same, an alarm interrupt is generated.

3. Operations of RTC Count Block and Setting Procedures

This section explains the operation of the RTC count block and shows examples of the setting procedures.

Figure 3-1 Initial Time Setting Procedures



(1) Read the value of the TRANS bit in the WTCR10 Register of the RTC count block.

(2) If the value of the TRANS bit is 1, wait until the value becomes 0.

(3) If the value of the RUN bit is 0, following step (4) to step (6) to complete the initial time setting is possible. If the value of the RUN bit is 1, see Time rewrite setting procedures (with time count continued) and Time rewrite setting procedures (with time count reset).

(4) Write the desired time to the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer, day of the week buffer (WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR, and WTDW) and write 1 to the ST bit in the WTCR10 Register.

(5) Write 1 to the CWRITE bit in the WTCR20 Register of the RTC count block. (CWRITE operation)

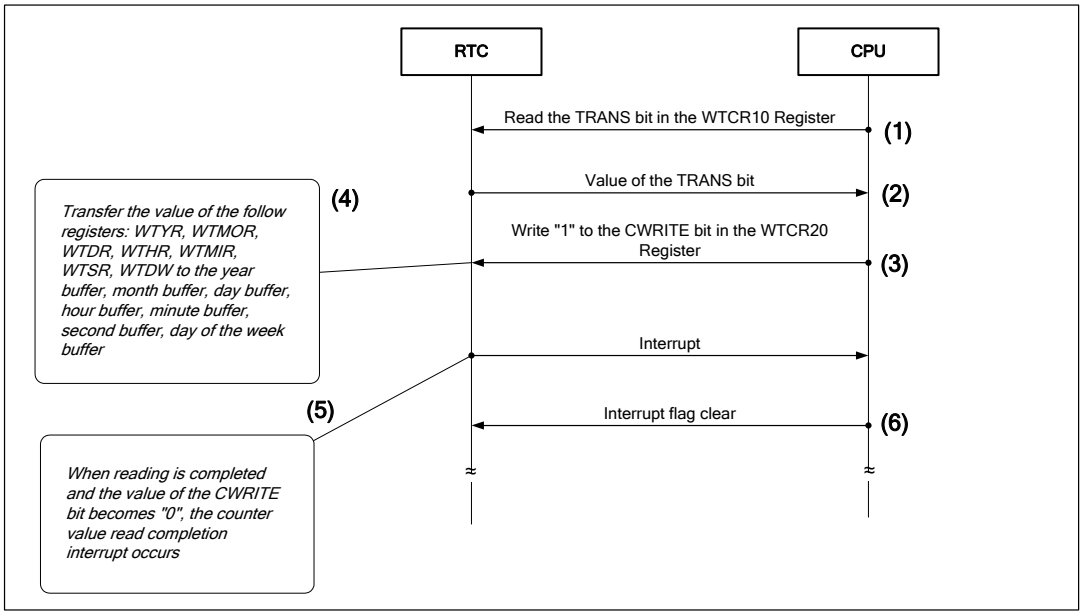
(6) If the value of the TRANS bit is 1, the CWRITE bit is operating.

If the value of the TRANS bit is 0, the operation of the CWRITE bit has completed.

Notes:

- *Access to the buffers in the RTC control block is prohibited during a recall operation or save operation.*
- *Run PCLK2 at 1 MHz or above during time rewrite.*
- *Do not reset the RTC control block or cut off power during transfer.*
  If the power is turned off during the save operation, set it again.
- *Do not perform any operation that will stop the RTCMCLK during the save operation.*

Figure 3-2 Time Read Setting Procedures



(1) Read the value of the TRANS bit in the WTCR10 Register.

(2) If the value of the TRANS bit is 1, wait until the value becomes 0.

(3) Write 1 to the CWRITE bit in the WTCR20 Register of the RTC count block. (CREAD operation)

(4) When the value of the CWRITE bit becomes 1, the value of the following registers: WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR, WTDW will be transferred to the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer, day of the week buffer (WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR, WTDW) respectively.

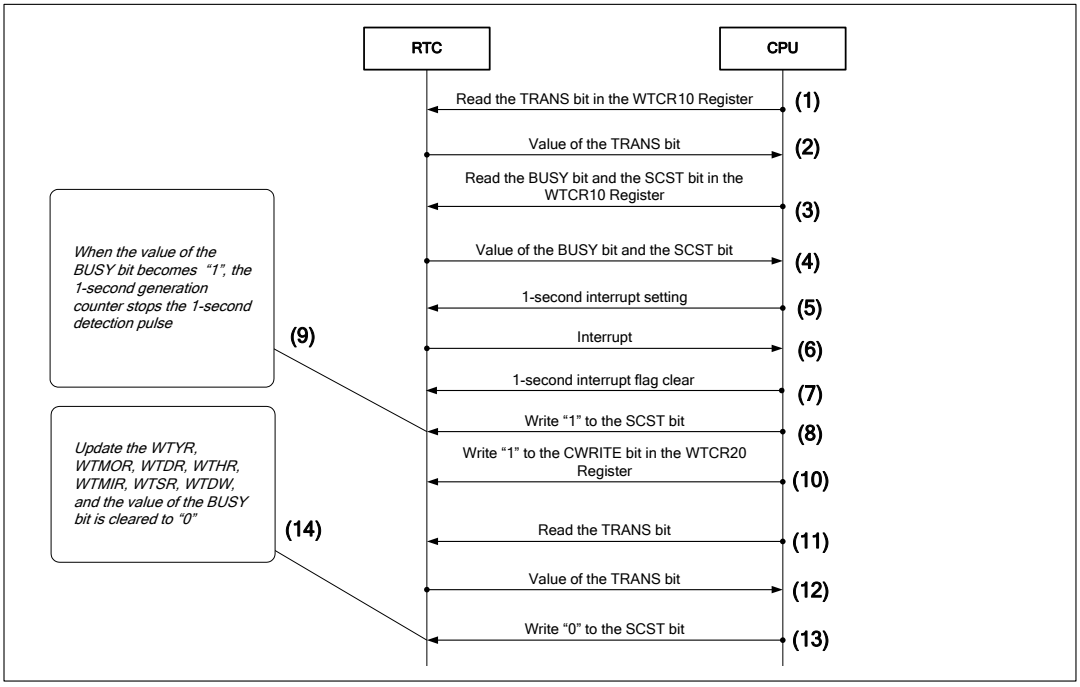
(5) When the above operation is completed, the value of the CREAD bit and that of the TRANS bit become 0, and the year/ month/ day/ hour/ minute/ second/ day of the week counter value read completion flag will occur.

(6) Clear the year/ month/ day/ hour/ minute/ second/ day of the week counter value read completion flag bit (INTCRI) in the WTCR12 Register of the RTC count block.

Notes:

- *Access to the buffers in the RTC control block is prohibited during a recall operation or save operation.*
- *Run PCLK2 at 1 MHz or above during time rewrite.*
- *Do not reset the RTC control block or cut off power during transfer.*
- *When the value of the CREAD bit is 1, writing 1 to the SCST bit and the SRST bit in the WTCR10 register of the RTC count block is prohibited.*
- *Do not perform any operation that will stop the RTCMCLK during the recall operation.*

Figure 3-3 Time Rewrite Setting Procedures (with Time Count Continued)



(1) Read the value of the TRANS bit in the WTCR10 Register.

(2) If the value of the TRANS bit is 1, wait until the value becomes 0.

(3) Read the value of the BUSY bit and the SCST bit in WTCR10 Register of the RTC count block.

(4) If the value of the BUSY bit is 1 and that of the SCST bit is 0, wait until the value of the BUSY bit becomes 0. In other cases, follow step (5) and onwards.

(5) Write 0 to the INTSI bit in the WTCR12 Register of the RTC count block to clear the interrupt flag bit. Write 1 to the INTSIE bit in the WTCR13 Register of the RTC count block to enable the interrupt.

(6) 1 second interrupt request will occur.

(7) Write 0 to the INTSI bit to clear the interrupt flag bit.

(8) Write 1 to the SCST bit.

(9) When 1 is written to the SCST bit, the value of the BUSY bit becomes 1. When the value of the BUSY bit becomes 1, the detection of the 1 second pulse of the 1 second generation counter stops.

(10) While the value of the BUSY bit is 1, write the desired year/ month/ day/ hour/ minute/ second/ day of the week to the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer, day of the week buffer (WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR, WTDW) respectively. Write "1" to the CWRITE bit in the WTCR20 register of the RTC count block.

(11) Read the value of the TRANS bit.

(12) If the value of the TRANS bit is 1, wait until the value becomes 0.

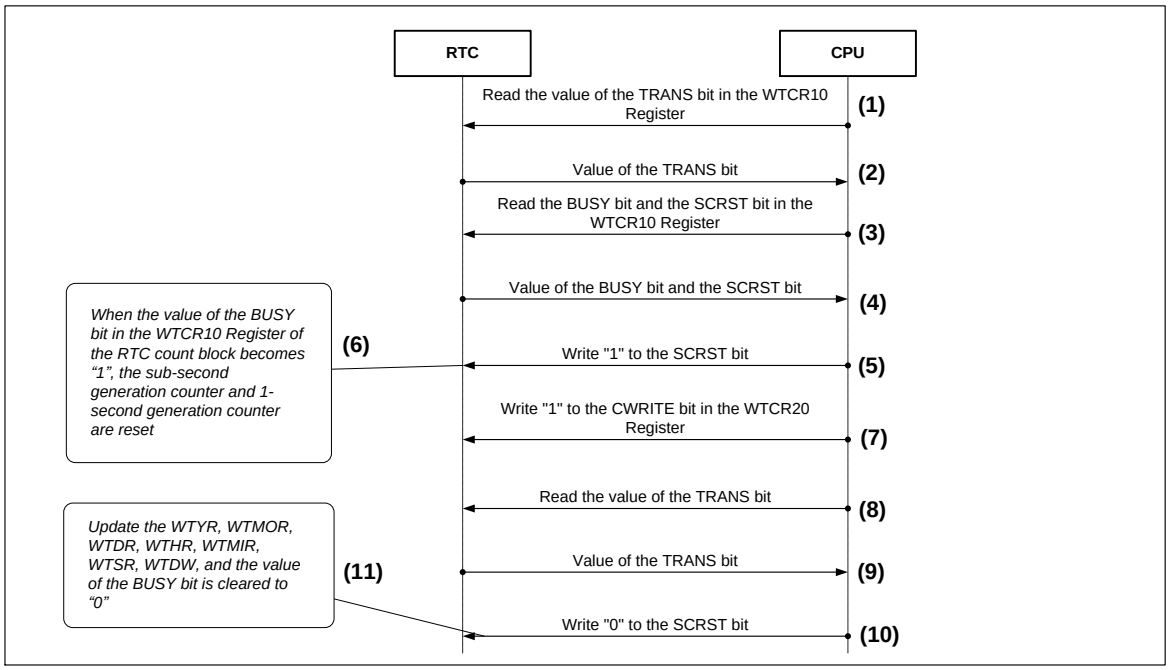
(13) Write 0 to the SCST bit.

(14) The value of the BUSY bit will be cleared to 0.

Notes:

- *Access to the buffers in the RTC control block is prohibited during a recall operation or save operation.*
- *Run PCLK2 at 1 MHz or above during time rewrite.*
- *Do not reset the RTC control block or cut off power during transfer. If the busy bit (BUSY) of control register 10 (WTCR10) is 1 after the reset is cancelled, set it again, starting from (8). If it is not set again, there may be a time lag.*
- *To rewrite the time, a recall must be performed. Rewrite the time after the latest time is read. If recall has not been performed, time lag occurs.*
- *If the value of the BUSY bit is 1 and that of the SCST bit is 0, writing 1 to the SCST bit is prohibited.*
- *If the value of the RUN bit is 0, writing 1 to the SCST bit is prohibited.*
- *Continuous time count cannot be guaranteed if the setting in step (7) to step (13) exceeds 1 second. In that case, a time rewrite error interrupt will occur. When the value of the INTERI bit in the WTCR12 Register becomes 1, time lag may occur. Therefore, write 0 to the SCST bit. After the time rewrite error flag is cleared, follow the above procedures from the beginning again to set the time.*
- *When the value of the SCST bit is 0 and that of the BUSY bit is 1, or that of the TRANS bit are 1, writing to the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer or day of the week buffer is prohibited because data is transferring from to the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer and day of the week buffer to the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR and WTDW.*
- *After setting the value of the SCST bit to 1, write 1 to the CREAD bit before updating the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR and WTDW. The value written in the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer or day of the week buffer will be overwritten to the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR and WTDW respectively.*
- *If RTCMCLK is stopped while the value of the BUSY bit is 1, the transfer of value from the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR and WTDW to the year counter, month counter, day counter, hour counter, minute counter, second counter and day of the week counter cannot function properly. Therefore, the value of the year counter, month counter, day counter, hour counter, minute counter, second counter and day of the week counter cannot be guaranteed.*
- *When the value of the BUSY bit is 1, writing 0 to the ST bit in the WTCR10 Register is prohibited.*
- *When the BUSY bit of control register 10 (WTCR10) is 1, or the 1-sec pulse detection stop bit (SCST) of WTCR10 is 1, it is prohibited to write 1 to the SRST bit of WTCR10.*
- *During the continuous time rewrite operation (i.e. when the RTC count block operation bit (RUN) of WTCR10 is 1, and the 1 sec pulse bit SCST of WTCR10 is 1), you may not write1 to the 1 sec pulse bit SCST of WTCR10 until the BUSY bit of WTCR10 is set to 0, after 0 is written to the 1 sec pulse bit SCST of WTCR10.*

Figure 3-4 Time Rewrite Setting Procedures (Time Count Reset)



(1) Read the value of the TRANS bit in the WTCR10 Register.

(2) If the value of the TRANS bit is 1, wait until the value becomes 0.

(3) Read the value of the BUSY bit and that of the SCRST bit in WTCR10 Register.

(4) If the value of the BUSY bit is 1 and that of the SCRST is 0, wait until the value of the BUSY bit becomes 0. In other cases, follow step (5) and onwards.

(5) Write 1 to the SCRST bit.

(6) When 1 is written to the SCRST bit, the value of the BUSY bit becomes 1. The sub-second generation/1 second generation counter is reset.

(7) While the value of the SCRST bit is 1, write the desired value for the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR, WTDW to the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer or day of the week buffer (WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR, WTDW) respectively. Write 1 to the CWRITE bit in the WTCR20 Register.

(8) Read the value of the TRANS bit.

(9) If the value of the TRANS bit is 1, wait until the value becomes 0.

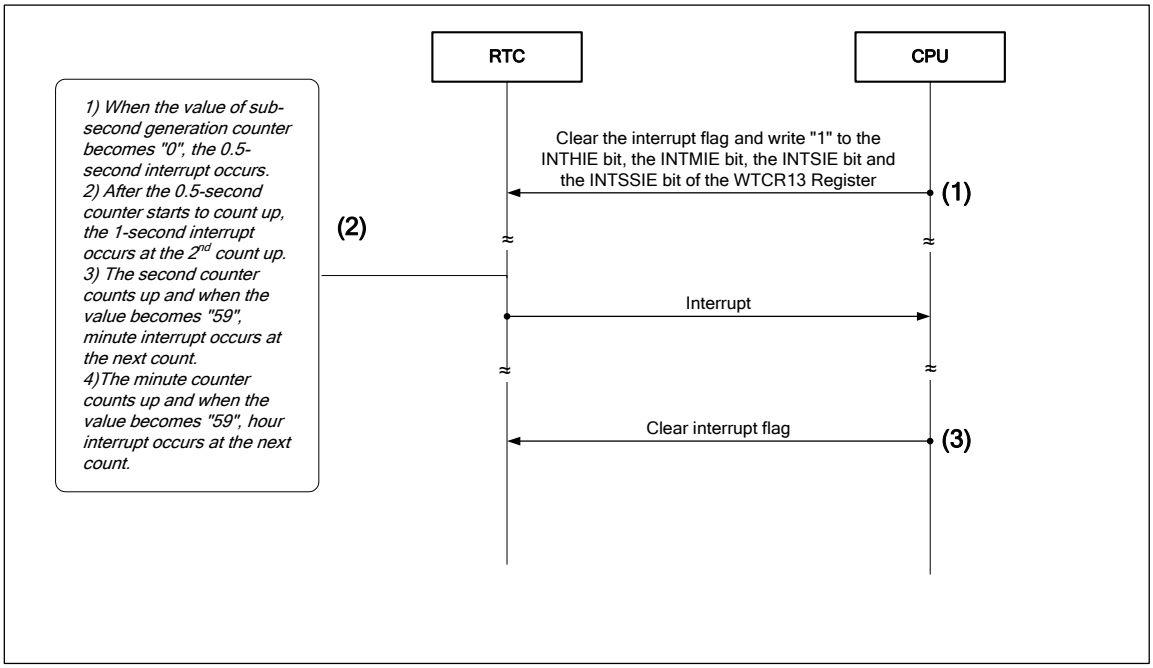
(10) Write 0 to the SCRST bit.

(11) When the value of the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer or day of the week buffer is transferred to the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR or WTDW respectively, the value of the BUSY bit is cleared to 0.

Notes:

- *Access to the buffers in the RTC control block is prohibited during a recall operation or save operation.*
- *Run PCLK2 at 1 MHz or above during time rewrite.*
- *Do not perform a reset or turn off the power during transfer (i.e. when the transfer flag bit (TRANS) of control register 10 (WTCR10) is 1) or when the sub-second generation/1-sec generation counter reset bit (SCRST) of control register 10 (WTCR10) is 1. If the busy bit (BUSY) of control register 10 (WTCR10) is 1 after the reset is cancelled, write 0 to the sub-second generation/1-sec generation counter reset bit (SCRST) of control register 10 (WTCR10), and then set it again, starting from (5). If it is not set again, there may be a time lag.*
- *To rewrite the time, recall must be performed. Rewrite the time after the latest time is read. If recall has not been performed, time lag occurs.*
- *If the value of the BUSY bit is 1 and that of the SCRST bit is 0, writing 1 to the SCRST bit is prohibited.*
- *If the value of the RUN bit is 0, writing 0 to the SCRST bit is prohibited.*
- *When the value of the SCRST bit is 0 and that of the BUSY bit is 1, or of the TRANS bit is 1, writing data to the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer or day of the week buffer is prohibited because data is transferring from the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer or day of the week buffer to the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR or WTDW respectively.*
- *After setting 1 to the SCRST bit, run the CREAD bit before updating the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR or WTDW. The value written in the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer or day of the week buffer will be overwritten to the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR or WTDW respectively.*
- *If RTCMCLK is stopped (transit to STOP mode or sub-oscillation stop control by WTOSCCNT) while the value of the BUSY bit is 1, the transfer of value from the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer or day of the week buffer to the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR or WTDW cannot function properly. Therefore, the value of the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR or WTDW cannot be guaranteed.*
- *When the value of the BUSY bit is 1, writing 0 to the ST bit is prohibited.*
- *When the busy bit (BUSY) of control register 10 (WTCR10) is 1, or the sub-second generation/1-sec generation counter reset bit (SCRST) of control register 10 (WTCR10) is 1, it is prohibited to write 1 to the RTC reset bit (SRST) of control register 10 (WTCR10).*

Figure 3-5 Setting Procedures of Every 0.5 second/ 1 second/ 1-minute/ 1-hour Interrupt

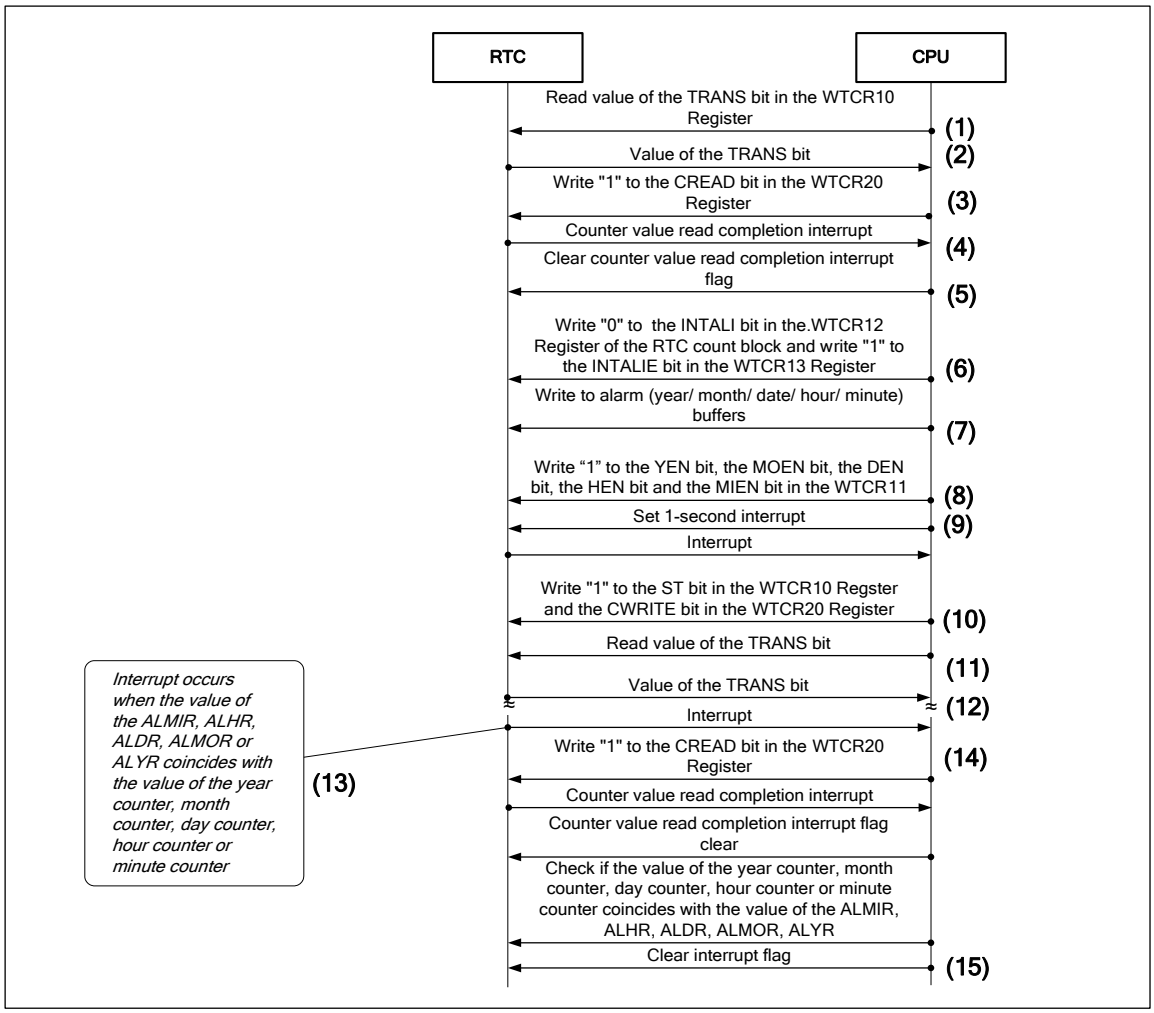


(1) Write 0 to the INTHI bit, the INTMI bit, the INTSI bit and the INTSSI bit in the WTCR12 Register to clear the interrupt flag bit. Write 1 to the desired interrupt enable bit among the INTHIE bit, the INTMIE bit, the INTSIE bit and the INTSSIE bit of the WTCR13 Register to enable the interrupt.

(2) When either 0.5 second interrupt, 1 second interrupt, 1-minute interrupt or 1-hour interrupt occurs, an interrupt request will occur.

(3) Write 0 to the INTHIE bit, the INTMIE bit, the INTSIE bit and the INTSSIE bit to clear the interrupt flag bit.

Figure 3-6 Alarm Interrupt Setting Procedures



(1) Read the value of the TRANS bit in the WTCR10 Register.

(2) If the value of the TRANS bit is 1, wait until the value becomes 0.

(3) Write 1 to the CREAD bit in the WTCR20 Register to read the counter value.

(4) When the transfer of value to the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer or day of the week buffer is completed, the value of the CREAD bit becomes 0 and the year/ month/ day/ hour/ minute/ second/ day of the week counter value read completion interrupt will occur.

(5) Clear the counter value read completion interrupt flag bit.

(6) Write 0 to the INTALI bit in the WTCR12 Register of the RTC count block to clear the alarm interrupt flag bit. Write 1 to the INTALIE bit in the WTCR13 Register to enable the alarm interrupt.

(7) Write the desired date and time for the alarm interrupt to the alarm (year/ month/ day/ hour) buffers.

(8) Write 1 to the YEN bit, the MOEN bit, the DEN bit, the HEN bit and the MIEN bit in the WTCR11.

(9) After setting the 1 second interrupt, wait for it.

(10) After the 1 second interrupt occurs, write 1 to the ST bit in the WTCR10 Register and the CWRITE bit in the WTCR20 Register to transfer the alarm value.

(11) Read the value of the TRANS bit.

(12) Wait until the value of the TRANS bit becomes 1.

(13) If the value of the ALMIR, ALHR, ALDR, ALMOR, ALYR and that of the year counter, month counter, day counter, hour counter or minute counter coincides, an interrupt request occurs.

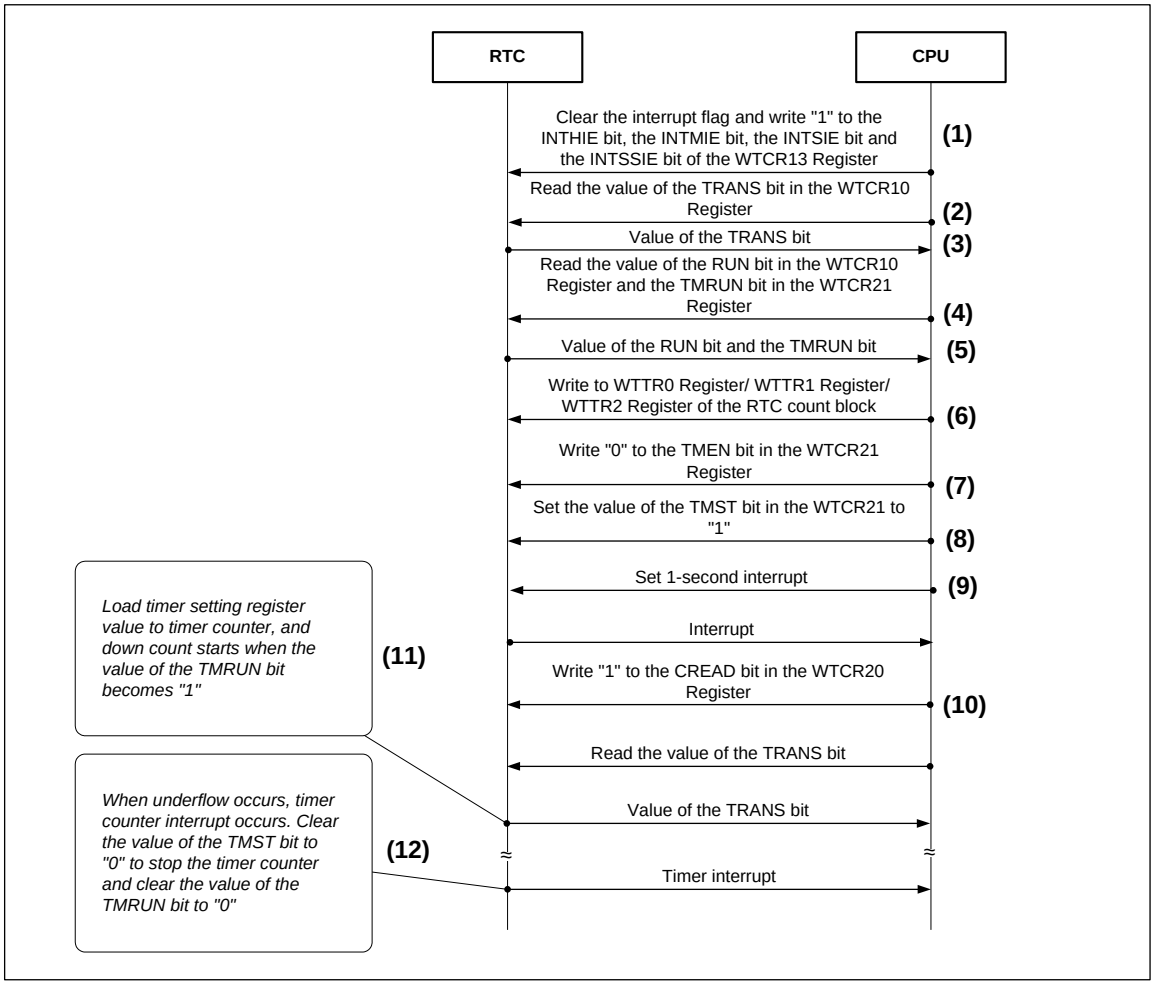
(14) Follow the time read setting procedures to read the time and check if the value of the year counter, month counter, day counter, hour counter or minute counter coincides with the value of the ALMIR, ALHR, ALDR, ALMOR, ALYR.

(15) Write 0 to the INTALI bit to clear the alarm interrupt flag bit.

Notes:

- *Interrupt may occur immediately after 1 is written to any of the alarm enable bits. Recall and read the time after the interrupt and check if the value of the year counter, month counter, day counter, hour counter or minute counter coincides with the value of the ALMIR, ALHR, ALDR, ALMOR, ALYR.*
- *Access to the buffers in the RTC control block is prohibited during a recall operation or save operation.*
- *Run PCLK2 at 1 MHz or above during time rewrite.*
- *Do not reset the RTC control block or cut off power during transfer.*

Figure 3-7 Timer Interrupt Setting Procedures (with (Hours, Minutes, and Seconds) Elapsed)



(1) Write 0 to the INTTMI bit in the WTCR12 Register of the RTC count block to clear the timer interrupt flag bit. Write 1 to the INTTMIE bit in the WTCR13 Register of the RTC Register to enable the timer interrupt.

(2) Read the value of the TRANS bit in the WTCR10 Register.

(3) If the value of the TRANS bit is 1, wait until the value becomes 0.

(4) Read the value of the TMRUN bit in the WTCR21 Register and that of the RUN bit in the WTCR10.

(5) Check if the value of the TMRUN bit is 0 (Timer is stopped). If the value of the RUN bit is 0, there is no need to follow step (9) to set the 1 second interrupt.

(6) Write timer setting to WTTR0 Register/ WTTR1 Register/ WTTR2 Register.

(7) Write 0 to the TMEN bit in the WTCR21 Register.

(8) Write 1 to the TMST bit in the WTCR21 Register.

(9) As mentioned in step (5), if the value of the RUN bit is 0, follow step (10). If the value of the RUN bit is 1, set the 1 second interrupt and wait for it.

(10) Write 1 to the CWRITE bit in the WTCR20 register to transfer the setting. Wait until the value of the TRANS bit becomes 0.

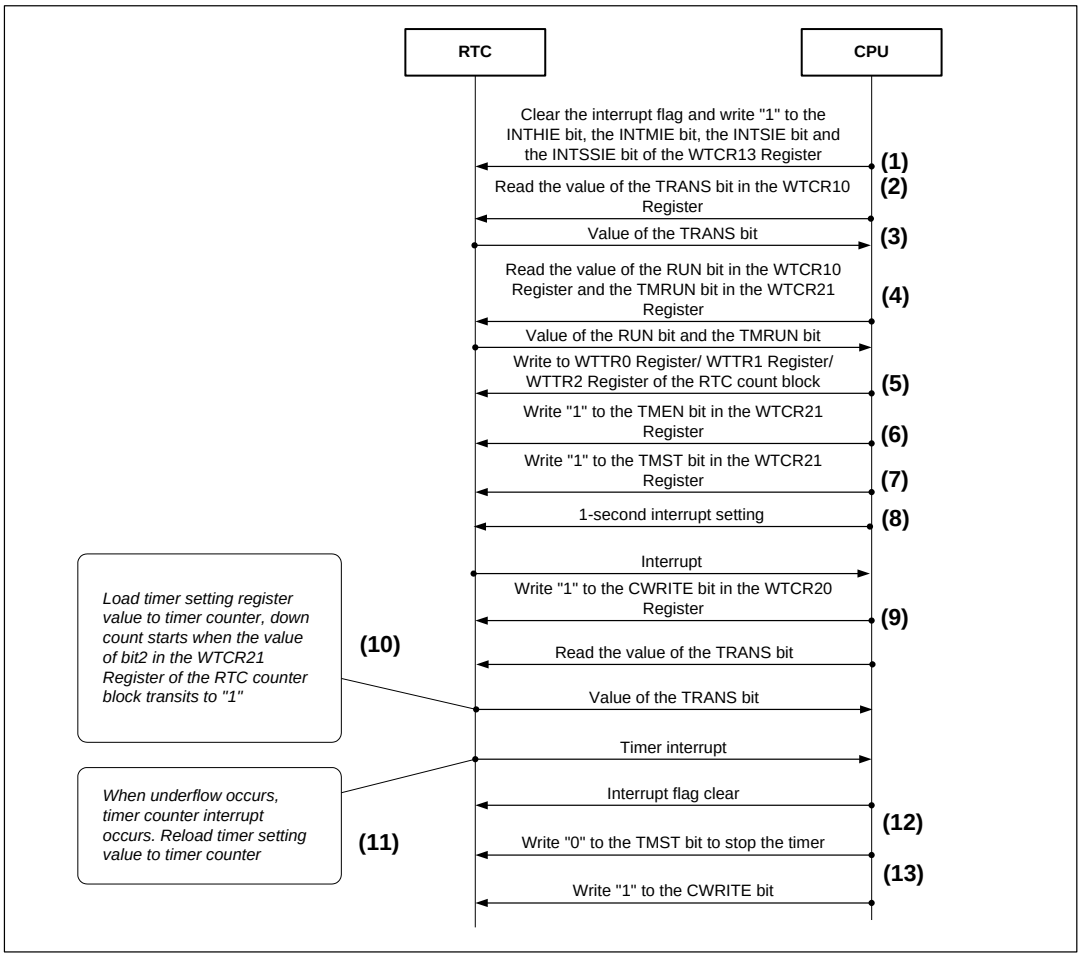
(11) The value of timer setting register transfers to the timer counter and the countdown begins.

(12) When there is underflow during count down, interrupt request occurs. The value of the TMST bit is cleared to 0 and the timer counter stops. After the timer counter has stopped, the value of the TMRUN bit becomes 0.

Notes:

- *During a timer counter operation (WTCR21:TMRUN=1), writing 1 to the TMST bit is prohibited before the TMRUN bit becomes 0 after 0 is written to the TMST bit.*
- *To change the setting of the TMEN bit, do so while the timer counter has stopped (WTCR21:TMRUN=0).*

Figure 3-8 Timer Interrupt Setting Procedures (in Intervals of (Hours, Minutes, and Seconds) Elapsed)



(1) Write 0 to the INTTMI in the WTCR12 register to clear the timer interrupt flag bit. Write 1 to the INTTMIE bit in the WTCR13 register to enable the timer interrupt.

(2) Read the value the TRANS bit in the WTCR10 register.

(3) If the value of the TRANS bit is 1, wait until the value becomes 0.

(4) Read the TMRUN bit in the WTCR21 register to check if the value is 0 (stopped). If the value of the RUN bit is 0, there is no need to follow step (8) to set the 1 second interrupt.

(5) Write timer setting to WTTR0 register/ WTTR1 register/ WTTR2 register of the RTC count block.

(6) Write 1 to the TMEN bit in the WTCR21 register.

(7) Write 1 to the TMST bit in the WTCR21 register.

(8) As mentioned in step (4), if the value of the RUN bit in the WTCR10 register is 0, follow the setting in step (9). If the value of the RUN bit is 1, set the 1 second interrupt and wait for it.

(9) Write 1 to the CWRITE bit in the WTCR20 register, and wait for the value of the TRANS bit to become 0.

(10) The value of timer setting register transfers to the timer counter and the countdown begins.

(11) When the count is completed, the RTC count block interrupt request will occur, and the timer setting register value will be reloaded to the timer counter and the operation will continue.

(12) Write 0 to the INTTMI bit to clear the timer interrupt flag bit.

(13) To stop the timer, write 0 to the TMST bit and 1 to the CWRITE bit.

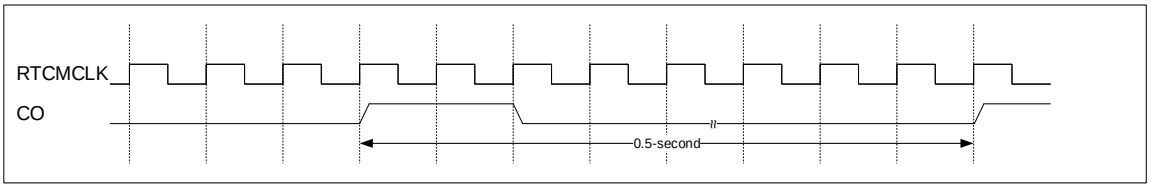
Notes:

- *During a timer counter operation (WTCR21:TMRUN=1), writing 1 to the TMST bit is prohibited before the TMRUN bit becomes 0 after 0 is written to the TMST bit.*
- *To change the setting of the TMEN bit, do so while the timer counter has stopped (WTCR21:TMRUN=0).*

Output Operation of CO External Pin

The RTC count block has CO external pin to output 0.5 second pulse.
Figure 3-9 shows the waveform of CO external pin output.

Figure 3-9 CO External Pin Output Waveform



4. RTC Control Block Reset Operation

This section explains the resetting of the RTC control block.

Low-voltage Detection Reset/ Power-on Reset Operation

The shaded parts in Table 4-1 are target bits of the low-voltage detection reset/ power-on reset. The sub-second generation counter, timer counter and year counter, month counter, day counter, hour counter, minute counter, second counter and day of the week counter not shown in Table 4-1 are not reset targets. Because the INTALI, RUN and TMRUN bits are generated in the VBAT domain, they cannot be cleared by a reset for the Always on domain.

Table 4-1 Low-voltage Detection Reset/ Power-on Reset Target Bits

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WTCR10	TRANS	BUSY	SCRST	SCST	SRST	RUN	-	ST
WTCR11	-	-	-	YEN	MOEN	DEN	HEN	MIEN
WTCR12	INTCRI	INTERI	INTALI	INTTMI	INTHI	INTMI	INTSI	INTSSI
WTCR13	INTCRIE	INTERIE	INTALIE	INTTMIE	INTHIE	INTMIE	INTSIE	INTSSIE
WTCR20	-	-	PWRITE	PREAD	BWRITE	BREAD	CWRITE	CREAD
WTCR21	-	-	-	-	-	TMRUN	TMEN	TMST
WTSR	-	TS2	TS1	TS0	S3	S2	S1	S0
WTMIR	-	TMI2	TMI1	TMI0	MI3	MI2	MI1	MI0
WTHR	-	-	TH1	TH0	H3	H2	H1	H0
WTDR	-	-	TD1	TD0	D3	D2	D1	D0
WTDW	-	-	-	-	-	DW2	DW1	DW0
WTMOR	-	-	-	TMO0	MO3	MO2	MO1	MO0
WTYR	TY3	TY2	TY1	TY0	Y3	Y2	Y1	Y0
ALMIR	-	TAMI2	TAMI1	TAMI0	AMI3	AMI2	AMI1	AMI0
ALHR	-	-	TAH1	TAH0	AH3	AH2	AH1	AH0
ALDR	-	-	TAD1	TAD0	AD3	AD2	AD1	AD0
ALMOR	-	-	-	TAMO0	AMO3	AMO2	AMO1	AMO0
ALYR	TAY3	TAY2	TAY1	TAY0	AY3	AY2	AY1	AY0
WTTR0	TM7	TM6	TM5	TM4	TM3	TM2	TM1	TM0
WTTR1	TM15	TM14	TM13	TM12	TM11	TM10	TM9	TM8
WTTR2	-	-	-	-	-	-	TM17	TM16

System Reset Operation

The shaded parts in Table 4-2 are target bits of the system reset.

The sub-second generation counter (for date and time/ for timer) and the year counter, month counter, day counter, hour counter, minute counter, second counter and day of the week counter are not reset targets.

Table 4-2 System Reset Target Bits

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WTCR10	TRANS	BUSY	SCRST	SCST	SRST	RUN	-	ST
WTCR11	-	-	-	YEN	MOEN	DEN	HEN	MIEN
WTCR12	INTCRI	INTERI	INTALI	INTTMI	INTHI	INTMI	INTSI	INTSSI
WTCR13	INTCRIE	INTERIE	INTALIE	INTTMIE	INTHIE	INTMIE	INTSIE	INTSSIE
WTCR20	-	-	PWRITE	PREAD	BWRITE	BREAD	CWRITE	CREAD
WTCR21	-	-	-	-	-	TMRUN	TMEN	TMST
WTSR	-	TS2	TS1	TS0	S3	S2	S1	S0
WTMIR	-	TMI2	TMI1	TMI0	MI3	MI2	MI1	MI0
WTHR	-	-	TH1	TH0	H3	H2	H1	H0
WTDR	-	-	TD1	TD0	D3	D2	D1	D0
WTDW	-	-	-	-	-	DW2	DW1	DW0
WTMOR	-	-	-	TMO0	MO3	MO2	MO1	MO0
WTYR	TY3	TY2	TY1	TY0	Y3	Y2	Y1	Y0
ALMIR	-	TAMI2	TAMI1	TAMI0	AMI3	AMI2	AMI1	AMI0
ALHR	-	-	TAH1	TAH0	AH3	AH2	AH1	AH0
ALDR	-	-	TAD1	TAD0	AD3	AD2	AD1	AD0
ALMOR	-	-	-	TAMO0	AMO3	AMO2	AMO1	AMO0
ALYR	TAY3	TAY2	TAY1	TAY0	AY3	AY2	AY1	AY0
WTTR0	TM7	TM6	TM5	TM4	TM3	TM2	TM1	TM0
WTTR1	TM15	TM14	TM13	TM12	TM11	TM10	TM9	TM8
WTTR2	-	-	-	-	-	-	TM17	TM16

RTC Reset Operation

The shaded parts in Table 4-3 are target bits of the RTC reset.

The sub-second generation counter (for date and time/ for timer) and the year counter, month counter, day counter, hour counter, minute counter, second counter and day of the week counter, 1 second counter and timer counter not shown in Table 4 3 are not reset targets.

Table 4-3 RTC Reset Target Bits

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WTCR10	TRANS	BUSY	SCRST	SCST	SRST	RUN	-	ST
WTCR11	-	-	-	YEN	MOEN	DEN	HEN	MIEN
WTCR12	INTCRI	INTERI	INTALI	INTTMI	INTHI	INTMI	INTSI	INTSSI
WTCR13	INTCRIE	INTERIE	INTALIE	INTTMIE	INTHIE	INTMIE	INTSIE	INTSSIE
WTCR20	-	-	PWRITE	PREAD	BWRITE	BREAD	CWRITE	CREAD
WTCR21	-	-	-	-	-	TMRUN	TMEN	TMST
WTSR	-	TS2	TS1	TS0	S3	S2	S1	S0
WTMIR	-	TMI2	TMI1	TMI0	MI3	MI2	MI1	MI0
WTHR	-	-	TH1	TH0	H3	H2	H1	H0
WTDR	-	-	TD1	TD0	D3	D2	D1	D0
WTDW	-	-	-	-	-	DW2	DW1	DW0
WTMOR	-	-	-	TMO0	MO3	MO2	MO1	MO0
WTYR	TY3	TY2	TY1	TY0	Y3	Y2	Y1	Y0
ALMIR	-	TAMI2	TAMI1	TAMI0	AMI3	AMI2	AMI1	AMI0
ALHR	-	-	TAH1	TAH0	AH3	AH2	AH1	AH0
ALDR	-	-	TAD1	TAD0	AD3	AD2	AD1	AD0
ALMOR	-	-	-	TAMO0	AMO3	AMO2	AMO1	AMO0
ALYR	TAY3	TAY2	TAY1	TAY0	AY3	AY2	AY1	AY0
WTTR0	TM7	TM6	TM5	TM4	TM3	TM2	TM1	TM0
WTTR1	TM15	TM14	TM13	TM12	TM11	TM10	TM9	TM8
WTTR2	-	-	-	-	-	-	TM17	TM16

Note:

- *After the RTC reset, make sure to write 00h to WTCR12.*

5. Leap Year Compliance of RTC Count Block

This section explains the leap year compliance of the RTC count block.

Leap Year Compliance

Table 5-1 shows the days of each month.

Table 5-1 List of Leap Years

Year	Leap Year	Month											
		1	2	3	4	5	6	7	8	9	10	11	12
00	○	31	29	31	30	31	30	31	31	30	31	30	31
01 to 03	×	31	28	31	30	31	30	31	31	30	31	30	31
04	○	31	29	31	30	31	30	31	31	30	31	30	31
05 to 07	×	31	28	31	30	31	30	31	31	30	31	30	31
08	○	31	29	31	30	31	30	31	31	30	31	30	31
09 to 11	×	31	28	31	30	31	30	31	31	30	31	30	31
12	○	31	29	31	30	31	30	31	31	30	31	30	31
13 to 15	×	31	28	31	30	31	30	31	31	30	31	30	31
16	○	31	29	31	30	31	30	31	31	30	31	30	31
17 to 19	×	31	28	31	30	31	30	31	31	30	31	30	31
20	○	31	29	31	30	31	30	31	31	30	31	30	31
21 to 23	×	31	28	31	30	31	30	31	31	30	31	30	31
24	○	31	29	31	30	31	30	31	31	30	31	30	31
25 to 27	×	31	28	31	30	31	30	31	31	30	31	30	31
28	○	31	29	31	30	31	30	31	31	30	31	30	31
29 to 31	×	31	28	31	30	31	30	31	31	30	31	30	31
32	○	31	29	31	30	31	30	31	31	30	31	30	31
33 to 35	×	31	28	31	30	31	30	31	31	30	31	30	31
36	○	31	29	31	30	31	30	31	31	30	31	30	31
37 to 39	×	31	28	31	30	31	30	31	31	30	31	30	31
40	○	31	29	31	30	31	30	31	31	30	31	30	31
41 to 43	×	31	28	31	30	31	30	31	31	30	31	30	31
44	○	31	29	31	30	31	30	31	31	30	31	30	31
45 to 47	×	31	28	31	30	31	30	31	31	30	31	30	31
48	○	31	29	31	30	31	30	31	31	30	31	30	31
49 to 51	×	31	28	31	30	31	30	31	31	30	31	30	31
52	○	31	29	31	30	31	30	31	31	30	31	30	31
53 to 55	×	31	28	31	30	31	30	31	31	30	31	30	31
56	○	31	29	31	30	31	30	31	31	30	31	30	31
57 to 59	×	31	28	31	30	31	30	31	31	30	31	30	31
60	○	31	29	31	30	31	30	31	31	30	31	30	31
61 to 63	×	31	28	31	30	31	30	31	31	30	31	30	31
64	○	31	29	31	30	31	30	31	31	30	31	30	31
65 to 67	×	31	28	31	30	31	30	31	31	30	31	30	31
68	○	31	29	31	30	31	30	31	31	30	31	30	31
69 to 71	×	31	28	31	30	31	30	31	31	30	31	30	31
72	○	31	29	31	30	31	30	31	31	30	31	30	31
73 to 75	×	31	28	31	30	31	30	31	31	30	31	30	31

Year	Leap Year	Month											
		1	2	3	4	5	6	7	8	9	10	11	12
76	○	31	29	31	30	31	30	31	31	30	31	30	31
77 to 79	×	31	28	31	30	31	30	31	31	30	31	30	31
80	○	31	29	31	30	31	30	31	31	30	31	30	31
81 to 83	×	31	28	31	30	31	30	31	31	30	31	30	31
84	○	31	29	31	30	31	30	31	31	30	31	30	31
85 to 87	×	31	28	31	30	31	30	31	31	30	31	30	31
88	○	31	29	31	30	31	30	31	31	30	31	30	31
89 to 91	×	31	28	31	30	31	30	31	31	30	31	30	31
92	○	31	29	31	30	31	30	31	31	30	31	30	31
93 to 95	×	31	28	31	30	31	30	31	31	30	31	30	31
96	○	31	29	31	30	31	30	31	31	30	31	30	31
97 to 99	×	31	28	31	30	31	30	31	31	30	31	30	31

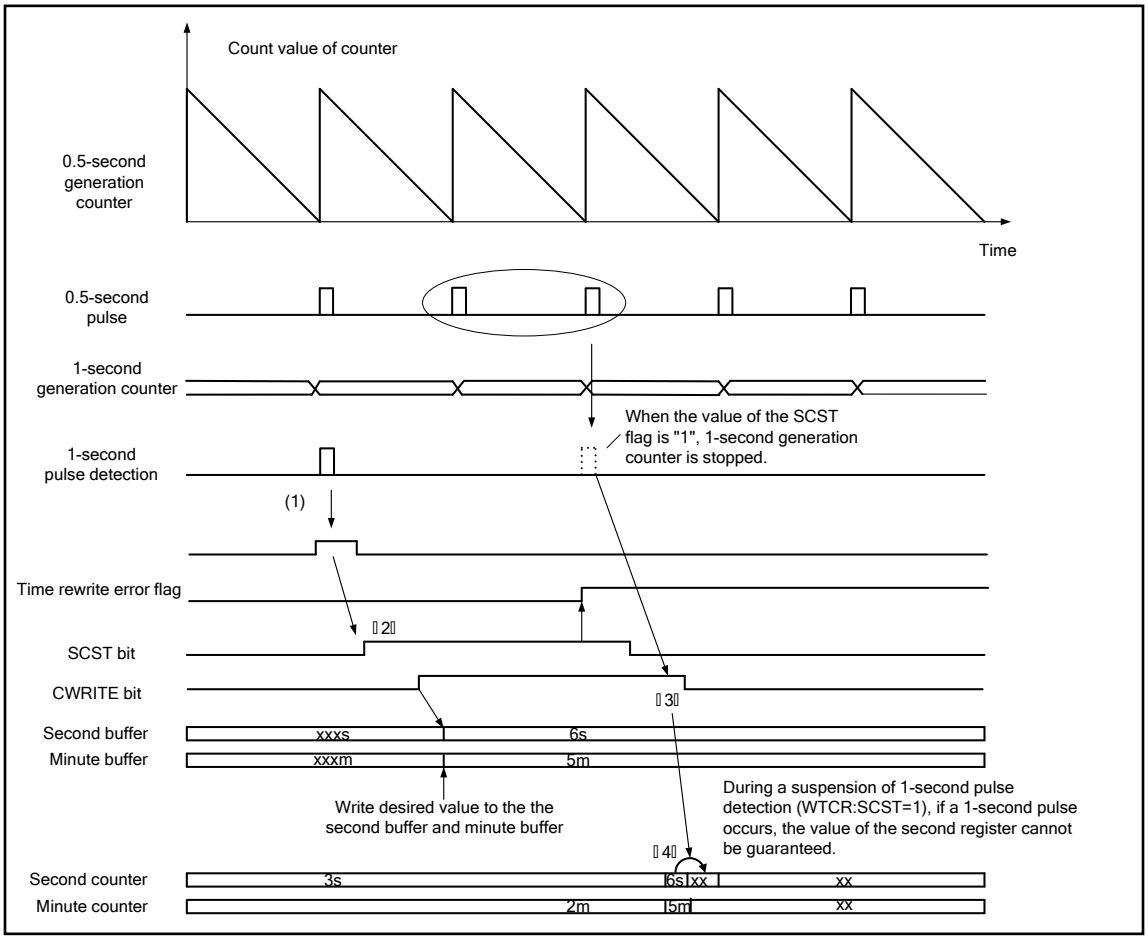
6. Time Rewrite Error

This section explains the time rewrite error during time rewrite (with time count continued).

Time Rewrite Error

Below shows the situation when 0.5 second pulse of the 0.5 second generation counter is detected for twice while the value of the SCST bit remains as 1 during time rewrite (time count continued).

■ When only second counter and minute counter are rewritten.



(1) After the 1 second interrupt is detected, clear the 1 second interrupt flag. Write 1 to the SCST bit and write the counter value.

(2) Set the value of the CWRITE bit to 1 and write the counter value.

(3) When 0.5 second pulse is detected for twice while the value of the SCST flag remains as 1, the value of time rewrite error flag becomes 1.

(4) The value of the second counter, minute counter, hour counter, week counter, month counter and year counter cannot be guaranteed.

Notes:

- *If 0.5 second pulse is detected less than once while the value of the SCST bit remains as 1, the value of time rewrite error flag will not become 1.*
- *When 0.5 second pulse is detected twice while the value of the SCST bit remains as 1, the value of second counter cannot be guaranteed. Therefore, revise the time rewrite value again.*
- *Rewrite the time in 1 second after the 1 second interrupt is detected.*

7. Registers in RTC Control Block

This section shows the list of registers in the RTC control block.

List of Registers in the RTC Control Block

Table 7-1 List of Registers in RTC Control Block

Abbreviation	Register Name	Interface Circuit Type	Reference
WTCR10	Control Register 10	Bit0 ST:2, Bit2 RUN:4	7.1
WTCR11	Control Register 11	2	7.2
WTCR12	Control Register 12	-	7.3
WTCR13	Control Register 13	-	7.4
WTCR20	Control Register 20	1	7.5
WTCR21	Control Register 21	2	7.6
WTSR	Second Register	2	7.7
WTMIR	Minute Register	2	7.8
WTHR	Hour Register	2	7.9
WTDR	Day Register	2	7.10
WTDW	Day of the Week Register	2	7.11
WTMOR	Month Register	2	7.12
WTYR	Year Register	2	7.13
ALMIR	Alarm Minute Register	2	7.14
ALHR	Alarm Hour Register	2	7.15
ALDR	Alarm Day Register	2	7.16
ALMOR	Alarm Month Register	2	7.17
ALYR	Alarm Year Register	2	7.18
WTTR0	Timer Setting Register 0	2	7.19
WTTR1	Timer Setting Register 1	2	7.20
WTTR2	Timer Setting Register 2	2	7.21

The registers shown in Table 7-1 correspond to Circuit Type 1 or 2 or 4 in the chapter VBAT Domain. For the Circuit Type 2, a system reset and RTC reset do not initialize the registers in the VBAT domain. They do, however, initialize the buffers in the Always ON domain. After a reset, therefore, the save operation must be performed after the value is set again or the recall operation is performed. The registers shown circuit type as “-“ don’t influence VBAT domain.

For the details of interface circuit type, refer to Interfacing with Always-on Domain in CHAPTER 7: VBAT Domain in the FM4 Family Peripheral Manual.

Note:

- *After 1 is written to the CWRITE bit, the value of the TRANS bit becomes 0 and the RTC control block buffer value is reflected on the registers in RTC count block (VBAT Domain).*
  During transfer (WTCR10[7]:TRANS=1), do not access any registers of the RTC count block, RTC control block or VBAT domain, except WTCR10.

7.1 Control Register 10 (WTCR 10)

This register controls the operations of the RTC control block.

bit	7	6	5	4	3	2	1	0
Field	TRANS	BUSY	SCRST	SCST	SRST	RUN	Reserved	ST
Attribute	R	R	R/W	R/W	W	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7] TRANS: Transfer flag bit

The TRANS bit indicates if the value is transferring.

When the value of this bit is 1, writing to RTC count block registers is prohibited.

bit	Description
0	Indicates that transfer of value has completed.
1	Indicates that value is transferring.

[bit6] BUSY: Busy bit

The BUSY bit indicates whether time rewrite is operating.

bit	Description
0	Indicates that time rewrite is not operating.
1	Indicates that any of the following conditions is happening: − When 1 is written to the SCST bit in WTCR10 register − When 1 is written to the SCRST bit in the WTCR register − The value of the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR and WTDW are transferring to the year counter, month counter, day counter, hour counter, minute counter, second counter and day of the week counter respectively

[bit5] SCRST: Sub-second generation/ 1 second generation counter reset bit

The SCRST bit controls the reset of the sub-second generation/ 1 second generation counter (for date and time)

bit	Description
0	Cancel the sub-second generation/ 1 second generation counter (for date and time) reset.
1	Reset the sub-second generation/ 1 second generation counter (for date and time).

If the value of this bit and that of the SCST bit are both set to 0 during the RTC operation (RUN=1), the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR and WTDW cannot be updated. Setting the value of SCST bit and that of the SCRST bit to 1 simultaneously is prohibited. When RTC operation has stopped (RUN=0), setting the value of this bit to 1 is prohibited.

When the SCRST bit is 1, setting the SRST bit to 1 is prohibited.

[bit4] SCST: 1 second pulse detection stop bit

The SCST bit controls the detection of 1 second pulse of 1 second generation counter.

bit	Description
0	Enable detection of 1 second pulse.
1	Stop Detection of 1 second pulse.

If this bit and SCRST bit are both set to 0 during the RTC operation (RUN=1), the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR and WTDW cannot be updated. Setting the value of SCST bit and SCRST bit to 1 simultaneously is prohibited. When RTC is stopped (RUN=0), setting the value of this bit to 1 is prohibited.

When the SCST bit is 1, setting the SRST bit to 1 is prohibited.

[bit3] SRST: RTC reset bit

The SRST bit is the RTC reset bit.
See Table 4-3 in chapter RTC Control Block Reset Operation for the registers or bits that are initiated by RTC reset.
This bit always reads 0.

bit	Description
read	Always read as 0
0 is written	No effect on operation.
1 is written	The hardware issues the RTC reset.

Write 1 to this bit, after confirming that the time rewrite operation active bit (BUSY) is 0.

[bit2] RUN: RTC count block operation bit

The RUN bit indicates the operation state of the RTC count block.
During RTC count block operation (WTCR10:ST=1), set the ST bit to 0 will stop the RTC count block operation and the value of the RUN bit will become0.

bit	Description
0	RTC count block is stopped.
1	RTC count block is operating.

[bit1] Reserved: Reserved bit

Always read as 0.
Set the value of this bit to 0 when writing.

[bit0] ST: Start bit

The ST bit controls the startup of the RTC count block.

1 cannot be written, when the sub-oscillation is stopped.

bit	Description
0	Stops the RTC count block.
1	Transfers the setting of the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR, and WTDW to the year counter, month counter, day counter, hour counter, minute counter, second counter, and day of the week counter respectively, and the RTC count block operation starts.

Note:

- *After the RTC reset, make sure to write 00h to WTCR12.*

7.2 Control Register 11 (WTCR 11)

This register controls the interrupt enable of the RTC control block.

bit	7	6	5	4	3	2	1	0
Field	Reserved			YEN	MOEN	DEN	HEN	MIEN
Attribute	R			R/W	R/W	R/W	R/W	R/W
Initial value	000			0	0	0	0	0

[bit7:5] Reserved: Reserved bits

Always read as 0.

Set the value of this bit to 0 when writing.

[bit4] YEN: Alarm year register enable bit

The YEN bit enables the comparison between the ALYR and the year counter. When the value of this bit is set to 1, this bit becomes the detection target of the alarm coincidence flag (INTALI).

bit	Description
0	Prohibit comparison of the ALYR and the year counter.
1	Enable the comparison between the ALYR and the year counter.

[bit3] MOEN: Alarm month register enable bit

The MOEN bit enables the comparison between the ALMOR and the month counter. When the value of this bit is set to 1, this bit becomes the detection target of the alarm coincidence flag (INTALI).

bit	Description
0	Prohibit comparison between the ALMOR and the month counter.
1	Enable the comparison between the ALMOR and the month counter.

[bit2] DEN: Alarm day register enable bit

The DEN bit enables the comparison between the ALDR and the day counter. When the value of this bit is set to 1, this bit becomes the detection target of the alarm coincidence flag (INTALI).

bit	Description
0	Prohibit comparison between the ALDR and the day counter.
1	Enable comparison between the ALDR and the day counter.

[bit1] HEN: Alarm hour register enable bit

The HEN bit enables the comparison between the ALHR and the hour counter. When the value of this bit is set to 1, this bit becomes the detection target of the alarm coincidence flag (INTALI).

bit	Description
0	Prohibit comparison between the ALHR and the hour counter.
1	Enable comparison between the ALHR and the hour counter.

[bit0] MIEN: Alarm minute register enable bit

The MIEN bit enables the comparison between the ALMIR and the minute counter. When the value of this bit is set to 1, this bit becomes the detection target of the alarm coincidence flag (INTALI).

bit	Description
0	Prohibit comparison between the ALMIR and the minute counter.
1	Enable comparison between the ALMIR and the minute counter.

7.3 Control Register 12 (WTCR 12)

This is the RTC control block interrupt flag register.

bit	7	6	5	4	3	2	1	0
Field	INTCRI	INTERI	INTALI	INTTMI	INTHI	INTMI	INTSI	INTSSI
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7] INTCRI: Year/ month/ day/ hour/ minute/ second/ day of the week counter value read completion flag bit

According to the CREAD bit, the INTCRI bit indicates the transfer state of the value of the year counter, month counter, day counter, hour counter, minute counter, second counter and the day of the week counter to the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR, and WTDW when the date and time is read.

During read access of read modify right access, 1 is always read.

bit	Description
When 0 is read	Reading of the value of the year counter, month counter, day counter, hour counter, minute counter, second counter and the day of the week counter has not completed.
When 1 is read	Reading of the value of the year counter, month counter, day counter, hour counter, minute counter, second counter and the day of the week counter has completed.
When 0 is written	Clear this flag.
When 1 is written	No effect on operation.

[bit6] INTERI: Time rewrite error flag bit

During time rewrite (SCST=1), the INTERI indicates that the second counter does not count up.

During read access of read modify right access, 1 is always read.

Bit	Description
When 0 is read	Time rewrite error is not occurring.
When 1 is read	Time rewrite error has occurred.
When 0 is written	Clear this flag.
When 1 is written	No effect on operation.

[bit5] INTALI: Alarm coincidence flag bit

The INTALI bit indicates if the value of the ALYR, ALMOR, ALDR, ALHR, or ALMIR coincides with the value of the year counter, month counter, day counter, hour counter, or minute counter.

During read access of read modify right access, 1 is always read.

Bit	Description
When 0 is read	Alarm coincidence is not occurring.
When 1 is read	Alarm coincidence occurred.
When 0 is written	This flag is cleared.
When 1 is written	No effect on operation.

[bit4] INTTMI: Timer underflow detection flag bit

When timer counter underflows, the value of the INTTMI bit becomes 1.
During read access of read modify right access, 1 is always read.

bit	Description
When 0 is read	Timer underflow is not occurring.
When 1 is read	Timer underflow occurred.
When 0 is written	This flag is cleared.
When 1 is written	No effect on operation.

[bit3] INTHI: Every hour flag bit

When hour counter counts up, the value of the INTHI bit becomes 1.
During read access of read modify right access, 1 is always read.

Bit	Description
When 0 is read	Hour counter count up is not occurring.
When 1 is read	Hour counter count up occurred.
When 0 is written	Clear this flag.
When 1 is written	No effect on operation.

[bit2] INTMI: Every minute flag bit

When minute counter counts up, the value of the INTMI bit becomes 1.
During read access of read modify right access, 1 is always read.

Bit	Description
When 0 is read	Minute counter count up is not occurring.
When 1 is read	Minute counter count up occurred.
When 0 is written	Clear this flag.
When 1 is written	No effect on operation.

[bit1] INTSI: Every second flag bit

When second counter counts up, the value of the INTSI bit becomes 1.
During read access of read modify right access, 1 is always read.

bit	Description
When 0 is read	Second counter count up is not occurring.
When 1 is read	Second counter count up occurred.
When 0 is written	Clear this flag.
When 1 is written	No effect on operation.

[bit0] INTSSI: Every 0.5 second flag bit

When 0.5 second pulse occurs, the value of the INTSSI bit becomes 1.
During read access of read modify right access, 1 is always read.

Bit	Description
When 0 is read	0.5 second pulse is not occurring.
When 1 is read	0.5 second pulse occurred.
When 0 is written	Clear this flag.
When 1 is written	No effect on operation.

7.4 Control Register 13 (WTCR 13)

This is the RTC control block interrupt enable register.

bit	7	6	5	4	3	2	1	0
Field	INTCRIE	INTERIE	INTALIE	INTTMIE	INTHIE	INTMIE	INTSIE	INTSSIE
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7] INTCRIE: Year/ month/ day/ hour/ minute/ second/ day of the week counter value read completion interrupt enable bit

The INTCRIE bit enables the year/ month/ day/ hour/ minute/ second/ day of the week counter value read completion interrupt.

bit	Description
0	Interrupt prohibited.
1	Interrupt enabled.

[bit6] INTERIE: Time rewrite error interrupt enable bit

The INTERIE bit enables the time rewrite error interrupt.

bit	Description
0	Interrupt prohibited.
1	Interrupt enabled.

[bit5] INTALIE: Alarm coincidence interrupt enable bit

The INTALIE bit enables the alarm coincidence interrupt.

bit	Description
0	Interrupt prohibited.
1	Interrupt enabled.

[bit4] INTTMIE: Timer underflow interrupt enable bit

The INTTMIE bit enables the timer underflow interrupt.

bit	Description
0	Interrupt prohibited.
1	Interrupt enabled.

[bit3] INTHIE: Every hour interrupt enable bit

The INTHIE bit enables the every hour interrupt.

bit	Description
0	Interrupt prohibited.
1	Interrupt enabled.

[bit2] INTMIE: Every minute interrupt enable bit

The INTMIE bit enables the every minute interrupt.

bit	Description
0	Interrupt prohibited.
1	Interrupt enabled.

[bit1] INTSIE: Every second interrupt enable bit

The INTSIE bit enables the every second interrupt.

bit	Description
0	Interrupt prohibited.
1	Interrupt enabled.

[bit0] INTSSIE: Every 0.5 second interrupt enable bit

The INTSSIE bit enables the every 0.5 second interrupt.

bit	Description
0	Interrupt prohibited.
1	Interrupt enabled.

7.5 Control Register 20 (WTCR 20)

This register controls the save operation and recall operation.

bit	7	6	5	4	3	2	1	0
Field	Reserved		PWRITE	PREAD	BWRITE	BREAD	CWRITE	CREAD
Attribute	R		R/W	R/W	R/W	R/W	R/W	R/W
Initial value	00		0	0	0	0	0	0

[bit7:6] Reserved: Reserved bits

Always read as 0.

Set the value of this bit to 0 when writing.

[bit5] PWRITE: VBAT PORT save control bit

When the value of the PWRITE bit is set to 1, the buffer value set in the Always ON Domain will start saving to the VBAT Domain. During read access of read modify right access, 0 is always read.

bit	Description
0 is read	Saving to the VBAT Domain has completed.
1 is read	Value is saving to the VBAT Domain.
0 is written	No effect on operation.
1 is written	Start to save buffer value from the Always ON Domain to the VBAT Domain.

[bit4] PREAD: VBAT PORT recall control bit

When the value of the PREAD bit is set to 1, the buffer value set in the VBAT Domain will start recalling to the Always ON Domain. During read access of read modify right access, 0 is always read.

bit	Description
0 is read	Recalling from the VBAT Domain has completed.
1 is read	Value is recalling from the VBAT Domain.
0 is written	No effect on operation.
1 is written	Start to recall register value from the VBAT Domain to the Always ON Domain.

[bit3] BWRITE: Backup register save control bit

When the value of the PWRITE bit is set to 1, the buffer value set in the Always ON Domain will start saving to the VBAT Domain. During read access of read modify right access, 0 is always read.

bit	Description
0 is read	Saving to the VBAT Domain has completed.
1 is read	Value is saving to the VBAT Domain.
0 is written	No effect on operation.
1 is written	Start to save buffer value from the Always ON Domain to the VBAT Domain.

[bit2] BREAD: Backup register recall control bit

When the value of the BREAD bit is set to 1, the register value set in the VBAT Domain will start recalling to the Always ON Domain. During read access of read modify right access, 0 is always read.

bit	Description
0 is read	Recalling from the VBAT Domain has completed.
1 is read	Value is recalling from the VBAT Domain.
0 is written	No effect on operation.
1 is written	Start to recall register value from the VBAT Domain to the Always ON Domain.

[bit1] CWRITE: RTC setting save control bit

When the value of the PWRITE bit is set to 1, the buffer value set in the Always ON Domain will start saving to the VBAT Domain.
During read access of read modify right access, 0 is always read.

1 cannot be written when the sub-oscillation is stopped.

bit	Description
0 is read	Saving to the VBAT Domain has completed.
1 is read	Value is saving to the VBAT Domain.
0 is written	No effect on operation.
1 is written	Start to save buffer from the Always ON Domain to the VBAT Domain.

[bit0] CREAD: RTC setting recall control bit

When the value of the BREAD bit is set to 1, the register value set in the VBAT Domain will start recalling to the Always ON Domain. During read access of read modify right access, 0 is always read.

1 cannot be written when the sub-oscillation is stopped.

bit	Description
0 is read	Recalling to the VBAT Domain has completed.
1 is read	Value is recalling to the VBAT Domain.
0 is written	No effect on operation.
1 is written	Start to recall register value from the Always ON Domain to the VBAT Domain.

Notes:

- *During transfer (WTCR10[7]:TRANS=1), do not access any registers of the RTC count block, RTC control block or VBAT domain, except WTCR10.*
- *There are restrictions on the combination of simultaneous transfer. See "Circuit connected to interface circuit" in Chapter VBAT Domain in the Peripheral Manual for restrictions on combination of simultaneous transfer details and transfer target registers.*

7.6 Control Register 21 (WTCR 21)

This register control timer operation of the RTC count block.

bit	7	6	5	4	3	2	1	0
Field	Reserved					TMRUN	TMEN	TMST
Attribute	R					R	R/W	R/W
Initial value	00000					0	0	0

[bit7:3] Reserved: Reserved bits

Always read as 0.

Set the value of this bit to 0 when writing.

[bit2] TMRUN: Timer counter operation bit

The TMRUN bit indicates the operation of timer counter.

If the timer counter control bit (TMEN) is 0, timer counter counts up and this bit will be cleared by the hardware. If the value of the TMEN bit is 1, remain the value of the TMRUN bit as 1 until 0 is written to the TMST bit.

During a timer operation (TMST=1), setting 0 to the TMST bit will stop the timer operation and the value of this bit will become 0.

bit	Description
0	Timer counter is stopped.
1	Timer counter is operating.

[bit1] TMEN: Time counter control bit

The TMEN bit controls whether the time counter operates after a specific time (hour, minute, second) or at a specific interval (hour, minute, second).

1 cannot be written when the sub-oscillation is stopped.

bit	Description
0	Time counter operates after a specific time (hour, minute, second)
1	Time counter operates at a specific interval (hour, minute, second)

[bit0] TMST: Time counter start bit

The TMST bit starts the time counter.

If the value of the TMEN bit is 0, the value of the TMST bit will be cleared to 0 by the hardware once the count has completed.

See time counter operation bit (TMRUN) for the time counter operation state. To rewrite the time setting register, do so after stopping this bit by writing 0 to it. Then rewrite the time setting register and write 1 to this bit to resume the operation.

1 cannot be written when the sub-oscillation is stopped.

bit	Description
0	Timer counter is stopped.
1	Timer counter starts operating.

7.7 Second Register (WTSR)

This register indicates the second information in the RTC count block. The register value is shown in Binary-Coded Decimal.

bit	7	6	5	4	3	2	1	0
Field	Reserved	TS2	TS1	TS0	S3	S2	S1	S0
Attribute	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7] Reserved: Reserved bit

Always read as 0.

Set the value of this bit to 0 when writing.

[bit6:4] TS2-TS0: Second register

The TS2 to TS0 bits show the 2nd digit of the second information in the RTC count block.

0 to 5: Valid

6, 7: Setting is prohibited

[bit3:0] S3-S0: Second register

The S3 to S0 bits show the 1st digit of the second information in the RTC count block.

0 to 9: Valid

A to F: Setting is prohibited

7.8 Minute Register (WRMIR)

This register indicates the minute information in the RTC count block. The register value is shown in BCD.

bit	7	6	5	4	3	2	1	0
Field	Reserved	TMI2	TMI1	TMI0	MI3	MI2	MI1	MI0
Attribute	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7] Reserved: Reserved bit

Always read as 0.

Set the value of this bit to 0 when writing.

[bit6:4] TMI2-TMI0: Minute register

The TMI2 to TMI0 bits show the 2nd digit of the minute information in the RTC count block.

0 to 5: Valid

6, 7: Setting is prohibited

[bit3:0] MI3-MI0: Minute register

The MI3 to MI0 bits show the 1st digit of the minute information in the RTC count block.

0 to 9: Valid

A to F: Setting is prohibited

7.9 Hour Register (WTHR)

This register indicates the hour information in the RTC count block. The register value is shown in BCD.

bit	7	6	5	4	3	2	1	0
Field	Reserved		TH1	TH0	H3	H2	H1	H0
Attribute	R		R/W	R/W	R/W	R/W	R/W	R/W
Initial value	00		0	0	0	0	0	0

[bit7:6] Reserved: Reserved bits

Always read as 0.

Set the value of this bit to 0 when writing.

[bit5:4] TH1, TH0: Hour register

The TH1 bit and TH0 bit show the 2nd digit of the hour information in the RTC count block.

0 to 2: Valid

3: Setting is prohibited

[bit3:0] H3-H0: Hour register

The H3 to H0 bits show the 1st digit of the hour information in the RTC count block.

0 to 9: Valid

A to F: Setting is prohibited

7.10 Day Register (WTDR)

This register indicates the day information in the RTC count block. The register value is shown in BCD.

bit	7	6	5	4	3	2	1	0
Field	Reserved		TD1	TD0	D3	D2	D1	D0
Attribute	R		R/W	R/W	R/W	R/W	R/W	R/W
Initial value	00		0	0	0	0	0	0

[bit7:6] Reserved: Reserved bits

Always read as 0.

Set the value of this bit to 0 when writing.

[bit5:4] TD1, TD0: Day register

The TD1 bit and TD0 bit show the 2nd digit of the day information in the RTC count block.

[bit3:0] D3-D0: Day register

The D3 to D0 bits show the 1st digit of the day information in the RTC count block.

0 to 9: Valid

A to F: Setting is prohibited

7.11 Day of the Week Register (WTDW)

This register indicates the day of the week information in the RTC count block. The register value is shown in BCD.

bit	7	6	5	4	3	2	1	0
Field	Reserved					DW2	DW1	DW0
Attribute	R					R/W	R/W	R/W
Initial value	00000					0	0	0

[bit7:3] Reserved: Reserved bits

Always read as 0.

Set the value of this bit to 0 when writing.

[bit2:0] DW2-DW0: Day of the week register

The DW2 to DW0 bits show the day of the week information in the RTC count block.

0: Sun
1: Mon
2: Tues
3: Wed
4: Thurs
5: Fri
6: Sat
7: Setting is prohibited.

7.12 Month Register (WTMOR)

This register indicates the month information in the RTC count block. The register value is shown in BCD.

bit	7	6	5	4	3	2	1	0
Field	Reserved			TMO0	MO3	MO2	MO1	MO0
Attribute	R			R/W	R/W	R/W	R/W	R/W
Initial value	000			0	0	0	0	0

[bit7:5] Reserved: Reserved bits

Always read as 0.

Set the value of this bit to 0 when writing.

[bit4] TMO0: Month register

The TMO0 bit shows the 2nd digit of the month information in the RTC count block.

[bit3:0] MO3-MO0: Month register

The MO3 to MO0 bits show the 1st digit of the month information in the RTC count block.

0 to 9: Valid

A to F: Setting is prohibited

7.13 Year Register (WTYR)

This register indicates the year information in the RTC count block. The register value is shown in BCD.

bit	7	6	5	4	3	2	1	0
Field	TY3	TY2	TY1	TY0	Y3	Y2	Y1	Y0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7:4] TY3-TY0: Year register

The TY3 to TY0 bits show the 2nd digit of the year information in the RTC count block.

0 to 9: Valid
A to F: Setting is prohibited

[bit3:0] Y3-Y0: Year register

The Y3 to Y0 bits show the 1st digit of the year information in the RTC count block.

0 to 9: Valid
A to F: Setting is prohibited

7.14 Alarm Minute Register (ALMIR)

This register indicates the minute information in alarm setting.

bit	7	6	5	4	3	2	1	0
Field	Reserved	TAMI2	TAMI1	TAMI0	AMI3	AMI2	AMI1	AMI0
Attribute	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7] Reserved: Reserved bit

Always read as 0.

Set the value of this bit to 0 when writing.

[bit6:4] TAMI2-TAMI0: Alarm minute register

The TAMI2 to TAMI0 bits show the 2nd digit of the minute information in the alarm setting.

0 to 5: Valid

6, 7: Setting is prohibited

[bit3:0] AMI3-AMI0: Alarm minute register

The AMI3 to AMI0 bits show the 1st digit of the minute information in the alarm setting.

0 to 9: Valid

A to F: Setting is prohibited

7.15 Alarm Hour Register (ALHR)

This register indicates the hour information in alarm setting.

bit	7	6	5	4	3	2	1	0
Field	Reserved		TAH1	TAH0	AH3	AH2	AH1	AH0
Attribute	R		R/W	R/W	R/W	R/W	R/W	R/W
Initial value	00		0	0	0	0	0	0

[bit7:6] Reserved: Reserved bits

Always read as 0.

Set the value of this bit to 0 when writing.

[bit5:4] TAH1, TAH0: Alarm hour register

The TAH1 bit and TAH0 bit show the 2nd digit of the hour information in the alarm setting.

0 to 2: Valid

3: Setting is prohibited

[bit3:0] AH3-AH0: Alarm hour register

The AH3 to AH0 bits show the 1st digit of the hour information in the alarm setting.

0 to 9: Valid

A to F: Setting is prohibited

7.16 Alarm Day Register (ALDR)

This register indicates the day information in alarm setting.

bit	7	6	5	4	3	2	1	0
Field	Reserved		TAD1	TAD0	AD3	AD2	AD1	AD0
Attribute	R		R/W	R/W	R/W	R/W	R/W	R/W
Initial value	00		0	0	0	0	0	0

[bit7:6] Reserved: Reserved bits

Always read as 0.

Set the value of this bit to 0 when writing.

[bit5:4] TAD1, TAD0: Alarm day register

The TAD1 bit and TAD0 bit show the 2nd digit of the day information in the alarm setting.

[bit3:0] AD3-AD0: Alarm day register

The AD3 to AD0 bits show the 1st digit of the day information in the alarm setting.

0 to 9: Valid

A to F: Setting is prohibited

7.17 Alarm Month Register (ALMOR)

This register indicates the month information in alarm setting.

bit	7	6	5	4	3	2	1	0
Field	Reserved			TAMO0	AMO3	AMO2	AMO1	AMO0
Attribute	R			R/W	R/W	R/W	R/W	R/W
Initial value	000			0	0	0	0	0

[bit7:5] Reserved: Reserved bits

Always read as 0.

Set the value of this bit to 0 when writing.

[bit4] TAMO0: Alarm month register

The TAMO0 bit shows the 2nd digit of the month information in the alarm setting.

[bit3:0] AMO3-AMO0: Alarm month register

The AMO3 to AMO0 bits show the 1st digit of the month information in the alarm setting.

0 to 9: Valid

A to F: Setting is prohibited

7.18 Alarm Year Register (ALYR)

This register indicates the year information in alarm setting.

bit	7	6	5	4	3	2	1	0
Field	TAY3	TAY2	TAY1	TAY0	AY3	AY2	AY1	AY0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7:4] TAY3-TAY0: Alarm year register

The TAY3 to TAY0 bits show the 2nd digit of the year information in the alarm setting.

0 to 9: Valid
A to F: Setting is prohibited

[bit3:0] AY3-AY0: Alarm year register

The AY3 to AY0 bits show the 1st digit of the year information in the alarm setting.

0 to 9: Valid
A to F: Setting is prohibited

7.19 Time Setting Register 0 (WTTR0)

This register sets a future time (in hours, minutes and seconds) or an interval (in hours, minutes and seconds) for the timer.
The value can be set from 1 second up to 1 day.

bit	7	6	5	4	3	2	1	0
Field	TM7	TM6	TM5	TM4	TM3	TM2	TM1	TM0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7:0] TM7-TM0: Timer Setting register

The TM7 to TM0 bits are timer setting information bits.

WTTR0 sets the 7 bit to 0 bit of time setting register. Use the WTTR0 register/ WTTR1 register/ WTTR2 register to set the timer.

Set the timer to a future time (in hours, minutes and seconds) or to an interval (in hours, minutes and seconds) within a day.

It is possible to set the time from 1 second up to 1 day at 0.5 second interval.

Check the setting to timer setting registers by the following formula.

TM [17:0] = (Time set[s] × 2) -1

1 to 172799 : Valid
0, 172800 to 262143: Setting is prohibited

7.20 Time Setting Register 1 (WTTR1)

This register sets a future time (in hours, minutes and seconds) or an interval (in hours, minutes and seconds) for the timer.
The value can be set from 1 second up to 1 day.

bit	7	6	5	4	3	2	1	0
Field	TM15	TM14	TM13	TM12	TM11	TM10	TM9	TM8
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7:0] TM15-TM8: Timer Setting register

These are the timer setting information bit.

WTTR1 sets the 15 bit to 8 bit of time setting register. Use the WTTR0 register/ WTTR1 register/ WTTR2 register to set the timer.

See 7.19 Time Setting Register 0 (WTTR0) for the setting to time setting register.

7.21 Time Setting Register 2 (WTTR2)

This register sets a future time (in hours, minutes and seconds) or an interval (in hours, minutes and seconds) for the timer. The value can be set from 1 second up to 1 day.

bit	7	6	5	4	3	2	1	0
Field	Reserved						TM17	TM16
Attribute	R						R/W	R/W
Initial value	000000						0	0

[bit7:2] Reserved: Reserved bits

Always read as 0.

Set the value of this bit to 0 when writing.

[bit1:0] TM17-TM16: Timer Setting register

These are the timer setting information bit.

WTTR1 sets the 17bit, 16bit of time setting register. Use the WTTR0 register/ WTTR1 register/ WTTR2 register to set the timer.

See 7.19 Time Setting Register 0 (WTTR0) for the setting to time setting register.

8. Usage Precautions

Note the following when using the RTC count block.

- Use PCLK2 (APB2 bus clock) with frequency 1 MHz or more.
- During time rewrite, always perform CWRITE after performing CREAD operation.
- To change the setting of the alarm registers, do so when the value of the alarm interrupt data control bits (WTCR11:YEN, WTCR11:MOEN, WTCR11:DEN, WTCR11:HEN, WTCR11:MIEN) are 0.
- If the value of any of the alarm interrupt data control bits (WTCR11:YEN, WTCR11:MOEN, WTCR11:DEN, WTCR11:HEN, WTCR11:MIEN) is set to 1, interrupt occurs immediately. Therefore, read and check the value of date and time after the interrupt.
- When WTCR10:TRANS is 1, access to any registers of the RTC count block, RTC control block or VBAT domain is prohibited.
- Do not stop the RTCMCLK during transfer.
- Complete transfer of time continue rewrite in 1 second after 1 second interrupt.
- When the Always ON Domain is reset with SCST assert (WTCR10:SCST=1), time lag may occur. Therefore, rewrite the time with the SCST bit again. After reset is canceled, if the value of the BUSY bit remains as 1, there is a need to reset.
- Write 1 to the RTC reset bit after confirming that the time rewrite operation active bit (BUSY) is 0.
- To use the RTC count block, use it after writing 0 to the Power-on bit (VDET:PON) (See 6.7 VDET register in chapter VBAT Domain in the Peripheral Manual)

CHAPTER 4-3: RTC Count Block (B)

This chapter explains the functions and operations of the RTC count block(B).

1. Overview of RTC Count Block
2. Block Diagram of RTC Count Block
3. Operations of RTC Count Block and Setting Procedures
4. RTC Control Block Reset Operation
5. Leap Year Compliance of RTC Count Block
6. Time Rewrite Error
7. Registers in RTC Control Block
8. Usage Precautions

1. Overview of RTC Count Block

The RTC count block counts date and time (year, month, day, hour, minute, second and day of the week) from 00 year to 99 year, and also sets an alarm and a timer. The block can set an alarm for a specific time (year, month, day, hour, minute) or for a specific year/month/day/hour/minute. It can also set the timer to a future time (in hours, minutes and seconds) or to an interval (in hours, minutes and seconds) within a day. An overview of the RTC count block is shown below.

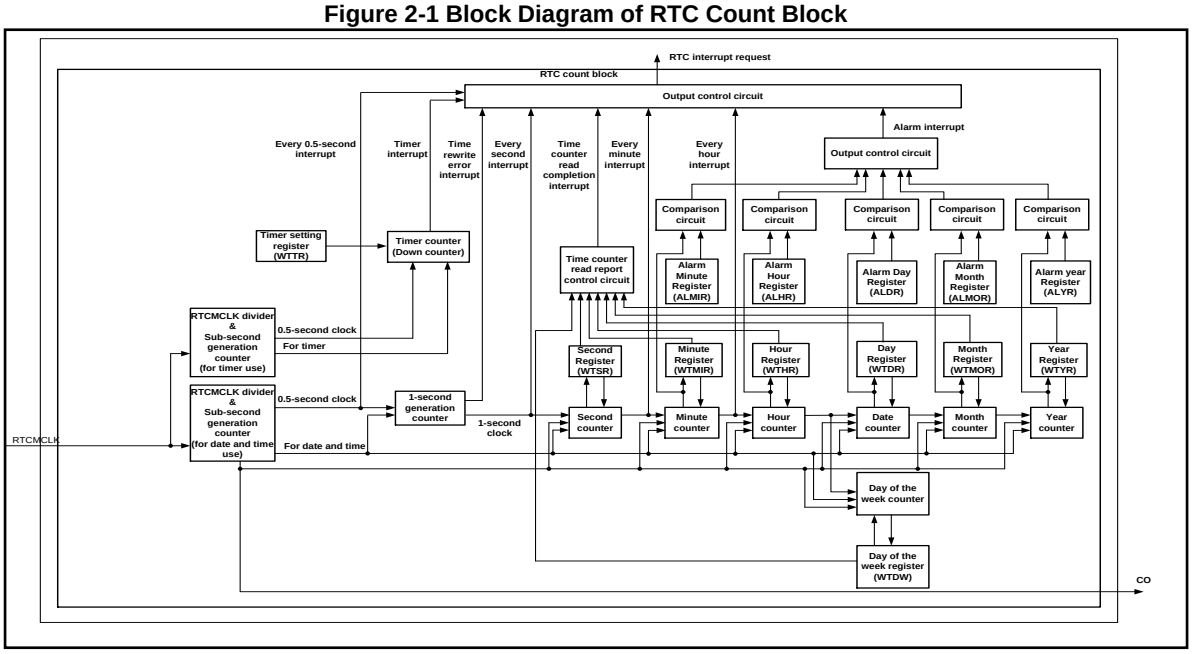
Overview of Functions of RTC Count Block

- Setting date and time (year, month, date, hour, minute, second, day of the week)
- Counting date and time (year (00 to 99), month, day, hour, minute, second and day of the week)
- Leap year compliance (00 year is operated as leap year)
- Alarm for a specific time (year, month, day, hour, minute)
- Alarm for a specific year/month/day/hour/minute
- Timer for a future time (in hours, minutes or seconds) or to an interval (in hours, minutes or seconds) within a day
- The RTC count block can reset the watch count of the RTC count block and modify the time for setting the time by the time signal.
- For changing time zone, the RTC count block can rewrite the time while keeping the watch count of the RTC count block running.(If the rewriting of the time is completed within 1 second, the RTC count block can keep counting the time without being interrupted.)
- The RTC count block can output the following interrupts:
  - Alarm (an interrupt to be generated at a designated date and time)
  - Every hour
  - Every minute
  - Every second
  - Every 0.5 second
  - Timer
  - Time rewrite error
  - Time counter read completion
  - Pulse output every 0.5 second

2. Block Diagram of RTC Count Block

Figure 2-1 shows the block diagram of the RTC count block.

Figure 2-1 Block Diagram of RTC Count Block



RTCMCLK Divider and Sub-second Generation Counter (for Timer)

The RTCMCLK divider generates a timer clock. The sub-second generation counter (for timer) operates using the clock generated by the RTCMCLK divider and counts the time by the sub-second (0.5 second).

RTCMCLK Divider and Sub-second Generation Counter (for Date and Time)

The RTCMCLK divider generates a date and clock. The sub-second generation counter (for date and time) operates using the clock generated by the RTCMCLK divider and counts the time by the sub-second (0.5 second).

Timer Setting Register (WTTR)

This register stores the future time (in hours, minutes and seconds) and the interval (in hours, minutes, and seconds) for the timer.

Timer Counter (Down Counter)

The timer counter counts down the value set in the Timer Setting Register with 0.5 second pulse that is output by the sub-second generation counter (for timer). This function is placed in Always on domain.

1 second Generation Counter

The timer counter generates 1 second pulses by counting 0.5 second pulses that the sub-second generation counter (for date and time) outputs.

Second Counter, Minute Counter, Hour Counter, Day Counter, Month Counter, Year Counter, and Day of the Week Counter

These counters count seconds, minutes, hours, days, months, years and days of the week respectively.

Second register (WTSR), Minute Register (WTMIR), Hour Register (WTHR), Day Register (WTDR), Month Register (WTMOR), and Year Register (WTYR)

These registers indicate the following data of the RTC count block respectively: second, minute, hour, day, month, and year.

Time Counter Read Report Control Circuit

This circuit reports the completion of the reading of the time counter.

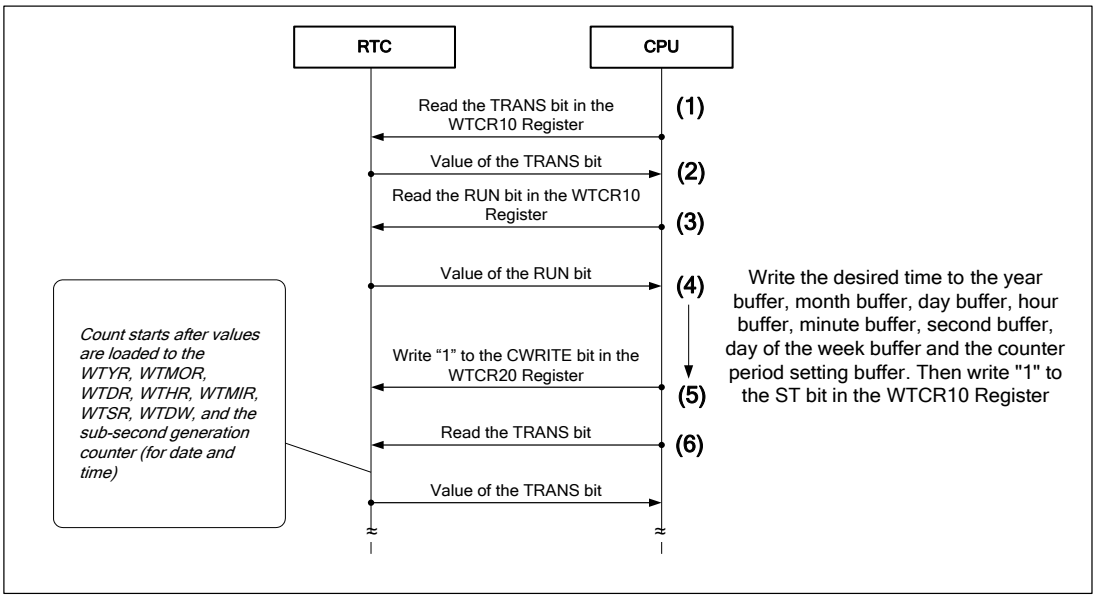
Alarm Minute Register (ALMIR), Alarm Hour Register (ALHR), Alarm Day Register (ALDR), Alarm Month Register (ALMOR), and Alarm Year Register (ALYR)

These registers store the minute, hour, day, month and year settings of the alarm respectively. If an alarm is set, a comparison circuit compares the value stored in one of the above registers with its corresponding counter value (minute counter, hour counter, day counter, month counter and year counter). If the two values are the same, an alarm interrupt is generated.

3. Operations of RTC Count Block and Setting Procedures

This section explains the operations of the RTC count block and shows examples of the setting procedures.

Figure 3-1 Initial Time Setting Procedures



(1) Read the value of the TRANS bit in the WTCR10 Register of the RTC count block.

(2) If the value of the TRANS bit is 1, wait until the value becomes 0.

(3) If the value of the RUN bit is 0, following step (4) to step (6) to complete the initial time setting is possible. If the value of the RUN bit is 1, see the Time rewrite setting procedures (with time count continued) and Time rewrite setting procedures (with time count reset).

(4) Write the desired time to the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer, day of the week buffer (WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR, and WTDW) and write 1 to the ST bit in the WTCR10 Register.

(5) Write 1 to the CWRITE bit in the WTCR20 Register of the RTC count block. (CWRITE operation)

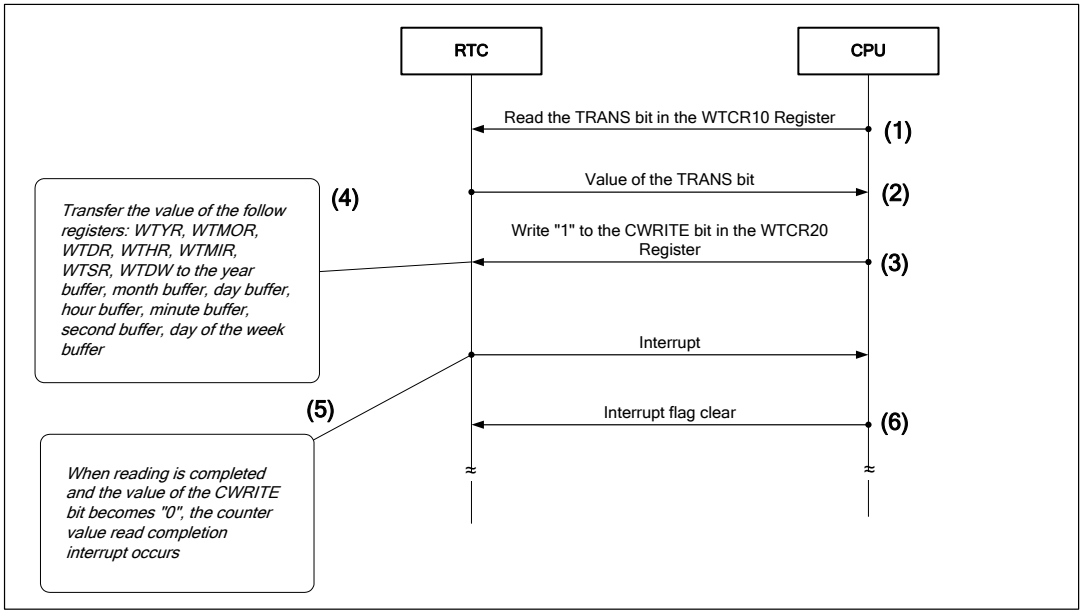
(6) If the value of the TRANS bit is 1, the CWRITE bit is operating.

If the value of the TRANS bit is 0, the operation of the CWRITE bit has completed.

Notes:

- *Access to the buffers in the RTC control block is prohibited during a recall operation or save operation.*
- *Do not reset the RTC control block or cut off power during transfer.*
  If the power is turned off during the save operation, set it again.
- *Do not perform any operation that will stop the RTCMCLK during the save operation.*

Figure 3-2 Time Read Setting Procedures



(1) Read the value of the TRANS bit in the WTCR10 Register.

(2) If the value of the TRANS bit is 1, wait until the value becomes 0.

(3) Write 1 to the CWRITE bit in the WTCR20 Register of the RTC count block. (CREAD operation)

(4) When the value of the CWRITE bit becomes 1, the value of the following registers: WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR, WTDW will be transferred to the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer, day of the week buffer (WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR, WTDW) respectively.

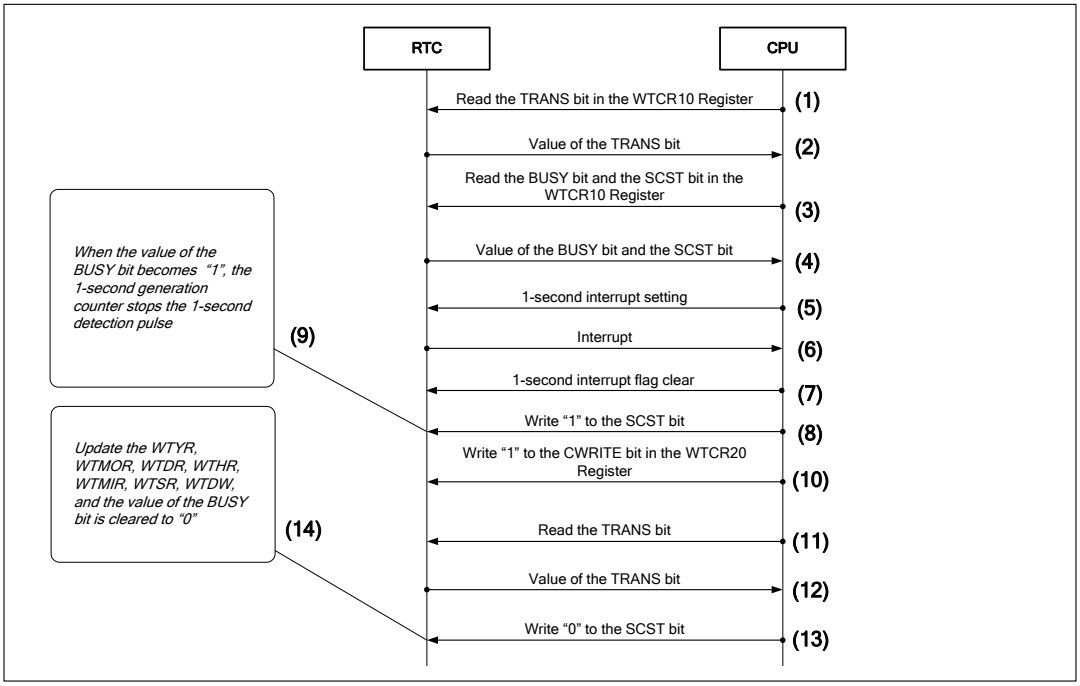
(5) When the above operation is completed, the value of the CREAD bit and that of the TRANS bit become 0, and the year/ month/ day/ hour/ minute/ second/ day of the week counter value read completion flag occurs.

(6) Clear the year/ month/ day/ hour/ minute/ second/ day of the week counter value read completion flag bit (INTCRI) in the WTCR12 Register of the RTC count block.

Notes:

- *Writing to the buffers in the RTC control block is prohibited during a recall operation or save operation.*
- *Do not reset the RTC control block or cut off power during transfer.*
- *When the value of the CREAD bit is 1, writing 1 to the SCST bit and the SRST bit in the WTCR10 Register of the RTC count block is prohibited.*
- *Do not perform any operation that will stop the RTCMCLK during the recall operation.*

Figure 3-3 Time Rewrite Setting Procedures (with Time Count Continued)



(1) Read the value of the TRANS bit in the WTCR10 Register.

(2) If the value of the TRANS bit is 1, wait until the value becomes 0.

(3) Read the value of the BUSY bit and the SCST bit in WTCR10 Register of the RTC count block.

(4) If the value of the BUSY bit is 1 and that of the SCST bit is 0, wait until the value of the BUSY bit becomes 0. In other cases, follow step (5) and onwards.

(5) Write 0 to the INTSI bit in the WTCR12 Register of the RTC count block to clear the interrupt flag bit. Write 1 to the INTSIE bit in the WTCR13 Register of the RTC count block to enable the interrupt.

(6) 1 second interrupt request will occur.

(7) Write 0 to the INTSI bit to clear the interrupt flag bit.

(8) Write 1 to the SCST bit.

(9) When 1 is written to the SCST bit, the value of the BUSY bit becomes 1. When the value of the BUSY bit becomes 1, the detection of the 1 second pulse of the 1 second generation counter stops.

(10) While the value of the BUSY bit is 1, write the desired year/ month/ day/ hour/ minute/ second/ day of the week to the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer, day of the week buffer (WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR, WTDW) respectively. Write 1 to the CWRITE bit in the WTCR20 Register of the RTC count block.

(11) Read the value of the TRANS bit.

(12) If the value of the TRANS bit is 1, wait until the value becomes 0.

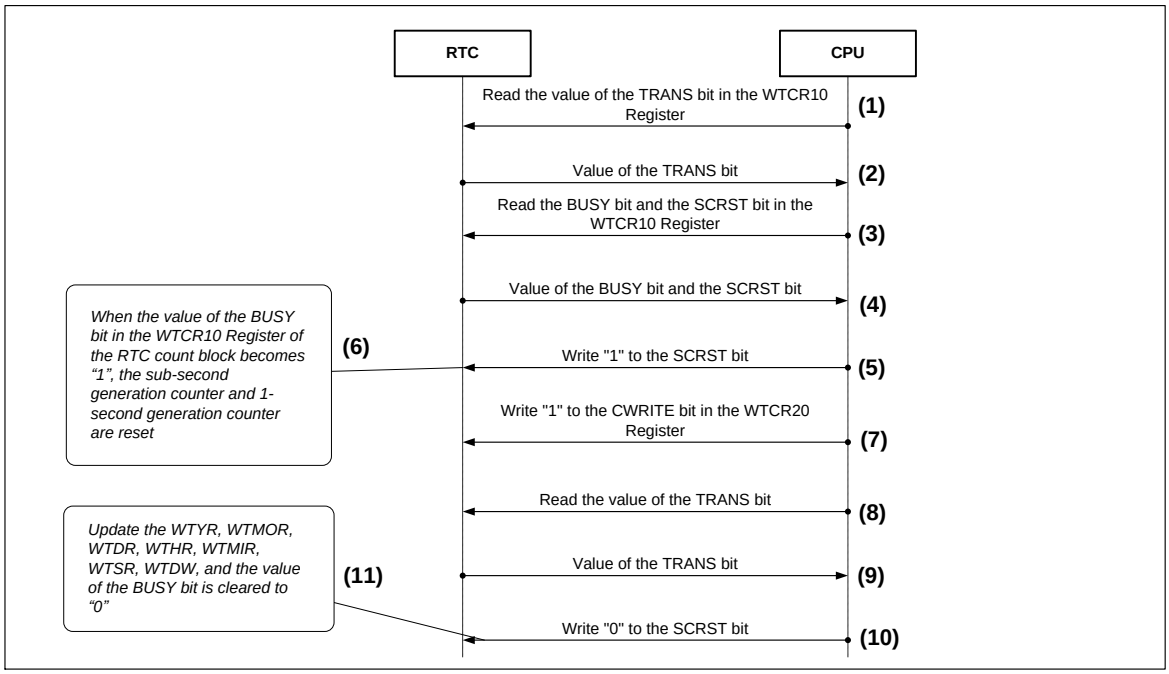
(13) Write 0 to the SCST bit.

(14) The value of the BUSY bit will be cleared to 0.

Notes:

- *Writing to the buffers in the RTC control block is prohibited during a recall operation or save operation.*
- *Do not reset the RTC control block or cut off power during transfer. If the busy bit (BUSY) of control register 10 (WTCR10) is 1 after the reset is cancelled, set it again, starting from (8). If it is not set again, there may be a time lag.*
- *To rewrite the time, recall must be performed. Rewrite the time after the latest time is read. If recall has not been performed, a time lag occurs.*
- *If the value of the BUSY bit is 1 and that of the SCST bit is 0, writing 1 to the SCST bit is prohibited.*
- *If the value of the RUN bit is 0, writing 1 to the SCST bit is prohibited.*
- *Continuous time count cannot be guaranteed if the setting in step (7) to step (13) exceeds 1 second. In that case, a time rewrite error interrupt will occur. When the value of the INTERI bit in the WTCR12 Register becomes 1, a time lag may occur. Therefore, write 0 to the SCST bit. After the time rewrite error flag is cleared, follow the above procedures from the beginning again to set the time.*
- *When the value of the SCST bit is 0 and that of the BUSY bit is 1, or that of the TRANS bit is 1, writing to the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer or day of the week buffer is prohibited because data is transferring from to the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer, and day of the week buffer to the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR, and WTDW.*
- *After setting the value of the SCST bit to 1, write 1 to the CREAD bit before updating the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR and WTDW. The value written in the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer, or day of the week buffer will be overwritten to the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR and WTDW respectively.*
- *If RTCMCLK is stopped while the value of the BUSY bit is 1, the transfer of value from the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR and WTDW to the year counter, month counter, day counter, hour counter, minute counter, second counter and day of the week counter cannot function properly. Therefore, the value of the year counter, month counter, day counter, hour counter, minute counter, second counter, and day of the week counter cannot be guaranteed.*
- *When the value of the BUSY bit is 1, writing 0 to the ST bit in the WTCR10 Register is prohibited.*

Figure 3-4 Time Rewrite Setting Procedures (Time Count Reset)



(1) Read the value of the TRANS bit in the WTCR10 Register.

(2) If the value of the TRANS bit is 1, wait until the value becomes 0.

(3) Read the value of the BUSY bit and that of the SCRST bit in WTCR10 Register.

(4) If the value of the BUSY bit is 1 and that of the SCRST is 0, wait until the value of the BUSY bit becomes 0. In other cases, follow step (5) and onwards.

(5) Write 1 to the SCRST bit.

(6) When 1 is written to the SCRST bit, the value of the BUSY bit becomes 1. The sub-second generation/1 second generation counter is reset.

(7) While the value of the SCRST bit is 1, write the desired value for the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR, WTDW to the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer or day of the week buffer (WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR, WTDW) respectively. Write 1 to the CWRITE bit in the WTCR20 Register.

(8) Read the value of the TRANS bit.

(9) If the value of the TRANS bit is 1, wait until the value becomes 0.

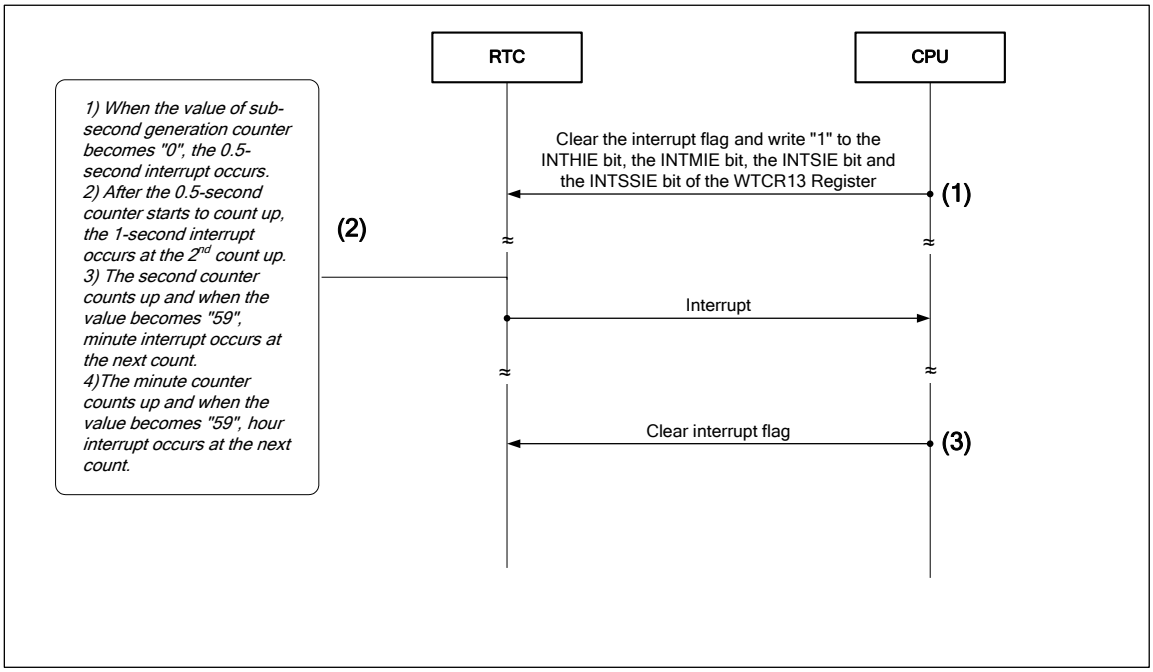
(10) Write 0 to the SCRST bit.

(11) When the value of the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer or day of the week buffer is transferred to the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR or WTDW respectively, the value of the BUSY bit is cleared to 0.

Notes:

- *Writing to the buffers in the RTC control block is prohibited during a recall operation or save operation.*
- *Do not perform a reset or turn off the power during transfer (i.e. when the transfer flag bit (TRANS) of control register 10 (WTCR10) is 1) or when the sub-second generation/1 sec generation counter reset bit (SCRST) of control register 10 (WTCR10) is 1. If the busy bit (BUSY) of control register 10 (WTCR10) is 1 after the reset is cancelled, write 0 to the sub-second generation/1 sec generation counter reset bit (SCRST) of control register 10 (WTCR10), and then set it again, starting from (5). If it is not set again, there may be a time lag.*
- *To rewrite the time, recall must be performed. Rewrite the time after the latest time is read. If recall has not been performed, a time lag occurs.*
- *If the value of the BUSY bit is 1 and that of the SCRST bit is 0, writing 1 to the SCRST bit is prohibited.*
- *If the value of the RUN bit is 0, writing 0 to the SCRST bit is prohibited.*
- *When the value of the SCRST bit is 0 and that of the BUSY bit is 1, or of the TRANS bit is 1, writing data to the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer or day of the week buffer is prohibited because data is transferring from the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer or day of the week buffer to the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR or WTDW respectively.*
- *After setting "1" to the SCRST bit, run the CREAD bit before updating the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR or WTDW. The value written in the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer or day of the week buffer will be overwritten to the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR or WTDW respectively.*
- *If RTCMCLK is stopped (transit to STOP mode or sub-oscillation stop control by WTOSCCNT) while the value of the BUSY bit is 1, the transfer of value from the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer, or day of the week buffer to the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR, or WTDW cannot function properly. Therefore, the value of the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR, or WTDW cannot be guaranteed.*
- *When the value of the BUSY bit is 1, writing 0 to the ST bit is prohibited.*

Figure 3-5 Setting Procedures of Every 0.5 second/ 1 second/ 1 minute/ 1 hour Interrupt

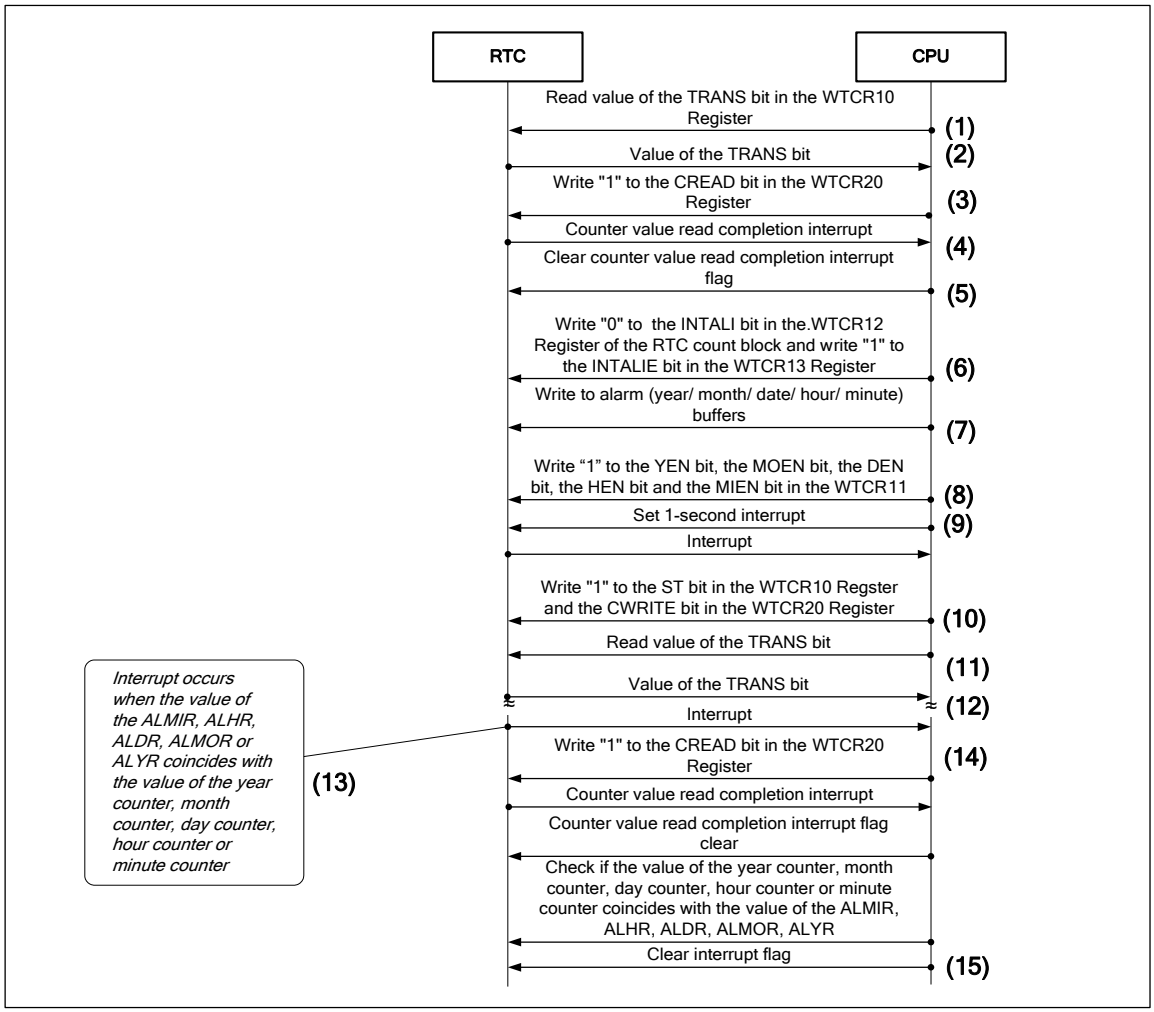


(1) Write 0 to the INTHI bit, the INTMI bit, the INTSI bit, and the INTSSI bit in the WTCR12 Register to clear the interrupt flag bit. Write 1 to the desired interrupt enable bit among the INTHIE bit, the INTMIE bit, the INTSIE bit and the INTSSIE bit of the WTCR13 Register to enable the interrupt.

(2) When either 0.5 second interrupt, 1 second interrupt, 1 minute interrupt or 1 hour interrupt occurs, an interrupt request will occur.

(3) Write 0 to the INTHIE bit, the INTMIE bit, the INTSIE bit and the INTSSIE bit to clear the interrupt flag bit.

Figure 3-6 Alarm Interrupt Setting Procedures



Read the value of the TRANS bit in the WTCR10 Register.

If the value of the TRANS bit is 1, wait until the value becomes 0.

Write 1 to the CREAD bit in the WTCR20 Register to read the counter value.

When the transfer of value to the year buffer, month buffer, day buffer, hour buffer, minute buffer, second buffer or day of the week buffer is completed, the value of the CREAD bit becomes 0 and the year/ month/ day/ hour/ minute/ second/ day of the week counter value read completion interrupt will occur.

Clear the counter value read completion interrupt flag bit.

Write 0 to the INTALI bit in the WTCR12 Register of the RTC count block to clear the alarm interrupt flag bit. Write 1 to the INTALIE bit in the WTCR13 Register to enable the alarm interrupt.

Write the desired date and time for the alarm interrupt to the alarm (year/ month/ day/ hour) buffers.

Write 1 to the YEN bit, the MOEN bit, the DEN bit, the HEN bit and the MIEN bit in the WTCR11.

After setting the 1 second interrupt, wait for it.

After the 1 second interrupt occurs, write 1 to the ST bit in the WTCR10 Register and the CWRITE bit in the WTCR20 Register to transfer the alarm value.

Read the value of the TRANS bit.

Wait until the value of the TRANS bit becomes 1.

If the value of the ALMIR, ALHR, ALDR, ALMOR, ALYR and that of the year counter, month counter, day counter, hour counter, or minute counter coincides, an interrupt request occurs.

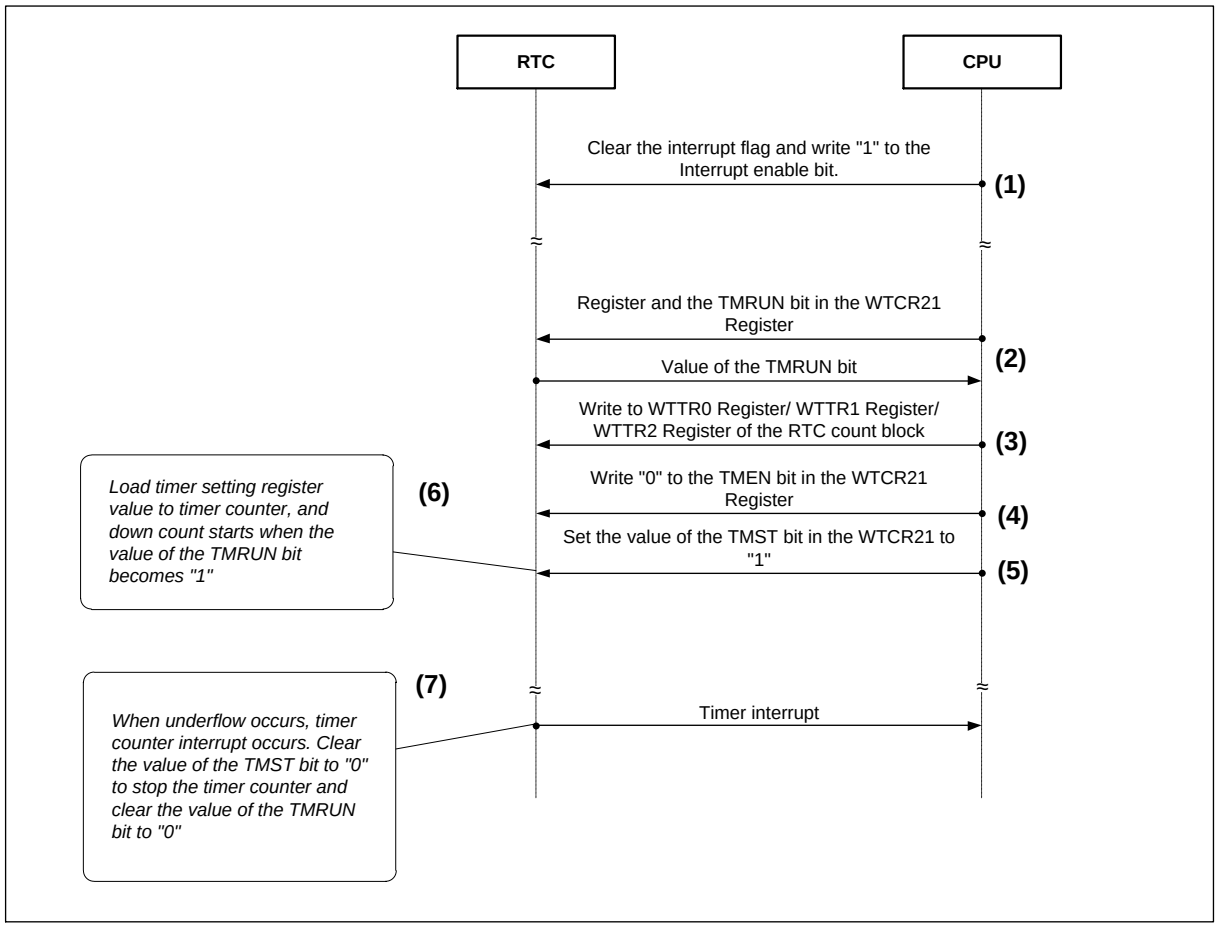
Follow the time read setting procedures to read the time and check if the value of the year counter, month counter, day counter, hour counter, or minute counter coincides with the value of the ALMIR, ALHR, ALDR, ALMOR, ALYR.

Write 0 to the INTALI bit to clear the alarm interrupt flag bit.

Notes:

- *An interrupt may occur immediately after 1 is written to any of the alarm enable bits. Recall and read the time after the interrupt and check if the value of the year counter, month counter, day counter, hour counter, or minute counter coincides with the value of the ALMIR, ALHR, ALDR, ALMOR, ALYR.*
- *Writing to the buffers in the RTC control block is prohibited during a recall operation or save operation.*
- *Do not reset the RTC control block or cut off power during transfer.*

Figure 3-7 Timer Interrupt Setting Procedures (with (Hours, Minutes, and Seconds) Elapsed)



(1) Write 0 to the INTTMI bit in the WTCR12 register of the RTC count block to clear the timer interrupt flag bit. Write 1 to the INTTMIE bit in the WTCR13 register of the RTC register to enable the timer interrupt.

(2) Check if the value of the TMRUN bit is 0 (Timer is stopped).

(3) Write timer setting to WTTR0 register / WTTR1 register / WTTR2 register.

(4) Write 0 to the TMEN bit in the WTCR21 register.

(5) Write 1 to the TMST bit in the WTCR21 register.

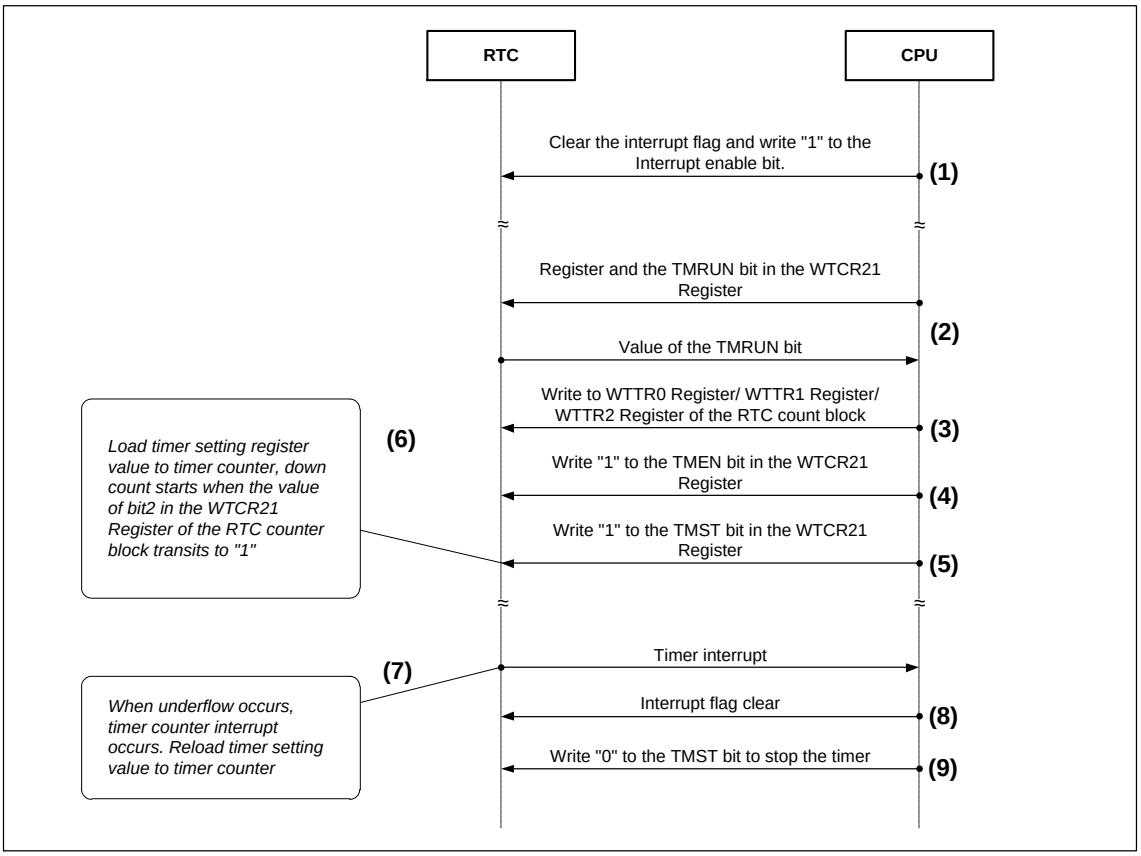
(6) The value of timer setting register transfers to the timer counter and the countdown begins.

(7) When there is underflow during count down, interrupt request occurs. The value of the TMST bit is cleared to 0 and the timer counter stops. After the timer counter has stopped, the value of the TMRUN bit becomes 0.

Notes:

- *During a timer counter operation (WTCR21:TMRUN=1), writing 1 to the TMST bit is prohibited before the TMRUN bit becomes 0 after 0 is written to the TMST bit.*
- *To change the setting of the TMEN bit, do so while the timer counter has stopped (WTCR21:TMRUN=0).*

Figure 3-8 Timer Interrupt Setting Procedures (in Intervals of (Hours, Minutes, and Seconds) Elapsed)



(1) Write 0 to the INTTMI in the WTCR12 register to clear the timer interrupt flag bit. Write 1 to the INTTMIE bit in the WTCR13 register to enable the timer interrupt.

(2) Read the TMRUN bit in the WTCR21 register to check if the value is 0 (stopped).

(3) Write timer setting to WTTR0 register / WTTR1 register / WTTR2 register of the RTC count block.

(4) Write 1 to the TMEN bit in the WTCR21 register.

(5) Write 1 to the TMST bit in the WTCR21 register.

(6) The value of timer setting register transfers to the timer counter and the countdown begins.

(7) When the count is completed, the RTC count block interrupt request will occur, and the timer setting register value will be reloaded to the timer counter and the operation will continue.

(8) Write 0 to the INTTMI bit to clear the timer interrupt flag bit.

(9) To stop the timer, write 0 to the TMST bit.

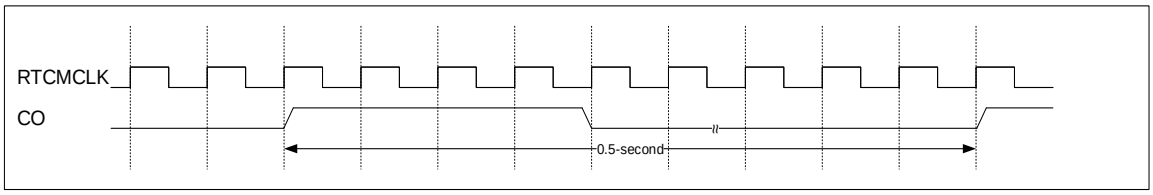
Notes:

- *During a timer counter operation (WTCR21:TMRUN=1), writing 1 to the TMST bit is prohibited before the TMRUN bit becomes 0 after 0 is written to the TMST bit.*
- *To change the setting of the TMEN bit, do so while the timer counter has stopped (WTCR21:TMRUN=0).*

Output Operation of CO External Pin

The RTC count block has CO external pin to output 0.5 second pulse.
Figure 3-9 shows the waveform of CO external pin output.

Figure 3-9 CO External Pin Output Waveform



4. RTC Control Block Reset Operation

This section explains the resetting of the RTC control block.

Low-voltage Detection Reset/ Power-on Reset Operation

The shaded parts in Table 4-1 are target bits of the low-voltage detection reset/ power-on reset.

In addition, the sub-second generation counter for timer counter and timer counter not shown in Table 4-1 are also reset targets.

The sub-second generation counter for date and time and year counter, month counter, day counter, hour counter, minute counter, second counter and day of the week counter not shown in Table 4-1 are not reset targets.

Because the INTALI and RUN bits are generated in the VBAT domain, they cannot be cleared by a reset for the Always on domain.

Table 4-1 Low-voltage Detection Reset/ Power-on Reset Target Bits

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WTCR10	TRANS	BUSY	SCRST	SCST	SRST	RUN	-	ST
WTCR11	-	-	-	YEN	MOEN	DEN	HEN	MIEN
WTCR12	INTCRI	INTERI	INTALI	INTTMI	INTHI	INTMI	INTSI	INTSSI
WTCR13	INTCRIE	INTERIE	INTALIE	INTTMIE	INTHIE	INTMIE	INTSIE	INTSSIE
WTCR20	-	-	PWRITE	PREAD	BWRITE	BREAD	CWRITE	CREAD
WTCR21	-	-	-	-	-	TMRUN	TMEN	TMST
WTSR	-	TS2	TS1	TS0	S3	S2	S1	S0
WTMIR	-	TMI2	TMI1	TMI0	MI3	MI2	MI1	MI0
WTHR	-	-	TH1	TH0	H3	H2	H1	H0
WTDR	-	-	TD1	TD0	D3	D2	D1	D0
WTDW	-	-	-	-	-	DW2	DW1	DW0
WTMOR	-	-	-	TMO0	MO3	MO2	MO1	MO0
WTYR	TY3	TY2	TY1	TY0	Y3	Y2	Y1	Y0
ALMIR	-	TAMI2	TAMI1	TAMI0	AMI3	AMI2	AMI1	AMI0
ALHR	-	-	TAH1	TAH0	AH3	AH2	AH1	AH0
ALDR	-	-	TAD1	TAD0	AD3	AD2	AD1	AD0
ALMOR	-	-	-	TAMO0	AMO3	AMO2	AMO1	AMO0
ALYR	TAY3	TAY2	TAY1	TAY0	AY3	AY2	AY1	AY0
WTTR0	TM7	TM6	TM5	TM4	TM3	TM2	TM1	TM0
WTTR1	TM15	TM14	TM13	TM12	TM11	TM10	TM9	TM8
WTTR2	-	-	-	-	-	-	TM17	TM16

System Reset Operation

The shaded parts in Table 4-2 are target bits of the system reset.

In addition, the sub-second generation counter for timer counter and timer counter not shown in Table 4-1 are also reset targets.

The sub-second generation counter (for date and time) and the year counter, month counter, day counter, hour counter, minute counter, second counter and day of the week counter are not reset targets.

Table 4-2 System Reset Target Bits

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WTCR10	TRANS	BUSY	SCRST	SCST	SRST	RUN	-	ST
WTCR11	-	-	-	YEN	MOEN	DEN	HEN	MIEN
WTCR12	INTCRI	INTERI	INTALI	INTTMI	INTHI	INTMI	INTSI	INTSSI
WTCR13	INTCRIE	INTERIE	INTALIE	INTTMIE	INTHIE	INTMIE	INTSIE	INTSSIE
WTCR20	-	-	PWRITE	PREAD	BWRITE	BREAD	CWRITE	CREAD
WTCR21	-	-	-	-	-	TMRUN	TMEN	TMST
WTSR	-	TS2	TS1	TS0	S3	S2	S1	S0
WTMIR	-	TMI2	TMI1	TMI0	MI3	MI2	MI1	MI0
WTHR	-	-	TH1	TH0	H3	H2	H1	H0
WTDR	-	-	TD1	TD0	D3	D2	D1	D0
WTDW	-	-	-	-	-	DW2	DW1	DW0
WTMOR	-	-	-	TMO0	MO3	MO2	MO1	MO0
WTYR	TY3	TY2	TY1	TY0	Y3	Y2	Y1	Y0
ALMIR	-	TAMI2	TAMI1	TAMI0	AMI3	AMI2	AMI1	AMI0
ALHR	-	-	TAH1	TAH0	AH3	AH2	AH1	AH0
ALDR	-	-	TAD1	TAD0	AD3	AD2	AD1	AD0
ALMOR	-	-	-	TAMO0	AMO3	AMO2	AMO1	AMO0
ALYR	TAY3	TAY2	TAY1	TAY0	AY3	AY2	AY1	AY0
WTTR0	TM7	TM6	TM5	TM4	TM3	TM2	TM1	TM0
WTTR1	TM15	TM14	TM13	TM12	TM11	TM10	TM9	TM8
WTTR2	-	-	-	-	-	-	TM17	TM16

RTC Reset Operation

The shaded parts in Table 4-3 are target bits of the RTC reset. The timer counter not shown in Table 4-3 are RTC reset targets as well.

The sub-second generation counter (for date and time/ for timer) and the year counter, month counter, day counter, hour counter, minute counter, second counter and day of the week counter, 1 second counter are not reset targets.

Table 4-3 RTC Reset Target Bits

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WTCR10	TRANS	BUSY	SCRST	SCST	SRST	RUN	-	ST
WTCR11	-	-	-	YEN	MOEN	DEN	HEN	MIEN
WTCR12	INTCRI	INTERI	INTALI	INTTMI	INTHI	INTMI	INTSI	INTSSI
WTCR13	INTCRIE	INTERIE	INTALIE	INTTMIE	INTHIE	INTMIE	INTSIE	INTSSIE
WTCR20	-	-	PWRITE	PREAD	BWRITE	BREAD	CWRITE	CREAD
WTCR21	-	-	-	-	-	TMRUN	TMEN	TMST
WTSR	-	TS2	TS1	TS0	S3	S2	S1	S0
WTMIR	-	TMI2	TMI1	TMI0	MI3	MI2	MI1	MI0
WTHR	-	-	TH1	TH0	H3	H2	H1	H0
WTDR	-	-	TD1	TD0	D3	D2	D1	D0
WTDW	-	-	-	-	-	DW2	DW1	DW0
WTMOR	-	-	-	TMO0	MO3	MO2	MO1	MO0
WTYR	TY3	TY2	TY1	TY0	Y3	Y2	Y1	Y0
ALMIR	-	TAMI2	TAMI1	TAMI0	AMI3	AMI2	AMI1	AMI0
ALHR	-	-	TAH1	TAH0	AH3	AH2	AH1	AH0
ALDR	-	-	TAD1	TAD0	AD3	AD2	AD1	AD0
ALMOR	-	-	-	TAMO0	AMO3	AMO2	AMO1	AMO0
ALYR	TAY3	TAY2	TAY1	TAY0	AY3	AY2	AY1	AY0
WTTR0	TM7	TM6	TM5	TM4	TM3	TM2	TM1	TM0
WTTR1	TM15	TM14	TM13	TM12	TM11	TM10	TM9	TM8
WTTR2	-	-	-	-	-	-	TM17	TM16

5. Leap Year Compliance of RTC Count Block

This section explains the leap year compliance of the RTC count block.

Leap Year Compliance

Table 5-1 shows the days of each month.

Table 5-1 List of Leap Years

Year	Leap Year	Month											
		1	2	3	4	5	6	7	8	9	10	11	12
00	○	31	29	31	30	31	30	31	31	30	31	30	31
01 to 03	×	31	28	31	30	31	30	31	31	30	31	30	31
04	○	31	29	31	30	31	30	31	31	30	31	30	31
05 to 07	×	31	28	31	30	31	30	31	31	30	31	30	31
08	○	31	29	31	30	31	30	31	31	30	31	30	31
09 to 11	×	31	28	31	30	31	30	31	31	30	31	30	31
12	○	31	29	31	30	31	30	31	31	30	31	30	31
13 to 15	×	31	28	31	30	31	30	31	31	30	31	30	31
16	○	31	29	31	30	31	30	31	31	30	31	30	31
17 to 19	×	31	28	31	30	31	30	31	31	30	31	30	31
20	○	31	29	31	30	31	30	31	31	30	31	30	31
21 to 23	×	31	28	31	30	31	30	31	31	30	31	30	31
24	○	31	29	31	30	31	30	31	31	30	31	30	31
25 to 27	×	31	28	31	30	31	30	31	31	30	31	30	31
28	○	31	29	31	30	31	30	31	31	30	31	30	31
29 to 31	×	31	28	31	30	31	30	31	31	30	31	30	31
32	○	31	29	31	30	31	30	31	31	30	31	30	31
33 to 35	×	31	28	31	30	31	30	31	31	30	31	30	31
36	○	31	29	31	30	31	30	31	31	30	31	30	31
37 to 39	×	31	28	31	30	31	30	31	31	30	31	30	31
40	○	31	29	31	30	31	30	31	31	30	31	30	31
41 to 43	×	31	28	31	30	31	30	31	31	30	31	30	31
44	○	31	29	31	30	31	30	31	31	30	31	30	31
45 to 47	×	31	28	31	30	31	30	31	31	30	31	30	31
48	○	31	29	31	30	31	30	31	31	30	31	30	31
49 to 51	×	31	28	31	30	31	30	31	31	30	31	30	31
52	○	31	29	31	30	31	30	31	31	30	31	30	31
53 to 55	×	31	28	31	30	31	30	31	31	30	31	30	31
56	○	31	29	31	30	31	30	31	31	30	31	30	31
57 to 59	×	31	28	31	30	31	30	31	31	30	31	30	31
60	○	31	29	31	30	31	30	31	31	30	31	30	31
61 to 63	×	31	28	31	30	31	30	31	31	30	31	30	31
64	○	31	29	31	30	31	30	31	31	30	31	30	31
65 to 67	×	31	28	31	30	31	30	31	31	30	31	30	31
68	○	31	29	31	30	31	30	31	31	30	31	30	31
69 to 71	×	31	28	31	30	31	30	31	31	30	31	30	31
72	○	31	29	31	30	31	30	31	31	30	31	30	31
73 to 75	×	31	28	31	30	31	30	31	31	30	31	30	31

Year	Leap Year	Month											
		1	2	3	4	5	6	7	8	9	10	11	12
76	○	31	29	31	30	31	30	31	31	30	31	30	31
77 to 79	×	31	28	31	30	31	30	31	31	30	31	30	31
80	○	31	29	31	30	31	30	31	31	30	31	30	31
81 to 83	×	31	28	31	30	31	30	31	31	30	31	30	31
84	○	31	29	31	30	31	30	31	31	30	31	30	31
85 to 87	×	31	28	31	30	31	30	31	31	30	31	30	31
88	○	31	29	31	30	31	30	31	31	30	31	30	31
89 to 91	×	31	28	31	30	31	30	31	31	30	31	30	31
92	○	31	29	31	30	31	30	31	31	30	31	30	31
93 to 95	×	31	28	31	30	31	30	31	31	30	31	30	31
96	○	31	29	31	30	31	30	31	31	30	31	30	31
97 to 99	×	31	28	31	30	31	30	31	31	30	31	30	31

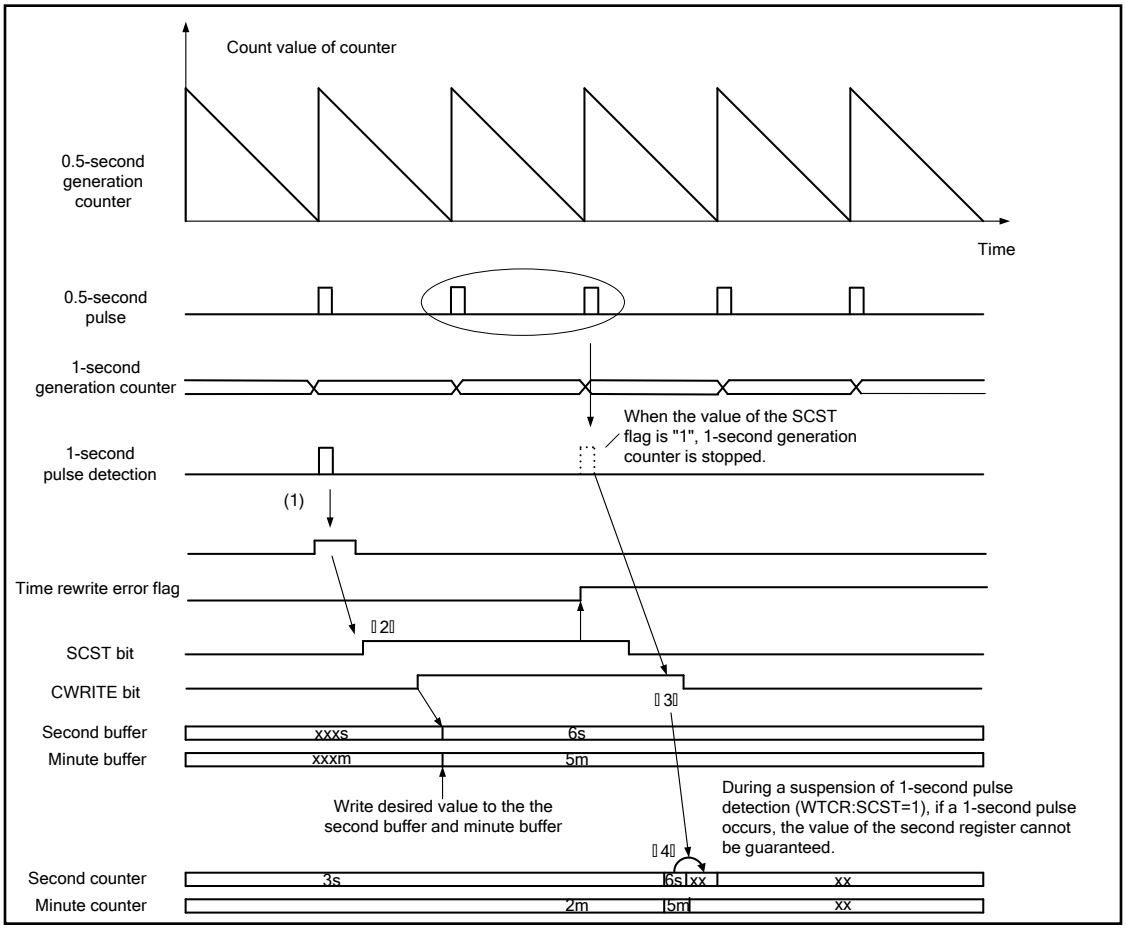
6. Time Rewrite Error

This section explains the time rewrite error during time rewrite (with time count continued).

Time Rewrite Error

Below shows the situation when 0.5 second pulse of the 0.5 second generation counter is detected twice while the value of the SCST bit remains 1 during time rewrite (time count continued).

■ When only the second counter and minute counter are rewritten.



(1) After the 1 second interrupt is detected, clear the 1 second interrupt flag. Write 1 to the SCST bit and write the counter value.

(2) Set the value of the CWRITE bit to 1 and write the counter value.

(3) When 0.5 second pulse is detected for twice while the value of the SCST flag remains as 1, the value of time rewrite error flag becomes 1.

(4) The value of the second counter, minute counter, hour counter, week counter, month counter and year counter cannot be guaranteed.

Notes:

- *If 0.5 second pulse is detected less than once while the value of the SCST bit remains as 1, the value of time rewrite error flag will not become 1.*
- *When 0.5 second pulse is detected twice while the value of the SCST bit remains as 1, the value of second counter cannot be guaranteed. Therefore, revise the time rewrite value again.*
- *Rewrite the time in 1 second after the 1 second interrupt is detected.*

7. Registers in RTC Control Block

This section shows the list of registers in the RTC control block.

Table 7-1 List of Registers in RTC Control Block

Abbreviation	Register Name	Interface Circuit Type	Reference
WTCR10	Control Register 10	Bit0 ST:2, Bit2 RUN:4	7.1
WTCR11	Control Register 11	2	7.2
WTCR12	Control Register 12	-	7.3
WTCR13	Control Register 13	-	7.4
WTCR20	Control Register 20	1	7.5
WTCR21	Control Register 21	2	7.6
WTSR	Second Register	2	7.7
WTMIR	Minute Register	2	7.8
WTHR	Hour Register	2	7.9
WTDR	Day Register	2	7.10
WTDW	Day Of the Week Register	2	7.11
WTMOR	Month Register	2	7.12
WTYR	Year Register	2	7.13
ALMIR	Alarm Minute Register	2	7.14
ALHR	Alarm Hour Register	2	7.15
ALDR	Alarm Day Register	2	7.16
ALMOR	Alarm Month Register	2	7.17
ALYR	Alarm Year Register	2	7.18
WTTR0	Timer Setting Register 0	-	7.19
WTTR1	Timer Setting Register 1	-	7.20
WTTR2	Timer Setting Register 2	-	7.21

The registers shown in Table 7-1 correspond to Circuit Type 1 or 2 or 4 in the chapter VBAT Domain. For the Circuit Type 2, a system reset and RTC reset do not initialize the registers in the VBAT domain. They do, however, initialize the buffers in the Always ON domain. After a reset, therefore, the save operation must be performed after the value is set again or the recall operation is performed. The registers shown circuit type as “-“ don’t influence the VBAT domain.

For the details of interface circuit type, refer to Interfacing with Always-on Domain in Chapter 7: VBAT Domain in FM4 Family Peripheral Manual.

Note:

- *After 1 is written to the CWRITE bit, the value of the TRANS bit becomes 0 and the RTC control block buffer value is reflected in the registers in the RTC count block (VBAT Domain).*
  Writing to the buffers in the RTC control block is prohibited while the value of the TRANS bit is 1.

7.1 Control Register 10 (WTCR 10)

This register controls the operations of the RTC control block.

bit	7	6	5	4	3	2	1	0
Field	TRANS	BUSY	SCRST	SCST	SRST	RUN	Reserved	ST
Attribute	R	R	R/W	R/W	W	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7] TRANS: Transfer flag bit

The TRANS bit indicates if the value is transferring.

When the value of this bit is 1, writing to RTC count block registers is prohibited.

bit	Description
0	Indicates that transfer of value has completed.
1	Indicates that value is transferring.

[bit6] BUSY: Busy bit

The BUSY bit indicates whether time rewrite is operating.

bit	Description
0	Indicates that time rewrite is not operating.
1	Indicates that any of the following conditions is happening: − When 1 is written to the SCST bit in WTCR10 Register − When 1 is written to the SCRST bit in the WTCR Register − The value of the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR and WTDW are transferring to the year counter, month counter, day counter, hour counter, minute counter, second counter and day of the week counter respectively

[bit5] SCRST: Sub-second generation/ 1 second generation counter reset bit

The SCRST bit controls the reset of the sub-second generation/ 1 second generation counter (for date and time)

bit	Description
0	Cancel the sub-second generation/ 1 second generation counter (for date and time) reset.
1	Reset the sub-second generation/ 1 second generation counter (for date and time).

If the value of this bit and that of the SCST bit are both set to 0 during the RTC operation (RUN=1), the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR, and WTDW cannot be updated. Setting the value of SCST bit and that of the SCRST bit to 1 simultaneously is prohibited. When RTC operation has stopped (RUN=0), setting the value of this bit to 1 is prohibited.

[bit4] SCST: 1 second pulse detection stop bit

The SCST bit controls the detection of 1 second pulse of 1 second generation counter.

bit	Description
0	Enable detection of 1 second pulse.
1	Stop Detection of 1 second pulse.

If this bit and SCRST bit are both set to 0 during the RTC operation (RUN=1), the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR and WTDW cannot be updated. Setting the value of SCST bit and SCRST bit to 1 simultaneously is prohibited. When RTC is stopped (RUN=0), setting the value of this bit to 1 is prohibited.

[bit3] SRST: RTC reset bit

The SRST bit is the RTC reset bit.

See Table 4-3 in chapter RTC Control Block Reset Operation for the registers or bits that are initiated by RTC reset.

This bit always reads 0.

bit	Description
read	Always read as 0
0 is written	No effect on operation.
1 is written	When 1 is written, the hardware issues the RTC reset.

[bit2] RUN: RTC count block operation bit

The RUN bit indicates the operation state of the RTC count block.

During RTC count block operation (WTCR10:ST=1), set the ST bit to 0 will stop the RTC count block operation and the value of the RUN bit will become0.

bit	Description
0	RTC count block is stopped.
1	RTC count block is operating.

[bit1] Reserved: Reserved bit

Always read as 0.

Set the value of this bit to 0 when writing.

[bit0] ST: Start bit

The ST bit controls the startup of the RTC count block.

1 cannot be written when the sub-oscillation is stopped.

bit	Description
0	Stops the RTC count block.
1	Transfers the setting of the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR and WTDW to the year counter, month counter, day counter, hour counter, minute counter, second counter and day of the week counter respectively, and the RTC count block operation starts.

7.2 Control Register 11 (WTCR 11)

This register controls the interrupt enable of the RTC control block.

bit	7	6	5	4	3	2	1	0
Field	Reserved			YEN	MOEN	DEN	HEN	MIEN
Attribute	R			R/W	R/W	R/W	R/W	R/W
Initial value	000			0	0	0	0	0

[bit7:5] Reserved: Reserved bits

Always read as 0.
Set the value of this bit to 0 when writing.

[bit4] YEN: Alarm year register enable bit

The YEN bit enables the comparison between the ALYR and the year counter. When the value of this bit is set to 1, this bit becomes the detection target of the alarm coincidence flag (INTALI).

bit	Description
0	Prohibit comparison of the ALYR and the year counter.
1	Enable the comparison between the ALYR and the year counter.

[bit3] MOEN: Alarm month register enable bit

The MOEN bit enables the comparison between the ALMOR and the month counter. When the value of this bit is set to 1, this bit becomes the detection target of the alarm coincidence flag (INTALI).

bit	Description
0	Prohibit comparison between the ALMOR and the month counter.
1	Enable the comparison between the ALMOR and the month counter.

[bit2] DEN: Alarm day register enable bit

The DEN bit enables the comparison between the ALDR and the day counter. When the value of this bit is set to 1, this bit becomes the detection target of the alarm coincidence flag (INTALI).

bit	Description
0	Prohibit comparison between the ALDR and the day counter.
1	Enable comparison between the ALDR and the day counter.

[bit1] HEN: Alarm hour register enable bit

The HEN bit enables the comparison between the ALHR and the hour counter. When the value of this bit is set to 1, this bit becomes the detection target of the alarm coincidence flag (INTALI).

bit	Description
0	Prohibit comparison between the ALHR and the hour counter.
1	Enable comparison between the ALHR and the hour counter.

[bit0] MIEN: Alarm minute register enable bit

The MIEN bit enables the comparison between the ALMIR and the minute counter. When the value of this bit is set to 1, this bit becomes the detection target of the alarm coincidence flag (INTALI).

bit	Description
0	Prohibit comparison between the ALMIR and the minute counter.
1	Enable comparison between the ALMIR and the minute counter.

7.3 Control Register 12 (WTCR 12)

This is the RTC control block interrupt flag register.

bit	7	6	5	4	3	2	1	0
Field	INTCRI	INTERI	INTALI	INTTMI	INTHI	INTMI	INTSI	INTSSI
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7] INTCRI: Year/ month / day / hour / minute / second / day of the week counter value read completion flag bit

According to the CREAD bit, the INTCRI bit indicates the transfer state of the value of the year counter, month counter, day counter, hour counter, minute counter, second counter, and the day of the week counter to the WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR and WTDW when the date and time is read.

During read access of read modify right access, 1 is always read.

bit	Description
When 0 is read	Reading of the value of the year counter, month counter, day counter, hour counter, minute counter, second counter and the day of the week counter has not completed.
When 1 is read	Reading of the value of the year counter, month counter, day counter, hour counter, minute counter, second counter and the day of the week counter has completed.
When 0 is written	Clear this flag.
When 1 is written	No effect on operation.

[bit6] INTERI: Time rewrite error flag bit

During time rewrite (SCST=1), the INTERI indicates that the second counter does not count up.

During read access of read modify right access, 1 is always read.

bit	Description
When 0 is read	Time rewrite error is not occurring.
When 1 is read	Time rewrite error has occurred.
When 0 is written	Clear this flag.
When 1 is written	No effect on operation.

[bit5] INTALI: Alarm coincidence flag bit

The INTALI bit indicates if the value of the ALYR, ALMOR, ALDR, ALHR or ALMIR coincides with the value of the year counter, month counter, day counter, hour counter or minute counter.

During read access of read modify right access, 1 is always read.

bit	Description
When 0 is read	Alarm coincidence is not occurring.
When 1 is read	Alarm coincidence has occurred.
When 0 is written	This flag is cleared.
When 1 is written	No effect on operation.

[bit4] INTTMI: Timer underflow detection flag bit

When timer counter underflows, the value of the INTTMI bit becomes 1.
During read access of read modify right access, 1 is always read.

bit	Description
When 0 is read	Timer underflow is not occurring.
When 1 is read	Timer underflow has occurred.
When 0 is written	This flag is cleared.
When 1 is written	No effect on operation.

[bit3] INTHI: Every hour flag bit

When hour counter counts up, the value of the INTHI bit becomes 1.
During read access of read modify right access, 1 is always read.

bit	Description
When 0 is read	Hour counter count up is not occurring.
When 1 is read	Hour counter count up has occurred.
When 0 is written	Clear this flag.
When 1 is written	No effect on operation.

[bit2] INTMI: Every minute flag bit

When minute counter counts up, the value of the INTMI bit becomes 1.
During read access of read modify right access, 1 is always read.

bit	Description
When 0 is read	Minute counter count up is not occurring.
When 1 is read	Minute counter count up has occurred.
When 0 is written	Clear this flag.
When 1 is written	No effect on operation.

[bit1] INTSI: Every second flag bit

When second counter counts up, the value of the INTSI bit becomes 1.
During read access of read modify right access, 1 is always read.

bit	Description
When 0 is read	Second counter count up is not occurring.
When 1 is read	Second counter count up has occurred.
When 0 is written	Clear this flag.
When 1 is written	No effect on operation.

[bit0] INTSSI: Every 0.5 second flag bit

When 0.5 second pulse occurs, the value of the INTSSI bit becomes 1.
During read access of read modify right access, 1 is always read.

Bit	Description
When 0 is read	0.5 second pulse is not occurring.
When 1 is read	0.5 second pulse has occurred.
When 0 is written	Clear this flag.
When 1 is written	No effect on operation.

7.4 Control Register 13 (WTCR 13)

This is the RTC control block interrupt enable register.

bit	7	6	5	4	3	2	1	0
Field	INTCRIE	INTERIE	INTALIE	INTTMIE	INTHIE	INTMIE	INTSIE	INTSSIE
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7] INTCRIE: Year / month / day / hour / minute / second / day of the week counter value read completion interrupt enable bit

The INTCRIE bit enables the year / month / day / hour / minute / second / day of the week counter value read completion interrupt.

bit	Description
0	Interrupt prohibited.
1	Interrupt enabled.

[bit6] INTERIE: Time rewrite error interrupt enable bit

The INTERIE bit enables the time rewrite error interrupt.

bit	Description
0	Interrupt prohibited.
1	Interrupt enabled.

[bit5] INTALIE: Alarm coincidence interrupt enable bit

The INTALIE bit enables the alarm coincidence interrupt.

bit	Description
0	Interrupt prohibited.
1	Interrupt enabled.

[bit4] INTTMIE: Timer underflow interrupt enable bit

The INTTMIE bit enables the timer underflow interrupt.

bit	Description
0	Interrupt prohibited.
1	Interrupt enabled.

[bit3] INTHIE: Every hour interrupt enable bit

The INTHIE bit enables the every hour interrupt.

bit	Description
0	Interrupt prohibited.
1	Interrupt enabled.

[bit2] INTMIE: Every minute interrupt enable bit

The INTMIE bit enables the every minute interrupt.

bit	Description
0	Interrupt prohibited.
1	Interrupt enabled.

[bit1] INTSIE: Every second interrupt enable bit

The INTSIE bit enables the every second interrupt.

bit	Description
0	Interrupt prohibited.
1	Interrupt enabled.

[bit0] INTSSIE: Every 0.5 second interrupt enable bit

The INTSSIE bit enables the every 0.5 second interrupt.

bit	Description
0	Interrupt prohibited.
1	Interrupt enabled.

7.5 Control Register 20 (WTCR 20)

This register controls the save operation and recall operation.

bit	7	6	5	4	3	2	1	0
Field	Reserved		PWRITE	PREAD	BWRITE	BREAD	CWRITE	CREAD
Attribute	R		W	W	W	W	W	W
Initial value	00		0	0	0	0	0	0

[bit7:6] Reserved: Reserved bits

Always read as 0.

Set the value of this bit to 0 when writing.

[bit5] PWRITE: VBAT PORT save control bit

When the value of the PWRITE bit is set to 1, the buffer value set in the Always ON Domain will start saving to the VBAT Domain.

bit	Description
read	Always read as 0
0 is written	No effect on operation.
1 is written	Start to save buffer value from the Always ON Domain to the VBAT Domain.

[bit4] PREAD: VBAT PORT recall control bit

When the value of the PREAD bit is set to 1, the buffer value set in the VBAT Domain will start recalling to the Always ON Domain.

bit	Description
read	Always read as 0
0 is written	No effect on operation.
1 is written	Start to recall register value from the VBAT Domain to the Always ON Domain.

[bit3] BWRITE: Back up register save control bit

When the value of the PWRITE bit is set to 1, the buffer value set in the Always ON Domain will start saving to the VBAT Domain.

bit	Description
read	Always read as 0
0 is written	No effect on operation.
1 is written	Start to save buffer value from the Always ON Domain to the VBAT Domain.

[bit2] BREAD: Back up register recall control bit

When the value of the BREAD bit is set to 1, the register value set in the VBAT Domain will start recalling to the Always ON Domain.

bit	Description
read	Always read as 0
0 is written	No effect on operation.
1 is written	Start to recall register value from the VBAT Domain to the Always ON Domain.

[bit1] CWRITE: RTC setting save control bit

When the value of the PWRITE bit is set to 1, the buffer value set in the Always ON Domain will start saving to the VBAT Domain. 1 cannot be written when the sub-oscillation is stopped.

bit	Description
read	Always read as 0
0 is written	No effect on operation.
1 is written	Start to save buffer from the Always ON Domain to the VBAT Domain.

[bit0] CREAD: RTC setting recall control bit

When the value of the BREAD bit is set to 1, the register value set in the VBAT Domain will start recalling to the Always ON Domain. 1 cannot be written when the sub-oscillation is stopped.

bit	Description
read	Always read as 0
0 is written	No effect on operation.
1 is written	Start to recall register value from the Always ON Domain to the VBAT Domain.

Note:

- *There are restrictions on combination of simultaneous transfer. See Circuit connected to interface circuit in the VBAT Domain chapter in the Peripheral Manual for restrictions on combinations of simultaneous transfer details and transfer target registers.*

7.6 Control Register 21 (WTCR 21)

This register control timer operation of the RTC count block.

bit	7	6	5	4	3	2	1	0
Field	Reserved					TMRUN	TMEN	TMST
Attribute	R					R	R/W	R/W
Initial value	00000					0	0	0

[bit7:3] Reserved: Reserved bits

Always read as 0.

Set the value of this bit to 0 when writing.

[bit2] TMRUN: Timer counter operation bit

The TMRUN bit indicates the operation of timer counter.

If the timer counter control bit (TMEN) is 0, the timer counter counts up and this bit will be cleared by the hardware. If the value of the TMEN bit is 1, the remain the value of the TMRUN bit remains 1 until 0 is written to the TMST bit.

During a timer operation (TMST=1), setting 0 to the TMST bit will stop the timer operation and the value of this bit will become 0.

bit	Description
0	Timer counter is stopped.
1	Timer counter is operating.

[bit1] TMEN: Time counter control bit

The TMEN bit controls whether the time counter operates after a specific time (hour, minute, second) or at a specific interval (hour, minute, second).

1 cannot be written when the sub-oscillation is stopped.

bit	Description
0	Time counter operates after a specific time (hour, minute, second)
1	Time counter operates at a specific interval (hour, minute, second)

[bit0] TMST: Time counter start bit

The TMST bit starts the time counter.

If the value of the TMEN bit is 0, the value of the TMST bit will be cleared to 0 by the hardware after the count has completed.

See the time counter operation bit (TMRUN) for the time counter operation state. To rewrite the time setting register, do so after stopping this bit by writing 0 to it. Then rewrite the time setting register and write 1 to this bit to resume the operation.

1 cannot be written when the sub-oscillation is stopped.

bit	Description
0	Timer counter is stopped.
1	Timer counter starts operating.

7.7 Second Register (WTSR)

This register indicates the second information in the RTC count block. The register value is shown in Binary-Coded Decimal.

bit	7	6	5	4	3	2	1	0
Field	Reserved	TS2	TS1	TS0	S3	S2	S1	S0
Attribute	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7] Reserved: Reserved bit

Always read as 0.

Set the value of this bit to 0 when writing.

[bit6:4] TS2-TS0: Second register

The TS2 to TS0 bits show the 2nd digit of the second information in the RTC count block.

0 to 5: Valid

6, 7: Setting is prohibited

[bit3:0] S3-S0: Second register

The S3 to S0 bits show the 1st digit of the second information in the RTC count block.

0 to 9: Valid

A to F: Setting is prohibited

7.8 Minute Register (WRMIR)

This register indicates the minute information in the RTC count block. The register value is shown in BCD.

bit	7	6	5	4	3	2	1	0
Field	Reserved	TMI2	TMI1	TMI0	MI3	MI2	MI1	MI0
Attribute	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7] Reserved: Reserved bit

Always read as 0.

Set the value of this bit to 0 when writing.

[bit6:4] TMI2-TMI0: Minute register

The TMI2 to TMI0 bits show the 2nd digit of the minute information in the RTC count block.

0 to 5: Valid

6, 7: Setting is prohibited

[bit3:0] MI3-MI0: Minute register

The MI3 to MI0 bits show the 1st digit of the minute information in the RTC count block.

0 to 9: Valid

A to F: Setting is prohibited

7.9 Hour Register (WTHR)

This register indicates the hour information in the RTC count block. The register value is shown in BCD.

bit	7	6	5	4	3	2	1	0
Field	Reserved		TH1	TH0	H3	H2	H1	H0
Attribute	R		R/W	R/W	R/W	R/W	R/W	R/W
Initial value	00		0	0	0	0	0	0

[bit7:6] Reserved: Reserved bits

Always read as 0.

Set the value of this bit to 0 when writing.

[bit5:4] TH1, TH0: Hour register

The TH1 bit and TH0 bit show the 2nd digit of the hour information in the RTC count block.

0 to 2: Valid

3: Setting is prohibited

[bit3:0] H3-H0: Hour register

The H3 to H0 bits show the 1st digit of the hour information in the RTC count block.

0 to 9: Valid

A to F: Setting is prohibited

7.10 Day Register (WTDR)

This register indicates the day information in the RTC count block. The register value is shown in BCD.

bit	7	6	5	4	3	2	1	0
Field	Reserved		TD1	TD0	D3	D2	D1	D0
Attribute	R		R/W	R/W	R/W	R/W	R/W	R/W
Initial value	00		0	0	0	0	0	0

[bit7:6] Reserved: Reserved bits

Always read as 0.

Set the value of this bit to 0 when writing.

[bit5:4] TD1, TD0: Day register

The TD1 bit and TD0 bit show the 2nd digit of the day information in the RTC count block.

[bit3:0] D3-D0: Day register

The D3 to D0 bits show the 1st digit of the day information in the RTC count block.

0 to 9: Valid

A to F: Setting is prohibited

7.11 Day of the Week Register (WTDW)

This register indicates the day of the week information in the RTC count block. The register value is shown in BCD.

bit	7	6	5	4	3	2	1	0
Field	Reserved					DW2	DW1	DW0
Attribute	R					R/W	R/W	R/W
Initial value	00000					0	0	0

[bit7:3] Reserved: Reserved bits

Always read as 0.

Set the value of this bit to 0 when writing.

[bit2:0] DW2-DW0: Day of the week register

The DW2 to DW0 bits show the day of the week information in the RTC count block.

0: Sun
1: Mon
2: Tues
3: Wed
4: Thurs
5: Fri
6: Sat
7: Setting is prohibited.

7.12 Month Register (WTMOR)

This register indicates the month information in the RTC count block. The register value is shown in BCD.

bit	7	6	5	4	3	2	1	0
Field	Reserved			TMO0	MO3	MO2	MO1	MO0
Attribute	R			R/W	R/W	R/W	R/W	R/W
Initial value	000			0	0	0	0	0

[bit7:5] Reserved: Reserved bits

Always read as 0.

Set the value of this bit to 0 when writing.

[bit4] TMO0: Month register

The TMO0 bit shows the 2nd digit of the month information in the RTC count block.

[bit3:0] MO3-MO0: Month register

The MO3 to MO0 bits show the 1st digit of the month information in the RTC count block.

0 to 9: Valid

A to F: Setting is prohibited

7.13 Year Register (WTYR)

This register indicates the year information in the RTC count block. The register value is shown in BCD.

bit	7	6	5	4	3	2	1	0
Field	TY3	TY2	TY1	TY0	Y3	Y2	Y1	Y0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7:4] TY3-TY0: Year register

The TY3 to TY0 bits show the 2nd digit of the year information in the RTC count block.

0 to 9: Valid
A to F: Setting is prohibited

[bit3:0] Y3-Y0: Year register

The Y3 to Y0 bits show the 1st digit of the year information in the RTC count block.

0 to 9: Valid
A to F: Setting is prohibited

7.14 Alarm Minute Register (ALMIR)

This register indicates the minute information in alarm setting.

bit	7	6	5	4	3	2	1	0
Field	Reserved	TAMI2	TAMI1	TAMI0	AMI3	AMI2	AMI1	AMI0
Attribute	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7] Reserved: Reserved bit

Always read as 0.

Set the value of this bit to 0 when writing.

[bit6:4] TAMI2-TAMI0: Alarm minute register

The TAMI2 to TAMI0 bits show the 2nd digit of the minute information in the alarm setting.

0 to 5: Valid
6, 7: Setting is prohibited

[bit3:0] AMI3-AMI0: Alarm minute register

The AMI3 to AMI0 bits show the 1st digit of the minute information in the alarm setting.

0 to 9: Valid
A to F: Setting is prohibited

7.15 Alarm Hour Register (ALHR)

This register indicates the hour information in alarm setting.

bit	7	6	5	4	3	2	1	0
Field	Reserved		TAH1	TAH0	AH3	AH2	AH1	AH0
Attribute	R		R/W	R/W	R/W	R/W	R/W	R/W
Initial value	00		0	0	0	0	0	0

[bit7:6] Reserved: Reserved bits

Always read as 0.

Set the value of this bit to 0 when writing.

[bit5:4] TAH1, TAH0: Alarm hour register

The TAH1 bit and TAH0 bit show the 2nd digit of the hour information in the alarm setting.

0 to 2: Valid

3: Setting is prohibited

[bit3:0] AH3-AH0: Alarm hour register

The AH3 to AH0 bits show the 1st digit of the hour information in the alarm setting.

0 to 9: Valid

A to F: Setting is prohibited

7.16 Alarm Day Register (ALDR)

This register indicates the day information in alarm setting.

bit	7	6	5	4	3	2	1	0
Field	Reserved		TAD1	TAD0	AD3	AD2	AD1	AD0
Attribute	R		R/W	R/W	R/W	R/W	R/W	R/W
Initial value	00		0	0	0	0	0	0

[bit7:6] Reserved: Reserved bits

Always read as 0.

Set the value of this bit to 0 when writing.

[bit5:4] TAD1, TAD0: Alarm day register

The TAD1 bit and TAD0 bit show the 2nd digit of the day information in the alarm setting.

[bit3:0] AD3-AD0: Alarm day register

The AD3 to AD0 bits show the 1st digit of the day information in the alarm setting.

0 to 9: Valid

A to F: Setting is prohibited

7.17 Alarm Month Register (ALMOR)

This register indicates the month information in alarm setting.

bit	7	6	5	4	3	2	1	0
Field	Reserved			TAMO0	AMO3	AMO2	AMO1	AMO0
Attribute	R			R/W	R/W	R/W	R/W	R/W
Initial value	000			0	0	0	0	0

[bit7:5] Reserved: Reserved bits

Always read as 0.

Set the value of this bit to 0 when writing.

[bit4] TAMO0: Alarm month register

The TAMO0 bit shows the 2nd digit of the month information in the alarm setting.

[bit3:0] AMO3-AMO0: Alarm month register

The AMO3 to AMO0 bits show the 1st digit of the month information in the alarm setting.

0 to 9: Valid

A to F: Setting is prohibited

7.18 Alarm Year Register (ALYR)

This register indicates the year information in alarm setting.

bit	7	6	5	4	3	2	1	0
Field	TAY3	TAY2	TAY1	TAY0	AY3	AY2	AY1	AY0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7:4] TAY3-TAY0: Alarm year register

The TAY3 to TAY0 bits show the 2nd digit of the year information in the alarm setting.

0 to 9: Valid
A to F: Setting is prohibited

[bit3:0] AY3-AY0: Alarm year register

The AY3 to AY0 bits show the 1st digit of the year information in the alarm setting.

0 to 9: Valid
A to F: Setting is prohibited

7.19 Time Setting Register 0 (WTTR0)

This register sets a future time (in hours, minutes, and seconds) or an interval (in hours, minutes, and seconds) for the timer.
The value can be set from 1 second up to 1 day.

bit	7	6	5	4	3	2	1	0
Field	TM7	TM6	TM5	TM4	TM3	TM2	TM1	TM0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7:0] TM7-TM0: Timer setting register

The TM7 to TM0 bits are timer setting information bits.

WTTR0 sets the 7 bit to 0 bit of time setting register. Use the WTTR0 register / WTTR1 register / WTTR2 register to set the timer.

Set the timer to a future time (in hours, minutes and seconds) or to an interval (in hours, minutes and seconds) within a day.

It is possible to set the time from 1 second up to 1 day at 0.5 second interval.

Check the setting to timer setting registers by the following formula.

TM [17:0] = (Time set[s] × 2) -1

1 to 172799 : Valid
0, 172800 to 262143: Setting is prohibited

7.20 Time Setting Register 1 (WTTR1)

This register sets a future time (in hours, minutes and seconds) or an interval (in hours, minutes and seconds) for the timer.
The value can be set from 1 second up to 1 day.

bit	7	6	5	4	3	2	1	0
Field	TM15	TM14	TM13	TM12	TM11	TM10	TM9	TM8
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7:0] TM15-TM8: Timer setting register

These are the timer setting information bits.

WTTR1 sets the 15 bit to 8 bit of the time setting register. Use the WTTR0 register / WTTR1 register / WTTR2 register to set the timer.

See 7.19 Time Setting Register 0 (WTTR0) for the settings of the time setting register.

7.21 Time Setting Register 2 (WTTR2)

This register sets a future time (in hours, minutes, and seconds) or an interval (in hours, minutes and seconds) for the timer. The value can be set from 1 second up to 1 day.

bit	7	6	5	4	3	2	1	0
Field	Reserved						TM17	TM16
Attribute	R						R/W	R/W
Initial value	000000						0	0

[bit1:0] TM17-TM16: Timer setting register

These are the timer setting information bit.

WTTR1 sets the 17bit, 16bit of time setting register. Use the WTTR0 Register/ WTTR1 Register/ WTTR2 Register to set the timer.

See 7.19 Time Setting Register 0 (WTTR0) for the settings for the time setting register.

8. Usage Precautions

Note the following when using the RTC count block.

- During time rewrite, always perform CWRITE after performing CREAD operation.
- To change the setting of the alarm registers, do so when the value of the alarm interrupt data control bits (WTCR11: YEN, WTCR11: MOEN, WTCR11: DEN, WTCR11: HEN, WTCR11: MIEN) are 0.
- If the value of any of the alarm interrupt data control bits (WTCR11: YEN, WTCR11: MOEN, WTCR11:DEN, WTCR11:HEN, WTCR11:MIEN) is set to 1, interrupt occurs immediately. Therefore, read and check the value of date and time after the interrupt.
- When the value of the TRANS bit is 1, writing to the RTC control block registers is prohibited.
- Do not stop the RTCMCLK during transfer.
- Complete transfer of time continue rewrite in 1 second after 1 second interrupt.
- When the Always ON Domain is reset with SCST asserted (WTCR10:SCST=1), time lag may occur. Therefore, rewrite the time with the SCST bit again. After reset is canceled, if the value of the BUSY bit remains as 1, there is a need to reset.
- To use the RTC count block, use it after writing 0 to the Power-on bit (VDET:PON). (See 6.7 VDET Register in chapter VBAT Domain in the Peripheral Manual.)

CHAPTER 4-4: RTC Count Block(C)

This chapter explains the functions and operations of the RTC count block(C).

1. Overview of RTC Count Block
2. Block Diagram of RTC Count Block
3. Operations of RTC Count Block and Setting Procedures
4. RTC Count Block Reset Operation
5. Leap Year Compliance of the RTC Count Block
6. Time Rewrite Error
7. Registers in RTC Control Block
8. Usage Precautions

1. Overview of RTC Count Block

The RTC count block counts years, months, dates, hours, minutes, seconds, and days of the week from 00 to 99 years. Alarm and timer settings are possible as well. An alarm can be set to a specific year, month, date, hour, and minute. It can also be set to a specific year, month, date, hours, or minutes independently. A timer can be set to a period up to one day. It can be set to a desired period (with the hours, minutes, and seconds specified) or in desired intervals (with hours, minutes, and seconds specified). An overview of the RTC count block is shown below.

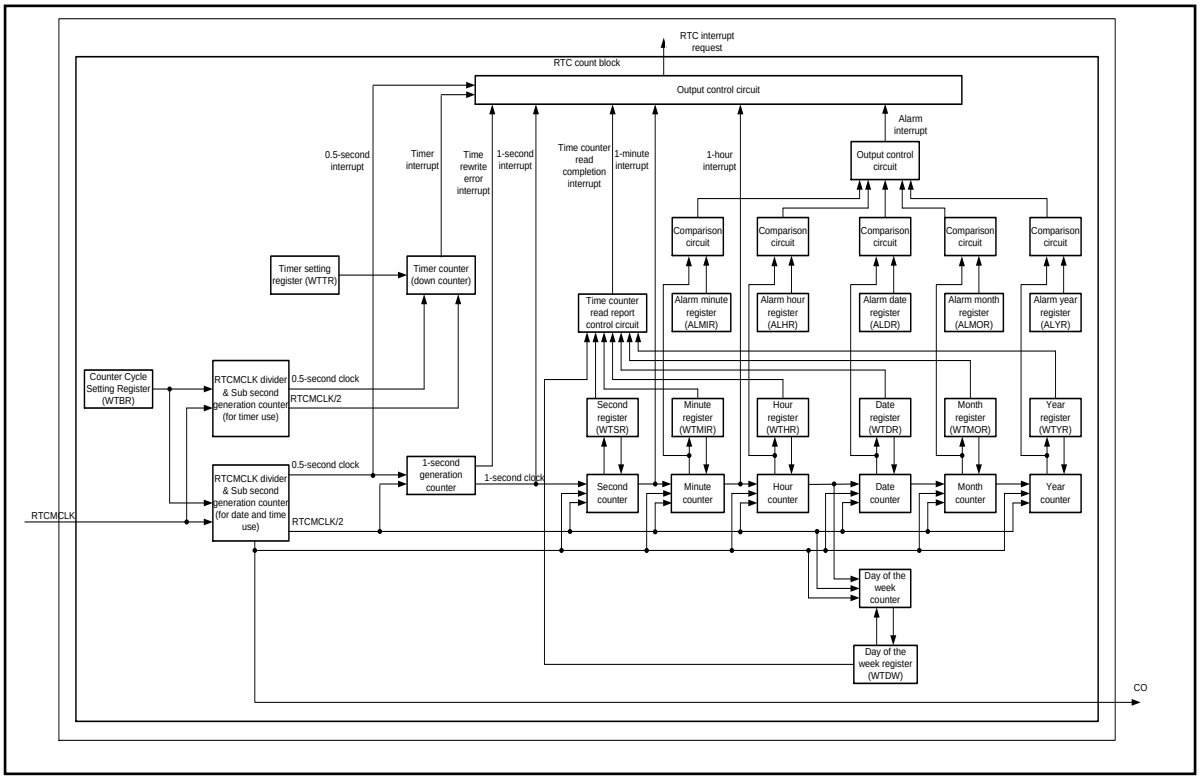
Overview of Functions of RTC Count Block

- Date and time (year/month/date/hour/minute/second/day of the week) settings
- Counts dates and time (years(00 to 99), months, days, hours, minutes, seconds, and days of the week)
- Leap year compliant (00 year is operated as leap year)
- Alarm settings with a specific date and time (year/month/date/hour/minute)
- A specific year, month, date, hour, or minute can be set individually as well
- A timer can be set to a period of up to one day. It can be set to a desired period (with the hours, minutes, and seconds specified) or in desired intervals (with hours, minutes, and seconds specified)
- It is possible to rewrite the time by resetting the watch count of the RTC count block to make time-signal-based settings
- It is possible to rewrite the time while the watch count of the RTC count block continues for time zone changes. In that case, the clock is guaranteed to continue time counting if the value is rewritten within a second
- The following interrupts can be output:
  - Alarm (with an interrupt generated at a set date and time)
  - Every hour
  - Every minute
  - Every second
  - Every 0.5 second
  - Timer
  - Time rewrite error
  - Time counter read completion
  - Pulse output in 0.5 second intervals

2. Block Diagram of RTC Count Block

Figure 2-1 shows the block diagram of the RTC count block.

Figure 2-1 Block Diagram of RTC Count Block



Counter Cycle Setting Register (WTBR)

This register stores a value to be loaded to a sub-second generation counter (for date, time, and timer use).

Set this register to a 0.5 second count value. The value in this register will be loaded to the sub-second generation counter when the RTC starts operating or the sub-second generation counter is set to 0.

RTCMCLK Divider and Sub-second Generation Counter (for Timer Use)

The RTCMCLK divider (for timer use) generates a clock from the RTCMCLK divided by 2. The sub-second generation counter (for timer use) operates at the generated clock in the RTCMCLK divider (for timer use) to count a sub-second (0.5 second) cycle.

RTCMCLK Divider and Sub-second Generation Counter (for Date and Time Use)

The RTCMCLK divider (for date and time use) generates a clock from the RTCMCLK divided by 2. The sub-second generation counter (for date and time use) operates at the generated clock in the RTCMCLK divider (for date and time use) to count a sub-second (0.5 second) cycle.

Timer Setting Register (WTTR)

This register stores a timer set value that will be up with an elapse of the set value (hours, minutes, and seconds) or in intervals of the set value (hours, minutes, and seconds).

Timer Counter (Down Counter)

The timer counter is loaded with a value set in the timer setting register, and counts down in a cycle of 0.5 second clock cycles output from the sub-second generation counter (for timer use).

1 second Generation Counter

This counter counts 0.5 second clock cycles output from the sub-second generation counter (for date and time use) and generates 1 second clock pulses.

Second Counter, Minute Counter, Hour Counter, Day Counter, Month Counter, Year Counter, and Day of the Week Counter

The second counter, minute counter, hour counter, date counter, month counter, year counter, and day of the week counter count seconds, minutes, hours, dates, months, years, and days of the week.

Second Register (WTSR), Minute Register (WTMIR), Hour Register (WTHR), Day Register (WTDR), Month Register (WTMOR), and Year Register (WTYR)

This register indicates the second, minute, hour, date, month, and year information in the RTC count block.

Time Counter Read Report Control Circuit

This circuit reports the completion of the reading of the time counter.

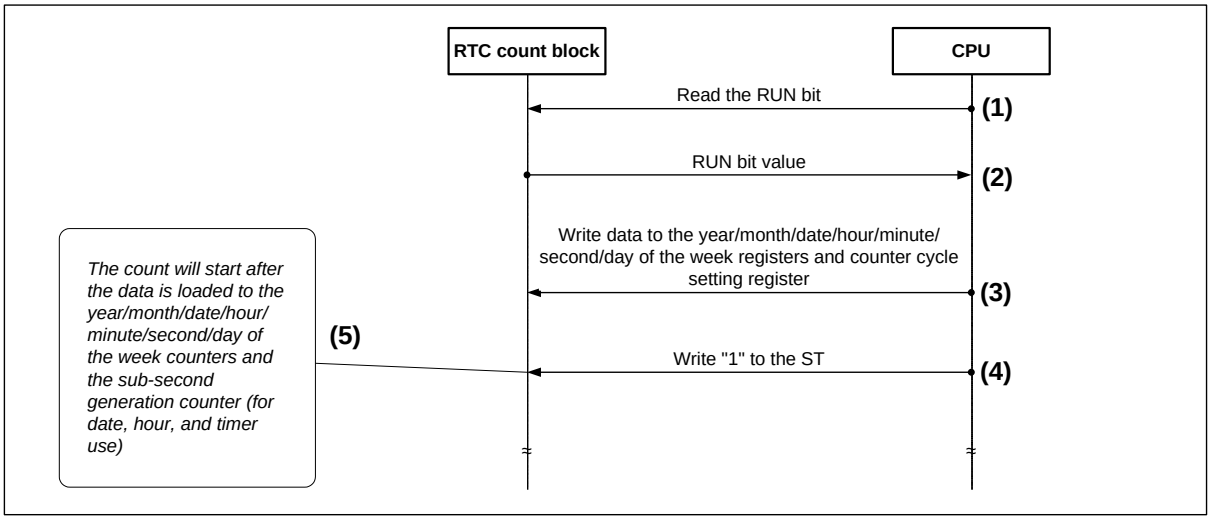
Alarm Minute Register (ALMIR), Alarm Hour Register (ALHR), Alarm Day Register (ALDR), Alarm Month Register (ALMOR) and Alarm Year Register (ALYR)

This register stores minute, hour, date, month, and year alarm set values. When an alarm is ON, the comparison circuit will compare the stored value in the register and the minute / hour / date / month / year counter value, and when the values coincides, an alarm interrupt will be generated.

3. Operations of RTC Count Block and Setting Procedures

This section explains the operation of the RTC count block and a setting procedures example.

Figure 3-1 Initial Time Setting Procedures



(1) Read the RUN bit.

(2) The following initial time settings are possible in the following flow while the RTC count block is not in operation under the following condition: RUN = 0.
See the examples of the time rewrite setting procedures (with time count continued) and time rewrite setting procedures (with time count reset) under the following condition: RUN = 1.

(3) Write the desired time to the year / month / date / hour / minute / second / day of the week registers (WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR, and WTDW). Write a desired 0.5 second count value to the counter cycle setting register (WTBR).

(4) Write the following value: ST = 1.

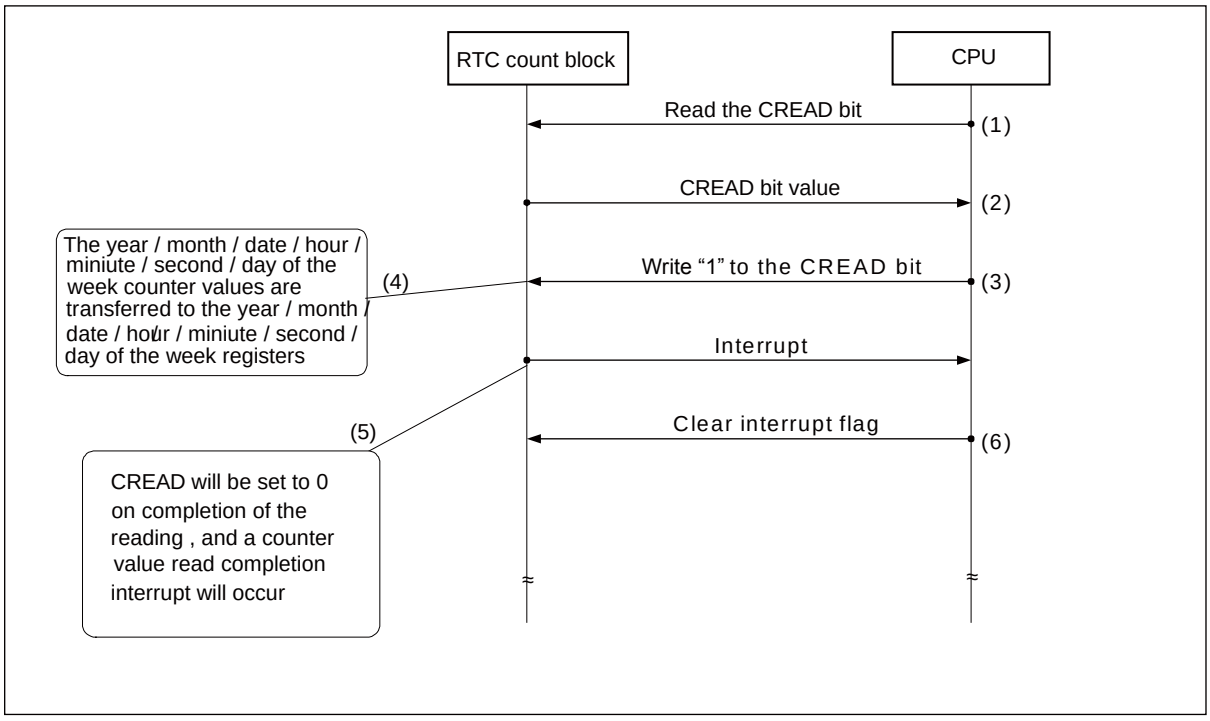
(5) When ST=1 is set, the following operations are executed to start counting:

- The year / month / date / hour / minute / second / day of the week register values are loaded to the year / month / date / hour / minute / second / day of the week counters.
- The value in the counter cycle setting register (WTBR) is loaded to the sub-second generation counters (for date, time, and timer use), and start counting.

Note:

- *If continuing the time after system reset or RTC reset, write CREAD=1 and wait CREAD=0 before writing ST=1. The time before these reset is transferred from the year/month/date/hour/minute/second/day of the week counters to the year, month, date, hour, minute, second, and day of the week registers. After writing ST=1, the value of the year, month, date, hour, minute, second, and day of the week registers is transferred to the year/month/date/hour/minute/second/day of the week counters, and it is possible to continue the time.*

Figure 3-2 Time Read Setting Procedures



(1) Read the CREAD bit.

(2) When the CREAD is 1, wait until that the CREAD value becomes 0.

(3) Write the following value: CREAD = 1.

(4) The year / month / date / hour / minute / second / day of the week counter values will be transferred to the year, month, date, hour, minute, second, and day of the week registers (WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR, WTDW).

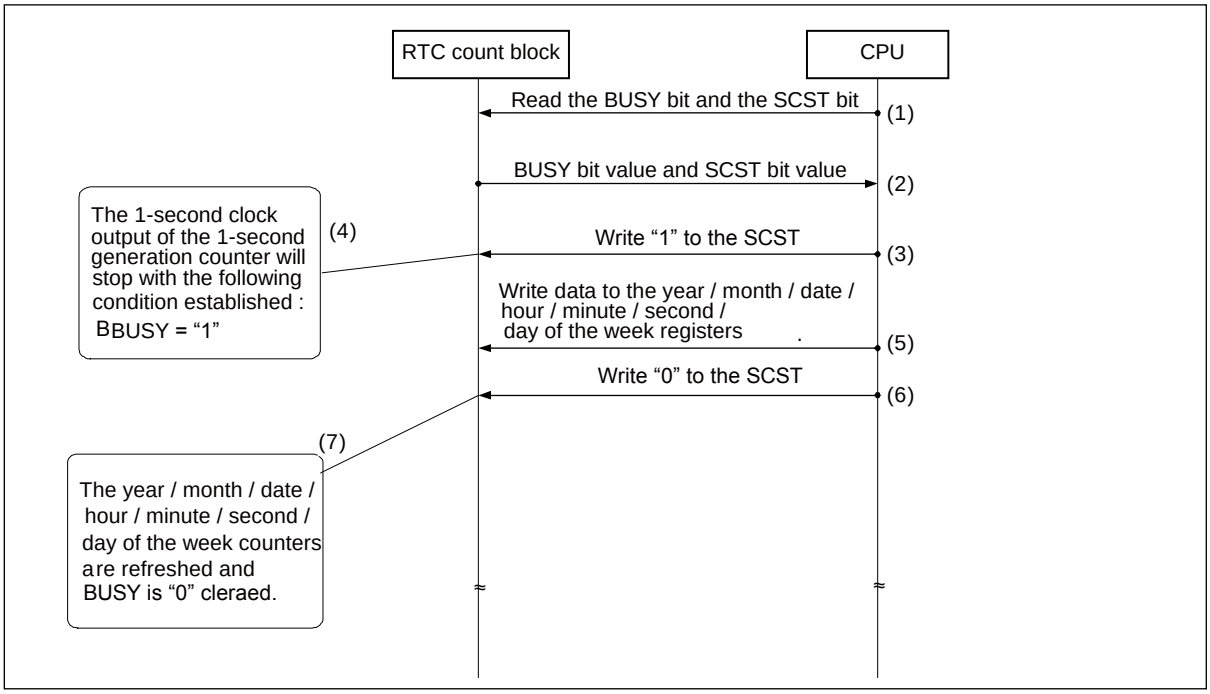
(5) When the above operation is completed, the following condition will be set :CREAD=0 and a year / month / date / hour / minute / second / day of the week counter value read completion interrupt will occur.

(6) Clear the year / month / date / hour / minute / second / day of the week counter value read completion interrupt flag bit.

Notes:

- *When CREAD=1, do not write 1 to SCST and SRST.*
- *While CREAD=1, do not set to Stop mode.*
- *After 1 is written to CREAD, do not stop the RTC count block (with 0 written to ST) until the year / month / date / hour / minute / second / day of the week counter read completion interrupt is generated.*

Figure 3-3 Time Rewrite Setting Procedures (with Time Count Continued)



(1) Read the BUSY bit and the SCST bit.

(2) If BUSY=1, wait until the following condition is established: BUSY = 0 and SCST=0.
In other cases, go to step(3).

(3) Write the following value: SCST = 1.

(4) BUSY will be set to 1.
The 1 second clock output of the 1 second generation counter will come to a stop.

(5) Write the desired year, month, date, hour, minute, second, day of the week value to the year / month / date / hour / minute / second / day of the week registers (WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR, WTDW) while the following condition is maintained: SCST = 1.

(6) Write the following value: SCST = 0.

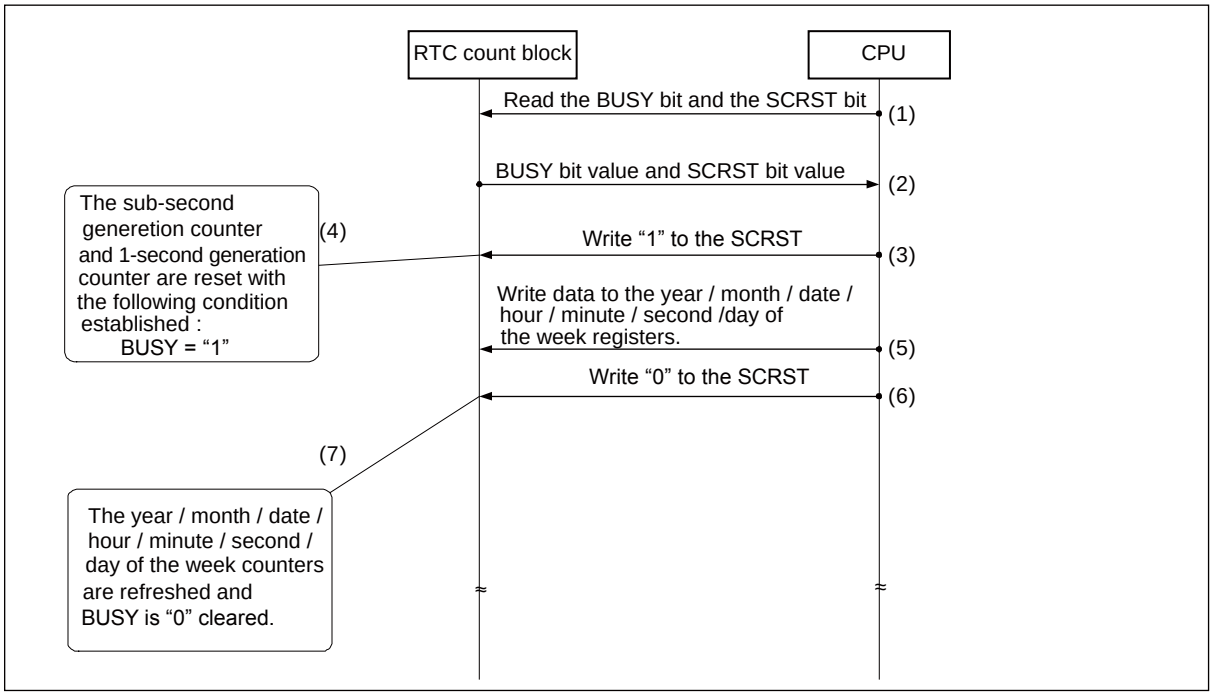
(7) Only the refreshed set values in the year / month / date / hour / minute / second / day of the week registers will be transferred to the year / month / date / hour / minute / second / day of the week counters and BUSY will be cleared to 0.

Notes:

- *Writing 1 to the SCST is not allowed under the following condition: BUSY = 1 and SCST=0.*
- *Writing 1 to SCST is not allowed under the following condition: RUN=0.*
- *Continuous time counting cannot be guaranteed if the period specified in (3) to (6) exceeds 1 second. In that case, a time rewrite error interrupt will occur. If the time lag occurs, the time rewrite error flag becomes 1. Set SCST=0 to clear the Time rewrite error flag and set the time again according to the above procedure.*
- *Writing data to the year / month / date / hour / minute / second / day of the week registers is not allowed while data is in transit from the year / month / date / hour / minute / second / day of the week registers to the year / month / date / hour / minute / second / day of the week counters under the following conditions: SCST = 0 and BUSY = 1.*

- *Keep in mind that the year / month / date / hour / minute / second / day of the week register values will be overwritten with the year / month / date / hour / minute / second / day of the week counter values if 1 is written to the CREAD before the year / month / date / hour / minute / second / day of the week counters are refreshed after the following condition is set: SCST = 1.*
- *The data transfer from the year / month / date / hour / minute / second / day of the week registers to the year / month / date / hour / minute / second / day of the week counters will not be performed correctly, and no year / month / date / hour / minute / second / day of the week counter values will be guaranteed if the STOP mode is set while the following condition is maintained: BUSY = 1.*
- *Writing 0 to ST is not allowed during BUSY = 1.*

Figure 3-4 Time Rewrite Setting Procedures (Time Count Reset)



(1) Read the BUSY bit and the SCRST bit.

(2) If BUSY = 1, wait until the following condition is established: BUSY = 0 and SCRST=0.
In other cases, go to step (3).

(3) Write the following value: SCRST = 1.

(4) BUSY will be set to 1.
The sub-second generation counter and 1 second generation counter will be reset.

(5) Write the desired new year, month, date, hour, minute, second, day of the week value to the year / month / date / hour / minute / second / day of the week registers (WTYR, WTMOR, WTDR, WTHR, WTMIR, WTSR, WTDW) while the following condition is maintained: SCRST = 1.

(6) Write the following value: SCRST = 0.

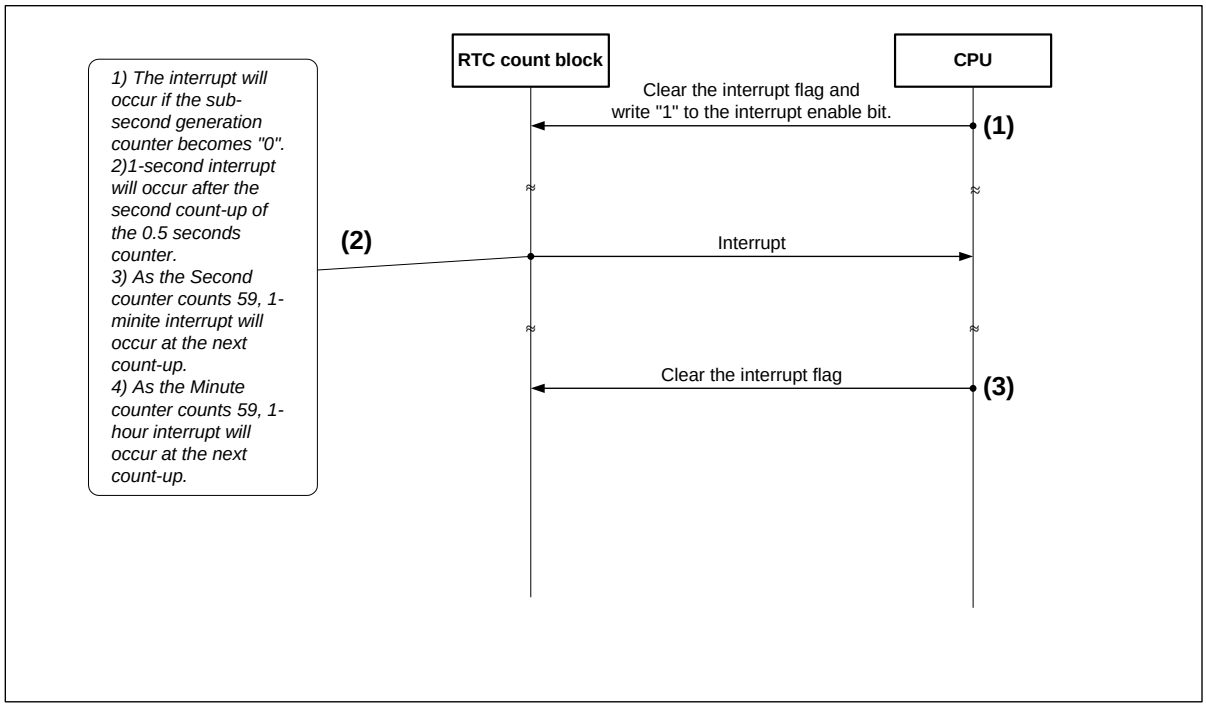
(7) Only the refreshed year / month / date / hour / minute / second / day of the week register values will be transferred to the year / month / date / hour / minute / second / day of the week counters and BUSY will be cleared to 0.

Notes:

- *Writing 1 to the SCRST is disabled under the following condition: BUSY = 1 and SCRST=0.*
- *Writing 0 to SCRST is not allowed under the following condition: RUN=0.*
- *Writing data to the year / month / date / hour / minute / second / day of the week registers are disabled while data is in transit from the year / month / date / hour / minute / second / day of the week registers to the year / month / date / hour / minute / second / day of the week counters under the following conditions: SCRST = 0 and BUSY = 1.*
- *Keep in mind that the year / month / date / hour / minute / second / day of the week register values will be overwritten with the year / month / date / hour / minute / second / day of the week counter values if CREAD is executed before the year / month / date / hour / minute / second / day of the week counters are refreshed after the following condition is set: SCRST = 1.*

- *The data transfer from the year / month / date / hour / minute / second / day of the week registers to the year / month / date / hour / minute / second / day of the week counters will not be performed correctly, and no year / month / date / hour / minute / second / day of the week counter values will be guaranteed if the STOP mode is set while the following condition is maintained: BUSY = 1.*
- *Writing 0 to ST is not allowed during BUSY=1.*

Figure 3-5 Setting Procedures of Every 0.5 second/ 1 second/ 1 minute/ 1 hour Interrupt

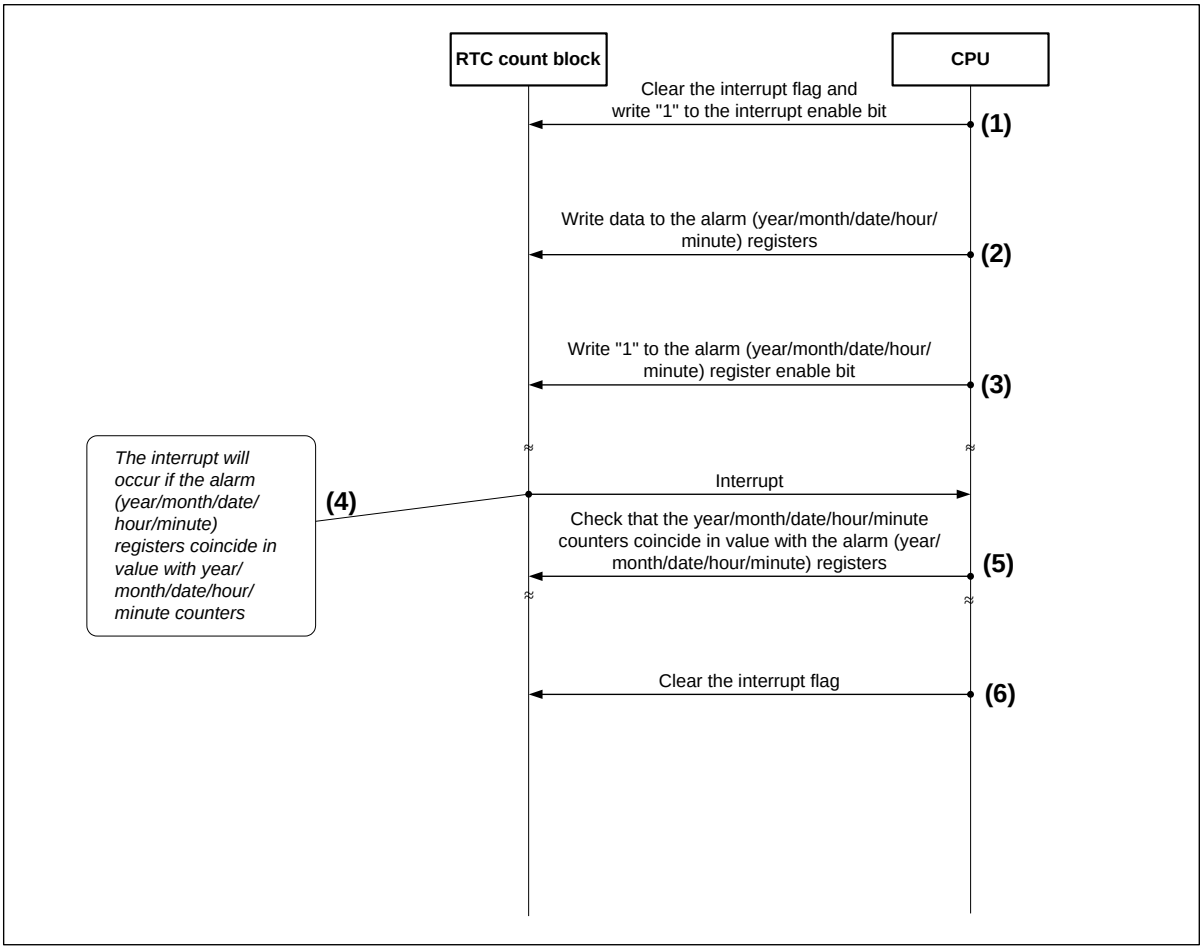


(1) Write INTSSI/ INTSI/ INTMI/ INTHI=0 to clear the interrupt flag bit.
Write 1 to the interrupt enable bit of INSSIE, INTSIE, INTMIE, or INHIE to be used to enable the interrupt.

(2) If either of 0.5 seconds / 1 second / 1 minute / 1 hour interrupt occurs, an interrupt will be generated.

(3) Write INSSIE / INTSIE / INTMIE / INHIE =0 to clear the interrupt flag bit.

Figure 3-6 Alarm Interrupt Setting Procedures



(1) Clear the alarm interrupt flag bit with the following condition written: INTALI = 0.
The alarm interrupt is enabled with the following condition written: INTALIE = 1.

(2) Write the desired time value to the alarm (year/month/date/hour/minute) registers so that the alarm interrupt will occur at the desired time.

(3) Write 1 to the alarm (year / month / date / hour / minute) register enable bit.

(4) The RTC count block interrupt request will be generated when the alarm (year / month / date / hour / minute) register values coincide with the year / month / date / hour / minute counter values.

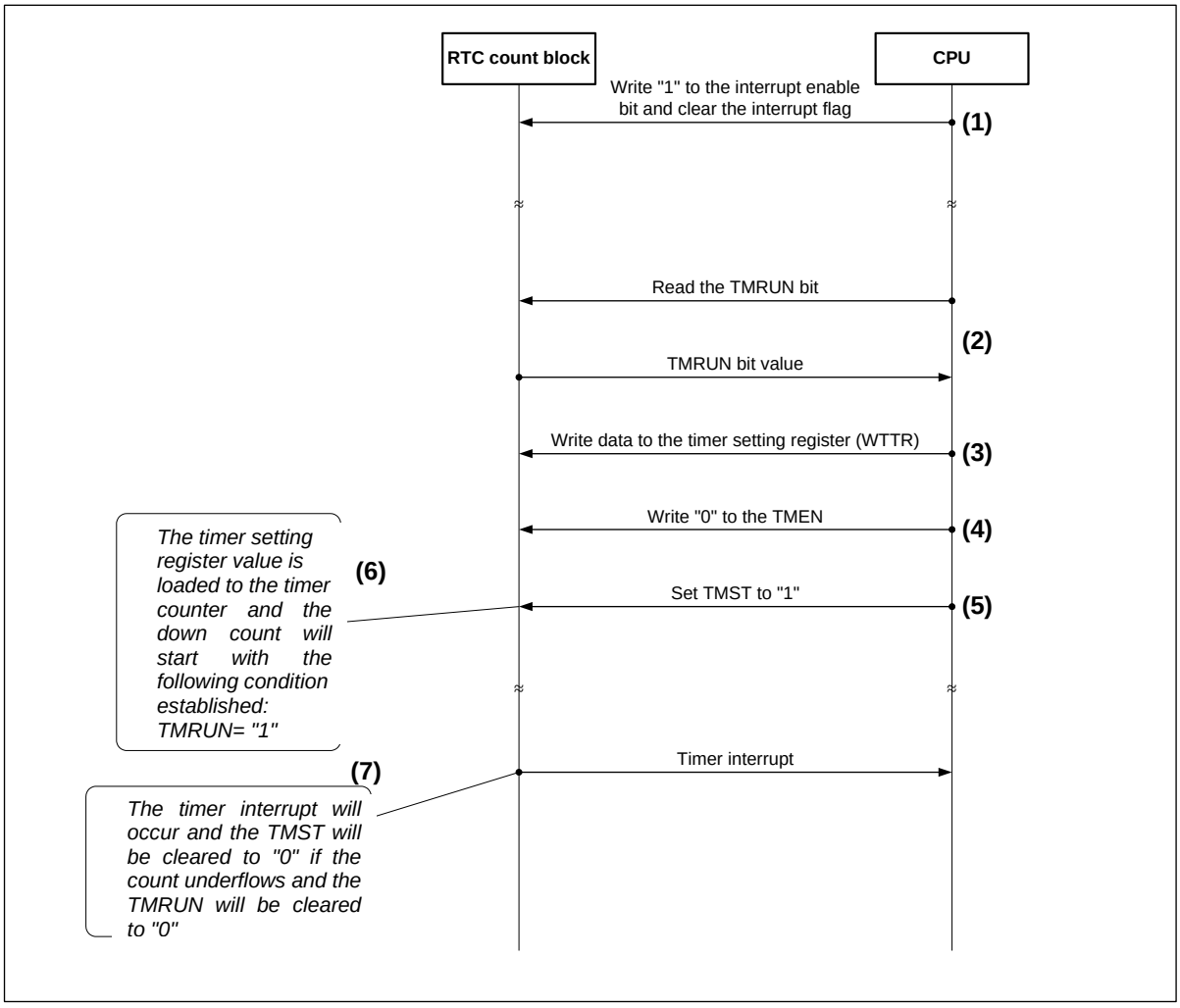
(5) Read the time by following the example of the time read setting procedures, and check that the year/month/date/hour/minute counter values coincides with the alarm (year / month / date / hour / minute) register values.

(6) Clear the alarm interrupt flag bit with the following condition written: INTALI = 0.

Note:

- *The interrupt may occur immediately after 1 is written to either of the Alarm register enable bit. Read the time after the interrupt to check the value of Year / Month / Date / Hour / Minute counter is the same as that of the Alarm (Year / Month / Date / Hour / Minute) register.*

Figure 3-7 Timer Interrupt Setting Procedures (with (Hours, Minutes, and Seconds) Elapsed)



Clear the timer interrupt flag bit with the following condition written: INTTMI = 0.

The timer interrupt is enabled with the following condition written: INTTMIE = 1.

(1) Read the timer counter operation bit (TMRUN) and check whether the value is 0 (not in operation).

(2) Write the desired timer set value to the timer setting register (WTTR).

(3) Write 0 to the timer counter control bit (TMEN).

(4) Write 1 to the timer counter start bit (TMST).

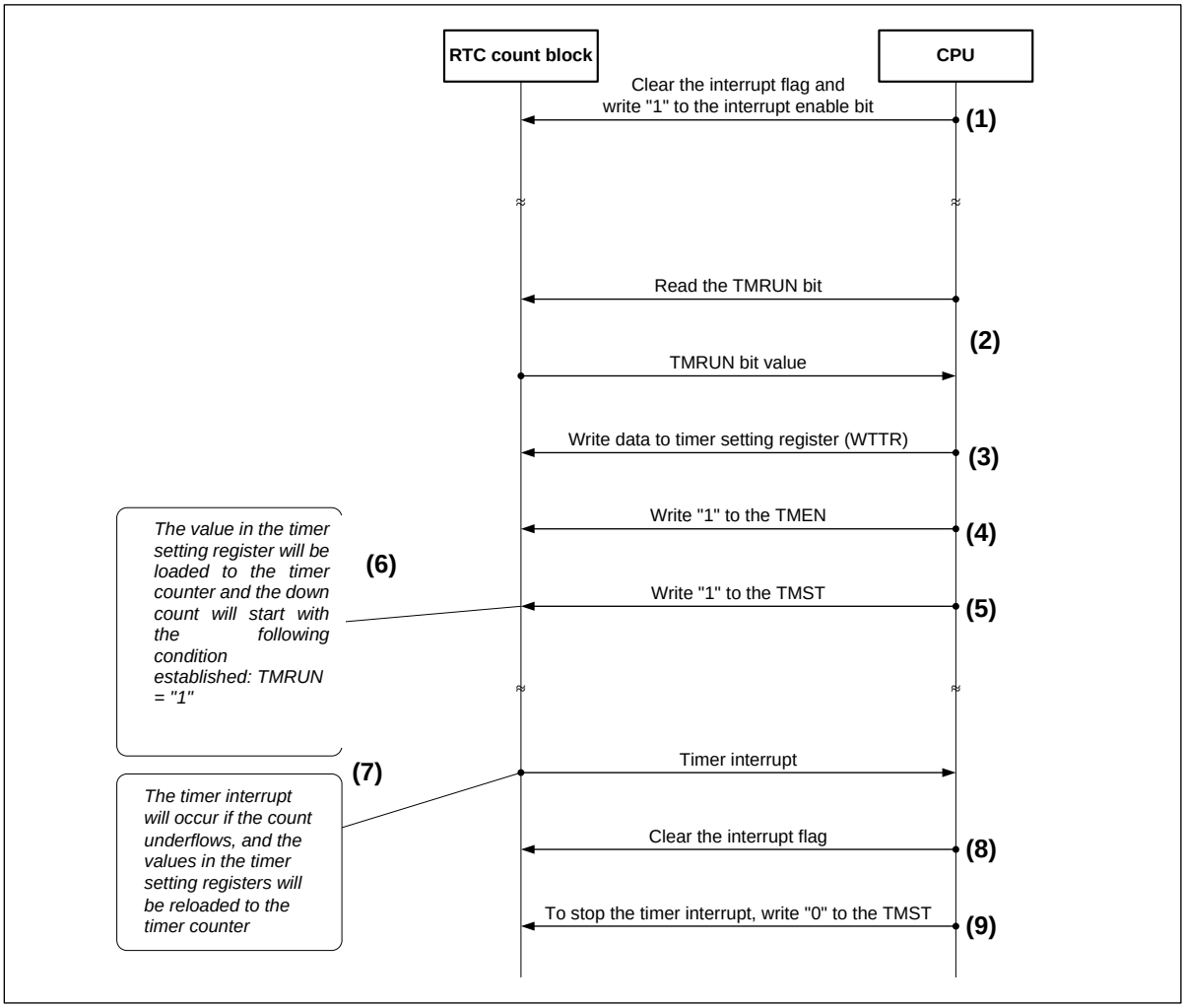
(5) The set value in the timer setting register value will be transferred to the timer counter, and the down count will start.

(6) If the down count underflows, an interrupt request will be generated, and TMST will be cleared to 0. Then the TMRUN will be cleared to 0 after the timer counter is stopped.

Notes:

- *Writing 1 to the TMST is disabled before the TMRUN value becomes 0 after 0 is written to the TMST while the timer counter is in operation (TMRUN = 1).*
- *TMEN settings can be changed only when the timer counter is not in operation (TMRUN = 0).*

Figure 3-8 Timer Interrupt Setting Procedures (in Intervals of (Hours, Minutes, and Seconds) Elapsed)



(1) Clear the timer interrupt flag bit with the following condition written: INTTMI = 0.
The timer interrupt is enabled with the following condition written: INTTMIE = 1.

(2) Read the timer counter operation bit (TMRUN) and check whether the value is 0 (not in operation).

(3) Write the desired timer set value to the timer setting register (WTTR).

(4) Write 1 to the timer counter control bit (TMEN).

(5) Write 1 to the timer counter start bit (TMST).

(6) The set value in the timer setting register value will be transferred to the timer counter, and the down count will start.

(7) The RTC count block interrupt request will be generated on completion of the count, and the timer setting register value will be reloaded to the timer counter to continue operation.

(8) Clear the timer interrupt flag bit with the following condition written: INTTMI = 0.

(9) To stop the timer interrupt, write 0 to the TMST.

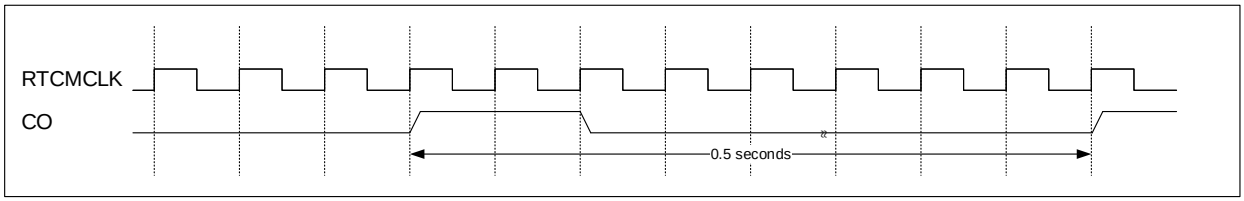
Notes:

- *Writing 1 to the TMST is disabled before the TMRUN value becomes 0 after 0 is written to the TMST while the timer counter is in operation (TMRUN = 1).*
- *TMEN settings can be changed only when the timer counter is not in operation (TMRUN = 0).*

Output Operation of CO External Pin

The RTC count block incorporates a CO external pin for a 0.5 second-clock output.
The CO external pin will output in 0.5 second clock (CO) cycles.
Figure 3-9 shows the waveform of CO external pin output.

Figure 3-9 Waveform of the CO External Pin Output



4. RTC Count Block Reset Operation

This section explains each reset action.

Low-voltage Detection Reset / Power-on Reset Operation

The shaded parts in Table 4-1are bits that are subject to low-voltage detection resetting/power-on resetting.

The sub-second generation counter, 1 second generation counter, timer counter, and year/month/date/hour/ minute/second/day of the week counter are subject to low-voltage detection resetting/power-on resetting as well, though these items are not shown in Table 4-1.

Table 4-1 Low-voltage Detection Reset/ Power-on Reset Target Bits

	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WTCR1	INTCRIE	INTERIE	INTALIE	INTTMIE	INTHIE	INTMIE	INTSIE	INTSSIE	INTCRI	INTERI	INTALI	INTTMI	INTHI	INTMI	INTSI	INTSSI
	-	-	-	YEN	MOEN	DEN	HEN	MIEN	-	BUSY	SCRST	SCST	SRST	RUN	OE	ST
WTCR2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	-	-	-	-	-	TMRUN	TMEN	TMST	-	-	-	-	-	-	-	CREAD
WTBR	-	-	-	-	-	-	-	-	BR23	BR22	BR21	BR20	BR19	BR18	BR17	BR16
	BR15	BR14	BR13	BR12	BR11	BR10	BR9	BR8	BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
WTDR/WTHR/ WTMIR/WTSR	-	-	TD1	TD0	D3	D2	D1	D0	-	-	TH1	TH0	H3	H2	H1	H0
	-	TMI2	TMI1	TMI0	MI3	MI2	MI1	MI0	-	TS2	TS1	TS0	S3	S2	S1	S0
WTYR/WTMOR/WTDW	-	-	-	-	-	-	-	-	TY3	TY2	TY1	TY0	Y3	Y2	Y1	Y0
	-	-	-	TMO0	MO3	MO2	MO1	MO0	-	-	-	-	-	DW2	DW1	DW0
ALDR/ALHR/ ALMIR	-	-	TAD1	TAD0	AD3	AD2	AD1	AD0	-	-	TAH1	TAH0	AH3	AH2	AH1	AH0
	-	TAMI2	TAMI1	TAMI0	AMI3	AMI2	AMI1	AMI0	-	-	-	-	-	-	-	-
ALYR/ALMOR	-	-	-	-	-	-	-	-	TAY3	TAY2	TAY1	TAY0	AY3	AY2	AY1	AY0
	-	-	-	TAMO0	AMO3	AMO2	AMO1	AMO0	-	-	-	-	-	-	-	-
WTTR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	TM17	TM16
	TM15	TM14	TM13	TM12	TM11	TM10	TM9	TM8	TM7	TM6	TM5	TM4	TM3	TM2	TM1	TM0

System Reset Operation

The shaded parts in Table 4-2 are bits that are subject to system resetting.

The 1 second generation counter and timer counter are subject to system resetting as well, though these items are not shown in Table 4-2.

The sub-second generation counter (for date, time, and timer use) and the year / month / date / hour / minute / second / day of the week counters are not subject to resetting.

Table 4-2 System Reset Target Bits

	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WTCR1	INTCRIE	INTERIE	INTALIE	INTTMIE	INTHIE	INTMIE	INTSIE	INTSSIE	INTCRI	INTERI	INTALI	INTTMI	INTHI	INTMI	INTSI	INTSSI
	-	-	-	YEN	MOEN	DEN	HEN	MIEN	-	BUSY	SCRST	SCST	SRST	RUN	OE	ST
WTCR2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	-	-	-	-	-	TMRUN	TMEN	TMST	-	-	-	-	-	-	-	CREAD
WTBR	-	-	-	-	-	-	-	-	BR23	BR22	BR21	BR20	BR19	BR18	BR17	BR16
	BR15	BR14	BR13	BR12	BR11	BR10	BR9	BR8	BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
WTDR/WTHR/ WTMIR/WTSR	-	-	TD1	TD0	D3	D2	D1	D0	-	-	TH1	TH0	H3	H2	H1	H0
	-	TMI2	TMI1	TMI0	MI3	MI2	MI1	MI0	-	TS2	TS1	TS0	S3	S2	S1	S0
WTYR/WTMO R/WTDW	-	-	-	-	-	-	-	-	TY3	TY2	TY1	TY0	Y3	Y2	Y1	Y0
	-	-	-	TMO0	MO3	MO2	MO1	MO0	-	-	-	-	-	DW2	DW1	DW0
ALDR/ALHR/ ALMIR	-	-	TAD1	TAD0	AD3	AD2	AD1	AD0	-	-	TAH1	TAH0	AH3	AH2	AH1	AH0
	-	TAMI2	TAMI1	TAMI0	AMI3	AMI2	AMI1	AMI0	-	-	-	-	-	-	-	-
ALYR/ALMOR	-	-	-	-	-	-	-	-	TAY3	TAY2	TAY1	TAY0	AY3	AY2	AY1	AY0
	-	-	-	TAMO0	AMO3	AMO2	AMO1	AMO0	-	-	-	-	-	-	-	-
WTTR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	TM17	TM16
	TM15	TM14	TM13	TM12	TM11	TM10	TM9	TM8	TM7	TM6	TM5	TM4	TM3	TM2	TM1	TM0

RTC Reset Operation

The shaded parts in Table 4-3 are bits that are subject to RTC resetting.

The 1 second generation counter and timer counter are subject to RTC resetting as well, though these items are not shown in Table 4-3.

The sub-second generation counter (for date, time, and timer use) and the year / month / date / hour / minute / second / day of the week counters are not subject to resetting.

Table 4-3 RTC Reset Target Bits

	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WTCR1	INTCRIE	INTERIE	INTALIE	INTTMIE	INTHIE	INTMIE	INTSIE	INTSSIE	INTCRI	INTERI	INTALI	INTTMI	INTHI	INTMI	INTSI	INTSSI
	-	-	-	YEN	MOEN	DEN	HEN	MIEN	-	BUSY	SCRST	SCST	SRST	RUN	OE	ST
WTCR2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	-	-	-	-	-	TMRUN	TMEN	TMST	-	-	-	-	-	-	-	CREAD
WTBR	-	-	-	-	-	-	-	-	BR23	BR22	BR21	BR20	BR19	BR18	BR17	BR16
	BR15	BR14	BR13	BR12	BR11	BR10	BR9	BR8	BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
WTDR/WTHR/ WTMIR/WTSR	-	-	TD1	TD0	D3	D2	D1	D0	-	-	TH1	TH0	H3	H2	H1	H0
	-	TMI2	TMI1	TMI0	MI3	MI2	MI1	MI0	-	TS2	TS1	TS0	S3	S2	S1	S0
WTYR/WTMOR/ WTDW	-	-	-	-	-	-	-	-	TY3	TY2	TY1	TY0	Y3	Y2	Y1	Y0
	-	-	-	TMO0	MO3	MO2	MO1	MO0	-	-	-	-	-	DW2	DW1	DW0
ALDR/ALHR/ ALMIR	-	-	TAD1	TAD0	AD3	AD2	AD1	AD0	-	-	TAH1	TAH0	AH3	AH2	AH1	AH0
	-	TAMI2	TAMI1	TAMI0	AMI3	AMI2	AMI1	AMI0	-	-	-	-	-	-	-	-
ALYR/ALMOR	-	-	-	-	-	-	-	-	TAY3	TAY2	TAY1	TAY0	AY3	AY2	AY1	AY0
	-	-	-	TAMO0	AMO3	AMO2	AMO1	AMO0	-	-	-	-	-	-	-	-
WTTR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	TM17	TM16
	TM15	TM14	TM13	TM12	TM11	TM10	TM9	TM8	TM7	TM6	TM5	TM4	TM3	TM2	TM1	TM0

5. Leap Year Compliance of the RTC Count Block

This section explains the leap year compliance of the RTC count block.

Leap Year Compliance

Table 5-1 shows the days of each month.

Table 5-1 List of Leap Years

Year	Leap Year	Month											
		1	2	3	4	5	6	7	8	9	10	11	12
00	○	31	29	31	30	31	30	31	31	30	31	30	31
01 to 03	×	31	28	31	30	31	30	31	31	30	31	30	31
04	○	31	29	31	30	31	30	31	31	30	31	30	31
05 to 07	×	31	28	31	30	31	30	31	31	30	31	30	31
08	○	31	29	31	30	31	30	31	31	30	31	30	31
09 to 11	×	31	28	31	30	31	30	31	31	30	31	30	31
12	○	31	29	31	30	31	30	31	31	30	31	30	31
13 to 15	×	31	28	31	30	31	30	31	31	30	31	30	31
16	○	31	29	31	30	31	30	31	31	30	31	30	31
17 to 19	×	31	28	31	30	31	30	31	31	30	31	30	31
20	○	31	29	31	30	31	30	31	31	30	31	30	31
21 to 23	×	31	28	31	30	31	30	31	31	30	31	30	31
24	○	31	29	31	30	31	30	31	31	30	31	30	31
25 to 27	×	31	28	31	30	31	30	31	31	30	31	30	31
28	○	31	29	31	30	31	30	31	31	30	31	30	31
29 to 31	×	31	28	31	30	31	30	31	31	30	31	30	31
32	○	31	29	31	30	31	30	31	31	30	31	30	31
33 to 35	×	31	28	31	30	31	30	31	31	30	31	30	31
36	○	31	29	31	30	31	30	31	31	30	31	30	31
37 to 39	×	31	28	31	30	31	30	31	31	30	31	30	31
40	○	31	29	31	30	31	30	31	31	30	31	30	31
41 to 43	×	31	28	31	30	31	30	31	31	30	31	30	31
44	○	31	29	31	30	31	30	31	31	30	31	30	31
45 to 47	×	31	28	31	30	31	30	31	31	30	31	30	31
48	○	31	29	31	30	31	30	31	31	30	31	30	31
49 to 51	×	31	28	31	30	31	30	31	31	30	31	30	31
52	○	31	29	31	30	31	30	31	31	30	31	30	31
53 to 55	×	31	28	31	30	31	30	31	31	30	31	30	31
56	○	31	29	31	30	31	30	31	31	30	31	30	31
57 to 59	×	31	28	31	30	31	30	31	31	30	31	30	31
60	○	31	29	31	30	31	30	31	31	30	31	30	31
61 to 63	×	31	28	31	30	31	30	31	31	30	31	30	31
64	○	31	29	31	30	31	30	31	31	30	31	30	31
65 to 67	×	31	28	31	30	31	30	31	31	30	31	30	31
68	○	31	29	31	30	31	30	31	31	30	31	30	31
69 to 71	×	31	28	31	30	31	30	31	31	30	31	30	31
72	○	31	29	31	30	31	30	31	31	30	31	30	31
73 to 75	×	31	28	31	30	31	30	31	31	30	31	30	31

Year	Leap Year	Month											
		1	2	3	4	5	6	7	8	9	10	11	12
76	○	31	29	31	30	31	30	31	31	30	31	30	31
77 to 79	×	31	28	31	30	31	30	31	31	30	31	30	31
80	○	31	29	31	30	31	30	31	31	30	31	30	31
81 to 83	×	31	28	31	30	31	30	31	31	30	31	30	31
84	○	31	29	31	30	31	30	31	31	30	31	30	31
85 to 87	×	31	28	31	30	31	30	31	31	30	31	30	31
88	○	31	29	31	30	31	30	31	31	30	31	30	31
89 to 91	×	31	28	31	30	31	30	31	31	30	31	30	31
92	○	31	29	31	30	31	30	31	31	30	31	30	31
93 to 95	×	31	28	31	30	31	30	31	31	30	31	30	31
96	○	31	29	31	30	31	30	31	31	30	31	30	31
97 to 99	×	31	28	31	30	31	30	31	31	30	31	30	31

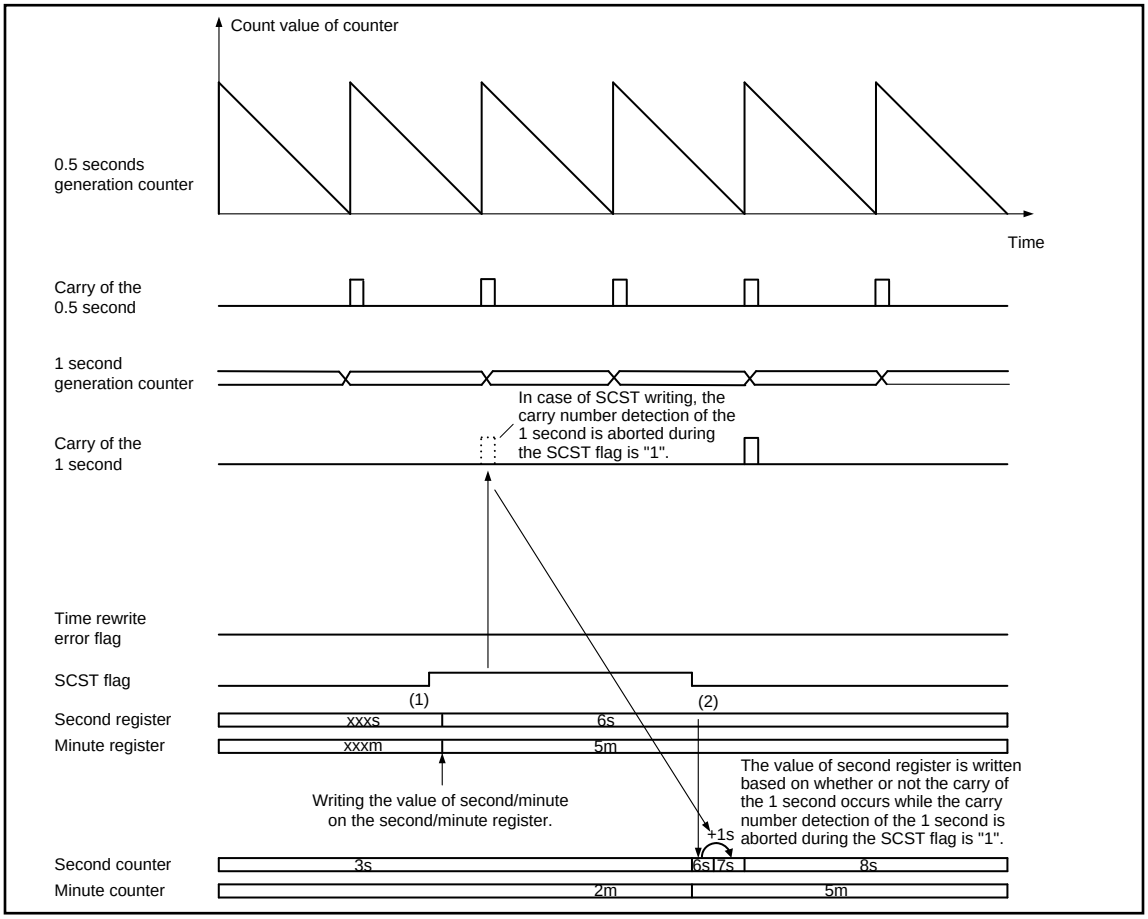
6. Time Rewrite Error

This section explains the time rewrite error during time rewrite (with time count continued).

Time Rewrite Error 1

The following provides an example that the carry number of the 0.5 seconds generation counter is two while the SCST flag is set to 1 during time rewriting (with time count continued).

■ Rewriting second counter and minute counter only



(1) Set the SCST flag to 1, and write 6 seconds on the second register and 5 minutes on the minute register.

(2) When the carry number of the 0.5 seconds is two while the SCST flag is set to 1 and then the SCST flag is set to 0. 6 seconds will be written on the second counter, then 1 is added and consequently the counter will be 7 seconds.

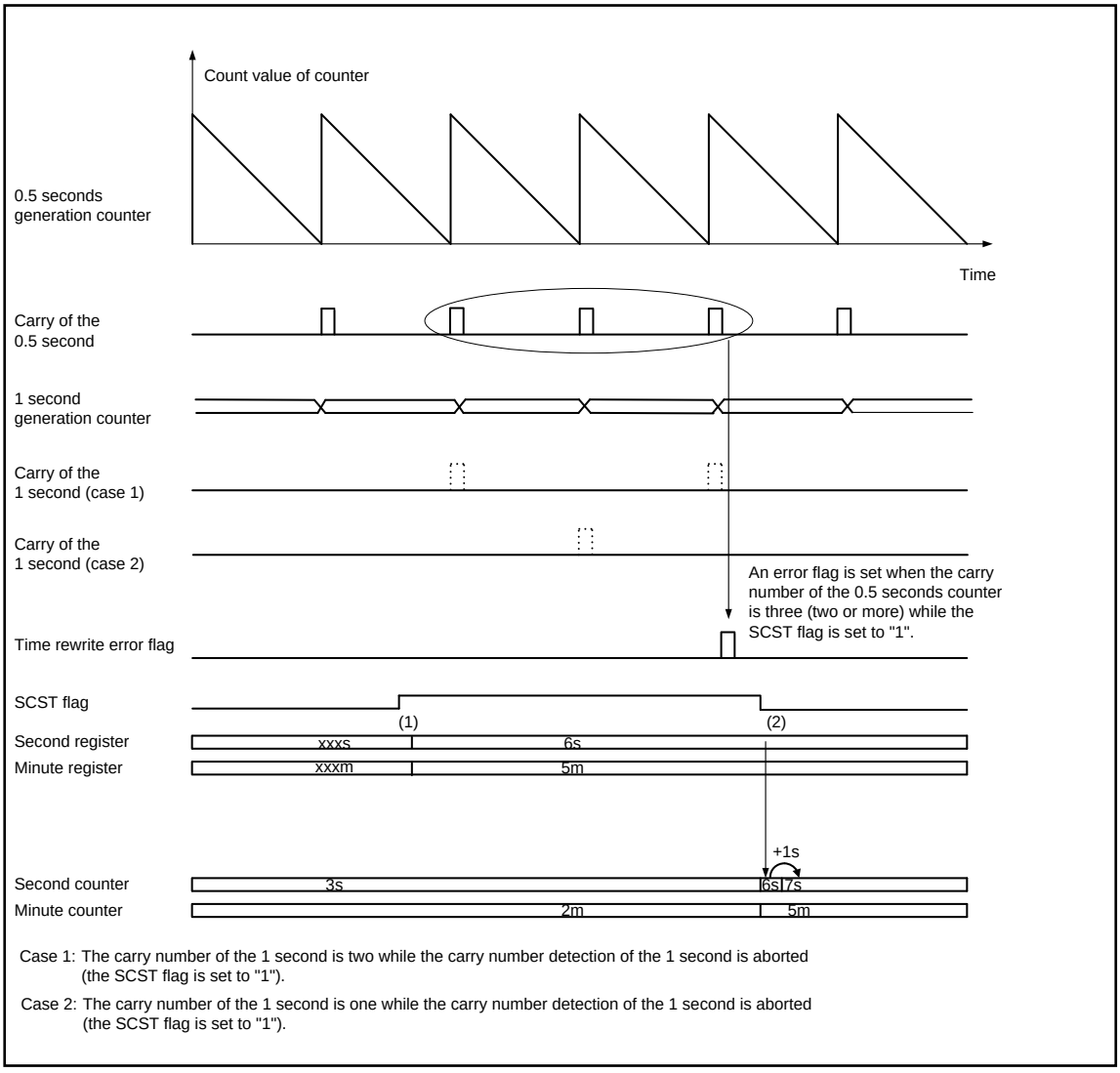
Notes:

- *If the carry number of the 0.5 seconds is two or less while the SCST flag is set to 1, the time rewrite error flag does not become 1.*
- *Because the carry number detection of the 1 second is aborted while the SCST flag is set to 1, the second counter does not count. When the carry number detection of the 1 second is aborted, the carry number of the 1 second is saved. Then, the value of second register is written on the second counter when the SCST flag is set to 0, and then 1 is added. If there is no carry of the 1 second while the SCST flag is set to 1, the value of second register is written on the second counter, however, 1 is not added.*

Time Rewrite Error 2

The following provides an example that the carry number of the 0.5 seconds generation counter is three while the SCST flag is set to 1 during time rewriting (with time count continued).

■ Rewriting second counter and minute counter only



(1) Set the SCST flag to 1, and write 6 seconds on the second register and 5 minutes on the minute register.

(2) When the carry number of the 0.5 seconds is three while the SCST flag is set to 1 and then the SCST flag is set to 0, the time rewrite error flag will be set to 1. 6 seconds will be written on the second counter, then 1 is added and consequently the counter will be 7 seconds.

Note:

- *When the time rewrite error flag is set to 1, a 1 second shift will occur for case 1 because the carry number of the 1 second is two while the carry number detection of the 1 second is aborted (the SCST flag is set to 1). The 1 second shift will not occur for case 2 because the carry number of the 1 second is one while the carry number detection of the 1 second is aborted (the SCST flag is set to 1). However, if a time rewrite error occurred, perform time rewriting again because you cannot determine which case happened.*

7. Registers in RTC Control Block

The Registers of the RTC count block are listed below.

List of Registers in the RTC Count Block

Table 7-1 List of Registers in RTC Count Block

Abbreviation	Register Name	Reference
WTCR1	Control register 1	7.1
WTCR2	Control register 2	7.2
WTBR	Counter cycle setting register	7.3
WTDR	Date register	7.4
WTHR	Hour register	7.5
WTMIR	Minute register	7.6
WTSR	Second register	7.7
WTYR	Year register	7.8
WTMOR	Month register	7.9
WTDW	Day of the week register	7.10
ALDR	Alarm date register	7.11
ALHR	Alarm hour register	7.12
ALMIR	Alarm minute register	7.13
ALYR	Alarm year register	7.14
ALMOR	Alarm month register	7.15
WTTR	Timer setting register	7.16

7.1 Control Register 1 (WTCR 1)

This register is used to control the operation of the RTC count block.

bit	31	30	29	28	27	26	25	24
Field	INTCRIE	INTERIE	INTALIE	INTTMIE	INTHIE	INTMIE	INTSIE	INTSSIE
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

bit	23	22	21	20	19	18	17	16
Field	INTCRI	INTERI	INTALI	INTTMI	INTHI	INTMI	INTSI	INTSSI
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

bit	15	14	13	12	11	10	9	8
Field	Reserved			YEN	MOEN	DEN	HEN	MIEN
Attribute		R		R/W	R/W	R/W	R/W	R/W
Initial value		000		0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Field	Reserved	BUSY	SCRST	SCST	SRST	RUN	Reserved	ST
Attribute	R	R	R/W	R/W	R/W	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

[bit31] INTCRIE: Year / month / day / hour / minute / second / day of the week counter value read completion interrupt enable bit

This is the year / month / date / hour / minute / second / day of the week counter value read completion interrupt enable bit.

Bit	Description
0	Interrupt disabled
1	Interrupt enabled.

[bit30] INTERIE: Time rewrite error interrupt enable bit

This is the time rewrite error interrupt enable bit.

Bit	Description
0	Interrupt disabled.
1	Interrupt enabled.

[bit29] INTALIE: Alarm interrupt enable bit

This is the alarm interrupt enable bit.

Bit	Description
0	Interrupt disabled
1	Interrupt enabled.

[bit28] INTTMIE: Timer underflow interrupt enable bit

This is the timer interrupt enable bit.

Bit	Description
0	Interrupt disabled
1	Interrupt enabled.

[bit27] INTHIE: 1-hour interrupt enable bit

This is the 1-hour interrupt enable bit.

Bit	Description
0	Interrupt disabled
1	Interrupt enabled.

[bit26] INTMIE: 1-minute interrupt enable bit

This is the 1-minute interrupt enable bit.

Bit	Description
0	Interrupt disabled
1	Interrupt enabled.

[bit25] INTSIE: 1 second interrupt enable bit

This is the 1 second interrupt enable bit.

Bit	Description
0	Interrupt disabled.
1	Interrupt enabled.

[bit24] INTSSIE: 0.5 second interrupt enable bit

This is the 0.5 second interrupt enable bit.

Bit	Description
0	Interrupt disabled
1	Interrupt enabled.

[bit23] INTCRI: Year / month / date / hour / minute / second / day of the week counter value read completion interrupt flag bit

This bit indicates the completion of the transfer of the year / month / date / hour / minute / second / day of the week counter values to the year/month/date/hour/minute/second/day of the week registers at the time of the date and time reading with the CREAD bit.

Always 1 will be read at the time of the read access in the read modify write access mode.

Bit		Description
Read	0	The year / month / date / hour / minute / second / day of the week counter value read has not been completed
	1	The year / month / date / hour / minute / second / day of the week counter value read has been completed
Write	0	This flag is cleared
	1	No effect on operation

[bit22] INTERI: Time rewrite error flag bit

This bit shows that the second counter has not been counting normally during time rewriting (SCST = 1).
Always 1 will be read at the time of the read access in the read modify write access mode.

Bit		Description
Read	0	No time rewriting error has been generated
	1	A time rewriting error has been generated
Write	0	This flag is cleared
	1	No effect on operation.

[bit21] INTALI: Alarm coinciding flag bit

This bit shows that the year/month/date/hour/minute register value coincides with the year / month / date / hour / minute counter value.
Always 1 will be read at the time of the read access in the read modify write access mode.

Bit		Description
Read	0	No alarm coinciding has been generated
	1	An alarm coinciding has been generated
Write	0	This flag is cleared.
	1	No effect on operation.

[bit20] INTTMI: Timer underflow flag bit

This flag will be set to 1 if the timer counter underflows.
Always 1 will be read at the time of the read access in the read modify write access mode.

Bit		Description
Read	0	No timer underflow has been generated
	1	A timer underflow has been generated
Write	0	This flag is cleared.
	1	No effect on operation.

[bit19] INTHI: 1 hour flag bit

This flag will be set to 1 if the 1 hour counter is up.
Always 1 will be read at the time of the read access in the read modify write access mode.

Bit		Description
Read	0	No 1 hour count-up has been generated
	1	A 1 hour count-up has been generated
Write	0	This flag is cleared
	1	No effect on operation.

[bit18] INTMI: 1 minute flag bit

This flag will be set to 1 if the 1 minute counter is up.
Always 1 will be read at the time of the read access in the read modify write access mode.

Bit		Description
Read	0	No 1 minute count-up has been generated
	1	A 1 minute count-up has been generated
Write	0	This flag is cleared
	1	No effect on operation.

[bit17] INTSI: 1 second flag bit

This flag will be set to 1 if the 1-second counter is up.
Always 1 will be read at the time of the read access in the read modify write access mode.

Bit		Description
Read	0	No 1 second count-up has been generated
	1	A 1 second count-up has been generated
Write	0	This flag is cleared
	1	No effect on operation.

[bit16] INTSSI: 0.5 second flag bit

This flag will be set to 1 if the 0.5 second counter is up.
Always 1 will be read at the time of the read access in the read modify write access mode.

Bit		Description
Read	0	No 0.5 second count-up has been generated
	1	A 0.5 second count-up has been generated
Write	0	This flag is cleared
	1	No effect on operation.

[bit15:13] Reserved: Reserved bits

Always 0 is read.
Set 0 when writing data.

[bit12] YEN: Alarm year register enable bit

This bit enables the comparison of the alarm year register and the year counter in the alarm interrupt.
When this bit is set to 1, this can be detected by the alarm interrupt flag (INTALI).

Bit	Description
0	The alarm year register is disabled
1	The alarm year register is enabled

[bit11] MOEN: Alarm month register enable bit

This bit enables the comparison of the alarm month register and the month counter.
When this bit is set to 1, this can be detected by the alarm coinciding flag (INTALI).

Bit	Description
0	The alarm month register is disabled.
1	The alarm month register is enabled.

[bit10] DEN: Alarm day register enable bit

This bit enables the comparison of the alarm date register and the date counter.
When this bit is set to 1, this can be detected by the alarm coinciding flag (INTALI).

Bit	Description
0	The alarm date register is disabled.
1	The alarm date register is enabled.

[bit9] HEN: Alarm hour register enable bit

This bit enables the comparison of the alarm hour register and the hour counter.
When this bit is set to 1, this can be detected by the alarm coinciding flag (INTALI).

Bit	Description
0	The alarm hour register is disabled.
1	The alarm hour register is enabled.

[bit8] MIEN: Alarm minute register enable bit

This bit enables the comparison of the alarm minute register and the minute counter.
When this bit is set to 1, this can be detected by the alarm coinciding flag (INTALI).

Bit	Description
0	The alarm minute register is disabled.
1	The alarm minute register is enabled.

[bit7] Reserved: Reserved bit

Always 0 is read.
Set 0 when writing data.

[bit6] BUSY: Busy bit

This bit indicates that time rewriting is in process.

Bit	Description
0	Time rewriting is not in process
1	One of the following conditions: − SCST = 1 − SCRST = 1 − The set values in the year/month/date/hour/minute/second/day of the week registers are being transferred to the year/month/date/hour/minute/second/day of the week counters

[bit5] SCRST: Sub-second generation/ 1-second generation counter reset bit

This bit performs the reset control of the sub-second generation/1-second generation counter (for date and time use).

bit	Description
0	This bit releases the reset state of the sub-second generation / 1 second generation counter (for date and time use)
1	This bit resets the sub-second generation / 1 second generation counter (for date and time use)

When this bit is 0 and SCST bit is 0 while RTC is operating (RUN=1), the values in the year / month / date / hour / minute / second / day of the week registers cannot be refreshed. SCST bit and SCRST bit must not be simultaneously set to 1. This bit must not be set to 1 while RTC is stopped (RUN=0).

[bit4] SCST: 1 second clock output stop bit

This bit controls the 1 second clock output of the 1 second generation counter.

Bit	Description
0	Output is enabled
1	Output is disabled

When this bit is 0 and SCRST bit is 0 while RTC is operating (RUN=1), the values in the year / month / date / hour / minute / second / day of the week registers cannot be refreshed. SCST bit and SCRST bit must not be simultaneously set to 1. This bit must not be set to 1 while RTC is stopped (RUN=0).

[bit3] SRST: RTC reset bit

See Table 4-3 in chapter "RTC Count Block Reset Operation" for the register bits initialized by the RTC reset function.

Always 0 will be read at the time of read access in the read modify write access mode.

Bit	Description
0	When RTC reset is completed
1	The hardware will issue an RTC reset when 1 is written

[bit2] RUN: RTC count block operation bit

This bit indicates the operating state of the RTC count block.

If the ST is set to 0 while the RTC count block is in operation with ST=1, the RTC count block will come to a stop and the following condition will be established: RUN = 0.

Bit	Description
0	The RTC count block is not in operation
1	The RTC count block is in operation

[bit1] Reserved: Reserved bit

Always 0 is read.

Set 0 when writing data.

[bit0] ST: Start bit

This bit controls the operation start of the RTC count block.

Bit	Description
0	The RTC count block comes to a stop.
1	The set values in the year / month / date / hour / minute / second / day of the week registers are transferred to the year / month / date / hour / minute / second/day of the week counters, and the RTC count block will start operating.

7.2 Control Register 2 (WTCR 2)

This register controls the operations of the RTC count block.

bit	31							24
Field	Reserved							
Attribute	R							
Initial value	0x00							

bit	23							16
Field	Reserved							
Attribute	R							
Initial value	0x00							

bit	15	14	13	12	11	10	9	8
Field	Reserved					TMRUN	TMEN	TMST
Attribute	R					R	R/W	R/W
Initial value	00000					0	0	0

bit	7	6	5	4	3	2	1	0
Field	Reserved							CREAD
Attribute	R							R/W
Initial value	0000000							0

[bit31:11] Reserved: Reserved bits

Always 0 is read.

Set 0 when writing data.

[bit10] TMRUN: Timer counter operation bit

This bit indicates the operation of the timer counter.

While the time counter control bit is 0, this bit will be cleared by the hardware if the count underflows.

While the timer counter control bit(TMEN) is 1, this bit will be remain 1 until the timer counter start bit (TMST) becomes 0.

If TMST bit is set to 0 while the timer is in operation with the TMST bit set to 1, the timer will stop operating and the following condition will be established: TMRUN = 0.

Bit	Description
0	The timer counter is not in operation
1	The timer counter is in operation

[bit9] TMEN: Timer counter control bit

This bit selects the control of the timer counter operating with an elapse of the desired time (with the hours, minutes, and seconds specified) or the timer counter in the desired intervals (with the hours, minutes, and seconds specified).

Bit	Description
0	The timer counter will operate with an elapse of the desired time (with the hours, minutes, and seconds specified).
1	The timer counter will operate in intervals of the desired time (with the hours, minutes, and seconds specified).

[bit8] TMST: Time counter start bit

This bit starts the operation of the timer counter.
When the time counter control bit is 0, this bit will be 0 cleared by the hardware when the count completes. See the timer counter operation bit (TMRUN) for the operation state of the timer counter. In the case of rewriting the timer setting register, stop this bit once with 0 and rewrite the timer setting register, and reset the timer setting register to 1 to start the operation of the timer setting register.

Bit	Description
0	The timer counter stops operating.
1	The timer counter starts operating.

[bit7:1] Reserved: Reserved bits

Always 0 is read.
Set 0 when writing data.

[bit0] CREAD: Year/month/date/hour/minute/second/day of the week counter value read control bit

The values in the year / month / date / hour / minute / second / day of the week counters will be transferred to the year / month / date / hour / minute / second / day of the week registers if this bit is set to 1 and the bit will be 0 cleared on completion of the transfer.
Always 0 will be read at the time of the read access in the read modify write access mode.

Bit		Description
Read	0	Data transfer from the year / month / date / hour / minute / second / day of the week counters to the year / month / date / hour / minute / second / day of the week registers has been completed.
	1	Data transfer from the year / month / date / hour / minute / second / day of the week counters to the year / month / date / hour / minute / second / day of the week registers is in process.
Write	0	No effect on operation.
	1	Data copy from the year / month / date / hour / minute / second / day of the week counters to the year / month / date / hour / minute / second / day of the week registers starts.

7.3 Counter Cycle Setting Register (WTBR)

This register stores values to be reloaded to the sub-second generation counter (for date, time, and timer use).

bit	31							24
Field	Reserved							
Attribute	R							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	BR23	BR22	BR21	BR20	BR19	BR18	BR17	BR16
Attribute	RW	RW	RW	RW	RW	RW	RW	RW
Initial value	0	0	0	0	0	0	0	0

bit	15	14	13	12	11	10	9	8
Field	BR15	BR14	BR13	BR12	BR11	BR10	BR9	BR8
Attribute	RW	RW	RW	RW	RW	RW	RW	RW
Initial value	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Field	BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
Attribute	RW	RW	RW	RW	RW	RW	RW	RW
Initial value	0	0	0	0	0	0	0	0

[bit31:24] Reserved: Reserved bits

Always 0 is read.

Set 0 when writing data.

[bit23:0] BR23 to BR0: Counter cycle setting bits

These bits set values to be reloaded to the sub-second generation counter (for date, time, and timer use).

Set this register to a 0.5 second count value for the sub-second generation counter. The value will be reloaded when the sub-second generation counter value becomes 0.

Obtain the Counter Cycle Setting Register (WTBR) set value from the following formula:

WTBR = (0.5 [s] / (2 × RTCMCLK cycles [s])) – 1

Notes:

- *In the case of setting the WTBR register, make sure that the ST value is 0 (RTC count block is not in operation) and the TMST value is 0 (timer counter is not in operation).*
- *Set the counter cycle setting register to value of 7 or larger. If a value of 6 or less is set, the right value will not be read by the year / month / date / hour / minute / second / day of the week counter value read executed.*

7.4 Day Register (WTDR)

This register indicates the day information in the RTC count block. The register value is displayed in BCD.

bit	7	6	5	4	3	2	1	0
Field	Reserved		TD1	TD0	D3	D2	D1	D0
Attribute	R		R/W	R/W	R/W	R/W	R/W	R/W
Initial value	00		0	0	0	0	0	0

[bit7:6] Reserved: Reserved bits

Always 0 is read.

Set 0 when writing data.

[bit5:4] TD1, TD0: Day register

This register stores the second digit of the date information in the RTC count block.

[bit3:0] D3-D0: Day register

This register stores the first digit of the date information in the RTC count block.

0 to 9: Enabled

A to F: Setting disabled

7.5 Hour Register (WTHR)

This register indicates the hour information in the RTC count block. The register value is displayed in BCD.

bit	7	6	5	4	3	2	1	0
Field	Reserved		TH1	TH0	H3	H2	H1	H0
Attribute	R		R/W	R/W	R/W	R/W	R/W	R/W
Initial value	00		0	0	0	0	0	0

[bit7:6] Reserved: Reserved bits

Always 0 is read.

Set 0 when writing data.

[bit5:4] TH1, TH0: Hour register

This register stores the second digit of the hour information in the RTC count block.

0 to 2: Valid

3: Setting is prohibited

[bit3:0] H3-H0: Hour register

This register stores the first digit of the hour information in the RTC count block.

0 to 9: Enabled

A to F: Setting disabled

7.6 Minute Register (WTMIR)

This register indicates the minute information in the RTC count block. The register value is displayed in BCD.

bit	7	6	5	4	3	2	1	0
Field	Reserved	TMI2	TMI1	TMI0	MI3	MI2	MI1	MI0
Attribute	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7] Reserved: Reserved bit

Always 0 is read.

Set 0 when writing data.

[bit6:4] TMI2-TMI0: Minute register

This register stores the second digit of the minute information in the RTC count block.

0 to 5: Enabled

6, 7: Setting disabled

[bit3:0] MI3-MI0: Minute register

This register stores the first digit of the minute information in the RTC count block.

0 to 9: Enabled

A to F: Setting disabled

7.7 Second Register (WTSR)

This register indicates the second information in the RTC count block. The register value is displayed in BCD.

bit	7	6	5	4	3	2	1	0
Field	Reserved	TS2	TS1	TS0	S3	S2	S1	S0
Attribute	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7] Reserved: Reserved bit

Always 0 is read.

Set 0 when writing data.

[bit6:4] TS2-TS0: Second register

This register stores the second digit of the second information in the RTC count block.

0 to 5: Enabled

6, 7: Setting disabled

[bit3:0] S3-S0: Second register

This register stores the first digit of the second information in the RTC count block.

0 to 9: Enabled

A to F: Setting disabled

7.8 Year Register (WTYR)

This register indicates the year information in the RTC count block. The register value is displayed in BCD.

bit	7	6	5	4	3	2	1	0
Field	TY3	TY2	TY1	TY0	Y3	Y2	Y1	Y0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7:4] TY3-TY0: Year register

This register stores the second digit of the year information in the RTC count block.

0 to 9: Enabled
A to F: Setting disabled

[bit3:0] Y3-Y0: Year register

This register stores the first digit of the year information in the RTC count block.

0 to 9: Enabled
A to F: Setting disabled

7.9 Month Register (WTMOR)

This register indicates the month information in the RTC count block. The register value is displayed in BCD.

bit	7	6	5	4	3	2	1	0
Field	Reserved			TMO0	MO3	MO2	MO1	MO0
Attribute	R			R/W	R/W	R/W	R/W	R/W
Initial value	000			0	0	0	0	0

[bit7:5] Reserved: Reserved bits

Always 0 is read.

Set 0 when writing data.

[bit4] TMO0: Month register

This register stores the second digit in the month information in the RTC count block.

[bit3:0] MO3-MO0: Month register

This register stores the first digit of the month information in the RTC count block.

0 to 9: Enabled

A to F: Setting disabled

7.10 Day of the Week Register (WTDW)

This register indicates the day of the week information in the RTC count block. he register value is displayed in BCD.

bit	7	6	5	4	3	2	1	0
Field	Reserved					DW2	DW1	DW0
Attribute	R					R/W	R/W	R/W
Initial value	00000					0	0	0

[bit7:3] Reserved: Reserved bits

Always 0 is read.

Set 0 when writing data.

[bit2:0] DW2-DW0: Day of the week register

This register stores the day information in the RTC count block.

0: Sunday
1: Monday
2: Tuesday
3: Wednesday
4: Thursday
5: Friday
6: Saturday
7: Setting disabled

7.11 Alarm Day Register (ALDR)

This register indicates the alarm-set date information.

bit	7	6	5	4	3	2	1	0
Field	Reserved		TAD1	TAD0	AD3	AD2	AD1	AD0
Attribute	R		R/W	R/W	R/W	R/W	R/W	R/W
Initial value	00		0	0	0	0	0	0

[bit7:6] Reserved: Reserved bits

Always 0 is read.

Set 0 when writing data.

[bit5:4] TAD1, TAD0: Alarm day register

This register stores the second digit of the alarm-set date information.

[bit3:0] AD3-AD0: Alarm day register

This register stores the first digit of the alarm-set date information.

0 to 9: Enabled

A to F: Setting disabled

7.12 Alarm Hour Register (ALHR)

This register indicates the alarm-set hour information.

bit	7	6	5	4	3	2	1	0
Field	Reserved		TAH1	TAH0	AH3	AH2	AH1	AH0
Attribute	R		R/W	R/W	R/W	R/W	R/W	R/W
Initial value	00		0	0	0	0	0	0

[bit7:6] Reserved: Reserved bits

Always 0 is read.

Set 0 when writing data.

[bit5:4] TAH1, TAH0: Alarm hour register

This register stores the second digit of the alarm-set hour information.

0 to 2: Enabled

3: Setting disabled

[bit3:0] AH3-AH0: Alarm hour register

This register stores the first digit of the alarm-set hour information.

0 to 9: Enabled

A to F: Setting disabled

7.13 Alarm Minute Register (ALMIR)

This register indicates the alarm-set minute information.

bit	7	6	5	4	3	2	1	0
Field	Reserved	TAMI2	TAMI1	TAMI0	AMI3	AMI2	AMI1	AMI0
Attribute	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7] Reserved: Reserved bit

Always 0 is read.

[bit6:4] TAMI2-TAMI0: Alarm minute register

This register stores the second digit of the alarm-set minute information.

0 to 5: Enabled

6, 7: Setting disabled

[bit3:0] AMI3-AMI0: Alarm minute register

This register stores the first digit of the alarm-set minute information.

0 to 9: Enabled

A to F: Setting disabled

7.14 Alarm Year Register (ALYR)

This register indicates the alarm-set year information.

bit	7	6	5	4	3	2	1	0
Field	TAY3	TAY2	TAY1	TAY0	AY3	AY2	AY1	AY0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7:4] TAY3-TAY0: Alarm year register

This register stores the second digit of the alarm-set year information.

0 to 9: Enabled
A to F: Setting disabled

[bit3:0] AY3-AY0: Alarm year register

This register stores the first digit of the alarm-set year information.

0 to 9: Enabled
A to F: Setting disabled

7.15 Alarm Month Register (ALMOR)

This register indicates the alarm-set month information.

bit	7	6	5	4	3	2	1	0
Field	Reserved			TAMO0	AMO3	AMO2	AMO1	AMO0
Attribute	R			R/W	R/W	R/W	R/W	R/W
Initial value	000			0	0	0	0	0

[bit7:5] Reserved: Reserved bits

Always 0 is read.

Set 0 when writing data.

[bit4] TAMO0: Alarm month register

This register stores the second digit of the alarm-set month information.

[bit3:0] AMO3-AMO0: Alarm month register

This register stores the first digit of the alarm-set month information.

0 to 9: Enabled

A to F: Setting disabled

7.16 Time Setting Register (WTTR)

This register is used to set a timer set value that will be up with an elapse of the set value (hours, minutes, and seconds) or in intervals of the set value (hours, minutes, and seconds). A value ranging from 1 second up to 1 day can be set.

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	R							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved						TM17	TM16
Attribute	R						RW	RW
Initial value	000000						0	0

bit	15	14	13	12	11	10	9	8
Field	TM15	TM14	TM13	TM12	TM11	TM10	TM9	TM8
Attribute	RW	RW	RW	RW	RW	RW	RW	RW
Initial value	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Field	TM7	TM6	TM5	TM4	TM3	TM2	TM1	TM0
Attribute	RW	RW	RW	RW	RW	RW	RW	RW
Initial value	0	0	0	0	0	0	0	0

[bit31:18] Reserved: Reserved bits

Always 0 is read.

Set 0 when writing data.

[bit17:0] TM17 to TM0: Timer setting register

This register is a timer setting information bit.

This register is set to store a 1-day timer set value that will be up with an elapse of the set value (hours, minutes, and seconds) or in intervals of the set value (hours, minutes, and seconds).

The available timer value is from 1 second to 1 day at a 0.5 seconds intervals.

Obtain the set value for the timer setting register from the following formula:

TM [17:0] = (Time set[s] × 2) -1

1 to 172799 : Enabled

0, 172800 to 262143: Setting disabled

8. Usage Precautions

Note the following when using the RTC count block.

- Use under the following frequency condition: PCLK ≥ RTCCLK / 2
- Change settings for each alarm register when any of the alarm interrupt data control bits (WTCR1:YEN, WTCR1:MOEN, WTCR1:DEN, WTCR1:HEN, WTCR1:MIEN) is 0
- An interrupt may occur immediately after any of the alarm interrupt data control bits (WTCR1:YEN, WTCR1:MOEN, WTCR1:DEN, WTCR1:HEN, and WTCR1:MIEN) is set to 1. After the interrupt, confirm that the value of Year / Month / Date / Hour / Minute counter by reading them.

CHAPTER 4-5: RTC Clock Control Block (A)

This chapter explains the functions and operations of the RTC clock control block(A).

1. Overview of the RTC Clock Control Block
2. Configuration of the RTC Clock Control Block
3. Operations of the RTC Clock Control Block
4. Setting Procedures of the RTC Clock Control Block
5. Registers of the RTC Clock Control Block

1. Overview of the RTC Clock Control Block

This chapter shows the overview of the functions of the RTC clock control block.

RTC Clock Control Block

The RTC clock control block has the following functions:

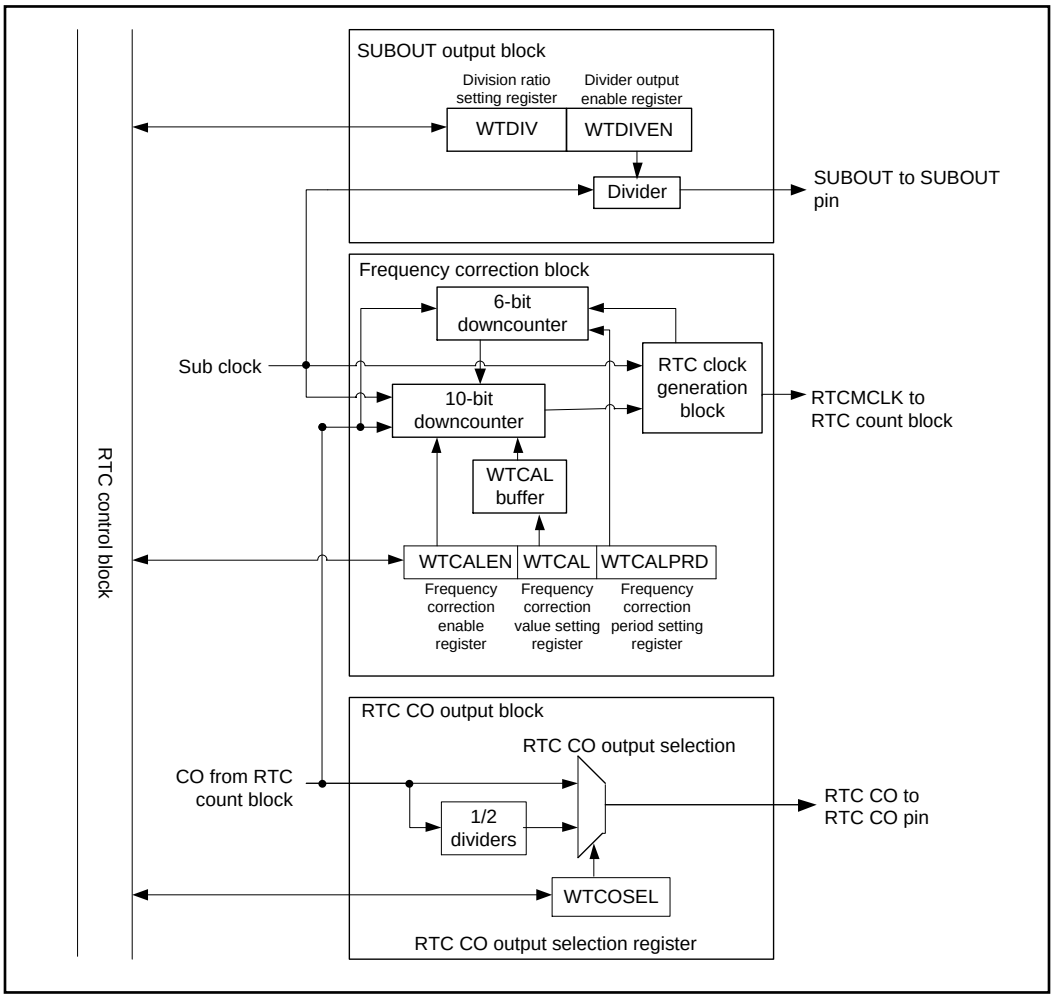
- Generation of the RTC clock (RTCMCLK) to be used in the RTC count block.
- Generation of the division clock to be output to the SUBOUT external pin.
- Generation of 0.5 second pulse or 1 second pulse to be output to the RTCCO external pin.
- Correction of fluctuation in input clock (sub clock) frequency due to temperature (frequency correction function).
  (The frequency correction function supposes that a temperature sensor is connected to the RTC clock control block externally.)

2. Configuration of the RTC Clock Control Block

This section shows the block diagram of the RTC clock control block.

Block Diagram of RTC Clock Control Block

Figure 2-1 Block Diagram of the RTC Clock Control Block



- Frequency correction block

  The frequency correction block masks the sub clock and outputs the RTCMCLK whose frequency has been corrected.

  The frequency correction block masks the sub clock for the number of clocks set in the WTCAL buffer every cycle set in the WTCALPRD Register.

- SUBOUT output block

  The SUBOUT output block generates the division clock to be output to the SUBOUT external pin. In deep standby RTC mode, no division clock can be output from the SUBOUT external pin.

- RTCCO output block

  The RTCCO output block generates the signal to be output to the RTCCO external pin. The signal to be output to the RTCCO external pin can be selected between the CO signal from the RTC count block and a signal generated by dividing the CO signal by 2. In deep standby RTC mode, the signal cannot be output from the RTCCO external pin.

3. Operations of the RTC Clock Control Block

This section explains the operations of the RTC clock control block.

Frequency Correction Block

The frequency correction block corrects the frequency lag in the sub clock.

The frequency correction block masks the sub clock for a certain period and outputs the RTCMCLK whose frequency has been corrected.

The period can be set in the Frequency Correction Period Setting Register (WTCALPRD).

The number of clocks to be masked can be set in the Frequency Correction Value Setting Register (WTCAL).

Figure 3-1 **Examples of Operations of Frequency Correction Block (WTCALPRD=19)**

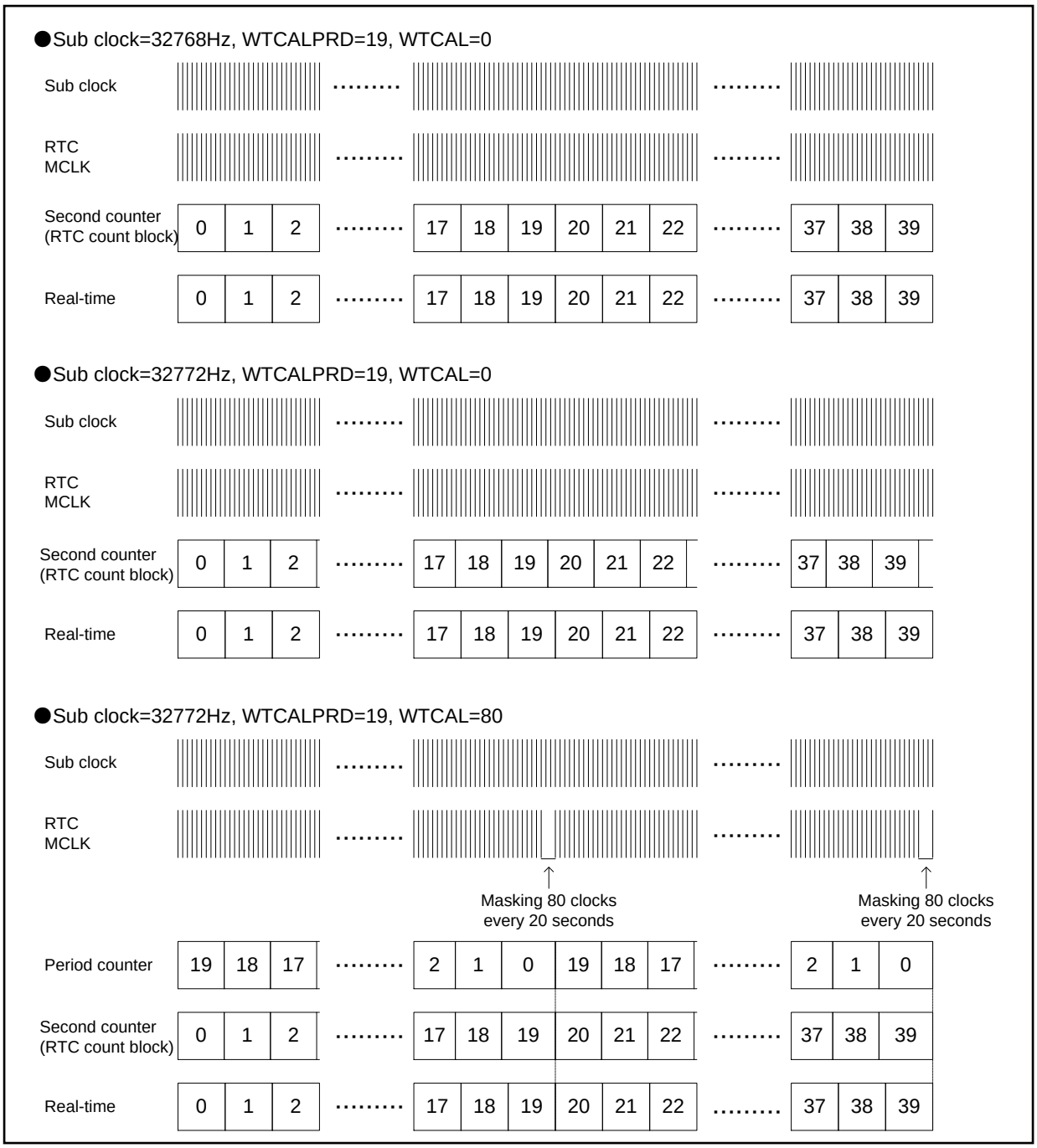
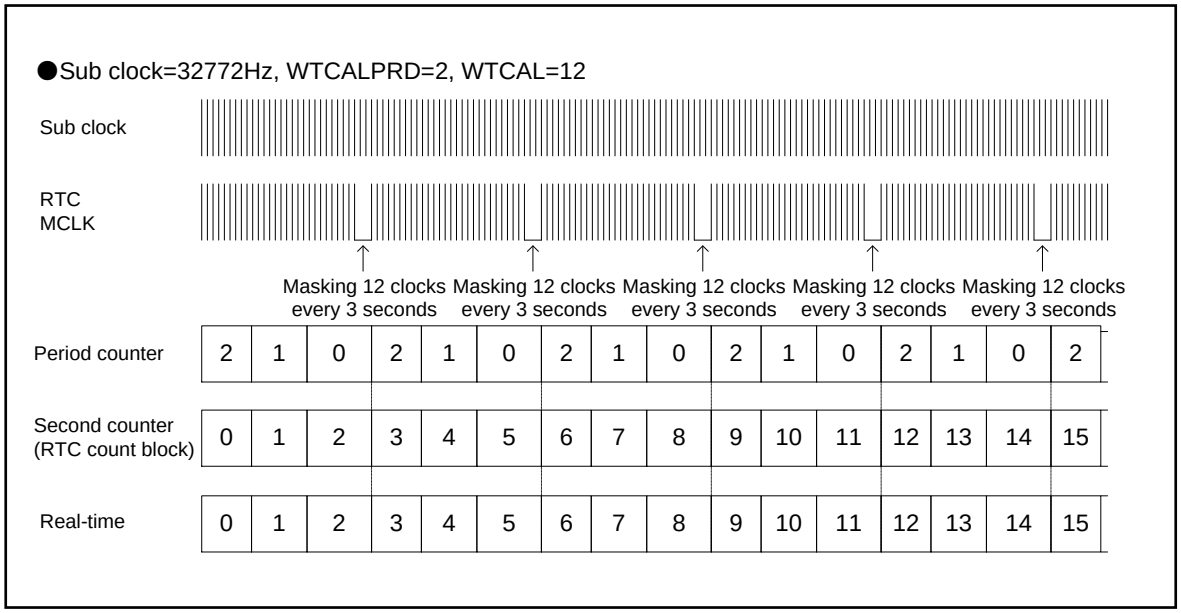


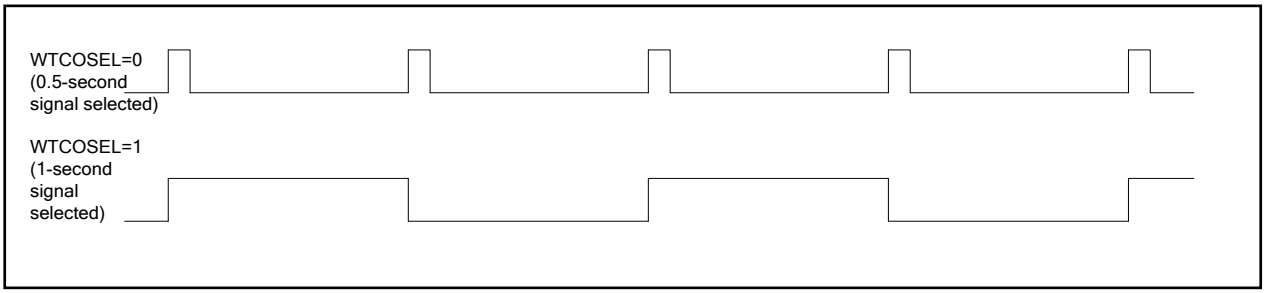
Figure 3-2 Examples of Operations of Frequency Correction Block (WTCALPRD=2)



RTCCO External Pin Output Clock Selection Block

The RTCCO external pin output clock selection block selects, according to the setting of the RTCCO Output Selection Register (WTCOSEL) either the CO signal (0.5 second) or the signal (1 second) generated by dividing the CO signal by 2, and outputs the selected signal to the RTCCO external pin.

Figure 3-3 Examples of Operations of Frequency Correction Block



Note:

- *When the clock set by the correction value setting register (WTCAL) is masked, the CO output cycle is extended for the masked amount.*
  For the CO signal (0.5 sec) from the RTC count block, see the chapter RTC Count Block.

■ Frequency correction range

Table 3-1 and Table 3-2 show the examples of the frequency correction range. The frequency correction block corrects a frequency according to a combination of settings of the WTCAL Register and WTCALPRD Register.

Table 3-1 Example of Frequency Correction Range with WTCALPRD = 19 (Target Frequency is 32768 Hz)

Sub Clock Frequency before Correction[Hz]	WTCAL	Correction Rate [ppm]
32768.00	0	0.0
32768.05	1	-1.53
:	:	:
32769.95	39	-59.51
32770.00	40	-61.0
32770.05	41	-62.6
:	:	:
32771.90	78	-119.0
32771.95	79	-120.5
32772.00	80	-122.1

Table 3-2 Example of Frequency Correction Range with WTCALPRD = 59 (Target Frequency is 32768 Hz)

Sub Clock Frequency before Correction[Hz]	WTCAL	Correction Rate [ppm]
32768.00	0	0.0
32768.02	1	-0.51
:	:	:
32771.98	239	-121.6
32772.00	240	-122.1
32772.02	241	-122.6
:	:	:
32779.97	718	-365.1
32779.98	719	-365.6
32780.00	720	-366.1

4. Setting Procedures of the RTC Clock Control Block

This section explains the setting procedures of the RTC clock control block.

Setting Procedures of Frequency Correction

1. Write the correction period to the Frequency Correction Period Setting Buffer (WTCALPRD) and the correction value to the Frequency Correction Value Setting Buffer (WTCAL).
   Find out the setting of WTCAL with the following formula.
   WTCAL = {(Frequency before correction – ideal Frequency) / ideal Frequency} ×32768×(WTCALPRD + 1)
2. Write 1 to the Frequency Correction Enable Buffer (WTCALEN) to enable frequency correction.
3. Set the VB_CLKDIV Register to a value that makes the frequency of the transfer clock become 1 MHz or below. For details of the VB_CLKDIV Register, see VB_CLKDIV Register in chapter VBAT Domain in Peripheral Manual.
4. Write 1 to the PWRITE bit in the WTCR20 Register.
5. Check that the value of the TRANS bit in the WTCR10 Register or that of the PWRITE bit in the WTCR20 Register has become “0”.

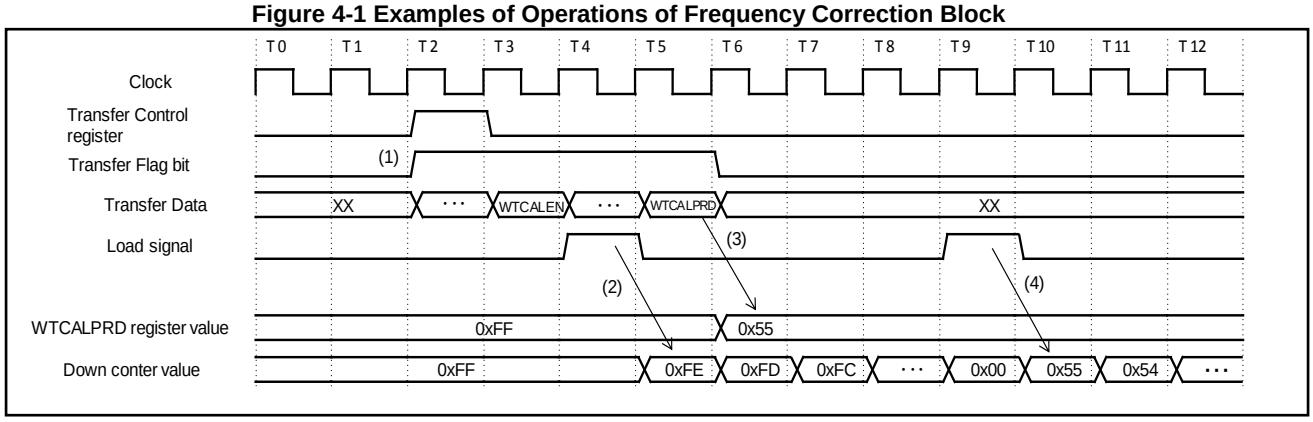
Procedure for Changing Settings during the Operation of the Frequency Correction Function

1. Check to make sure that the transfer flag bit (TRANS) of control register 10 (WTCR10) is 0.
2. Write a correction cycle to the frequency correction cycle setting buffer (WTCALPRD), and a correction value to the frequency correction value setting buffer (WTCAL).
3. Set the transfer clock division setting register (VB_CLKDIV) (for details, see the VB_CLKDIV Register in chapter VBAT Domain of the Peripheral Manual) so that the transfer clock is set to 1 MHz or less.
4. Set a 0.5 sec interrupt. For details, see Every 0.5 sec, Every-second, Every-minute and Every-hour Interrupt Setting Operation Flow in chapter RTC Count Block of the Peripheral Manual.
5. Set the VBAT PORT save operation control bit (PWRITE) of control register 20 (WTCR20) to 1 during the period from the occurrence of an every 0.5 sec interrupt to the occurrence of the next every 0.5 sec interrupt.
6. Check to make sure that the transfer flag bit (TRANS) of control register 10 (WTCR10) is set to “0”.

The timing of reflecting the setting value varies depending on the number of transfers, and whether the frequency correction cycle buffer (WTCALPRD) is changed and the frequency correction is enabled in a single transfer or two separate transfers.

Figure 4-1 shows the timing chart for the case in which the frequency correction is set in a single transfer.

Figure 4-1 Examples of Operations of Frequency Correction Block



(1) Write 1 to the frequency correction register (WTCALEN), set a correction cycle in the frequency correction cycle setting register (WTCALPRD), and then write 1 to the VBAT PORT control bit (PWRITE) of control register 20 (WTCR20).

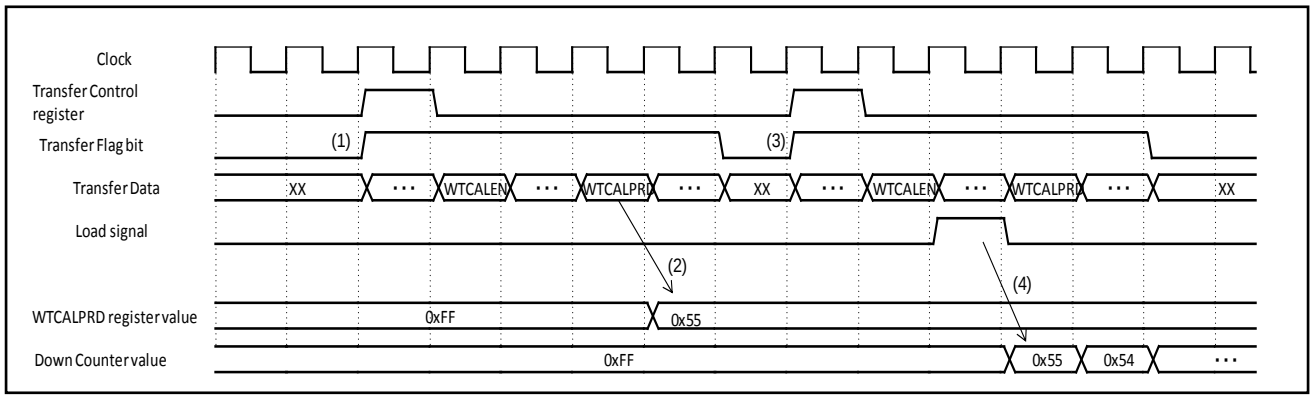
(2) The down counter starts to operate when the value is reflected in the frequency correction register (WTCALEN) of the VBAT domain. The count starts from the down counter value that was present before its reflection in the frequency correction cycle setting register (WTCALPRD).

(3) The value of the frequency correction cycle setting register (WTCALPRD) is reflected in the VBAT domain.

(4) The down counter value underflows, the setting value of the frequency correction cycle setting register (WTCALPRD) is reflected in the down counter, and the down count starts.

Figure 4-2 shows the timing chart for the case in which the frequency correction is set in two separate transfers.

Figure 4-2 Timing Chart for Case in which Frequency Correction is Set in Two Separate Transfers



(1) Write 0 to the frequency correction register (WTCALEN), set a correction cycle in the frequency correction cycle setting register (WTCALPRD), and then write 1 to the VBAT PORT control bit (PWRITE) of control register 20 (WTCR20).

(2) The value of the frequency correction cycle setting register (WTCALPRD) is reflected in the VBAT domain.

(3) Write 1 to the frequency correction register (WTCALEN), and then write 1 to the VBAT PORT control bit (PWRITE) of control register 20 (WTCR20).

(4) The down counter starts to operate when the value is reflected in the frequency correction register (WTCALEN) of the VBAT domain.

Note:

- *When the clock set by the correction value setting register (WTCAL) is masked, the CO output cycle is extended for the masked amount.*

Setting procedures of SUBOUT output block

1. Write 0 to the divider output enable bit (WTDIVEN). The divider stops and the SUBOUT external output outputs the L level.
2. Read the divider state bit (WTDIVRDY) and wait for the value of that bit to become 0.
3. Write the division ratio to the division ratio setting bit (WTDIV).
   See 5.4. Division Ratio Setting Register (WTDIV) for the division ratio setting.
4. Write 1 to the divider output enable bit (WTDIVEN) to enable the operation of the divider.
5. Set the VB_CLKDIV Register to a value that makes the frequency of the transfer clock become 1 MHz or below. For details of the VB_CLKDIV Register, see 6.1. VB_CLKDIV Register in chapter VBAT Domain in Peripheral Manual.
6. Write 1 to the PWRITE bit in the WTCR20 Register.
7. Check that the value of the TRANS bit in the WTCR10 Register has become 0.

5. Registers of the RTC Clock Control Block

This section shows the list of registers of the RTC clock control block.

Table 5-1 List of Registers of the RTC Clock Control Block

Abbreviation	Register Name	Reference
WTCAL0	Frequency Correction Value Setting Register 0	0
WTCAL1	Frequency Correction Value Setting Register 1	5.2
WTCALEN	Frequency Correction Enable Register	5.3
WTDIV	Division Ratio Setting Register	5.4
WTDIVEN	Divider Output Enable Register	5.5
WTCALPRD	Frequency Correction Period Setting Register	5.6
WTCOSEL	RTCCO Output Selection Register	5.7

The registers shown in Table 5-1 correspond to Circuit Type 3 in chapter VBAT Domain. For that reason, a system reset and RTC reset do not initialize the registers in the VBAT domain. They do, however, initialize the buffers in the Always ON domain. After a reset, therefore, the save operation must be performed after the value is set again or the recall operation is performed.

5.1 Frequency Correction Value Setting Register 0 (WTCAL0)

The Frequency Correction Value Setting Register 0 (WTCAL0) sets the frequency correction value of the RTC clock (RTCMCLK) to be output to the RTC count block.

Bit	7	0
Field	WTCAL0	
Attribute	R/W	
Initial value	00000000	

[bit7:0] WTCAL0: Frequency correction value setting bits 0

These bits set the number of clocks to be masked for the period set in the WTCALPRD register.

If the WTCALPRD register is set to 19, the WTCAL to 8, the input clock (sub clock) is masked for 8 clocks every 20 seconds and the RTCMCLK is output to the RTC count block.

For values set in WTCAL, see Setting procedure of frequency correction in Setting Procedures of the RTC Clock Control Block.

5.2 Frequency Correction Value Setting Register 1 (WTCAL1)

The Frequency Correction Value Setting Register 1 (WTCAL1) the frequency correction value of the RTC clock to be output to the RTC count block.

Bit	7	2	1	0
Field	Reserved		WTCAL1	
Attribute	R		R/W	
Initial value	000000		00	

[bit7:2] Reserved: Reserved bits

The read value is always 0.

Write 0 to a reserved bit in a write access to it.

[bit1:0] WTCAL1: Frequency correction value setting bits 1

These bits set the number of clocks to be masked for the period set in the WTCALPRD register.

If the WTCALPRD register is set to 19, the WTCAL to 8, the input clock (sub clock) is masked for 8 clocks every 20 seconds and the RTCMCLK is output to the RTC count block.

For values set in the WTCAL, see Setting procedure of frequency correction in Setting Procedures of the RTC Clock Control Block.

5.3 Frequency Correction Enable Register (WTCALEN)

The Frequency Correction Enable Register (WTCALEN) enables correcting the frequency of the RTC clock (RTCMCLK) to be input to the RTC count block.

Bit	7	1	0
Field	Reserved		WTCALEN
Attribute	R		R/W
Initial value	0000000		0

[bit7:1] Reserved: Reserved bits

The read value is always 0.

Write 0 to a reserved bit in a write access to it.

[bit0] WTCALEN: Frequency correction value setting bit

This bit enables frequency correction.

Bit	Description
0	Disables the frequency correction
1	Enables frequency correction.

5.4 Division Ratio Setting Register (WTDIV)

The Division Ratio Setting Register (WTDIV) sets the division ratio of the divider.

Bit	7	6	5	4	3	2	1	0
Field	Reserved				WTDIV			
Attribute	R				R/W			
Initial value	0	0	0	0	0	0	0	0

[bit7:4] Reserved: Reserved bits

The read value is always 0.
Write 0 to a reserved bit in a write access to it.

[bit3:0] WTDIV: Division ration setting bits

These bits set the division ratio for the input clock and the division clock (SUBOUT) that the divider outputs.

Bit3:0	Description
0000	No division
0001	Division ratio: 1/2
0010	Division ratio: 1/4
0011	Division ratio: 1/8
0100	Division ratio: 1/16
0101	Division ratio: 1/32
0110	Division ratio: 1/64
0111	Division ratio: 1/128
1000	Division ratio: 1/256
1001	Division ratio: 1/512
1010	Division ratio: 1/1024
1011	Division ratio: 1/2048
1100	Division ratio: 1/4096
1101	Division ratio: 1/8192
1110	Division ratio: 1/16384
1111	Division ratio: 1/32768

Note:

- *Before writing a value to the WTDIV bits, ensure that the divider enable bit (WTDIVEN) in the Divider Output Enable register (WTDIVEN) is 0.*

5.5 Divider Output Enable Register (WTDIVEN)

The Divider Output Enable Register (WTDIVEN) enables the output of divider.

Bit	7	2	1	0
Field	Reserved		WTDIVRDY	WTDIVEN
Attribute	R		R	R/W
Initial value	000000		0	0

[bit7:2] Reserved: Reserved bits

The read value is always 0.

Write 0 to a reserved bit in a write access to it.

[bit1] WTDIVRDY: Divider state bit

This bit shows the state of the divider.

Bit	Description
0	The divider has stopped operating. The SUBOUT external pin output is fixed at “Low”.
1	The divider is operating.

[bit0] WTDIVEN: Divider enable bit

This bit enables the operation of the divider.

Bit	Description
0	Stops the operation of the divider.
1	Enables the operation of the divider.

5.6 Frequency Correction Period Setting Register (WTCALPRD)

The Frequency Correction Period Setting Register (WTCALPRD) sets the period for frequency correction.

Bit	7	6	5	0
Field	Reserved		WTCALPRD	
Attribute	R		R/W	
Initial value	00		010011	

[bit7:6] Reserved: Reserved bits

The read value is always 0.

Write 0 to a reserved bit in a write access to it.

[bit5:0] WTCALPRD: Frequency correction value setting bits

Set these bits to a value that is the remainder of subtracting 1 from the period (in seconds) of masking the clock for frequency correction.

For instance, if these bits are set to 0, the period becomes 1 second long; if these bits are set to 19, the period becomes 20 seconds long.

5.7 RTCCO Output Selection Register (WTCOSEL)

The RTCCO Output Selection Register (WTCOSEL) selects the RTCCO output.

Bit	7	1	0
Field	Reserved		WTCOSEL
Attribute	R		R/W
Initial value	0000000		0

[bit7:1] Reserved: Reserved bits

The read value is always 0.

Write 0 to a reserved bit in a write access to it.

[bit0] WTCOSEL: RTCCO output selection bit

This bit selects the RTCCO output.

Bit	Description
0	The RTCCO output block outputs the CO signal of the RTC count block to the RTCCO external pin.
1	The RTC count block outputs a signal generated by dividing the CO signal by 2 to the RTCCO external pin.

CHAPTER 4-6: RTC Clock Control Block(B)

This chapter explains the functions and operations of the RTC clock control block(B).

1. Overview of the RTC Clock Control Block
2. Configuration of the RTC Clock Control Block
3. Operations of the RTC Clock Control Block
4. Setting Procedures of the RTC Clock Control Block
5. Registers of the RTC Clock Control Block

1. Overview of the RTC Clock Control Block

This chapter shows the overview of the functions of the RTC clock control block.

RTC Clock Control Block

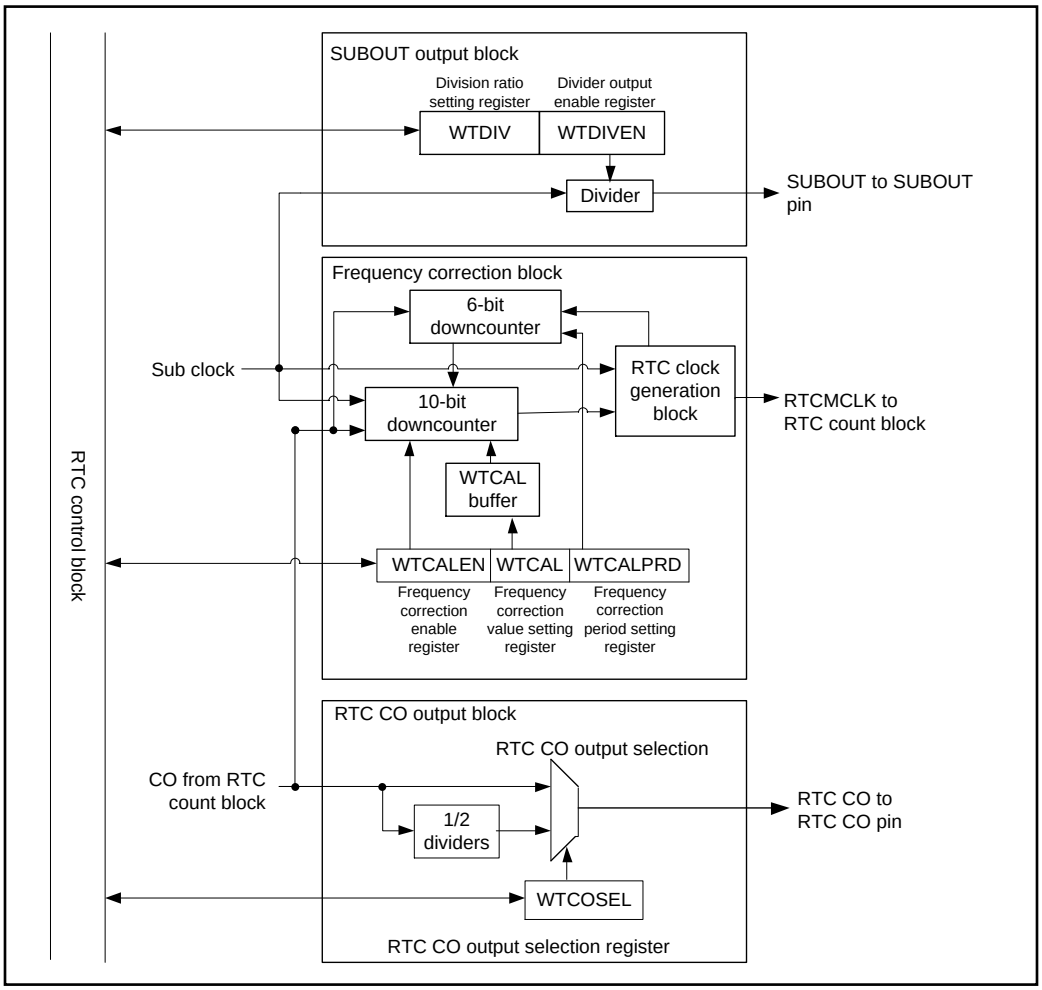
The RTC clock control block has the following functions:

- Generation of the RTC clock (RTCMCLK) to be used in the RTC count block.
- Generation of the division clock to be output to the SUBOUT external pin.
- Generation of 0.5 second pulse or 1 second pulse to be output to the RTCCO external pin.
- Correction of fluctuation in input clock (sub clock) frequency due to temperature (frequency correction function).
  (The frequency correction function supposes that a temperature sensor is connected to the RTC clock control block externally.)

2. Configuration of the RTC Clock Control Block

This section shows the block diagram of the RTC clock control block.

Figure 2-1 Block Diagram of the RTC Clock Control Block



- Frequency correction block

  The frequency correction block masks the sub clock and outputs the RTCMCLK whose frequency has been corrected.

  The frequency correction block masks the sub clock for the number of clocks set in the WTCAL buffer every cycle set in the WTCALPRD register.

- SUBOUT output block

  The SUBOUT output block generates the division clock to be output to the SUBOUT external pin. In deep standby RTC mode, no division clock can be output from the SUBOUT external pin.

- RTCCO output block

  The RTCCO output block generates the signal to be output to the RTCCO external pin. The signal to be output to the RTCCO external pin can be selected between the CO signal from the RTC count block and a signal generated by dividing the CO signal by 2. In deep standby RTC mode, the signal cannot be output from the RTCCO external pin.

3. Operations of the RTC Clock Control Block

This section explains the operations of the RTC clock control block.

Frequency Correction Block

The frequency correction block corrects the frequency lag in the sub clock.

The frequency correction block masks the sub clock for a certain period and outputs the RTCMCLK whose frequency has been corrected.

The period can be set in the Frequency Correction Period Setting register (WTCALPRD).

The number of clocks to be masked can be set in the Frequency Correction Value Setting register (WTCAL).

Figure 3-1 Examples of Operations of Frequency Correction Block (WTCALPRD=19)

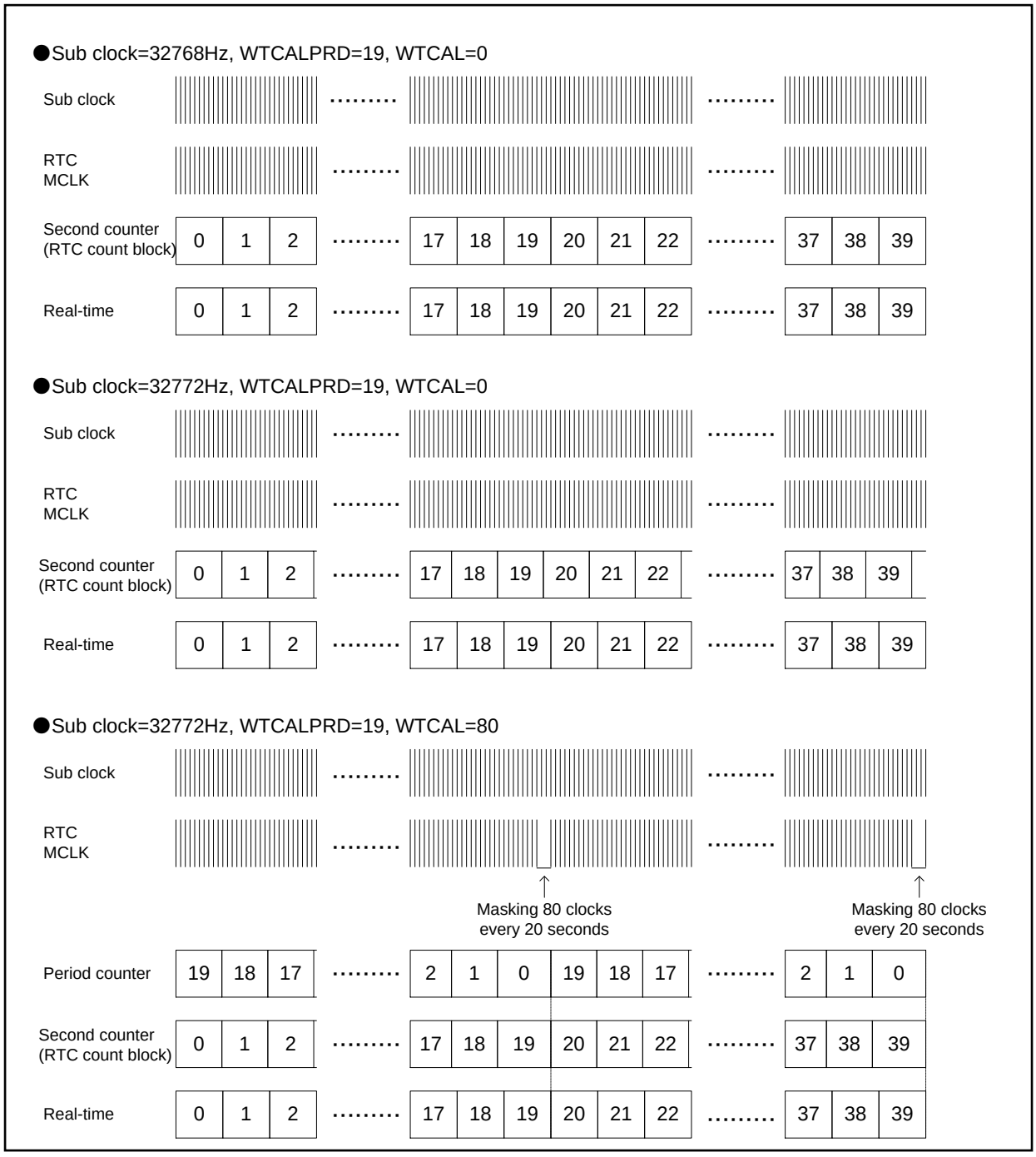
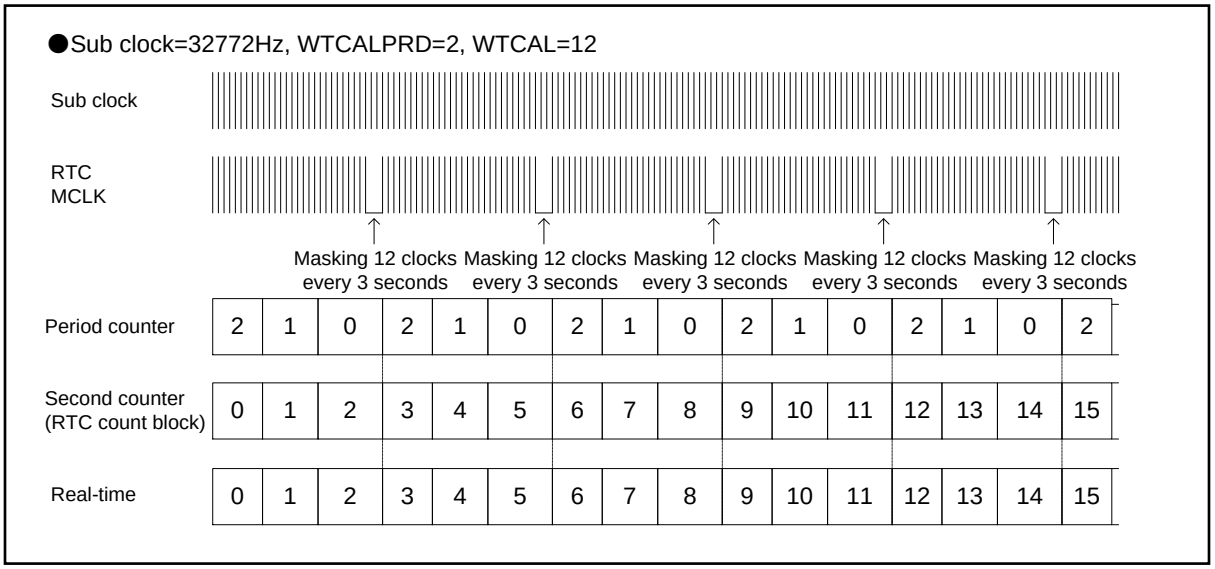


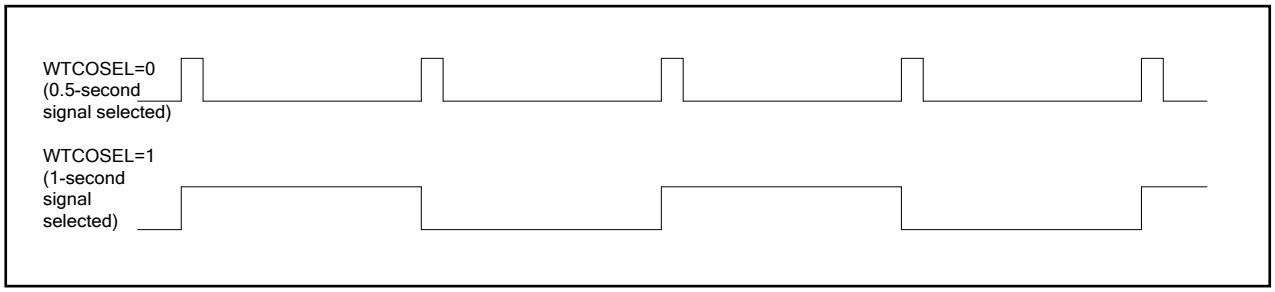
Figure 3-2 Examples of Operations of Frequency Correction Block (WTCALPRD=2)



RTCCO External Pin Output Clock Selection Block

The RTCCO external pin output clock selection block selects, according to the setting of the RTCCO Output Selection Register (WTCOSEL) either the CO signal (0.5 second) or the signal (1 second) generated by dividing the CO signal by 2, and outputs the selected signal to the RTCCO external pin.

Figure 3-3 Examples of Operations of Frequency Correction Block



Note:

- *When the clock set by the correction value setting register (WTCAL) is masked, the CO output cycle is extended for the masked amount.*
  For the CO signal (0.5 sec) from the RTC count block, see the chapter RTC Count Block.

■ Frequency correction range

Table 3-1 and Table 3-2 show the examples of the frequency correction range. The frequency correction block corrects a frequency according to a combination of settings of the WTCAL Register and WTCALPRD register.

Table 3-1 Example of Frequency Correction Range with WTCALPRD = 19 (Target Frequency is 32768 Hz)

Sub Clock Frequency before Correction[Hz]	WTCAL	Correction Rate [ppm]
32768.00	0	0.0
32768.05	1	-1.53
:	:	:
32769.95	39	-59.51
32770.00	40	-61.0
32770.05	41	-62.6
:	:	:
32771.90	78	-119.0
32771.95	79	-120.5
32772.00	80	-122.1

Table 3-2 Example of Frequency Correction Range with WTCALPRD = 59 (Target Frequency is 32768 Hz)

Sub Clock Frequency before Correction[Hz]	WTCAL	Correction Rate [ppm]
32768.00	0	0.0
32768.02	1	-0.51
:	:	:
32771.98	239	-121.6
32772.00	240	-122.1
32772.02	241	-122.6
:	:	:
32779.97	718	-365.1
32779.98	719	-365.6
32780.00	720	-366.1

4. Setting Procedures of the RTC Clock Control Block

This section explains the setting procedures of the RTC clock control block.

Setting Procedures of Frequency Correction

1. Write the correction period to the Frequency Correction Period Setting Buffer (WTCALPRD) and the correction value to the Frequency Correction Value Setting Buffer (WTCAL).
   Find out the setting of WTCAL with the following formula.
   WTCAL = {(Frequency before correction – ideal Frequency) / ideal Frequency} ×32768×(WTCALPRD + 1)
2. Write 1 to the Frequency Correction Enable Buffer (WTCALEN) to enable frequency correction.
3. Set the VB_CLKDIV register to a value that makes the frequency of the transfer clock become 1 MHz or below. For details of the VB_CLKDIV Register, see VB_CLKDIV register in chapter VBAT Domain in Peripheral Manual.
4. Write 1 to the PWRITE bit in the WTCR20 register.
5. Check that the value of the TRANS bit in the WTCR10 Register or that of the PWRITE bit in the WTCR20 register has become 0.

Procedure for Changing Settings during the Operation of the Frequency Correction Function

1. Check to make sure that the transfer flag bit (TRANS) of control register 10 (WTCR10) is 0.
2. Write a correction cycle to the frequency correction cycle setting buffer (WTCALPRD), and a correction value to the frequency correction value setting buffer (WTCAL).
3. Set the transfer clock division setting register (VB_CLKDIV) (for details, see VB_CLKDIV register in chapter VBAT Domain of the Peripheral Manual) so that the transfer clock is set to 1 MHz or less.
4. Set a 0.5 sec interrupt. For details, see Every-0.5 sec, Every-second, Every-minute and Every-hour Interrupt Setting Operation Flow in chapter RTC Count Block of the Peripheral Manual.
5. Set the VBAT PORT save operation control bit (PWRITE) of control register 20 (WTCR20) to 1 during the period from the occurrence of an every-0.5 sec interrupt to the occurrence of the next every-0.5-sec interrupt.
6. Check to make sure that the transfer flag bit (TRANS) of control register 10 (WTCR10) is set to 0.

Setting Procedures of SUBOUT Output Block

1. Write 0 to the divider output enable bit (WTDIVEN). The divider stops and the SUBOUT external output outputs the L level.
2. Read the divider state bit (WTDIVRDY) and wait for the value of that bit to become 0.
3. Write the division ratio to the division ratio setting bit (WTDIV).
   See 5.4. Division Ratio Setting Register (WTDIV) for the division ratio setting.
4. Write 1 to the divider output enable bit (WTDIVEN) to enable the operation of the divider.

5. Registers of the RTC Clock Control Block

This section shows the list of registers of the RTC clock control block.

Table 5-1 List of Registers of the RTC Clock Control Block

Abbreviation	Register Name	Reference
WTCAL0	Frequency Correction Value Setting Register 0	0
WTCAL1	Frequency Correction Value Setting Register 1	5.2
WTCALEN	Frequency Correction Enable Register	5.3
WTDIV	Division Ratio Setting Register	5.4
WTDIVEN	Divider Output Enable Register	5.5
WTCALPRD	Frequency Correction Period Setting Register	5.6
WTCOSEL	RTCCO Output Selection Register	5.7

The registers except WTDIV and WTDIVEN shown in Table 5-1 correspond to Circuit Type 3 in chapter VBAT Domain. For that reason, a system reset and RTC reset do not initialize the registers in the VBAT domain. They do, however, initialize the buffers in the Always ON domain. After a reset, therefore, the save operation must be performed after the value is set again or the recall operation is performed.

5.1 Frequency Correction Value Setting Register 0 (WTCAL0)

The Frequency Correction Value Setting Register 0 (WTCAL0) sets the frequency correction value of the RTC clock (RTCMCLK) to be output to the RTC count block.

Bit	7	0
Field	WTCAL0	
Attribute	R/W	
Initial value	00000000	

[bit7:0] WTCAL0: Frequency correction value setting bits 0

These bits set the number of clocks to be masked for the period set in the WTCALPRD Register.

If the WTCALPRD Register is set to 19, the WTCAL to 8, the input clock (sub clock) is masked for 8 clocks every 20 seconds and the RTCMCLK is output to the RTC count block.

For values set in the WTCAL, see Setting procedure of frequency correction in Setting Procedures of the RTC Clock Control Block.

5.2 Frequency Correction Value Setting Register 1 (WTCAL1)

The Frequency Correction Value Setting Register 1 (WTCAL1) the frequency correction value of the RTC clock to be output to the RTC count block.

Bit	7	2	1	0
Field	Reserved		WTCAL1	
Attribute	R		R/W	
Initial value	000000		00	

[bit7:2] Reserved: Reserved bits

The read value is always 0.

Write 0 to a reserved bit in a write access to it.

[bit1:0] WTCAL1: Frequency correction value setting bits 1

These bits set the number of clocks to be masked for the period set in the WTCALPRD register.

If the WTCALPRD register is set to 19, the WTCAL to 8, the input clock (sub clock) is masked for 8 clocks every 20 seconds and the RTCMCLK is output to the RTC count block.

For values set in WTCAL, see Setting procedure of frequency correction in Setting Procedures of the RTC Clock Control Block.

5.3 Frequency Correction Enable Register (WTCALEN)

The Frequency Correction Enable Register (WTCALEN) enables correcting the frequency of the RTC clock (RTCMCLK) to be input to the RTC count block.

Bit	7	1	0
Field	Reserved		WTCALEN
Attribute	R		R/W
Initial value	0000000		0

[bit7:1] Reserved: Reserved bits

The read value is always 0.

Write 0 to a reserved bit in a write access to it.

[bit0] WTCALEN: Frequency correction value setting bit

This bit enables frequency correction.

Bit	Description
0	Disables the frequency correction
1	Enables frequency correction.

5.4 Division Ratio Setting Register (WTDIV)

The Division Ratio Setting register (WTDIV) sets the division ratio of the divider.

Bit	7	6	5	4	3	2	1	0
Field	Reserved				WTDIV			
Attribute	R				R/W			
Initial value	0	0	0	0	0	0	0	0

[bit7:4] Reserved: Reserved bits

The read value is always 0.

Write 0 to a reserved bit in a write access to it.

[bit3:0] WTDIV: Division ration setting bits

These bits set the division ratio for the input clock and the division clock (SUBOUT) that the divider outputs.

Bit3:0	Description
0000	No division
0001	Division ratio: 1/2
0010	Division ratio: 1/4
0011	Division ratio: 1/8
0100	Division ratio: 1/16
0101	Division ratio: 1/32
0110	Division ratio: 1/64
0111	Division ratio: 1/128
1000	Division ratio: 1/256
1001	Division ratio: 1/512
1010	Division ratio: 1/1024
1011	Division ratio: 1/2048
1100	Division ratio: 1/4096
1101	Division ratio: 1/8192
1110	Division ratio: 1/16384
1111	Division ratio: 1/32768

Note:

- *Before writing a value to the WTDIV bits, ensure that the divider enable bit (WTDIVEN) in the Divider Output Enable register (WTDIVEN) is 0.*

5.5 Divider Output Enable Register (WTDIVEN)

The Divider Output Enable register (WTDIVEN) enables the output of divider.

Bit	7	2	1	0
Field	Reserved		WTDIVRDY	WTDIVEN
Attribute	R		R	R/W
Initial value	000000		0	0

[bit7:2] Reserved: Reserved bits

The read value is always 0.

Write 0 to a reserved bit in a write access to it.

[bit1] WTDIVRDY: Divider state bit

This bit shows the state of the divider.

Bit	Description
0	The divider has stopped operating. The SUBOUT external pin output is fixed at Low.
1	The divider is operating.

[bit0] WTDIVEN: Divider enable bit

This bit enables the operation of the divider.

Bit	Description
0	Stops the operation of the divider.
1	Enables the operation of the divider.

5.6 Frequency Correction Period Setting Register (WTCALPRD)

The Frequency Correction Period Setting register (WTCALPRD) sets the period for frequency correction.

Bit	7	6	5	0
Field	Reserved		WTCALPRD	
Attribute	R		R/W	
Initial value	00		010011	

[bit7:6] Reserved: Reserved bits

The read value is always 0.

Write 0 to a reserved bit in a write access to it.

[bit5:0] WTCALPRD: Frequency correction value setting bits

Set these bits to a value that is the remainder of subtracting 1 from the period (in seconds) of masking the clock for frequency correction.

For instance, if these bits are set to 0, the period becomes 1 second long; if these bits are set to 19, the period becomes 20 seconds long.

5.7 RTCCO Output Selection Register (WTCOSEL)

The RTCCO Output Selection register (WTCOSEL) selects the RTCCO output.

Bit	7	1	0
Field	Reserved		WTCOSEL
Attribute	R		R/W
Initial value	0000000		0

[bit7:1] Reserved: Reserved bits

The read value is always 0.

Write 0 to a reserved bit in a write access to it.

[bit0] WTCOSEL: RTCCO output selection bit

This bit selects the RTCCO output.

Bit	Description
0	The RTCCO output block outputs the CO signal of the RTC count block to the RTCCO external pin.
1	The RTC count block outputs a signal generated by dividing the CO signal by 2 to the RTCCO external pin.

CHAPTER 4-7: RTC Clock Control Block (C)

This chapter explains the functions and operations of the RTC clock control block(C).

1. Overview of the RTC Clock Control Block
2. Configuration of the RTC Clock Control Block
3. Operations of the RTC Clock Control Block
4. Setting Procedures of the RTC Clock Control Block
5. Registers of the RTC Clock Control Block

1. Overview of the RTC Clock Control Block

This chapter shows the overview of the functions of the RTC clock control block.

RTC Clock Control Block

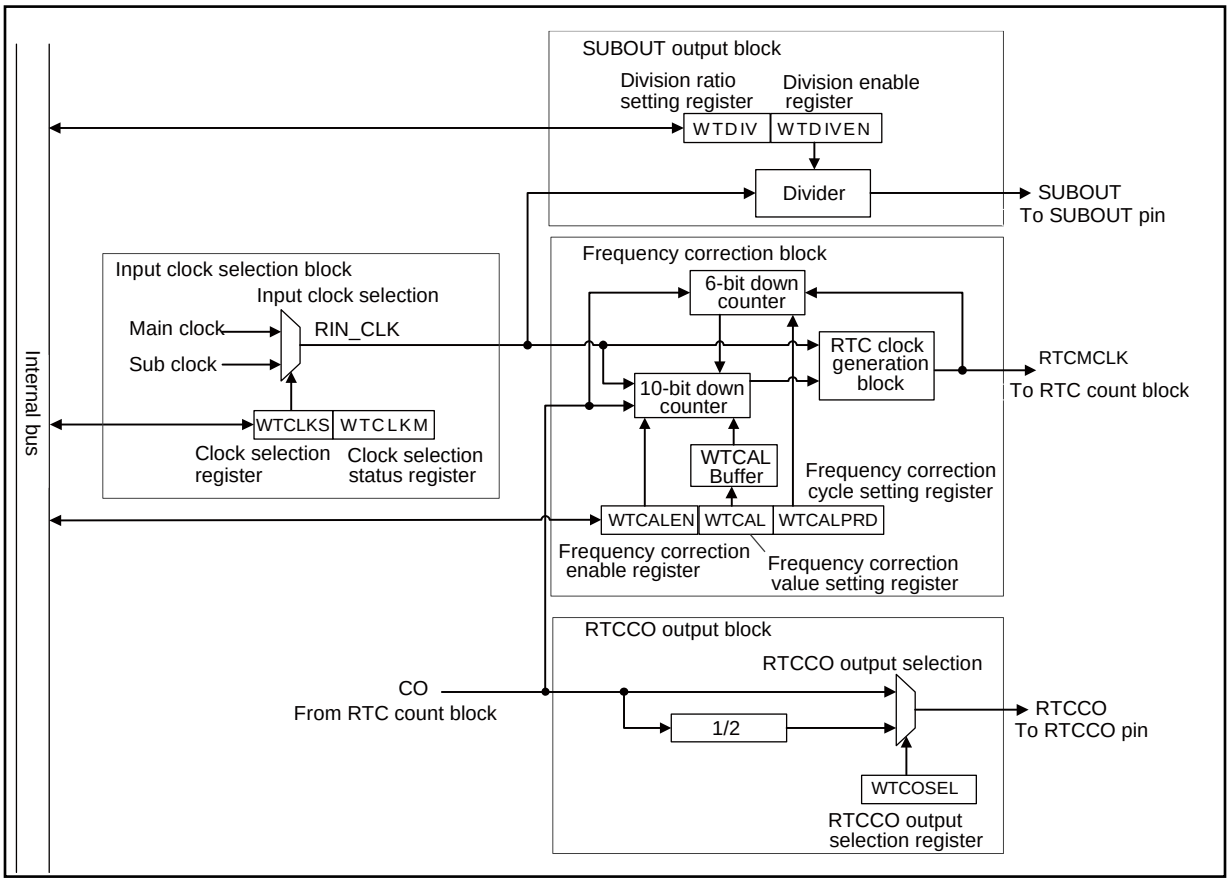
The RTC clock control block has the following functions:

- Generation of the RTC clock (RTCMCLK) to be used in the RTC count block.
- Selection of a main clock and sub clock as an input clock (RIN_CLK).
- Generation of the division clock to be output to the SUBOUT external pin.
- Generation of 0.5 second pulse or 1 second pulse to be output to the RTCCO external pin.
- Correction of fluctuation in input clock (sub clock) frequency due to temperature (frequency correction function).
  (The frequency correction function supposes that a temperature sensor is connected to the RTC clock control block externally.)

2. Configuration of the RTC Clock Control Block

This section shows the block diagram of the RTC clock control block.

Figure 2-1 Block Diagram of the RTC Clock Control Block



- Input clock selection block

  Select the input clock (RIN_CLK) as the main clock and sub clock by setting the clock selection register (WTCALS).

- Frequency correction block

  The frequency correction block masks RIN_CLK and outputs frequency-corrected RTCMCLK.
  The frequency correction block masks RIN_CLK according the number of the value set in the WTCAL buffer at the cycles set as WTCALPRD register.

- SUBOUT output block

  The SUBOUT output block generates the division clock to be output to the SUBOUT external pin.
  In deep standby RTC mode, no division clock can be output from the SUBOUT external pin.

- RTCCO output block

  The RTCCO output block generates a signal as an RTCCO external pin output.
  The RTCCO external pin output selects a possible CO signal from an RTC count block or 2 divisions of CO signal.
  In deep standby RTC mode, no output from RTCCO is possible.

3. Operations of the RTC Clock Control Block

This section explains the operations of the RTC clock control block.

Frequency Correction Block

A gap of the frequency of RIN_CLK is corrected.

The mask of RIN_CLK is carried out a fixed cycle, and the RTCMCLK that performed frequency correction is outputted.

A cycle is set as frequency correction cycle setting register (WTCALPRD).

The number of clocks which carry out a mask to frequency correction value setting register (WTCAL) is set.

Figure 3-1 Example of a Frequency Correction Block of Operation (WTBR = 8190 and WTCALPRD = 19)

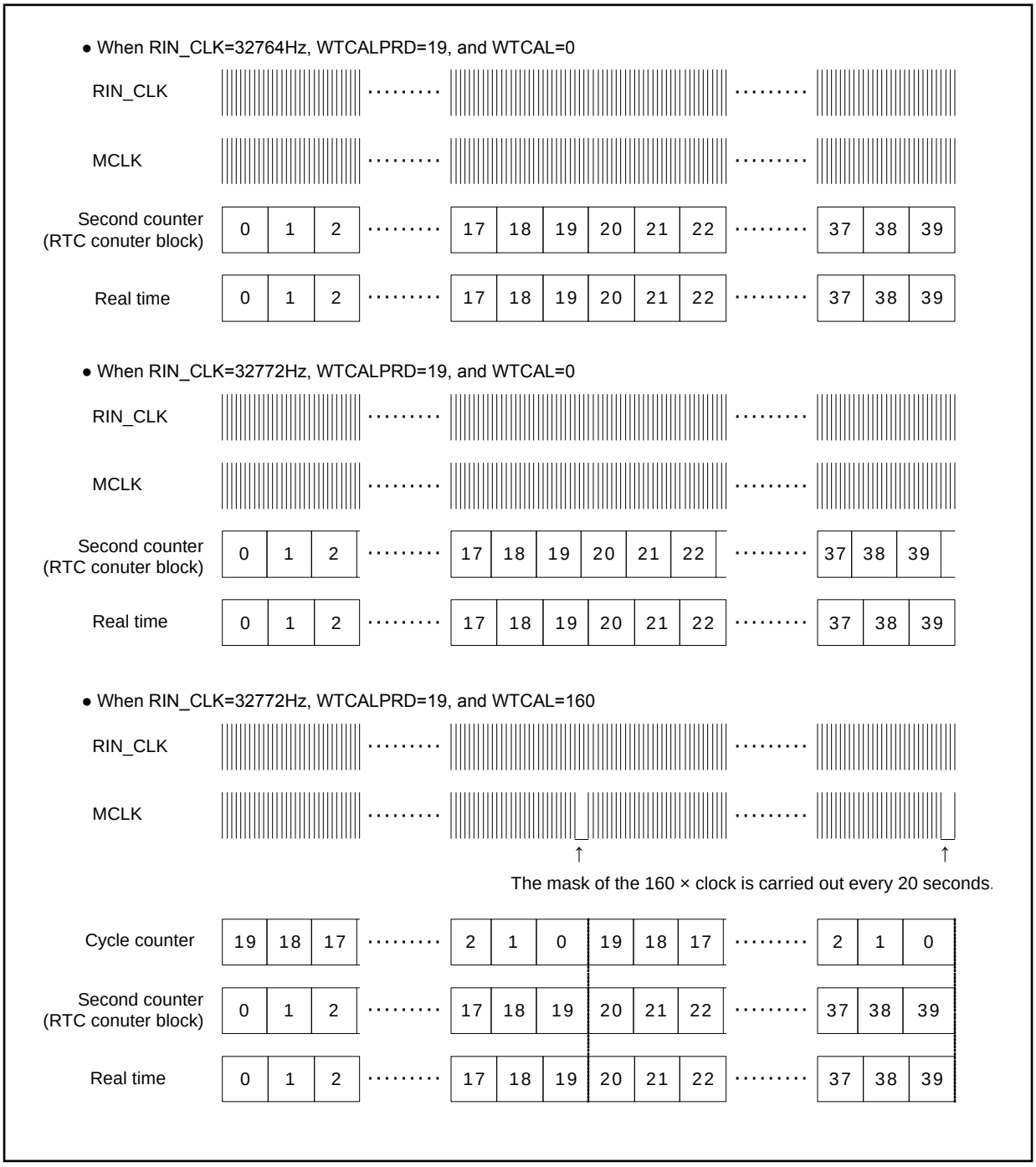
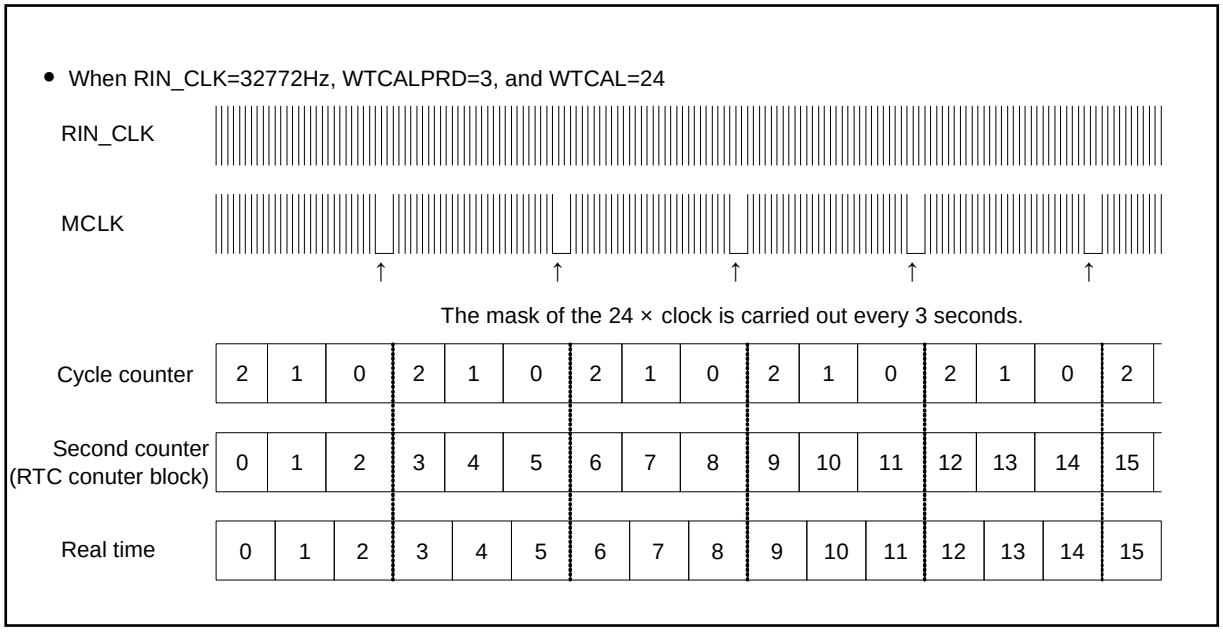


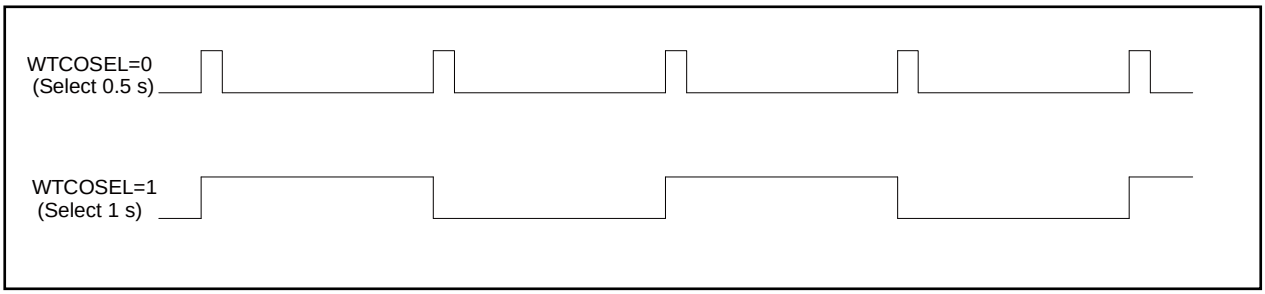
Figure 3-2 Example of a Frequency Correction Block of Operation (WTBR = 8190 and WTCALPRD = 3)



RTCCO External Pin Output Clock Selection Block

By setup of the RTCCO clock selection register (WTCOSEL), CO signal (0.5 second) from an RTC count block or the 2 divisions (1 second) of CO signal is selected, and it outputs to an RTCCO external pin.

Figure 3-3 Examples of Operations of Frequency Correction Block



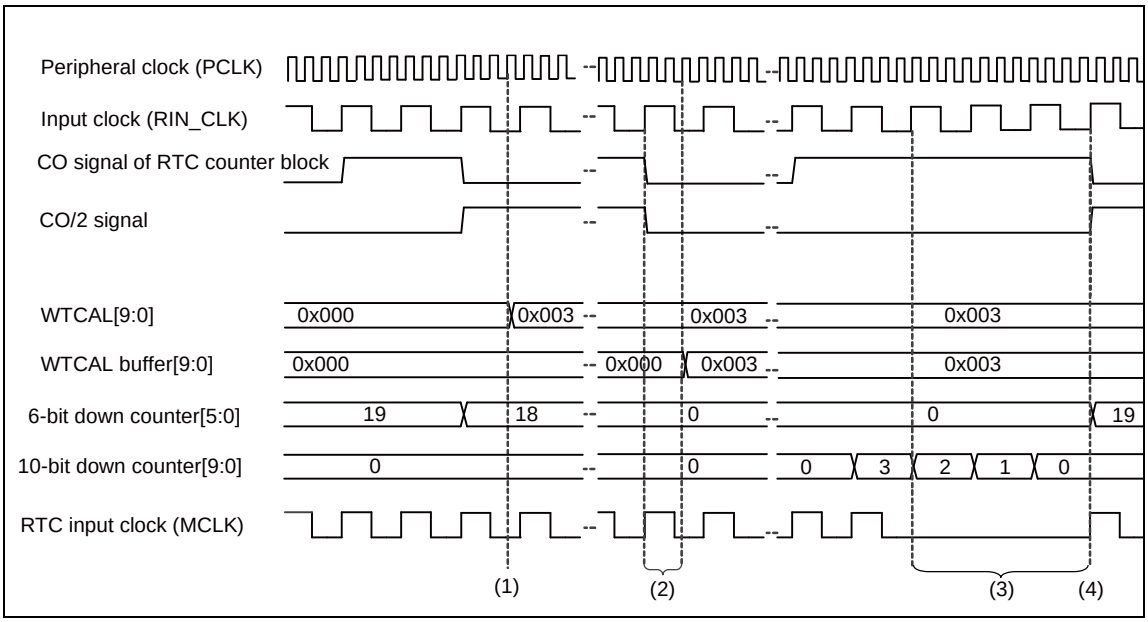
See the chapter RTC Count Block for CO signal (0.5 second) from an RTC count block.

Operation of the WTCAL Buffer

The frequency correction value setting register (WTCAL) sets the number of clock cycles masked by the frequency correction function.

The frequency correction block incorporates a WTCAL buffer because this block in operation makes the frequency correction value setting register (WTCAL) rewritable.

Figure 3-4 Operation Diagram of the WTCAL Buffer



(1) The WTCAL buffer writes the number of clocks to be masked in the frequency correction value setting register (WTCAL).

(2) 6-bit down counter = 0 it is set to zero and the value of WTCAL is transmitted after 3 clocks of the APB2 bus clock (PCLK2) at a WTCAL buffer.

(3) The value of a WTCAL register is loaded to a 10-bit down counter just before the underflow of 6-bit down counter, and carry out the mask of the clock of the set-up value.

(4) 6-bit down counter loads the value of a WTCAL buffer at the time of underflow.

Note:

- *The CO signal of an RTC count block is High at the mask of the clock set up by the WTCAL register is carried out.*

Frequency Correction Range

Table 3-1 and Table 3-2 show the examples of the frequency correction range. The frequency correction block corrects a frequency according to a combination of settings of the WTBR register of an RTC count block, a WTCAL register, and a WTCALPRD register.

Table 3-1 Example of Frequency Correction Range (WTCALPRD = 19) (Ideal Value)

WTCAL	WTBR = 8190		WTBR = 8189	
	Correction Rate [ppm]	Sub Clock Frequency [Hz]	Correction Rate [ppm]	Sub Clock Frequency [Hz]
0	122.1	32764.00	244.1	32760.00
1	120.5	32764.05	242.6	32760.05
2	119.0	32764.10	241.1	32760.10
:	:	:	:	:
79	1.5	32767.95	123.6	32763.95
80	0.0	32768.00	122.1	32764.00
81	-1.5	32768.05	120.5	32764.05
:	:	:	:	:
159	-120.5	32771.95	1.5	32767.95
160	-122.1	32772.00	0.0	32768.00
161	-123.6	32772.05	-1.5	32768.05
:	:	:	:	:
318	-363.2	32779.90	-241.1	32775.90
319	-364.7	32779.95	-242.6	32775.95
320	-366.2	32780.00	-244.1	32776.00

Table 3-2 Example of Frequency Correction Range (WTCALPRD = 59) (Ideal Value)

WTCAL	WTBR = 8190	WTBR = 8189	WTBR = 8190	WTBR = 8189
	Correction Rate [ppm]	Sub Clock Frequency [Hz]	Correction Rate [ppm]	Sub Clock Frequency [Hz]
0	122.1	32764.00	244.1	32760.00
1	121.6	32764.02	243.6	32760.02
2	121.1	32764.03	243.1	32760.03
:	:	:	:	:
239	0.5	32767.98	122.6	32763.98
240	0.0	32768.00	122.1	32764.00
241	-0.5	32768.02	121.6	32764.02
:	:	:	:	:
479	-121.6	32771.98	0.5	32767.98
480	-122.1	32772.00	0.0	32768.00
481	-122.6	32772.02	-0.5	32768.02
:	:	:	:	:
958	-365.2	32779.97	-243.1	32775.97
959	-365.7	32779.98	-243.6	32775.98
960	-366.2	32780.00	-244.1	32776.00

4. Setting Procedures of the RTC Clock Control Block

This section explains the setting procedures of the RTC clock control block.

Setting Procedures of Frequency Correction (with Sub Clock Selected)

(1) Write 0 to the input clock selection bit (WTCLKS) to select the sub clock.

(2) Read the clock selection status bit (WTCLKM) and wait until the sub clock 10 is selected.

(3) Write the correction cycle to frequency correction cycle setting register (WTCALPRD) and the correction value to the frequency correction value setting register (WTCAL).
Obtain the set value for the WTCAL from the following formula:
WTCAL = {(Frequency before correction - (WTBR+1) × 4) / (WTCALPRD + 1)} × 2^{20}

(4) The frequency correction will be enabled with 1 written to the frequency correction enable bit (WTCALEN).

Procedure for Changing Settings during the Operation of the Frequency Correction Function

(1) Write 0 to the divider output enable bit (WTDIVEN).
The divider will stop operating and the SUBOUT external output will output a low level.

(2) Read the divider status bit (WTDIVRDY) and wait until the value becomes 0 (the divider is not in operation).

(3) Write the divider ratio to the divider ratio setting bit (WTDIV). For divider ratio settings, see 5.6 Divider Output Enable Register (WTDIVEN).

(4) The divider is set to operation enabled by writing 1 to the divider output enable bit (WTDIVEN).

5. Registers of the RTC Clock Control Block

This section shows the list of registers of the RTC clock control block.

Table 5-1 List of Registers of the RTC Clock Control Block

Abbreviation	Register Name	Reference
WTCLKS	Clock selection register	5.1
WTCLKM	Selection clock status register	5.2
WTCAL	Frequency correction value setting register	5.3
WTCALEN	Frequency correction enable register	5.4
WTDIV	Divider ratio setting register	5.5
WTDIVEN	Divider output enable register	5.6
WTCALPRD	Frequency correction cycle setting register	5.7
WTCOSEL	RTCCO output selection register	5.8

5.1 Clock Selection Register (WTCLKS)

This register is used for the input clock (RIN_CLK) selection.

bit	7	1	0
Field	Reserved		WTCLKS
Attribute	R		R/W
Initial value	0000000		0

[bit7:1] Reserved: Reserved bits

The read value is always 0.

Write 0 to a reserved bit in a write access to it.

[bit0] WTCLKS: Input clock selection bit

This bit is used for the following input clock (RIN_CLK) selection.

Bit	Description
0	Selects the sub clock.
1	Selects the main clock.

5.2 Selection Clock Status Register (WTCLKM)

This register shows the status of the input clock (RIN_CLK) selection.

bit	7	2	1	0
Field	Reserved		WTCLKM	
Attribute	R		R	
Initial value	000000		00	

[bit7:2] Reserved: Reserved bits

The read value is always 0.

Write 0 to a reserved bit in a write access to it.

[bit1:0] WTCLKM: Clock selection status bits

This bit shows the status of the input clock (RIN_CLK) selection.

Bit1:0	Description
0x	The RIN_CLK is not in operation
10	The sub clock is selected.
11	The main clock is selected.

Note:

- *A software reset, RTC reset, or APB2 bus reset does not initialize this register.*

5.3 Frequency Correction Value Setting Register (WTCAL)

The Frequency Correction Value Setting register 1 (WTCAL1) causes the frequency correction value of the RTC clock to be output to the RTC count block.

bit	15	14	13	12	11	10	9	8
Field	Reserved						WTCAL	
Attribute	R						R/W	
Initial value	000000						00	

bit	7	6	5	4	3	2	1	0
Field	WTCAL							
Attribute	R/W							
Initial value	00000000							

[bit15:10] Reserved: Reserved bits

The read value is always 0.
Write 0 to a reserved bit in a write access to it.

[bit9:0] WTCAL: Frequency correction value setting bits

The number of cycles to be masked is set cycle as the WTCALPRD register.
Eight clocks will be masked from the input clock (RIN_CLK) for each 20 s and the RTCMCLK output will be generated to the RTC count block if the WTCALPRD is set as 19 and the WTCAL is set to 8.
For the WTCAL set value, see Setting procedures of frequency correction (with sub clock selected) in 4. Setting Procedures of the RTC Clock Control Block.

Note:

- *A software reset or APB2 bus reset does not initialize this register.*

5.4 Frequency Correction Enable Register (WTCALEN)

This register enables frequency corrections to the clock (RTCMCLK) input into the RTC count block.

bit	7	1	0
Field	Reserved		WTCALEN
Attribute	R		R/W
Initial value	0000000		0

[bit7:1] Reserved: Reserved bits

The read value is always 0.

Write 0 to a reserved bit in a write access to it.

[bit0] WTCALEN: Frequency correction value setting bit

This bit enables frequency correction.

Bit	Description
0	Disables the frequency correction
1	Enables frequency correction.

5.5 Division Ratio Setting Register (WTDIV)

This register sets the division ratio of the divider.

bit	7	6	5	4	3	2	1	0
Field	Reserved				WTDIV			
Attribute	R				R/W			
Initial value	0	0	0	0	0	0	0	0

[bit7:4] Reserved: Reserved bits

The read value is always 0.

Write 0 to a reserved bit in a write access to it.

[bit3:0] WTDIV: Division ration setting bits

These bits set the division ratio for the input clock and for the division clock (SUBOUT) that the divider outputs.

bit3:0	Description
0000	No division
0001	Division ratio: 1/2
0010	Division ratio: 1/4
0011	Division ratio: 1/8
0100	Division ratio: 1/16
0101	Division ratio: 1/32
0110	Division ratio: 1/64
0111	Division ratio: 1/128
1000	Division ratio: 1/256
1001	Division ratio: 1/512
1010	Division ratio: 1/1024
1011	Division ratio: 1/2048
1100	Division ratio: 1/4096
1101	Division ratio: 1/8192
1110	Division ratio: 1/16384
1111	Division ratio: 1/32768

Notes:

- *Before writing a value to the WTDIV bits, ensure that the divider enable bit (WTDIVEN) in the Divider Output Enable register (WTDIVEN) is 0.*
- *A software reset or APB2 bus reset does not initialize this register.*

5.6 Divider Output Enable Register (WTDIVEN)

This register enables the output of divider.

bit	7	2	1	0
Field	Reserved		WTDIVRDY	WTDIVEN
Attribute	R		R	R/W
Initial value	000000		0	0

[bit7:2] Reserved: Reserved bits

The read value is always 0.

Write 0 to a reserved bit in a write access to it.

[bit1] WTDIVRDY: Divider state bit

This bit shows the state of the divider.

Bit	Description
0	The divider has stopped operating. The SUBOUT external pin output is fixed at Low.
1	The divider is operating.

[bit0] WTDIVEN: Divider enable bit

This bit enables the operation of the divider.

Bit	Description
0	Stops the operation of the divider.
1	Enables the operation of the divider.

Note:

- *A software reset or APB2 bus reset does not initialize this register.*

5.7 Frequency Correction Period Setting Register (WTCALPRD)

This register sets the period for frequency correction.

bit	7	6	5	0
Field	Reserved		WTCALPRD	
Attribute	R		R/W	
Initial value	00		010011	

[bit7:6] Reserved: Reserved bits

The read value is always 0.

Write 0 to a reserved bit in a write access to it.

[bit5:0] WTCALPRD: Frequency correction value setting bits

Set these bits to a value that is the remainder of subtracting 1 from the period (in seconds) of masking the clock for frequency correction.

For instance, if these bits are set to 0, the period becomes 1 second long; if these bits are set to 19, the period becomes 20 seconds long.

Note:

- *A software reset or APB2 bus reset does not initialize this register.*

5.8 RTCCO Output Selection Register (WTCOSEL)

This register selects the RTCCO output.

bit	7	1	0
Field	Reserved		WTCOSEL
Attribute	R		R/W
Initial value	0000000		0

[bit7:1] Reserved: Reserved bits

The read value is always 0.

Write 0 to a reserved bit in a write access to it.

[bit0] WTCOSEL: RTCCO output selection bit

This bit selects the RTCCO output.

Bit	Description
0	The CO signal of the RTC count block is output
1	The 2 divisions of CO signal are output.

CHAPTER 5-1: Base Timer I/O Select Function

This chapter explains the base timer I/O select function.

1. Overview
2. Configuration
3. I/O Mode
4. Registers

1. Overview

The base timer I/O select function sets the I/O mode, and thereby determines the method to input and output signals (external clock, external start trigger, and waveform) to/from the base timer.

By switching timer function, each channel of the base timer can be also used as one of the following timers:

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

Overview

One of the following 9 types of I/O modes can be selected for each 2 channels.

Software-based simultaneous startup function is provided for multiple channels, enabling up to 16 channels to be started up via software.

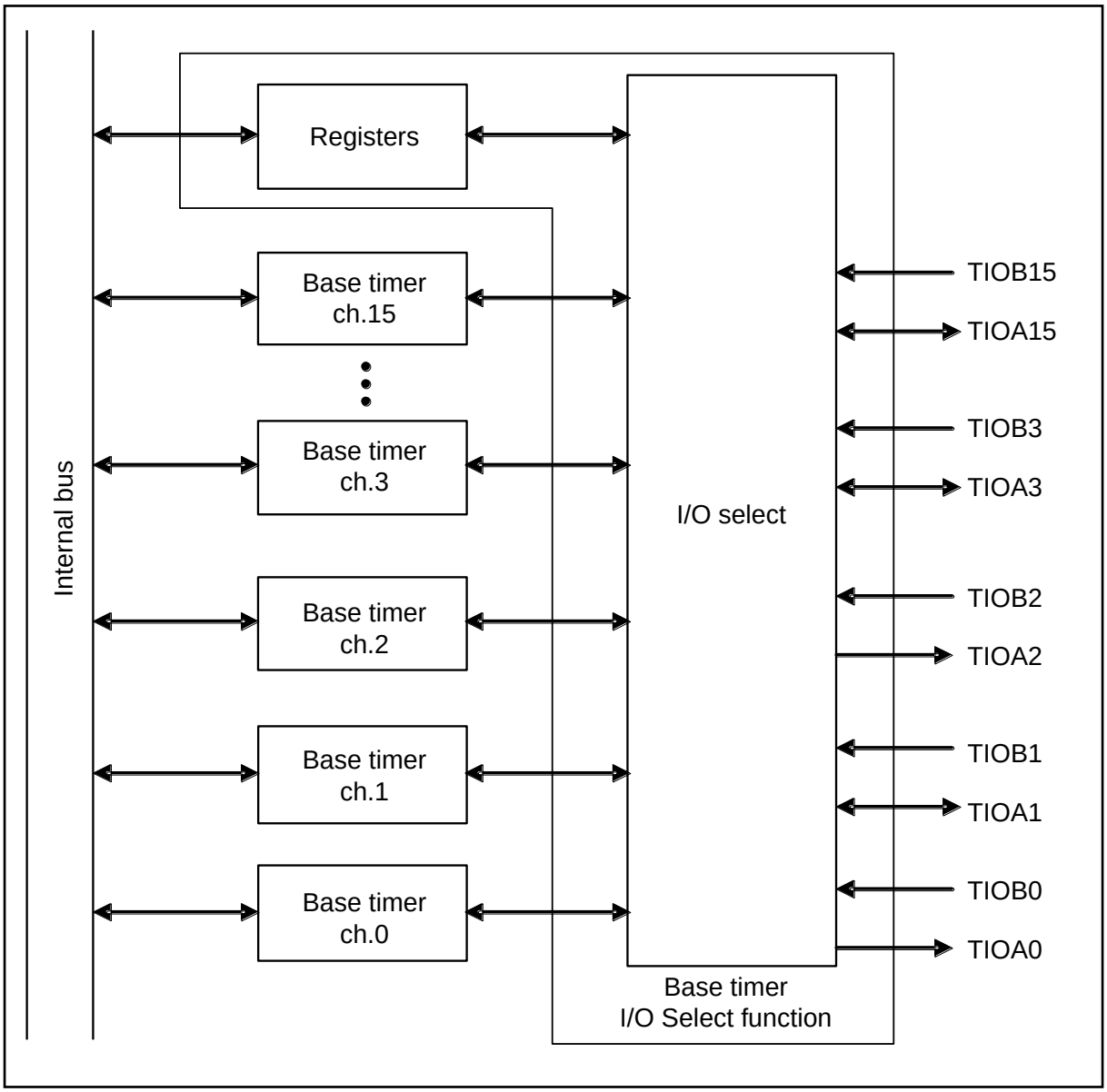
- I/O mode 0: Standard 16-bit timer mode
  This mode operates each channel of the base timer individually.
- I/O mode 1: Timer full mode
  This mode assigns each even channel signal of the base timer with an external pin individually to operate the channel.
- I/O mode 2: Shared external trigger mode
  This mode can input an external startup trigger to two channels of the base timer simultaneously. Using this mode, the base timer of two channels can be started up simultaneously.
- I/O mode 3: Shared channel signal trigger mode
  This mode uses an external signal from another channel as an external startup trigger. This mode cannot be selected for channel 0 or 1.
- I/O mode 4: Timer start/stop mode
  This mode controls the start/stop of the odd channel using the even channel. The odd channel starts on the rising edge of output signal from the even channel, and stops on the falling edge.
- I/O mode 5: Software-based simultaneous startup mode
  This mode starts up multiple channels simultaneously via software.
- I/O mode 6: Software-based startup and timer start/stop mode
  This mode controls the start/stop of the odd channel using the even channel. An even channel is started up via software. The odd channel starts on the rising edge of output signal from the even channel, and stops on the falling edge.
- I/O mode 7: Timer start mode
  This mode controls the start of the odd channel using the even channel. The odd channel starts on the rising edge of output signal from the even channel.
- I/O mode 8: Shared channel signal trigger and timer start/stop mode
  This mode uses an external signal from another channel as an external startup trigger. This mode cannot be selected for channel 0 or 1.
- I/O mode 9: Event counter mode (External clock mode)
  This mode is equipped for TYPE5-M4 and TYPE6-M4 products.
  This mode is the input clock (count clock) of the odd channel uses the external clock.

2. Configuration

The base timer I/O select function consists of the following blocks.

Figure 2-1 shows the block diagram of the base timer I/O select function.

Figure 2-1 Block Diagram of Base Timer I/O Select Function



- I/O select
  A circuit that selects the I/O mode of the base timer for each channel.
- Base timer (Channels 0 to 15)
  Base timer channels 0 to 15 (up to 16 channels).
- Registers
  Registers of base timer I/O select function.

3. I/O Mode

This section explains pins used by the base timer I/O select function to set the I/O mode, and also explains each I/O mode.

3.1. Pins

3.2. I/O Mode

3.1 Pins

This section explains pins used by the base timer I/O select function to set the I/O mode.

Each channel of the base timer has 2 types of external pins and 5 types of internal signals. Also the base timer I/O select function has 2 types of internal signals. By connecting an internal signal with an external pin, the signal corresponding to the connected (external clock (ECK signal)/external startup trigger (TGIN signal)/waveform (TIN signal)) is input to or output from the base timer. The external pin and internal signal can be connected by setting the I/O mode of the base timer. The pin used and the signal input or output differ depending on the I/O mode.

External Pins

- TIOA pin

  This pin is used to output the base timer waveform (TOUT signal), or input an external startup trigger (TGIN signal).

- TIOB pin

  This pin is used to input external startup trigger (TGIN signal)/external clock (ECK signal)/another channel waveform (TIN signal).

Internal Signals

A signal is input or output to/from the base timer by being connected with an above external pin, or by inputting an output signal from another channel.

- TOUT signal

  This signal is the output waveform of the base timer. (Not used by the 16-/32-bit PWC timer.)

- ECK signal

  This signal is an external clock of the base timer. (Not used by the 16-/32-bit PWC timer.)
  It is input when the external clock is selected as a counting clock.

- TGIN signal

  This signal is the external startup trigger of the base timer. (Not used by the 16-/32-bit PWC timer.)
  When the valid edge of external startup trigger is selected, the base timer detects the edge of this signal to start up.

- TIN signal

  This signal is the input waveform of the base timer. This signal is the waveform to be measured. (Used only by the 16-/32-bit PWC timer.)

- DTRG signal

  This signal is the trigger input to the base timer. The base timer stops operating on the falling edge of this signal.

- COUT signal

  This signal is the trigger output of the base timer I/O select function. This signal is output signal to another channel of the base timer.

- CIN signal

  This signal is the trigger input to the base timer I/O select function. This signal is input signal from another channel of the base timer.

Connecting the External Pin to the Internal Signal

The external pin and internal signal can be connected by setting the I/O mode of the base timer. Table 3-1 shows the correspondence between I/O modes and pin connections.

Table 3-1 Correspondence between I/O Modes and Pin Connections

I/O Mode	TIOAn (Even channel)		TIOBn (Even channel)		TIOAn+1 (Odd channel)		TIOBn+1 (Odd channel)	
	Connected to	I/O	Connected to	I/O	Connected to	I/O	Connected to	I/O
0	Ch.n TOUT	Output	Ch.n ECK/TGIN/ TIN	Input	Ch.n+1 TOUT	Output	Ch.n+1 ECK/TGIN/ TIN	Input
1	Ch.n TOUT	Output	Ch.n ECK	Input	Ch.n TGIN	Input	Ch.n TIN	Input
2	Ch.n TOUT	Output	Ch.n/Ch.n+1 ECK/TGIN/ TIN *1	Input	Ch.n+1 TOUT	Output	Not used	
3	Ch.n TOUT	Output	Not used					
4	Ch.n TOUT	Output	Ch.n ECK/TGIN/ TIN	Input				
5	Ch.n TOUT	Output	Not used					
6	Ch.n TOUT	Output						
7	Ch.n TOUT	Output	Ch.n ECK/TGIN/ TIN	Input				
8	Ch.n TOUT	Output	Not used					
9	Ch.n TOUT	Output	Ch.n ECK/TGIN/ TIN	Input			Ch.n+1 ECK	Input

n: Even (n=0, 2, 4, 6, 8, 10, 12, 14) However, n depends on the number of channels mounted.
Ch.n: Even channel
Ch.n+1: Odd channel
*1: Synchronized by the peripheral clock (PCLK)

3.2 I/O Mode

I/O mode selected by the I/O Select Register (BTSEL) determines the functions of external pins and the start/stop timing of the base timer.

I/O Mode 0 (Standard 16-bit Timer Mode)

This mode uses each channel of the base timer individually.

Table 3-2 shows the external pins used when this mode is selected.

Table 3-2 External Pins Used When I/O Mode 0 Is Selected.

	Even Channel	Odd Channel
Number of input pins	1	1
Number of output pins	1	1

Table 3-3 shows the internal signals to which the external pins connect, and signals input or output.

Table 3-3 External Pin Connections and Input/output Signals When I/O Mode 0 Is Selected.

External Pin	I/O	Connected to (Internal Signal)	Signal Input/Output
TIOA	Output	TOUT	Outputs the base timer waveform
TIOB	Input	ECK/TGIN/TIN*	Uses the input signal as one of the following signals: – External clock (ECK signal) – External startup trigger (TGIN signal) – Waveform to be measured (TIN signal)

*: The usage of input signals (ECK/TGIN/TIN) differs depending on the Timer Control Register (TMCR) setting of the base timer.

Figure 3-1 provides the block diagram of I/O mode 0 (Standard 16-bit timer mode).

Figure 3-1 I/O Mode 0 (Standard 16-bit Timer Mode) Block Diagram

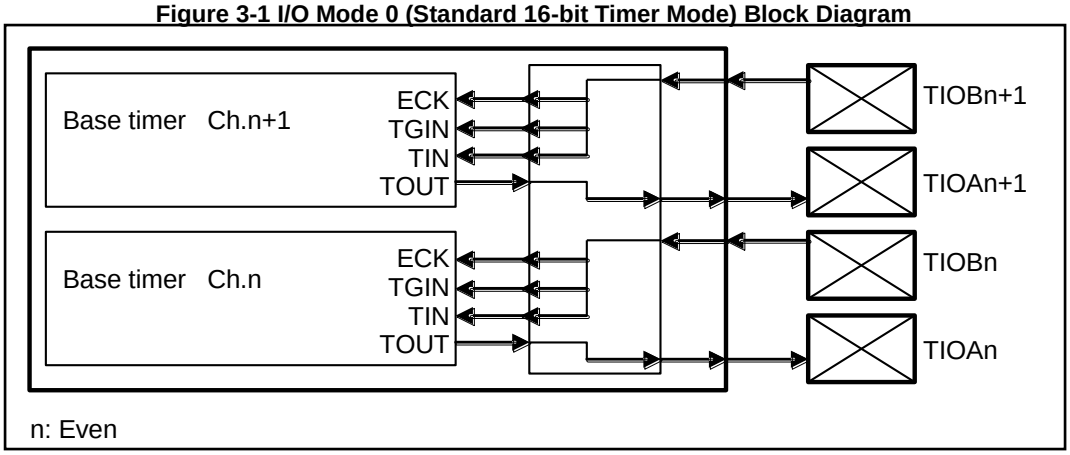


Table 3-4 shows signal connections in I/O mode 0.

Table 3-4 I/O Mode 0 Signal Connections

Connected from (Signal)	Connected to
Ch.n TOUT signal	Output from the TIOAn pin
Input signal from the TIOBn pin	Input to Ch.n as ECK/TGIN/TIN signals
Ch.n+1 TOUT signal	Output from the TIOAn+1 pin
Input signal from the TIOBn+1 pin	Input to Ch.n+1 as ECK/TGIN/TIN signals

n: Even

I/O Mode 1 (Timer Full Mode)

This mode assigns every even channel signal with an external pin individually.

Table 3-5 shows the external pins used when this mode is selected.

Table 3-5 External Pins Used When I/O Mode 1 Is Selected.

	Even Channel
Number of input pins	3
Number of output pins	1

Table 3-6 shows the internal signals to which the external pins connect, and signals input or output.

Table 3-6 External Pin Connections and Input/output Signals When I/O Mode 1 Is Selected.

External Pin	I/O	Connected to (Internal Signal)	Signal Input/Output
TIOAn	Output	Even channel TOUT	Outputs the even channel waveform
TIOBn	Input	Even channel ECK	Inputs an external clock (ECK signal) to the even channel.
TIOAn+1	Input	Even channel TGIN	Inputs an external startup trigger (TGIN signal) to the even channel.
TIOBn+1	Input	Even channel TIN	Inputs the waveform to be measured (TIN signal) to the even channel.

n: Even

Figure 3-2 shows the block diagram of I/O mode 1 (timer full mode).

Figure 3-2 I/O Mode 1 (timer full mode) Block Diagram

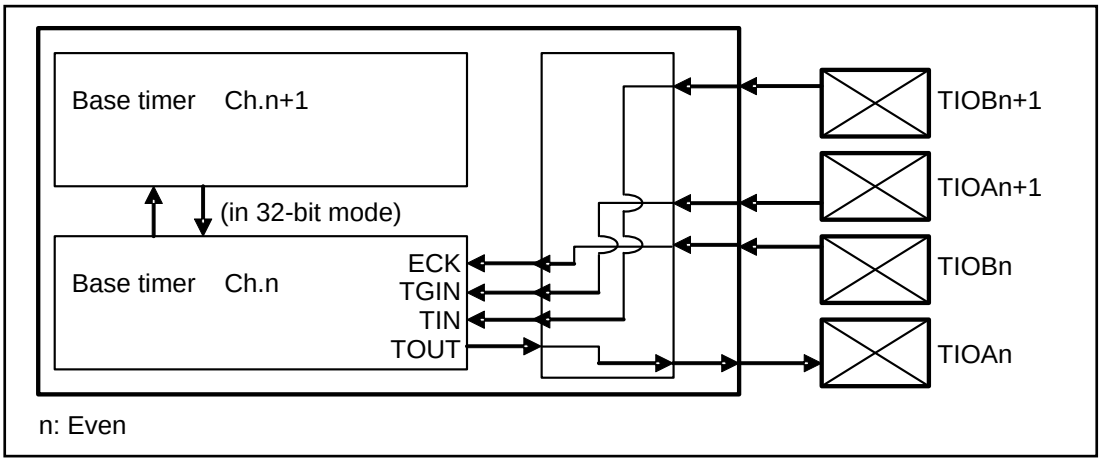


Table 3-7 shows signal connections in I/O mode 1.

Table 3-7 I/O Mode 1 Signal Connections

Connected from (Signal)	Connected to
Ch.n TOUT signal	Output from the TIOAn pin
Input signal from the TIOBn pin	Input to Ch.n as an ECK signal
TIOAn+1 pin	Input to Ch.n as a TGIN signal
TIOBn+1 pin	Input to Ch.n as an TIN signal

n : Even

Note:

- *When this mode is selected, the TIOA pins (TIOA1, TIOA3, etc.) corresponding to the odd channel must be set to port input mode with the Port Function Register (PFR) of GPIO.*

I/O Mode 2 (Shared External Trigger Mode)

This mode shares the input signals (ECK/TGIN/TIN) of the base timer between two channels.

Table 3-8 shows the external pins used when this mode is selected.

Table 3-8 External Pins Used When I/O Mode 2 Is Selected

	Even Channel	Odd Channel
Number of input pins	1 (shared by two channels)	
Number of output pins	1	1

Table 3-9 shows the internal signals to which the external pins connect, and signals input or output.

Table 3-9 External Pin Connections and Input/output Signals When I/O Mode 2 Is Selected

External Pin	I/O	Connected to (Internal Signal)	Signal Input/Output
TIOAn	Output	Even channel TOUT	Outputs the even channel waveform
TIOAn+1	Output	Odd channel TOUT	Outputs the odd channel waveform
TIOBn	Input	ECK/TGIN/TIN of even and odd channels *	Input to both the even and odd channels (synchronized by the peripheral clock (PCLK)) and used as one of the following signals: - External clock (ECK signal) - External startup trigger (TGIN signal) - Waveform to be measured (TIN signal)
TIOBn+1	-	-	Not used

n: Even

*: The usage of input signals (ECK/TGIN/TIN) differs depending on the Timer Control Register (TMCR) setting of the base timer.

Figure 3-3 shows the block diagram of I/O mode 2 (Shared external trigger mode).

Figure 3-3 I/O Mode 2 (Shared External Trigger Mode) Block Diagram

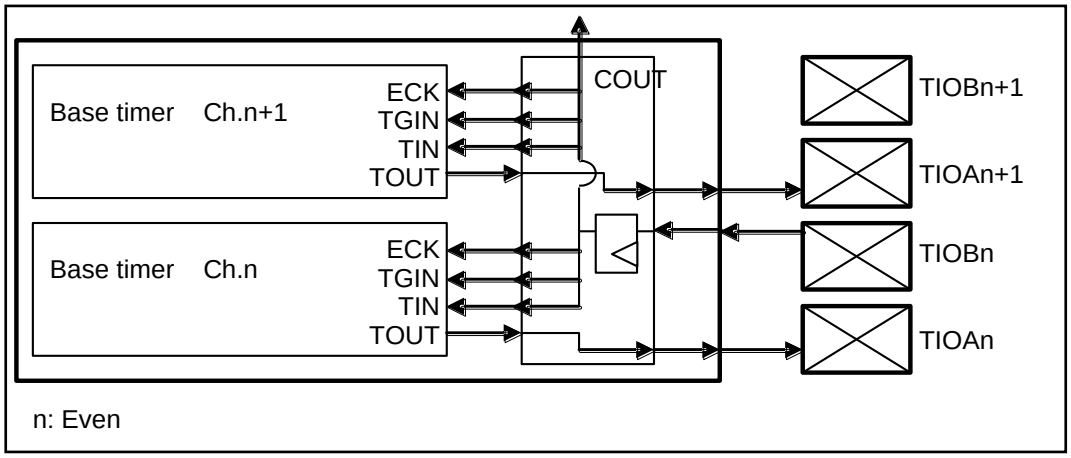


Table 3-10 shows signal connections in I/O mode 2.

Table 3-10 I/O Mode 2 Signal Connections

Connected from (Signal)	Connected to	Remarks
Ch.n TOUT signal	Output from the TIOAn pin	
Input signal from the TIOBn pin	– Input to Ch.n and Ch.n+1 as ECK/TGIN/TIN signals – Output to another channel as a COUT signal	Synchronized by the peripheral clock (PCLK)
Ch.n+1 TOUT signal	Output from the TIOAn+1 pin	

n: Even

Notes:

- *If the upper two channels of the channels set to this mode (n+2, n+3) are set to I/O mode 3 (Shared channel signal trigger mode), the input signals (ECK/TGIN/TIN) can be input to the 4 channels simultaneously.*
- *(Example: If channels 0 and 1 are set to this mode, and channels 2 and 3 are set to I/O mode 3, input signals (ECK/TGIN/TIN) can be input to four channels of 0 to 3 simultaneously.)*

I/O Mode 3 (Shared Channel Signal Trigger Mode)

This mode inputs the COUT signal from channels of the lower two channels as a CIN signal, and uses it as ECK/TGIN/TIN signals.

Table 3-11 shows the external pins used when this mode is selected.

Table 3-11 External Pins Used When I/O Mode 3 Is Selected

	Even Channel	Odd Channel
Number of input pins	Not used	
Number of output pins	1	1

Table 3-12 shows the internal signals to which the external pins connect, and signals input or output.

Table 3-12 External Pin Connections and Input/output Signals When I/O Mode 3 Is Selected

External Pin	I/O	Connected to (Internal Signal)	Signal Input/Output
TIOAn	Output	Even channel TOUT	Outputs the even channel waveform
TIOAn+1	Output	Odd channel TOUT	Outputs the odd channel waveform
TIOBn TIOBn+1	-	-	Not used

n: Even

Figure 3-4 shows the block diagram of I/O mode 3 (Shared channel signal trigger mode).

Figure 3-4 I/O Mode 3 (Shared Channel Signal Trigger Mode) Block Diagram

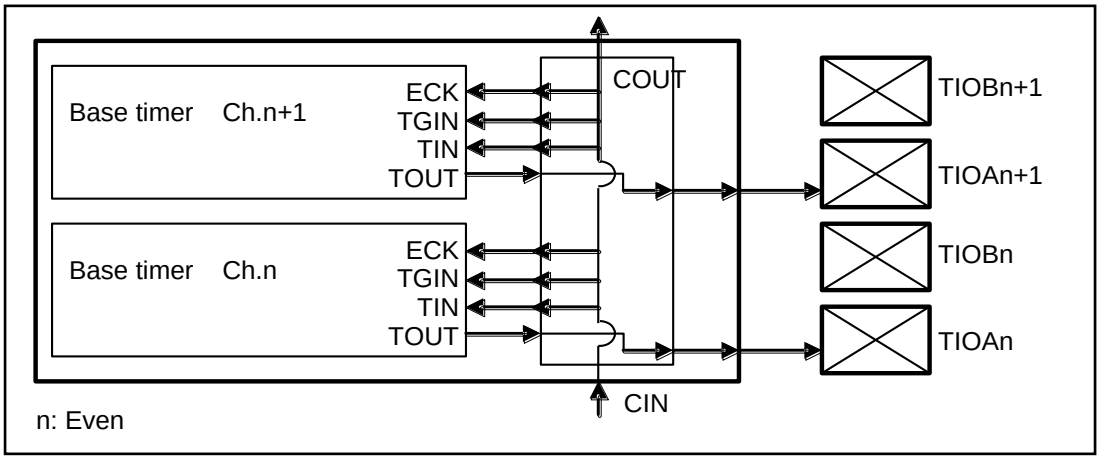


Table 3-13 shows signal connections in I/O mode 3.

Table 3-13 I/O Mode 3 Signal Connections

Connected from (Signal)	Connected to
Ch.n TOUT signal	Output from the TIOAn pin
CIN signal *	– Input to Ch.n and Ch.n+1 as ECK/TGIN/TIN signals – Output to another channel as a COUT signal
Ch.n+1 TOUT signal	Output from the TIOAn+1 pin

n: Even

*: The COUT signal from another channel is input as a CIN signal.

The following shows Ch.n-2/n-1 signals that can be input to ECK/TGIN/TIN of Ch.n/n+1.

- Signal that the peripheral clock generates by synchronizing TIOBn-2 input in I/O mode 2.
- Trigger signal input from Ch.n-4/n-3 in I/O mode 3.
- TIOAn-2 output in I/O mode 4.
- TIOAn-2 output in I/O mode 6.
- TIOAn-2 output in I/O mode 7.
- Trigger signal input from Ch.n-4/n-3 in I/O mode 8.

Notes:

- *Select the rising edge as a trigger input edge using the EGS1 and EGS0 bits in the Timer Control Register (TMCR) of the base timer. (Set EGS1 and EGS0 to 0b01.)*
- *The channels set to this mode use the COUT signal from lower two channels (n-2 and n-1) as a CIN signal. (Example: If channels 2 and 3 are set to this mode, they use the COUT signal from channels 0 and 1.) Therefore, channels 0 and 1 cannot be set to this mode.*

I/O Mode 4 (Timer Start/stop Mode)

This mode can control the start/stop of the odd channel using the even channel.

The odd channel starts on the rising edge of output waveform (TOUT signal) of the even channel, and stops on the falling edge.

Table 3-14 shows the external pins used when this mode is selected.

Table 3-14 External Pins Used When I/O Mode 4 Is Selected

	Even Channel	Odd Channel
Number of input pins	1	Not used
Number of output pins	1	1

Table 3-15 shows the internal signals to which the external pins connect, and signals input or output.

Table 3-15 External Pin Connections and Input/output Signals When I/O Mode 4 Is Selected

External Pin	I/O	Connected to (Internal Signal)	Signal Input/Output
TIOAn	Output	Even channel TOUT	Outputs the even channel waveform
TIOAn+1	Output	Odd channel TOUT	Outputs the odd channel waveform
TIOBn	Input	ECK/TGIN/TIN of even channel *	Input to the even channel and used as one of the following signals: – External clock (ECK signal) – External startup trigger (TGIN signal) – Waveform to be measured (TIN signal)
TIOBn+1	-	-	Not used

n: Even

*: The usage of input signals (ECK/TGIN/TIN) differs depending on the Timer Control Register (TMCR) setting of the base timer.

Figure 3-5 shows the block diagram of I/O mode 4 (Timer start/stop mode).

Figure 3-5 I/O Mode 4 (Timer Start/stop Mode) Block Diagram

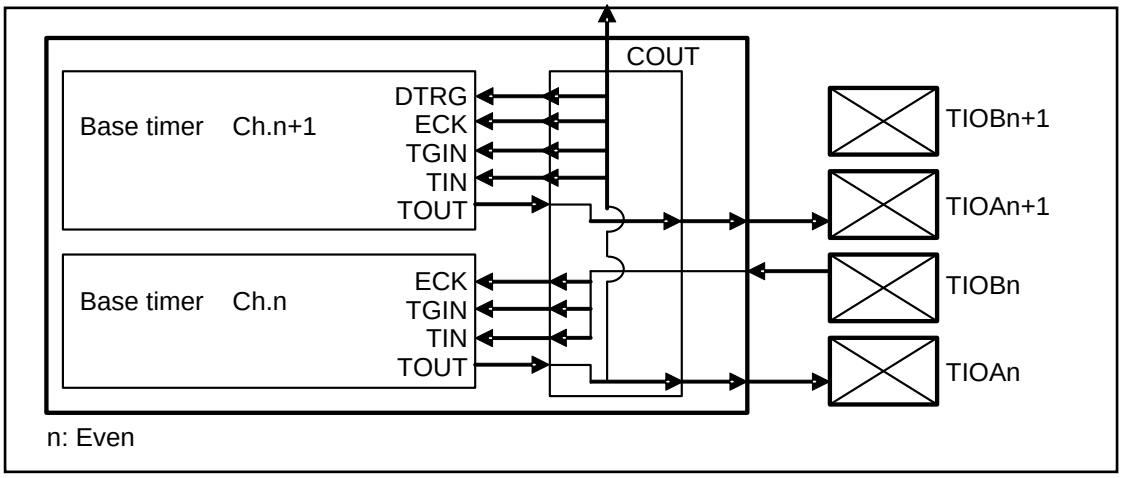


Table 3-16 shows signal connections in I/O mode 4.

Table 3-16 I/O Mode 4 Signal Connections

Connected from (Signal)	Connected to
Ch.n TOUT signal	– Output from the TIOAn pin – Input to Ch.n+1 as ECK/TGIN/TIN and DTRG signals – Output to another channel as a COUT signal
Input signal from the TIOBn pin	Input to Ch.n as ECK/TGIN/TIN signals
Ch.n+1 TOUT signal	Output from the TIOAn+1 pin

n: Even

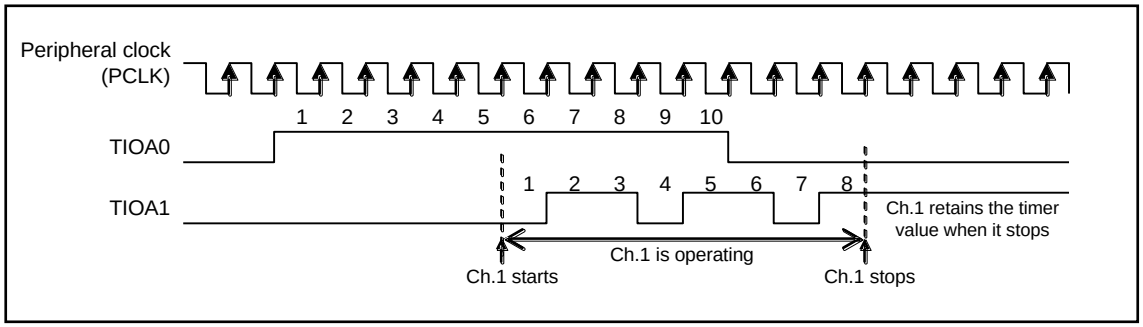
Notes:

- *Select the rising edge as a trigger input edge of the odd channel using the EGS1 and EGS0 bits in the Timer Control Register (TMCR) of the base timer. (Set EGS1 and EGS0 to 0b01.)*
- *The odd channel stops operating when a falling edge is detected in the DTRG signal.*

Figure 3-6 shows example operation when I/O mode 4 (Timer start/stop mode) is selected, and when channels 0 and 1 are used as PWM timer.

Base Timer Ch.0	Set Value	Base Timer Ch.1	Set Value
Cycle Setup Register (PCSR)	0x0010	Cycle Setup Register (PCSR)	0x0002
Duty Setup Register (PDUT)	0x0009	Duty Setup Register (PDUT)	0x0001
Timer Control Register (TMCR)	0x0013	Timer Control Register (TMCR)	0x0112

Figure 3-6 I/O Mode 4 (Timer Start/stop Mode) Operation Example



I/O Mode 5 (Software-based Simultaneous Startup Mode)

This mode starts up multiple channels simultaneously using the Software-based Simultaneous Startup Register (BTSSSR).

All the channels corresponding to the Software-based Simultaneous Startup Register (BTSSSR) bits that have been set to 1 start up simultaneously.

Table 3-17 shows the external pins used when this mode is selected.

Table 3-17 External Pins Used When I/O Mode 5 Is Selected

	Even Channel	Odd Channel
Number of input pins	Not used	
Number of output pins	1	1

Table 3-18 shows the internal signals to which the external pins connect, and signals input or output.

Table 3-18 External Pin Connections and Input/output Signals When I/O Mode 5 Is Selected

External Pin	I/O	Connected to (Internal Signal)	Signal Input/Output
TIOAn	Output	Even channel TOUT	Outputs the even channel waveform
TIOAn+1	Output	Odd channel TOUT	Outputs the odd channel waveform
TIOBn TIOBn+1	-	-	Not used

n: Even

Figure 3-7 shows the block diagram of I/O mode 5 (Software-based simultaneous startup mode).

Figure 3-7 I/O Mode 5 (Software-based Simultaneous Startup Mode) Block Diagram

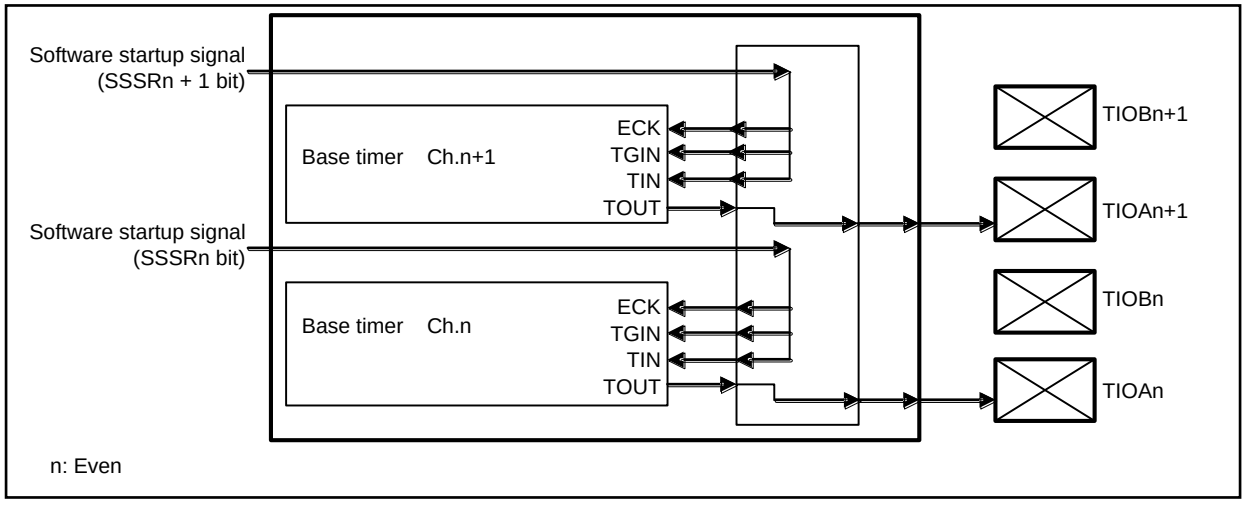


Table 3-19 shows signal connections in I/O mode 5.

Table 3-19 I/O Mode 5 Signal Connections

Connected from (Signal)	Connected to
Ch.n TOUT signal	Output from the TIOAn pin
Software startup signal (Write 1 to the SSSRn bit in the BTSSSR)	Input to Ch.n as ECK/TGIN/TIN signals
Ch.n+1 TOUT signal	Output from the TIOAn+1 pin
Software startup signal (Write 1 to the SSSRn+1 bit in the BTSSSR)	Input to Ch.n+1 as ECK/TGIN/TIN signals

n: Even

BTSSSR: Software-based Simultaneous Startup Register

When 1 is written to a Software-based Simultaneous Startup Register (BTSSSR), a rising edge is input (ECK/TGIN/TIN signals) to the channel corresponding to the bit.

Note:

- *Select the rising edge as a trigger input edge using the EGS1 and EGS0 bits in the Timer Control Register (TMCR) of the base timer. (Set EGS1 and EGS0 to 0b01.)*

I/O Mode 6 (Software-based Startup and Timer Start/stop Mode)

This mode can control the start/stop of the odd channel using the even channel.

The even channel can be started by writing 1 to the Software-based Simultaneous Startup Register (BTSSSR).

The odd channel starts when the rising edge is detected in output waveform (TOUT signal) of the even channel, and stops when the falling edge is detected.

Table 3-20 shows the external pins used when this mode is selected.

Table 3-20 External Pins Used When I/O Mode 6 Is Selected

	Even Channel	Odd Channel
Number of input pins	Not used	
Number of output pins	1	1

Table 3-21 shows the internal signals to which the external pins connect, and signals input or output.

Table 3-21 External Pin Connections and Input/output Signals When I/O Mode 6 Is Selected

External Pin	I/O	Connected to (Internal Signal)	Signal Input/Output
TIOAn	Output	Even channel TOUT	Outputs the even channel waveform
TIOAn+1	Output	Odd channel TOUT	Outputs the odd channel waveform
TIOBn TIOBn+1	-	-	Not used

n: Even

Figure 3-8 shows the block diagram of I/O mode 6 (Software-based startup and timer start/stop mode).

Figure 3-8 I/O Mode 6 (Software-based Startup and Timer Start/stop Mode) Block Diagram

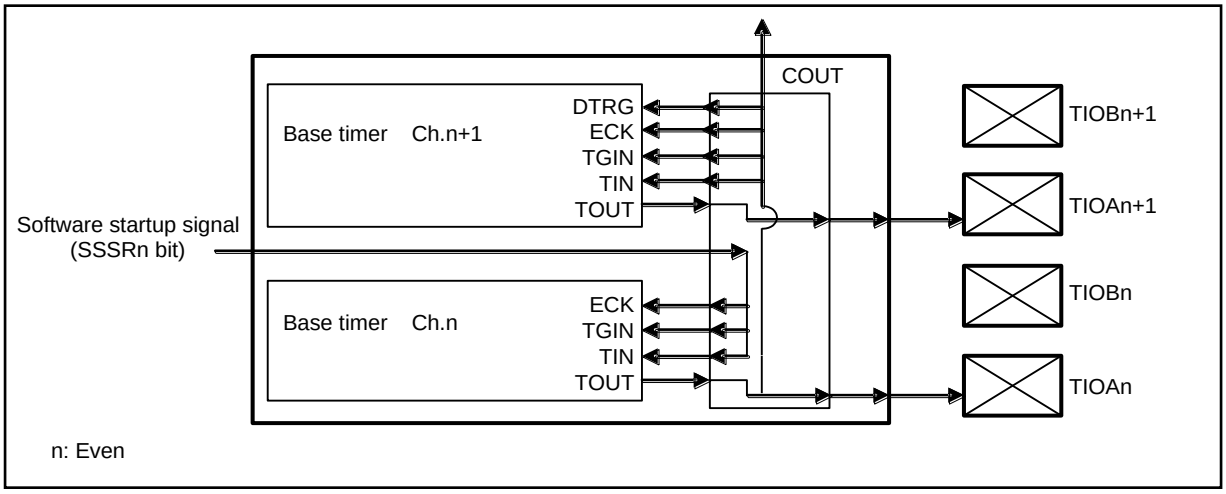


Table 3-22 shows signal connections in I/O mode 6.

Table 3-22 I/O Mode 6 Signal Connections

Connected from (Signal)	Connected to
Ch.n TOUT signal	– Output from the TIOAn pin – Input to Ch.n+1 as ECK/TGIN/TIN/DTRG signals – Output to another channel as a COUT signal
Software startup signal (Write 1 to the SSSRn bit in the BTSSSR)	Input to Ch.n as ECK/TGIN/TIN signals
Ch.n+1 TOUT signal	Output from the TIOAn+1 pin

n: Even

BTSSSR: Software-based Simultaneous Startup Register

When 1 is written to the Software-based Simultaneous Startup Register (BTSSSR) bit corresponding to the even channel you want to start up, a rising edge is input (ECK/TGIN/TIN signals) to the channel.

The start/stop timing of Ch.n is the same as that for I/O mode 4.

Notes:

- *Select the rising edge as a trigger input edge using the EGS1 and EGS0 bits in the Timer Control Register (TMCR) of the base timer. (Set EGS1 and EGS0 to 0b01.)*
- *The odd channel stops operating when a falling edge is detected in the DTRG signal.*

I/O Mode 7 (Timer Start Mode)

This mode uses the output waveform (TOUT signal) from the even channel as input signals (ECK/TGIN/TIN signals) of the odd channel.

Table 3-23 shows the external pins used when this mode is selected.

Table 3-23 External Pins Used When I/O Mode 7 Is Selected

	Even Channel	Odd Channel
Number of input pins	1	Not used
Number of output pins	1	1

Table 3-24 shows the internal signals to which the external pins connect, and signals input or output.

Table 3-24 External Pin Connections and Input/output Signals When I/O Mode 7 Is Selected

External Pin	I/O	Connected to (Internal Signal)	Signal Input/Output
TIOAn	Output	Even channel TOUT	Outputs the even channel waveform
TIOAn+1	Output	Odd channel TOUT	Outputs the odd channel waveform
TIOBn	Input	Even channel ECK/ TGIN/TIN *	Input to the even channel and used as one of the following signals: – External clock (ECK signal) – External startup trigger (TGIN signal) – Waveform to be measured (TIN signal)
TIOBn+1	-	-	Not used

n: Even

*: The usage of input waveforms (ECK/TGIN/TIN signals) differs depending on the Timer Control Register (TMCR) setting.

Figure 3-9 shows the block diagram of I/O mode 7 (Timer start mode).

Figure 3-9 I/O Mode 7 (Timer Start Mode) Block Diagram

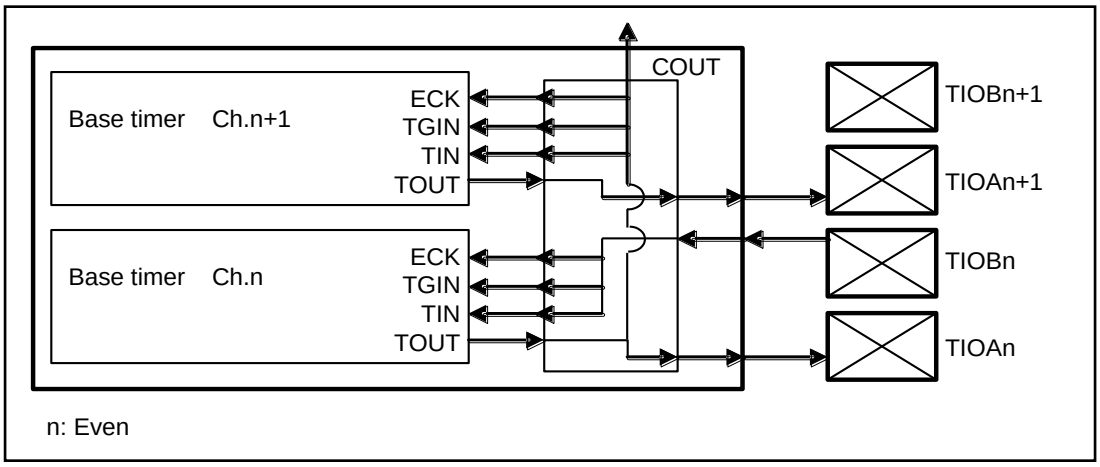


Table 3-25 shows signal connections in I/O mode 7.

Table 3-25 I/O Mode 7 Signal Connections

Connected from (Signal)	Connected to
Ch.n TOUT signal	– Output from the TIOAn pin – Input to Ch.n+1 as ECK/TGIN/TIN signals – Output to another channel as a COUT signal
Input signal from the TIOBn pin	Input to Ch.n as ECK/TGIN/TIN signals
Ch.n+1 TOUT signal	Output from the TIOAn+1 pin

n: Even

The start timing of Ch.n is the same as that for I/O mode 4.

I/O Mode 8 (Shared Channel Signal Trigger and Timer Start/stop Mode)

This mode inputs the COUT signal from channels of the lower two channels as a CIN signal, and uses it as an external startup trigger (TGIN signal).

Table 3-26 shows the external pins used when this mode is selected.

Table 3-26 External Pins Used When I/O Mode 8 Is Selected

	Even Channel	Odd Channel
Number of input pins	Not used	
Number of output pins	1	1

Table 3-27 shows the internal signals to which the external pins connect, and signals input or output.

Table 3-27 External Pin Connections and Input/output Signals When I/O Mode 8 Is Selected

External Pin	I/O	Connected to (Internal Signal)	Signal Input/Output
TIOAn	Output	Even channel TOUT	Outputs the even channel waveform
TIOAn+1	Output	Odd channel TOUT	Outputs the odd channel waveform
TIOBn TIOBn+1	-	-	Not used

n: Even

Figure 3-10 shows the block diagram of I/O mode 8 (Shared channel signal trigger and timer start/stop mode).

Figure 3-10 I/O Mode 8 (Shared Channel Signal Trigger and Timer Start/stop Mode) Block Diagram

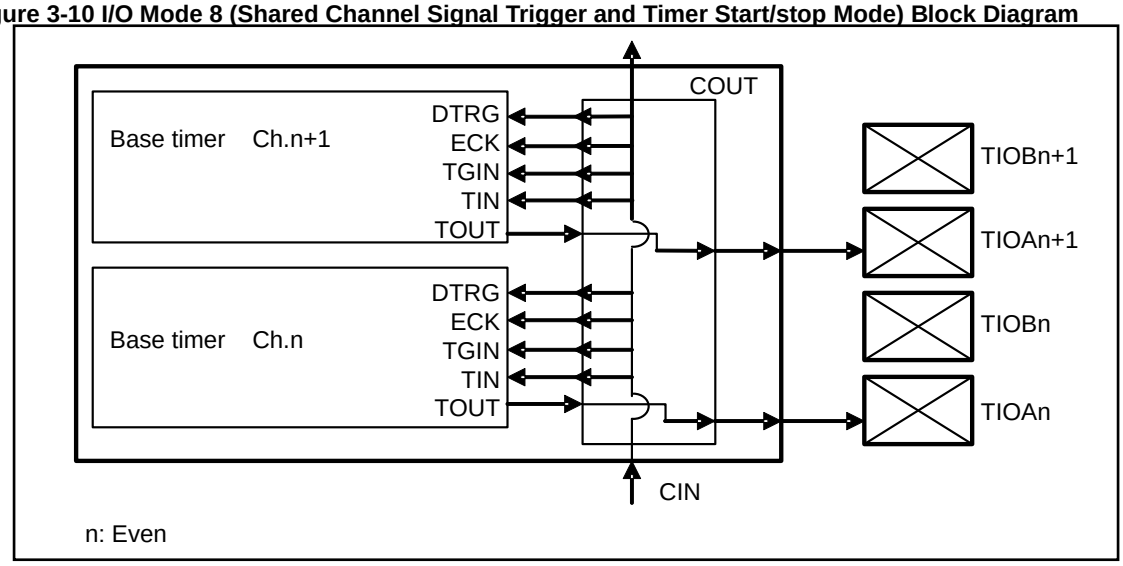


Table 3-28 shows signal connections in I/O mode 8.

Table 3-28 I/O Mode 8 Signal Connections

Connected from (Signal)	Connected to
Ch.n TOUT signal	Output from the TIOAn pin
Ch.n+1 TOUT signal	Output from the TIOAn+1 pin
CIN signal *	– Input to Ch.n and Ch.n+1 as ECK/TGIN/TIN and DTRG signals – Output to another channel as a COUT signal

n: Even

*: The COUT signal from another channel is input as a CIN signal.

The following shows Ch.n-2/n-1 signals that can be input to ECK/TGIN/TIN of Ch.n/n+1.

- Signal that the peripheral clock generates by synchronizing TIOBn-2 input in I/O mode 2.
- Trigger signal input from Ch.n-4/n-3 in I/O mode 3.
- TIOAn-2 output in I/O mode 4.
- TIOAn-2 output in I/O mode 6.
- TIOAn-2 output in I/O mode 7.
- Trigger signal input from Ch.n-4/n-3 in I/O mode 8.

Notes:

- *The channels set to this mode use the COUT signal from lower 2 channels (n-2 and n-1) as a CIN signal. (Example: If channels 2 and 3 are set to this mode, they use the COUT signal from channels 0 and 1.) Therefore, channels 0 and 1 cannot be set to this mode.*
- *Select the rising edge as a trigger input edge, for the channel set in this mode, using the EGS1 and EGS0 bits in the Timer Control Register (TMCR) of the base timer. (Set EGS1 and EGS0 to 0b01.)*
  However, do not enable this setting if the timer function is set to the 16/32-bit PWC timer using FMD2 to FMD0 bits in the Timer Control Register (TMCR) of the base timer (FMD2 to FMD0 are set to 0b100).
- *Base timer stops operating when a falling edge is detected in the DTRG signal.*

I/O Mode 9 (Event Counter Mode (External Clock Mode))

This mode is equipped for TYP5-M4 and TYPE6-M4 products.

This mode is the input clock(ECK signal) of the odd channel uses the external clock.
The even channel generates any pulse by PWM timer function.
The odd channel uses gate function of Reload timer and calculates “H” pulse width of the even channel output wave (TOUT signal).
It is possible to calculate the frequency of the external clock by this setting.

Table 3-29 shows the external pins used when this mode is selected.

Table 3-29 External Pins Use When I/O Mode 9 Is Selected

	Even Channel	Odd Channel
Number of input pins	Not used	1
Number of output pins	1	Not used

Table 3-30 shows the internal signals to which the external pins connect, and signals input or output.

Table 3-30 External Pin Connections and Input/output Signals When I/O Mode 9 Is Selected

External Pin	I/O	Connected to (Internal Signal)	Signal Input/Output
TIOAn	Output	Even channel TOUT	Outputs the even channel waveform
TIOAn+1	Output	Odd channel TOUT	Outputs the odd channel waveform
TIOBn	Input	Even channel ECK/ TGIN/TIN *	Input to the even channel and used as one of the following signals: − External clock (ECK signal) − External startup trigger (TGIN signal) − Waveform to be measured (TIN signal)
TIOBn+1	Input	Even channel ECK	Inputs an external clock (ECK signal) to the even channel.

n: Even
*: The usage of input waveforms (ECK/TGIN/TIN signals) differs depending on the Timer Control Register (TMCR) setting.

Figure 3-11 shows the block diagram of I/O mode 9 (Event counter mode)

Figure 3-11 I/O Mode 9 (Event Counter Mode) Block Diagram

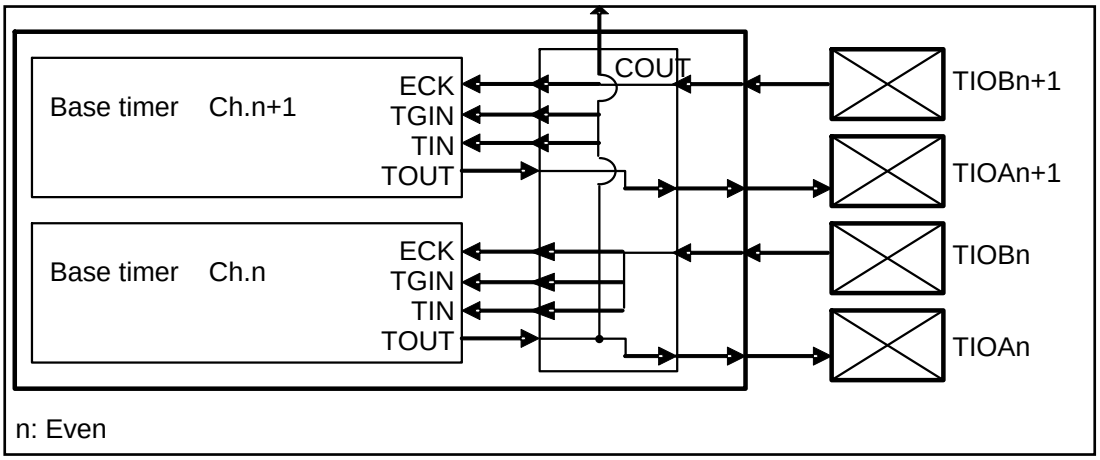


Table 3-31 shows signal connections in I/O mode 8.

Table 3-31 I/O Mode 9 Signal Connections

Connected from (Signal)	Connected to
Input signal from the TIOBn pin	Input to Ch.n as a ECK/TGIN/TIN signal
Ch.n TOUT signal	Output from the TIOAn pin
Input signal from the TIOBn+1 pin	Input to Ch.n+1 as a ECK signal
Ch.n+1 TOUT signal	Output from the TIOAn+1 pin

n: Even

The calculation of the external clock frequency is below.

$$\text{The external clock frequency} = \frac{\text{TMR (Measurement of reload timer) of the odd channel}}{\text{"H" pulse width of PWM signal}}$$

$$\text{(H pulse width of PWM signal)} = \frac{\text{PDUT setting values of the odd channel}}{\text{Count clock frequency of the even channel}}$$

4. Registers

This section provides the register list of the base timer I/O select function.

Base Timer I/O Select Function Registers

Table 4-1 Register List of Base Timer I/O Select Function

Abbreviation	Register Name	Reference
BTSEL0123	I/O Select Register	4.1
BTSEL4567	I/O Select Register	4.2
BTSEL89AB	I/O Select Register	4.3
BTSELCDEF	I/O Select Register	4.4
BTSSSR	Software-based Simultaneous Startup Register	4.5

4.1 I/O Select Register (BTSEL0123)

This register selects the I/O mode for channels 0 to 3 of the base timer.

Register configuration

bit	15	14	13	12	11	10	9	8
Field	SEL23_3	SEL23_2	SEL23_1	SEL23_0	SEL01_3	SEL01_2	SEL01_1	SEL01_0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Register functions

[bit15:12] SEL23_3 to SEL23_0: I/O select bits for Ch.2/Ch.3

bit15	bit14	bit13	bit12	I/O select bits
0	0	0	0	I/O mode 0 (Standard 16-bit timer mode)
0	0	0	1	I/O mode 1 (Timer full mode)
0	0	1	0	I/O mode 2 (Shared external trigger mode)
0	0	1	1	I/O mode 3 (Shared channel signal trigger mode)
0	1	0	0	I/O mode 4 (Timer start/stop mode)
0	1	0	1	I/O mode 5 (Software-based simultaneous startup mode)
0	1	1	0	I/O mode 6 (Software-based startup and timer start/stop mode)
0	1	1	1	I/O mode 7 (Timer start mode)
1	0	0	0	I/O mode 8 (Shared channel signal trigger and timer start/stop mode)
1	0	0	1	I/O mode 9 (Event counter mode)
Others				Setting is prohibited.

[bit11:8] SEL01_3 to SEL01_0: I/O select bits for Ch.0/Ch.1

bit11	bit10	bit9	bit8	I/O select bits
0	0	0	0	I/O mode 0 (Standard 16-bit timer mode)
0	0	0	1	I/O mode 1 (Timer full mode)
0	0	1	0	I/O mode 2 (Shared external trigger mode)
0	0	1	1	I/O mode 3 (Shared channel signal trigger mode)
0	1	0	0	I/O mode 4 (Timer start/stop mode)
0	1	0	1	I/O mode 5 (Software-based simultaneous startup mode)
0	1	1	0	I/O mode 6 (Software-based startup and timer start/stop mode)
0	1	1	1	I/O mode 7 (Timer start mode)
1	0	0	0	I/O mode 8 (Shared channel signal trigger and timer start/stop mode)
1	0	0	1	I/O mode 9 (Event counter mode)
Others				Setting is prohibited.

Notes:

- *Channels 0 and 1 are the lowest channels of the base timer, and cannot use the modes that use signal from lower channels. Therefore, the following modes cannot be selected for the channels:*
- *I/O mode 3 (Shared channel signal trigger mode)*
- *I/O mode 8 (Shared channel signal trigger and timer start/stop mode)*
- *Before rewriting this register, set the base timer to reset mode using the FMD[2:0] bits in the Timer Control Register (TMCR) of the base timer. (Set FMD[2:0] to 0b000.)*
- *I/O mode 9 is equipped for TYP5-M4 and TYP6-M4 products.*
  TYPE1-M4, TYPE2-M4, TYPE3-M4, TYP4-M4 cannot be selected for I/O mode 9.

4.2 I/O Select Register (BTSEL4567)

This register selects the I/O mode for channels 4 to 7 of the base timer.

Register configuration

bit	15	14	13	12	11	10	9	8
Field	SEL67_3	SEL67_2	SEL67_1	SEL67_0	SEL45_3	SEL45_2	SEL45_1	SEL45_0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Register functions

[bit15:12] SEL67_3 to SEL67_0: I/O select bits for Ch.6/Ch.7

bit15	bit14	bit13	bit12	I/O select bits
0	0	0	0	I/O mode 0 (Standard 16-bit timer mode)
0	0	0	1	I/O mode 1 (Timer full mode)
0	0	1	0	I/O mode 2 (Shared external trigger mode)
0	0	1	1	I/O mode 3 (Shared channel signal trigger mode)
0	1	0	0	I/O mode 4 (Timer start/stop mode)
0	1	0	1	I/O mode 5 (Software-based simultaneous startup mode)
0	1	1	0	I/O mode 6 (Software-based startup and timer start/stop mode)
0	1	1	1	I/O mode 7 (Timer start mode)
1	0	0	0	I/O mode 8 (Shared channel signal trigger and timer start/stop mode)
1	0	0	1	I/O mode 9 (Event counter mode)
Others				Setting is prohibited.

[bit11:8] SEL45_3 to SEL45_0: I/O select bits for Ch.4/Ch.5

bit11	bit10	bit9	bit8	I/O select bits
0	0	0	0	I/O mode 0 (Standard 16-bit timer mode)
0	0	0	1	I/O mode 1 (Timer full mode)
0	0	1	0	I/O mode 2 (Shared external trigger mode)
0	0	1	1	I/O mode 3 (Shared channel signal trigger mode)
0	1	0	0	I/O mode 4 (Timer start/stop mode)
0	1	0	1	I/O mode 5 (Software-based simultaneous startup mode)
0	1	1	0	I/O mode 6 (Software-based startup and timer start/stop mode)
0	1	1	1	I/O mode 7 (Timer start mode)
1	0	0	0	I/O mode 8 (Shared channel signal trigger and timer start/stop mode)
1	0	0	1	I/O mode 9 (Event counter mode)
Others				Setting is prohibited.

Notes:

- *Before rewriting this register, set the base timer to reset mode using the FMD[2:0] bits in the Timer Control register (TMCR) of the base timer. (Set FMD[2:0] to 0b000.)*
- *I/O mode 9 is equipped for TYP5-M4 and TYP6-M4 products.*
  TYPE1-M4, TYPE2-M4, TYPE3-M4, TYP4-M4 cannot be selected for I/O mode 9.

4.3 I/O Select Register (BTSEL89AB)

This register selects the I/O mode for channels 8 to 11 of the base timer.

Register configuration

bit	15	14	13	12	11	10	9	8
Field	SELAB_3	SELAB_2	SELAB_1	SELAB_0	SEL89_3	SEL89_2	SEL89_1	SEL89_0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Register functions

[bit15:12] SELAB_3 to SELAB_0: I/O select bits for Ch.10/Ch.11

bit15	bit14	bit13	bit12	I/O select bits
0	0	0	0	I/O mode 0 (Standard 16-bit timer mode)
0	0	0	1	I/O mode 1 (Timer full mode)
0	0	1	0	I/O mode 2 (Shared external trigger mode)
0	0	1	1	I/O mode 3 (Shared channel signal trigger mode)
0	1	0	0	I/O mode 4 (Timer start/stop mode)
0	1	0	1	I/O mode 5 (Software-based simultaneous startup mode)
0	1	1	0	I/O mode 6 (Software-based startup and timer start/stop mode)
0	1	1	1	I/O mode 7 (Timer start mode)
1	0	0	0	I/O mode 8 (Shared channel signal trigger and timer start/stop mode)
1	0	0	1	I/O mode 9 (Event counter mode)
Others				Setting is prohibited.

[bit11:8] SEL89_3 to SEL89_0: I/O select bits for Ch.8/Ch.9

bit11	bit10	bit9	bit8	I/O select bits
0	0	0	0	I/O mode 0 (Standard 16-bit timer mode)
0	0	0	1	I/O mode 1 (Timer full mode)
0	0	1	0	I/O mode 2 (Shared external trigger mode)
0	0	1	1	I/O mode 3 (Shared channel signal trigger mode)
0	1	0	0	I/O mode 4 (Timer start/stop mode)
0	1	0	1	I/O mode 5 (Software-based simultaneous startup mode)
0	1	1	0	I/O mode 6 (Software-based startup and timer start/stop mode)
0	1	1	1	I/O mode 7 (Timer start mode)
1	0	0	0	I/O mode 8 (Shared channel signal trigger and timer start/stop mode)
1	0	0	1	I/O mode 9 (Event counter mode)
Others				Setting is prohibited.

Notes:

- *Before rewriting this register, set the base timer to reset mode using the FMD[2:0] bits in the Timer Control register (TMCR) of the base timer. (Set FMD[2:0] to 0b000.)*
- *I/O mode 9 is equipped for TYP5-M4 and TYP6-M4 products.*
  TYPE1-M4, TYPE2-M4, TYPE3-M4, TYP4-M4 cannot be selected for I/O mode 9.

4.4 I/O Select Register (BTSELCDEF)

This register selects the I/O mode for channels 12 to 15 of the base timer.

Register configuration

bit	15	14	13	12	11	10	9	8
Field	SELEF_3	SELEF_2	SELEF_1	SELEF_0	SELCD_3	SELCD_2	SELCD_1	SELCD_0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Register functions

[bit15:12] SELEF_3 to SELEF_0: I/O select bits for Ch.14/Ch.15

bit15	bit14	bit13	bit12	I/O select bits
0	0	0	0	I/O mode 0 (Standard 16-bit timer mode)
0	0	0	1	I/O mode 1 (Timer full mode)
0	0	1	0	I/O mode 2 (Shared external trigger mode)
0	0	1	1	I/O mode 3 (Shared channel signal trigger mode)
0	1	0	0	I/O mode 4 (Timer start/stop mode)
0	1	0	1	I/O mode 5 (Software-based simultaneous startup mode)
0	1	1	0	I/O mode 6 (Software-based startup and timer start/stop mode)
0	1	1	1	I/O mode 7 (Timer start mode)
1	0	0	0	I/O mode 8 (Shared channel signal trigger and timer start/stop mode)
1	0	0	1	I/O mode 9 (Event counter mode)
Others				Setting is prohibited.

[bit11:8] SELCD_3 to SELCD_0: I/O select bits for Ch.12/Ch.13

bit11	bit10	bit9	bit8	I/O select bits
0	0	0	0	I/O mode 0 (Standard 16-bit timer mode)
0	0	0	1	I/O mode 1 (Timer full mode)
0	0	1	0	I/O mode 2 (Shared external trigger mode)
0	0	1	1	I/O mode 3 (Shared channel signal trigger mode)
0	1	0	0	I/O mode 4 (Timer start/stop mode)
0	1	0	1	I/O mode 5 (Software-based simultaneous startup mode)
0	1	1	0	I/O mode 6 (Software-based startup and timer start/stop mode)
0	1	1	1	I/O mode 7 (Timer start mode)
1	0	0	0	I/O mode 8 (Shared channel signal trigger and timer start/stop mode)
1	0	0	1	I/O mode 9 (Event counter mode)
Others				Setting is prohibited.

Notes:

- *Before rewriting this register, set the base timer to reset mode using the FMD[2:0] bits in the Timer Control register (TMCR) of the base timer. (Set FMD[2:0] to 0b000.)*
- *I/O mode 9 is equipped for TYP5-M4 and TYP6-M4 products.*
  TYPE1-M4, TYPE2-M4, TYPE3-M4, TYP4-M4 cannot be selected for I/O mode 9.

4.5 Software-based Simultaneous Startup Register (BTSSSR)

This register starts up the base timer using software simultaneously.

Up to 16 channels can be started simultaneously if the bits corresponding to the channel are set to "1".

Register configuration

bit	15														0
Field	SSSR15 to SSSR0														
Attribute	W														
Initial value	0xXXXX														

Register functions

[bit15:0] SSSR15 to SSSR0: Software-based simultaneous startup bits

bit	Software-based simultaneous startup bits
0	Writing "0" to these bits is invalid
1	Starts Ch.x of the base timer

x: 15 to 0

Notes:

- *Do not write to this register unless set to either of the following modes:*
- *I/O mode 5 (Software-based simultaneous startup mode)*
- *I/O mode 6 (Software-based startup and timer start/stop mode)(Even channels only)*
- *For the channel started up by using this register, select the rising edge as a trigger input edge using the EGS1 and EGS0 bits in the Timer Control register (TMCR) of the base timer. (Set EGS1 and EGS0 to 0b01.)*

CHAPTER 5-2: Base Timer

This chapter explains the functions and operations of the base timer.

1. Overview of the Base Timer
2. Block Diagram of the Base Timer
3. Operations of the Base Timer
4. 32-bit Mode Operations
5. Base Timer Interrupt
6. Starting the DMA Controller (DMAC)
7. Registers of the Base Timer
8. Notes on using the Base Timer
9. Descriptions of Base Timer Functions

1. Overview of the Base Timer

The function of the base timer can be set to either of the reset mode, 16-bit PWM timer, 16-bit PPG timer, 16/32-bit reload timer, or 16-/32-bit PWC timer using the FMD[2:0] bits in the Timer Control Register (TMCR). The following provides an overview of each selectable timer function.

Relationship between mode settings and timer functions

Settings of FMD[2:0] bits of Timer Control Register (TMCR)	Function
000	Reset mode
001	16-bit PWM timer
010	16-bit PPG timer
011	16/32-bit reload timer
100	16/32-bit PWC timer

Reset Mode

The reset mode is a status where the base timer macros are reset (with each register set to the initial value). Be sure to set this mode before switching to a different timer function or T32 bit setting. However, it is not necessary to set this mode before setting the timer function or T32 bit immediately after the macros are reset.

16-bit PWM Timer

This timer consists of a 16-bit down counter, a 16-bit data register with a cycle set buffer, a 16-bit compare register with a duty set buffer, and a pin controller.

The cycle and duty data is stored in a buffered register and thus can be rewritten while the timer is in operation.

The counter clock of the 16-bit down counter can be selected from eight internal clocks (1, 4, 16, 128, 256, 512, 1024, and 2048 frequency divisions of the machine clock) and three external events (detection of a rising edge, a falling edge, or both).

The one-shot mode, where the counting stops at an underflow, or the continuous mode, where the counting is repeated after reloading, can be selected.

The start event of the 16-bit PWM timer can be selected from a software trigger and three external events (detection of a rising edge, a falling edge, or both).

16-bit PPG Timer

This timer consists of a 16-bit down counter, a 16-bit data register for setting the HIGH width, a 16-bit data register for setting the LOW width, and a pin controller.

The count clock of the 16-bit down counter can be selected from eight internal clocks (1, 4, 16, 128, 256, 512, 1024, and 2048 frequency divisions of the machine clock) and three external events (detection of a rising edge, a falling edge, or both).

The one-shot mode, where the counting stops at an underflow, or the continuous mode, where the counting is repeated after reloading, can be selected.

The start event of the 16-bit PPG timer can be selected from a software trigger and three external events (detection of a rising edge, a falling edge, or both).

16-/32-bit Reload Timer

This timer consists of a 16-bit down counter, a 16-bit reload register, and a pin controller.

The count clock of the 16-bit down counter can be selected from eight internal clocks (1, 4, 16, 128, 256, 512, 1024, and 2048 frequency divisions of the machine clock) and three external events (detection of a rising edge, a falling edge, or both).

The one-shot mode, where the counting stops at an underflow, or the continuous mode, where the counting is repeated after reloading, can be selected.

The start event of the 16/32-bit reload timer can be selected from a software trigger and three external events (detection of a rising edge, a falling edge, or both).

The gate function is provided which execute the down count only at the effective level input from external. The effective level can be selected from two levels (High level or Low level).

16-/32-bit PWC Timer

This timer consists of a 16-bit up counter, a measurement input pin, and a control register.

This timer measures the time between any events using an external pulse input.

The reference count clock can be selected from eight internal clocks (1, 4, 16, 128, 256, 512, 1024, and 2048 frequency divisions).

Measurement modes	HIGH pulse width (↑ to ↓) / LOW pulse width (↓ to ↑) Rising cycle (↑ to ↑) / Falling cycle (↓ to ↓) Edge interval measurement (↑ or ↓ to ↓ or ↑)

An interrupt request can be generated when the measurement is completed.

One-time or continuous measurement can be selected.

2. Block Diagram of the Base Timer

Figure 2-1 to Figure 2-4 show block diagrams of the base timer in each mode.

Figure 2-1 Block Diagram of 16-bit PWM Timer

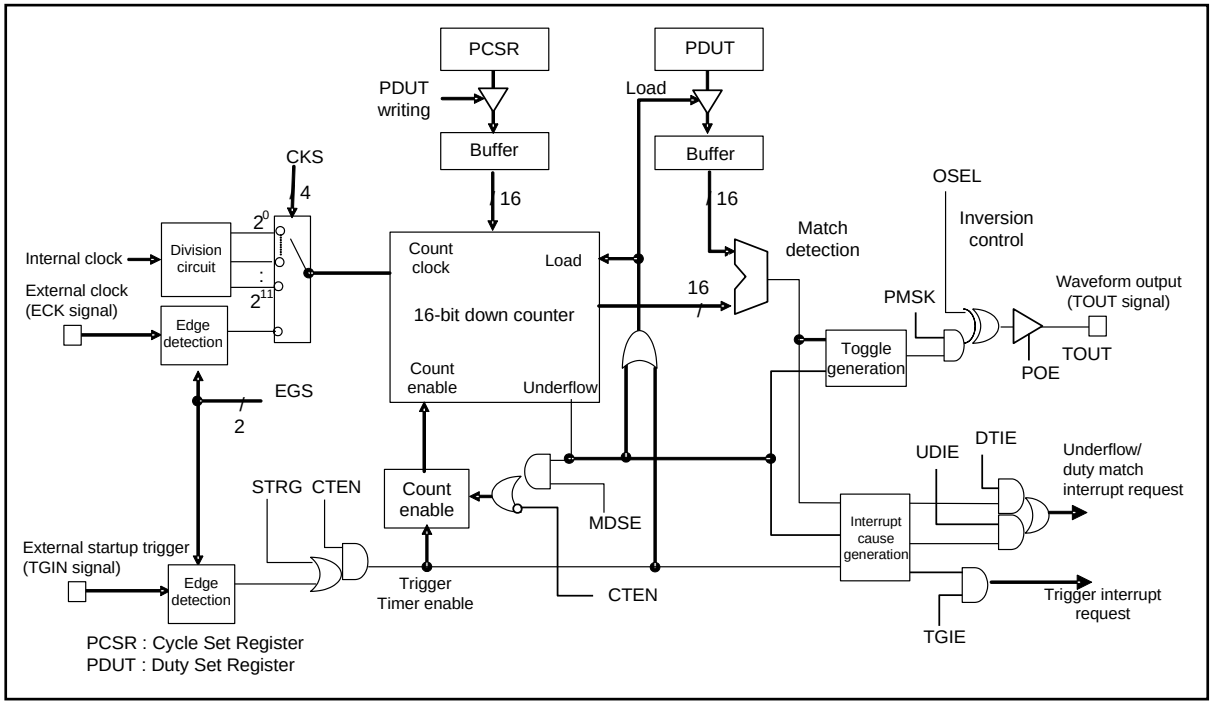


Figure 2-2 Block Diagram of 16-bit PPG Timer

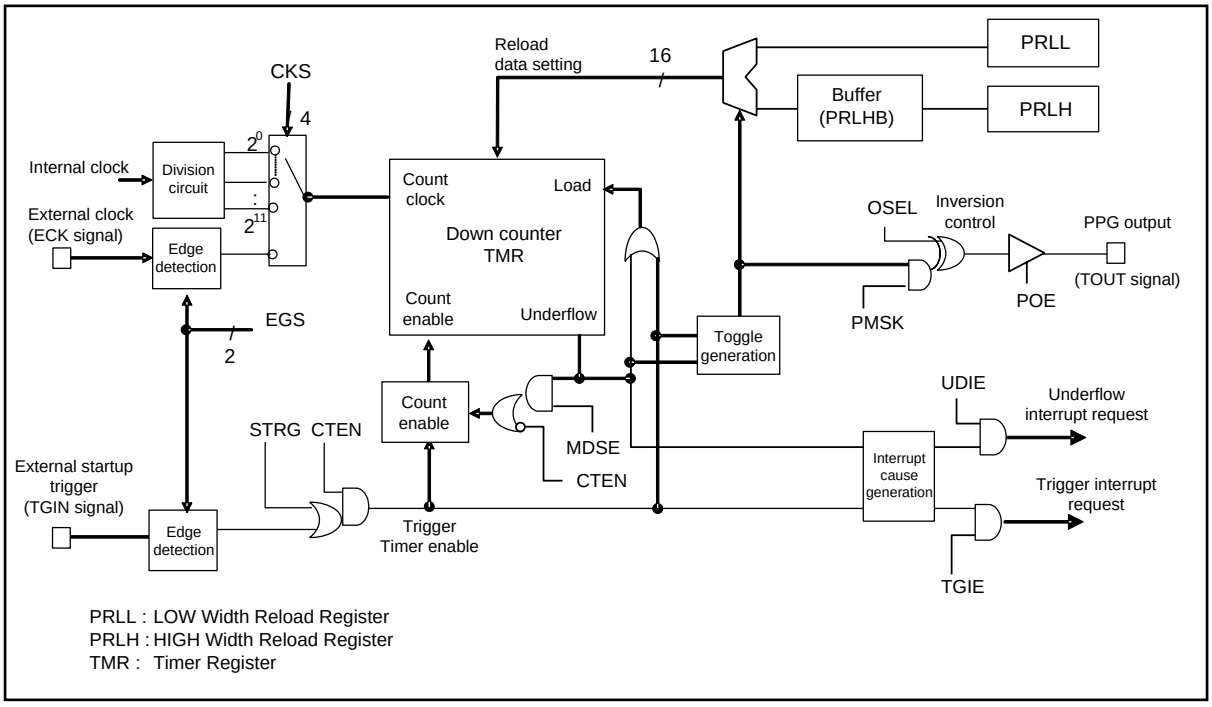
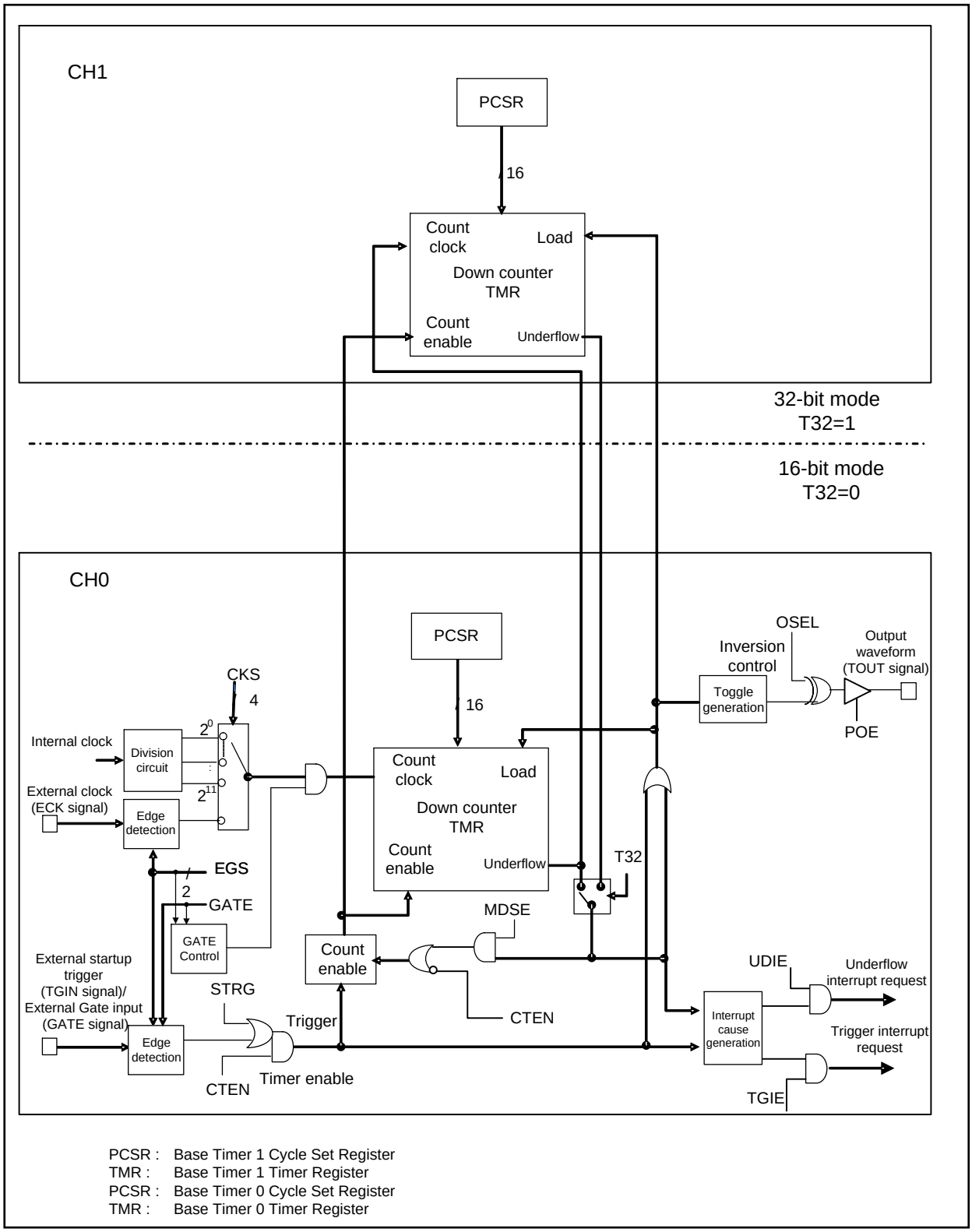
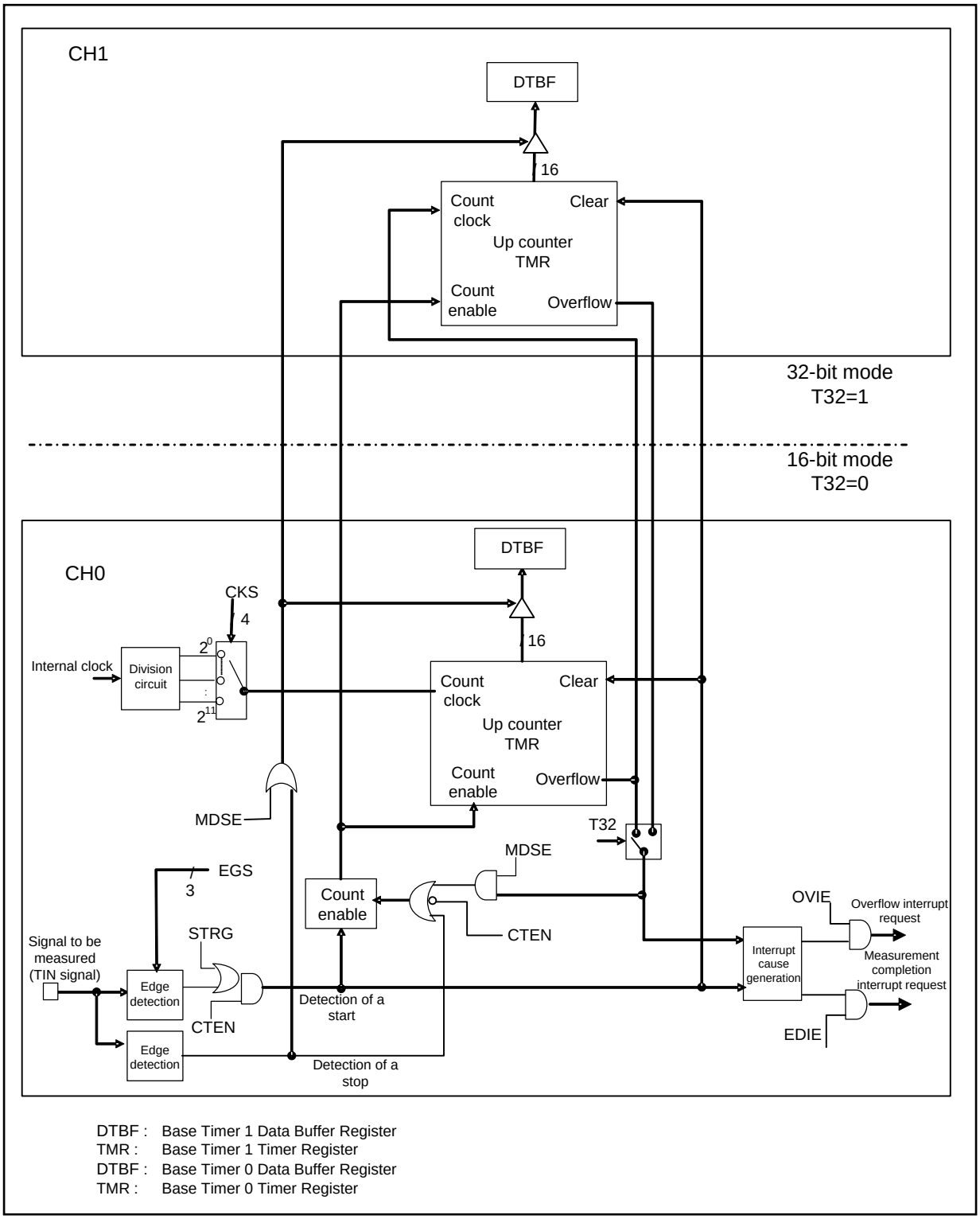


Figure 2-3 Block Diagram of 16-/32-bit Reload Timer (ch.1 and ch.0)



PCSR : Base Timer 1 Cycle Set Register
TMR : Base Timer 1 Timer Register
PCSR : Base Timer 0 Cycle Set Register
TMR : Base Timer 0 Timer Register

Figure 2-4 Block Diagram of 16-/32-bit PWC Timer (ch.1 and ch.0)



3. Operations of the Base Timer

This section explains operations of the base timer.

Operations of the Base Timer

- Reset mode

The reset mode is a status where the base timer macros are reset (with each register set to the initial value). Be sure to set this mode before switching to a different timer function or T32 bit setting. However, it is not necessary to set this mode before setting the timer function or T32 bit immediately after the macros are reset. In a 32-bit mode, setting this mode for the even channel also resets the odd channel. It is not necessary to set the reset mode for the odd channel.

- 16-bit PWM timer

When triggered, the 16-bit PWM timer starts decrementing from the cycle set value. First, it outputs a LOW level pulse. When the 16-bit down counter matches the value set in the PWM Duty Set Register, the output inverts to the HIGH level. Then, the output inverts again to the LOW level when a counter underflow occurs. This can generate waveforms with any cycle and duty.

- 16-bit PPG timer

When triggered, the 16-bit PPG timer starts decrementing from the value set in the LOW Width Reload Register. First, it outputs a LOW level pulse. The output inverts to the HIGH level upon an underflow. Then, it starts decrementing from the value set in the HIGH Width Reload Register. The output inverts to the LOW level when an underflow occurs. This can generate waveforms having any LOW and HIGH widths.

- 16-bit reload timer

When triggered, the 16-bit reload timer starts decrementing from the cycle set value. When an underflow occurs on the 16-bit down counter, an interrupt flag is set. The output is either the toggle output where the level inverts according to the MDSE bit setting as an underflow occurs or the pulse output where the level is HIGH at the start of counting and LOW at the occurrence of an underflow.

- 32-bit reload timer

This timer has the same basic operations as the 16-bit reload timer. However, it uses two channels, even and odd, to operate as a 32-bit reload timer. The even channel operates as a lower 16-bit timer and the odd channel as an upper 16-bit timer. The interrupt control and output waveform control are defined by the settings for the even channel only. When setting the cycle, first write it in the upper register (odd channel) and then in the lower register (even channel).

When reading the timer value, read it from the lower register (even channel) and then from the upper channel (odd channel).

- 16-bit PWC timer

The PWC timer starts the 16-bit up counter with input of the specified measurement start edge and stops the counter with detection of a measurement end edge. The value counted in between is stored as a pulse width in the data buffer register.

- 32-bit PWC timer

This timer has the same basic operations as the 16-bit PWC timer. However, it uses two channels, even and odd, to operate as a 32-bit PWC timer. The even channel operates as a lower 16-bit counter and the odd channel as an upper 16-bit counter. The interrupt control is defined by the settings for the even channel only. When reading the measured or count value, read it from the lower register (even channel) and then from the upper channel (odd channel).

4. 32-bit Mode Operations

Using two channels, the reload timer and PWC provide 32-bit mode operations. This section explains the basic functions and operations of the 32-bit mode functions.

32-bit Mode Functions

This function enables the operations of a 32-bit data reload timer or 32-bit data PWC timer by combining two channels of base timers. Since the upper 16-bit timer counter value in the odd channel is read together with the lower 16-bit timer counter value in the even channel, the timer counter value can be read during operation.

32-bit Mode Settings

First, set "0b000" to set the reset mode to reset the status of the FMD[2:0] bits in the TMCR register of the even channel. Then, as carried out for in 16-bit mode, select the reload or PWC timer and set the operation. By writing 1 also to the T32 bit in the TMCR register, the 32-bit operation mode is set. Do not change 0 for the T32 bit in the odd channel. It is also not necessary to set it to reset mode. For the reload timer, set the reload value of the upper 16 of 32 bits in the PWM Cycle Set Register of the odd channel. Then, set the reload value of the lower 16 bits in the PWM Cycle Set Register of the even channel.

Because transition to 32-bit operation mode is reflected immediately after the T32 bit is written, stop the counting before changing the settings in each channel.

To change from 32-bit mode to 16-bit mode, set it to reset mode by setting "0b000" for the FMD[2:0] bits in the TMCR register of the even channel. This resets the status of both even and odd channels, enabling settings in 16-bit mode in each channel.

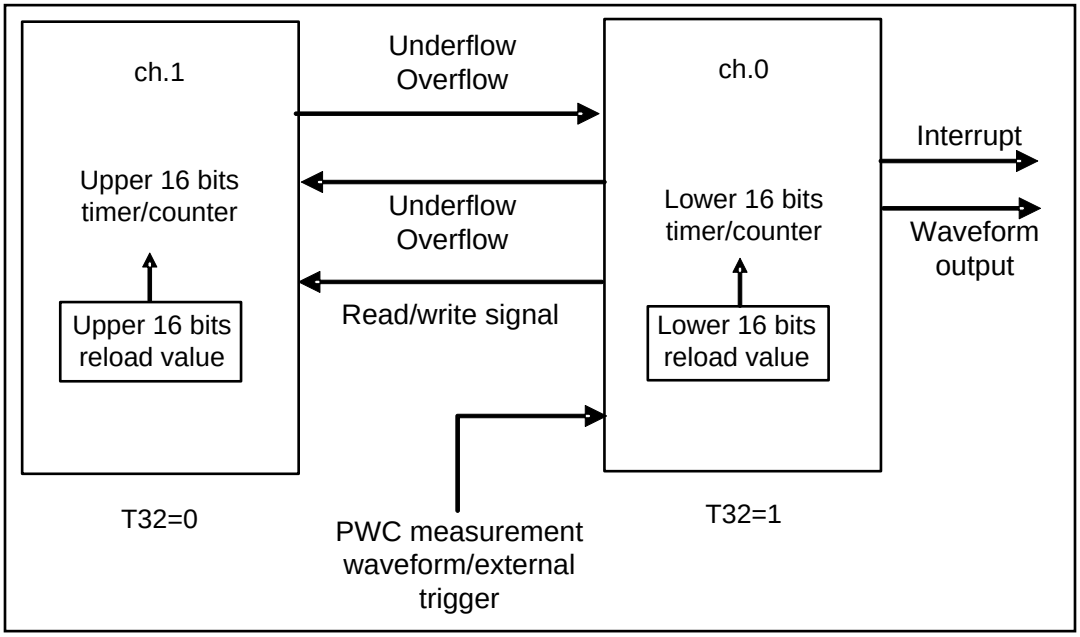
32-bit Mode Operations

After transition to 32-bit mode, if the reload or PWC timer is started by control of the even channel, the timer/counter in the even channel operates with the lower 16 bits. Also, the time/counter in the odd channel operates with the upper 16 bits.

The operations in 32-bit mode are defined by the settings for the even channel. For this reason, the settings for the odd channel (except the Cycle Set Register for the reload timer) are ignored. For the timer start, waveform output, and interrupt signal functions, settings for the even channel are also applied (the odd channel is masked and fixed to LOW).

Figure 4-1 shows the configuration of ch.0 and ch.1.

Figure 4-1 Configuration of 32-bit Operations (for ch.0 and ch.1)



5. Base Timer Interrupt

This section provides a list of interrupt request flags, interrupt enable bits, and interrupt factors for each function of the base timer.

Interrupt Control Bits and Interrupt Factors for Each Function

Table 5-1 shows the interrupt control bits and interrupt factors for each function.

Table 5-1 Interrupt Control Bits and Interrupt Factors in Each Mode

	Status Control Register (STC)			
	Interrupt Request Flag Bit	**Interrupt Request Enable Bit**	**Interrupt Factors**	**Interrupt Factor Output Signal**
PWM timer function (16-bit PWM timer)	UDIR: bit0	UDIE: bit4	Detection of an underflow	IRQ0
	DTIR: bit1	DTIE: bit5	Detection of a match in duty	
	TGIR: bit2	TGIE: bit6	Detection of a timer start trigger	IRQ1
PPG timer function (16-bit PPG timer)	UDIR: bit0	UDIE: bit4	Detection of an underflow	IRQ0
	TGIR: bit2	TGIE: bit6	Detection of a timer start trigger	IRQ1
Reload timer function (16-/32-bit Reload timer)	UDIR: bit0	UDIE: bit4	Detection of an underflow	IRQ0
	TGIR: bit2	TGIE: bit6	Detection of a timer start trigger	IRQ1
PWC timer function (16-/32-bit PWC timer)	OVIR: bit0	OVIE: bit4	Detection of an overflow	IRQ0
	EDIR: bit2	EDIE: bit6	Detection of the completion of measurement	IRQ1

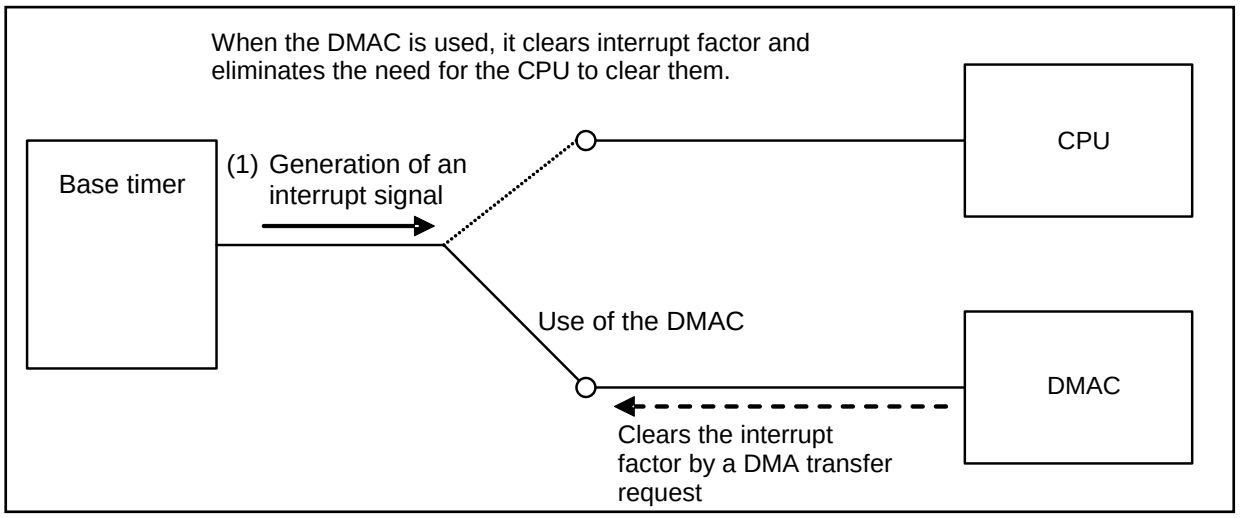
6. Starting the DMA Controller (DMAC)

The DMAC can be started using the generation of an interrupt factors by the base timer.

DMA Transfer Operation Using Interrupt Factors of the Base Timer

The DMAC can be started using the generation of an interrupt factor by the base timer. Figure 6-1 gives an overview of starting the DMAC using the base timer.

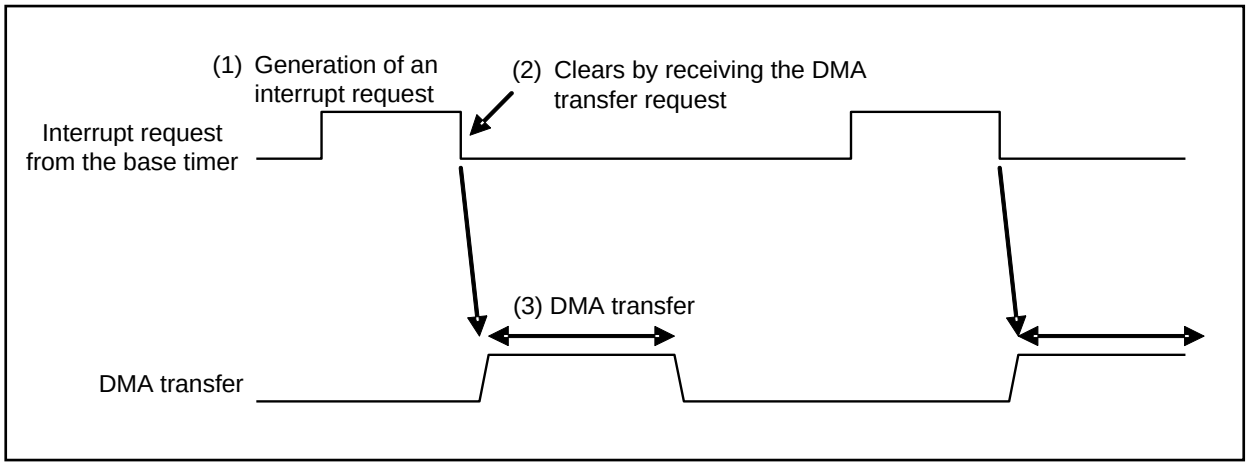
Figure 6-1 Overview of Starting the DMAC Using the Base Timer



Before starting the DMAC using the base timer, configure the DMAC. For settings details on the DMAC, see Chapters DMAC and Interrupt in Peripheral Manual.

Figure 6-2 gives an example of a DMA transfer operation using an interrupt request by the base timer.

Figure 6-2 Example of DMA transfer operation



7. Registers of the Base Timer

This section provides register lists of the base timer in each mode.

List of Registers Used When the 16-bit PWM Timer Is Selected

Table 7-1 List of Registers Used When the 16-bit PWM Timer Is Selected

Abbreviation	Register Name	Reference
TMCR	Timer Control Register	9.1.6
TMCR2	Timer Control Register 2	9.1.6
STC	Status Control Register	9.1.6
PCSR	PWM Cycle Set Register	9.1.7
PDUT	PWM Duty Set Register	9.1.8
TMR	Timer Register	9.1.9

List of Registers Used When the 16-bit PPG Timer Is Selected

Table 7-2 List of Registers Used When the 16-bit PPG Timer Is Selected

Abbreviation	Register Name	Reference
TMCR	Timer Control Register	9.2.6
TMCR2	Timer Control Register 2	9.2.6
STC	Status Control Register	9.2.6
PRLL	LOW Width Reload Register	9.2.7
PRLH	HIGH Width Reload Register	9.2.8
TMR	Timer Register	9.2.9

List of Registers Used When the Reload Timer is Selected

Table 7-3 List of Registers Used When the Reload Timer Is Selected

Abbreviation	Register Name	Reference
TMCR	Timer Control Register	9.3.3
TMCR2	Timer Control Register 2	9.3.3
STC	Status Control Register	9.3.3
PCSR	PWM Cycle Set Register	9.3.4
TMR	Timer Register	9.3.5

List of Registers Used When the PWC Timer Is Selected

Table 7-4 List of Registers Used When the PWC Timer Is Selected

Abbreviation	Register Name	Reference
TMCR	Timer Control Register	9.4.2
TMCR2	Timer Control Register 2	9.4.2
STC	Status Control Register	9.4.2
DTBF	Data Buffer Register	9.4.3

8. Notes on using the Base Timer

This section provides notes on using the base timer.

Notes on Setting the Program Common to Each Timer

- It is prohibited to rewrite the following bits in the TMCR2 and TMCR registers during operation. Rewriting of the bits must be performed before starting or after stopping the operation.

[TMCR2 bit8], [TMCR bit14:12]	CKS3 to CKS0 : Clock selection bits
[bit10:8]	EGS2, EGS1, EGS0 : Measurement edge selection bits
[bit7]	T32 : 32-bit timer selection bit (When the reload timer PWC function is selected)
[bit6:4]	FMD[2:0] : Timer function selection bits
[bit2]	MDSE : Measurement mode (one-shot/continuous) selection bit

- When the FMD[2:0] bits in the TMCR register are set to reset mode with "0b000", all registers of the base timer are initialized. Therefore, all registers must be set again.
- When the FMD[2:0] bits in the TMCR register are set to reset mode with "0b000", settings for the bits other than the FMD[2:0] bits in the TMCR register are ignored and initialized.

Notes on Using the 16-bit PWM/PPG/Reload Timer

- If the interrupt request flag set timing coincides the clear timing, the flag set operation takes precedence and the clear operation is not performed.
- If the load timing and count timing of the down counter coincide, the load operation takes precedence.
- Set the timer function with the FMD[2:0] bits in the TMCR register, and then set the cycle, duty, HIGH width, and LOW width.
- In one-shot mode, if a restart is detected at the end of counting, the count value is reloaded and the restart operation is started.

Notes on Using the PWC Timer

- If the count start enable bit (CTEN) is set to 1, the counter is cleared. As the result, the data existed in the counter before the start is enabled becomes invalid.
- If the setting for PWC mode (FMD[2:0] = 100) and the setting for starting measurement (CTEN = 1) are performed simultaneously in system reset/reset mode, the resultant operation may depend on the status of the last measurement signal.
- In continuous measurement mode, if a measurement start edge is detected at the same time a restart is set, the counting is started immediately from "0x0001".
- If a restart is performed after the count operation has been started, the following operations may occur depending on the timing.
- If it coincides with a measurement end edge in pulse width one-shot measurement mode:
  The timer is restarted and waits for detection of a measurement start edge. However, a measurement end flag (EDIR) is set.
- If it coincides with a measurement end edge in pulse width continuous measurement mode:
  The timer is restarted and waits for detection of a measurement start edge. However, a measurement end flag (EDIR) is set and the measurement result at the time is transferred to the DTBF.

When restarting the timer during operation, pay attention to flag operations as described above and use the interrupt control.

9. Descriptions of Base Timer Functions

This section explains each function of the base timer.

Base Timer Functions

9.1. PWM Timer Function
9.2. PPG Timer Function
9.3. Reload Timer Function
9.4. PWC Timer Function

9.1 PWM Timer Function

The function of the base timer can be set to either the 16-bit PWM timer, 16-bit PPG timer, 16-/32-bit reload timer, or 16-/32-bit PWC timer using the FMD[2:0] bits in the Timer Control Register. This section explains the timer functions available when PWM is set.

9.1.1. 16-bit PWM Timer Operations

9.1.2. One-shot Operation

9.1.3. Interrupt Factors and Timing Chart

9.1.4. Output Waveforms

9.1.5. PWM Timer Operation Flowchart

9.1.6. Timer Control Registers (TMCR and TMCR2) and Status Control Register (STC) used when the PWM Timer is selected

9.1.7. PWM Cycle Set Register (PCSR)

9.1.8. PWM Duty Set Register (PDUT)

9.1.9. Timer Register (TMR)

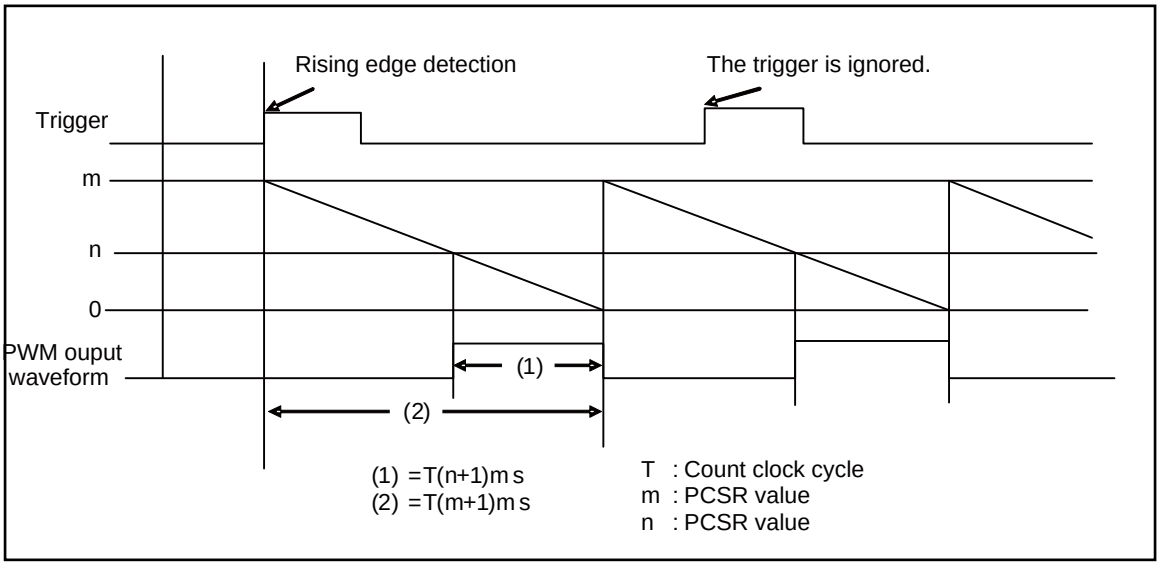
9.1.1 16-bit PWM Timer Operations

In PWM timer operations, waveforms in the specified cycle from the detection of a trigger can be output in one-shot or continuously. The cycle of the output pulse can be controlled by changing the PCSR value. The duty ratio can be controlled by changing the PDUT value. After writing data to the PCSR, be sure to write it to the PDUT.

Continuous Operation

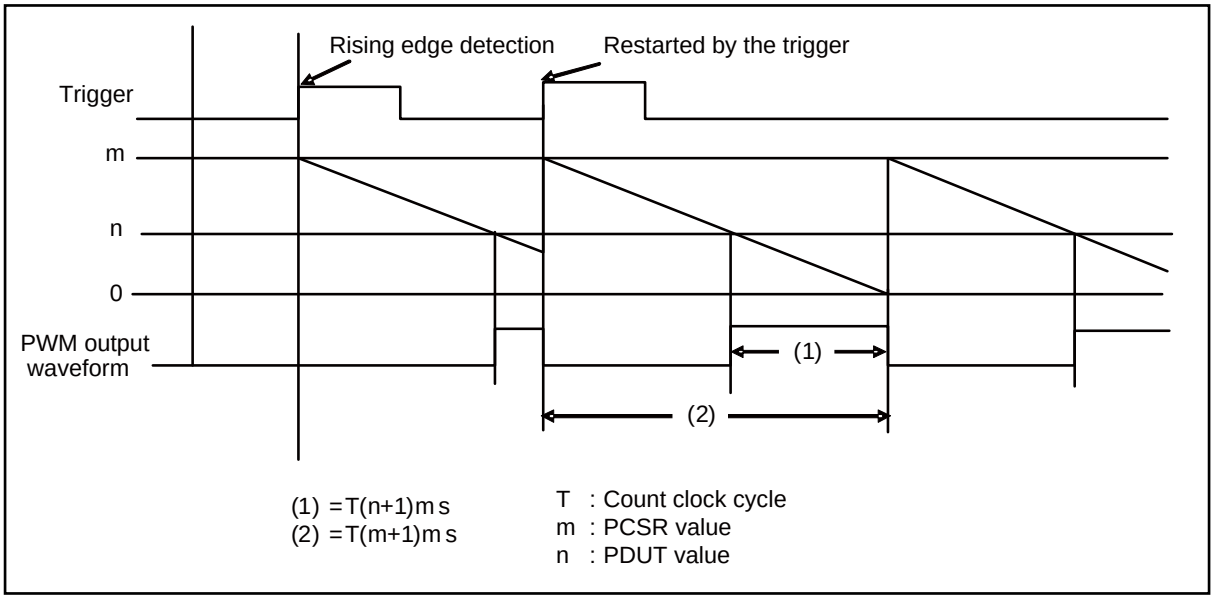
- When a restart is disabled (RTGEN = 0)

Figure 9-1 PWM Operation Timing Chart (When a Restart Is Disabled)



- When a restart is enabled (RTGEN = 1)

Figure 9-2 PWM Operation Timing Chart (When a Restart Is Enabled)



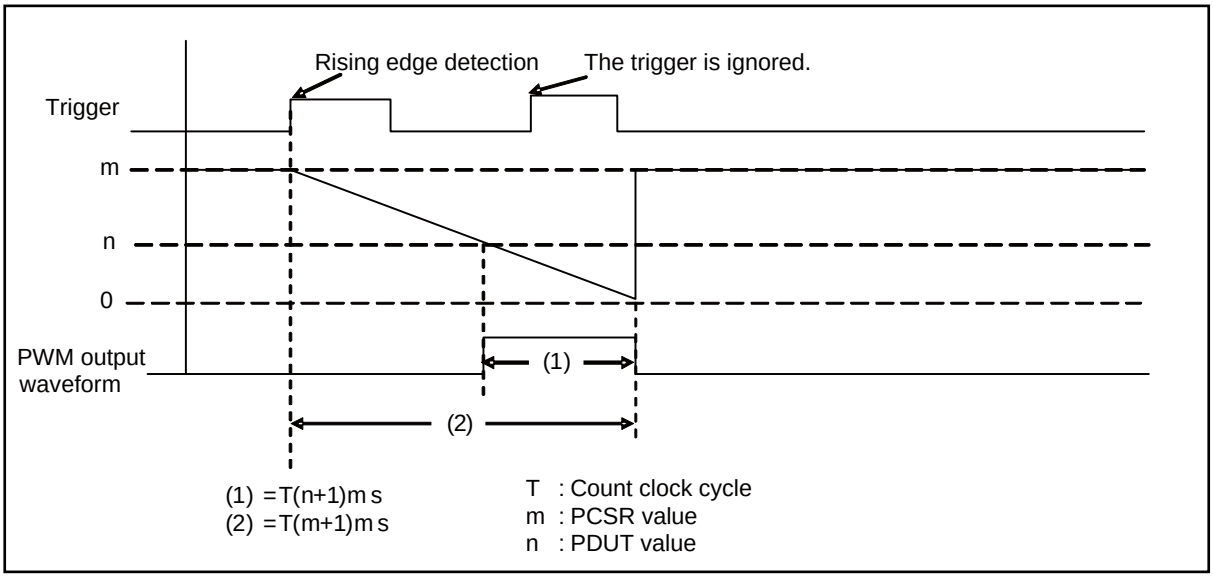
9.1.2 One-shot Operation

In one-shot operation, a single pulse of any width can be output using a trigger. When a restart is enabled, the counter is reloaded when an edge is detected during operation.

One-shot Operation

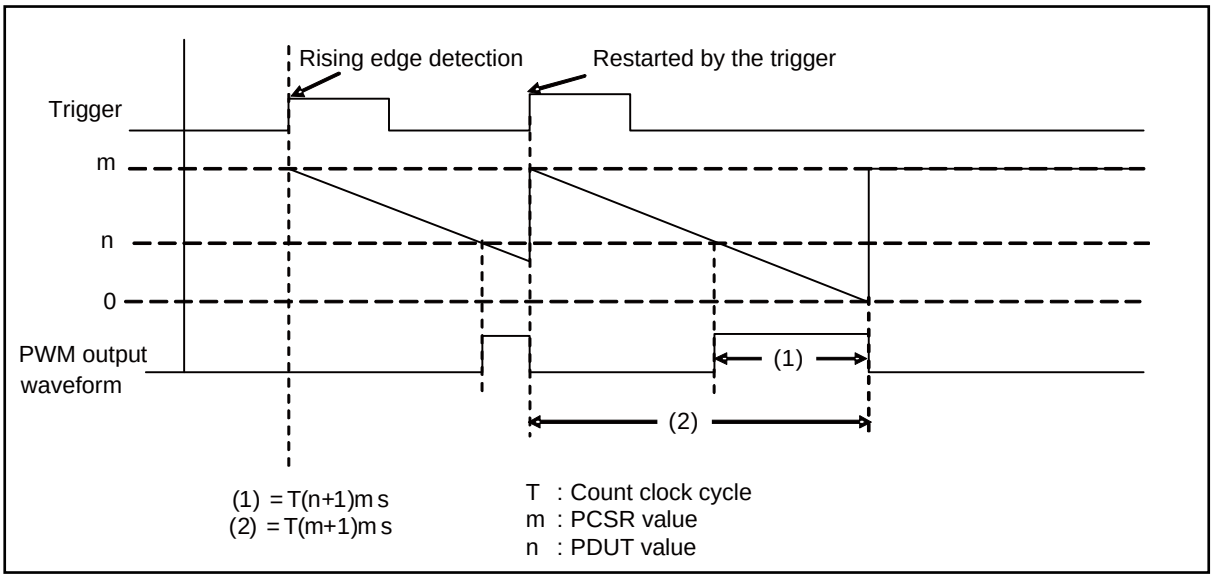
■ When a restart is disabled (RTGEN = 0)

Figure 9-3 One-shot Operation Timing Chart (Trigger Restart Is Disabled)



■ When a restart is enabled (RTGEN = 1)

Figure 9-4 One-shot Operation Timing Chart (Trigger Restart Is Enabled)



9.1.3 Interrupt Factors and Timing Chart

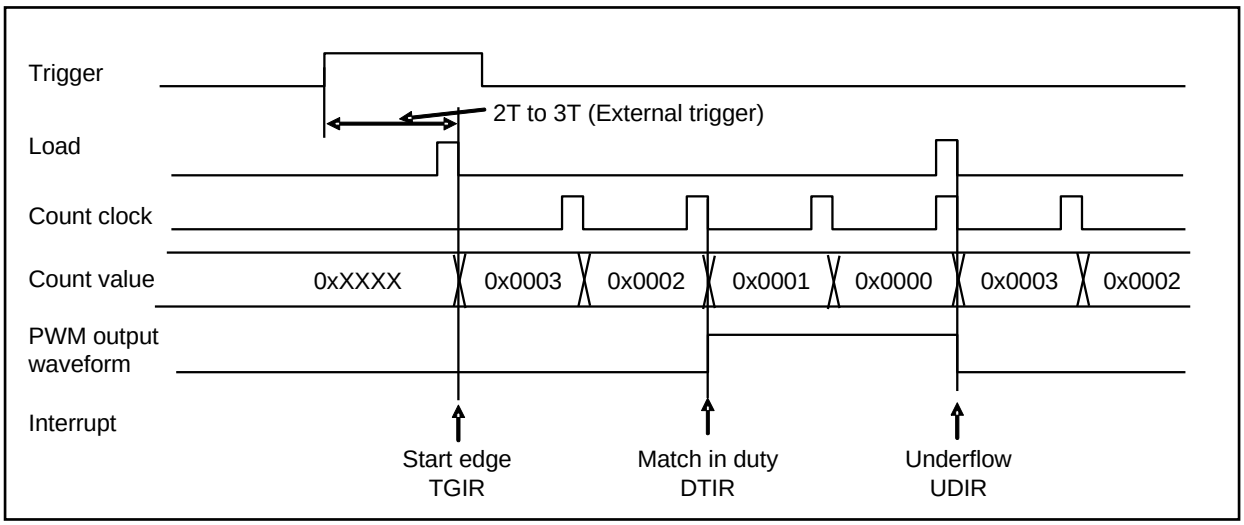
This section explains interrupt factors and a timing chart.

Interrupt Factors and Timing Chart (PWM Output: Normal Polarity)

As a time from trigger input to loading of the counter value, T is required for software triggering or 2T to 3T (T: machine cycle) for external triggering.

Figure 9-5 shows the interrupt factors and a timing chart where the cycle set value = 3 and duty value = 1.

Figure 9-5 Interrupt Factors and Timing Chart of the PWM Timer



9.1.4 Output Waveforms

This section explains the PWM output.

How to make an all-LOW or all-HIGH PWM output

Figure 9-6 shows how to make all-LOW PWM output and Figure 9-7 shows how to make all-HIGH output.

Figure 9-6 Example of Outputting All-LOW Level Waveforms as PWM Output

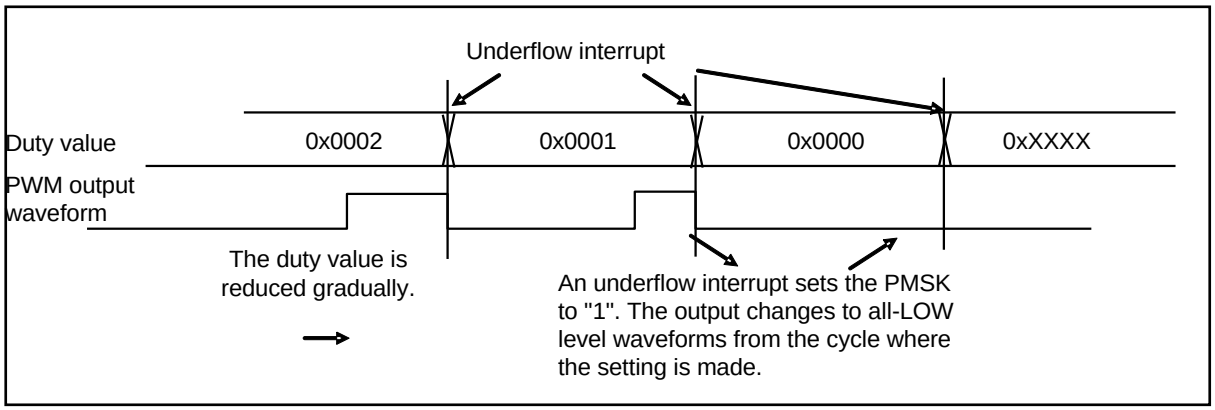
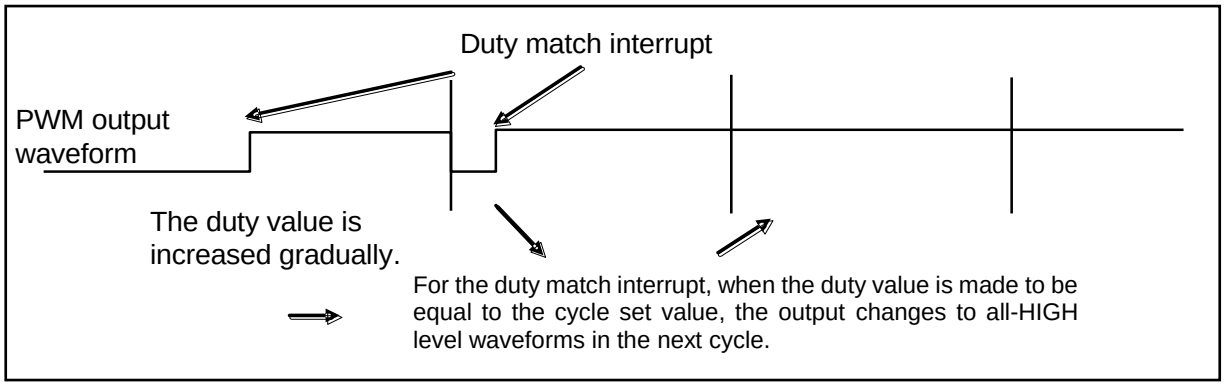


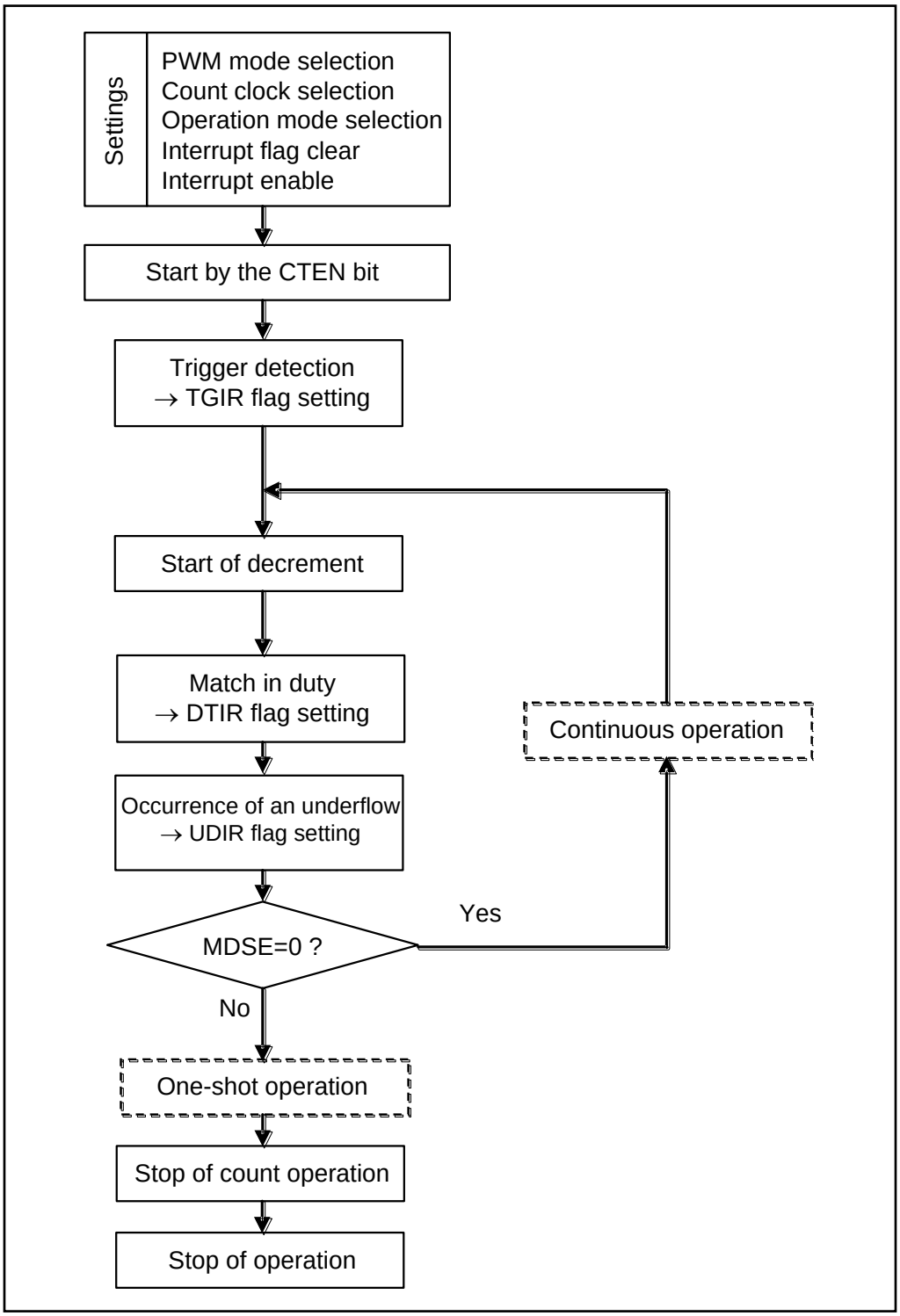
Figure 9-7 Example of Outputting All-HIGH Level Waveforms as PWM Output



9.1.5 PWM Timer Operation Flowchart

This section provides an operation flowchart of the PWM timer.

PWM Timer Operation Flowchart



9.1.6 Timer Control Registers (TMCR and TMCR2) and Status Control Register (STC) used when the PWM Timer is selected

The Timer Control Register (TMCR) controls the PWM timer. Note that some bits cannot be rewritten while the PWM timer is in operation.

Timer Control Register (Upper bytes of TMCR)

bit	15	14	13	12	11	10	9	8
Field	Reserved	CKS2	CKS1	CKS0	RTGEN	PMSK	EGS1	EGS0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit15] Reserved: Reserved bit

The read value is 0.

Set 0 to this bit.

[bit14:12, TMCR2:bit8] CKS3 to CKS0: Count clock selection bits

- Select the count clock for the 16-bit down counter.
- Changes to the count clock setting are applied immediately. For this reason, changes to CKS3 through CKS0 must be made when the counting is stopped (CTEN = 0). However, it is possible to make changes at the same time you set 1 to the Count Operation enable bit (CTEN).

CKS3	CKS2	CKS1	CKS0	Description
0	0	0	0	ϕ
0	0	0	1	ϕ /4
0	0	1	0	ϕ /16
0	0	1	1	ϕ /128
0	1	0	0	ϕ /256
0	1	0	1	External clock (rising edge event)
0	1	1	0	External clock (falling edge event)
0	1	1	1	External clock (both edge event)
1	0	0	0	ϕ /512
1	0	0	1	ϕ /1024
1	0	1	0	ϕ /2048
Values other than the above				Setting is prohibited.

[bit11] RTGEN: Restart enable bit

This bit enables restart by a software trigger or trigger input.

bit	Description
0	Restart disabled
1	Restart enabled

[bit10] PMSK: Pulse output mask bit

- This bit controls the output level of PWM output waveforms.
- When this bit is set to 0, PWM waveforms are output as they are.
- When this bit is set to 1, the PWM output is masked with LOW output regardless of the cycle and duty set values.

bit	Description
0	Normal output
1	Fixed to LOW output

Note:

- *When Output polarity specification bit (OSEL) of Timer Control Register (Lower bytes of TMCR) is set to inverted output, setting PMSK bit to 1 masks the output with HIGH.*

[bit9:8] EGS1, EGS0: Trigger input edge selection bits

- These bits select a valid edge for input waveforms as an external start cause and set the trigger condition.
- When the initial value or 0b00 is set, the timer is not started by external waveforms because the setting means that no valid edge is selected for input waveforms.
- Changes to EGS1 or EGS0 must be made when the counting is stopped (CTEN = "0"). However, it is possible to make changes at the same time you set 1 to the CTEN bit.

Note:

bit9	bit8	Description
0	0	Trigger input disabled
0	1	Rising edge
1	0	Falling edge
1	1	Both edges

- *If the STRG bit is set to 1, software triggering is enabled regardless of the EGS1 and EGS0 settings.*

Timer Control Register (Lower bytes of TMCR)

bit	7	6	5	4	3	2	1	0
Field	Reserved	FMD2	FMD1	FMD0	OSEL	MDSE	CTEN	STRG
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7] Reserved: Reserved bit

The read value is 0.

Set 0 to this bit.

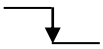
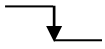
[bit6:4] FMD2 to FMD0: Timer function selection bits

- These bits select the timer function.
- When the FMD[2:0] bits are set to 0b001, the PWM function is selected.
- Changes must be made while the timer is stopped (CTEN = 0). However, it is possible to make changes at the same time you set 1 to the CTEN bit.

bit6	bit5	bit4	Description
0	0	0	Reset mode
0	0	1	16-bit PWM timer
0	1	0	16-bit PPG timer
0	1	1	16/32-bit reload timer
1	0	0	16/32-bit PWC timer
1	0	1	Setting is prohibited.
1	1	0	
1	1	1	

[bit3] OSEL: Output polarity specification bit

- This bit sets the polarity of the PWM output.

Polarity	After reset	Match in duty	Underflow
Normal	LOW output		
Inverted	HIGH output		

bit	Description
0	Normal polarity
1	Inverted polarity

[bit2] MDSE: Mode selection bit

- This bit selects continuous pulse output or one-shot pulse output.
- Changes must be made while the timer is stopped (CTEN = 0). However, it is possible to make changes at the same time you set 1 to the CTEN bit.

bit	Description
0	Continuous operation
1	One-shot operation

[bit1] CTEN: Count operation enable bit

- This bit enables the operation of the down counter.
- When the counter is in operation enabled status (the CTEN bit is 1), writing 0 to this bit stops the counter.

bit	Description
0	Stop
1	Operation enabled

Note:

- *By writing 0 to CTEN bit, the output waveform becomes Low.*

[bit0] STRG: Software trigger bit

- When the CTEN bit is 1, writing 1 to the STRG bit enables software triggering.
- The read value of the STRG bit is always 0.

bit	Description
0	Invalid
1	Start triggered by software

Notes:

- *Software triggering is also enabled when 1 is written to the CTEN and STRG bits simultaneously.*
- *If the STRG bit is set to 1, software triggering is enabled regardless of the EGS1 and EGS0 settings.*

Timer Control Register 2 (TMCR2)

bit	15	14	13	12	11	10	9	8
Field	Reserved							CKS3
Attribute				R/W				R/W
Initial value				0000000				0

Note:

- *This register is placed above the STC register.*

[bit15:9] Reserved: Reserved bits

The read value is 0.
Set 0 to these bits.

[bit8] CKS3: Count clock selection bit

See [bit14:12, TMCR2:bit8] CKS3 to CKS0: Count clock selection bit in 9.1.6 Timer Control Registers (TMCR and TMCR2) and Status Control Register (STC) used when the PWM Timer is selected.

Status Control Register (STC)

bit	7	6	5	4	3	2	1	0
Field	Reserved	TGIE	DTIE	UDIE	Reserved	TGIR	DTIR	UDIR
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Note:

- *The TMCR2 register is placed in the upper bytes of this register.*

[bit7] Reserved: Reserved bit

The read value is 0.

Set 0 to this bit.

[bit6] TGIE: Trigger interrupt request enable bit

- This bit controls interrupt requests of bit2 TGIR.
- When the TGIE bit is enabled, setting bit2 TGIR generates an interrupt request to the CPU.

bit	Description
0	Disables interrupt requests.
1	Enables interrupt requests.

[bit5] DTIE: Duty match interrupt request enable bit

- This bit controls interrupt requests of bit1 DTIR.
- When the DTIE bit is enabled, setting bit1 DTIR generates an interrupt request to the CPU.

bit	Description
0	Disables interrupt requests.
1	Enables interrupt requests.

[bit4] UDIE: Underflow interrupt request enable bit

- This bit controls interrupt requests of bit0 UDIR.
- When the UDIE bit is enabled, setting bit0 UDIR generates an interrupt request to the CPU.

bit	Description
0	Disables interrupt requests.
1	Enables interrupt requests.

[bit3] Reserved: Reserved bit

The read value is 0.

Set 0 to this bit.

[bit2] TGIR: Trigger interrupt request bit

- When a software trigger or trigger input is detected, the TGIR bit is set to 1.
- The TGIR bit is cleared by writing 0.
- Even if 1 is written to the TGIR bit, the bit value is not affected.
- The read value of read-modify-write instructions is 1 regardless of the bit value.

bit	Description
0	Clears an interrupt factor.
1	Detects an interrupt factor.

[bit1] DTIR: Duty match interrupt request bit

- When the count value matches the duty set value, the DTIR bit is set to 1.
- The DTIR bit is cleared by writing 0.
- Even if 1 is written to the DTIR bit, the bit value is not affected.
- The read value of read-modify-write instructions is 1 regardless of the bit value.

bit	Description
0	Clears an interrupt factor.
1	Detects an interrupt factor.

[bit0] UDIR: Underflow interrupt request bit

- When a count value underflow from 0x0000 to 0xFFFF occurs, the UDIR bit is set to 1.
- The UDIR bit is cleared by writing 0.
- Even if 1 is written to the UDIR bit, the bit value is not affected.
- The read value of read-modify-write instructions is 1 regardless of the bit value.

bit	Description
0	Clears an interrupt factor.
1	Detects an interrupt factor.

9.1.7 PWM Cycle Set Register (PCSR)

The PWM Cycle Set Register (PCSR) is a buffered register for setting the cycle. Transfer to the Timer Register is performed at startup and underflow.

bit	15	0
Field	PCSR[15:0]	
Attribute	R/W	
Initial value	0xXXXX	

This is a buffered register for setting the cycle. Transfer to the Timer Register is performed at startup and underflow.

When initializing or rewriting the PWM Cycle Set register, be sure to perform writing to the PWM Duty Set Register after performing writing to the PWM Cycle Set register.

- Do not access the PCSR register with 8-bit data.
- Set the cycle for the PCSR register after setting the PWM function using the FMD[2:0] bits in the TMCR register.

9.1.8 PWM Duty Set Register (PDUT)

The PWM Duty Set Register (PDUT) is a buffered register for setting the duty. Transfer from the buffer is performed at an underflow.

bit	15	0
Field	PDUT[15:0]	
Attribute	R/W	
Initial value	0xXXXX	

This is a buffered register for setting the duty. Transfer from the buffer is performed at an underflow.

When the cycle set register value is set equal to the duty set register value, an all-HIGH pulse is output under normal polarity and an all-LOW pulse is output under inverted polarity.

Do not set a value that makes PCSR < PDUT. The PWM output becomes undefined.

- Do not access the PDUT register with 8-bit data.
- Set the duty for the PDUT register after setting the PWM function using the FMD[2:0] bits in the TMCR register.

9.1.9 Timer Register (TMR)

The Timer Register (TMR) reads the value of the 16-bit down counter.

bit	15	0
Field	TMR[15:0]	
Attribute	R	
Initial value	0x0000	

The value of the 16-bit down counter is read.

- Do not access the TMR register with 8-bit data.

9.2 PPG Timer Function

The function of the base timer can be set to either the 16-bit PWM timer, 16-bit PPG timer, 16-/32-bit reload timer, or 16-/32-bit PWC timer using the FMD[2:0] bits in the Timer Control Register. This section explains the timer functions available when PPG is set.

9.2.1. 16-bit PPG Timer Operations

9.2.2. Continuous Operation

9.2.3. One-shot Operation

9.2.4. Interrupt Factors and Timing Chart

9.2.5. PPG Timer Operation Flowchart

9.2.6. Timer Control Registers (TMCR and TMCR2) and Status Control Register (STC) used when the PPG Timer is selected

9.2.7. LOW Width Reload Register (PRLL)

9.2.8. HIGH Width Reload Register (PRLH)

9.2.9. Timer Register (TMR)

9.2.1 16-bit PPG Timer Operations

In PPG timer operations, any output pulse can be controlled by setting the LOW and HIGH widths of the pulse in respective reload registers.

Overview of Operations

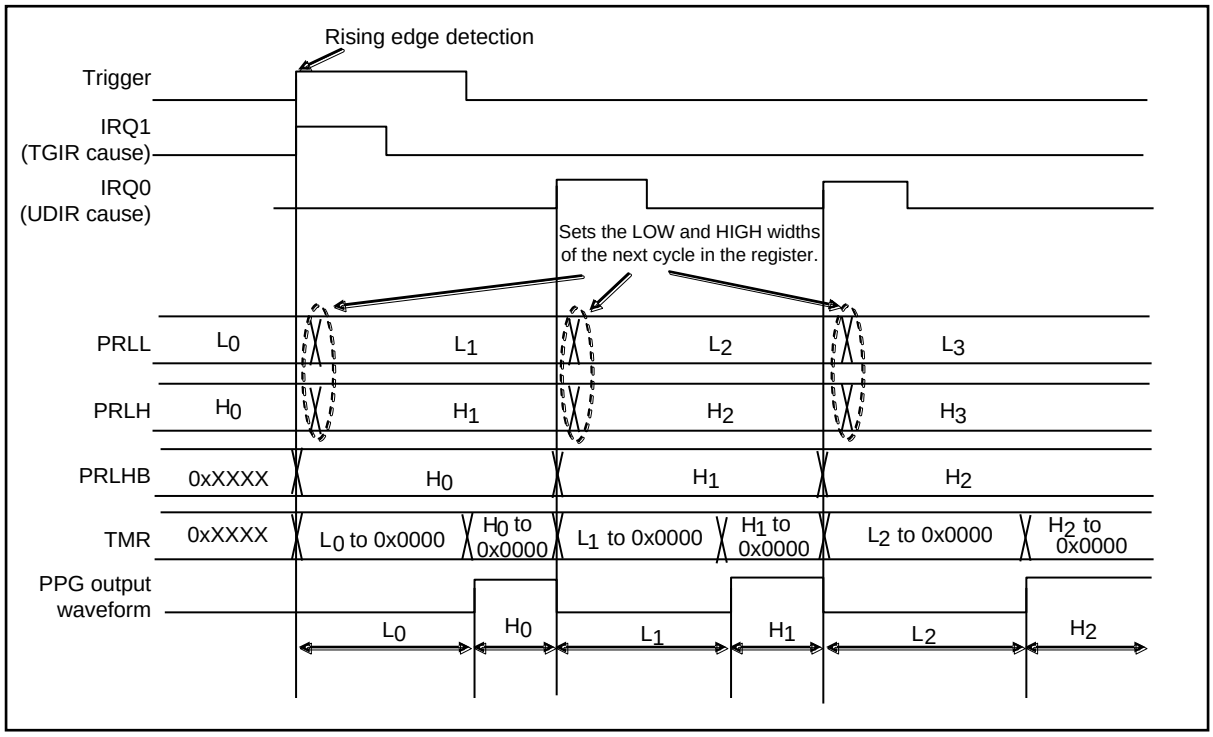
Two 16-bit reload registers for setting the LOW and HIGH widths, respectively, and one buffer for setting the HIGH width are used (PRLL, PRLH, and PRLHB).

A start trigger initially causes the PRLL set value to be loaded to the 16-bit down counter and, at the same time, the PRLH set value to be transferred to the PRLHB. The PPG timer changes the output level to LOW and counts down for every count clock. Upon detection of an underflow, the PPG timer reloads the PRLHB value to the counter, inverts the PPG output waveforms, and continues to count down. At the next detection of an underflow, it inverts the PPG output waveforms, reloads the PRLL set value to the counter, and transfers the PRLH set value to the PRLHB.

This operation causes the output waveform to be pulse output having LOW and HIGH widths corresponding to the values in the respective reload registers.

Timing of Writing to the Reload Registers

Data writing to the PRLL and PRLH reload registers occurs upon detection of a start trigger and during the period from when an underflow interrupt factor (UDIR) is set to when the next cycle starts. The data set here is used as the setting for the next cycle. The items of data set in the PRLL and PRLH are automatically transferred to the TMR and PRLHB, respectively, when a start trigger is detected and when an underflow occurs at the completion of HIGH width counting. The data transferred to the PRLHB is automatically reloaded to the TMR when an underflow occurs at the completion of LOW width counting.



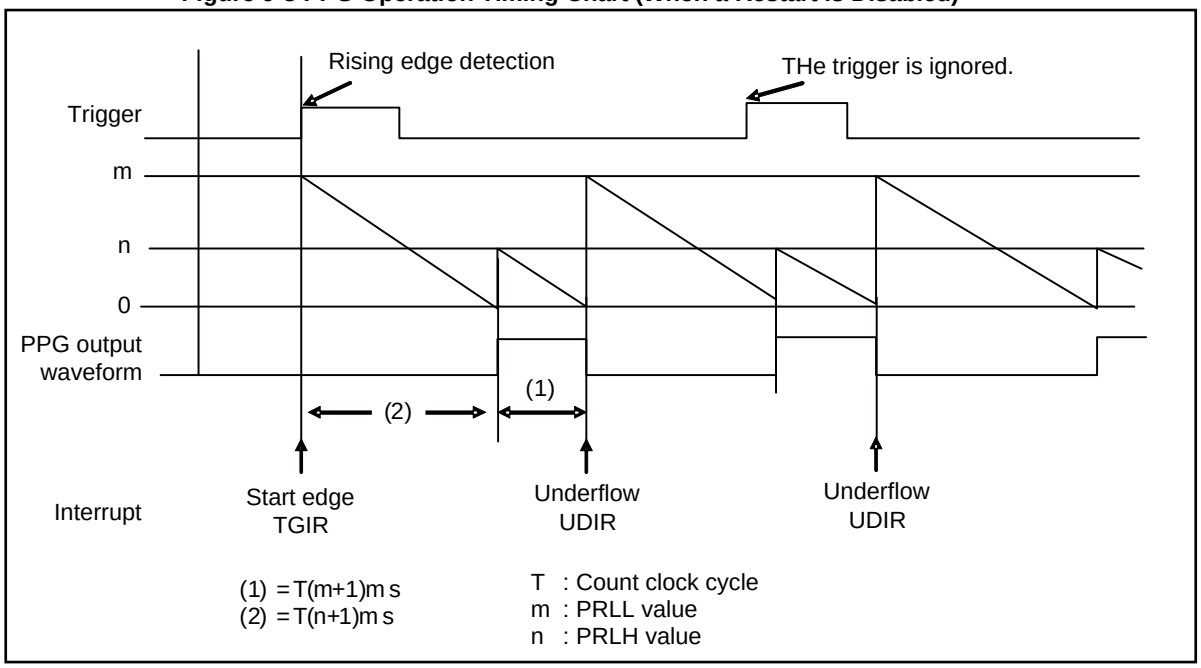
9.2.2 Continuous Operation

In continuous operations, any pulse can be output continuously by updating the LOW and HIGH widths at the set timing of each interrupt factor. When a restart is enabled, the counter is reloaded when an edge is detected during operation.

Continuous Operation

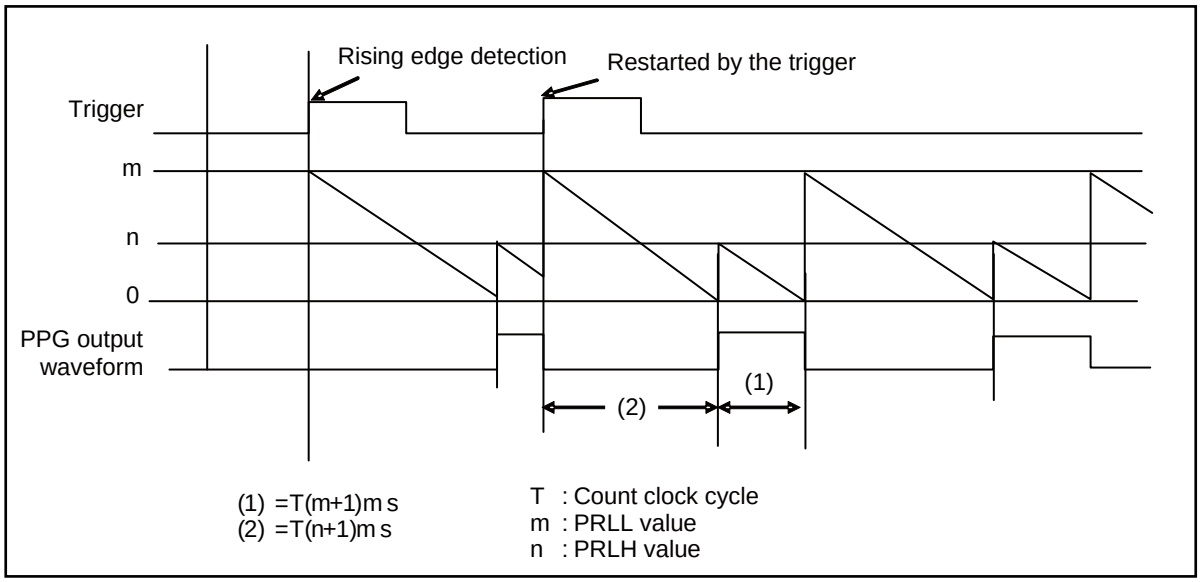
■ When a restart is disabled (RTGEN = 0)

Figure 9-8 PPG Operation Timing Chart (When a Restart is Disabled)



■ When a restart is enabled (RTGEN = 1)

Figure 9-9 PPG Operation Timing Chart (When a Restart is Enabled)



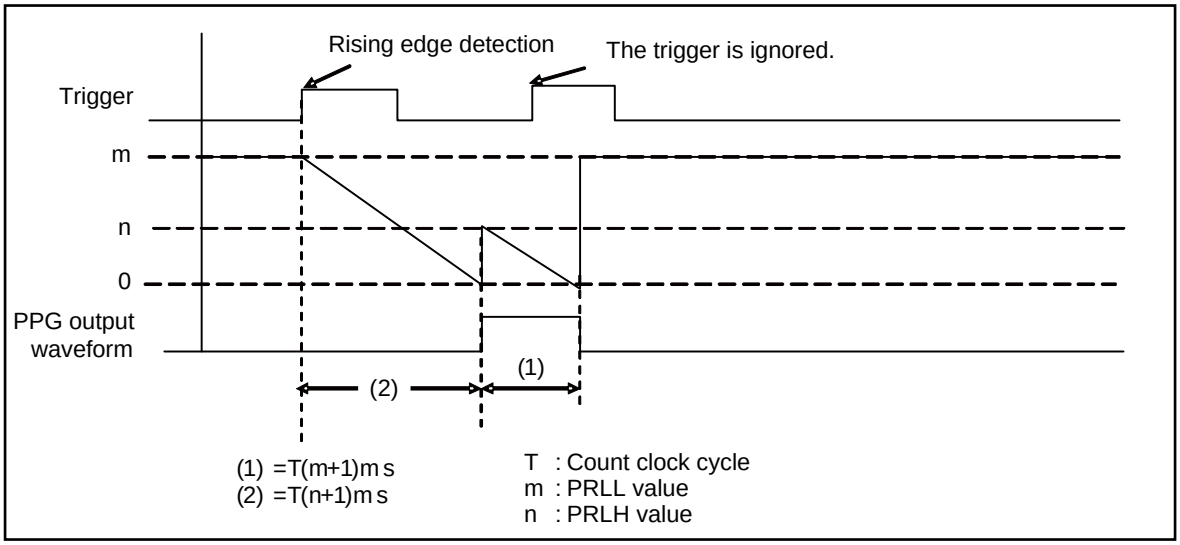
9.2.3 One-shot Operation

In one-shot operation, a single pulse of any width can be output using a trigger. When a restart is enabled, the counter is reloaded when an edge is detected during operation.

One-shot Operation

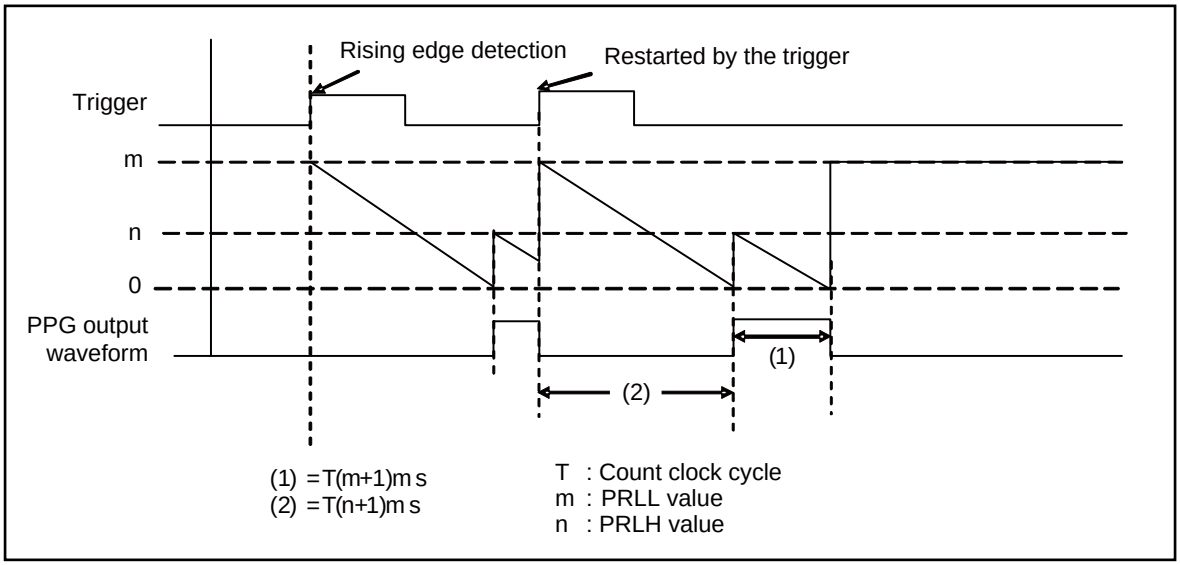
- When a restart is disabled (RTGEN = 0)

Figure 9-10 One-shot Operation Timing Chart (Trigger Restart is Disabled)



- When a restart is enabled (RTGEN = 1)

Figure 9-11 One-shot Operation Timing Chart (Trigger Restart is Enabled)



Relationship between Reload Value and Pulse Width

The output pulse width is equal to the 16-bit reload register value added by 1, and which is multiplied by the count clock cycle. Therefore, when the reload register value is "0x0000", the pulse width is equal to one count clock cycle. When the reload register value is 0xFFFF, the pulse width is equal to 65536 count clock cycle. The pulse width calculation formulas are as follows:

PL = T × (L + 1)	PL:	Width of LOW pulse
PH = T × (H + 1)	PH:	Width of HIGH pulse
	T:	Count clock cycle
	L:	PRLL value
	H:	PRLH value

9.2.4 Interrupt Factors and Timing Chart

This section explains interrupt factors and a timing chart.

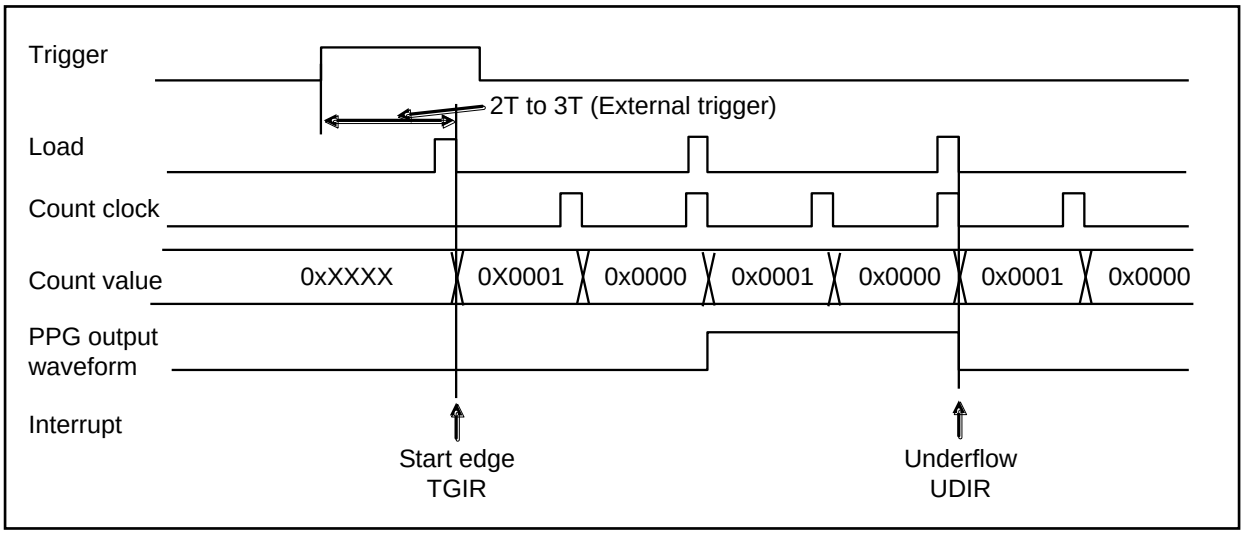
Interrupt Factors and Timing Chart (PPG Output: Normal Polarity)

As a time from trigger input to loading of the counter value, T is required for software triggering or 2T to 3T (T: machine cycle) for external triggering.

Interrupt factors are set to detection of a PPG start trigger and an underflow in HIGH level output.

Figure 9-12 shows the interrupt factors and a timing chart where LOW width set value = 1 and HIGH width set value = 1.

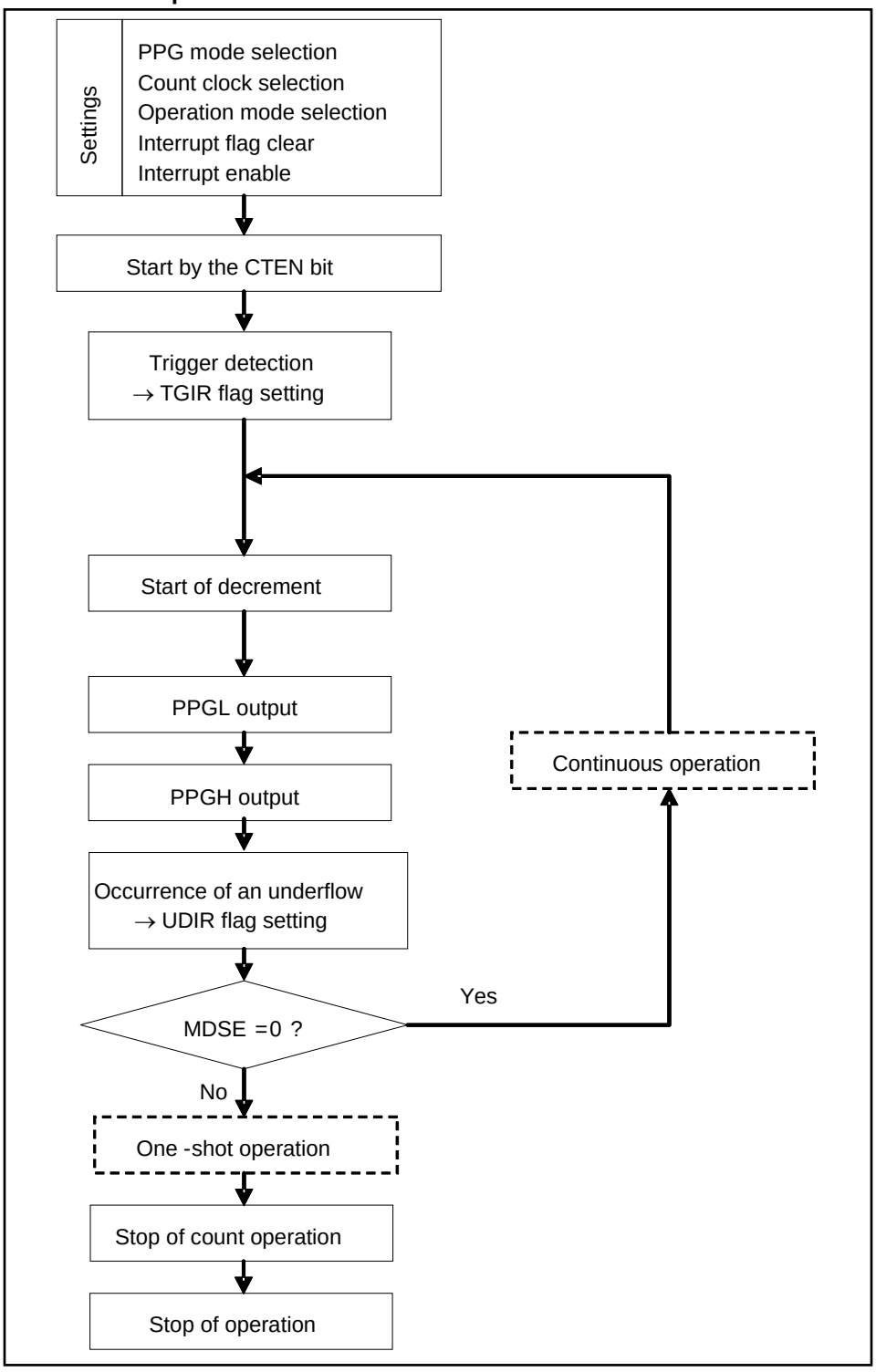
Figure 9-12 Interrupt Factors and Timing Chart of the PPG Timer



9.2.5 PPG Timer Operation Flowchart

This section provides an operation flowchart of the PPG timer.

PPG Timer Operation Flowchart



9.2.6 Timer Control Registers (TMCR and TMCR2) and Status Control Register (STC) used when the PPG Timer is selected

The Timer Control Register (TMCR) controls the PPG timer. Note that some bits cannot be rewritten while the PPG timer is in operation.

Timer Control Register (Upper bytes of TMCR)

bit	15	14	13	12	11	10	9	8
Field	Reserved	CKS2	CKS1	CKS0	RTGEN	PMSK	EGS1	EGS0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit15] Reserved: Reserved bit

The read value is 0.

Set 0 to this bit.

[bit14:12, TMCR2: bit 8] CKS3 to CKS0: Count clock selection bits

- Select the count clock for the 16-bit down counter.
- Changes to the count clock setting are applied immediately. For this reason, changes to CKS3 through CKS0 must be made when the counting is stopped (CTEN = 0). However, it is possible to make changes at the same time you set 1 to the CTEN bit.

CKS3	CKS2	CKS1	CKS0	Description
0	0	0	0	ϕ
0	0	0	1	ϕ /4
0	0	1	0	ϕ /16
0	0	1	1	ϕ /128
0	1	0	0	ϕ /256
0	1	0	1	External clock (rising edge event)
0	1	1	0	External clock (falling edge event)
0	1	1	1	External clock (both edge event)
1	0	0	0	ϕ /512
1	0	0	1	ϕ /1024
1	0	1	0	ϕ /2048
Others				Setting is prohibited.

[bit11] RTGEN: Restart enable bit

This bit enables restart by a software trigger or trigger input.

bit	Description
0	Restart disabled
1	Restart enabled

[bit10] PMSK: Pulse output mask bit

- This bit controls the output level of PPG output waveforms.
- When this bit is set to 0, PPG waveforms are output as they are.
- When this bit is set to 1, the PPG output is masked with LOW output regardless of the cycle and duty set values.

bit	Description
0	Normal output
1	Fixed to LOW output

Note:

- *When OSEL in bit3 is set to inverted output, setting PMSK to 1 masks the output with HIGH.*

[bit9:8] EGS1, EGS0: Trigger input edge selection bits

- These bits select a valid edge for input waveforms as an external start cause and set the trigger condition.
- When the initial value or 0b00 is set, the timer is not started by external waveforms because the setting means that no valid edge is selected for input waveforms.
- Changes to EGS1 or EGS0 must be made when the counting is stopped (CTEN = 0). However, it is possible to make changes at the same time you set 1 to the CTEN bit.

bit9	bit8	Description
0	0	Trigger input disabled
0	1	Rising edge
1	0	Falling edge
1	1	Both edges

Note:

- *If the STRG bit is set to 1, software triggering is enabled regardless of the EGS1 and EGS0 settings.*

Timer Control Register (Lower bytes of TMCR)

bit	7	6	5	4	3	2	1	0
Field	Reserved	FMD2	FMD1	FMD0	OSEL	MDSE	CTEN	STRG
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7] Reserved: Reserved bit

The read value is 0.

Set 0 to this bit.

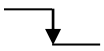
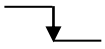
[bit6:4] FMD2 to FMD0: Timer function selection bits

- These bits select the timer function.
- When the FMD[2:0] bits are set to 0b010, the PPG function is selected.
- Changes must be made while the timer is stopped (CTEN = 0). However, it is possible to make changes at the same time you set 1 to the CTEN bit.

bit6	bit5	bit4	Description
0	0	0	Reset mode
0	0	1	Selection of the PWM function
0	1	0	Selection of the PPG function
0	1	1	Selection of the reload timer function
1	0	0	Selection of the PWC function
1	0	1	Setting is prohibited.
1	1	0	
1	1	1	

[bit3] OSEL: Output polarity specification bit

This bit sets the polarity of the PPG output.

Polarity	After reset	Completion of LOW width counting	Completion of HIGH width counting
Normal	LOW output		
Inverted	HIGH output		

bit	Description
0	Normal polarity
1	Inverted polarity

[bit2] MDSE: Mode selection bit

- This bit selects continuous pulse output or one-shot pulse output.
- Changes must be made while the timer is stopped (CTEN = 0). However, it is possible to make changes at the same time you set 1 to the CTEN bit.

bit	Description
0	Continuous operation
1	One-shot operation

[bit1] CTEN: Count operation enable bit

- This bit enables the operation of the down counter.
- When the counter is in operation enabled status (the CTEN bit is 1), writing 0 to this bit stops the counter.

bit	Description
0	Stop
1	Operation enabled

Note:

- *By writing "0" to CTEN bit, the output waveform becomes Low.*

[bit0] STRG: Software trigger bit

- When the CTEN bit is 1, writing 1 to the STRG bit enables software triggering.
- The read value of the STRG bit is always 0.

bit	Description
0	Invalid
1	Start triggered by software

Notes:

- *Software triggering is also enabled when 1 is written to the CTEN and STRG bits simultaneously.*
- *If the STRG bit is set to 1, software triggering is enabled regardless of the EGS1 and EGS0 settings.*

Timer Control Register 2 (Upper bytes of TMCR2)

bit	15	14	13	12	11	10	9	8
Field	Reserved							CKS3
Attribute	R/W							R/W
Initial value	0000000							0

Note:

- *This register is placed above the STC register.*

[bit15:9] Reserved: Reserved bits

The read value is 0.
Set 0 to these bits.

[bit8] CKS3: Count clock selection bit

See [bit14:12, TMCR2: bit 8] CKS3 to CKS0: Count clock selection bit in 9.2.6 Timer Control Registers (TMCR and TMCR2) and Status Control Register (STC) used when the PPG Timer is selected.

Status Control Register (STC)

bit	7	6	5	4	3	2	1	0
Field	Reserved	TGIE	Reserved	UDIE	Reserved	TGIR	Reserved	UDIR
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Note:

- *The TMCR2 register is placed in the upper bytes of this register.*

[bit7] Reserved: Reserved bit

The read value is 0.

Set 0 to this bit.

[bit6] TGIE: Trigger interrupt request enable bit

- This bit controls interrupt requests of bit2 TGIR.
- When the TGIE bit is enabled, setting bit2 TGIR generates an interrupt request to the CPU.

bit	Description
0	Disables interrupt requests.
1	Enables interrupt requests.

[bit5] Reserved: Reserved bit

The read value is 0.

Set 0 to this bit.

[bit4] UDIE: Underflow interrupt request enable bit

- This bit controls interrupt requests of bit0 UDIR.
- When the UDIE bit is enabled, setting bit0 UDIR generates an interrupt request to the CPU.

bit	Description
0	Disables interrupt requests.
1	Enables interrupt requests.

[bit3] Reserved: Reserved bit

The read value is 0.

Set 0 to this bit.

[bit2] TGIR: Trigger interrupt request bit

- When a software trigger or trigger input is detected, the TGIR bit is set to 1.
- The TGIR bit is cleared by writing 0.
- Even if 1 is written to the TGIR bit, the bit value is not affected.
- The read value of read-modify-write instructions is 1 regardless of the bit value.

bit	Description
0	Clears an interrupt factor.
1	Detects an interrupt factor.

[bit1] Reserved: Reserved bit

The read value is 0.

Set 0 to this bit.

[bit0] UDIR: Underflow interrupt request bit

- When a count value underflow from 0x0000 to 0xFFFF occurs during counting from the value for which the HIGH width is set, the UDIR bit is set to 1.
- The UDIR bit is cleared by writing 0.
- Even if 1 is written to the UDIR bit, the bit value is not affected.
- The read value of read-modify-write instructions is 1 regardless of the bit value.

bit	Description
0	Clears an interrupt factor.
1	Detects an interrupt factor.

9.2.7 LOW Width Reload Register (PRLL)

The LOW Width Reload Register (PRLL) is a register used to set the LOW width of PPG output waveforms. Transfer to the Timer Register is performed at detection of a start trigger or at an underflow after the completion of HIGH width counting.

bit	15	0
Field	PRLL[15:0]	
Attribute	R/W	
Initial value	0xXXXX	

This register is used to set the LOW width of PPG output waveforms. Transfer to the Timer Register is performed at detection of a start trigger and at an underflow at the completion of HIGH width counting.

- Do not access the PRLL register with 8-bit data.
- Set the LOW width for the PRLL register after setting the PPG function using the FMD[2:0] bits in the TMCR register.

9.2.8 HIGH Width Reload Register (PRLH)

The HIGH Width Reload Register (PRLH) is a buffered register used to set the HIGH width of PPG output waveforms. Transfer from the PRLH to the buffer register is performed at detection of a start trigger and at an underflow after the completion of HIGH width counting. Transfer from the buffer register to the Timer Register is performed at an underflow at the completion of LOW width counting.

bit	15	0
Field	PRLH[15:0]	
Attribute	R/W	
Initial value	0xXXXX	

This register is used to set the HIGH width of PPG output waveforms. Transfer from the PRLH to the buffer register is performed at detection of a start trigger and at an underflow at the completion of HIGH width counting. Transfer from the buffer register to the Timer Register is performed at an underflow at the completion of LOW width counting.

- Do not access the PRLH register with 8-bit data.
- Set the HIGH width for the PRLH register after setting the PPG function using the FMD[2:0] bits in the TMCR register.

9.2.9 Timer Register (TMR)

The Timer Register (TMR) reads the value of the 16-bit down counter.

bit	15	0
Field	TMR[15:0]	
Attribute	R	
Initial value	0x0000	

The value of the 16-bit down counter is read.

- Do not access the TMR register with 8-bit data.

9.3 Reload Timer Function

The function of the base timer can be set to either the 16-bit PWM timer, 16-bit PPG timer, 16/32-bit reload timer, or 16/32-bit PWC timer using the FMD[2:0] bits in the Timer Control Register. This section explains the timer functions available when the reload timer is set.

9.3.1. Operations of the 16-bit Reload Timer

9.3.2. Reload Timer Operation Flowchart

9.3.3. Timer Control Registers (TMCR and TMCR2) and Status Control Register (STC) used when the Reload Timer is selected

9.3.4. Cycle Set Register (PCSR)

9.3.5. Timer Register (TMR)

9.3.1 Operations of the 16-bit Reload Timer

In reload timer operations, countdown is performed from the value set in the PWM Cycle Set Register in synchronization with the count clock. This operation continues until the count value reaches 0 or the cycle setting is loaded automatically to stop the countdown.

Count Operation Performed When the Internal Clock Is Selected

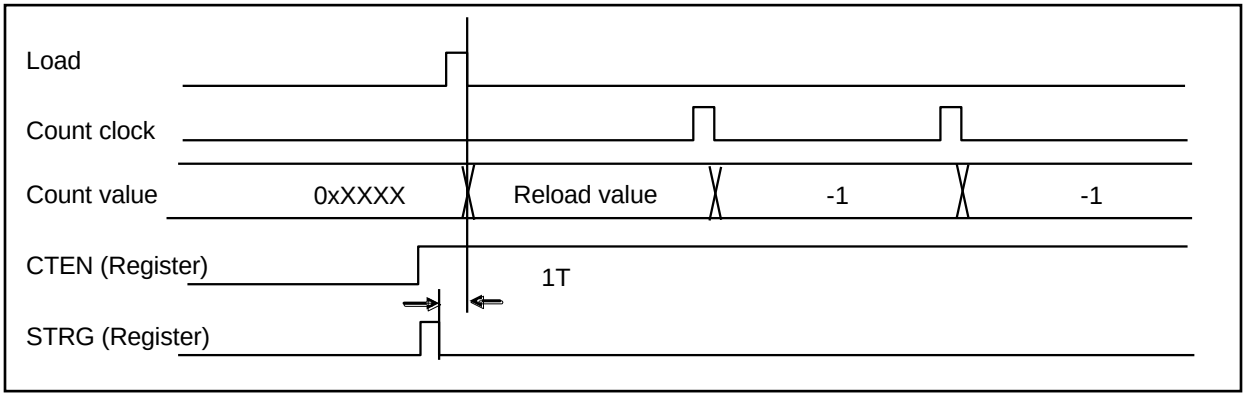
To start the count operation at the same time counting is enabled, write 1 to both CTEN and STRG bits in the Timer Control Register. When the timer is started (CTEN = 1), trigger input with the STRG bit is valid regardless of the operation mode.

When the count operation is enabled and the timer is started with a software trigger or an external trigger, the value in the PWM Cycle Set Register is loaded to the counter and countdown is started.

It takes a time of 1T (T: machine cycle) from setting of a counter start trigger to loading of the PWM Cycle Set Register data to the counter.

Figure 9-13 shows the start of the counter by a software trigger and counter operation.

Figure 9-13 Count Operation Performed When the Internal Clock Is Selected



Underflow Operation

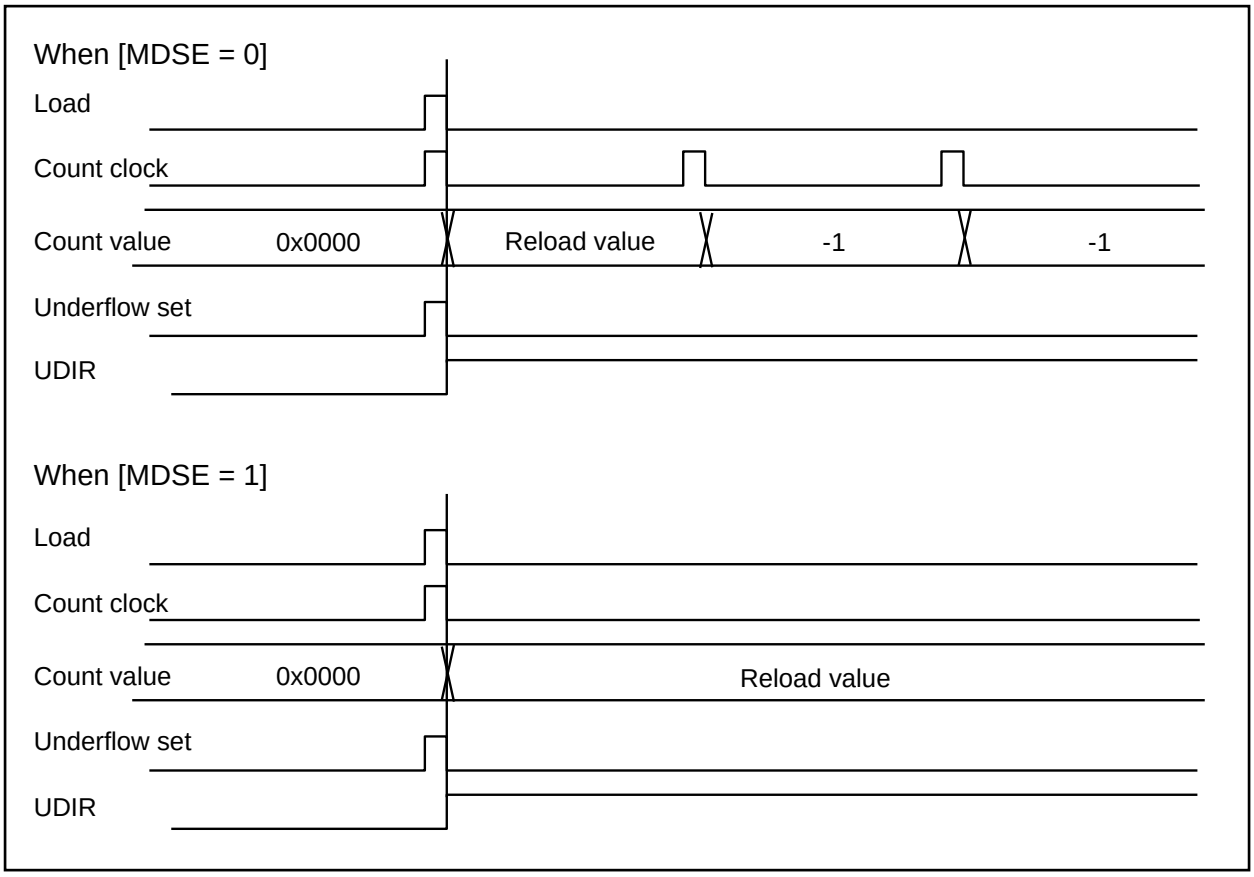
An underflow occurs when the counter value changes from 0x0000 to 0xFFFF. Therefore, an underflow occurs at a count of [Set value in the PWM Cycle Set Register + 1].

When an underflow occurs, the contents of the PWM Cycle Set Register (PCSR) are loaded to the counter. When the MDSE bit in the Timer Control Register (TMCR) is 0, the count operation continues. When the MDSE bit is 1, the counter stops while keeping the loaded counter value.

An underflow sets the UDIR bit in the Status Control Register (STC). In this case, an interrupt request occurs when the UDIE bit is 1.

Figure 9-14 shows a timing chart of underflow operations.

Figure 9-14 Underflow Operation Timing Chart

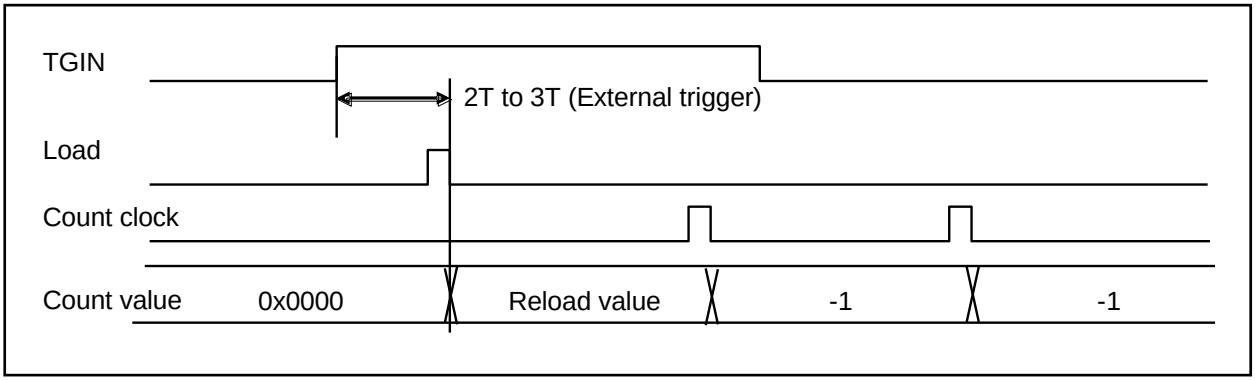


Operation of the Input Pin Function

The TGIN pin can be used for trigger input. When a valid edge is input to the TGIN pin, the contents of the PWM Cycle Set Register are loaded to the counter and the count operation is started. As a time from trigger input to loading of the counter value, 2T to 3T (T: machine cycle) is required. When the gate Input enable bit of the Timer Control Register 2 is set to1(GATE=1), the TGIN pin can be used for trigger input.

Figure 9-15 shows a trigger input operation performed when a rising edge is specified as a valid edge.

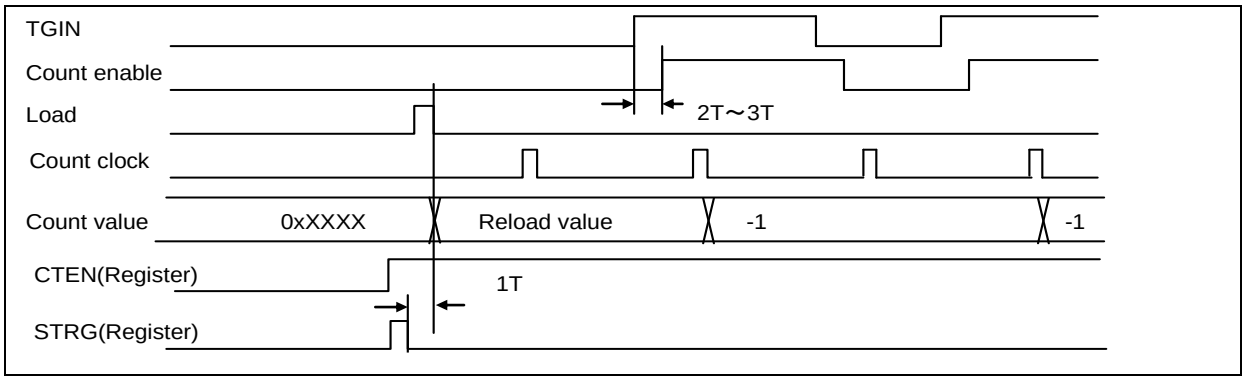
Figure 9-15 Operation Caused by a Trigger Input



When the gate Input enable bit of the Timer Control Register 2 is set to1(GATE=1), enabling of the count operation and stating of the timer by software trigger cause loading the cycle setting register value to the counter and decrementing with the count clock while the valid level is input to the TGIN pin. As a time from valid level input to enabling of the count, 2T to 3T (T: machine cycle) is required.

Figure 9-16 shows the decrement operation when the specified invalid level is set to “HIGH”.

Figure 9-16 Operation When GATE Input Enabled (GATE=1)

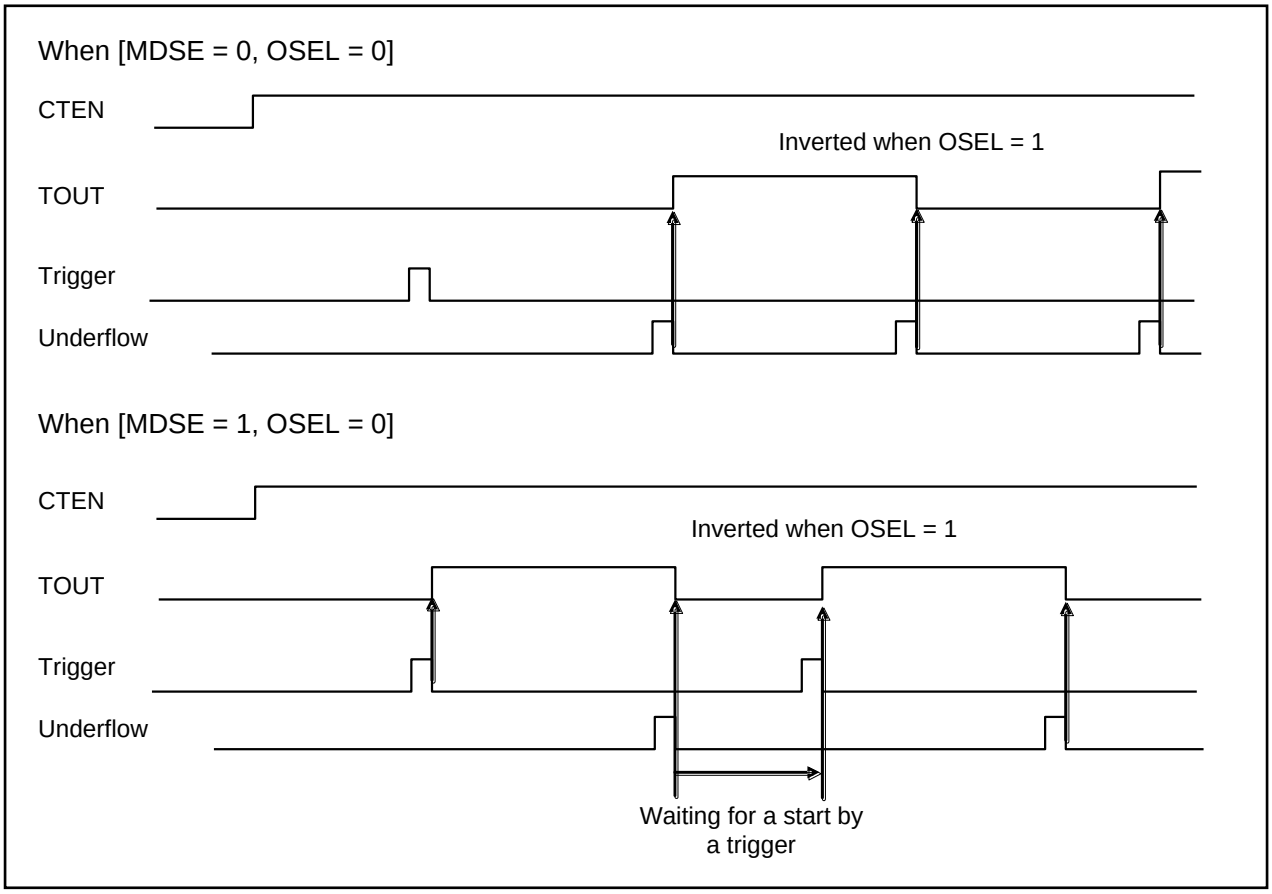


Operation of the Output Pin Function

The TOUT output pin functions as, in reload mode, toggle output inverted by an underflow and, in one-shot mode, pulse output indicating that counting is in progress. The output polarity can be set with the OSEL bit in the Timer Control Register (TMCR). If OSEL = 0, toggle output has an initial value of 0, and one-shot pulse output is 1 during counting. When OSEL is set to 1, the output waveform is inverted.

Figure 9-17 shows a timing chart of output pin function operations.

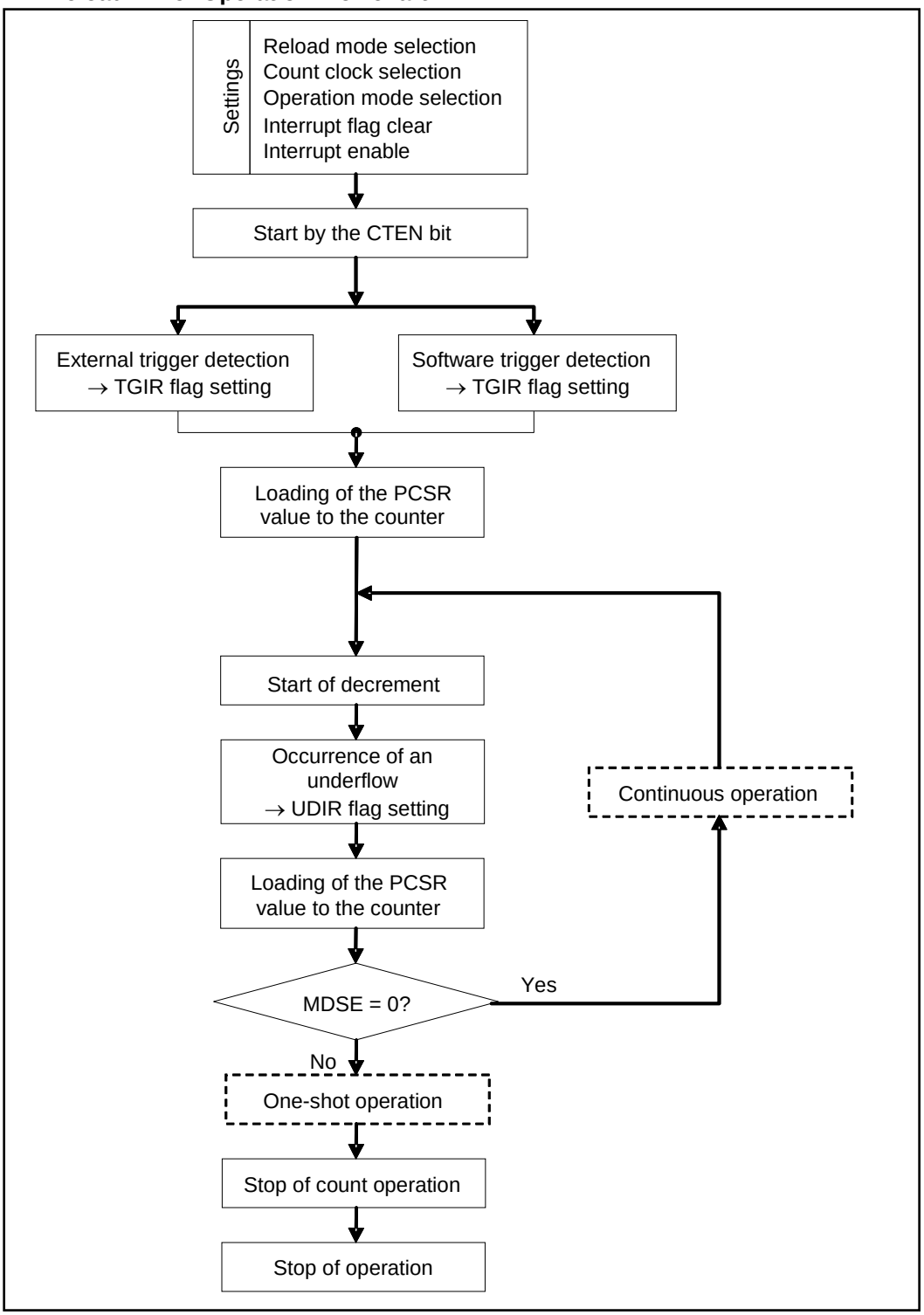
Figure 9-17 Output Pin Function Operation Timing Chart



9.3.2 Reload Timer Operation Flowchart

This section provides an operation flowchart of the reload timer.

Reload Timer Operation Flowchart



9.3.3 Timer Control Registers (TMCR and TMCR2) and Status Control Register (STC) used when the Reload Timer is selected

The Timer Control Register (TMCR) controls timer operations.

Timer Control Register (Upper bytes of TMCR)

bit	15	14	13	12	11	10	9	8
Field	Reserved	CKS2	CKS1	CKS0	Reserved		EGS1	EGS0
Attribute	R/W	R/W	R/W	R/W	R/W		R/W	R/W
Initial value	0	0	0	0	00		0	0

[bit15] Reserved: Reserved bit

The read value is 0.

Set 0 to this bit.

[bit14:12, TMCR2:bit 8] CKS3 to CKS0: Count clock selection bits

- Select the count clock for the 16-bit down counter.
- Changes to the count clock setting are applied immediately. For this reason, changes to CKS3 through CKS0 must be made when the counting is stopped (CTEN = 0). However, it is possible to make changes at the same time you set 1 to the CTEN bit.

CKS3	CKS2	CKS1	CKS0	Description
0	0	0	0	ϕ
0	0	0	1	ϕ /4
0	0	1	0	ϕ /16
0	0	1	1	ϕ /128
0	1	0	0	ϕ /256
0	1	0	1	External clock (rising edge event)
0	1	1	0	External clock (falling edge event)
0	1	1	1	External clock (both edge event)
1	0	0	0	ϕ /512
1	0	0	1	ϕ /1024
1	0	1	0	ϕ /2048
Others				Setting is prohibited.

[bit11:10] Reserved: Reserved bits

The read value is 0.

Set 0 to these bits.

[bit9:8] EGS1, EGS0: Selection bits of trigger input edge and gate function level

- When the trigger input is selected (GATE=0), these bits select a valid edge for input waveforms as an external start cause and set the trigger condition.
- When the trigger input is selected (GATE=0) and the initial value or 0b00 is set, the timer is not started by external waveforms because the setting means that no valid edge is selected for input waveforms.
- When the GATE function is selected (GATE=1), these bits select a valid edge for input waveforms as an external count cause and the down count decrements while the specified level is valid.
- Changes to EGS1 or EGS0 must be made when the counting is stopped (CTEN = 0). However, it is possible to make changes at the same time you set 1 to the CTEN bit.

N

bit9	bit8 *o*	Description	
		Trigger input selected (GATE=0)	Gate function selected (GATE=1)
0	*t* 0	Trigger input disabled	LOW level
0	*e* 1	External trigger (rising edge)	HIGH level
1	*:* 0	External trigger (falling edge)	LOW level
1	1	External trigger (both edges)	HIGH level

– *I*

f

the STRG bit is set to 1, software triggering is enabled regardless of the EGS1 and EGS0 settings.

Timer Control Register 2 (Lower bytes of TMCR)

bit	7	6	5	4	3	2	1	0
Field	T32	FMD2	FMD1	FMD0	OSEL	MDSE	CTEN	STRG
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7] T32: 32-bit timer selection bit

- This bit selects the 32-bit timer function.
- When the FMD[2:0] bits are set to 0b011 to select the reload timer function, setting the T32 bit to 1 selects 32-bit timer mode.
- Changes must be made while the timer is stopped (CTEN = 0). However, it is possible to make changes at the same time you set 1 to the CTEN bit (see 32-bit Mode Operations).

bit	Description
0	16-bit timer mode
1	32-bit timer mode

[bit6:4] FMD2 to FMD0: Timer function selection bits

- These bits select the timer function.
- When the FMD[2:0] bits are set to 0b011, the reload timer function is selected.
- Changes must be made while the timer is stopped (CTEN = 0). However, it is possible to make changes at the same time you set 1 to the CTEN bit.

bit 6	bit 5	bit 4	Description
0	0	0	Reset mode
0	0	1	Selection of the PWM function
0	1	0	Selection of the PPG function
0	1	1	Selection of the reload timer function
1	0	0	Selection of the PWC function
Others			Setting is prohibited.

[bit3] OSEL: Output polarity specification bit

- This bit selects whether to invert the timer output level.
- Used in combination with bit 2 MDSE, this bit generates the following output waveforms.

MDSE	OSEL	Output waveforms
0	0	Toggle output at the LOW level at the start of counting
0	1	Toggle output at the HIGH level at the start of counting
1	0	Rectangular waves at the HIGH level during counting
1	1	Rectangular waves at the LOW level during counting

bit	Description
0	Normal polarity
1	Inverted polarity

[bit2] MDSE: Mode selection bit

- When the MDSE bit is set to 0, reload mode is selected. When a count value underflow from 0x0000 to 0xFFFF occurs, the reload register value is loaded to the counter at the same time, and the count operation is continued.
- When the MDSE bit is set to 1, one-shot mode is selected. A count value underflow from 0x0000 to 0xFFFF stops the operation.
- Changes must be made while the timer is stopped (CTEN = 0). However, it is possible to make changes at the same time you set 1 to the CTEN bit.

bit	Description
0	Reload mode
1	One-shot mode

[bit1] CTEN: Timer enable bit

- This bit enables the operation of the down counter.
- When the counter is in operation enabled status (the CTEN bit is 1), writing 0 to this bit stops the counter.

bit	Description
0	Stop
1	Operation enabled

Note:

- *By writing 0 to CTEN bit, the output waveform becomes Low.*

[bit0] STRG: Software trigger bit

- When the CTEN bit is 1, writing 1 to the STRG bit enables software triggering.
- The read value of the STRG bit is always 0.

bit	Description
0	Invalid
1	Start triggered by software

Notes:

- *Software triggering is also enabled when 1 is written to the CTEN and STRG bits simultaneously.*
- *If the STRG bit is set to 1, software triggering is enabled regardless of the EGS1 and EGS0 settings.*

Timer Control Register 2 (Upper bytes of TMCR2)

bit	15	14	13	12	11	10	9	8
Field	GATE	Reserved						CKS3
Attribute	R/W	R/W						R/W
Initial value	0	000000						0

Note: This register is placed above the STC register.

[bit15] GATE: Gate Input Enable bit

- This bit selects the Trigger input function or the Gate function for the external cause pin.
- Trigger input function: When the valid edge is input to the external cause pin, the decrement is started.
- -Gate function: While the valid edge is input to the external cause pin, the decrement continues.

bit	Description
0	Trigger input function
1	GATE function

[bit14:9] Reserved: Reserved bits

The read value is 0.
Set 0 to these bits.

[bit8] CKS3: Count clock selection bit

See [bit14:12, TMCR2:bit8] CKS3 to CKS0: Count clock selection bit in 9.3.3 Timer Control Registers (TMCR and TMCR2) and Status Control Register (STC) used when the Reload Timer is selected.

Status Control Register (STC)

bit	7	6	5	4	3	2	1	0
Field	Reserved	TGIE	Reserved	UDIE	Reserved	TGIR	Reserved	UDIR
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Note:

- *The TMCR2 register is placed in the upper bytes of this register.*

[bit7] Reserved: Reserved bit

The read value is 0.

Set 0 to this bit.

[bit6] TGIE: Trigger interrupt request enable bit

- This bit controls interrupt requests of bit2 TGIR.
- When the TGIE bit is enabled, setting bit2 TGIR generates an interrupt request to the CPU.

bit	Description
0	Disables interrupt requests.
1	Enables interrupt requests.

[bit5] Reserved: Reserved bit

The read value is 0.

Set 0 to this bit.

[bit4] UDIE: Underflow interrupt request enable bit

- This bit controls interrupt requests of bit0 UDIR.
- When the UDIE bit is enabled, setting bit0 UDIR generates an interrupt request to the CPU.

bit	Description
0	Disables interrupt requests.
1	Enables interrupt requests.

[bit3] Reserved: Reserved bit

The read value is 0.

Set 0 to this bit.

[bit2] TGIR: Trigger interrupt request bit

- When a software trigger or trigger input is detected, the TGIR bit is set to 1.
- The TGIR bit is cleared by writing 0.
- Even if 1 is written to the TGIR bit, the bit value is not affected.
- The read value of read-modify-write instructions is "1" regardless of the bit value.

bit	Description
0	Clears an interrupt factor.
1	Detects an interrupt factor.

[bit1] Reserved: Reserved bit

The read value is 0.

Set 0 to this bit.

[bit0] UDIR: Underflow interrupt request bit

- When a count value underflow from 0x0000 to 0xFFFF occurs during counting from the value for which the HIGH width is set, the UDIR bit is set to 1.
- The UDIR bit is cleared by writing 0.
- Even if 1 is written to the UDIR bit, the bit value is not affected.
- The read value of read-modify-write instructions is 1 regardless of the bit value.

bit	Description
0	Clears an interrupt factor.
1	Detects an interrupt factor.

9.3.4 Cycle Set Register (PCSR)

The Cycle Set Register (PCSR) is a register for storing the initial counter value. In 32-bit mode and for the even channel, the initial count value of the lower 16 bits is stored. For the odd channel, the initial count value of the upper 16 bits is stored. The initial value after a reset is undefined. Do not access this register with 8-bit data.

bit	15	0
Field	PCSR [15:0]	
Attribute	R/W	
Initial value	0xXXXX	

This is a register for setting the cycle. Transfer to the Timer Register is performed at an underflow.

- Do not access the PCSR register with 8-bit data.
- Set the cycle for the PCSR register after setting the reload timer function using the FMD[2:0] bits in the TMCR register.
- When writing data in the PCSR register in 32-bit mode, access the upper 16-bit data (odd channel data) first, and then access the lower 16-bit data (even channel data).

9.3.5 Timer Register (TMR)

The Timer Register (TMR) is a register that reads the count value of a timer. In 32-bit mode and for the even channel, the count value of the lower 16 bits is read. For the odd channel, the count value of the upper 16 bits is read. The initial value is undefined.

Do not access this register with 8-bit data.

bit	15	0
Field	TMR [15:0]	
Attribute	R	
Initial value	0xXXXX	

The value of the 16-bit down counter is read.

- Do not access the TMR register with 8-bit data.
- When reading the TMR register in 32-bit mode, read the lower 16-bit data (even channel data) first, and then read the upper 16-bit data (odd channel data).

9.4 PWC Timer Function

The function of the base timer can be set to either the 16-bit PWM timer, 16-bit PPG timer, 16-/32-bit reload timer, or 16-/32-bit PWC timer using the FMD[2:0] bits in the Timer Control Register. This section explains the timer functions available when PWC is set.

9.4.1. Operations of the PWC Timer

9.4.2. Timer Control Registers (TMCR and TMCR2) and Status Control Register (STC) used when the PWC Timer is selected

9.4.3. Data Buffer Register (DTBF)

9.4.1 Operations of the PWC Timer

The PWC timer has the pulse width measurement function. Five types of count clock are available for measuring the time and cycle between any input pulse events by the counter. This section explains the basic functions and operations of the pulse width measurement function.

Pulse Width Measurement Function

Count operation is not performed until the counter is started and cleared to 0x0000 and the specified measurement start edge is input. Upon detecting a measurement start edge, the counter starts count-up from "0x0001" and stops counting upon detecting a measurement end edge. The value counted in between is stored as a pulse width in the register.

An interrupt request can be generated when the measurement is completed or an overflow occurs.

After the completion of measurement, it operates as follows depending on the measurement mode:

- In one-shot measurement mode: Stops the operation.
- In continuous measurement mode: Transfers the counter value to the buffer register and stops counting until the measurement start edge is input again.

Figure 9-18 Pulse Width Measurement Operation (One-shot Measurement Mode/HIGH Width Measurement)

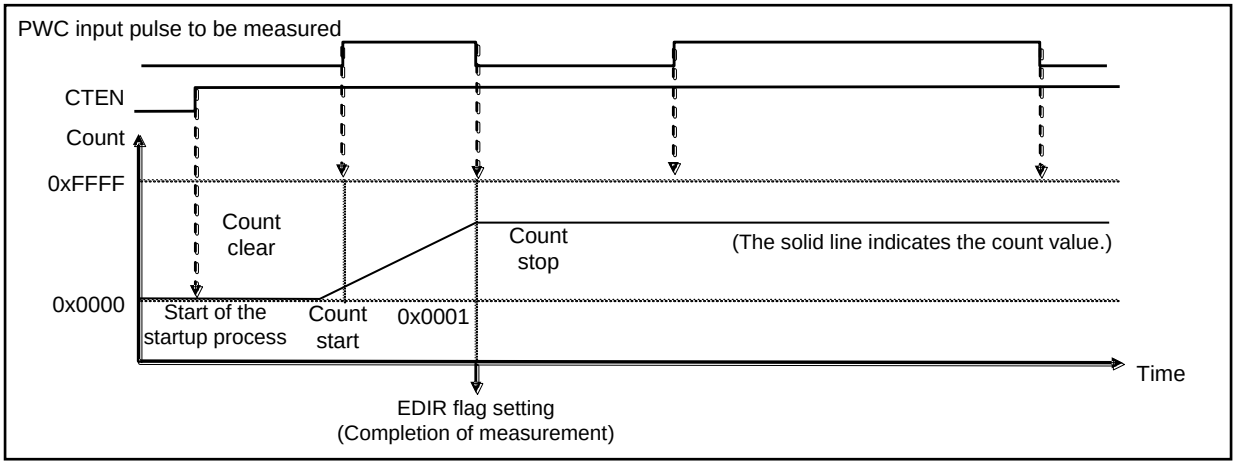
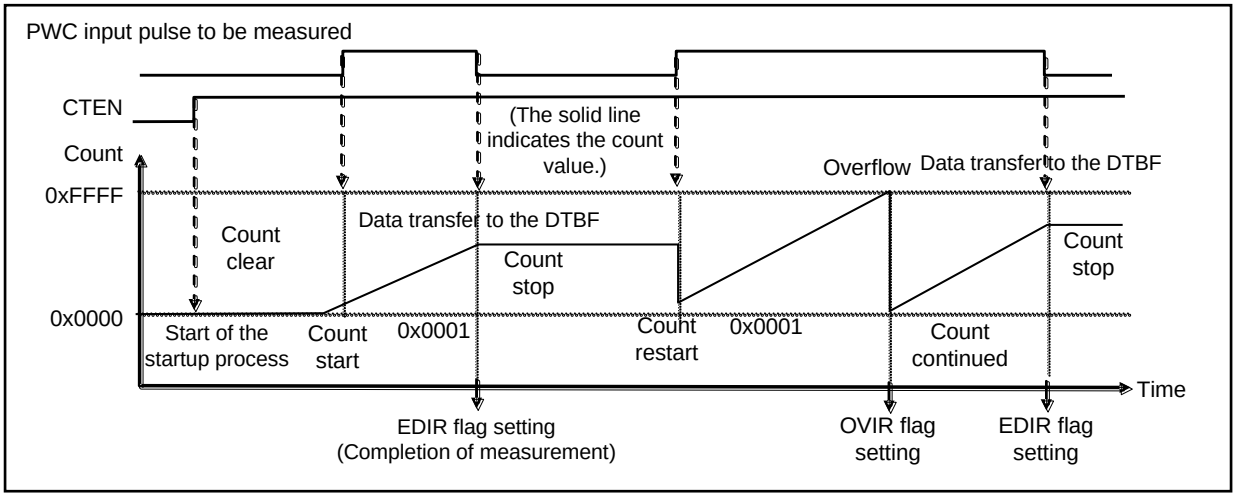


Figure 9-19 Pulse Width Measurement Operation (Continuous Measurement Mode/HIGH Width Measurement)



Selection of Count Clock

The count clock of the counter can be selected from eight types by setting bit8: CKS3 in the TMCR2 register and bit14:12: CKS2, CKS1, and CKS0 in the TMCR register.

The selectable count clocks are as follows:

TMCR2 and TMCR registers CKS3, CKS2, CKS1, and CKS0 bits	Internal count clock to be selected
0000	Machine clock [Initial value]
0001	1/4 frequency of the machine clock
0010	1/16 frequency of the machine clock
0011	1/128 frequency of the machine clock
0100	1/256 frequency of the machine clock
0101	Setting is prohibited.
0110	
0111	
1000	1/512 frequency of the machine clock
1001	1/1024 frequency of the machine clock
1010	1/2048 frequency of the machine clock
Others	Setting is prohibited.

The machine clock is selected as the initial value after a reset.

Be sure to select the count clock before starting the counter.

Selection of Operation Mode

Set the TMCR to select the operation/measurement mode.

Operation mode setting ... TMCR bit10:8: EGS2, EGS1, and EGS0 (Selection of measurement edge)
Measurement mode setting ... TMCR bit2: MDSE (Selection of one-shot/continuous measurement)

The following provides a list of operation mode settings.

Operation mode		MDSE	EGS2	EGS1	EGS0
↑ to ↓ HIGH pulse width measurement	Continuous measurement: Buffer enabled	0	0	0	0
	One-shot measurement: Buffer disabled	1	0	0	0
↑ to ↑ Cycle measurement between rising edges	Continuous measurement: Buffer enabled	0	0	0	1
	One-shot measurement: Buffer disabled	1	0	0	1
↓ to ↓ Cycle measurement between falling edges	Continuous measurement: Buffer enabled	0	0	1	0
	One-shot measurement: Buffer disabled	1	0	1	0
↑ or ↓ to ↑ or ↓ Interval measurement between all edges	Continuous measurement: Buffer enabled	0	0	1	1
	One-shot measurement: Buffer disabled	1	0	1	1
↓ to ↑ LOW pulse width measurement	Continuous measurement: Buffer enabled	0	1	0	0
	One-shot measurement: Buffer disabled	1	1	0	0
Setting is prohibited.		0	1	0	1
		1	1	0	1
		0	1	1	0
		1	1	1	0
		0	1	1	1
		1	1	1	1

HIGH pulse width measurement in one-shot measurement mode is selected as the initial value after a reset.
Be sure to select an operation mode before starting the counter.

Starting and Stopping Pulse Width Measurement

Set bit 1: CTEN bit in the TMCR to start, restart, or stop forcibly each operation.

The pulse width measurement is started or restarted by writing 1 to the CTEN bit, and it is stopped forcibly by writing 0 to the CTEN bit.

CTEN	Function
1	Starts or restarts the pulse width measurement.
0	Forcibly stops the pulse width measurement.

Operation after a Restart

After the counter is restarted in pulse measurement mode, counting is not performed until a measurement start edge is input. After a measurement start edge is detected, the 16-bit up counter starts counting from "0x0001".

Restart

An operation to start the counter again after it has been started and while it is in operation (writing 1 again while the CTEN bit is 1) is referred to as a restart. When restarted, the counter performs the following operation:

- When waiting for a measurement start edge:

  Has no effect on operation.

- When performing measurement:

  Clears the count to 0x0000 and waits for a measurement start edge again. When detection of a measurement end edge and the restart operation occur simultaneously, a measurement end flag (EDIR) is set and, when in continuous measurement mode, the measurement result is transferred to the DTBF.

Stop

In one-shot measurement mode, since the count operation is stopped automatically by a counter overflow or completion of measurement, you do not have to be aware of the stop. In continuous measurement mode or when you want to stop the operation before it stops automatically, you have to stop it forcibly.

Counter Clear and Initial Value

The 16-bit up counter is cleared to 0x0000 in the following cases:

- When a reset is performed
- When 1 is written to bit 1: CTEN bit in the TMCR (including the cases for restarting)

The 16-bit up counter is initialized to 0x0001 in the following case:

- When a measurement start edge is detected

Details on Pulse Width Measurement Operations

■ One-shot measurement and continuous measurement

Pulse width measurement can be performed in two modes: one for performing measurement only one time and the other for performing it continuously. Each mode is selected with the MDSE bit in the TMCR (see “Selection of Operation Mode").Differences between these modes are as follows:

- One-shot measurement mode:

  When the first measurement end edge is input, the counter stops counting, a measurement end flag (EDIR) in the STC is set, and no further measurement is performed.
  However, when restarted at the same time, it waits to start measurement.

- Continuous measurement mode:

  When a measurement end edge is input, the counter stops counting, a measurement end flag (EDIR) in the STC is set, and the counter stops until the measurement start edge is input again. When the measurement start edge is input again, the counter is initialized to 0x0001 and measurement is started. After the measurement is completed, the result in the counter is transferred to the DTBF.

Be sure to select/change measurement modes while the counter is stopped.

■ Measurement result data

There are differences between one-shot and continuous modes in handling of measurement results and counter values and in DTBF functions. Differences between these modes in handling of measurement results are as follows:

- One-shot measurement mode:

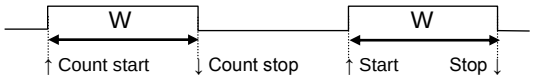
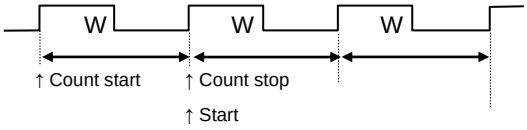
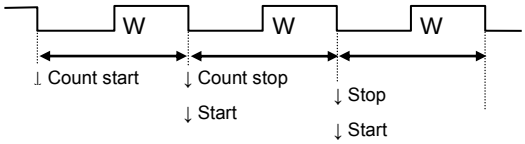
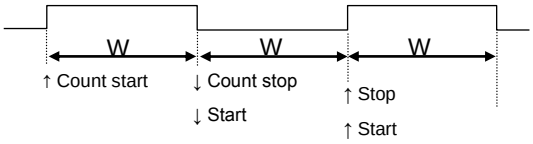
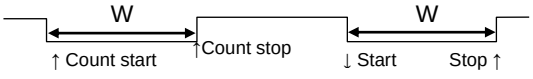
  Reading the DTBF during operation obtains the count value being measured.
  Reading the DTBF after the completion of measurement obtains the measurement result data.

- Continuous measurement mode:

  After the measurement is completed, the result in the counter is transferred to the DTBF.
  Reading the DTBF obtains the last measurement result. The previous measurement result is retained during the measurement operation. It is not possible to read the count value being measured.
  In continuous measurement mode, if the next measurement is completed before the measurement result is read, the previous result is overwritten by the new result. In this case, an error flag (ERR) in the STC is set. The error flag is cleared automatically when the DTBF is read.

■ Measurement modes and count operations

The measurement mode can be selected from five types, differing in which part of the input pulse is measured. The following are explanations:

Measurement mode	EGS[2:0]	Item to be measured (W: Pulse width to be measured)
HIGH pulse width measurement	000	 The width of the HIGH period is measured. Count (measurement) start: At detection of a rising edge Count (measurement) end: At detection of a falling edge
Cycle measurement between rising edges	001	 The cycle between rising edges is measured. Count (measurement) start: At detection of a rising edge Count (measurement) end: At detection of a rising edge
Cycle measurement between falling edges	010	 The cycle between falling edges is measured. Count (measurement) start: At detection of a falling edge Count (measurement) end: At detection of a falling edge
Pulse width measurement between all edges	011	 The width between continuously input edges is measured. Count (measurement) start: At detection of an edge Count (measurement) end: At detection of an edge
LOW pulse width measurement	100	 The width of the LOW period is measured. Count (measurement) start: At detection of a falling edge Count (measurement) end: At detection of a rising edge

In any measurement mode, the counter is cleared to 0x0000 when started, and it does not perform the count operation until a measurement start edge is input. Once a measurement start edge is input, the counter continues incrementing for every count clock until a measurement end edge is input.

In pulse width measurement between all edges or cycle measurement in continuous measurement mode, an end edge is also a start edge for the next measurement.

■ Pulse width/cycle calculation method

After completion of measurement, the measured pulse width/cycle can be calculated as follows from the measurement result data stored in the DTBF:

$T_W = n \times t$	T_W:	Measured pulse width/cycle
	n:	Measurement result data stored in the DTBF
	t:	Count clock cycle

■ Generation of interrupt requests

Two interrupt requests can be generated.

- Interrupt request due to a counter overflow

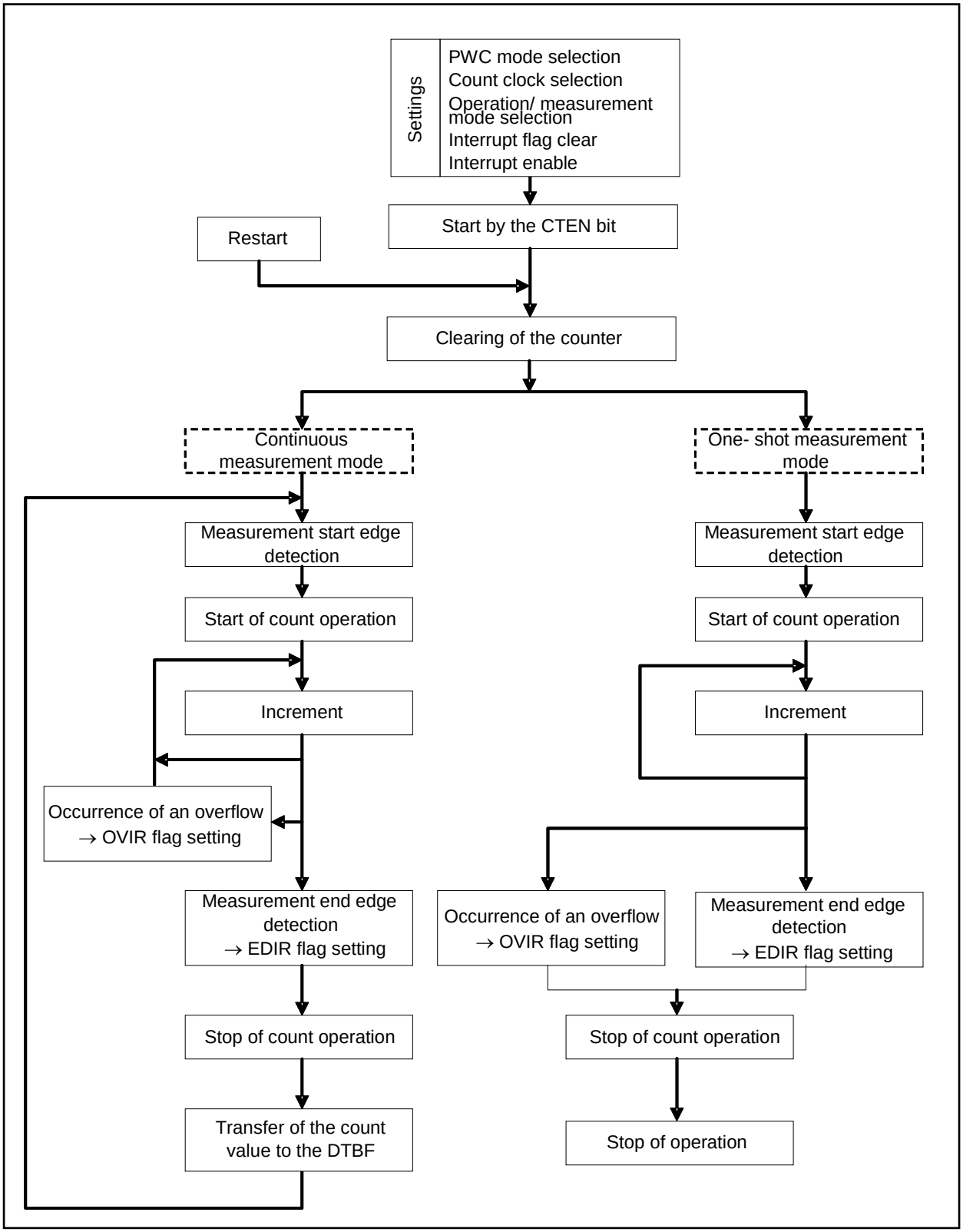
  When count-up causes an overflow during measurement, an overflow flag (OVIR) is set and an interrupt request is generated if overflow interrupt requests are enabled.

- Interrupt request due to completion of measurement

  When a measurement end edge is detected, a measurement end flag (EDIR) in the STC is set and an interrupt request is generated if measurement end interrupt requests are enabled.
  The measurement end flag (EDIR) is cleared automatically when the measurement result DTBF is read.

■ Pulse width measurement operation flowchart

Figure 9-20 Pulse Width Measurement Operation Flowchart



9.4.2 Timer Control Registers (TMCR and TMCR2) and Status Control Register (STC) used when the PWC Timer is selected

The Timer Control Register (TMCR) controls timer operations.

Timer Control Register (Upper bytes of TMCR)

bit	15	14	13	12	11	10	9	8
Field	Reserved	CKS2	CKS1	CKS0	Reserved	EGS2	EGS1	EGS0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit15] Reserved: Reserved bit

The read value is 0.

Set 0 to this bit.

[bit14:12, TMCR2:bit 8] CKS3 to CKS0: Count clock selection bits

- Select the count clock for the 16-bit down counter.
- Changes to the count clock setting are applied immediately. For this reason, changes to CKS3 through CKS0 must be made when the counting is stopped (CTEN = 0). However, it is possible to make changes at the same time you set 1 to the CTEN bit.

CKS3	CKS2	CKS1	CKS0	Description
0	0	0	0	ϕ
0	0	0	1	ϕ /4
0	0	1	0	ϕ /16
0	0	1	1	ϕ /128
0	1	0	0	ϕ /256
0	1	0	1	Setting is prohibited.
0	1	1	0	
0	1	1	1	
1	0	0	0	ϕ /512
1	0	0	1	ϕ /1024
1	0	1	0	ϕ /2048
Others				Setting is prohibited.

[bit11] Reserved: Reserved bit

The read value is 0.

Set 0 to this bit.

[bit10:8] EGS2 to EGS0: Measurement edge selection bits

- These bits set measurement edge conditions.
- Changes to EGS2, EGS1, or EGS0 must be made when the counting is stopped (CTEN = 0). However, it is possible to make changes at the same time you set 1 to the CTEN bit.

bit10	bit9	bit8	Description
0	0	0	HIGH pulse width measurement (↑ to ↓)
0	0	1	Cycle measurement between rising edges (↑ to ↑)
0	1	0	Cycle measurement between falling edges (↓ to ↓)
0	1	1	Pulse width measurement between all edges (↑ or ↓ to ↓ or ↑)
1	0	0	LOW pulse width measurement (↓ to ↑)
1	0	1	Setting is prohibited.
1	1	0	
1	1	1	

Timer Control Register (Lower bytes of TMCR)

bit	7	6	5	4	3	2	1	0
Field	T32	FMD2	FMD1	FMD0	Reserved	MDSE	CTEN	Reserved
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7] T32: 32-bit timer selection bit

- This bit selects the 32-bit timer function.
- When the FMD[2:0] bits are set to 0b100 to select the PWC function, setting the T32 bit to 1 selects 32-bit PWC mode.
- Changes must be made while the timer is stopped (CTEN = 0). However, it is possible to make changes at the same time you set 1 to the CTEN bit (see 32-bit mode operation.)

bit	Description
0	16-bit timer mode
1	32-bit timer mode

[bit6:4] FMD2 to FMD0: Timer function selection bits

- These bits select the timer function.
- When the FMD[2:0] bits are set to 0b100, the PWC timer function is selected.
- Changes must be made while the timer is stopped (CTEN = 0). However, it is possible to make changes at the same time you set 1 to the CTEN bit.

bit6	bit5	bit4	Description
0	0	0	Reset mode
0	0	1	Selection of the PWM function
0	1	0	Selection of the PPG function
0	1	1	Selection of the reload timer function
1	0	0	Selection of the PWC function
1	0	1	Setting is prohibited.
1	1	0	
1	1	1	

[bit3] Reserved: Reserved bit

The read value is 0.

Set 0 to this bit.

[bit2] MDSE: Mode selection bit

- Changes must be made while the timer is stopped (CTEN = 0). However, it is possible to make changes at the same time you set 1 to the CTEN bit.

bit	Description
0	Continuous measurement mode (Buffer register enabled)
1	One-shot measurement mode (Stops after one measurement)

[bit1] CTEN: Timer enable bit

- This bit enables the start or restart of the up counter.
- When the counter is in operation enabled status (the CTEN bit is 1), writing 1 restarts the counter. The counter is cleared and waits for a measurement start edge.
- When the counter is in operation enabled status (the CTEN bit is 1), writing 0 to this bit stops the counter.

bit	Description
0	Stop
1	Operation enabled

Note:

- *By writing 0 to CTEN bit, the output waveform becomes Low.*

[bit0] Reserved: Reserved bit

The read value is 0.

Set 0 to this bit.

Timer Control Register 2 (Upper bytes of TMCR2)

bit	15	14	13	12	11	10	9	8
Field	Reserved							CKS3
Attribute	R/W							R/W
Initial value	0000000							0

Note:

- *This register is placed above the STC register.*

[bit15:9] Reserved: Reserved bits

The read value is 0.
Set 0 to these bits.

[bit8] CKS3: Count clock selection bit

See [bit14:12, TMCR2:bit8] CKS3 to CKS0: Count Count clock selection bit in 9.4.2 Timer Control Registers (TMCR and TMCR2) and Status Control Register (STC) used when the PWC Timer is selected.

Status Control Register (STC)

bit	7	6	5	4	3	2	1	0
Field	ERR	EDIE	Reserved	OVIE	Reserved	EDIR	Reserved	OVIR
Attribute	R	R/W	R/W	R/W	R/W	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Note:

- *The TMCR2 register is placed in the upper bytes of this register.*

[bit7] ERR: Error flag bit

- This flag indicates that the next measurement has been completed in continuous measurement mode before the measurement result is read from the DTBF register. In this case, the result of the previous measurement in the DTBF register is replaced by that of the next measurement.
- The measurement is continued regardless of the ERR bit value.
- The ERR bit is read-only. Writing a value does not affect the bit value.
- The ERR bit is cleared by reading the measurement result (DTBF).

bit	Description
0	Normal status
1	A measurement result not yet read was overwritten by the next measurement result.

[bit6] EDIE: Measurement completion interrupt request enable bit

- This bit controls interrupt requests of bit 2 EDIR.
- When the EDIE bit is enabled, setting bit 2 EDIR generates an interrupt request to the CPU.

bit	Description
0	Disables interrupt requests.
1	Enables interrupt requests.

[bit5] Reserved: Reserved bit

The read value is 0.

Set 0 to this bit.

[bit4] OVIE: Overflow interrupt request enable bit

- This bit controls interrupt requests of bit 0 OVIR.
- When the OVIE bit is enabled, setting bit 0 OVIR generates an interrupt request to the CPU.

bit	Description
0	Disables interrupt requests.
1	Enables interrupt requests.

[bit3] Reserved: Reserved bit

The read value is 0.

Set 0 to this bit.

[bit2] EDIR: Measurement completion interrupt request bit

- This bit indicates that the completion of measurement. The flag is set to 1 when the measurement is completed.
- The EDIR bit is cleared by reading the measurement result (DTBF).
- The EDIR bit is read-only. Writing a value does not affect the bit value.

bit	Description
0	Reads the measurement result (DTBF).
1	Detects an interrupt cause.

[bit1] Reserved: Reserved bit

The read value is 0.

Set 0 to this bit.

[bit0] OVIR: Overflow interrupt request bit

- When a count value overflow from 0xFFFF to 0x0000 occurs, the flag is set to 1.
- The OVIR bit is cleared by writing 0.
- Even if 1 is written to the OVIR bit, the bit value is not affected.
- The read value of read-modify-write instructions is 1 regardless of the bit value.

bit	Description
0	Clears an interrupt factor.
1	Detects an interrupt factor.

9.4.3 Data Buffer Register (DTBF)

The Data Buffer Register (DTBF) is a register that reads the measured or count value of the PWC timer. In 32-bit mode, the value of the lower 16 bits is read for the even channel and that of the upper 16 bits for the odd channel.

Do not access this register with 8-bit data.

bit	15	0
Field	DTBF[15:0]	
Attribute	R	
Initial value	0x0000	

- The DTBF register is read-only in both continuous and one-shot measurement modes. Writing a value does not change the register value.
- In continuous measurement mode (TMCR bit3 MDSE = 1), this register works as a buffer register that stores the previous measurement result.
- In one-shot measurement mode (TMCR bit3 MDSE = 0), the DTBF register accesses the up counter directly. The count value can be read during counting. The measurement value is retained after the completion of measurement.
- Do not access the DTBF register with 8-bit data.

CHAPTER 6: Multifunction Timer

This chapter explains the multifunction timer unit.

1. Overview of the Multifunction Timer
2. Configuration of the Multifunction Timer
3. Registers of the Multifunction Timer
4. Operations of the Multifunction Timer
5. Multifunction Timer Control Examples
6. Detailed Timing of the Multifunction Timer Input/Output Signals

1. Overview of the Multifunction Timer

The multifunction timer is a function block that enables three-phase motor control. In conjunction with a PPG and an A/D converter (called ADC hereafter), it can provide a variety of motor controls. An overview of the multifunction timer is provided below.

Functions

The multifunction timer has the following functionality.

- It can output PWM signals with any cycle/pulse length (PWM signal output function).
- It can start a PPG in synchronization with PWM signal output. It can superimpose a PPG's output signal on the PWM signal and output it (DC chopper waveform output function).
- It can generate a non-overlap signal that maintains the response time of the power transistor (dead time) from PWM signal output (dead timer function).
- It can capture the timing of input signal changes and pulse width in synchronization with PWM signal output (Input capture function).
- It can start the ADC at any time, in synchronization with PWM signal output (ADC start function).
- It performs noise canceling of the emergency motor shutdown interrupt signal (DTTIX input signal). It can freely set the pin state at the time of motor shutdown when a valid signal input is detected (DTIF interrupt function).

Abbreviations

In this chapter, the following abbreviations are used in explanations.

MFT	Multifunction Timer
PPG	Programmable Pulse Generator
FRT	Free-run Timer
FRTS	Free-run Timer Selector
OCU	Output Compare Unit
WFG	Waveform Generator
NZCL	Noise Canceler
ICU	Input Capture Unit
ADCMP	ADC Start Compare

2. Configuration of the Multifunction Timer

This chapter explains the configuration of the multifunction timer and the functions of each function block and I/O pin.

2.1. Block Diagram of the Multifunction Timer

2.2. Description of Each Function Block

2.3. I/O Pins of the Multifunction Timer Unit

2.4. Function Differences by Product Type

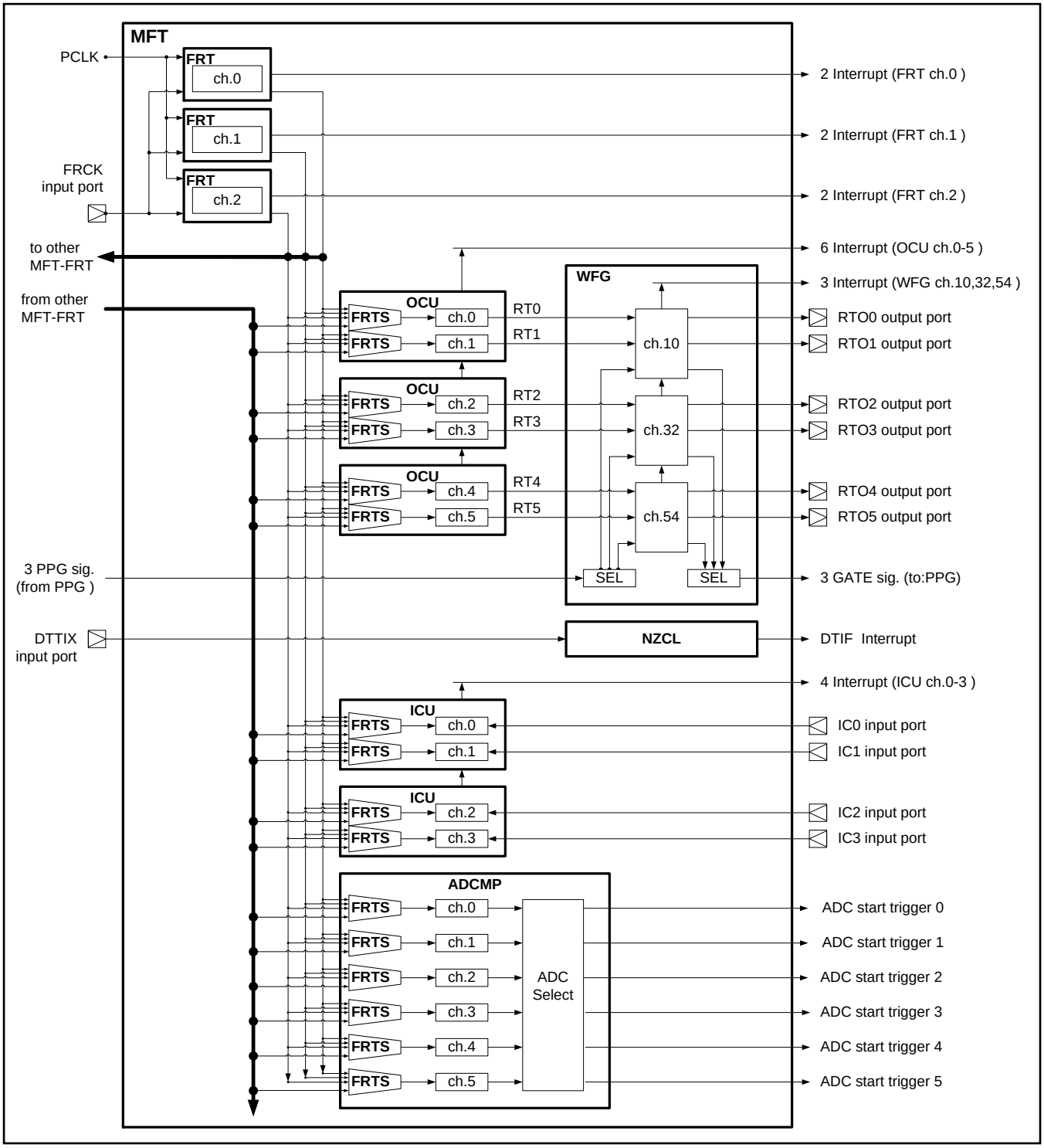
2.1 Block Diagram of the Multifunction Timer

This section explains the entire configuration of the Multifunction Timer (MFT).

2.1.1 Block Diagram

Figure 2-1 shows the block diagram of the entire function timer.

Figure 2-1 Block Diagram of MFT



2.1.2 Outline of Function Blocks

MFT (1 unit) consists of the following function blocks:

- FRT (Free-run Timer) Unit

  An FRT is a timer function block that outputs counter values for the operational criteria of the function blocks in the MFT. The MFT employs 3 channels.

- OCU (Output Compare Unit)

  An OCU is a function block that generates and outputs PWM signals on the basis of the counter values of the FRT. The OCU employs 6 channels (2 channels × 3 units).

- WFG (Waveform Generator) Unit

  A WFG is a function block that is located downstream from the OCU and generates signal waveforms for motor control from OCU output (RT0 to RT5) signals and PPG signals. The WFG employs 3 channels.

- NZCL (Noise Canceller) Unit

  An NZCL is a function block that generates DTIF interrupts to the CPU from external input signal (DTTIX signal) for motor emergency shutdown. The NZCL employs 1 channel.

- ICU (Input Capture) Unit

  An ICU is a function block that captures the FRT count value and generates an interrupt in the CPU when a valid edge is detected in an external input pin signal. The ICU employs 4 channels (2 channels × 2 units).

- ADCMP (ADC Start Compare Unit)

  An ADCMP is a function block that generates AD conversion start signals on the basis of the FRT counter value. The ADCMP employs 6 channels.

One MFT has a configuration that allows one 3-phase motor control to occur. Some products of this family incorporate multiple MFTs. They support multiple 3-phase motor control.

The MFT unit employs three FRTs, which can operate independently from one another. Inside the MFT, the output of the FRT counter value is connected to the OCU, ICU, and ADCMP. These units have a circuit (FRTS: Free-run Timer Selector) that selects the FRT to be connected. Interlocked operation can be performed based on the output of the counter value of the selected FRT. All of the units can be interlocked by a single FRT, or 2 or 3 groups can be formed as interlocked operational groups.

2.2 Description of Each Function Block

This section explains the configurations and operations of the functions in Multifunction Timer.

2.2.1 FRT: 3 Channels

An FRT is a timer function block that outputs the reference counter value for the operation of each function block in the MFT. Figure 2-2 shows the configuration of an FRT. An FRT consists of a clock prescaler, 16-bit Up/Down counter, cycle setting register (TCCP register) and controller.

- The clock prescaler divides the peripheral clock (PCLK) signal inside the LSI to generate the operating clock for the 16-bit Up/Down counter.
- The TCCP register sets the Peak value (the count cycle) and the offset values for the 16-bit Up/Down counter. It has a buffer register to change the settings during count operation.
- The 16-bit Up/Down counter performs Up-count or Down-count operation in the count cycle specified by the Peak value (the count cycle) and the offset values to output a counter value.

The following processing can be achieved by instructing the controller via the CPU.

- The division ratio of the clock prescaler can be selected.
- The use of PCLK (internal clock) and FRCK (external clock) can be selected.
- The count mode for the 16-bit Up/Down counter can be selected from below.
  - Normal Up-count mode
  - Normal Up/Down-count mode
  - Offset Up-count mode (After TYPE3-M4 products)
  - Offset Up/Down-count mode (After TYPE3-M4 products)
- The buffer register function of the TCCP register can be enabled or disabled.
- Interrupts can be generated in the CPU by detecting a case where the count value is set to "0x0000" or the peak value (= TCCP value) (two interrupt signals output per FRT1 channel).
- Generation of the interrupts can be masked at a specified ratio.
- Multiple FRTs can be started, stopped or cancelled at the same time.

Figure 2-2 Configuration of FRT

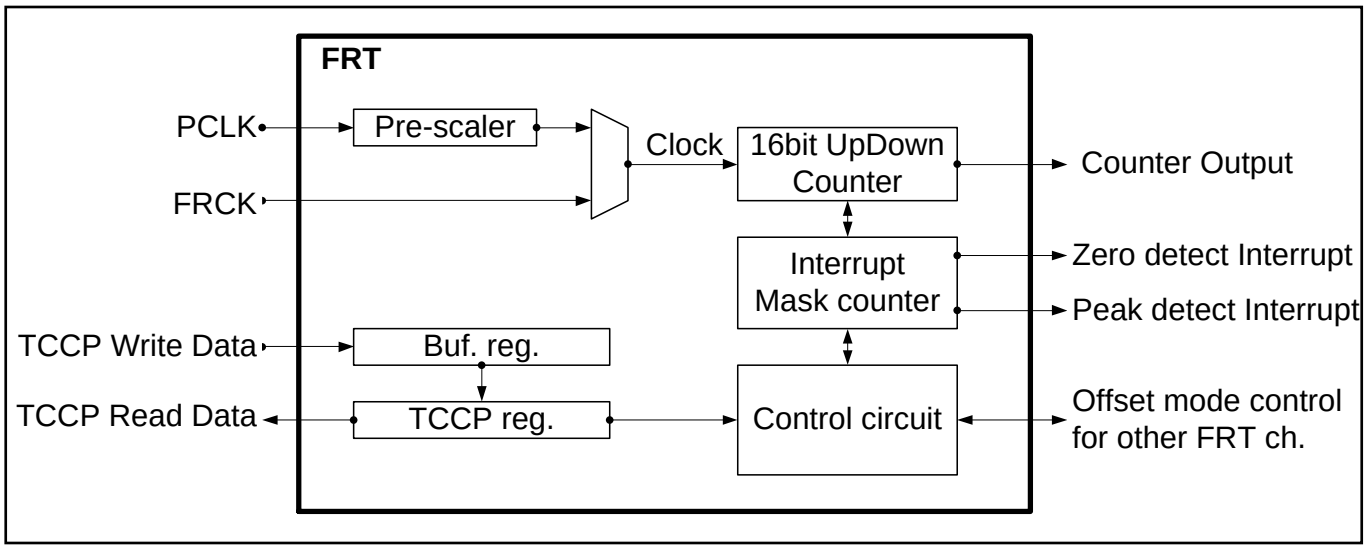


Figure 2-3 shows an example of FRT operation in Normal up-count mode.

Figure 2-3 Example of FRT Operation in Normal Up-count Mode

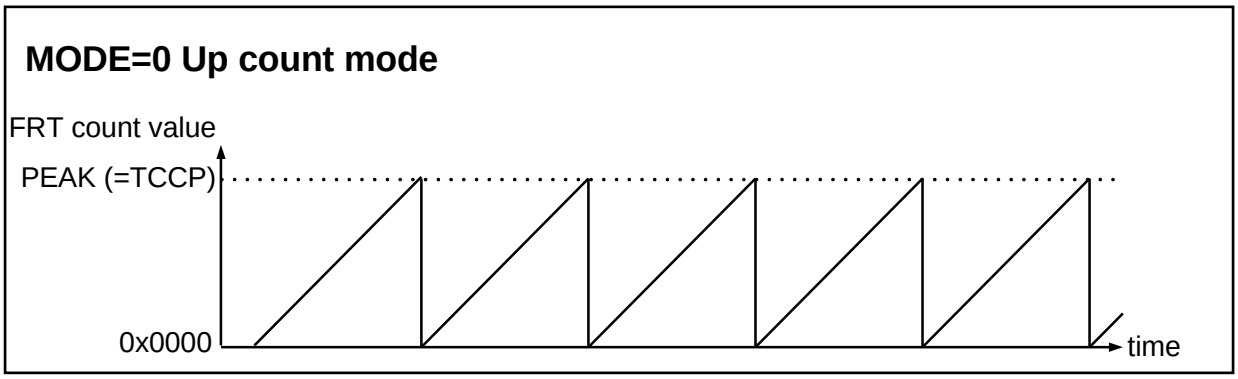


Figure 2-4 shows an example of FRT operation in Normal Up/Down-count mode.

Figure 2-4 Example of FRT Operation in Normal Up/Down-count Mode

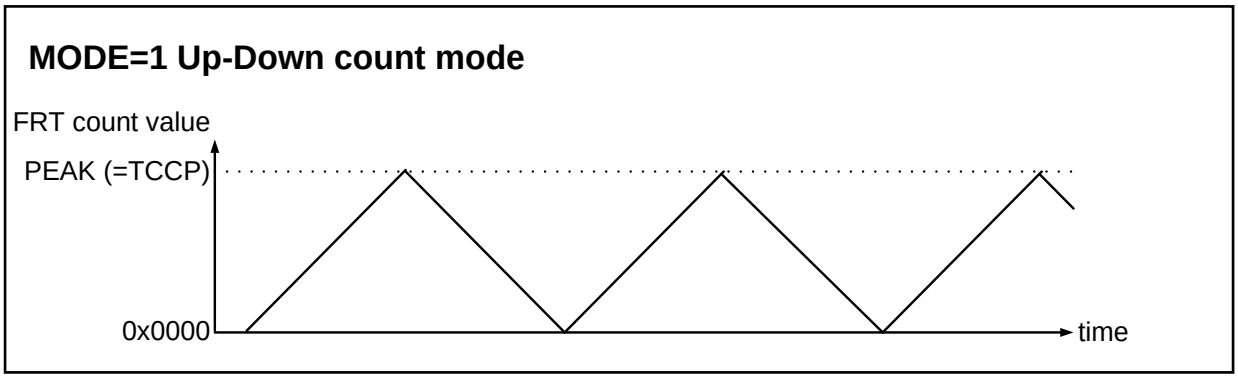
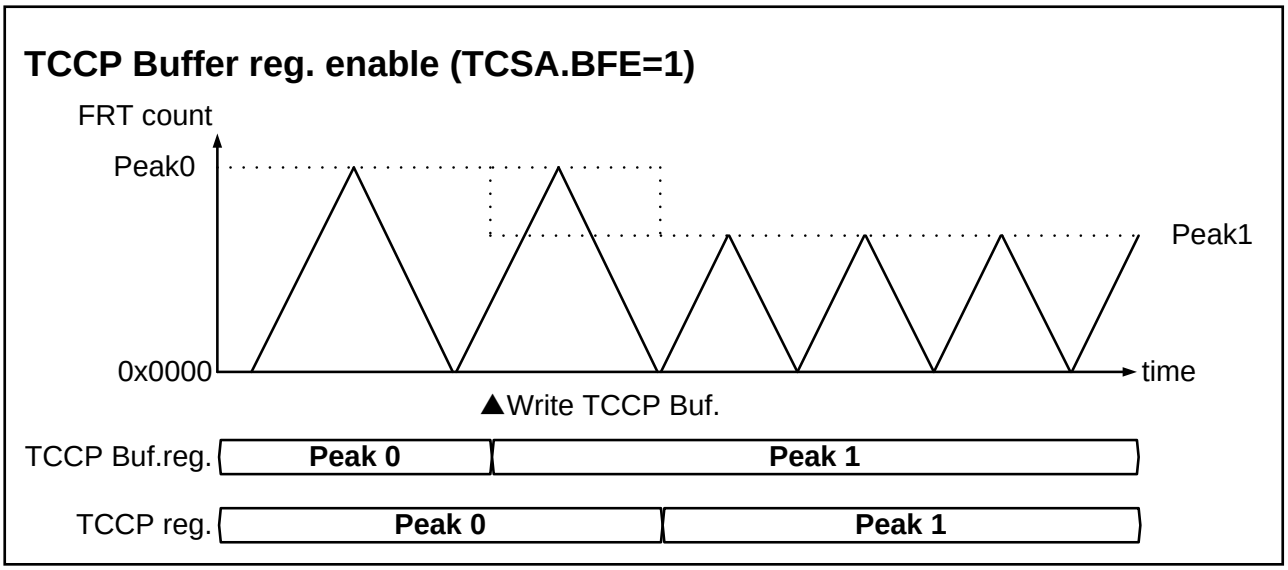


Figure 2-5 shows an example of FRT cycle change in Normal Up/Down-count mode using the buffer functions of the TCCP register.

Figure 2-5 FRT Cycle Change in Normal Up/Down-count Mode



2.2.2 OCU: 6 Channels (2 Channels × 3 Units)

An OCU is a function block that generates and outputs PWM signals based on the counter value of the FRT. The signal names of the PWM signals output by an OCU are RT0 to RT5. These signals are output to the LSI's external output pins via the WFG. Figure 2-6 shows the configuration of an OCU. An OCU consists of an FRTS, a compare value store register (OCCP register), an output condition change specification register (OCSE register), and a controller. The basic unit is in a 2-channel configuration with two sets of each circuit.

- FRTS is a circuit that selects the counter value of the FRT to be connected to the OCU for use.
- The OCCP register specifies the timing of PWM signal changes as the compare value for an FRT counter value. It has a buffer register to enable data to be written to the OCCP register asynchronously from an FRT's count operation.
- The OCSE register is used to specify change conditions of PWM signals. It has a buffer register to enable data to be written to the OCSE register asynchronously from an FRT's count operation.

The following processing can be achieved by instructing the controller from the CPU.

- The FRT to be connected to an OCU can be selected.
- Whether to enable or disable an OCU's operation can be specified.
- The output levels of signals RT0 to RT5 can be specified directly when an OCU's operation is disabled.
- When an OCU's operation is enabled, the output levels of signals RT0 to RT5 change based on the specification of the OCSE register when the FRT counter value is compared with the value of the compare value store register and it is detected that these values match or do not match.
- Change conditions for signals RT0, RT2 and RT4 can be specified arbitrarily by specifying an FRT value and a direction using the result of comparison with the OCCP0 register value.
- Change conditions for signals RT1, RT3 and RT5 can be specified arbitrarily by specifying an FRT value and a direction using the result of comparison with the OCCP0 and OCCP1 register values.
- Interrupts can be generated in the CPU when it is detected that the value of the OCCP register matches the FRT counter value.
- Whether or not to use the buffer register of the OOCP and OCSE registers and the timing of transfer can be selected.
- The Buffer transfer can be linked with an FRT interrupt mask. (After TYPE3-M4 products)

Each MFT contains three of these OCU's and consists of a total of 6 compare registers, 6 output signal pins and 6 interrupt outputs (2-channel × 3-unit configuration). The match detection signal between the OCCP register and an FRT is output to the ADCMP for ADCMP offset start mode.

Figure 2-6 Configuration of OCU

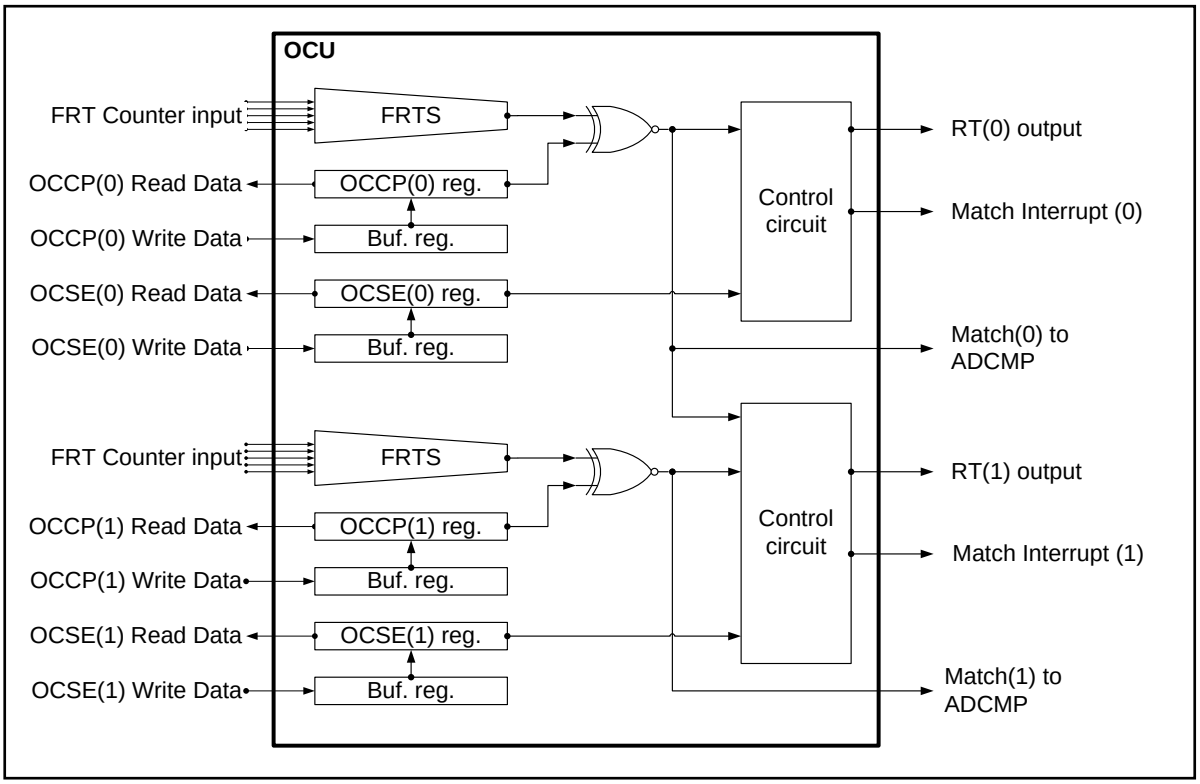


Figure 2-7 shows the output waveforms of signals RT0 and RT1, which are output from the OCU that is connected to the FRT in up-count mode.

Figure 2-7 Example of OCU Output Wave Form

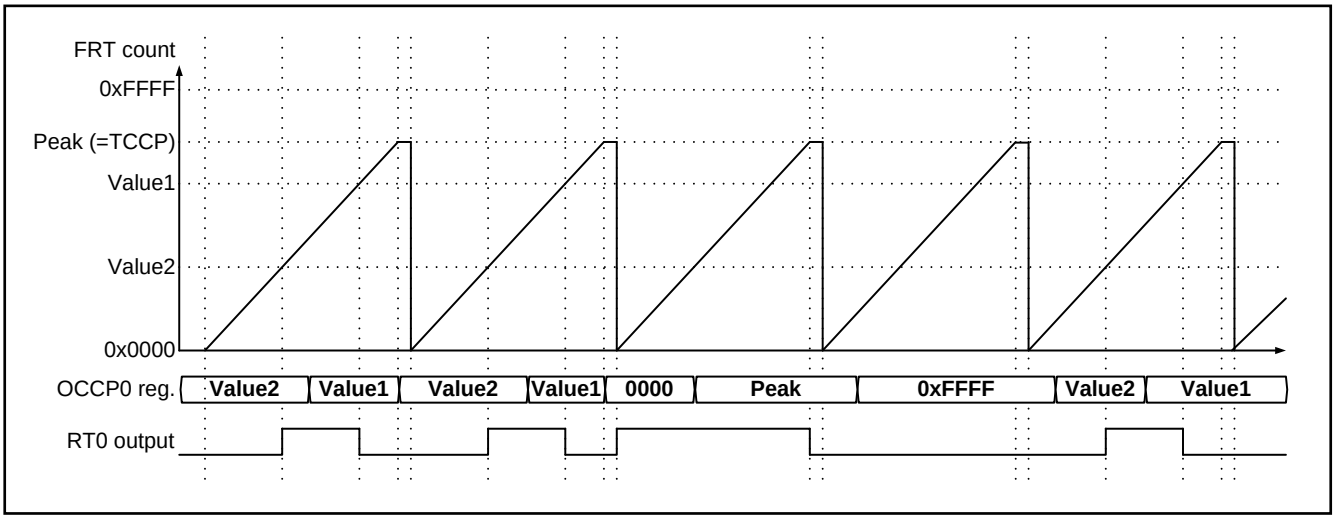
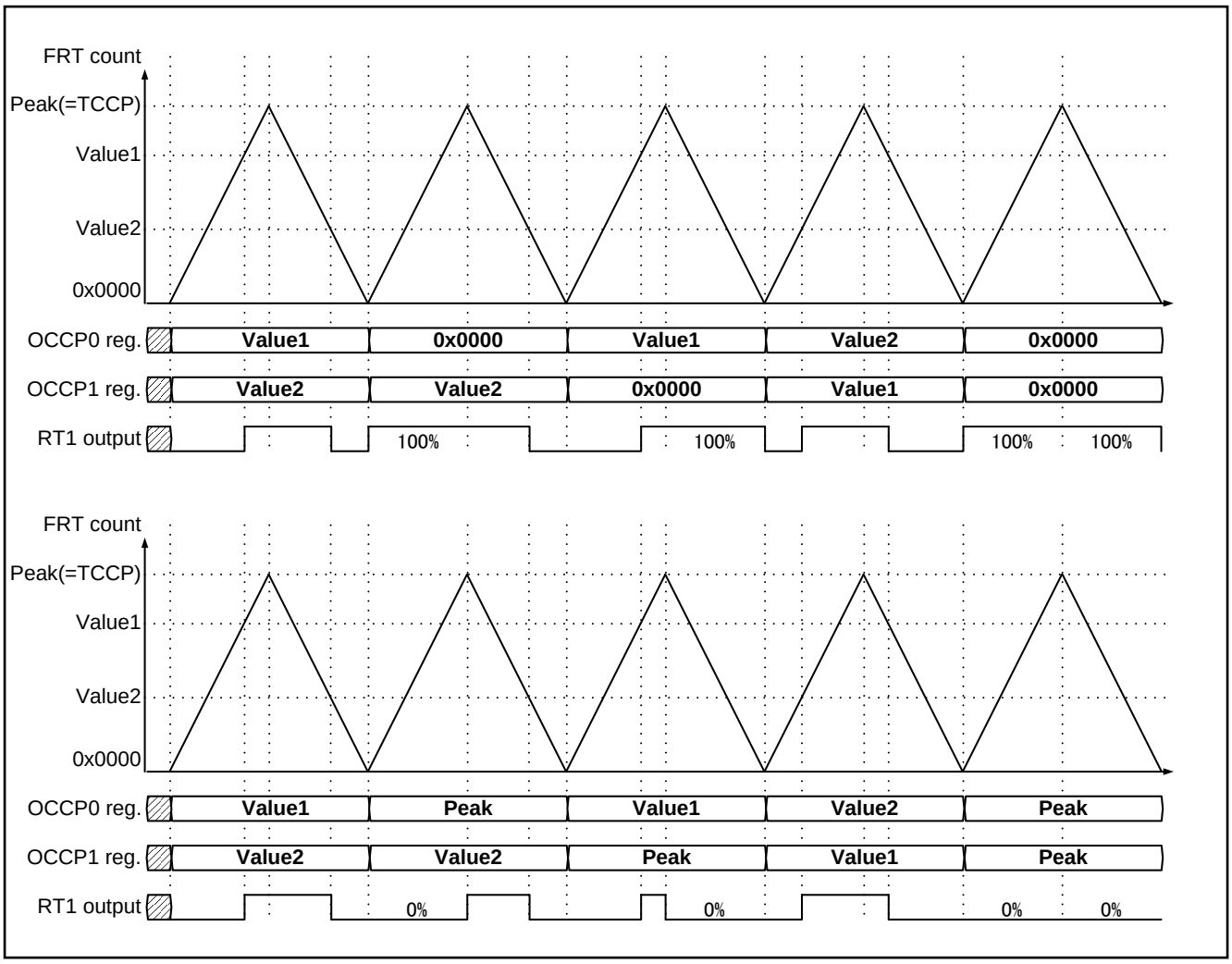


Figure 2-8 shows the output waveforms of signal RT1 output from an OCU that is connected to an FRT in up/down-count mode.

Figure 2-8 Example of OCU Output Waveform



2.2.3 WFG: 3 Channels

A WFG is a function block that is located downstream from an OCU and generates signal waveforms for motor control from OCU output signals (RT0 to RT5) and PPG signals (PPGs are located outside the multifunction timer). Figure 2-9 shows the configuration of a WFG. The signal outputs to LSI external pins from a WFG are called RTO0 to RTO5. They are divided into blocks: a block that outputs RTO0 and RTO1 from RT0 and RT1, respectively; a block that outputs RTO2 and RTO3 from RT2 and RT3, respectively; and a block that outputs RTO4 and RTO5 from RT4 and RT5, respectively. These blocks are called WFG ch.10, WFG ch.32 and WFG ch.54, respectively. A WFG consists of a clock prescaler, a WFG timer, a WFG timer initial value register (WFTA and WFTB registers), a pulse counter, a pulse counter initial value register (WFTF register), a waveform generator, PPG timer unit selectors, and a controller.

- The clock prescaler divides the peripheral clock signal (PCLK) inside the LSI to generate the operating clock for a WFG timer.
- A WFG timer is a timer circuit that counts the time set by the WFTA and WFTB registers and generates signal waveforms.
- The pulse counter is a timer circuit that counts the time set by a WFTF and performs a filtering process for signals RT0 to RT5, and PPGs.
- The pulse counter in a mode that does not perform a filtering process can be used as a single reload timer allowing periodical interrupts in the CPU. Each WFG has one reload timer interrupt output.
- The waveform generator is a block that generates LSI external output signals through waveform generation processing based on signals RT0 to RT5 from an OCU, signals from a PPG, and the count state of a WFG timer.
- A PPG timer unit selector is a circuit that selects the PPG timer unit to be used by a WFG. It selects the output destination of the instruction signal (GATE signal) for PPG activation and PPG output signals.

The following processing can be achieved by instructing the controller from the CPU.

- The division ratio of the clock prescaler can be selected.
- The following modes are available and can be selected for wave generation.
  - Through mode:
  - This mode allows through output for input signals from OCUs and PPGs.
  - RT-PPG mode: This mode allows the superimposition of the input signal from an OCU onto the input signal from a PPG for output (Figure 2-10).
  - Timer-PPG mode: This mode allows the activation of a WFG timer with input signals from an OCU, and outputting of the input signal from a PPG for the timer count period specified by WFTA and WFTB (Figure 2-11).
  - RT-dead timer mode: This mode allows the generation of a 2-phase non-overlapping signal with the RT1 input signal from an OCU. Dead time for output signals can be specified separately with WFTA and WFTB (Figure 2-12, Figure 2-13).
  - RT-dead timer filter mode: This mode allows the filtering of RT1 input signals from an OCU with a pulse width value of WFTF or less, and the generation of a 2-phase non-overlapping signal. Dead time for output signals can be specified separately with WFTA and WFTB.
  - PPG-dead timer mode: This mode allows the generation of a 2-phase non-overlapping signal from the input signal from a PPG. Dead time for output signals can be specified separately with WFTA and WFTB.
  - PPG-dead timer filter mode: This mode allows the filtering of input signals from a PPG with a pulse width value of WFTF or less, and the generation of a 2-phase non-overlapping signal. Dead time for output signals can be specified separately with WFTA and WFTB.

- A GATE signal can be output to instruct a PPG to start up.
- The polarity of outputs for signals RTO0 to RTO5 can be inverted.

Figure 2-9 Configuration of the WFG

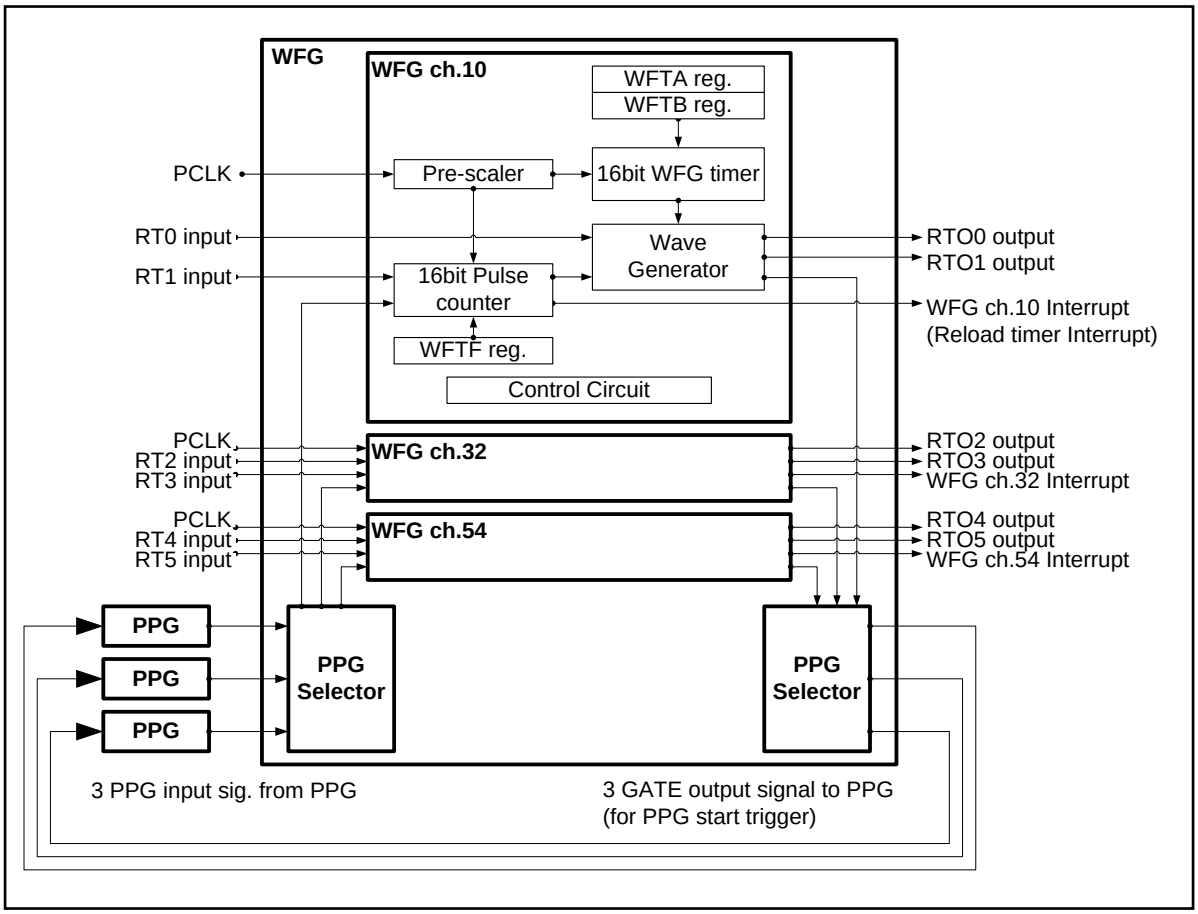


Figure 2-10 Example of Operation in RT-PPG Mode

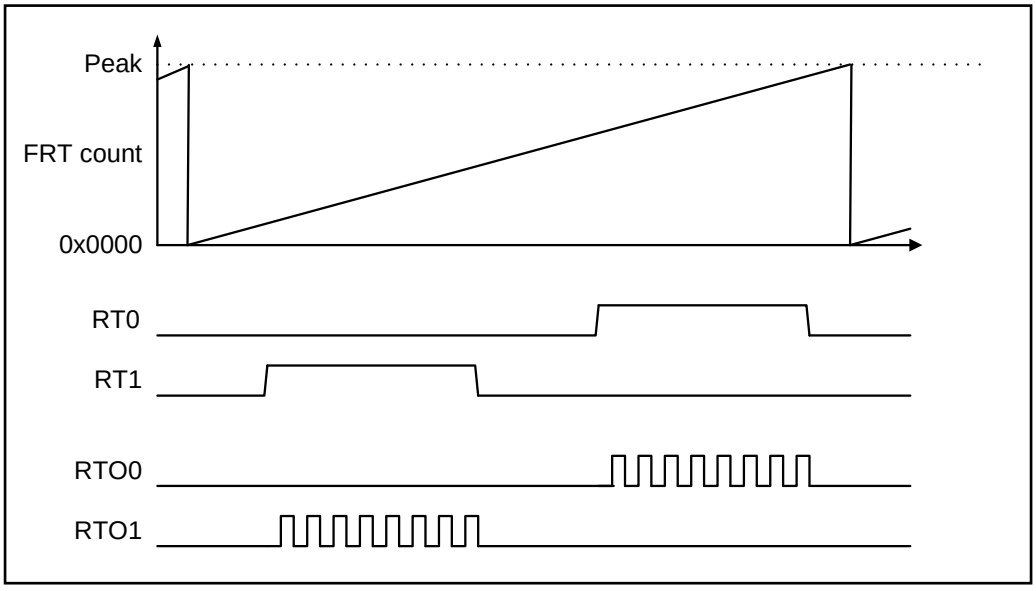


Figure 2-11 Example of Operation in Timer-PPG Mode

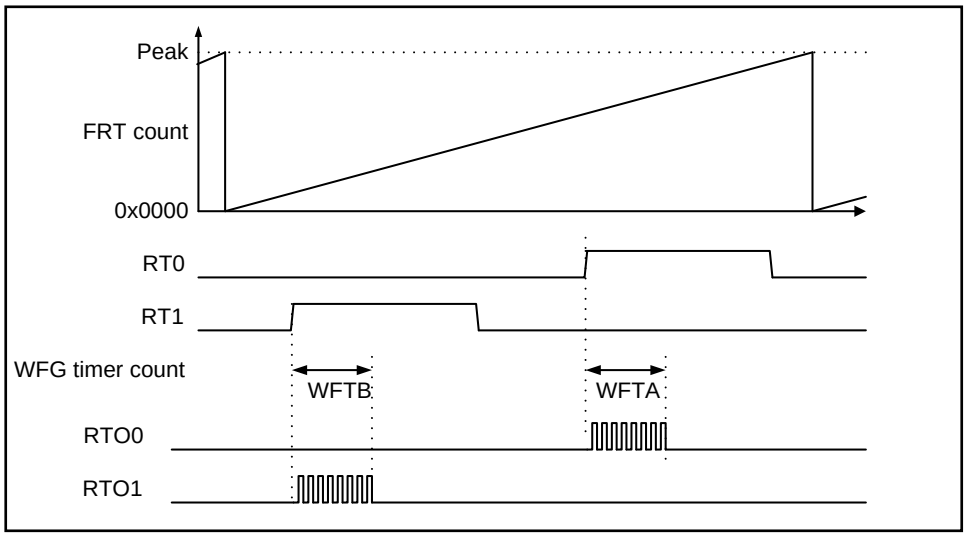


Figure 2-12 Example of Operation in RT-dead Timer Mode (When FRT is in Normal Up/Down-count Mode)

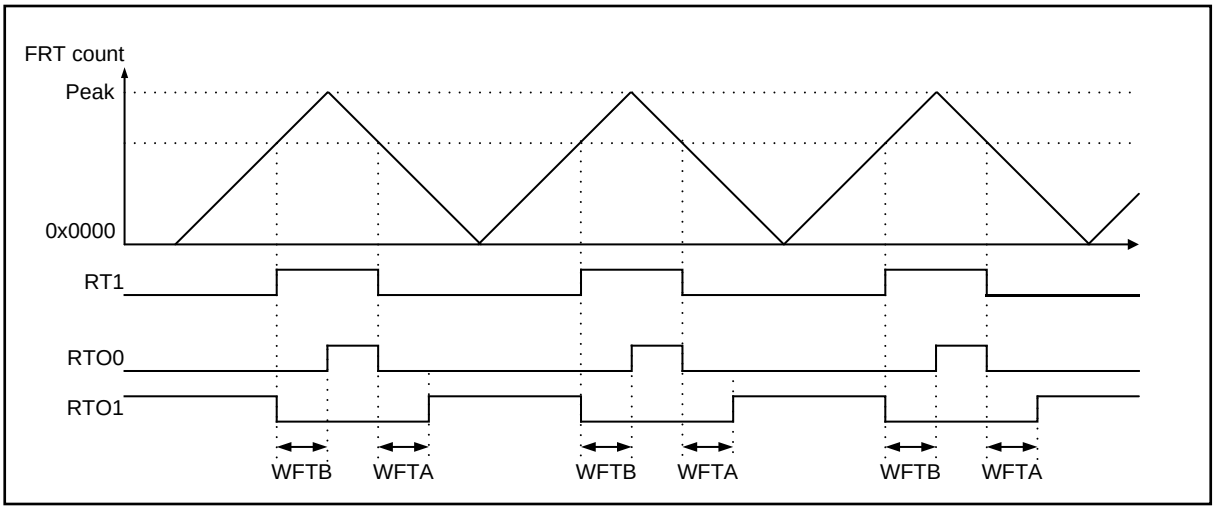
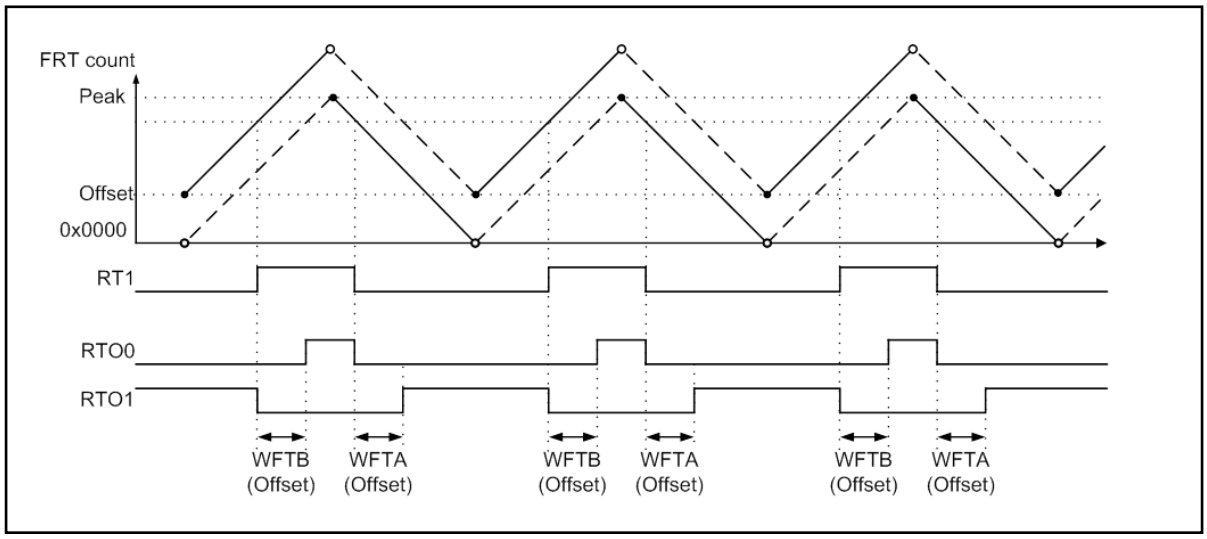


Figure 2-13 Example of Operation in RT-dead Timer Mode (When FRT is in Offset Up/Down-count Mode)

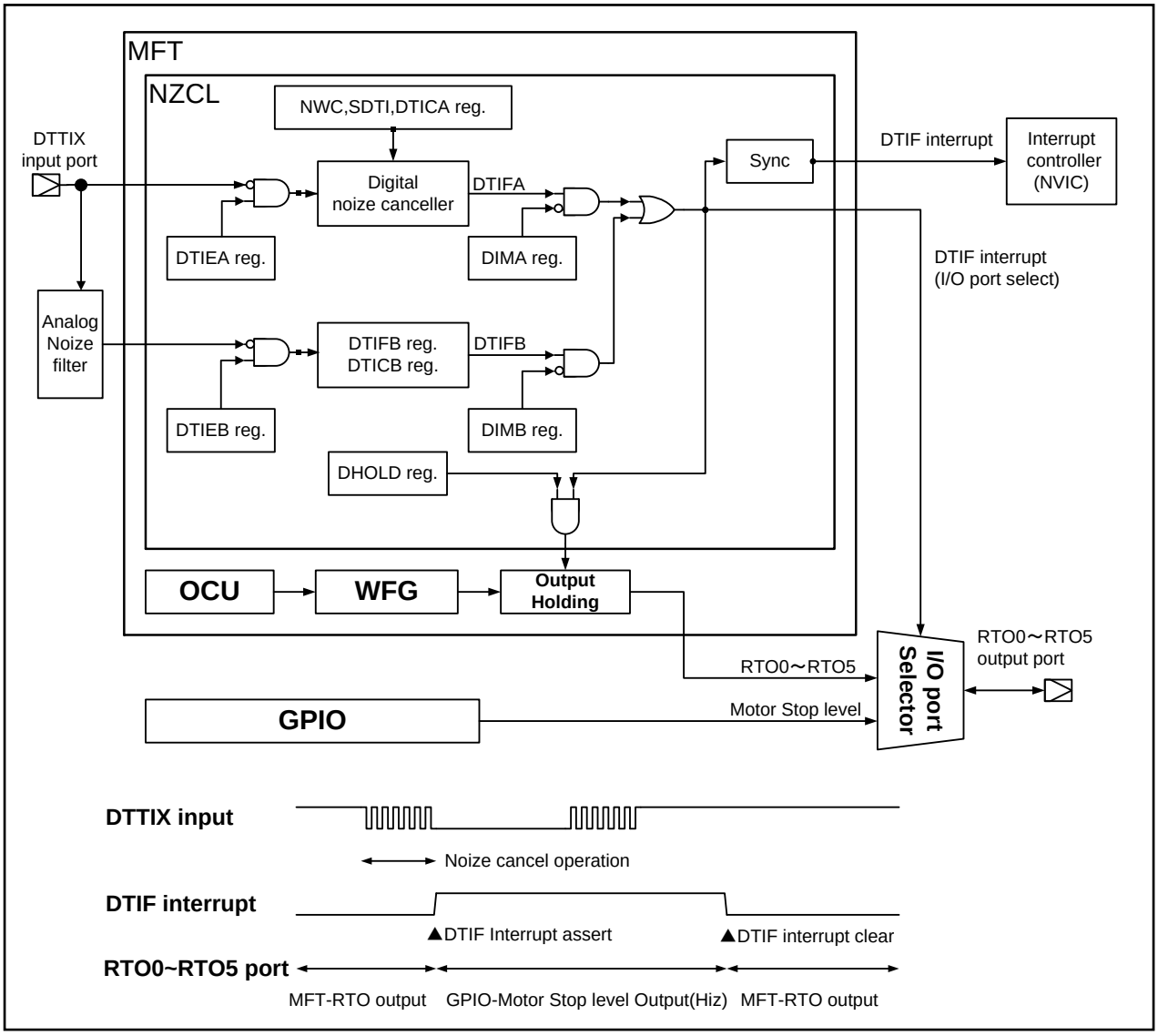


2.2.4 NZCL

An NZCL is a function block that generates DTIF interrupts from the specific input signal (DTTIX signal) for emergency motor shutdown. Figure 2-14 shows the configuration of an NZCL and I/O port selector. An NZCL consists of a digital noise canceller and a controller.

- DTIF interrupts can be generated from the DTIF input signals via the digital noise canceller.
- DTIF interrupts can be generated from the DTIF input signals via an analog noise filter with no clock without going through the digital noise canceller. (The path passing through the analog noise filter in the figure is shown below. This function is available only in TYPE3-M4 products and later.)
- It can be switched to the state of the GPIO port, which is also used for WFG's external output signals (RTO0 to RTO5), using the selection function of the I/O port block while a DTIF interrupt is being generated. Emergency shutdown of the motor can be performed by setting the I/O state of the GPIO port to the Motor Stop level. If clockless DTIF interrupt signal is enabled, the motor can perform an emergency stop of the motor even if the MCU clock is in a stopped state.
- While a DTIF interrupt is being generated, an output holding function selected by the DHOLD register can be used to hold the output level for WFG external output signals (RTO0 to RTO5) immediately before the DTIF interrupt is generated.

Figure 2-14 Configuration of NZCL and I/O Port Selector



2.2.5 ICU: 4 Channels (2 Channels × 2 Units)

An ICU is a function block that captures an FRT count value and generates an interrupt in the CPU when a valid edge is detected at an external input pin signal. Figure 2-15 shows the configuration of an ICU. An ICU consists of an FRTS, an edge detector, a 16-bit capture register and a control register. Its basic unit is in a 2-channel configuration with two sets of each circuit.

- An FRTS is a circuit that selects the counter value of the FRT to be connected to ICU for use.
- An edge detector is a circuit that detects the valid edge of an input signal.
- The ICCP register captures the timing of input signal changes as an FRT's count value.

The following processing can be achieved by instructing the controller from the CPU.

- The FRT to be connected to an ICU can be selected.
- The valid edge of the input signal can be selected from the rising edge, the falling edge or both edges.
- Whether to enable or disable an ICU's operation can be specified.
- An interrupt can be generated in the CPU when a valid edge is detected and the capture operation is performed.

Each MFT contains 2 ICU's and consists of a total of 4 external input pins and 4 capture registers (2-channel × 2-unit configuration). The LSI external input signals to an ICU are called IC0 to IC3. Some ICU input signals can be switched to LSI's internal signals for use, other than LSI external pins, using the selection function of the I/O port block (See 2.3 I/O Pins of the Multifunction Timer Unit for more details). Figure 2-16 shows an example of ICU operation.

Figure 2-15 Configuration of ICU

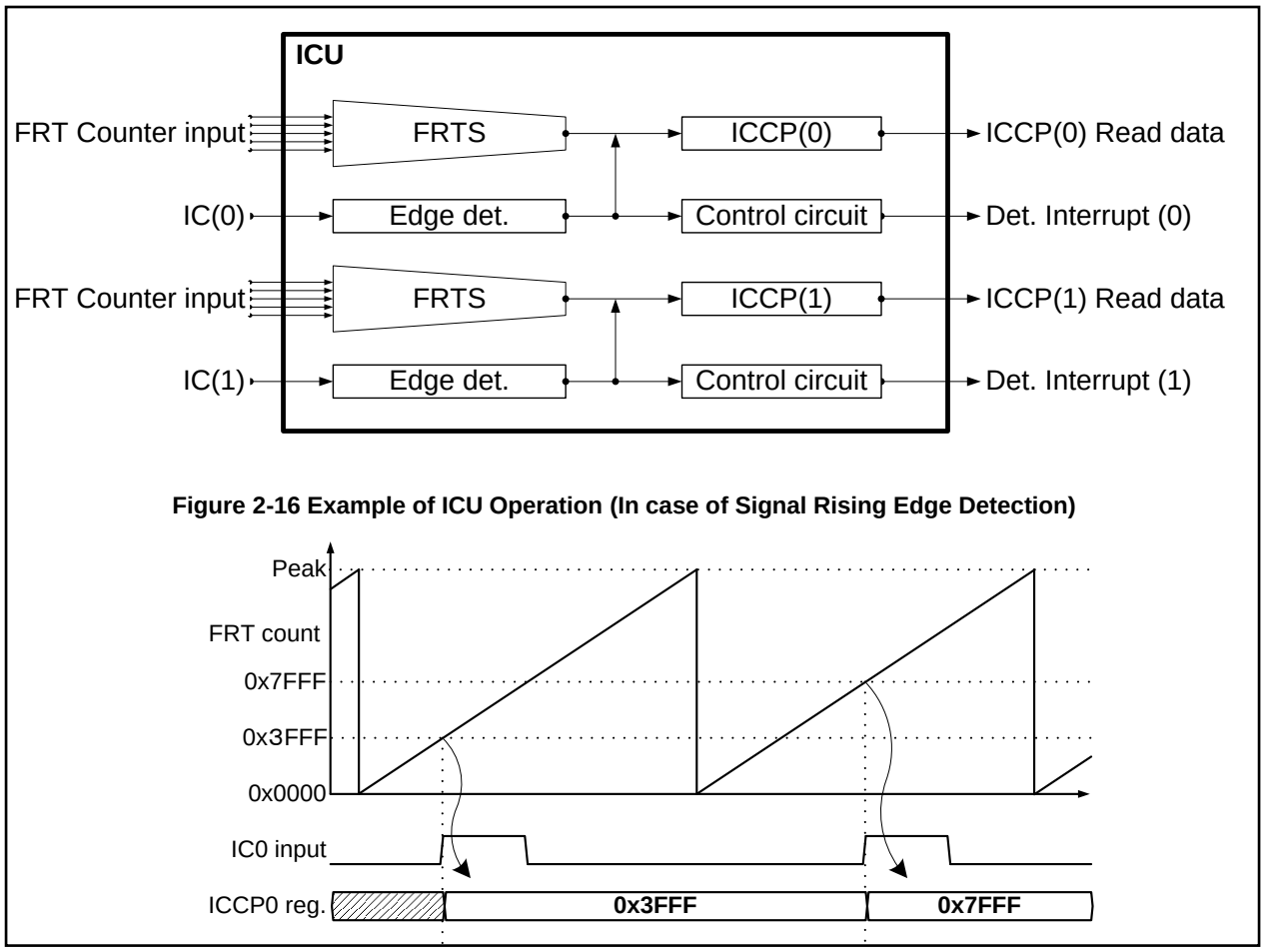


Figure 2-16 Example of ICU Operation (In case of Signal Rising Edge Detection)

2.2.6 ADCMP: 6 Channels

An ADCMP is a function block that generates AD conversion start signals based on the counter value of an FRT. An ADCMP consists of 6 channels. Figure 2-17 shows the configuration of an ADCMP. An ADCMP consists of an FRTS, compare registers (ACMP register), an offset start down counter, an output selector and a control register.

- An FRTS is a circuit that selects the counter value of the FRT to be connected to an ADCMP for use.
- In normal mode, the ACMP register is used to specify the AD conversion start timing as a compare value for an FRT counter value.
- In offset start mode, the ACMP register is used to specify an offset delay time until AD conversion start after a match is detected by an OCU.
- Both the ACMP and the FRT have a buffer register so that writing to the ACMP register can be done asynchronously from the FRT's count operation.
- An offset down counter is used in offset start mode. When an OCU detects a match with the OCCP, it counts the time (offset time) specified by the ACMP register and generates an AD conversion start signal.
- An output selector is used to select the ADC to which the generated AD conversion start signal will be sent.

The following processing can be achieved by instructing the controller from the CPU.

- The FRT to be connected to an ADCMP can be selected.
- Whether to enable or disable ADCMP operations can be specified.
- The ADC to output an AD conversion start signal can be selected.
- In normal mode, the timing of AD conversion start can be set by specifying an FRT value and a direction.
- In offset start mode, the match detection timing in an OCU can be set by specifying an FRT value and a direction, and an offset time from that point until AD conversion start can be set.
- Whether or not to use the ACMP's buffer register can be specified and the timing of transfer from the buffer register can be selected.
- Buffer transfer can be linked with an FRT interrupt mask. (TYPE3-M4 products and later only)
- The ACMC register can be used to perform ADC start linked with an FRT interrupt mask. (TYPE3-M4 products and later only)

After the start signals from an ADCMP to each ADC are selected by the output selector of each respective channel, they are processed as a logical OR per the respective ADC unit and output. Selecting the same ADC unit for multiple ADCMP channels allows the setting of up to 12 ADC conversion start times during one FRT cycle.

Figure 2-17 Configuration of ADCMP

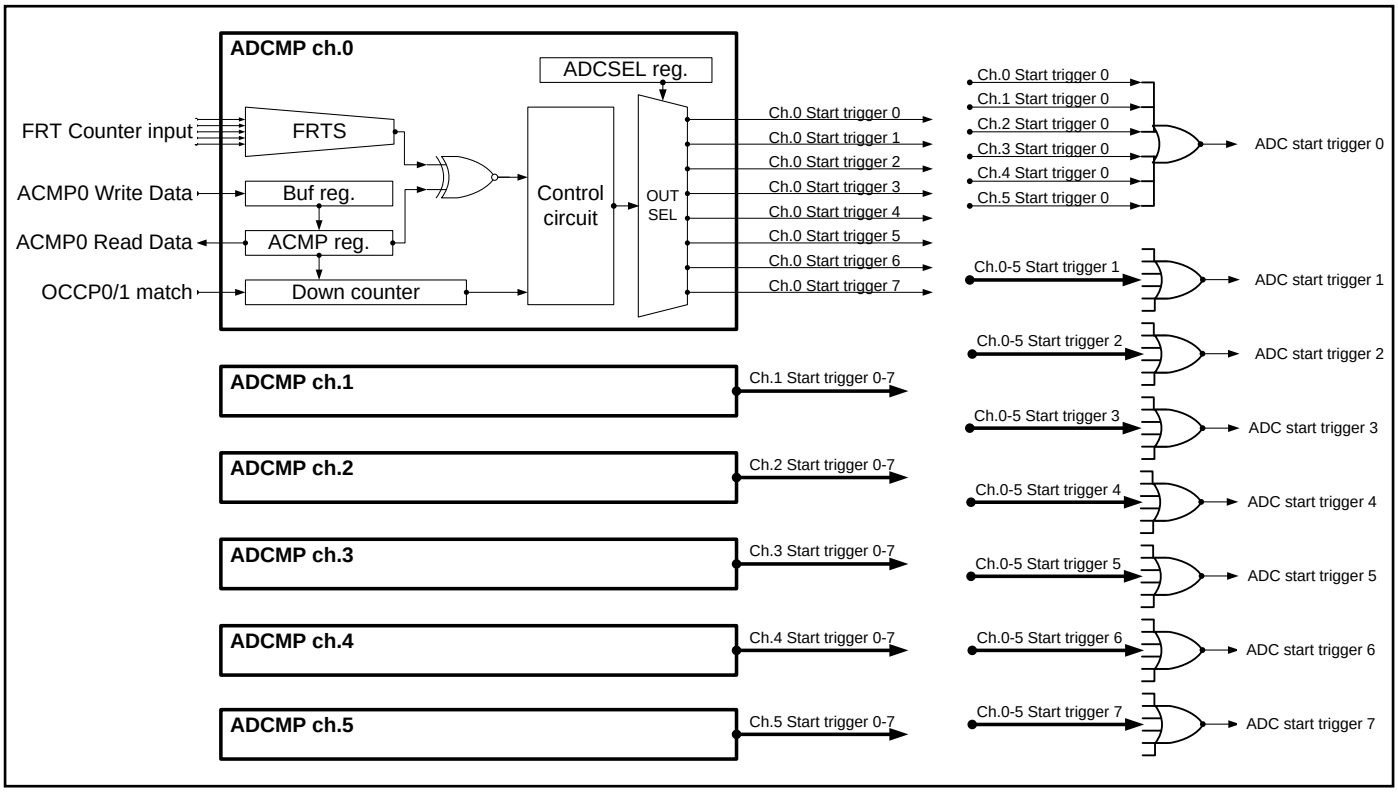


Figure 2-18 shows an example of ADCMP operation in normal mode with parallel use of 2 channels.

Figure 2-18 Example of ADCMP Operation in Normal Mode

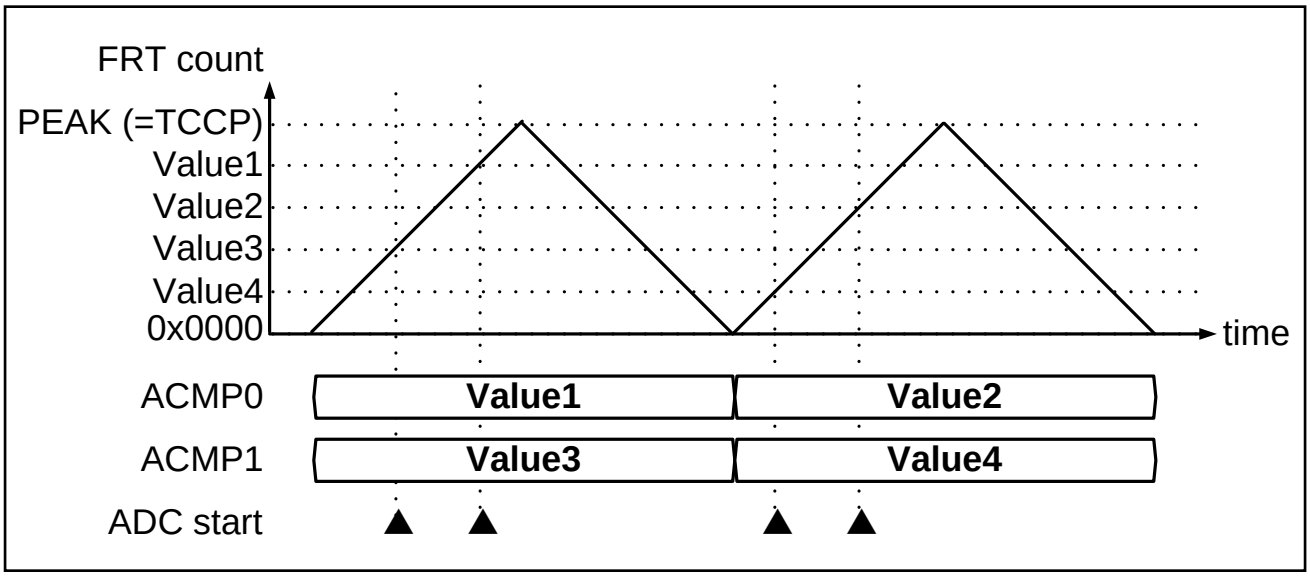


Figure 2-19 shows an example of ADCMP operation in offset start mode.

Figure 2-19 Example of ADCMP Operation in Offset Mode

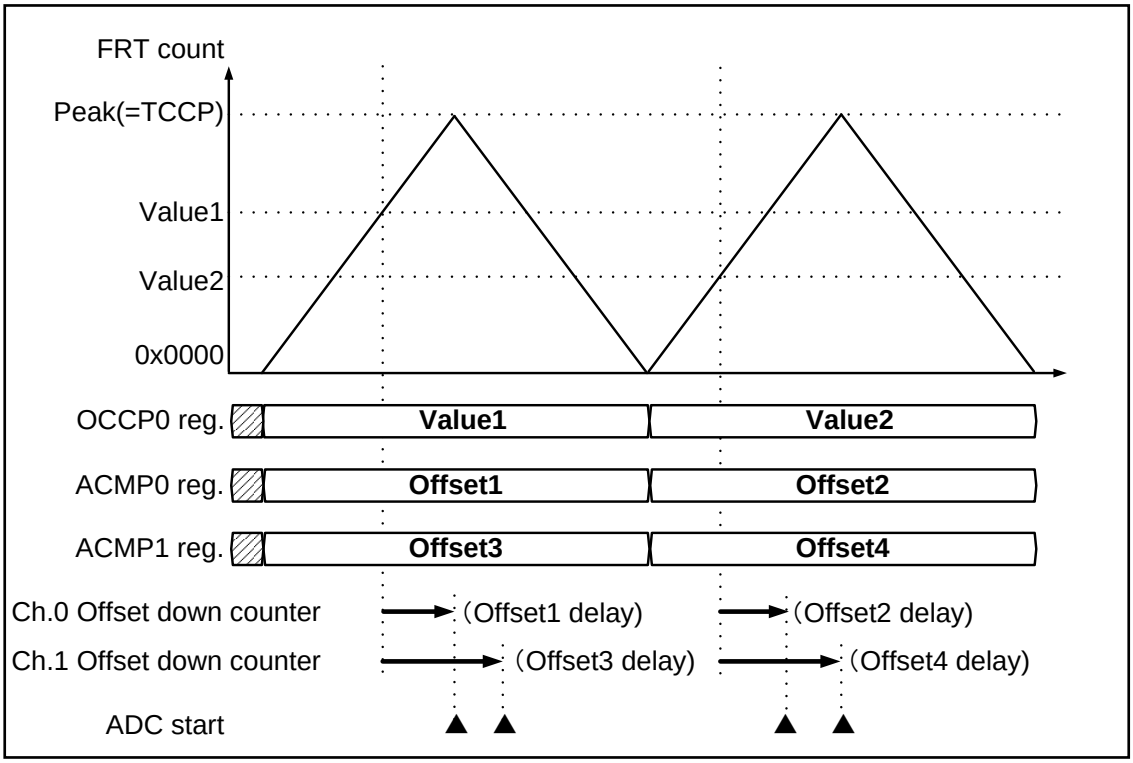
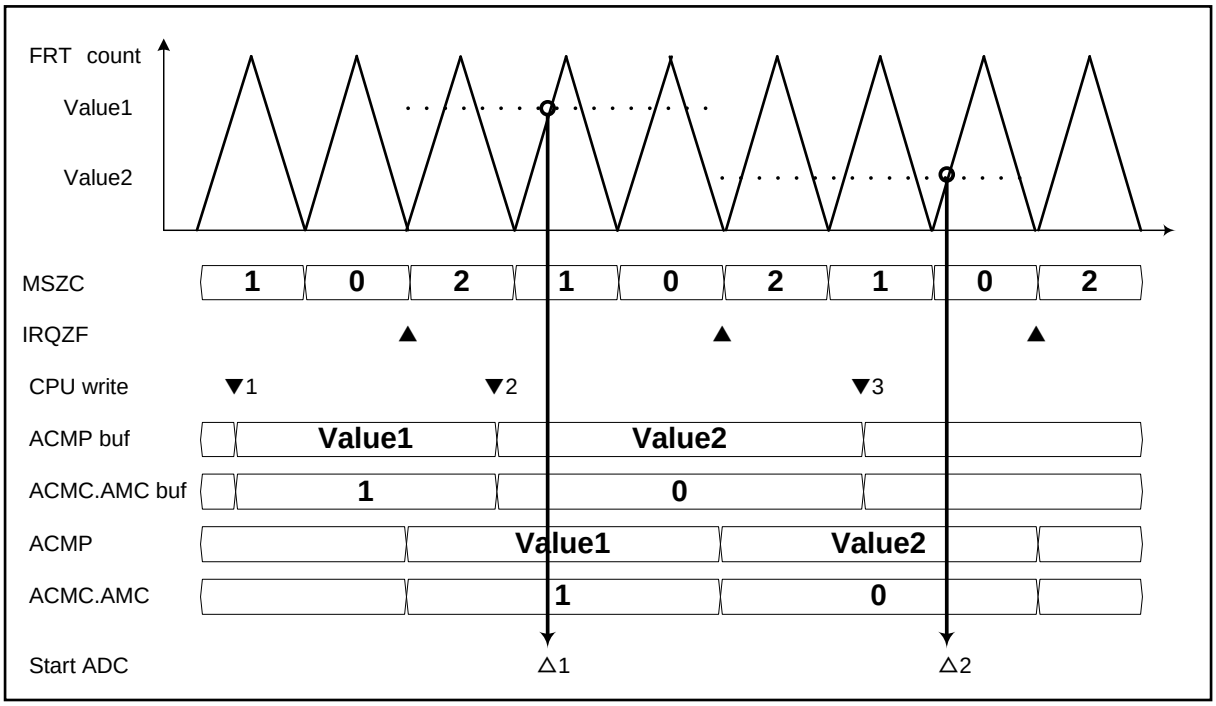


Figure 2-20 shows an example of ADC Start linked with FRT interrupt mask counter.

Figure 2-20 ADC Start Linked with FRT Interrupt Mask Counter



2.3 I/O Pins of the Multifunction Timer Unit

This section explains the I/O pins of the multifunction timer unit.

2.3.1 Correspondence with External I/O Pins

Of all the I/O signals illustrated in the block diagram of Figure 2-1, Table 2-1 shows a list of the correspondence between MFT unit I/O pins and LSI external I/O pins. In this series, some models have more than one MFT unit. Therefore, LSI pin names are composed of the I/O pin names shown in the block diagram Figure 2-1, plus the MFT's unit number (0, 1, 2). It should be noted that descriptions in this chapter are based on the pin names shown in the block diagram Figure 2-1.

Table 2-1 Correspondence Table for MFT Unit I/O Pins and External I/O Pins

Name of the MFT Unit Pin (Pin Name in Figure 2-1)	Function	External Pin Name		
		MFT-unit0	MFT-unit1	MFT-unit2
FRCK	FRT external input clock	FRCK0	FRCK1	FRCK2
DTTIX	Motor emergency shutdown request input	DTTI0X	DTTI1X	DTTI2X
RTO0	WFG→PWM output ch.0	RTO00	RTO10	RTO20
RTO1	WFG→PWM output ch.1	RTO01	RTO11	RTO21
RTO2	WFG→PWM output ch.2	RTO02	RTO12	RTO22
RTO3	WFG→PWM output ch.3	RTO03	RTO13	RTO23
RTO4	WFG→PWM output ch.4	RTO04	RTO14	RTO24
RTO5	WFG→PWM output ch.5	RTO05	RTO15	RTO25
IC0	ICU input ch.0	IC00	IC10	IC20
IC1	ICU input ch.1	IC01	IC11	IC21
IC2	ICU input ch.2	IC02	IC12	IC22
IC3	ICU input ch.3	IC03	IC13	IC23

The ICU's input pins can be switched with the following LSI internal signals, in addition to the external pin inputs, using the selector function of the I/O port block.

- SYNC signal when the LYN function of the multifunction serial block is used
- Internal CR oscillator/oscillation frequency trimming input signal

For details, see the chapter I/O Port in the Peripheral Manual.

2.3.2 Interrupt Signal Outputs

Of all the I/O signals illustrated in the block diagram of Figure 2-1, Table 2-2 shows a list of interrupt signals generated from the MFT unit. Any model that contains more than one MFT unit has interrupt outputs equivalent to the number of mounted MFT units.

Table 2-2 List of Interrupt Signals Generated from MFT Unit

Generation Block	Interrupt Type
FRT ch.0	Zero value detection interrupt
FRT ch.1	Zero value detection interrupt
FRT ch.2	Zero value detection interrupt
FRT ch.0	Peak value detection interrupt
FRT ch.1	Peak value detection interrupt
FRT ch.2	Peak value detection interrupt
OCU ch.0	Match detection interrupt
OCU ch.1	Match detection interrupt
OCU ch.2	Match detection interrupt
OCU ch.3	Match detection interrupt
OCU ch.4	Match detection interrupt
OCU ch.5	Match detection interrupt
ICU ch.0	Input signal edge detection interrupt
ICU ch.1	Input signal edge detection interrupt
ICU ch.2	Input signal edge detection interrupt
ICU ch.3	Input signal edge detection interrupt
NZCL	DTIF interrupt (emergency motor shutdown interrupt)
WFG ch.10	WFG10 reload timer interrupt
WFG ch.32	WFG32 reload timer interrupt
WFG ch.54	WFG54 reload timer interrupt

2.3.3 Other I/O Signals

The following section explains the other signals shown in the bock diagram Figure 2-1.

- PCLK

This is an LSI internal peripheral clock signal used in the MFT unit. It uses the clock signal of the APB bus to be connected. The FRT (when the internal peripheral clock is selected), the WFG timer, and pulse counter operate based on the count clock divided from a PCLK.

- FRT input and FRT output of external MFT

Models that contain more than one MFT unit can use the FRT count output for the other MFTs. This connection configuration allows OCU, ICU and ADCMP mounted separately on multiple MFT units to be interlocked by a single FRT.
(Models that contain 2 MFT units can output 12 channels of PWM simultaneously. Models that contain 3 MFT units can output 18 channels of PWM simultaneously.
For details, see 4.8 FRT Selection of OCU, ICU, and ADCMP.

- GATE signal / PPG signal

A GATE signal is a PPG start signal that is output from an MFT and input into a PPG. A PPG signal is output from a PPG and input into an MFT. The PPG units that will be connected for these signals vary depending on the mounted MFT unit. For details of their connection, see 4.9 PPG Timer Unit Connected to WFG.

- AD conversion start signal

As shown in Table 2-3, AD conversion start signals are connected to the scan start signals and priority start signals of each ADC that is outside of the MFT. Select the ADCMP output destinations according to the start triggers of the ADCs to be started.

Table 2-3 Destination for AD Conversion Start Signals

Output Signal Name	Destination for ADC
ADC start trigger 0	ADC unit0 scan conversion start
ADC start trigger 1	ADC unit0 priority conversion start
ADC start trigger 2	ADC unit1 scan conversion start
ADC start trigger 3	ADC unit1 priority conversion start
ADC start trigger 4	ADC unit2 scan conversion start
ADC start trigger 5	ADC unit2 priority conversion start
ADC start trigger 6	Not connected
ADC start trigger 7	Not connected

In models that contain more than one MFT unit, start signals undergo a logical OR for each ADC unit, and are used in each ADC unit. For details, see the chapter A/D Converter in Analog Macro Part.

2.4 Function Differences by Product Type

Among the functions of the multifunction timer unit, specific functions and operation vary depending on the installed product type. Table 2-4 shows the function differences by product type. For further details, see the respective chapter.

Table 2-4 Function Differences by Product Type

Function	Refer to	Applicable Control Register	TYPE1-M4	TYPE2-M4	TYPE3-M4 TYPE4-M4 TYPE5-M4	TYPE6-M4
FRT counter mode operation with offset	3.3.3 4.1.2	TCSD.OFMD1 TCSD.OFMD2	Function not included		Function included	
OCU/ADCMP/ICU connected FRT selection range	3.3.7 3.3.20 3.3.24 4.8	OCFS.FSO0 OCFS.FSO1 ICFS.FSI0 ICFS.FSI1 ACFS.FSA0 ACFS.FSA1	Selectable ranges for TYPE1-M4 and TYPE2-M4 are identical		Selectable range is expanded	Selectable range is expanded Product mounting 2 units and independent 1unit
FRT mask counter linked with OCU buffer transfer	3.3.11 3.3.12 4.2.4	OCSD.OPBM0 OCSD.OPBM1 OCSD.OEBM0 OCSD.OEBM1	Function not included		Function included	
OCU comparison condition expansion	3.3.12	OCSD.OFEX0 OCSD.OFEX1	Function not included		Function included	
WFG RT dead timer and filter mode operation, PPG dead timer and filter mode operation	3.3.15 4.4.11	WFSA.TMD	Some operations differ from TYPE2-M4 products and later.	Operations for TYPE2-M4 and later are identical.		
DTTIX digital noise filter cancel width	3.3.18	NZCL.NWS	Selectable ranges for TYPE1-M4 and TYPE2-M4 are identical		Selectable range is expanded	
RTO holding function at DTIF assert	3.3.18	NZCL.DHOLD	Function not included		Function included	
Clockless DTIF function	3.3.18	NZCL.DTIEB NZCL.DIMB WFIR.DTIFB WFIR.DTICB	Function not included		Function included	
ADCMP buffer transfer linked with FRT mask counter	3.3.26 4.6.4	ACSC.APBM	Function not included		Function included	
ADCMP ADC start linked with FRT mask counter	3.3.29 4.6.5	ACMC.MZCE ACMC.MPCE ACMC.AMC	Function not included		Function included	

3. Registers of the Multifunction Timer

This chapter explains the registers of the multifunction timer.

3.1. Individual Notations and Common Notations of Channel Numbers in Descriptions of Functions
3.2. List of Multifunction Timer Registers
3.3. Details of Register Functions

3.1 Individual Notations and Common Notations of Channel Numbers in Descriptions of Functions

This section explains the individual notations and common notations of channel numbers in the descriptions of functions in this chapter.

Because the multifunction timer unit contains multiple identical function blocks and consists of multiple channel circuits, there are some common issues across all the channels. Where there is no need to distinguish among the channels, and functions that are common to all of the channels are being explained, notations that are without channel numbers and with parentheses (common notations) are used to avoid repeated explanations and to simplify explanations. Where there is a need to make distinctions in explaining operations among channels, I/O signals or control registers, a notation clearly stating the channel numbers (individual notation) is used for such explanations. The rules of notation and some examples are provided below.

- Where channel numbers are notated directly, that indicates individual notation.
  This notation indicates that the operation, I/O signal or control register of the corresponding channel is being explained.
- Some control registers control 2 channels at the same time. In such cases, the two corresponding channel numbers are stated in individual notation to distinguish between them.
- Where channel numbers are omitted from a notation, it indicates the common notation.
  This notation indicates that an operation, I/O signal, or control register that is common to all channels is being explained and that duplicate explanations have been omitted.
- Where channel numbers are stated with a figure in parentheses, it indicates the common notation for some channels. Where there is a need to distinguish between even-numbered channels and odd-numbered channels among the channels that are mounted, (0) and (1) are stated respectively. In this case, (0) indicates that a function that is common to the even-numbered channels is being explained, while (1) indicates that a function that is common to the odd-numbered channels is being explained.

ICU-ch.3 of MFT unit 0 can select the calibration input of the internal CR oscillator.

Example 1 is an example of the individual notation, which indicates that the calibration input of the internal CR oscillator can be selected by only ICU-ch.3 of MFT unit 0. This notation indicates that the calibration input of the internal CR oscillator cannot be selected by ICU-ch.0 to ch.2 of MFT unit 0 or ICU ch.0 to ch.3 of other MFT units.

The ICFS10 register is the register that selects the FRT to be connected to ICU-ch.1 and ICU-ch.0.

The ICFS32 register is the register that selects the FRT to be connected to ICU-ch.3 and ICU-ch.2.

Examples 2 and 3 are examples of individual notation that states a control register (ICFS) with two channel numbers (10 and 32).

The ICFS register is the register that selects the FRT to be connected to ICU.

Example 4 is an example of common notation that omits the channel numbers of the control register (ICFS). The meaning that the description is explaining is that, similar to Examples 2 and 3, repeated explanations have been omitted by the common notation.

ICFS10.FSI0[3:0] is the register that selects the FRT to be connected to ICU-ch.0.

ICFS10.FSI1[3:0] is the register that selects the FRT to be connected to ICU-ch.1.

ICFS32.FSI0[3:0] is the register that selects the FRT to be connected to ICU-ch.2.

ICFS32.FSI1[3:0] is the register that selects the FRT to be connected to ICU-ch.3.

Examples 5 to 8 are examples of individual notation that clearly identifies the correspondence between the control bit and the channel in the control registers by stating two channel numbers in the control register (ICFS).

ICFS.FSI0[3:0] is the register that selects the FRT to be connected to ICU-ch.(0).

ICFS.FSI1[3:0] is the register that selects the FRT to be connected to ICU-ch.(1).

Examples 9 and 10 are examples of common notation with parentheses that omits the channel numbers of the control registers. The meaning that the description is explaining is that, similar to Examples 5 to 8, repeated explanations have been omitted by the common notation. It should be required that where common notation is used in the explanation of each function block, as shown above, it must be converted to individual notation for the relevant channel when it is read. Table 3-1 to Table 3-3 show the correspondence tables for individual notation and common notation. For the correspondence between the individual notation and common notation regarding register names, see the list of registers.

Table 3-1 Individual Notation and Common Notation of OCU/ADCMP

Channel Number		5	4	3	2	1	0
OCU/ ADCMP channel number	Individual notation	ch.5	ch.4	ch.3	ch.2	ch.1	ch.0
	Common notation	ch.(1)	ch.(0)	ch.(1)	ch.(0)	ch.(1)	ch.(0)
OCCP register name	Individual notation	OCCP5	OCCP4	OCCP3	OCCP2	OCCP1	OCCP0
	Common notation	OCCP(1)	OCCP(0)	OCCP(1)	OCCP(0)	OCCP(1)	OCCP(0)
OCU output signal name	Individual notation	RT5	RT4	RT3	RT2	RT1	RT0
	Common notation	RT(1)	RT(0)	RT(1)	RT(0)	RT(1)	RT(0)
ACMP register name	Individual notation	ACMP5	ACMP4	ACMP3	ACMP2	ACMP1	ACMP0
	Common notation	ACMP(1)	ACMP(0)	ACMP(1)	ACMP(0)	ACMP(1)	ACMP(0)

Table 3-2 Individual Notation and Common Notation of WFG

Channel Number		54		32		10	
WFG channel number	Individual notation	ch.54		ch.32		ch.10	
	Common notation	No notation					
WFG input signal name	Individual notation	RT5	RT4	RT3	RT2	RT1	RT0
	Common notation	RT(1)	RT(0)	RT(1)	RT(0)	RT(1)	RT(0)
WFG output signal name	Individual notation	RTO5	RTO4	RTO3	RTO2	RTO1	RTO0
	Common notation	RTO(1)	RTO(0)	RTO(1)	RTO(0)	RTO(1)	RTO(0)
PPG input signal name	Individual notation	CH10_PPG		CH32_PPG		CH54_PPG	
	Common notation	CH_PPG					
GATE output signal name	Signal name	CH10_GATE		CH32_GATE		CH54_GATE	
	Common notation	CH_GATE					

Table 3-3 Individual Notation and Common Notation of ICU

Channel Number		3	2	1	0
ICU channel number	Individual notation	ch.3	ch.2	ch.1	ch.0
	Common notation	ch.(1)	ch.(0)	ch.(1)	ch.(0)
ICU input signal name	Individual notation	IC3	IC2	IC1	IC0
	Common notation	IC(1)	IC(0)	IC(1)	IC(0)
ICCP register name	Individual notation	ICCP3	ICCP2	ICCP1	ICCP0
	Common notation	ICCP(1)	ICCP(0)	ICCP(1)	ICCP(0)

3.2 List of Multifunction Timer Registers

This section provides a list of the registers that exist in the multifunction timer unit.

Table 3-4 shows a list of the registers that exist in the multifunction timer unit.

The control registers of the multifunction timer unit are in the same configuration across all of the mounted channels. In this section, the operation of registers with the same function is explained using common notation. The List of Registers states names in individual notation and common notation for each register. Replace the name in common notation that appears in descriptions with the name in individual notation when reading the descriptions.

Registers shown in the List of Registers refer to the registers that exist in the Multifunction Timer 1 unit.
Models that contain more than one multifunction timer unit have the same number of sets of registers for the number of multifunction timer units. Only one TCAL (FRT simultaneous start control register) is present in the Unit0 independent of number of units.

Table 3-4 List of Multifunction Timer Unit Registers

Block Name	Register Name (Individual Notation)	Register Function	Register Name (Common Notation)	Reference
FRT	TCSA0	FRT ch.0 control register A	TCSA	3.3.1
	TCSA1	FRT ch.1 control register A		
	TCSA2	FRT ch.2 control register A		
	TCSC0	FRT ch.0 control register C	TCSC	3.3.2
	TCSC1	FRT ch.1 control register C		
	TCSC2	FRT ch.2 control register C		
	TCSD	FRT ch.1, ch.2 control register D	TCSD	3.3.3
	TCCP0	FRT ch.0 cycle setting register	TCCP	3.3.4
	TCCP1	FRT ch.1 cycle setting register		
	TCCP2	FRT ch.2 cycle setting register		
	TCDT0	FRT ch.0 count value register	TCDT	3.3.5
	TCDT1	FRT ch.1 count value register		
	TCDT2	FRT ch.2 count value register		
	TCAL	FRT simultaneous start control register	TCAL	3.3.6
OCU	OCFS10	OCU ch.1, ch.0 connecting FRT select register	OCFS	3.3.7
	OCFS32	OCU ch.3, ch.2 connecting FRT select register		
	OCFS54	OCU ch.5, ch.4 connecting FRT select register		
	OCSA10	OCU ch.1, ch.0 control register A	OCSA	3.3.8
	OCSA32	OCU ch.3, ch.2 control register A		
	OCSA54	OCU ch.5, ch.4 control register A		
	OCSB10	OCU ch.1, ch.0 control register B	OCSB	3.3.9
	OCSB32	OCU ch.3, ch.2 control register B		
	OCSB54	OCU ch.5, ch.4 control register B		
	OCSC	OCU ch.5～ch.0 control register C	OCSC	3.3.10
	OCSD10	OCU ch.1, ch.0 control register D	OCSD	3.3.11 3.3.12
	OCSD32	OCU ch.3, ch.2 control register D		
	OCSD54	OCU ch.5, ch.4 control register D		

Block Name	Register Name (Individual Notation)	Register Function	Register Name (Common Notation)		Reference
OCU	OCSE0	OCU ch.0 control register E	OCSE	OCSE(0)	3.3.13
	OCSE1	OCU ch.1 control register E		OCSE(1)	
	OCSE2	OCU ch.2 control register E		OCSE(0)	
	OCSE3	OCU ch.3 control register E		OCSE(1)	
	OCSE4	OCU ch.4 control register E		OCSE(0)	
	OCSE5	OCU ch.5 control register E		OCSE(1)	
	OCCP0	OCU ch.0 compare value store register	OCCP	OCCP(0)	3.3.14
	OCCP1	OCU ch.1 compare value store register		OCCP(1)	
	OCCP2	OCU ch.2 compare value store register		OCCP(0)	
	OCCP3	OCU ch.3 compare value store register		OCCP(1)	
	OCCP4	OCU ch.4 compare value store register		OCCP(0)	
	OCCP5	OCU ch.5 compare value store register		OCCP(1)	
WFG	WFSA10	WFG ch.10 control register A	WFSA		3.3.15
	WFSA32	WFG ch.32 control register A			
	WFSA54	WFG ch.54 control register A			
	WFTA10	WFG ch.10 timer value register A	WFTA		3.3.16
	WFTA32	WFG ch.32 timer value register A			
	WFTA54	WFG ch.54 timer value register A			
	WFTB10	WFG ch.10 timer value register B	WFTB		3.3.16
	WFTB32	WFG ch.32 timer value register B			
	WFTB54	WFG ch.54 timer value register B			
	WFTF10	WFG ch.10 timer value register F	WFTF		3.3.17
	WFTF32	WFG ch.32 timer value register F			
	WFTF54	WFG ch.54 timer value register F			
NZCL	NZCL	NZCL control register	NZCL		3.3.18
	WFIR	WFG Interrupt control register	WFIR		3.3.19
ICU	ICFS10	ICU ch.1, ch.0 connecting FRT select register	ICFS		3.3.20
	ICFS32	ICU ch.3, ch.2 connecting FRT select register			
	ICSA10	ICU ch.1, ch.0 control register A	ICSA		3.3.21
	ICSA32	ICU ch.3, ch.2 control register A			
	ICSB10	ICU ch.1, ch.0 control register B	ICSB		3.3.22
	ICSB32	ICU ch.3, ch.2 control register B			
	ICCP0	ICU ch.0 capture value store register	ICCP	ICCP(0)	3.3.23
	ICCP1	ICU ch.1 capture value store register		ICCP(1)	
	ICCP2	ICU ch.2 capture value store register		ICCP(0)	
	ICCP3	ICU ch.3 capture value store register		ICCP(1)	

Block Name	Register Name (Individual Notation)	Register Function	Register Name (Common Notation)		Reference
ADCMP	ACFS10	ADCMP ch.1, ch.0 connecting FRT select register	ACFS		3.3.24
	ACFS32	ADCMP ch.3, ch.2 connecting FRT select register			
	ACFS54	ADCMP ch.5, ch.4 connecting FRT select register			
	ACSA	ADCMP ch.5～ch.0 control register A	ACSA		3.3.25
	ACSC0	ADCMP ch.0 control register C	ACSC		3.3.26
	ACSC1	ADCMP ch.1 control register C			
	ACSC2	ADCMP ch.2 control register C			
	ACSC3	ADCMP ch.3 control register C			
ADCMP	ACSC4	ADCMP ch.4 control register C	ACSC		3.3.26
	ACSC5	ADCMP ch.5 control register C			
	ACSD0	ADCMP ch.0 control register D	ACSD		3.3.27
	ACSD1	ADCMP ch.1 control register D			
	ACSD2	ADCMP ch.2 control register D			
	ACSD3	ADCMP ch.3 control register D			
	ACSD4	ADCMP ch.4 control register D			
	ACSC5	ADCMP ch.5 control register D			
	ACMP0	ADCMP ch.0 compare value store register	ACMP	ACMP(0)	3.3.28
	ACMP1	ADCMP ch.1 compare value store register		ACMP(1)	
	ACMP2	ADCMP ch.2 compare value store register		ACMP(0)	
	ACMP3	ADCMP ch.3 compare value store register		ACMP(1)	
	ACMP4	ADCMP ch.4 compare value store register		ACMP(0)	
	ACMP5	ADCMP ch.5 compare value store register		ACMP(1)	
	ACMC0	ADCMP ch.0 mask compare value store register	ACMC		3.3.29
	ACMC1	ADCMP ch.1 mask compare value store register			
	ACMC2	ADCMP ch.2 mask compare value store register			
	ACMC3	ADCMP ch.3 mask compare value store register			
	ACMC4	ADCMP ch.4 mask compare value store register			
	ACMC5	ADCMP ch.5 mask compare value store register			

3.3 Details of Register Functions

This section explains details of the registers in the multifunction timer unit.

3.3.1. FRT Control Register A (TCSA)
3.3.2. FRT Control Register C (TCSC)
3.3.3. FRT Control Register D (TCSD) (Products after TYPE3-M4)
3.3.4. FRT Cycle Setting Register (TCCP)
3.3.5. FRT Count Value Register (TCDT)
3.3.6. FRT Simultaneous Start Control Register (TCAL)
3.3.7. OCU Connecting FRT Select Register (OCFS)
3.3.8. OCU Control Register A (OCSA)
3.3.9. OCU Control Register B (OCSB)
3.3.10. OCU Control Register C (OCSC)
3.3.11. OCU Control Register D (OCSD) (TYPE1-M4, TYPE2-M4 products)
3.3.12. OCU Control Register D (OCSD) (Products after TYPE3-M4)
3.3.13. OCU Control Register E (OCSE)
3.3.14. OCU Compare Value Store Register (OCCP)
3.3.15. WFG Control Register A (WFSA)
3.3.16. WFG Timer Value Register (WFTA/WFTB)
3.3.17. Pulse Counter Value Register (WFTF)
3.3.18. NZCL Control Register (NZCL)
3.3.19. WFG Interrupt Control Register (WFIR)
3.3.20. ICU Connecting FRT Select Register (ICFS)
3.3.21. ICU Control Register A (ICSA)
3.3.22. ICU Control Register B (ICSB)
3.3.23. ICU Capture Value Store Register (ICCP)
3.3.24. ADCMP Connecting FRT Select Register (ACFS)
3.3.25. ADCMP Control Register A (ACSA)
3.3.26. ADCMP Control Register C (ACSC)
3.3.27. ADCMP Control Register D (ACSD)
3.3.28. ADCMP Compare Value Store Register (ACMP)
3.3.29. ADCMP Mask Compare Value Storage Register (ACMC)

3.3.1 FRT Control Register A (TCSA)

TCSA is a 16-bit register that controls FRT.
Each mounted channel has three registers: TCSA0, TCSA1 and TCSA2.
TCSA0 controls FRT-ch.0.
TCSA1 controls FRT-ch.1.
TCSA2 controls FRT-ch.2.

When the setting TCSD.OFMD1=1 is used to specify the count mode with offset for FRT-ch.1, the TCSA1 register is not used. The TCSA0 register performs simultaneous control of ch.0 and ch.1.

When the setting TCSD.OFMD2=1 is used to specify the count mode with offset for FRT-ch.2, the TCSA2 register is not used. The TCSA0 register performs simultaneous control of ch.0 and ch.2.

Configuration of Register

bit	15	14	13	12	11	10	9	8
Field	ECKE	IRQZF	IRQZE	Reserved			ICLR	ICRE
Attribute	R/W	R/W	R/W	-			R/W	R/W
Initial value	0	0	0	000			0	0

bit	7	6	5	4	3	2	1	0
Field	BFE	STOP	MODE	SCLR	CLK[3:0]			
Attribute	R/W	R/W	R/W	W	R/W			
Initial value	0	1	0	0	0000			

Functions of Register

[bit3:0] CLK[3:0]

The CLK[3:0] bits are bits that set the count clock cycle of FRT counter (16-bit Up/Down counter). Change the setting of this register while the FRT is stopped.

Process	Value	Function
Write	0000	Sets FRT's count clock cycle to the same value as PCLK.
	0001	Sets FRT's count clock cycle to PCLK multiplied by 2.
	0010	Sets FRT's count clock cycle to PCLK multiplied by 4.
	0011	Sets FRT's count clock cycle to PCLK multiplied by 8.
	0100	Sets FRT's count clock cycle to PCLK multiplied by 16.
	0101	Sets FRT's count clock cycle to PCLK multiplied by 32.
	0110	Sets FRT's count clock cycle to PCLK multiplied by 64.
	0111	Sets FRT's count clock cycle to PCLK multiplied by 128.
	1000	Sets FRT's count clock cycle to PCLK multiplied by 256.
	1001	Sets FRT's count clock cycle to PCLK multiplied by 512.
	1010	Sets FRT's count clock cycle to PCLK multiplied by 1024.
	Other than above	Setting is prohibited.
Read	-	Reads the register setting.

As for FRT count clocks, either the PCLK in LSI, which is divided by the prescaler, or an external clock input can be selected for use. Because this register setting is the setting for the prescaler, its value has no

meaning if an external clock input is selected. The FRT's count clock cycle is determined based on the PCLK cycle and the clock division ratio set by this register. The following table shows examples of CLK[3:0] settings and FRT count clock cycles.

CLK [3:0]	Cycle Ratio	FRT Count Clock Cycle		
		PCLK=25 ns (40 MHz)	PCLK=12.5 ns (80 MHz)	PCLK=6.25 ns (160 MHz)
0000	1	25 ns	12.5 ns	6.25 ns
0001	2	50 ns	25 ns	12.5 ns
0010	4	100 ns	50 ns	25 ns
0011	8	200 ns	100 ns	50 ns
0100	16	400 ns	200 ns	100 ns
0101	32	800 ns	400 ns	200 ns
0110	64	1.6 µs	800 ns	400 ns
0111	128	3.2 µs	1.6 µs	800 ns
1000	256	6.4 µs	3.2 µs	1.6 µs
1001	512	12.8 µs	6.4 µs	3.2 µs
1010	1024	25.6 µs	12.8 µs	6.4 µs

[bit4] SCLR

The SCLR bit is the bit that requests FRT operation state initialization. For information about how to use this register, see [bit6] STOP.

Process	Value	Function
Write	0	Does nothing.
	1	Issues FRT operation state initialization request.
Read	-	0 is always read.

[bit5] MODE

The MODE is the register that selects the FRT's count mode. Select the FRT count mode by combining it with the TCSD.OFMD1 or 2 register. See Table 4-2, Table 4-3 and Table 4-4. Change the setting of this register while the FRT is stopped.

Process	Value	Function
Write	0	Sets Normal Up-count mode or Offset Up-count mode.
	1	Sets Normal count mode or Offset Up/Down-count mode.
Read	-	Read the register setting.

[bit6] STOP

The STOP bit is the bit that controls the starting and stopping of the FRT's operation.

Process	Value	Function
Write	0	Puts FRT in operating state.
	1	Puts FRT in stopped state.
Read	-	Reads the register setting

The STOP bit is used in the combination with SCLR, as shown below.

While the FRT's count operation is stopped (current value of STOP is 1):

- When 0 is written to both STOP and SCLR, FRT starts counting from the current TCDT value.
- When 0 is written to STOP and 1 to SCLR, TCDT value is cleared to start counting from TCDT=0x0000. An initial value is loaded into the interrupt Mask Counter.
- When 1 is written to STOP and 0 to SCLR, the current stop state of FRT continues and does nothing.
- When 1 is written to STOP and 1 to SCLR, TCDT is cleared with FRT stopped. An initial value is loaded into the interrupt Mask Counter. The timing that FRT starts counting from "0x0000" (from 0x0000 to 0x0001) is when the FRT is set to the running state.

While the FRT's count operation is running (current value of STOP is 0):

- When 0 is written to both STOP and SCLR, the current running state of the FRT continues and does nothing.
- When 0 is written to STOP and 1 to SCLR, TCDT value is cleared to start counting from TCDT=0x0000. An initial value is loaded into the interrupt Mask Counter.
- When 1 is written to STOP and 0 to SCLR, it stops counting with the FRT counting state left as is.
- When 1 is written to STOP and 1 to SCLR, the FRT is stopped and TCDT is cleared. The timing at which the FRT starts counting from 0x0000 (from 0x0000 to 0x0001) is when the FRT is set to the running state.

When you rewrite other bits in the TCSA register while the FRT is counting (STOP=0), write 0 to both STOP and SCLR. When you rewrite other bits in the TCSA register while the FRT is stopped (STOP=1), write 1 to STOP and 0 to SCLR.

Figure 3-1 and Figure 3-2 show the write values for STOP and SCLR and an example of FRT counting.

Figure 3-1 FRT Count Start, Clear and Stop (Normal Up-count Mode)

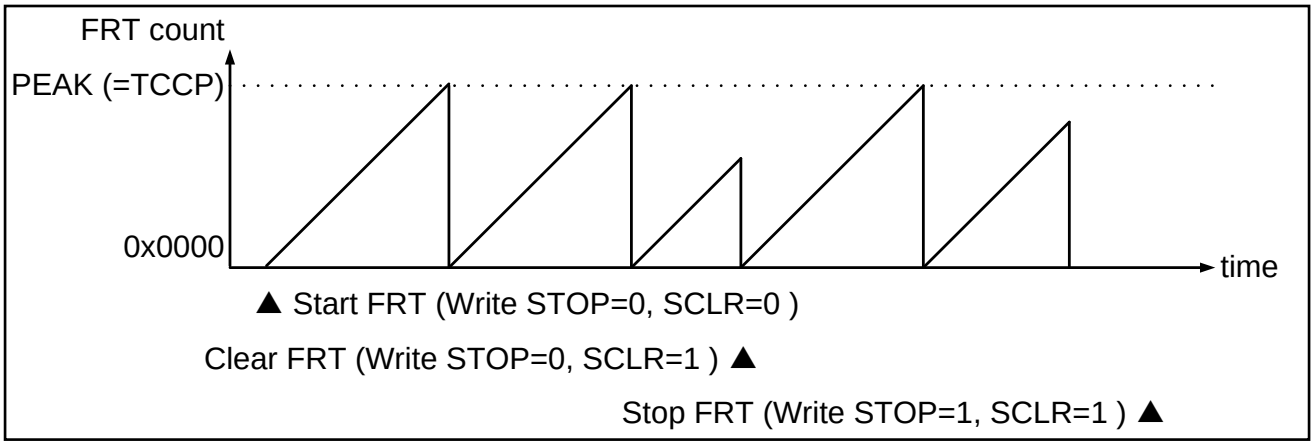
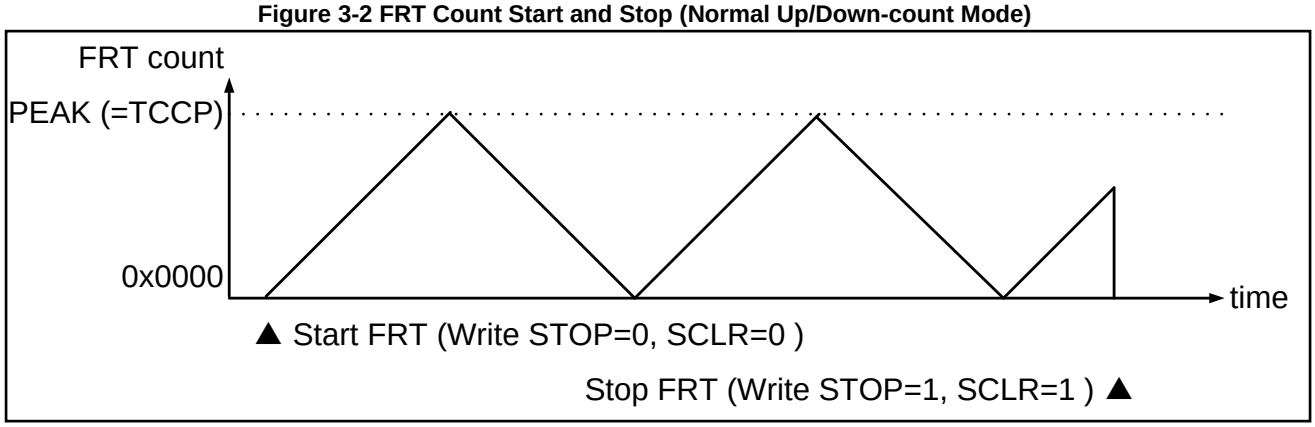


Figure 3-2 FRT Count Start and Stop (Normal Up/Down-count Mode)



[bit7] BFE

The BFE bit is the bit that specifies whether to enable or disable the buffer function of the TCCP register. See 3.3.4 FRT Cycle Setting Register (TCCP).

Process	Value	Function
Write	0	Disables TCCP's buffer function.
	1	Enables TCCP's buffer function.
Read	-	Reads the register setting.

[bit8] ICRE

The ICRE is the bit that specifies whether to notify the CPU in the event that ICLR is set as an interrupt (enabling interrupt) or not to notify it (disabling interrupt). See 4.10 Treatment of Event Detect Register and Interrupt.

Process	Value	Function
Write	0	Does not generate interrupt when 1 is set to ICLR.
	1	Generates interrupt when 1 is set to ICLR.
Read	-	Reads the register setting.

[bit9] ICLR

The ICLR is the bit that is set to 1 when the FRT counter value (TCDT) changes from the TCCP value to 0x0000 (or TCCP-1).

Process	Value	Function
Write	0	Clears this register to 0.
	1	Does nothing.
Read	0	Indicates that no match has been detected between the FRT's count value and the TCCP value.
	1	Indicates that a match has been detected between the FRT's count value and the TCCP value.
Read during RMW access		1 is always read.

Reading this register determines whether or not the FRT count value has reached the TCCP value. This register can be cleared by writing 0 to this register. When you rewrite other registers in the TCSA register, be sure to write 1 to this register. See 4.10 Treatment of Event Detect Register and Interrupt.

If an FRT is initialized by bus reset or writing 1 to SCLR, this register will not be set with the first FRT count operation.

When FRT is initialized by bus reset or writing SCLR=1, this bit is not set at the first FRT count operation.

When the interrupt mask function of TCSC register is used, the set of ICLR register is masked according to the value of the mask counter.

[bit12:10] Reserved: Reserved bits

0 must be written at write access. Read value is 0.

[bit13] IRQZE

The IRQZE is the bit that specifies whether to notify the CPU in the event that IRQZF is set as an interrupt (enabling interrupt) or not to notify it (disabling interrupt). See 4.10 Treatment of Event Detect Register and Interrupt.

Process	Value	Function
Write	0	Does not generate interrupt when 1 is set to IRQZF.
	1	Generates interrupt, when 1 is set to IRQZF.
Read	-	Reads the register setting.

[bit14] IRQZF

IRQZF is the bit that is set to 1 when the FRT counter value (TCDT) changes from 0x0000 to 0x0001.

Process	Value	Function
Write	0	Clears this register to 0.
	1	Does nothing.
Read	0	Indicates that a match between FRT's count value and "0x0000" has not been detected.
	1	Indicates that a match between FRT's count value and "0x0000" has already been detected.
Read during RMW access		1 is always read.

Reading this register determines whether or not the FRT count value has reached 0x0000. This register can be cleared by writing 0 to this register. When you rewrite other registers in the TCSA register, be sure to write 1 to this re4gister. See 4.10 Treatment of Event Detect Register and Interrupt.

If the FRT is initialized by a bus reset or writing 1 to SCLR, this register will not be set with the first FRT count operation.

When the interrupt mask function of TCSC register is used, the set of IRQZF register is masked according to the value of the mask counter.

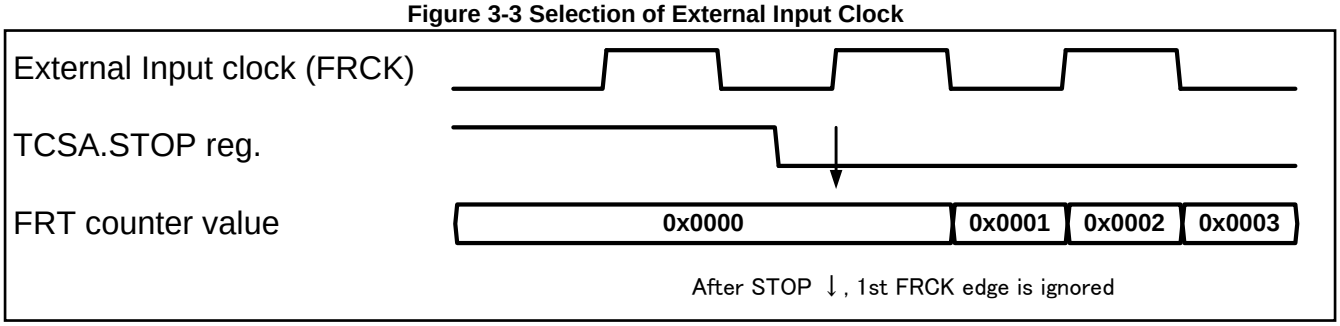
[bit15] ECKE

ECKE is the bit that selects the clock signal to be used as the FRT's count clock. Change the setting of this register while the FRT is stopped.

Process	Value	Function
Write	0	Uses the internal clock (PCLK) as FRT's count clock.
	1	Uses an external input clock (FRCK) as FRT's count clock.
Read	-	Reads the setting value.

To select an external input clock, the FRCK pin to be used in the I/O port block must be predetermined. Count operations are performed both at the rising edge and falling edge of an external input clock signal. To operate it with an external input clock, the first edge from the external input clock after FRT operation starts (writing 0 to STOP) is ignored, irrespective of the rising or falling edge, and the count operation starts from the next edge.

Figure 3-3 Selection of External Input Clock



3.3.2 FRT Control Register C (TCSC)

TCSC is a 16-bit register that controls an FRT.
Each mounted channel has three registers: TCSC0, TCSC1 and TCSC2.
TCSC0 controls FRT ch.0.
TCSC1 controls FRT ch.1.
TCSC2 controls FRT ch.2.

When the setting TCSD.OFMD1=1 is used to specify the count mode with offset for FRT-ch.1, the TCSC1 register is not used. The TCSC0 register is used to generate an interrupt from ch.0.

When the setting TCSD.OFMD2=1 is used to specify the count mode with offset for FRT-ch.2, the TCSC2 register is not used. The TCSC0 register is used to generate an interrupt from ch.0.

Configuration of Register

bit	31	30	29	28	27	26	25	24
Field	MSPC[3:0]				MSZC[3:0]			
Attribute	R				R			
Initial value	0000				0000			

bit	23	22	21	20	19	18	17	16
Field	MSPI[3:0]				MSZI[3:0]			
Attribute	R/W				R/W			
Initial value	0000				0000			

Functions of Register

[bit19:16] MSZI

MSZI sets the number of masked zero value detection by specifying the initial value of zero value detection mask counter.

Process	Function
Write	Sets the number of masked zero value detections.
Read	Reads the register setting.

[bit23:20] MSPI

MSPI sets the number of masked peak value detection by specifying the initial value of peak value detection mask counter.

Process	Function
Write	Sets the number of masked peak value detections.
Read	Reads the register setting.

[bit27:24] MSZC

MSZC reads the current counter value from a zero value detection mask counter.

Process	Function
Write	Does nothing.
Read	Reads the current counter value from a zero value detection mask counter.

[bit31:28] MSPC

MSPC reads the current counter value from a peak value detection mask counter.

Process	Function
Write	Does nothing.
Read	Reads the current counter value from a peak value detection mask counter.

See 4.1.4.2 Operation of Interrupt Mask Counters.

3.3.3 FRT Control Register D (TCSD) (Products after TYPE3-M4)

TCSD is an 8-bit register that performs FRT control.
This register controls FRT ch.1 and ch.2.

Notes:

- *The TCSD register is included in TYPE3-M4 products and later only.*
- *The TCSD register is not included in TYPE1-M4 or TYPE2-M4 products.*
- *Count mode operation with FRT offset is possible for TYPE3-M4 products and later only.*

Configuration of Register

bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	OFMD2	OFMD1
Attribute	-	-	-	-	-	-	R/W	R/W
Initial value	-	-	-	-	-	-	0	0

Functions of Register

[bit0] OFMD1

This bit is the register that selects the count mode with offset for FRT ch.1. See Table 4-3. Change the setting for this bit after FRT ch.0 and FRT ch.1 have stopped.

Process	Value	Function
Write	0	Sets FRT ch.1 count operation to normal count mode.
	1	Sets FRT ch.1 count operation to count mode with offset.
Read	-	Reads the register setting.

[bit1] OFMD2

This bit is the register that selects the count mode with offset for FRT ch.2. See Table 4-3. Change the setting for this bit after FRT ch.0 and FRT ch.2 have stopped.

Process	Value	Function
Write	0	Sets FRT ch.2 count operation to normal count mode.
	1	Sets FRT ch.2 count operation to count mode with offset.
Read	-	Reads the register setting.

[bit7:2] Reserved

Write value is invalid. Read value is 0.

For details of the operation of the FRT offset count mode. See 4.1 Descriptions of FRT Operation

3.3.4 FRT Cycle Setting Register (TCCP)

TCCP is a 16-bit register that sets the peak value (count cycles) or the offset value for FRT.
Each mounted channel has three registers: TCCP0, TCCP1 and TCCP2.
TCCP0 sets the peak value for FRT ch.0.
TCCP1 sets the peak value or the offset value for FRT ch.1.
TCCP2 sets the peak value or the offset value for FRT ch.2.
It should be noted that this register does not allow for byte access.

Configuration of Register

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Field	TCCP[15:0]															
Attribute	R/W															
Initial value	0xFFFF															

Functions of Register

TCCP is a 16-bit register that sets the peak value (count cycles) or the offset value for FRT. During FRT count operations, writing can be performed to the TCCP register to change the peak value or offset value. The FRT peak value set for the TCCP register is used to determine the FRT count cycle as shown below.

- In Up-count mode : FRT's count cycle = (TCCP+1) × FRT's count clock cycle
- In Up/Down-count mode : FRT's count cycle = TCCP × 2 × FRT's count clock cycle

The TCCP register has a buffer function. When the FRT peak value is set to the TCCP register, the TCSA.BUFE register setting can be used to select enable or disable for the buffer register function.

When the buffer register function is enabled (TCSA.BUFE=1), the peak value written to the TCCP register from the CPU is first stored in the TCCP buffer register. Then, zero detection of the FRT is used to transfer the value from the TCCP buffer register to the TCCP register.

When the buffer register function is disabled (TCSA.BUFE=0), the peak value written to the TCCP register from the CPU is immediately transferred to the TCCP register.

When count mode with offset is selected in the FRT, and an FRT offset value is set in the TCCP register, the buffer register function is always disabled. In this case, the offset value written to the TCCP register from the CPU is immediately transferred to the TCCP register. However, even if the offset value changes, the offset value of the FRT counter value is not immediately changed, and the updated value is applied starting from the next cycle.

If data is read from this address area, the value in the TCCP register is read, rather than the value in the buffer register. While the buffer function is enabled, the previous value is read until the transfer is finished.

Notes:

- *Bit rewriting with RMW access to this area is not allowed.*
- *It is prohibited to write 0x0000 to this register as the peak value.*

[bit31:16] TCCP[15:0]

bit	Function
Write	Sets the FRT peak value or the FRT offset value. Written values are stored in the TCCP buffer register. It is prohibited to write "0x0000" to this register as the peak value.
Read	Reads values in the TCCP register (not values in the TCCP buffer register).

3.3.5 FRT Count Value Register (TCDT)

TCDT is a 16-bit register that reads and writes FRT count values.
Each mounted channel has three registers: TCDT0, TCDT1 and TCDT2.
TCDT0 is the timer count value of FRT-ch.0.
TCDT1 is the timer count value of FRT-ch.1.
TCDT2 is the timer count value of FRT-ch.2.
It should be noted that this register does not allow for byte access.

Configuration of Register

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Field	TCDT[15:0]															
Attribute	R/W															
Initial value	0x0000															

Functions of Register

The TCDT register is a 16-bit register that reads and writes FRT count values. The value read from the TCDT register becomes the FRT's count value at that point. Do not write any data during the FRT's operation. When data is written while the FRT is stopped in normal count mode, the FRT starts counting from that value.

Data cannot be written in count mode with offset even if the FRT is stopped.

[bit15:0] TCDT[15:0]

Process	Function
Write	Rewrites the FRT count value.(Only while the FRT is stopped in normal count mode)
Read	Reads the current FRT count value.

3.3.6 FRT Simultaneous Start Control Register (TCAL)

TCAL is a 32-bit register that controls simultaneous starting, simultaneous stopping and simultaneous clearing for multiple FRTs in the MFT. There is only one of these registers, regardless of the number of built-in MFT units. Only word access (32 bits) is available.

Configuration of Register

bit	31	30	29	28	27	26	25	24
Field	Reserved							SCLR22
Attribute	R	R	R	R	R	R	R	W
Initial value	0	0	0	0	0	0	0	0

bit	23	22	21	20	19	18	17	16
Field	SCLR21	SCLR20	SCLR12	SCLR11	SCLR10	SCLR02	SCLR01	SCLR00
Attribute	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

bit	15	14	13	12	11	10	9	8
Field	Reserved							STOP22
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

bit	7	6	5	4	3	2	1	0
Field	STOP21	STOP20	STOP12	STOP11	STOP10	STOP02	STOP01	STOP00
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

Functions of Register

Writing to this register allows the batch control of simultaneous starting, stopping and clearing of multiple FRTs in multiple MFT units with a single CPU access.

Before performing a simultaneous start, initialize the operating mode with the TCSA, TCCP and TCDT registers in each FRT.

[bit8:0] STOPxy (x indicates MFT unit number, y for FRT channel number)

These bits are a mirror register of the STOP register located in each TCSA register. Writing to this area results in writing the same value to the STOP register in each TCSA register. Separate writes to the STOP register in each TCSA register update the read value of this register to the same value.

Process	Function
Write	Processes simultaneous writes to relevant TCSA.STOP bit.
Read	Processes simultaneous reads from relevant TCSA.STOP bit.

If any FRT that does not control simultaneous starts is present, the TCAL register must be read, and the same value as the read value must be written to the STOP register.

Any write or read to/from a non-existent MFT unit will become an invalid process.

If there is an FRT-ch.1 or ch.2 where count mode with offset has been selected, write 1 to the corresponding STOP register. The value written to the STOP register of FRT-ch.0, which is operating simultaneously, is used to control ch.0 synchronously.

[bit24:16] SCLRxy (x indicates MFT unit number, y for FRT channel number)

These bits are a mirror register of the SCLR register located in each TCSA register. Writing to this area results in writing the same value to the SCLR register in each TCSA register. Writing 1 clears the corresponding FRT at the same time.

Process	Function
Write	Processes simultaneous writes to relevant TCSA.SCLR register.
Read	0 is always read.

0 must be written to FRTs that do not control simultaneous starts. Any write or read to/from a non-existent MFT unit will become an invalid process.

If there is an FRT-ch.1 or ch.2 where count mode with offset has been selected, write 0 to the corresponding SCLR register. The value written to the SCLR register of FRT-ch.0, which is operating simultaneously, is used to control ch.0 synchronously.

Note:

- *TCAL register can be accessed by only registers existing in Unit0. Registers in Unit1 and Unit2 are prohibited to access TCAL register area (base address + 0x0164 address).*

3.3.7 OCU Connecting FRT Select Register (OCFS)

OCFS is an 8-bit register that selects and sets the FRT to be connected to an OCU.
Each mounted channel has three registers: OCFS10, OCFS32 and OCFS54.
OCFS10 controls OCU ch.1 and OCU ch.0.
OCFS32 controls OCU ch.3 and OCU ch.2.
OCFS54 controls OCU ch.5 and OCU ch.4.
Bit positions of OCFS10, OCFS32 and OCFS54 are [7:0], [15:8] and [23:16] respectively.

Configuration of Register

bit	23/15/7	22/14/6	21/13/5	20/12/4	19/11/3	18/10/2	17/9/1	16/8/0
Field	FSO1[3:0]				FSO0[3:0]			
Attribute	R/W				R/W			
Initial value	0000				0000			

Functions of Register

[bit3:0/11:8/19:16] FSO0[3:0]

These bits are the register that selects the FRT to be connected to ch.(0) of an OCU and uses it.
Changing the setting of this register while the operation of OCU to be connected is prohibited.

Process	Value	Function
Write	0000	Connects FRT ch.0 to OCU ch.(0).
	0001	Connects FRT ch.1 to OCU ch.(0).
	0010	Connects FRT ch.2 to OCU ch.(0).
	0011 to 1000	For models with multiple MFT units: Connects FRT of an external MFT. For models with one MFT unit: Setting is prohibited.
	Other than above	Setting is prohibited.
Read	-	Reads the register setting.

[bit7:4/15:12/23:20] FSO1[3:0]

These bits are the register that selects the FRT to be connected to ch.(1) of an OCU and uses it.
Changing the setting of this register while the operation of OCU to be connected is prohibited.

Process	Value	Function
Write	0000	Connects FRT ch.0 to OCU ch.(1).
	0001	Connects FRT ch.1 to OCU ch.(1).
	0010	Connects FRT ch.2 to OCU ch.(1).
	0011 to 1000	For products with multiple MFT units: Connects FRT of an external MFT. For products with one MFT unit: Setting is prohibited.
	Other than above	Setting is prohibited.
Read	-	Reads the register setting.

For products with multiple MFT units, the connection to an FRT that exists in another MFT unit can be selected. For related settings, see 4.8 FRT Selection of OCU, ICU, and ADCMP.

3.3.8 OCU Control Register A (OCSA)

OCSA is an 8-bit register that controls an OCU's operation.
Each mounted channel has three registers: OCSA10, OCSA32 and OCSA54.
OCSA10 controls OCU ch.1 and OCU ch.0.
OCSA32 controls OCU ch.3 and OCU ch.2.
OCSA54 controls OCU ch.5 and OCU ch.4.

Configuration of Register

bit	7	6	5	4	3	2	1	0
Field	IOP1	IOP0	IOE1	IOE0	Reserved	Reserved	CST1	CST0
Attribute	R/W	R/W	R/W	R/W	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Functions of Register

[bit0] CST0

This bit is the bit that selects the operation state of OCU ch(0).

Process	Value	Function
Write	0	Disables the operation of OCU ch.(0). ・Holds RT(0) output and OCSA.IOP0 state. ・Reflects the value written to OCSB.OTD0 on the RT(0) output.
	1	Enables the operation of OCU ch.(0). ・Reflects register settings to RT(0) output and OCSA.IOP0. ・Ignores the value written to OCSB.OTD0.
Read	-	Reads the register setting.

[bit1] CST1

This bit is the bit that selects the operation state of OCU ch(1).

Process	Value	Function
Write	0	Disables the operation of OCU ch.(1). ・Holds RT(0) output and OCSA.IOP1 state. ・Reflects the value written to OCSB.OTD1 on the RT(1) output.
	1	Enables the operation of OCU ch.(1). ・Reflects register settings to RT(1) output and OCSA.IOP1. ・Ignores the value written to OCSB.OTD1.
Read	-	Reads the register setting.

For the OCU's operating modes, see 4.2 Description of OCU Operation.

Notes:

Always perform control according to the procedures below when starting PWM signal output by OCU.

1. *Initial setting*
   Set FRT operating mode (FRT control register other than TCSA.STOP).
   Set OCU operating mode and initialize the output level (OCU control register other than OCSA.CST0 and OCSA.CST1).
   Set the OCCP compare value (writing the OCCP value).
2. *Start FRT count operation (writing 0 to TCSA:STOP).*
3. *Enable OCU's operation (writing 1 to OCSA:CST0 and OCSA:CST1).*

Always perform control according to the procedure below when finishing PWM signal output by OCU.

1. *Disable OCU's operation (writing 0 to CST0 and CST1).*
2. *Reset the output level of the OCU output pins (writing to OCSB:OTD0 and OCSB:OTD1, if necessary).*
3. *Stop FRT's count operation (writing 1 to TCSA:STOP and TCSA:SCLR).*

[bit3:2] Reserved

Values written to this area are ignored. 00 is read.

[bit4] IOE0

This bit is the bit that specifies whether to notify the CPU in the event that IOP0 is set to 1 as an interrupt (enabling interrupt), or not to notify it (disabling interrupt). See 4.10 Treatment of Event Detect Register and Interrupt.

Process	Value	Function
Write	0	Does not generate interrupt, when IOP0 is set to 1.
	1	Generates interrupt, when IOP0 is set to 1.
Read	-	Reads the register setting.

[bit5] IOE1

This bit is the bit that specifies whether to notify the CPU in the event that IOP1 is set to 1 as an interrupt (enabling interrupt), or not to notify it (disabling interrupt). See 4.10 Treatment of Event Detect Register and Interrupt.

Process	Value	Function
Write	0	Does not generate interrupt, when IOP1 is set to 1.
	1	Generates interrupt, when IOP1 is set to 1.
Read	-	Reads the register setting.

[bit6] IOP0

This bit is the bit that is set to 1 when a match is detected between the count value of the FRT connected to OCU ch.(0) and the value of OCCP(0) when the operation of OCU ch.(0) is enabled (CST0=1).

Process	Value	Function
Write	0	Clears IOP0 to 0.
	1	Does nothing.
Read	0	Indicates that no match has been detected between the FRT's count value and the OCCP(0) value at OCU ch.(0).
	1	Indicates that a match has already been detected between the FRT's count value and the OCCP(0) value at OCU ch.(0).
Read at RMW access		1 is always read.

[bit7] IOP1

This bit is the bit that is set to 1 when a match is detected between the count value of the FRT connected to OCU ch.(1) and the value of OCCP(1) when the operation of OCU ch.(1) is enabled (CST1=1).

Process	Value	Function
Write	0	Clears IOP1 to 0.
	1	Does nothing.
Read	0	Indicates that no match has been detected between the FRT's count value and OCCP(1) value at OCU ch.(1).
	1	Indicates that a match has already been detected between the FRT's count value and OCCP(1) value at OCU ch.(1).
Read at RMW access		1 is always read.

The following explanation is common to IOP0 and IOP1.

Whether FRT's count value has reached the OCCP value or not can be determined by reading from this bit. Conditions for match detection are updated by specifying the OCSB, OCSC and OCSE registers. For operating modes, see 4.2 Description of OCU Operation.

This register can be cleared by writing 0 from the CPU. Always write 1 to the register when rewriting to another register in the same address area. This bit does nothing, if 1 is written. See 4.10 Treatment of Event Detect Register and Interrupt for details.

3.3.9 OCU Control Register B (OCSB)

OCSB is an 8-bit register that controls an OCU's operation.
Each mounted channel has three registers: OCSB10, OCSB32 and OCSB54.
OCSB10 controls OCU ch.1 and OCU ch.0.
OCSB32 controls OCU ch.3 and OCU ch.2.
OCSB54 controls OCU ch.5 and OCU ch.4.

Configuration of Register

bit	15	14	13	12	11	10	9	8
Field	FM4	Reserved	Reserved	CMOD	Reserved	Reserved	OTD1	OTD0
Attribute	R/W	R	R	R/W	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Functions of Register

[bit8] OTD0

This bit is the bit that reads the state of the RT(0) output pin of OCU ch.(0) and sets its output level.

Process	Value	Function
Write	0	Sets the output level of the RT(0) pin to Low, when OCSA:CST0=0. No effect on the operation when OCSA:CST0=1.
	1	Sets the output level of the RT(0) pin to High, when OCSA:CST0=0. No effect on the operation when OCSA:CST0=1.
Read	0	Indicates that the RT(0) output pin is in the Low-level output state.
	1	Indicates that the RT(0) output pin is in the High-level output state.

[bit9] OTD1

This bit is the bit that reads the state of the RT(1) output pin of OCU ch.(1) and sets its output level.

Process	Value	Function
Write	0	Sets the output level of the RT(1) pin to Low, when OCSA.CST1=0. No effect on the operation when OCSA.CST1=1.
	1	Sets the output level of the RT(1) pin to High, when OCSA.CST1=0. No effect on the operation when OCSA.CST1=1.
Read	0	Indicates that the RT(1) output pin is in the Low-level output state.
	1	Indicates that the RT(1) output pin is in the High-level output state.

The following explanation is shared by ODT0 and OTD1.

The output level of the OCU output pins (RT0 to RT5) can be set by writing to these registers when the OCU's operation is disabled. When the OCU's operation is enabled, any writing that is performed to these registers is ignored. The read value of these registers indicates the output level of the OCU output pins, irrespective of OCU's operation state.

Notes:

- *After being processed by the WFG, the OCU's output pins (RT0 to RT5) become the LSI's external output pins (RTO0 to RTO5). For this reason, the level of the OCU's output pins does not match the level of the LSI's external output pins in some of the WFG's operating modes; therefore care must be taken. The state of the LSI's external output pins can be read from the PDIR register of the I/O port block.*
- *Follow the procedure below to set the output level to Low by stopping the OCU's operation when CST0=1 (OCU operation enabled) and OTD0=1 (High-level output).*
  - *No value can be written to OTD0 while the OCU's operation is enabled; therefore, first write "0" to CST0 to stop the OCU's operation.*
  - *Then, write 0 to OTD0 to set the output level to Low.*
- *It should be noted that if the above steps were reversed, the value written to OTD0 would be ignored. It should also be noted that if CST0=0 and OTD0=0 were written to the OCSA and OCSB registers by half-word access, the value written to OTD0 would be ignored because the OCU's operation is enabled. Similarly, care must be taken when writing to OTD1.*

[bit11:10] Reserved

Values written to this area are ignored. 00 is read.

[bit12] CMOD

This bit is the bit that selects the OCU's operating mode in FM3 compatible mode (OCSB.FM4=0). Use this register to specify the operating mode for FM3 compatible mode in combination with OCSC:MOD0 to MOD5. In FM4 mode (OCSB.FM4=1), the register setting of this register is ignored. Change the setting of this register, while the OCU's operation is disabled. For details of the operating modes that depend on this register setting, see 4.3 OCU FM3 Family Product-compatible Operation.

Process	Value	Function
Write	0	Writes "0" to this register.
	1	Writes "1" to this register.
Read	-	Reads the register setting.

When setting OCSB10:CMOD, the common setting applies to ch.1 and ch.0. When setting OCSB32:CMOD, the common setting applies to ch.3 and ch.2. When setting OCSB54:CMOD, the common setting applies to ch.5 and ch.4.

[bit14:13] Reserved: Reserved bits

Values written to this area are ignored. 00 is read.

[bit15] FM4

This bit is the bit that selects the OCU's operating mode.

Process	Value	Function
Write	0	Selects FM3-compatible mode for operating mode.
	1	Selects FM4 mode for operating mode.
Read	-	Reads the register setting.

Change the setting of this register while the OCU's operation is disabled. For details of the operating modes that depend on this register setting, see 4.2 Description of OCU Operation and 4.3 OCU FM3 Family Product-compatible Operation.

When setting OCSB10.FM4, the common setting applies to ch.1 and ch.0. When setting OCSB32.FM4, the common setting applies to ch.3 and ch.2. When setting OCSB54.FM4, the common setting applies to ch.5 and ch.4.

3.3.10 OCU Control Register C (OCSC)

OCSC is an 8-bit register that controls the OCU's operation.
This register controls all of OCU channels ch.0 to ch.5.

Configuration of Register

bit	15	14	13	12	11	10	9	8
Field	Reserved	Reserved	MOD5	MOD4	MOD3	MOD2	MOD1	MOD0
Attribute	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	-	-	0	0	0	0	0	0

Functions of Register

[bit13:8] MOD5 to MOD0

This bit is the register that selects the OCU's operating mode in FM3 compatible mode (OCSB.FM4=0). Use this bit to specify the operating mode for FM3 compatible mode in combination with OCSB:CMOD. In FM4 mode (OCSB.FM4=1), the register setting of this register is ignored. Change the setting of this register, while the OCU's operation is disabled. For details of the operating modes that depend on this register setting, see 4.3 OCU FM3 Family Product-compatible Operation.

Process	Value	Function
Write	0	Writes 0 to this register.
	1	Writes 1 to this register.
Read	-	Reads the register setting.

MOD0 and MOD1 determine the operating mode of OCU ch.0/ch.1 for FM3 mode in combination with OCSB10:CMOD.
MOD2 and MOD3 determine the operating mode of OCU ch.2/ch.3 for FM3 mode in combination with OCSB32:CMOD.
MOD4 and MOD5 determine the operating mode of OCU ch.4/ch.5 for FM3 mode in combination with OCSB54:CMOD.

[bit15:14] Reserved

Write value is invalid. Read value is undefined.

3.3.11 OCU Control Register D (OCSD) (TYPE1-M4, TYPE2-M4 products)

This section describes the OCSD register functions of TYPE1-M4 and TYPE2-M4 products. For details on the OCSD register functions for TYPE3-M4 products and later, see 3.3.12 OCU Control Register D (OCSD) (Products after TYPE3-M4).

OCSD is a 16-bit register that controls the OCU's operation.
Each mounted channel has three registers: OCSD10, OCSD32 and OCSD54.
OCSD10 controls OCU ch.1 and OCU ch.0.
OCSD32 controls OCU ch.3 and OCU ch.2.
OCSD54 controls OCU ch.5 and OCU ch.4.

Configuration of Register

bit	31	30	29	28	27	26	25	24
Field	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Attribute	-	-	-	-	-	-	-	-
Initial value	-	-	-	-	-	-	-	-

bit	23	22	21	20	19	18	17	16
Field	OCSE1BUFE[1:0]		OCSE0BUFE[1:0]		OCCP1BUFE[1:0]		OCCP0BUFE[1:0]	
Attribute	R/W		R/W		R/W		R/W	
Initial value	00		00		00		00	

Functions of Register

[bit17:16] OCCP0BUFE[1:0]

These bits are registers that specify whether to enable or disable the buffer function and the transfer timing of OCCP(0) register.

Process	Value	Function
Write	00	Disables the buffer function of the OCCP(0) register. Buffer transfer is always made when writing to OCCP(0) from the CPU.
	01	Enables the buffer function of the OCCP(0) register. Buffer transfer is made when counter value of FRT connected to ch.(0) is Zero/Bottom status.
	10	Enables the buffer function of the OCCP(0) register. Buffer transfer is made when counter value of FRT connected to ch.(0) is Peak/Top status.
	11	Enables the buffer function of the OCCP(0) register. Buffer transfer is made when counter value of FRT connected to ch.(0) is both Zero/Bottom and Peak/Top status.
Read	-	Reads the register setting.

[bit19:18] OCCP1BUFE[1:0]

These bits are registers that specify whether to enable or disable the buffer function and the transfer timing of OCCP(1) register.

Process	Value	Function
Write	00	Disables the buffer function of the OCCP(1) register. Buffer transfer is always made when writing to OCCP(1) from the CPU.
	01	Enables the buffer function of the OCCP(1) register. Buffer transfer is made when counter value of FRT connected to ch.(1) is Zero/Bottom status.
	10	Enables the buffer function of the OCCP(1) register. Buffer transfer is made when counter value of FRT connected to ch.(1) is Peak/Top status.
	11	Enables the buffer function of the OCCP(1) register. Buffer transfer is made when counter value of FRT connected to ch.(1) is both Zero/Bottom and Peak/Top status.
Read	-	Reads the register setting.

The following explanation is shared by OCCP0BUFE[1:0] and OCCP1BUFE[1:0].

Change the setting of this bit while the OCU's operation is disabled (OCSA.CST0=0, OCSACST1=0). In FM3 compatible mode (OCSB.FM4=0), there are some restrictions on values that can be set depending on the operation mode. See 4.3 OCU FM3 Family Product-compatible Operation for details.

[bit21:20] OCSE0BUFE[1:0]

These bits are registers that specify whether to enable or disable the buffer function and the transfer timing of OCSE(0) register.

Process	Value	Function
Write	00	Disables the buffer function of the OCSE(0) register. Buffer transfer is always made when writing to OCSE(0) from the CPU.
	01	Enables the buffer function of the OCSE(0) register. Buffer transfer is made when counter value of FRT connected to ch.(0) is Zero/Bottom status.
	10	Enables the buffer function of the OCSE(0) register. Buffer transfer is made when counter value of FRT connected to ch.(0) is Peak/Top.
	11	Enables the buffer function of the OCSE(0) register. Buffer transfer is made when counter value of FRT connected to ch.(0) is both Zero/Bottom and Peak/Top status.
Read	-	Reads the register setting.

[bit23:22] OCSE1BUFE[1:0]

These bits are registers that specify whether to enable or disable the buffer function and the transfer timing of OCSE(1) register.

Process	Value	Function
Write	00	Disables the buffer function of the OCSE(1) register. Buffer transfer is always made when writing to OCSE(1) from the CPU.
	01	Enables the buffer function of the OCSE(1) register. Buffer transfer is made when counter value of FRT connected to ch.(1) is Zero/Bottom status.
	10	Enables the buffer function of the OCSE(1) register. Buffer transfer is made when counter value of FRT connected to ch.(1) is Peak/Top status.
	11	Enables the buffer function of the OCSE(1) register. Buffer transfer is made when counter value of FRT connected to ch.(1) is both Zero/Bottom and Peak/Top status.
Read	-	Reads the register setting.

The following explanation is shared by OCSE0BUFE[1:0] and OCSE1BUFE[1:0].

Change the setting of this register while OCU's operation is disabled (OCSA.CST0=0, OCSACST1=0). In FM3 compatible mode (OCSB.FM4=0), values other than "00" cannot be set for these registers.

[bit31:24] Reserved : Reserved bits

This is a reserved register. The written values do not hold any meaning. The readout values are all 1.

3.3.12 OCU Control Register D (OCSD) (Products after TYPE3-M4)

This section describes the OCSD register functions of TYPE3-M4 products and later. For details on the OCSD register functions of TYPE1-M4 and TYPE2-M4 products, see 3.3.11 OCU Control Register D (OCSD) (TYPE1-M4, TYPE2-M4 products).

OCSD is a 16-bit register that controls the OCU's operation.
Each mounted channel has three registers: OCSD10, OCSD32 and OCSD54.
OCSD10 controls OCU ch.1 and OCU ch.0.
OCSD32 controls OCU ch.3 and OCU ch.2.
OCSD54 controls OCU ch.5 and OCU ch.4.

Configuration of Register

bit	31	30	29	28	27	26	25	24
Field	Reserved	Reserved	OFEX1	OFEX0	OEBM1	OEBM0	OPBM1	OPBM0
Attribute	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	-	-	0	0	0	0	0	0

bit	23	22	21	20	19	18	17	16
Field	OCSE1BUFE[1:0]		OCSE0BUFE[1:0]		OCCP1BUFE[1:0]		OCCP0BUFE[1:0]	
Attribute	R/W		R/W		R/W		R/W	
Initial value	00		00		00		00	

Functions of Register

[bit17:16] OCCP0BUFE[1:0] and [bit24] OPBM0

OCCP0BUFE[1:0] are registers that specify whether to enable or disable the buffer function and the transfer timing of OCCP(0) register. OPBM0 sets the link transfer settings with the FRT interrupt mask counter.

Process	Value		Function	
	OPBM0	OCCP0 BUFE	Buffer	Transfer Timing
Write	0	00	Disable	Always when writing to OCCP(0) from CPU.
	0	01	Enable	When FRT connected to ch.(0) is Zero/Bottom status.
	0	10		When FRT connected to ch.(0) is Peak/Top status.
	0	11		When FRT connected to ch.(0) is Zero/Bottom status, or Peak/Top status.
	1	00	Disable	Always when writing to OCCP(0) from CPU.
	1	01	Enable	When FRT connected to ch.(0) is Zero/Bottom status and MSZC=0000.
	1	10		When FRT connected to ch.(0) is Peak/Top status and MSPC=0000.
	1	11		Condition A: FRT connected to ch.(0) is Zero/Bottom status. Condition B: FRT connected to ch.(0) is MSZC=0000. Condition C: FRT connected to ch.(0) is Peak/Top status. Condition D: FRT connected to ch.(0) is MSPC=0000. When (Condition A and Condition B) or (Condition C and Condition D).
Read	-	-	Reads the register setting.	

[bit19:18] OCCP1BUFE[1:0] and [bit25] OPBM1

OCCP1BUFE[1:0] are registers that specify whether to enable or disable the buffer function and the transfer timing of OCCP(1) register. OPBM1 sets the linked transfer settings with the FRT interrupt mask counter.

Process	Value		Function	
	OPBM1	OCCP1 BUFE	Buffer Function	Transfer Timing
Write	0	00	Disable	Always when writing to OCCP(1) from CPU.
	0	01	Enable	When FRT connected to ch.(1) is Zero/Bottom status.
	0	10		When FRT connected to ch.(1) is Peak/Top status.
	0	11		When FRT connected to ch.(1) is Zero/Bottom status, or Peak/Top status.
	1	00	Disable	Always when writing to OCCP(1) from CPU.
	1	01	Enable	When FRT connected to ch.(1) is Zero/Bottom status and MSZC=0000.
	1	10		When FRT connected to ch.(1) is Peak/Top status and MSPC=0000.
	1	11		Condition A: FRT connected to ch.(1) is Zero/Bottom status. Condition B: FRT connected to ch.(1) is MSZC=0000. Condition C: FRT connected to ch.(1) is Peak/Top status. Condition D: FRT connected to ch.(1) is MSPC=0000. When (Condition A and Condition B) or (Condition C and Condition D).
Read	-	-	Reads the register setting.	

The following explanation is shared by OCCP0BUFE[1:0], OCCP1BUFE[1:0], OPBM0 and OBPM1.

Change the setting of this bit while the OCU's operation is disabled (OCSA.CST0=0, OCSACST1=0). In FM3 compatible mode (OCSB.FM4=0), there are some restrictions on values that can be set depending on the operation mode. See 4.3 OCU FM3 Family Product-compatible Operation for details.

[bit21:20] OCSE0BUFE[1:0] and [bit26] OEBM0

OCSE0BUFE[1:0] are registers that specify whether to enable or disable the buffer function and the transfer timing of OCSE(0) register. OEBM0 sets the linked transfer settings with the FRT interrupt mask counter.

Process	Value		Function	
	OEBM0	OCSE0 BUFE	Buffer function	Transfer timing
Write	0	00	Disable	Always when writing to OCSE(0) from CPU.
	0	01	Enable	When FRT connected to ch.(0) is Zero/Bottom status.
	0	10		When FRT connected to ch.(0) is Peak/Top status.
	0	11		When FRT connected to ch.(0) is Zero/Bottom status, or Peak/Top status.
	1	00	Disable	Always when writing to OCSE(0) from CPU.
	1	01	Enable	When FRT connected to ch.(0) is Zero/Bottom status and MSZC=0000.
	1	10		When FRT connected to ch.(0) is Peak/Top status and MSPC=0000.
	1	11		Condition A: FRT connected to ch.(0) is Zero/Bottom status. Condition B: FRT connected to ch.(0) is MSZC=0000. Condition C: FRT connected to ch.(0) is Peak/Top status. Condition D: FRT connected to ch.(0) is MSPC=0000. When (Condition A and Condition B) or (Condition C and Condition D).
Read	-	-	Reads the register setting.	

[bit23:22] OCSE1BUFE[1:0] and [bit27] OEBM1

OCSE1BUFE[1:0] are registers that specify whether to enable or disable the buffer function and the transfer timing of OCSE(1) register. OEBM1 sets the linked transfer settings with the FRT interrupt mask counter.

Process	Value		Function	
	OEBM1	OCSE1 BUFE	Buffer Function	Transfer Timing
Write	0	00	Disable	Always when writing to OCSE(1) from CPU.
	0	01	Enable	When FRT connected to ch.(1) is Zero/Bottom status.
	0	10		When FRT connected to ch.(1) is Peak/Top status.
	0	11		When FRT connected to ch.(1) is Zero/Bottom status, or Peak/Top status.
	1	00	Disable	Always when writing to OCSE(1) from CPU.
	1	01	Enable	When FRT connected to ch.(1) is Zero/Bottom status and MSZC=0000.
	1	10		When FRT connected to ch.(1) is Peak/Top status and MSPC=0000.
	1	11		Condition A: FRT connected to ch.(1) is Zero/Bottom status. Condition B:FRT connected to ch.(1) is MSZC=0000. Condition C: FRT connected to ch.(1) is Peak/Top status. Condition D: FRT connected to ch.(1) is MSPC=0000. When (Condition A and Condition B) or (Condition C and Condition D).
Read	-	-	Reads the register setting.	

The following explanation is shared by OCSE0BUFE[1:0], OCSE1BUFE[1:0], OEBM0 and OEBM1..
Change the setting of this register while OCU's operation is disabled (OCSA.CST0=0, OCSACST1=0). In FM3 mode (OCSB.FM4=0), values other than 00 cannot be set for OCSE0BUFE[1:0] and OCSE1BUFE[1:0], and then values other than 0 cannot be set for OEBM0 and OEBM1.

[bit24] OFEX0

This bit is used to extend the matching determination conditions of the connected FRT with the OCCP(0) register value in OCU-ch.(0).

Process	Value	Function
Write	0	Writes 0 to this register and does not extend the matching determination conditions.
	1	Writes 1 to this register and extends the matching determination conditions.
Read	-	Reads the register setting.

[bit25] OFEX1

This bit is used to extend the matching determination conditions of the connected FRT with the OCCP(1) register value in OCU-ch.(1).

Process	Value	Function
Write	0	Writes 0 to this register and does not extend the matching determination conditions.
	1	Writes 1 to this register and extends the matching determination conditions.
Read	-	Reads the register setting.

This description applies to both OFEX0 and OFEX1.
For details about this register function, see the section on the OCSE register. The functions of this register can only be used in FM4 mode (OCSB.FM4=1). Write 0 when set to FM3 compatibility mode (OCSB.FM4=0). This register does not have a buffer function. Change the setting of this bit while OCU operation is prohibited (OCSA:CST0=0).

3.3.13 OCU Control Register E (OCSE)

OCSE is a 16-bit/32-bit register that controls the OCU's operation.
Each mounted channel has six registers: OCSE0 to OCSE5.
OCSE0 controls OCU ch.0 (16-bit register)
OCSE1 controls OCU ch.1 (32-bit register)
OCSE2 controls OCU ch.2 (16-bit register)
OCSE3 controls OCU ch.3 (32-bit register)
OCSE4 controls OCU ch.4 (16-bit register)
OCSE5 controls OCU ch.5 (32-bit register)
Use half-word access for OCSE(0) registers.
Use word access for OCSE(1) registers.

Configuration of Register (OCSE(0))

bit	31	16	15	0
Field	Reserved		OCSE[15:0]	
Attribute	R		R/W	
Initial value	-		0x0000	

Configuration of Register (OCSE(1))

bit	31	0
Field	OCSE[31:0]	
Attribute	R/W	
Initial value	0x0000 0000	

Functions of Register

The OCSE register is a 16/32 bit register that specifies OCU operation. The items below are specified.

- Match detection register (OCSA.IOP0, OCSA.IOP1) setting conditions
- Output signal (RT(0), RT(1)) change conditions

The OCU compares the OCCP register value and FRT value, and the match detection register (OCSA.IOP0 register) and RT(0) output signal are changed based on the setting specified by the OCSE register and OCSD.OFEX0/1 register. The timing when OCU match is detected and the output signal is changed can be changed according to the application.
This register is enabled in FM4 mode (OCSB.FM4=1) only. In FM3 compatibility mode (OCSB:FM4=0), do not overwrite the initial values (All 0).
The OCSE register has a buffer function. When data is written to this address area, the data is first stored in the buffer register. Then, data is transferred to the OCSE register from the buffer register under the conditions below.

- When buffer function is disabled (OCSD.OCSEBUFE=00)
  Data is transferred immediately after it is written to the buffer register.
- When buffer function is enabled (OCSD:OCSEBUFE≠00)
  Data is transferred when FRT counting is stopped (TCSA.STOP=1) or at the specified transfer timing.

When the buffer function is enabled, while OCU operation is allowed, rewriting data to this register enables the setting conditions of the OCU match detection register and the change conditions of the output signal to be changed.
When the buffer function is disabled, OCSE overwriting cannot be performed while OCU operation is allowed.
When data is read from this address area, the OCSE register value, not the buffer register value, is read. This results in reading the previous value until the end of the transfer when the buffer function is enabled. Also, overwriting bits by RMW access to this address area is not allowed.

3.3.13.1 Functions of OCSE(0) bits

OCU-ch.(0) determines the operation details from the connected FRT count status and the OCCP(0)-FRT comparison determination results. The OCSE(0) register has bits for specifying the details for changing the output signal (RT(0)) and the setting conditions of the match detection register (OCSA.IOP0) for the respective control conditions.

Table 3-5 shows the bit positions of the OCSE(0) register that specifies the RT(0) output change conditions and the OCSA.IOP0 register setting conditions once the control conditions are met.

Table 3-5 OCU ch.(0) Control Conditions and Specified Bit Positions

Control Condition		OCSE(0) Specified Bit Position	
FRT Count Status (condition 1)	**Comparison Result of OCCP(0) and FRT (condition 2)**	**Bit Position to Specify RT(0) Output Change Condition**	**Bit Position to Specify IOP0 Set Condition**
Zero/Bottom	Matched	bit [11:10]	bit [3]
	Not matched	bit [15:14]	None:Hold
Up	Matched	bit [9:8]	bit [2]
	Not matched	None:Hold	None:Hold
Peak/Top	Matched	bit [7:6]	bit [1]
	Not matched	bit [13:12]	None:Hold
Down	Matched	bit [5:4]	bit [0]
	Not matched	None:Hold	None:Hold

For the values specified by bit[3:0] of OCSE(0), see Table 3-7. For the values specified by bit[15:4], see Table 3-8. In Table 3-5, when "None:Hold" appears in the bit position field, there is no bit that specifies the operation when the condition is met. When this condition is met, the hold operation of the current value is performed. Also, the FRT which is the comparison target of OCCP(0) refers to the FRT selected by OCFS:FSO0.

The OCCP(0) and FRT comparison determination results are determined to match when OCCP(0)==FRT. However, a match is also determined when the conditions below are met.

- When the FRT to be connected is normal up/down-count mode or up/down-count mode with offset (TCSA:MODE=1), OCCP(0) and FRT are determined to be matched when OCCP(0) is 0xFFFF at the Peak/Top status. This process is not performed when the FRT is normal up-count mode or up-count mode with offset (TCSA:MODE=0).
- When OCSD.OFEX0=1 is set, OCCP(0) and FRT are determined to match if OCCP(0) is at the FRT count value or higher at the Peak/Top status. This process is not performed when OCSD.OFEX0=0.
- When OCSD.OFEX0=1 is set, OCCP(0) and FRT are determined to match if OCCP(0) is at the FRT count value or lower at the Zero/Bottom status. This process is not performed when OCSD.OFEX0=0.

The details above are shown in Table 3-6. The X in the table indicates that the conditions are ignored. In TYPE1-M4 and TYPE2-M4 products, OCSD.OFEX0 is considered to be 0.

Table 3-6 OCCP(0) and FRT Match Determination Conditions

OCSD. OFEX0	TCSA. MODE	FRT Count State	Comparison of OCCP(0) and 0xFFFF	Comparison of OCCP(0) and FRT	Comparison Determination Results
X	X	X	X	Matched	Matched
X	1	Peak/Top	Matched	X	Matched
1	X	Zero/Bottom	X	OCCP(0) <= FRT	Matched
		Peak/Top	X	OCCP(0) >= FRT	Matched
When the above conditions do not apply					Not matched

The following explains the operations of the OCU with the values set for each bit of the OCSE(0) register.

[bit3:0] OCSE(0) [3:0]

Specification for bit[3:0] is used to specify set conditions for match detection register (OCSA.IOP0).

Table 3-7 OCSE(0)[3:0] Specified Details

Process	Value	Function
Write	0	When conditions 1 and 2 in Table 3-5 are met, IOP0 is held. (Hold)
	1	When conditions 1 and 2 in Table 3-5 are met, IOP0 is set. (Set)
Read	-	Reads the register setting (not buffer register values).

(Example of specification)

- When OCSE0[0]=0 is specified and FRT=OCCP0 is detected while FRT is counting down, the IOP0 value is held at that time (Hold).
- When OCSE0[0]=1 is specified and FRT=OCCP0 is detected while FRT is counting down, the IOP0 value is set to 1 at that time (Set).

[bit15:4] OCSE(0) [15:4]

The various change conditions for output signal: RT(0) are specified by specifying every two bits of bit[15:4].

Table 3-8 OCSE(0)[15:4] Specified Details

Process	Value	Function
Write	00	When conditions 1 and 2 in Table 3-5 are met, RT(0) output signal is held. (Hold)
	01	When conditions 1 and 2 in Table 3-5 are met, RT(0) output signal is set to High. (Set)
	10	When conditions 1 and 2 in Table 3-5 are met, RT(0) output signal is set to Low. (Reset)
	11	When conditions 1 and 2 in Table 3-5 are met, RT(0) output signal is reversed. (Reverse)
Read	-	Reads OCSE(0) register value (not buffer register values).

(Example of specification)

- When OCSE0[5:4]=00 if FRT=OCCP0 is detected while FRT is counting down, match detection is ignored, RT0 output is held (Hold).
- When OCSE0[5:4]=01, if FRT=OCCP0 is detected while FRT is counting down, RT0 output is set to High level. If the signal is already at the High level at this point, the High level continues. (Set)
- When OCSE0[5:4]=10, if FRT=OCCP0 is detected while FRT is counting down, RT0 output is set to Low level. If the signal is already at the Low level at this point, the Low level continues. (Reset)
- When OCSE0[5:4]=11, if FRT=OCCP0 is detected while FRT is counting down, RT0 output is reversed. If the signal is at the Low level at this point, it is changed to the High Level. If the signal is at the High level at this point, it is changed to the Low level. (Reverse)

See 4.2 Description of OCU Operation for examples of detailed settings for OSCE register.

3.3.13.2 Functions of OCSE(1) bits

OCU-ch.(1) determines the operation details from the connected FRT count status and the OCCP(0), OCCP(1), and FRT comparison determination results. The OCSE(1) register has bits for specifying the change details for the output signal (RT(1)) and the setting conditions of the match detection register (OCSA.IOP1) for the respective control conditions. In addition to the comparison results of OCCP(1) and FRT, OCU-ch.(1) can be used for output signal control of the OCCP(0) and FRT comparison results.

Table 3-9 shows the bit positions of the OCSE(1) register which specifies the RT(1) output change conditions and OCSA.IOP1 register setting conditions once the control conditions are met.

Table 3-9 OCU ch.(1) Control Conditions and Specified Bit Positions

Control Conditions			Specified Bits	
FRT Count Status (condition 1)	**Comparison Results of OCCP(1) and FRT (condition 2)**	**Comparison Results of OCCP(0) and FRT (condition 3)**	**Bit Position to Specify RT(1) Output Change Condition**	**Bit Position to Specify IOP1 Set Condition**
Zero/Bottom	Matched	Matched	bit [27:26]	bit [3]
	Matched	Not matched	bit [11:10]	
	Not matched	Matched	bit [31:30]	None:Hold
	Not matched	Not matched	bit [15:14]	
Up	Matched	Matched	bit [25:24]	bit [2]
	Matched	Not matched	bit [9:8]	
	Not matched	Matched	bit [19:18]	None:Hold
	Not matched	Not matched	None:Hold	
Peak/Top	Matched	Matched	bit [23:22]	bit [1]
	Matched	Not matched	bit [7:6]	
	Not matched	Matched	bit [29:28]	None:Hold
	Not matched	Not matched	bit [13:12]	
Down	Matched	Matched	bit [21:20]	bit [0]
	Matched	Not matched	bit [5:4]	
	Not matched	Matched	bit [17:16]	None:Hold
	Not matched	Not matched	None:Hold	

For the values specified by bit[3:0] of OCSE(1), see Table 3-11. For the values specified by bit[31:4], see Table 3-12. In Table 3-9, when "None:Hold" appears in the bit position field, there is no bit that specifies the operation when the condition is met. When this condition is met, the hold operation of the current value is performed. Also, the FRT that is the target for comparison with OCCP(0) refers to the FRT selected by OCFS:FSO0, and the FRT that is the target for comparison with OCCP(1) refers to the FRT selected by OCFS:FSO1.

The OCCP(0) and FRT comparison determination results are determined to match when OCCP(0)==FRT. However, a match is also determined when the conditions shown in Table 3-6 are met.

The OCCP(1) and FRT comparison determination results are determined to match when OCCP(1)==FRT. However, a match is also determined when the conditions shown below are met.

- When the FRT to be connected is normal up/down-count mode or up/down-count mode with offset (TCSA:MODE=1), OCCP(1) and FRT are determined to match when OCCP(1) is 0xFFFF at the Peak/Top status. This process is not performed when the FRT is normal up-count mode or up-count mode with offset (TCSA:MODE=0).
- When OCSD.OFEX1=1 is set, OCCP(1) and FRT are determined to match if OCCP(1) is at the FRT count value or higher at the Peak/Top status. This process is not performed when OCSD.OFEX1=0.

- When OCSD.OFEX1=1 is set, OCCP(1) and FRT are determined to match if OCCP(1) is at the FRT count value or lower at the Zero/Bottom status. This process is not performed when OCSD.OFEX1=0.

The above details are shown in Table 3-10. The X in the table indicates that the conditions are ignored. In TYPE1-M4 and TYPE2-M4 products, OCSD.OFEX1 is considered to be 0.

Table 3-10 OCCP(1) and FRT Match Determination Conditions

OCSD. OFEX1	TCSA. MODE	FRT Count State	Comparison of OCCP(1) and 0xFFFF	Comparison of OCCP(1) and FRT	Comparison Determination Results
X	X	X	X	Matched	Matched
X	1	Peak/Top	Matched	X	Matched
1	X	Zero/Bottom	X	OCCP(1) <= FRT	Matched
		Peak/Top	X	OCCP(1) >= FRT	Matched
When the above conditions do not apply					Not matched

The following explains the operations of the OCU with the values set for each bit of the OCSE(1) register.

[bit3:0] OCSE(1) [3:0]

The setting conditions for interrupt flag (OCSA.IOP1) are specified by specifying each bit of bit[3:0].

Table 3-11 OCSE(1)[3:0] Specified Details

Process	Value	Function
Write	0	When conditions 1 and 2 in Table 3-9 are met, IOP1 is held. (Hold) Condition 3 is ignored.
	1	When conditions 1 and 2 in Table 3-9 are met, IOP0 is set. (Set) Condition 3 is ignored.
Read	-	Reads the register setting (not buffer register values).

[bit31:4] OCSE(1) [31:4]

The change conditions for output signal: RT(1) are specified by specifying every two bits of bit[31:4].

Table 3-12 OCSE(1)[31:4] Specified Details

Process	Value	Function
Write	00	When conditions 1, 2 and 3 in Table 3-9 are met, RT(1) output signal is held. (Hold)
	01	When conditions 1, 2 and 3 in Table 3-9 are met, RT(1) output signal is set to High. (Set)
	10	When conditions 1, 2 and 3 in Table 3-9 are met, RT(1) output signal is set to High. (Reset)
	11	When conditions 1, 2 and 3 in Table 3-9 are met, RT(1) output signal is reversed. (Reverse)
Read	-	Reads the register setting (not buffer register values).

Example of specification:

- When OCSE1[5:4]=00, if FRT≠OCCP0 and FRT=OCCP1 are detected while the FRT is counting down, match detection is ignored, RT0 output is held. (Hold)
- When OCSE1[5:4]=01 and FRT≠OCCP0 and FRT=OCCP1 are detected while FRT is counting down, RT0 output is set to High level. If the signal is already at the High level at this point, the High level continues. (Set)
- When OCSE1[5:4]=10 and FRT≠OCCP0 and FRT=OCCP1 are detected while FRT is counting down, RT0 output is set to Low level. If the signal is already at the Low level at this point, the Low level continues. (Reset)
- When OCSE1[5:4]=11 and FRT≠OCCP0 and FRT=OCCP1 are detected while FRT is counting down, RT0 output is reversed. If the signal is at the High level at this point, it is changed to the Low level. (Reverse)

See 4.2 Description of OCU Operation for examples of detailed settings for OSCE register.

3.3.13.3 Channel Independent Operation and Channel Linked Operation

The RT(0) output signal of OCU-ch.(0) can be activated by the OCCP(0) register and the FRT comparison results. By contrast, the RT(1) output signal of OCU-ch.(1) can be selected to be activated by either the OCCP(1) register and FRT comparison results (channel independent operation) or be activated by both the comparison results of the OCCP(0) register and OCCP(1) register (channel linked operation).

When a 12-bit value that is the same as bit[31:20] and bit[15:4] of the OCSE(1) register is specified, and bit[19:16]=0000 is specified, the effect of the OCCP(0) value can be eliminated from the change conditions of the RT(1) output signal of OCU-ch.(1). This is because the RT(1) change conditions when the OCCP(0) and FRT comparison results match and do not match are completely identical to the comparison results of OCCP(1).

In the case of these setting conditions, usage as separate independent OCU is possible where the RT(0) output of ch.(0) is controlled by OCCP(0) and where the RT(1) output of ch.(1) is controlled by OCCP(1). If these conditions are not satisfied, the RT(1) output signal of ch.(1) is affected by the OCCP(0) value in some form or another, and independent operation is not performed.

3.3.14 OCU Compare Value Store Register (OCCP)

The OCCP is a 16-bit register that specifies the timing of the OCU's output signal changes as the compare value of the FRT's count value.
Each mounted channel has six registers: OCCP0 to OCCP5.

OCCP0 stores the compare value of OCU ch.0 (also available for OCU ch.1).
OCCP1 stores the compare value of OCU ch.1.
OCCP2 stores the compare value of OCU ch.2 (also available for OCU ch.3).
OCCP3 stores the compare value of OCU ch.3.
OCCP4 stores the compare value of OCU ch.4 (also available for OCU ch.5).
OCCP5 stores the compare value of OCU ch.5.
It should be noted that this register does not allow for byte access.

Configuration of Register

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Field	OCCP[15:0]															
Attribute	R/W															
Initial value	0x0000															

Functions of Register

The OCCP is a 16-bit register that specifies the timing of OCU output signal changes as the compare value of the FRT's count value. When data is written to this address area, the data is first stored in the buffer register. And then, the data is transferred from the buffer register to the OCCP register under the following conditions.

- When the buffer function is disabled (OCSD.OCCPBUFE=00), data is transferred immediately after it is written to the buffer register.
- Data is transferred when the buffer function is enabled (OCSD.OCCPBUFE≠00), data is transferred FRT is stopped counting (TCSA.STOP=1) or at a specified transfer timing.

When the OCU's operation is enabled, the pulse width of OCU's output signals (RT(0), RT(1)) can be changed by rewriting to this register. When the buffer function is disabled, the written value can be immediately reflected in the OCCP register. When the buffer function is enabled, the OCCP registry settings for multiple channels can be synchronized. When an FRT to be connected is in Up/Down-count mode (TCSA.MODE=1), writing 0xFFFF to this register value allows processing for fixed outputs.

When data is read from the address area, values are read from the OCCP register, not from the buffer register. This results in reading the previous value until the end of the transfer when buffer function is enabled. Bit rewriting with RMW access to this area is not allowed.

[bit31:16] OCCP[15:0]

bit	Function
Write	Specifies the timing of OCU output signal changes. Stores the written value in the buffer register.
Read	Reads the value in the OCCP register (not the value in the OCCP buffer register).

3.3.15 WFG Control Register A (WFSA)

WFSA is a 16-bit register that controls WFG operation.
Each mounted channel has three registers: WFSA10, WFSA32 and WFSA54.
WFSA10 controls WFG ch.10 (the output processing block of OCU ch.1 and OCU ch.0).
WFSA32 controls WFG ch.32 (the output processing block of OCU ch.3 and OCU ch.2).
WFSA54 controls WFG ch.54 (the output processing block of OCU ch.5 and OCU ch.4).

Configuration of Register

bit	15	14	13	12	11	10	9	8
Field	Reserved	Reserved	DMOD[1:0]		PGEN[1:0]		PSEL[1:0]	
Attribute	R	R	R/W		R/W		R/W	
Initial value	-	-	00		00		00	

bit	7	6	5	4	3	2	1	0
Field	GTEN[1:0]		TMD[2:0]			DCK[2:0]		
Attribute	R/W		R/W			R/W		
Initial value	00		000			000		

Functions of Register

[bit2:0] DCK[2:0]

These bits are bits that set the count clock cycle for the WFG timer and Pulse counter.

The clock for the WFG timer and Pulse counter in WFG is generated by dividing the peripheral clock (PCLK), which is connected to the MFT, by the prescaler. These bits set the division ratio of the prescaler. The count clock cycle for the WFG timer and Pulse counter is determined according to the PCLK cycle and the clock division ratio set by this register.

Change the setting of these bits, while the WFG timer and Pulse counter are stopped.

Process	Value	Function
Write	000	Sets the count clock cycle to the same value as PCLK.
	001	Sets the count clock cycle to PCLK multiplied by 2.
	010	Sets the count clock cycle to PCLK multiplied by 4.
	011	Sets the count clock cycle to PCLK multiplied by 8.
	100	Sets the count clock cycle to PCLK multiplied by 16.
	101	Sets the count clock cycle to PCLK multiplied by 32.
	110	Sets the count clock cycle to PCLK multiplied by 64.
	111	Sets the count clock cycle to PCLK multiplied by 128.
Read	-	Reads the register setting.

The table below shows examples of DCK[2:0] settings and the count clock cycle for the WFG timer and Pulse counter.

DCK[2:0]	Cycle Ratio	Count Clock Cycle for WFG Timer and Pulse Counter		
		PCLK=25 ns (40 MHz)	PCLK=12.5 ns (80 MHz)	PCLK=6.25 ns (160 MHz)
000	1	25 ns	12.5 ns	6.25 ns
001	2	50 ns	25 ns	12.5 ns
010	4	100 ns	50 ns	25 ns
011	8	200 ns	100 ns	50 ns
100	16	400 ns	200 ns	100 ns
101	32	800 ns	400 ns	200 ns
110	64	1.6 µs	800 ns	400 ns
111	128	3.2 µs	1.6 µs	800 ns

[bit5:3] TMD[2:0]

These bits are bits that select the WFG's operation mode.

Process	Value	Function	Availability of reload timer
Write	000	Through mode	○
	001	RT-PPG mode	○
	010	Timer-PPG mode	○
	011	Setting is prohibited.	×
	100	RT-dead timer mode	○
	101	RT-dead timer filter mode	×
	110	PPG-dead timer filter mode	×
	111	PPG-dead timer mode	○
Read	-	Reads the register setting.	-

For the operation modes using these bit settings, see 4.4 Description of WFG Operation. When the WFG's operation mode is set to a mode that does not use the Pulse counter (○ in the table), the WFG timer can be used as a 16bit reload timer independent of wave form generation.

Change the setting of these bits while the OCU and PPG timer unit to be connected are stopped. If the value set in this register is rewritten to a different value, the count states of the WFG timer and Pulse counter are reset.

[bit7:6] GTEN[1:0]

These bits are a register that selects the output conditions for the CH_GATE output signal of the WFG. The CH_GATE signal generated commands the PPG to start. Change this register setting while the OCU and PPG timer units to be connected are stopped. Each WFG channel can output a GATE signal that starts the PPG and superimpose the PPG signal from the PPG timer unit on the RT signal from the OCU for output. See 4.4 Description of WFG Operation for detail.

Process	Value	Function
Write	00	Does not generate the CH_GATE signal.
	Other than above	Generates the CH_GATE signal. For details, see 4.4 Description of WFG Operation.
Read	-	Reads the register setting.

[bit9:8] PSEL[1:0]

These bits are bits that select the PPG timer unit to be used for each channel of the WFG. These bits select the PPG timer unit to be used as the output destination of the GATE signal and the input source of the PPG signal all at once. Change the setting of this register while the OCU and PPG timer unit to be connected are stopped.

Process	Value	Function
Write	00	Sets the output destination of the GATE signal to ch.0 of the PPG timer unit. Sets the input source of the PPG signal to ch.0 of the PPG timer unit.
	01	Sets the output destination of the GATE signal to ch.2 of the PPG timer unit. Sets the input source of the PPG signal to ch.2 of the PPG timer unit.
	10	Sets the output destination of the GATE signal to ch.4 of the PPG timer unit. Sets the input source of the PPG signal to ch.4 of the PPG timer unit.
	11	Setting is prohibited.
Read	-	Reads the register setting.

Figure 3-4 shows a configuration diagram of the PPG selector. The following section explains the configuration and operation of the PPG selector.

Each channel of the WFG can output a trigger signal (CH_GATE signal) to start the PPG timer unit. The CH10_GATE signal, CH32_GATE signal and CH54_GATE signal refer to the GATE signal for each channel of WFG, which has been generated at WFG ch.10, WFG ch.32 and WFG ch.54, respectively.

After the output is selected by WFSA:PSEL[1:0] for each PPG timer unit to be connected, each CH_GATE signal undergoes a logical OR by the PPG timer unit and is output to each PPG unit.

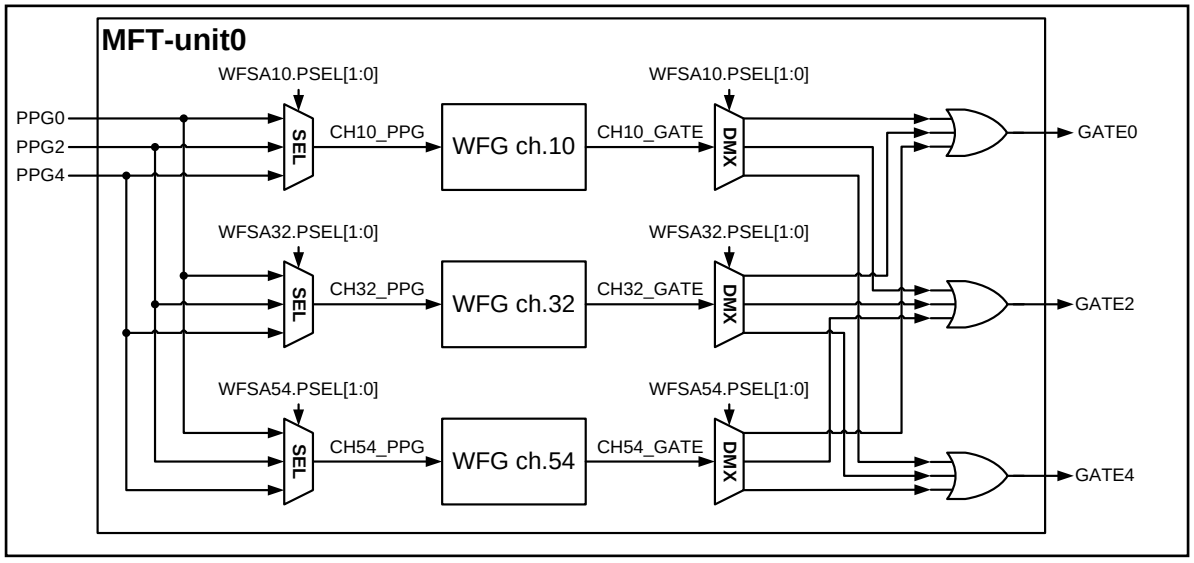
The GATE0 signal, GATE2 signal and GATE4 signal refer to the GATE signal that is output to ch.0, ch.2 and ch.4 of the PPG timer unit, respectively.

Each PPG timer unit can be started by a GATE signal and output the PPG signal.

The PPG0 signal, PPG2 signal and PPG4 signal refer to the PPG signal that is output from ch.0, ch.2 and ch.4 of the PPG timer unit, respectively, and input to WFG.

The CH10_PPG signal, CH32_PPG signal and CH54_PPG signal refer to the PPG signal that is used at WFG ch.10, WFG ch.32 and WFG ch.54 respectively, of which input has been selected by WFSA.PSEL[1:0].

Figure 3-4 Diagram of PPG Selector Configuration



■ Example PSEL register setting 1

When WFSA10:PSEL[1:0]=00, WFSA32:PSEL[1:0]=00 and WFSA54:PSEL[1:0]=00 are set, ch.0 of the PPG timer unit is shared by all the channels of WFG. GATE0 becomes the logic OR signal of CH10_GATE, CH32_GATE and CH54_GATE. Both GATE2 and GATE4 are set to Low fixed output. Each channel of WFG instructs ch.0 of the PPG timer unit to start up.

CH10_PPG, CH32_PPG and CH54_PPG all become PPG0 signals. Each channel of WFG uses the output signal of ch.0 of the PPG timer unit for waveform generation.

■ Example PSEL register setting 2

When WFSA10:PSEL[1:0]=00, WFSA32:PSEL[1:0]=01 and WFSA54:PSEL[1:0]=10 are set, ch.0, ch.2 and ch.4 of the PPG timer unit are used individually for each channel of WFG. GATE0=CH10_GATE, GATE2=CH32_GATE, and GATE4=CH54_GATE are output separately. Each channel instructs ch.0, ch.2 or ch.4 of the PPG timer unit to start up, individually.

CH10_PPG = PPG0, CH32_PPG=PPG2, and CH54_PPG=PPG4 are set. Each channel of WFG uses the output signal of the corresponding PPG timer unit for waveform generation.

Notes:

- *The channel number of the PPG timer unit to be connected is different per MFT unit depending on the PSEL[1:0] value. The descriptions above are intended for the PSEL[1:0] bits in MFT unit0. For information about MFT-unit1 and –unit2, see 4.9 PPG Timer Unit Connected to WFG.*
- *To use the GATE signal, the PPG timer unit must be set beforehand. For details, see the chapter PPG.*
- *Even without the use of the GATE signal, the PPG timer unit can start outputting upon instruction by the CPU.*

[bit11:10] PGEN[1:0]

PGEN[1:0] is the bit that specifies how to reflect the CH_PPG signal that is input to each channel of the WFG to the WFG output. Change the setting while the OCU and the PPG timer units to be connected are stopped. See 4.4 Description of WFG Operation for detail.

Process	Value	Function
Write	00	Does not reflect the CH_PPG signal to WFG output (RTO output).
	Other than above	Specifies the condition to be used to reflect the CH_PPG signal to WFG output. For details of the conditions for reflecting signals to WFG output, see “4.4 Description of WFG Operation”.
Read	-	Reads the register setting.

When the WFG's operation mode is set to Through mode, the CH_PPG signal can be output to the RTO pin without any change, according to the PGEN[1:0] setting. This register setting has no meaning when TMD[2:0] is set to 100 101,110, 111.

[bit13:12] DMOD

These bits are bits that specifies polarity for RTO(0) and RTO(1) signal outputs. Change the setting while the OCU and PPG timer units to be connected are stopped.

Process	Value	Function
Write	00	Outputs RTO(1) and RTO(0) signals without changing the level.
	01	Outputs both RTO(1) and RTO(0) signals reversed.
	10	Outputs the RTO(0) signal reversed. Outputs the RTO(1) signal without changing the level.
	11	Outputs the RTO(0) signal without changing the level. Outputs the RTO(1) signal reversed.
Read	-	Reads the register setting.

This bit setting allows the polarity for RTO(0) and RTO(1) output signals to be selected. This bit is valid for any value of TMD[2:0]. Note that the scope of validity of the function of this bit is different from FM3 family products.

In RT dead timer mode, RT dead timer filter mode, PPG dead timer mode, and PPG dead timer filter mode (WFSA.TMD=100, 101, 110, 111), DMOD=00,01 is used when using IGBT, N-Ch driver × 2, or other same-polarity driver. DMOD=10,11 is used when using MOSFET(N-Ch＋P-Ch) or other drivers with different polarity. Check and set the specifications for the driver that is connected.

Notes:

- *As shown in Figure 4-44 of 4.4.12 Output Polarity Revered by WESA.DMOD, if RT dead timer mode (WFSA.TMD=100), DMOD=10, or other incorrect settings are made, a short-circuit will occur between the power supply and GND.*
- *Be aware that the range for which this register function is enabled is different from the range of FM3 Family products.*

[bit15:14] Reserved

Writing is invalid. Undefined value is read.

3.3.16 WFG Timer Value Register (WFTA/WFTB)

WFTA and WFTB are 16-bit registers that set the initial value of the WFG timer.
Each mounted channel has six registers: WFTA10, WFTB10, WFTA32, WFTB32, WFTA54 and WFTB54.
WFTA10 and WFTB10 set the initial value of the WFG timer for WFG ch.10.
WFTA32 and WFTB32 set the initial value of the WFG timer for WFG ch.32.
WFTA54 and WFTB54 set the initial value of the WFG timer for WFG ch.54.
It should be noted that these registers do not allow for byte access.

Configuration of Register

bit	31	16	15	0
Field	WFTB[15:0]		WFTA[15:0]	
Attribute	R/W		R/W	
Initial value	0x0000		0x0000	

Functions of Register

WFTA[15:0] and WFTB[15:0] are applied in each WFG mode as shown in the table below:

Operation mode	TMD	WFTA	WFTB
Through mode	000	Ignored.	Ignored.
RT-PPG mode	001	Ignored.	Ignored.
Timer-PPG mode	010	Number of WFG timer counts from RT(0) rising edge	Number of WFG timer counts from RT(1) rising edge
RT-dead timer mode	100	Number of WFG timer counts from RTO(0) falling edge to RTO(1) rising edge (Polarity is positive)	Number of WFG timer counts from RTO(1) falling edge to RTO(0) rising edge (Polarity is positive)
RT-dead timer filter mode	101		
PPG-dead timer filter mode	110		
PPG-dead timer mode	111		

The WFTA and WFTB registers hold the initial reload values for the WFG timer circuit. The WFG timer circuit loads the initial values from the WFTA and WFTB registers and starts counting down. The operating time of the WFG timer can be set as shown below. Setting 0x0000 means 65536.

Operating time of WFG timer = (WFTA value or WFTB value) × Operation clock cycle of WFG timer

These registers are rewritten independently of whether the WFG timer is running or stopped. When these registers are rewritten, the time at which the values become valid is from the next timer startup.

[bit31:16] WFTA[15:0], [bit15:0] WFTB[15:0]

Process	Function
Write	Sets the initial value of the WFG timer. Setting 0x0000 means 65536 setting.
Read	Reads the register setting.

3.3.17 Pulse Counter Value Register (WFTF)

WFTF is a 16-bit register that sets the initial value of a Pulse counter.
Each mounted channel has three registers: WFTF10, WFTF32 and WFTF54.
WFTF10 sets the initial value of the Pulse counter for WFG ch.10.
WFTF32 sets the initial value of the Pulse counter for WFG ch.32.
WFTF54 sets the initial value of the Pulse counter for WFG ch.54.
It should be noted that this register does not allow for byte access.

Configuration of Register

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Field	WFTF[15:0]															
Attribute	R/W															
Initial value	0x0000															

Functions of Register

WFTF[15:0] is applied in each WFG mode as shown in the table below:

Operation mode	TMD	WFTF
Through mode	000	Number of 16-bit reload timer counts
RT-PPG mode	001	
Timer-PPG mode	010	
RT-dead timer mode	100	
RT-dead timer filter mode	101	Number of filter counts
PPG-dead timer filter mode	110	
PPG-dead timer mode	111	Number of 16-bit reload timer counts

The WFTF register holds the initial reload value for the Pulse counter circuit. The internal Pulse counter circuit loads the initial value from the WFTF register and starts counting down. The operating time of the Pulse counter can be set as shown below. Setting 0x0000 means 65536.

Operating time of Pulse counter = (WFTF value) × Operation clock cycle of Pulse counter

This register is rewritten independently of whether the Pulse counter is running or stopped. When this register is rewritten, the time at which the values become valid is from the next Pulse counter startup.

[bit31:16] WFTF[15:0]

Process	Function
Write	Sets the initial value of a Pulse counter. Setting 0x0000 means setting 65536.
Read	Reads the register setting.

3.3.18 NZCL Control Register (NZCL)

NZCL is a 16-bit register that controls DTIF interrupts (interrupts for emergency motor shutdown by signal input from the DTTIX pin) and reload timer interrupts for the WFG.

Configuration of Register

bit	15	14	13	12	11	10	9	8
Field	Reserved	WIM54	WIM32	WIM10	Reserved	Reserved	DIMB	DIMA
Attribute	R/W	R/W	R/W	R/W	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Field	DHOLD	Reserved	DTIEB	SDTI	NWS[2:0]			DTIEA
Attribute	R/W	R/W	R/W	W	R/W			R/W
Initial value	0	0	0	0	000			0

Functions of Register

[bit0] DTIEA

The DTIEA is the register which selects whether the WFIR.DTIFA register is set for the path via digital noise filter from the DTTIX input pin.

Process	Value	Function
Write	0	Disables the path for digital noise filter from DTTIX pin.
	1	Enables the path for digital noise filter from DTTIX pin.
Read	-	Reads the register setting.

[bit3:1] NWS[2:0]

NWS[2:0] are registers that set the noise-canceling width for a digital noise-canceller.

Process	Value	Function
Write	000	DTIF interrupt is generated immediately after Low-level input from the DTTIX pin. (No noise-canceling)
	001	Sets the noise-canceling width to 4 PCLK cycles.
	010	Sets the noise-canceling width to 8 PCLK cycles.
	011	Sets the noise-canceling width to 16 PCLK cycles.
	100	Sets the noise-canceling width to 32 PCLK cycles.
	101	Sets the noise-canceling width to 64 PCLK cycles.
	110	Sets the noise-canceling width to 128 PCLK cycles.
	111	Sets the noise-canceling width to 256 PCLK cycles. (See margin.)
Read	-	Reads the register setting.

- The NWS=111 setting is possible for TYPE3-M4 products and later only. The NWS=111 setting is prohibited for TYPE1-M4 and TYPE2-M4 products.

[bit4] SDTI

The SDTI bit is a bit that sets the WFIR.DTIFA register by writing to the register from the CPU.

Process	Value	Function
Write	0	Does nothing.
	1	Forcibly sets WFIR.DTIFA independently of DTIEA setting.
Read	-	0 is always read.

Writing 1 to this register sets the WFIR.DTIFA register and generates a DTIF interrupt irrespective of the NZCL:DTIE setting and the state of the DTTIX pin. Writing to this register allows for the use of the output switch function for the RTO pin in the I/O port controller. The generated interrupt signal is deasserted by clearing the WFIR:DTIFA register (i.e. writing 1 to the WFIR:DTICA register).

[bit5] DTIEB

The DTIEB is the register that selects whether to set the WFIR.DTIFB flag for the path from the DTTIX pin for input signal to an analog noise filter.

This bit can be used for TYPE3-M4 products and later only. Be sure to always set to 0 for TYPE1-M4 and TYPE2-M4 products.

Process	Value	Function
Write	0	Disables the path from DTTIX pin to analog noise filter.
	1	Enables the path from DTTIX pin to analog noise filter.
Read	-	Reads the register setting.

[bit6] Reserved: Reserved bits

0 must be written at write access. Read value is 0.

[bit7] DHOLD

This bit is used to select whether the RTO output signal of WFG is held when the DTIF interrupt signal is asserted.

This bit can be used for TYPE3-M4 products and later only. Be sure to always set to 0 for TYPE1-M4 and TYPE2-M4 products.

Process	Value	Function
Write	0	Does not hold WFG-RTO output signal when DTIF interrupt signal is asserted.
	1	Holds WFG-RTO output signal when DTIF interrupt signal is asserted.
Read	-	Reads the register setting.

[bit8] DIMA

DIMA is the register that selects whether a DTIF interrupt is masked when the WFIR.DTIFA flag is set.

Process	Value	Function
Write	0	DTIF interrupt is enabled.
	1	DTIF interrupt is disabled.
Read	-	Reads the register setting.

[bit9] DIMB

DIMB is the register that selects whether a DTIF interrupt is masked when the WFIR.TIFDTIFB flag is set.

This bit can be used for TYPE3-M4 products and later only. Be sure to always set to 0 for TYPE1-M4 and TYPE2-M4 products.

Process	Value	Function
Write	0	DTIF interrupt is enabled.
	1	DTIF interrupt is disabled.
Read	-	Reads the register setting.

[bit11:10] Reserved: Reserved bits

00 must be written at write access. Read value is 00.

[bit12] WIM10

WIM10 is the register that selects whether a WFG10 reload timer interrupt is masked when the WFIR.TMIF10 flag is set.

Process	Value	Function
Write	0	WFG10 reload timer interrupt is enabled.
	1	WFG10 reload timer interrupt is disabled.
Read	-	Reads the register setting.

[bit13] WIM32

WIM32 is the register that selects whether a WFG32 reload timer interrupt is masked when the WFIR.TMIF32 flag is set.

Process	Value	Function
Write	0	WFG32 reload timer interrupt is enabled.
	1	WFG32 reload timer interrupt is disabled.
Read	-	Reads the register setting.

[bit14] WIM54

WIM54 is the register that selects whether a WFG54 reload timer interrupt is masked when the WFIR.TMIF54 flag is set.

Process	Value	Function
Write	0	WFG54 reload timer interrupt is enabled.
	1	WFG54 reload timer interrupt is disabled.
Read	-	Reads the register setting.

[bit15] Reserved

0 must be written at write access. Read value is 0.

3.3.18.1 Operations of NZCL

Figure 3-5 shows a block diagram and time chart of the DTTIX pin and DTIF interrupt.

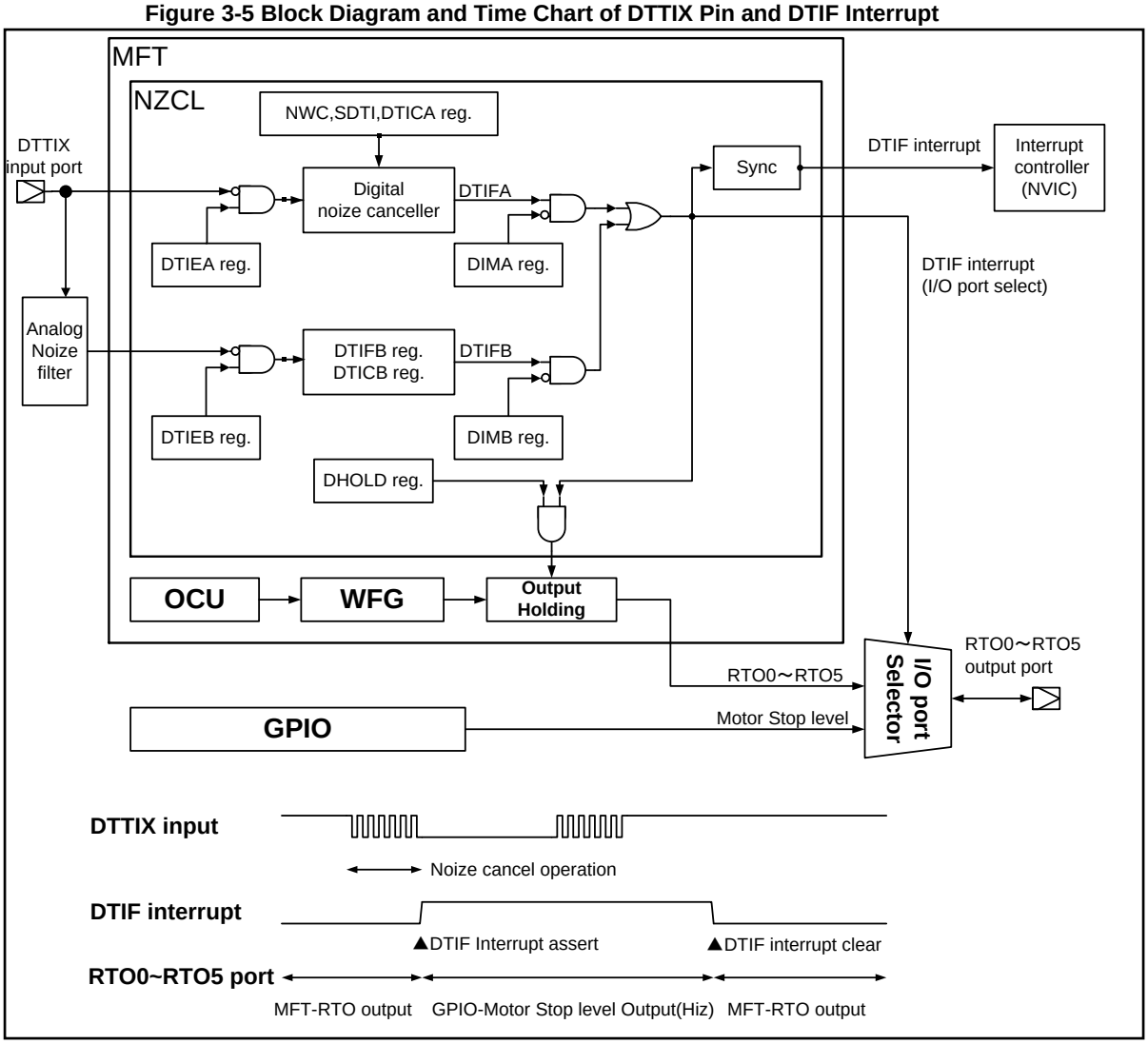
The DTTIX pin is a special pin dedicated to inputting an external signal for emergency motor shutdown. When a Low level is input, it recognizes the signal as a request for emergency motor shutdown.
The input signal to this pin is processed with 2 systems in NZCL to notify the interrupt controller as an interrupt signal.

Whether the system to be input to a digital noise-canceller circuit from the DTTIX pin is enabled or disabled is selected by the NZCL:DTIEA register. If a Low-level pulse no less than the value set by the noise canceller (NZCL.NWS) is input, the WFIR:DTIFAF register is set.

Whether the system to be input to analog noise filter from the DTTIX pin is enabled or disabled is selected by the NZCL:DTIEB register. If a Low-level pulse no less than the value specified by the analog noise filter is input, the WFIR:DTIFB register is set.

DTIF interrupt when the WFIR:DTIFA or WFIR:DTIFB register is set can be masked with NZCL:DIMA and NZCL:DIMB respectively. When either the WFIR:DTIFA register or the WFIR:DTIFB register is set without an interrupt mask, the DTIF interrupt signal is asserted to generate an interrupt to the CPU (See Figure below).

Figure 3-5 Block Diagram and Time Chart of DTTIX Pin and DTIF Interrupt



The DTIF interrupt signal is connected to the interrupt controller and the I/O port selector. The I/O port selector can switch the state of output pins RTO0 to RTO5 to the setting state of the shared GPIO port, while the DTIF interrupt is being generated. As the timing chart described in this figure, the signal required for emergency motor shutdown can be output to pins RTO0 to RTO5 by setting the GPIO pin shared with the RTO0 to RTO5 pins to the motor non-operating level beforehand.

The path of the DTIF interrupt signal that passes through an analog noise filter has a configuration that does not use an MCU clock. When this path is enabled, if the MCU clock is stopped, the DTIF interrupt cannot be recognized, but output for emergency stopping of the motor can be issued to the RTO0 through RTO05 terminals. This clockless DTIF function can be used in TYPE3-M4 products and later.

If 1 is set for the NZCL.DHOLD register, the RTO0 to RTO5 output signals are held when the DTIF interrupt signal is asserted. The output level immediately before can be held until the DTIF interrupt is cleared by the CPU.

The generated interrupt signal is deasserted by clearing the WFIR:DTIFA and WFIR:DTIFB registers (writing 1 to both WFIR:DTICA and WFIR:DTICB registers).

3.3.18.2 Setting for GPIO Switchover Function

Table 3-13 shows a list of function settings for the GPIO pin. PFR, DDR and PDOR in the table refer to the corresponding registers of the GPIO port that are shared with pins RTO0 to RTO5.

Table 3-13 Setting List of Motor Non-operating Level by DTTIX Pin Interrupt

	Setting of GPIO Register					Setting of NZCL	DTIF Signal Level	State of RTO Pin
	PFR	EPFR1[11:0]	EPFR1[12]	DDR	PDOR	DHOLD		
When switching output state of pin by DTIF interrupt	1	101010101010 or 010101010101	1	1	1	0	0	Output RTO0 - RTO5
							1	Output High level
				1	0		0	Output RTO0 - RTO5
							1	Output Low level
				0	Setting ignored		0	Output RTO0 - RTO5
							1	Hi-Z state
When not switching output state of pin by DTIF interrupt			0	Setting ignored	Setting ignored		Signal state ignored	Output RTO0 - RTO5
When the terminal previous output state is held by DTIF interrupt						1	0	Output RTO0 - RTO5
							1	Output RTO0 - RTO5 immediately before is held

- PFR, EPFR1[11:0] is the basic setting for using the LSI pin as RTO output of MFT.
- EPFR1[12] specifies whether or not to switch the pin function by interrupt.
- Setting the DDR, PDOR register specifies the motor non-operating level when the pin function is switched.
- The EPFR1 register controls the pin used in MFT unit0. In the case of MFT unit1, the EPFR2 is used.

If the output state is not to be switched by DTIF interrupt (EPFR1[12]=0), the state of the output pin is not switched, but a DTIF interrupt is generated; therefore, the CPU can receive interrupt notifications.

3.3.19 WFG Interrupt Control Register (WFIR)

WFIR is the register that controls DTIF interrupts and the WFG reload timer.

This register is a special register dedicated to interrupt control. Each register bit is configured so that its state is not affected by writing 0. For this reason, reading before writing to the register is not required. Also, each register bit is configured so that its state is not affected by writing the read value back.

Configuration of Register

bit	15	14	13	12	11	10	9	8
Field	TMIS54	TMIE54	TMIC54	TMIF54	TMIS32	TMIE32	TMIC32	TMIF32
Attribute	W	R/W	W	R	W	R/W	W	R
Initial value	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Field	TMIS10	TMIE10	TMIC10	TMIF10	DTICB	DTIFB	DTICA	DTIFA
Attribute	W	R/W	W	R	W	R	W	R
Initial value	0	0	0	0	0	0	0	0

Functions of Register

[bit0] DTIFA

DTIFA is the bit that detects the event of DTTIX signal input via digital noise-canceller.

Process	Value	Function
Write	-	Writing is invalid.
Read	0	Indicates that DTIFA flag is not set.
	1	Indicates that DTIFA flag is set.

[bit1] DTICA

DTICA is the bit that clears the DTIFA interrupt flag.

Process	Value	Function
Write	0	No effect on operation.
	1	Clears DTIFA register.
Read	-	0 is always read.

[bit2] DTIFB

DTIFB is the bit that detects DTTIX signal input via analog noise filter.

This bit can be used for TYPE3-M4 products and later only.

Process	Value	Function
Write	-	Writing is invalid.
Read	0	Indicates that DTTIX signal via analog noise filter is not detected.
	1	Indicates that that DTTIX signal via analog noise filter is detected.

[bit3] DTICB

DTICB is the bit that clears DTIFB bit.

This bit can be used for TYPE3-M4 products and later only.

Process	Value	Function
Write	0	No effect on operation.
	1	Clears DTIFB register.
Read	-	0 is always read.

[bit4] TMIF10

TMIF10 is the bit that detects the event of WFG10 reload timer interrupt occurrence.

Process	Value	Function
Write	-	Writing is invalid.
Read	0	Indicates that WFG10 reload timer interrupt has not been generated.
	1	Indicates that WFG10 reload timer interrupt has been generated.

[bit5] TMIC10

TMIC10 is the bit that clears TIMF10 bit.

Process	Value	Function
Write	0	No effect on operation..
	1	Clears TMIF10 and deasserts the WFG10 timer interrupt signal.
Read	-	0 is always read.

[bit6] TMIE10

TMIE10 is the bit that starts WFG10 reload timer and checks the operation state of it.

Process	Value	Function
Write	0	No effect on operation..
	1	Starts the WFG10 timer (or does nothing, if it has already been started).
Read	0	Indicates that the WFG10 reload timer is currently stopped.
	1	Indicates that the WFG10 reload timer is currently in operation.

[bit7] TMIS10

TMIS10 is the bit that stops the WFG10 reload timer and clears TMIF10.

Process	Value	Function
Write	0	No effect on operation
	1	Stops the WFG10 reload timer (and also clears an interrupt at the same time, if an interrupt occurs.)
Read	-	0 is always read.

[bit11:8] TMIS32, TMIE32, TMIC32, TMIF32

The TMIS32, TMIE32, TMIC32 and TMIF32 bits control the reload timer for WFG ch.32. The function and use of these bits are the same as TMIS10, TMIE10, TMIC10 and TMIF10.

[bit15:12] TMIS54, TMIE54, TMIC54, TMIF54

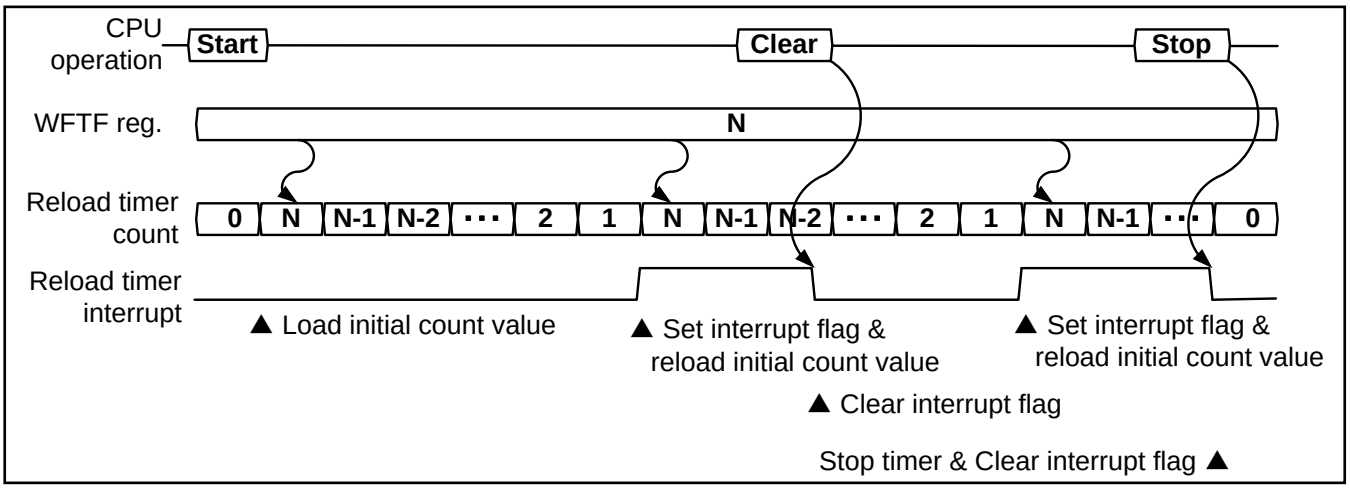
The TMIS54, TMIE54, TMIC54 and TMIF54 bits control the reload timer for WFG ch.54. The function and use of these bits are the same as TMIS10, TMIE10, TMIC10 and TMIF10.

3.3.19.1 Operations of Reload Timer Function

If the WFG pulse counter is not used for waveform generation(WFSA.TMD=000,001,010,100,111), the pulse counter of each channel can be used as an independent reload timer that generates interrupts regularly to the CPU.

Figure 3-6 shows a diagram of the operation when the pulse counter is used as a reload timer.

Figure 3-6 Diagram of Operation when Pulse Counter is Used as Reload Timer



Below is the procedure for using the pulse counter as a reload timer.

- First, set the initial value of the timer to the WFTF register and the clock division ratio to WFSA:DCK . Interval time of the interrupt generated from the timer
  = (WFTF value) × (WFG division ratio (WFSA:DCK)) × PCLK cycle.
- Writing 1 to TMIE starts the timer. The pulse counter loads the initial value from the WFTF register, performs Down-count operation, and generates an interrupt when the count value is set to 1. At the same time, it reloads the initial value from the WFTF register and continues the Down-count operation.
- If 1 is read from TMIE, it indicates that the pulse counter is operating as a reload timer.
- If 1 is read from TMIF, it indicates that an interrupt has occurred.
- Writing 1 to TMIC allows clearing TMIF (clearing an interrupt). Counting continues.
- Writing 1 to TMIS allows clearing TIME (stops the timer) and stops counting. No interrupt will be generated anymore.
- If TMIF has already been set when 1 is written to TMIS, the TMIF is cleared (interrupt is cleared) at the same time.
- The value in the WFTF register can be rewritten while the timer is operating. The changed value is reflected from the next timer reload.
- The following priority order applies to the processing when 1 is written to TMIS, TMIC and TMIE at the same time:
  (Highest priority) Stop the timer > Clear the timer interrupt > Start the timer (Lowest priority)
- Interrupt signal assertion on interrupt flag set can be masked with the use of WIM10, WIM32 and WIM54 bits of the NZCL register.

3.3.20 ICU Connecting FRT Select Register (ICFS)

ICFS is an 8-bit register that selects and sets the FRT to be connected to an ICU.
Each mounted channel has two registers: ICFS10 and ICFS32.
ICFS10 controls ICU ch.1 and ICU ch.0.
ICFS32 controls ICU ch.3 and ICU ch.2.
ICFS10 is located at an even-numbered address, while ICFS32 is located at an odd-numbered address; therefore, their bit positions are [7:0] and [15:8].

Configuration of Register

Bit	15/7	14/6	13/5	12/4	11/3	10/2	9/1	8/0
Field	FSI1[3:0]				FSI0[3:0]			
Attribute	R/W				R/W			
Initial value	0000				0000			

Functions of Register

[bit3:0/11:8] FSI0[3:0]

FSI0[3:0] are the registers that select the FRT to be connected to ICU-ch.(0) for use. Change the setting of these registers while operation of the ICU to be connected to is disabled.

Process	Value	Function
Write	0000	Connects FRT ch.0 to ICU ch.(0).
	0001	Connects FRT ch.1 to ICU ch.(0).
	0010	Connects FRT ch.2 to ICU ch.(0).
	0011 to 1000	For models with multiple MFTs: Connects FRT of an external MFT. For models with one MFT: Setting is prohibited.
	Other than above	Setting is prohibited.
Read	-	Reads the register setting.

[bit7:4/15:12] FSI1[3:0]

FSI1[3:0] are the registers that select the FRT to be connected to ICU-ch.(1) for use. Change the setting of these registers while the operation of the ICU to be connected is disabled.

Process	Value	Function
Write	0000	Connects FRT ch.0 to ICU ch.(1).
	0001	Connects FRT ch.1 to ICU ch.(1).
	0010	Connects FRT ch.2 to ICU ch.(1).
	0011 to 1000	For models with multiple MFTs: Connects FRT of an external MFT. For models with one MFT: Setting is prohibited.
	Other than above	Setting is prohibited.
Read	-	Reads the register setting.

For products with multiple MFTs, the connection to an FRT that exists in different MFT unit can be selected. For related settings, see 4.8 FRT Selection of OCU, ICU, and ADCMP.

3.3.21 ICU Control Register A (ICSA)

ICSA is an 8-bit register that controls ICU operations.
Each mounted channel has two registers: ICSA10 and ICSA32.
ICSA10 controls ICU ch.1 and ICU ch.0.
ICSA32 controls ICU ch.3 and ICU ch.2.I

Configuration of Register

bit	7	6	5	4	3	2	1	0
Field	ICP1	ICP0	ICE1	ICE0	EG1[1:0]		EG0[1:0]	
Attribute	R/W	R/W	R/W	R/W	R/W		R/W	
Initial value	0	0	0	0	00		00	

Functions of Register

[bit1:0] EG0[1:0]

EG0[1:0] are the bit that enable/disable the operation of ICU ch.(0) and select valid edges.

Process	Value	Function
Write	00	Disables the operation of ICU ch.(0). Ignores IC(0) signal input.
	01	Enables the operation of ICU ch.(0). Handles only the rising edge of IC(0) signal input as a valid edge.
	10	Enables the operation of ICU ch.(0). Handles only the falling edge of IC(0) signal input as a valid edge.
	11	Enables the operation of ICU ch.(0). Handles both the rising and falling edges of IC(0) signal input as valid edges.
Read	-	Reads the register setting.

[bit3:2] EG1[1:0]

EG1[1:0] are the bit that enable/disable the operation of ICU ch.(1) and select valid edges.

Process	Value	Function
Write	00	Disables the operation of ICU ch.(1). Ignores IC(1) signal input.
	01	Enables the operation of ICU ch.(1). Handles only the rising edge of IC(1) signal input as a valid edge.
	10	Enables the operation of ICU ch.(1). Handles only the falling edge of IC(1) signal input as a valid edge.
	11	Enables the operation of ICU ch.(1). Handles both the rising and falling edges of IC(1) signal input as valid edges.
Read	-	Reads the register setting.

[bit4] ICE0

ICE0 is the bit that specifies whether to notify the CPU in the event that 1 is set to ICP0 as an interrupt (enabling interrupt) or not to notify it (disabling interrupt).

Process	Value	Function
Write	0	Does not generate interrupt, when 1 is set to ICP0.
	1	Generates interrupt, when 1 is set to ICP0.
Read	-	Reads the register setting.

[bit5] ICE1

ICE1 is the bit that specifies whether to notify the CPU in the event that 1 is set to ICP1 as an interrupt (enabling interrupt) or not to notify it (disabling interrupt).

Process	Value	Function
Write	0	Does not generate an interrupt, when 1 is set to ICP1.
	1	Generates an interrupt, when 1 is set to ICP1.
Read	-	Reads the register setting

[bit6] ICP0

ICP0 is the bit to which 1 is set upon detection of a valid edge/capture operation when the operation of ICU-ch.(0) is enabled.

Process	Value	Function
Write	0	Clears this register to 0.
	1	No effect on operation.
Read	0	Indicates that no valid edge has been detected at ICU ch.(0) and no capture operation has been performed.
	1	Indicates that a valid edge has been detected at ICU ch.(0) and the capture operation has been performed.
Read at RMW access		1 is always read.

[bit7] ICP1

ICP1 is the bit to which 1 is set upon detection of a valid edge/capture operation when the operation of ICU-ch.(1) is enabled.

Process	Value	Function
Write	0	Clears this register to 0.
	1	No effect on operation.
Read	0	Indicates that no valid edge has been detected at ICU ch.(1) and no capture operation has been performed.
	1	Indicates that a valid edge has been detected at ICU ch.(1) and the capture operation has been performed.
Read at RMW access		1 is always read.

The following explanation is shared by ICP0 and ICP1.

By reading from ICP0 and ICP1 registers, it can be determined whether or not a valid edge has been detected and the capture operation has been performed. These registers can be cleared by writing 0. Always write 1 to the register when rewriting to another register in the same address area. These registers do nothing, if 1 is written. 1 is always read from this bit at RMW access. See 4.10 Treatment of Event Detect Register and Interrupt.

3.3.21.1 ICU Operations

If a valid edge is detected in the input signal when an ICU's operation is enabled, it performs a capture operation that captures the FRT's count output in the ICCP register. At the same time, it notifies the CPU via ICP0 and ICP1 that a valid edge has been detected. The valid edge of the input signal can be selected from the rising edge only, the falling edge only, or both rising and falling edges. When the operation is disabled, it does nothing and ignores the input signal.

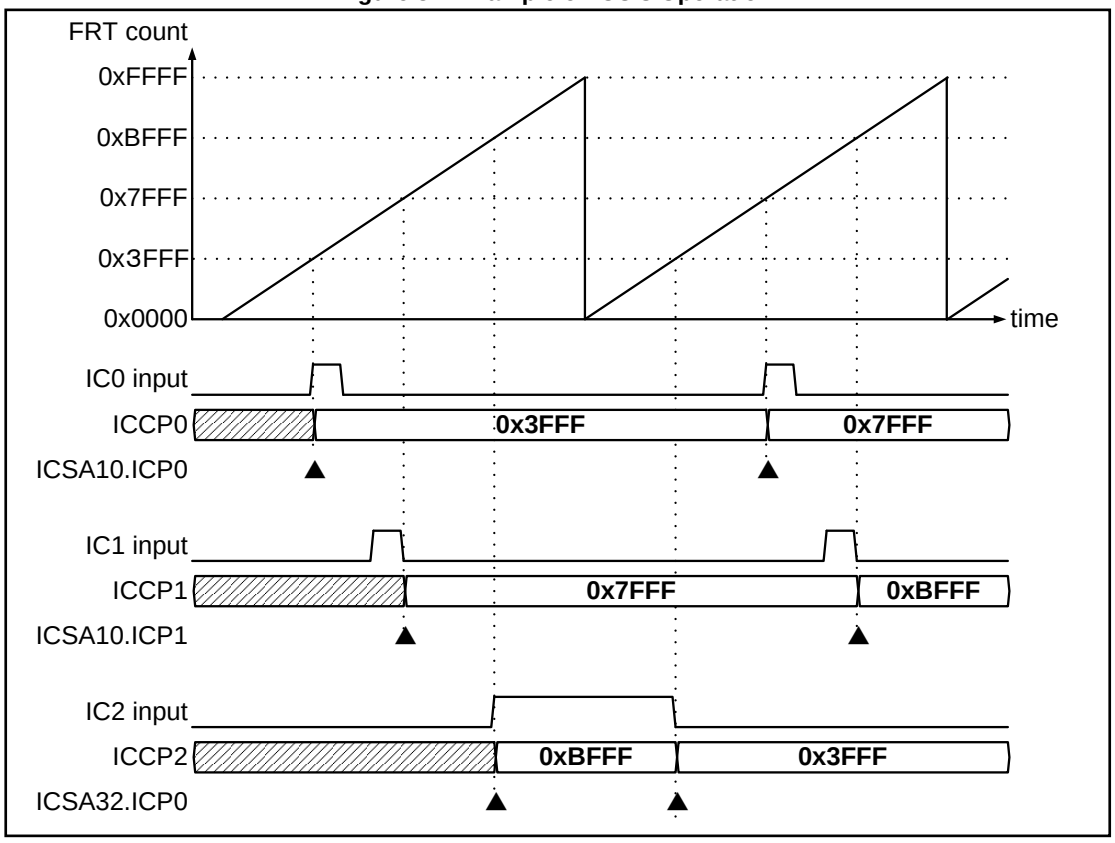
Figure 3-7 shows an example of ICU's operation. "▲" indicates that an event detection register is set.

ICU ch.0 indicates the operation to be performed upon detection of the rising edge of IC0 signal input.

ICU ch.1 indicates the operation to be performed upon detection of the falling edge of IC1 signal input.

ICU ch.2 indicates the operation to be performed upon detection of both the rising and falling edges of IC signal input.

Figure 3-7 Example of ICU's Operation



3.3.22 ICU Control Register B (ICSB)

ICSB is an 8-bit register that reads the operation state of an ICU.
Each mounted channel has two registers: ICSB10 and ICSB32.
ICSB10 reads the operation state of ICU ch.1 and ICU ch.0.
ICSB32 reads the operation state of ICU ch.3 and ICU ch.2.

Configuration of Register

Bit	15	14	13	12	11	10	9	8
Field	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	IEI1	IE10
Attribute	-	-	-	-	-	-	R	R
Initial value	-	-	-	-	-	-	0	0

Functions of Register

[bit8] IEI0

IEI0 is the bit that indicates the latest valid edge of ICU ch.(0).

Process	Value	Function
Write	-	Writing is ignored.
Read	0	Indicates that the latest capture operation of ICU ch.(0) was performed at a falling edge.
	1	Indicates that the latest capture operation of ICU ch.(0) was performed at a rising edge.

[bit9] IEI1

IEI1 is a bit that indicates the latest valid edge of ICU ch.(1).

Process	Value	Function
Write	-	Writing is ignored.
Read	0	Indicates that the latest capture operation of ICU ch.(1) was performed at a falling edge.
	1	Indicates that the latest capture operation of ICU ch.(1) was performed at a rising edge.

The following explanation is shared by IEI0 and IE11.

By reading from IEI0 and IE11 bit, it can be determined at which edge the latest capture operation was performed. As the initial value of this bit is 0, 0 can be read if the capture operation has never been performed. It is also updated every time the valid edge of an input signal is detected. After the capture operation is performed, it is necessary to read from these bits before the next valid edge.

[bit15:10] Reserved

The written value is ignored. Read value is undefined.

3.3.23 ICU Capture Value Store Register (ICCP)

ICCP is a 16-bit register that reads the value captured in an ICU.
Each mounted channel has four registers: ICCP0, ICCP1, ICCP2 and ICCP3.
ICCP0 stores the capture value of ICU ch.0.
ICCP1 stores the capture value of ICU ch.1.
ICCP2 stores the capture value of ICU ch.2.
ICCP3 stores the capture value of ICU ch.3.
It should be noted that this register does not allow for byte access.

Configuration of Register

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Field	ICCP[15:0]															
Attribute	R															
Initial value	0x0000															

Functions of Register

[bit31:16] ICCP[15:0]

ICCP is a 16-bit register that reads the value captured at each channel of an ICU.

Process	Function
Write	Writing is ignored.
Read	Reads the data captured to ICU.

This register is updated every time the valid edge of an input signal is detected. After the capture operation is performed, it is necessary to read from this register before the next valid edge.

3.3.24 ADCMP Connecting FRT Select Register (ACFS)

ACFS is an 8-bit register that selects and sets an FRT to be connected to an ADCMP.
Each mounted channel has three registers: ACFS10, ACFS32 and ACFS54.
ACFS10 controls ADCMP ch.1 and ADCMP ch.0.
ACFS32 controls ADCMP ch.3 and ADCMP ch.2.
ACFS54 controls ADCMP ch.5 and ADCMP ch.4.
The bit positions of ACFS10, ACFS32 and ACFS54 are [7:0], [15:8] and [23:16] respectively.

Configuration of Register

bit	23/15/7	22/14/6	21/13/5	20/12/4	19/11/3	18/10/2	17/9/1	16/8/0
Field	FSA1[3:0]				FSA0[3:0]			
Attribute	R/W				R/W			
Initial value	0000				0000			

Functions of Register

[bit3:0/11:8/19:16] FSA0[3:0]

FSA0[3:0] are used to specify the FRT to be connected to ADCMP ch.(0). Change the setting of these bits, while the operation of the ADCMP to be connected to is disabled.

Process	Value	Function
Write	0000	Connects FRT ch.0 to ADCMP ch.(0).
	0001	Connects FRT ch.1 to ADCMP ch.(0).
	0010	Connects FRT ch.2 to ADCMP ch.(0).
	0011 to 1000	For products with multiple MFTs: Connects FRT of an external MFT. For product with one MFT: Setting is prohibited.
	Other than above	Setting is prohibited.
Read	-	Reads the register setting.

[bit7:4/15:12/23:20] FSA1[3:0]

FSA1[3:0] are used to specify the FRT to be connected to ADCMP ch.(1). Change the setting of these bits while the operation of the ADCMP to be connected to is disabled.

Process	Value	Function
Write	0000	Connects FRT ch.0 to ADCMP ch.(1).
	0001	Connects FRT ch.1 to ADCMP ch.(1).
	0010	Connects FRT ch.2 to ADCMP ch.(1).
	0011 to 1000	For products with multiple MFTs: Connects FRT of an external MFT. For products with one MFT: Setting is prohibited.
	Other than above	Setting is prohibited.
Read	-	Reads the register setting.

For products with multiple MFTs, the connection to an FRT that exists in different MFT unit can be selected. For detailed settings, see 4.8 FRT Selection of OCU, ICU, and ADCMP.

3.3.25 ADCMP Control Register A (ACSA)

ACSA is a 16-bit register that controls ADCMP operations. This register controls compatibility with FM3 Family products. This register controls all of ch.0 to ch.5 of ADCMP. See 4.7 ADCMP FM3 Family Product-compatible Operation for information about compatibility with FM3 Family products.

Configuration of Register

bit	15	14	13 12	11 10	9 8
Field	Reserved	Reserved	SEL54[1:0]	SEL32[1:0]	SEL10[1:0]
Attribute	-	-	R/W	R/W	R/W
Initial value	0	0	00	00	00

bit	7	6	5 4	3 2	1 0
Field	Reserved	Reserved	CE54[1:0]	CE32[1:0]	CE10[1:0]
Attribute	-	-	R/W	R/W	R/W
Initial value	0	0	00	00	00

Functions of Register

[bit1:0] CE10[1:0]

CE10 enables/disables compatibility of ADCMP ch.1 and ch.0 with FM3 Family products.

Process	Value	Function
Write	00	Disables the operations of ADCMP ch.0 and ch.0.
	01	Enables compatible operations of ADCMP ch.1 and ch.0 with FM3 Family products.
	10,11	Setting is prohibited.
Read	-	Reads the register setting.

[bit3:2] CE32[1:0]

CE32 enables/disables compatibility of ADCMP ch.3 and ch.2 with FM3 Family products.

Process	Value	Function
Write	00	Disables the operations of ADCMP ch.3 and ch.2.
	01	Enables compatible operations of ADCMP ch.3 and ch.2 with FM3 Family products.
	10,11	Setting is prohibited.
Read	-	Reads the register setting.

[bit5:4] CE54[1:0]

CE54 enables/disables compatibility of ADCMP ch.5 and ch.4 with FM3 Family products.

Process	Value	Function
Write	00	Disables the operations of ADCMP ch.5 and ch.4.
	01	Enables compatible operations of ADCMP ch.5 and ch.4 with FM3 Family products.
	10,11	Setting is prohibited.
Read	-	Reads the register setting.

[bit7:6] Reserved

0 must be written at write access. Read value is 0.

[bit9:8] SEL10[1:0]

SEL10 register selects compatible operation of ADCMP ch.1 and ch.0 with FM3 Family products.

Process	Function
Write	Selects operation of ADCMP ch.0 and ch.1 . See 4.7 ADCMP FM3 Family Product-compatible Operation.
Read	Reads the register setting.

[bit11:10] SEL32[1:0]

SEL32 register selects compatible operation of ADCMP ch.3 and ch.2 with FM3 Family products.

Process	Function
Write	Selects operation of ADCMP ch.3 and ch.2. See 4.7 ADCMP FM3 Family Product-compatible Operation.
Read	Reads the register setting.

[bit13:12] SEL54[1:0]

SEL54 register selects compatible operation of ADCMP ch.5 and ch.4 with FM3 Family products.

Process	Function
Write	Selects operation of ADCMP ch.5 and ch.4. See 4.7 ADCMP FM3 Family Product-compatible Operation.
Read	Reads the register setting.

[bit15:14] Reserved

0 must be written upon write access. Read value is 0.

3.3.26 ADCMP Control Register C (ACSC)

ACSC is an 8-bit register that controls ADCMP operations. Each mounted channel has six registers: ACSC0 to ACSC5.
ACSC0 controls ADCMP ch.0.
ACSC1 controls ADCMP ch.1.
ACSC2 controls ADCMP ch.2.
ACSC3 controls ADCMP ch.3.
ACSC4 controls ADCMP ch.4.
ACSC5 controls ADCMP ch.5.

Configuration of Register

bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	APBM	ADSEL[2:0]			BUFE[1:0]	
Attribute	R	R	R/W	R/W			R/W	
Initial value	0	0	0	000			00	

Functions of Register

[bit1:0] BUFE[1:0] and [bit5] APBM

BUFE[1:0] makes the buffer function settings for the ACMP register and ACMC register. It allows the buffer function to be enabled/disabled and the transfer timing to be selected. APBM sets the linked transfer with the FRT interrupt mask counter.
APBM can be used for TYPE3-M4 products and later only. TYPE1-M4 and TYPE2-M4 products are handled as APBM=0.
Change the setting of these bits when the operation of ADCMP is disabled.

Process	Value		Function	
	APBM	BUFE	Buffer Function	Transfer Timing
Write	0	00	Disabled	Always when writing to ACMP and ACMC from CPU
	0	01	Enabled	When connected FRT is Zero/Bottom status
	0	10		When connected FRT is Peak/Top status
	0	11		When connected FRT is Zero/Bottom status or Peak/Top status
	1	00	Disabled	Always when writing to ACMP and ACMC from CPU
	1	01	Enabled	When connected FRT is Zero/Bottom status, and MSZC=0000
	1	10		When connected FRT is Peak/Pop status, and MSPC=0000
	1	11		Condition A : connected FRT is Zero/Bottom status. Condition B :connected FRT is MSZC=0000. Condition C: connected FRT is Peak/Top status Condition D: connected FRT is MSPC=0000. When (Condition A and Condition B) or (Condition C and Condition D)
Read	-	-	Reads the register setting.	

If the buffer function setting is changed from disabled to enabled by the ACSC register, when the ACSC register and ACMC register are overwritten simultaneously using 32-bit access (word access), the value written to the ACMC register at that time becomes buffer function enabled after it is transferred to the ACMC register.

[bit4:2] ADCSEL

ADCSEL bits specify the destinations of ADC start signals that are output by ADCMP. Change the setting of these bits when operation of ADCMP is disabled. ACSC.ADSEL value of multiple channels can be selected to the same destination. In this case, multiple ADC start time can be set for the same ADC.

Process	Value	Function
Write	000	Outputs ADC start trigger 0.
	001	Outputs ADC start trigger 1.
	010	Outputs ADC start trigger 2.
	011	Outputs ADC start trigger 3.
	100	Outputs ADC start trigger 4.
	101	Outputs ADC start trigger 5.
	110	Outputs ADC start trigger 6.
	111	Outputs ADC start trigger 7.
Read	-	Reads the register setting.

[bit7:5] Reserved

0 must be written upon write access. Read value is 0.

3.3.27 ADCMP Control Register D (ACSD)

ACSD is an 8-bit register that controls ADCMP operations.
Each mounted channel has six registers: ACSD0 to ACSD5.
ACSD0 controls ADCMP ch.0.
ACSD1 controls ADCMP ch.1.
ACSD2 controls ADCMP ch.2.
ACSD3 controls ADCMP ch.3.
ACSD4 controls ADCMP ch.4.
ACSD5 controls ADCMP ch.5.

Configuration of Register

bit	15	14	13	12	11	10	9	8
field	ZE	UE	PE	DE	Reserved	Reserved	OCUS	AMOD
Attribute	R/W	R/W	R/W	R/W	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Functions of Register

[bit8] AMOD

AMOD selects operation mode for ADCMP.

Process	Value	Function
Write	0	Starts ADCMP in normal mode.
	1	Starts ADCMP in offset mode.
Read	-	Reads the register setting.

In normal mode, when a match is detected between the ACMP register and the FRT, an ADC start signal is output.

In offset mode, when a match is detected between the selected OCCP and the FRT, the ACMP value is loaded into the offset start down counter. After the offset start down counter finishes the counting specified by ACMP, an ADC start signal is output. The offset time from the match detection for OCCP to ADC start is as follows:

Offset time = ACMP value×Free-run timer clock cycle

[bit9] OCUS

OCUS selects the OCU OCCP register that will become the start for offset start. When AMOD=0 is specified, the value of this register means nothing.

Process	Value	Function
Write	0	Selects OCCP(0).
	1	Selects OCCP(1).
Read	-	Reads the register setting.

Which OCCP will be selected by OCUS value depends on the ADCMP channel number. See 4.6 Description of ADCMP Operation.

[bit11:10] Reserved

00 must be written upon write access. Read value is 00.

[bit12] DE

This bit is used to select ADCMP operation allow or prohibit when the FRT connected to ADCMP is Down status.

Process	Value	Function
Write	0	Prohibits ADCMP operation when the FRT connected to ADCMP is Down status.
	1	Allows ADCMP operation when the FRT connected to ADCMP is Down status. When AMOD=0, the ADC start signal is output when ACMP=FRT and the ACMC matches. When AMOD=1, the offset down-counter is started when OCCP=FRT and the ACMC matches.
Read	-	Reads the register setting.

[bit13] PE

This bit is used to select ADCMP operation allow or prohibit when the FRT connected to ADCMP is Peak/Top status.

Process	Value	Function
Write	0	Prohibits ADCMP operation when the FRT connected to ADCMP is Peak/Top status.
	1	Allows ADCMP operation when the FRT connected to ADCMP is Peak/Top status. When AMOD=0, the ADC start signal is output when ACMP=FRT and the ACMC matches. When AMOD=1, the offset down-counter is started when OCCP=FRT and the ACMC matches.
Read	-	Reads the register setting.

[bit14] UE

This bit is used to select ADCMP operation allow or prohibit when the FRT connected to ADCMP is Up status.

Process	Value	Function
Write	0	Prohibits ADCMP operation when the FRT connected to ADCMP is Up status.
	1	Allows ADCMP operation when the FRT connected to ADCMP is Up status. When AMOD=0, the ADC start signal is output when ACMP=FRT and the ACMC matches. When AMOD=1, the offset down-counter is started when OCCP=FRT and the ACMC matches.
Read	-	Reads the register setting.

[bit15] ZE

This bit is used to select ADCMP operation allow or prohibit when the FRT connected to ADCMP is Zero/Bottom status.

Process	Value	Function
Write	0	Prohibits ADCMP operation when the FRT connected to ADCMP is Zero/Bottom status.
	1	Allows ADCMP operation when the FRT connected to ADCMP is Zero/Bottom status. When AMOD=0, the ADC start signal is output when ACMP=FRT and ACMC matches. When AMOD=1, the offset down-counter is started when OCCP=FRT and ACMC matches.
Read	-	Reads the register setting.

Writing 1 to either DE, PE, UE or ZE enables the operation of ADCMP.

When either the ACSD0 register or the ACSD1 register is used to enable operation of ADCMP-ch.0 or ch.1, setting ACSA.CE10=1 is prohibited.

When either the ACSD2 register or the ACSD3 register is used to enable operation of ADCMP-ch.2 or ch.3, setting ACSA.CE32=1 is prohibited.

When either the ACSD4 register or the ACSD5 register is used to enable operation of ADCMP-ch.4 or ch.5, setting ACSA.CE54=1 is prohibited.

3.3.28 ADCMP Compare Value Store Register (ACMP)

ACMP is a 16-bit register that uses ADCMP to specify an AD conversion start time as a compare value for a FRT count value or an offset value after match detection by an OCU.
Each mounted channel has six registers: ACMP0 to 5.
ACMP0 stores ADCMP ch.0 compare and offset values.
ACMP1 stores ADCMP ch.1 compare and offset values.
ACMP2 stores ADCMP ch.2 compare and offset values.
ACMP3 stores ADCMP ch.3 compare and offset values.
ACMP4 stores ADCMP ch.4 compare and offset values.
ACMP5 stores ADCMP ch.5 compare and offset values.
It should be noted that this register does not allow for byte access.

Configuration of Register

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
field	ACMP[15:0]															
Attribute	R/W															
Initial value	0x0000															

Functions of Register

The ACMP register is used to specify an AD conversion start time (FRT compare value or offset value). When data is written to this address area, the data is first stored in the buffer register. And then, the data is transferred from the buffer register to the ACMP register under the following conditions.

- When the buffer function is disabled (ACSC.BUFE=00), data is transferred immediately after it is written to the buffer register.
- When the buffer function is enabled (ACSC.BUFE≠00), FRT counting is stopped (TCSA.STOP=1) or at a specified time, data is transferred.

When FRT is counting, the AD conversion start time can be changed by rewriting to this register. When the buffer function is disabled, the written value can be immediately reflected in the ACMP register. When the buffer function is enabled, the ACMP register settings for multiple channels can be synchronized.

When data is read from the address area, values are read from the ACMP register, not from the buffer register. This results in reading the previous value until the end of the transfer when the buffer function is enabled. Bit rewriting with RMW access to this area is not allowed.

[bit31:16] ACMP[15:0]

Process	Function
Write	Specifies the AD conversion start time (FRT compare value or offset value). The value is written to ACMP buffer register.
Read	Reads ACMP register value (not ACMP buffer register value).

3.3.29 ADCMP Mask Compare Value Storage Register (ACMC)

The ACMC is an 8-bit register that specifies the timing at which AD conversion is started by ADCMP as the value to be compared with the FRT interrupt mask counter.

ACMC0 stores the ADCMP ch.0 compare and offset values.
ACMC1 stores the ADCMP ch.1 compare and offset values.
ACMC2 stores the ADCMP ch.2 compare and offset values.
ACMC3 stores the ADCMP ch.3 compare and offset values.
ACMC4 stores the ADCMP ch.4 compare and offset values.
ACMC5 stores the ADCMP ch.5 compare and offset values.

Note:

- *This register is included in TYPE3-M4 products and later only.*

Configuration of Register

bit	23	22	21	20	19	18	17	16
field	MPCE	MZCE	Reserved	Reserved	AMC[3:0]			
Attribute	R/W	R/W	-	-	R/W			
Initial value	0	0	-	-	0000			

Functions of Register

The ACMC register is used to specify the AD conversion start time as the value to be compared with the FRT interrupt mask counter. AD conversion can be started at the timing when the FRT interrupt mask counter matches the compare value.

When data is written to this address area, the data for each bit is first stored in the buffer register. Then, the data is transferred from the buffer register to the respective bits of the ACMC register under the conditions below.

- When buffer function is disabled (ACSC.BUFE=00)
  Data is transferred immediately after is written to the buffer register.
- When buffer function is enabled (ACSC.BUFE≠00)
  Data is transferred when FRT counting is stopped (TCSA.STOP=1) or at the specified transfer timing.

During the FRT count operation, the AD conversion start time can be changed by overwriting the bits of this register. When the buffer function is disabled, the written value can be immediately applied to the ACMC register. When the buffer function is enabled, ACMC register settings for multiple channels can be synchronized.

When data is read out from the address area, values are read from the ACMC register, not the buffer register. This results in reading the previous value until the end of the transfer when the buffer function is enabled. Also, bit overwriting by RMW access to this address area is not allowed.

[bit19:16] AMC[3:0]

This bit specifies the value to be compared with the FRT interrupt mask counter.

Process	Function
Write	Specifies the AD conversion start time by the value to be compared with the FRT interrupt mask counter. The value is written to the buffer register.
Read	Reads the AMC register value (not the AMC buffer register value).

[bit21:20] Reserved

00 must be written upon write access. Read value is 00.

[bit22] MZCE

This bit specifies whether a comparison is performed with the FRT zero interrupt mask counter.

Process	Value	Function
Write	0	Comparison is not performed with the FRT zero interrupt mask counter. The value is written to the buffer register.
	1	Comparison is performed with the FRT zero interrupt mask counter. The value is written to the buffer register.
Read	-	Reads the MZCE register value (not the MZCE buffer register value).

[bit23] MPCE

This bit specifies whether a comparison is performed with the FRT peak interrupt mask counter.

Process	Value	Function
Write	0	Comparison is not performed with the FRT peak interrupt mask counter. The value is written to the buffer register.
	1	Comparison is performed with the FRT peak interrupt mask counter. The value is written to the buffer register.
Read	-	Reads the MZCE register value (not the MZCE buffer register value).

The ACMC match determination described below is performed based on the specified settings for the MZCE and MPCE registers above and the comparison results between AMC[3:0] and the connected FRT interrupt mask counter. Processing is performed by ADCMP based on these determination results.

・When MPCE=0 and MZCE=0, this is determined to be an ACMC match regardless of the AMC[3:0] value and connected FRT mask counter value.

・When MPCE=0 and MZCE=1, this is determined to be an ACMC match when the AMC[3:0] value matches the connected FRT zero interrupt mask counter value (MSZC[3:0]).

・When MPCE=1 and MZCE=0, this is determined to be an ACMC match when the AMC[3:0] value matches the connected FRT peak interrupt mask counter value (MSPC[3:0]).

・When MPCE=1 and MZCE=1, this is determined to be an ACMC match when the AMC[3:0] value matches the connected FRT zero interrupt mask counter value or the peak interrupt mask counter value.

The above information is shown in Table 3-14. The X in the table indicates that the condition is ignored. In TYPE1-M4 and TYPE2-M4 products, this is treated as MPCE=MZCE=0.

Table 3-14 ACMC Match Determination Results

MPCE	MZCE	Comparison Result of AMC[3:0] and MSPC[3:0]	Comparison Result of AMC[3:0] and MSZC[3:0]	ACMC Match Determination Result
0	0	X	X	Match
0	1	X	Match	Match
		X	Mismatch	Mismatch
1	0	Match	X	Match
		Mismatch	X	Mismatch
1	1	Match	X	Match
		X	Match	Match
		Mismatch	Mismatch	Mismatch

As shown above, by specifying the ACMC register, the ADC start signal output/offset down-counter can be started only when the FRT interrupt mask counter value matches the specified value. When MPCE=MZCE=0, processing can be performed regardless of the FRT interrupt mask counter value.

See the sections on ZE, UE, PE, and DE in ADC Start Linked with FRT Interrupt Mask Counter and 3.3.7 OCU Connecting FRT Select Register (OCFS).

If the FRT where the connection is selected by ADCMP is count mode with offset (ch.1 or ch.2), the FRT interrupt mask counter value is connected to the ch.0 interrupt mask counter value which is operating simultaneously. As a result, even if the FRT of count mode with offset is connected, it is possible to perform AD start linked to the interrupt mask counter.

The register settings have the restrictions below, and so careful attention is needed.

- When ACMC.MZCE=1 is set, the ACSD.ZE=1 setting is not allowed.
- When ACMC.MPCE=1 is set, the ACSD.PE=1 setting is not allowed.

Notes:

- *This register function is available in TYPE-M4 products or later only. In TYPE1-M4 and TYPE2-M4 products, operation is identical to operation when the MPCE=MZCE=0 value was set, and this is treated as a constant ACMC match.*
- *In TYPE1-M4 and TYPE2-M4 products, be aware that all of the values are read as "1" when reading the address area of this register.*
- *This register function can be used when an ACSD register is used to output the ADC start signal. Be aware that it cannot be used for FM3 compatible start using the ACSA register.*

4. Operations of the Multifunction Timer

This section describes details of the operations of the multifunction timer.

4.1. Descriptions of FRT Operation
4.2. Description of OCU Operation
4.3. OCU FM3 Family Product-compatible Operation
4.4. Description of WFG Operation
4.5. WFG FM3 Family Product-compatible Operation
4.6. Description of ADCMP Operation
4.7. ADCMP FM3 Family Product-compatible Operation
4.8. FRT Selection of OCU, ICU, and ADCMP
4.9. PPG Timer Unit Connected to WFG
4.10. Treatment of Event Detect Register and Interrupt

4.1 Descriptions of FRT Operation

FRT operation is described below.

4.1.1 FRT Control Register

The FRT control registers are shown in Table 4-1. An overview of the register functions and setting timing are also provided in this table.

The initial basic settings of the FRT (setting clock frequency division ratio, selecting count mode) are performed while the FRT count operation is stopped. After the initial settings are completed, the count operation is started (TCSA.STOP=0).

The FRT count value and count state are input to the OCU, ICU, and ADCMP connected to the FRT. Each block can perform synchronized output signal changes, buffer transfer operations, and similar operations based on this input.

When the FRT counter counts to 0x0000, the Zero value detection register (TCSA.IRQZF) is set. When the peak value (=TCCP) is counted, the peak value detection register (TCSA.ICLR) is set. These event detection registers can be used to generate interrupts to the CPU. The number of times that the zero detection and peak detection registers are set can be reduced by a fixed count ratio using the interrupt mask counter.

The TCAL register can be used to enable simultaneous count start, stop, and initialization of multiple FRTs.

Table 4-1 FRT Control Register

Setting Register	Register Function	Register Change Timing
TCSA.STOP TCAL.STOP	Starts/stops count operation	Any user-selected timing after the initial settings are completed
TCSA.SCLR TCAL.SCLR	Initializes counter value	
TCSA.CLK	Sets clock frequency division ratio	Set while the count operation is stopped Changing of the settings is prohibited after the count operation is started
TCSA.BFE	Selects TCCP register buffer function	
TCSA.MODE	Selects count mode	
TCSD.OFMD1/2 (TYPE3-M4 products and later)	Selects count mode with offset	
TCSA.ECKE	Selects external clock	
TCSC.MSZI TCSC.MSPI	Sets initial value of interrupt mask counter	Any user-selected timing
TCSC.MSZC TCSC.MSPC	Reads interrupt mask counter value	
TCSA.ICLR TCSA.IRQZF	Reads and clears match detection register	
TCSA:ICLRE TCSA.IRQZE	Allows/prohibits interrupt	
TCCP	Specifies peak value/offset value	Buffer function enabled: Any user-selected timing Buffer function disabled: Pay careful attention to the timing when the settings are changed

4.1.2 FRT Count Operation

4.1.2.1 Count Mode Selection

Table 4-2, Table 4-3, and Table 4-4 show the selection conditions for the count mode of each FRT channel, selected count modes, and the relationship of the control registers in that case.

Table 4-2 Selection of FRT-ch.0 Count Mode

Operation Mode Selection Condition	FRT-ch.0 Count Mode	Control Register
TCSA0.MODE=0	Normal up-count	TCSA0: Basic control TCSC0: Interrupt mask counter TCCP0: Peak value (count cycle) setting TCDT0: Readout of current ch.0 counter value
TCSA0.MODE=1	Normal up/down-count	

Table 4-3 Selection of FRT-ch.1 Count Mode

Operation Mode Selection Condition	FRT-ch.1 Operation Mode	Register where Control is Performed
TCSD.OFMD1=0 TCSA1.MODE=0	Normal up-count	TCSA1: Basic control TCSC1: Interrupt mask counter TCCP1: Peak value (count cycle) setting TCDT1: Readout of current ch.1 counter value
TCSD.OFMD1=0 TCSA1.MODE=1	Normal up/down-count	
TCSD.OFMD1=1 TCSA0.MODE=0	Up-count with offset	TCSA0: Basic control (ch.0 and ch.1 are controlled simultaneously) TCSA1: Not used for control TCSC0: Interrupt mask counter TCSC1: Not used for control TCCP0: Peak value (count cycle) setting TCCP1: Offset value setting TCDT0: Readout of current ch.0 counter value TCDT1: Readout of current ch.1 counter value
TCSD.OFMD1=1 TCSA0.MODE=1	Up/down-count with offset	

Table 4-4 Selection of FRT-ch.2 Count Mode

Operation Mode Selection Condition	FRT-ch.2 Operation Mode	Register where Control is Performed
TCSD.OFMD2=0 TCSA2.MODE=0	Normal up-count	TCSA2: Basic control TCSC2: Interrupt mask counter TCCP2: Peak value (count cycle) setting TCDT2: Readout of current counter value
TCSD.OFMD2=0 TCSA2.MODE=1	Normal up/down-count	
TCSD.OFMD2=1 TCSA0.MODE=0	Up-count with offset	TCSA0: Basic control (ch.0 and ch.2 are controlled simultaneously) TCSA2: Not used for control TCSC0: Interrupt mask counter TCSC2: Not used for control TCCP0: Peak value (count cycle) setting TCCP2: Offset value setting TCDT0: Readout of current ch.0 counter value TCDT2: Readout of current ch.2 counter value
TCSD.OFMD2=1 TCSA0.MODE=1	Up/down-count with offset	

For ch.0, either normal up-count mode or normal up/down-count mode can be selected. Count mode with offset cannot be selected.

For ch.1 and ch.2, one of normal up-count mode, normal up/down-count mode, up-count mode with offset, and up/down-count mode with offset can be selected.

For ch.0, ch.1, and ch.2, if normal count mode is selected, there is no effect on the count operation of other FRT channels. This channel can be used as an FRT independently from other channels. FRT counter operation control uses the TCSA, TCSC, TCCP, and TCDT registers to perform control separately.

If count mode with offset is selected (TCSD.OFMD1=1) for ch.1, ch.1 performs the count operation in subordination to ch.0. If ch.0 is set to normal up-count mode (TCSA0.MODE=0), ch.1 is set to up-count mode with offset. If ch.0 is set to normal up/down-count mode (TCSA0.MODE=1), ch.1 is up/down-count mode with offset. The TCSA0 register and TCSC0 register settings are enabled for both the ch.0 and ch.1 counters, and count operation control is performed simultaneously. The TCSA1 register and TCSC1 register are not used. The peak value is specified by the TCCP0 register. The offset value is set by the TCCP1 register. The ch.0 counter value can be read out by the TCDT0 register, and the ch.1 counter value can be read out by the TCDT1 register.

If count mode with offset is selected (TCSD.OFMD2=1) for ch.2, ch.2 performs the count operation in subordination to ch.0. If ch.0 is set to normal up-count mode (TCSA0.MODE=0), ch.2 is set to up-count mode with offset. If ch.0 is set to normal up/down-count mode (TCSA0.MODE=1), ch.2 is up/down-count mode with offset. The TCSA0 register and TCSC0 register settings are enabled for both the ch.0 and ch.2 counters, and count operation control is performed simultaneously. The TCSA2 register and TCSC2 register are not used. The peak value is specified by the TCCP0 register. The offset value is set by the TCCP2 register. The ch.0 counter value can be read out by the TCDT0 register, and the ch.2 counter value can be read out by the TCDT2 register.

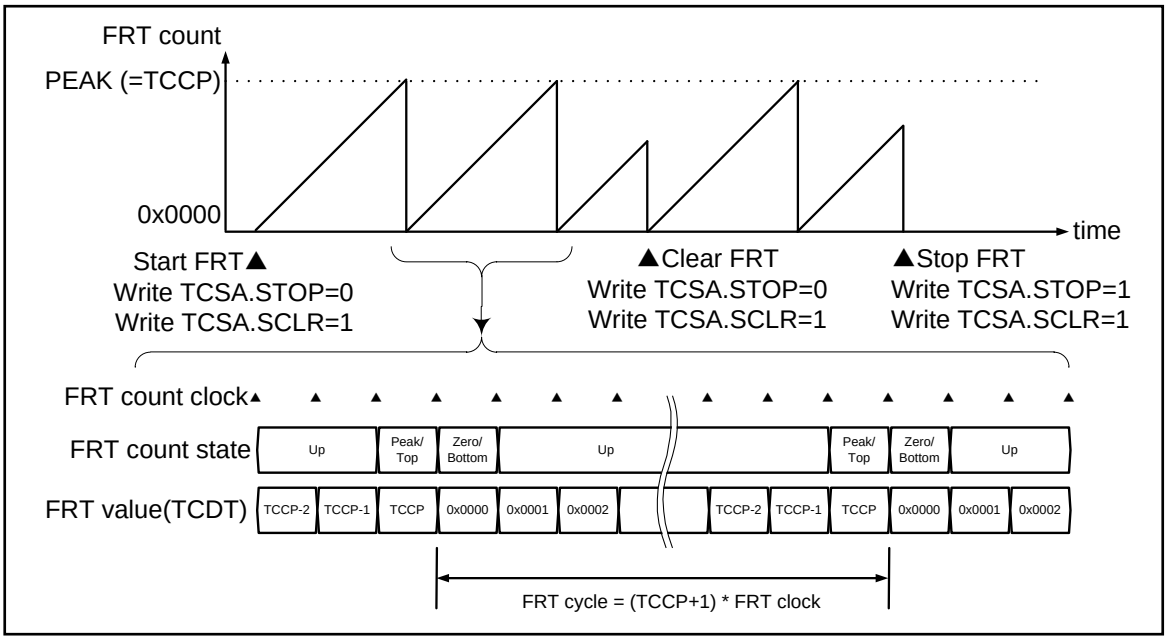
Both ch.1 and ch.2 can be set to count mode with offset by setting TCSD.OFMD1=1 and TCSD.OFMD2=1. The TCSA0 register and TCSC0 register are used to perform count operation control simultaneously for ch.0, ch.1, and ch.2. In this case, the TCSA1 and TCSA2 registers and the TCSC1 and TCSC2 registers are not used. The peak value is specified by the TCCP0 register. The ch.1 offset value can be specified by the TCCP1 register, and the ch.2 offset value can be specified by the TCCP2 register. The ch.0, ch.1, and ch.2 counter values can be read out by the TCDT0, TCDT1, TCDT2 registers, respectively.

Count mode with offset can be selected in TYPE3-M4 products and later. Normal count mode only can be selected in TYPE1-M4 and TYPE2-M4 products.

4.1.2.2 Normal Up-count Mode Operation (ch.0,1,2)

The descriptions in this section apply to ch.0, ch.1, and ch.2. If the common notation omits the channel number of the register name, simply insert the applicable channel number when reading. Figure 4-1 shows the FRT count operation when normal up-count mode is selected.

Figure 4-1 FRT Operation in Normal Up-count Mode



The count mode operation and control procedure are described below.

Normal up-count mode is selected.

- For ch.0, TCSA0.MODE=0 is specified.
- For ch.1, TCSA1.MODE=0 and TCSD.OFMD1=0 are specified.
- For ch.2, TCSA2.MODE=0 and TCSD.OFMD2=0 are specified.

The FRT peak value is set to TCCP.

Writing of TCSA.STOP=0 and TCSA.SCLR=1 is performed. The FRT counter value (=TCDT) is initialized to 0x0000, and the count operation is started.

The FRT counter value starts increment counting from 0x0000. After increment counting to the peak value (=TCCP register setting value), the value returns to 0x0000. Then, this count operation is repeated. The FRT count cycle is (TCCP+1) × count clock cycle.

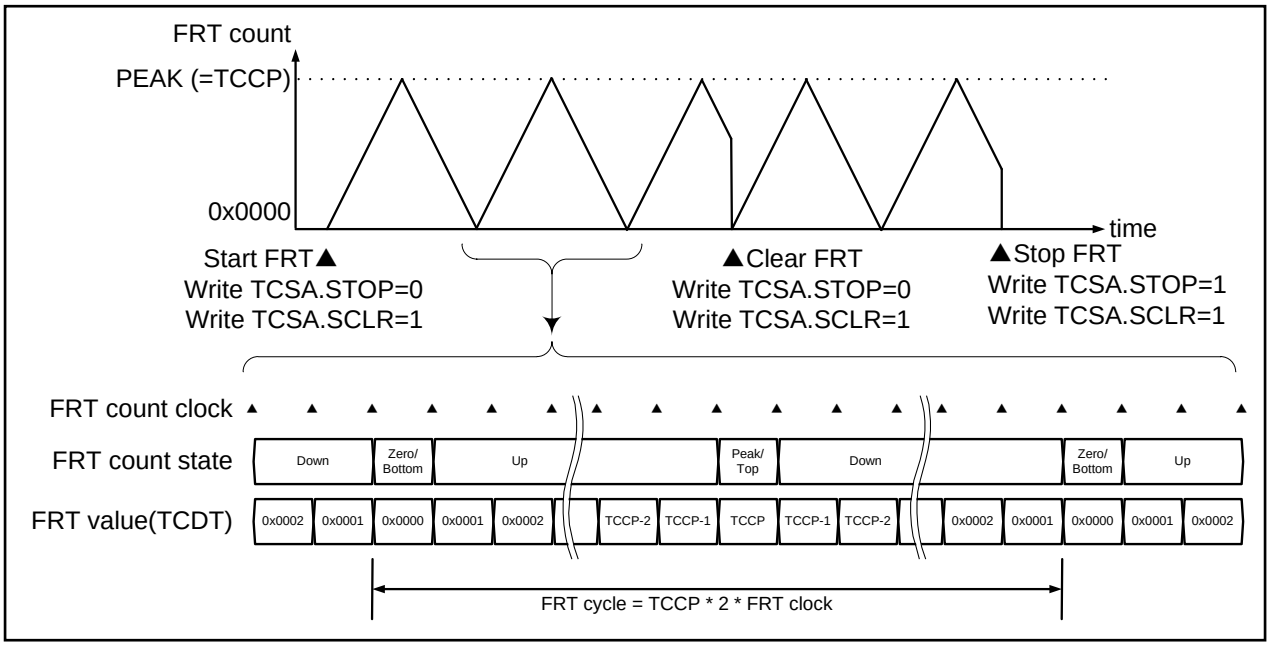
During a count operation, writing of TCSA.STOP=0 and TCSA.SCLR=1 can be performed to initialize the counter value to 0x0000 and to continue the subsequent count operation.

Writing of TCSA.STOP=1 and TCSA.SCLR=1 can be performed to initialize the counter value to 0x0000 and stop the count operation.

4.1.2.3 Normal Up/Down-count Mode Operation (ch.0,1,2)

The descriptions in this section apply to ch.0, ch.1, and ch.2. If the common notation omits the channel number of the register name, simply insert the applicable channel number when reading. Figure 4-2 shows the FRT count operation when normal up/down-count mode is selected.

Figure 4-2 FRT Operation in Normal Up/Down-count Mode (ch.0, ch.1, ch.2)



The count mode operation and control procedure are described below.

Normal up/down-count mode is selected.

- For ch.0, TCSA0.MODE=1 is specified.
- For ch.1, TCSA1.MODE=1 and TCSD.OFMD1=0 are specified.
- For ch.2, TCSA2.MODE=1 and TCSD.OFMD2=0 are specified.

The FRT peak value is set to TCCP.

Writing of TCSA.STOP=0 and TCSA.SCLR=1 is performed. The FRT counter value (=TCDT) is initialized to 0x0000, and the count operation is started.

The FRT counter value (=TCDT) starts counting from 0x0000. Increment counting is performed until the peak value (=TCCP register setting value). Then, decrement counting is performed until 0x0000. Following this, the count operation is repeated. The FRT count cycle is (TCCP) × 2 × count clock cycle.

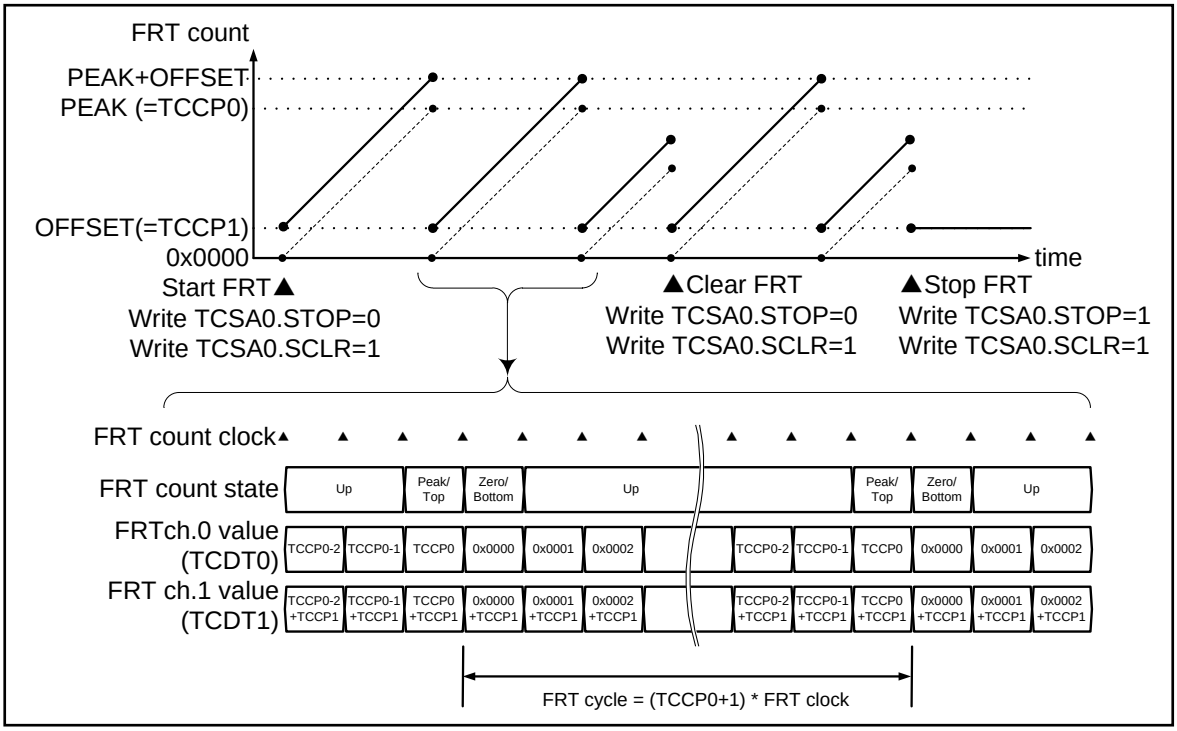
During a count operation, writing of TCSA.STOP=0 and TCSA.SCLR=1 can be performed to initialize the counter value to 0x0000 and to continue the subsequent count operation. After initialization, the count is restarted in the up direction.

Writing of TCSA.STOP=1 and TCSA.SCLR=1 clears the counter value to 0x0000 and stops the count.

4.1.2.4 Offset Up-count Mode Operation (ch.1)

This section describes ch.1. The FRT count operation for ch.1 up/down-count mode with offset is shown in Figure 4-3. The solid lines in the figure indicate ch.1 count operations, and the dashed lines indicate ch.0 count operations. To make the figure easier to read, the peak of ch.0 was changed to zero, and the change from the ch.1 peak+offset to the offset is not connected by a line.

Figure 4-3 FRT Operation in Up-count Mode with Offset (ch.1)



The count mode operation and control procedure are described below.

FRT-ch.0 is set to normal up-count mode, and FRT-ch.1 is set to up-count mode with offset. (TCSA0.MODE=0 and TCSD.OFMD1=1)

The ch.0 peak value is set to TCCP0, and the ch.1 offset value is set to TCCP1.

Writing of TCSA0.STOP=0 and TCSA0.SCLR=1 is performed. The FRT-ch.0 counter value (=TCDT0) is initialized to 0x0000, and the FRT-ch.1 counter value (=TCDT1) is initialized to the offset value (=TCCP1). The count operation is started simultaneously for ch.0 and ch.1.

Operation is performed in the above-described normal up-count mode for the ch.0 counter value. Counting is started from the offset value (=TCCP1) for the ch.1 counter value and then incremented to the peak + offset value (=TCCP0+TCCP1). Then, the value decrements to the offset value (=TCCP1). Following this, the count operation is repeated. The FRT count cycle is (TCCP0+1) × count clock cycle for both ch.0 and ch.1.

During a count operation, writing of TCSA0.STOP=0 and TCSA0.SCLR=1 can be performed to simultaneously initialize the ch.0 count value to 0x0000 and initialize the ch.1 count value to the offset value (=TCCP1) and to continue the subsequent count operation.

Writing of TCSA0.STOP=1 and TCSA0.SCLR=1 can be performed to simultaneously initialize the ch.0 counter value to 0x0000 and initialize the ch.1 counter value to the offset value (=TCCP1) and stop the count operation.

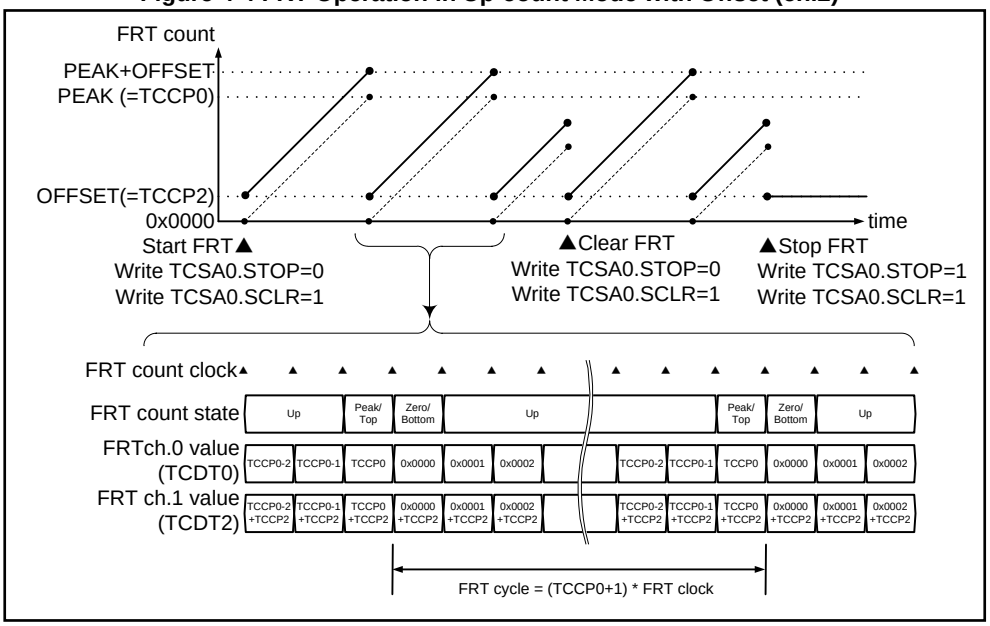
After count mode with offset is selected, when counting is started the first time, be sure to always write TCSA0.SCLR=1 for the first time. Writing this value initializes the counter values for both ch.0 and ch.1.

When TCSD.OFMD1=1, the ch.1 control registers (TCSA1 and TCSC1) are not used. Both ch.0 and ch.1 are controlled simultaneously by the ch.0 control registers (TCSA0 and TCSC0).

4.1.2.5 Offset Up-count Mode Operation (ch.2)

This section describes FRT-ch.2. The FRT count operation for FRT-ch.2 up-count mode with offset is shown in Figure 4-4. The solid lines in the figure indicate ch.2 count operations, and the dashed lines indicate ch.0 count operations. To make the figure easier to read, the peak of ch.0 was changed to zero, and the change from the ch.2 peak+offset to the offset is not connected by a line.

Figure 4-4 FRT Operation in Up-count Mode with Offset (ch.2)



If up-count mode with offset is selected in ch.2, the count operation is identical to ch.1 up-count mode with offset. The count mode operation and control procedure are described below.

FRT-ch.0 is set to normal up-count mode, and FRT-ch.2 is set to up-count mode with offset. (TCSA0.MODE=0 and TCSD.OFMD2=1)

The ch.0 peak value is set to TCCP0, and the ch.2 offset value is set to TCCP2.

Writing of TCSA0.STOP=0 and TCSA0.SCLR=1 is performed. The FRT-ch.0 counter value (=TCDT0) is initialized to 0x0000, and the FRT-ch.2 counter value (=TCDT2) is initialized to the offset value (=TCCP2). The count operation is started simultaneously for ch.0 and ch.2.

Operation is performed in the above-described normal up-count mode for the ch.0 counter value. Counting is started from the offset value (=TCCP2) for the ch.2 counter value and then incremented to the peak + offset value (=TCCP0+TCCP2). Then, the value decrements to the offset value (=TCCP2). Following this, the count operation is repeated. The FRT count cycle is (TCCP0+1) × count clock cycle for both ch.0 and ch.2.

During a count operation, writing of TCSA0.STOP=0 and TCSA0.SCLR=1 can be performed to simultaneously initialize the ch.0 count value to 0x0000 and initialize the ch.2 count value to the offset value (=TCCP2) and to continue the subsequent count operation.

Writing of TCSA0.STOP=1 and TCSA0.SCLR=1 can be performed to simultaneously initialize the ch.0 counter value to 0x0000 and initialize the ch.2 counter value to the offset value (=TCCP2) and stop the count operation.

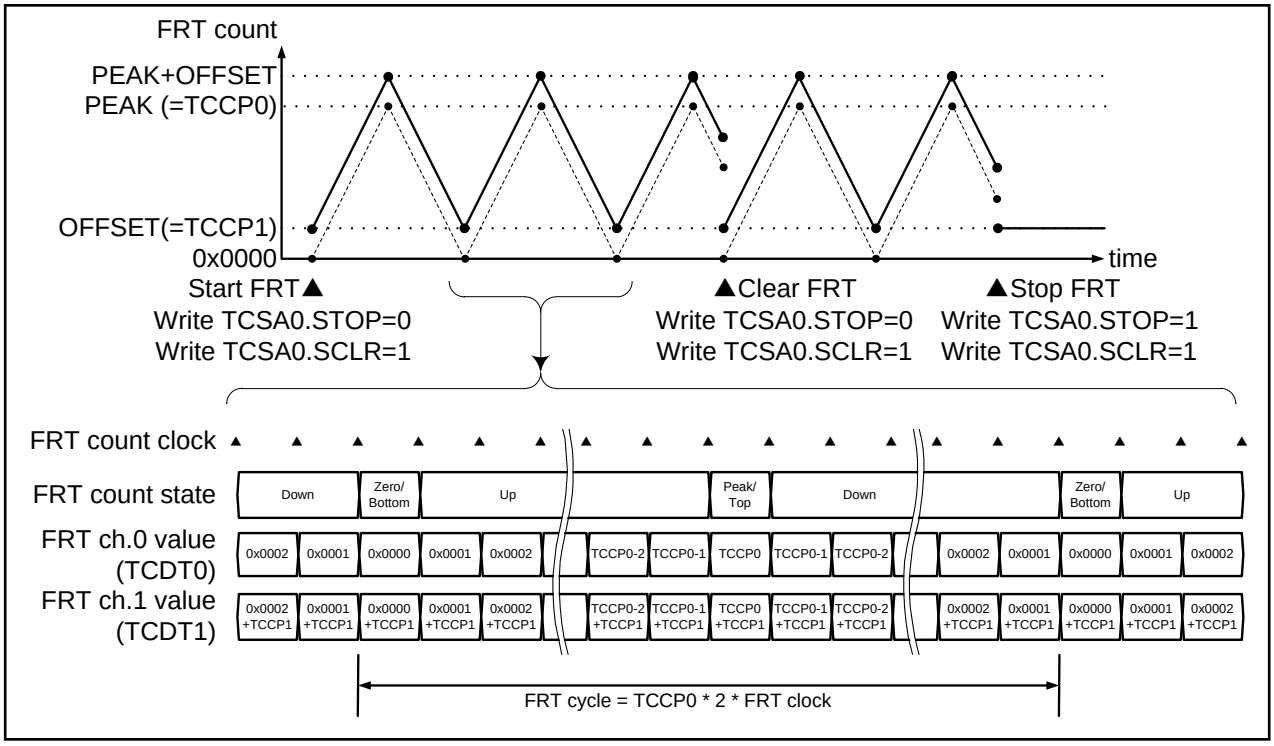
After count mode with offset is selected, when counting is started the first time, be sure to always write TCSA0.SCLR=1 for the first time. Writing this value initializes the counter values for both ch.0 and ch.2.

When TCSD.OFMD2=1, the ch.2 control registers (TCSA2 and TCSC2) are not used. Both ch.0 and ch.2 are controlled simultaneously by the ch.0 control registers (TCSA0 and TCSC0).

4.1.2.6 Offset Up/Down-count Mode Operation (ch.1)

This section describes FRT-ch.1. The FRT count operation for FRT-ch.1 up/down-count mode with offset is shown in Figure 4-5. The solid lines in the figure indicate ch.1 count operations, and the dashed lines indicate ch.0 count operations. To make the figure easier to read, the change when the counter value was cleared is not connected by a line.

Figure 4-5 FRT Operation in Up/down-count Mode with Offset (ch.1)



The count mode operation and control procedure are described below.

FRT-ch.0 is set to normal up/down-count mode, and FRT-ch.1 is set to up/down-count mode with offset. (TCSA0.MODE=1 and TCSD.OFMD1=1)

The ch.0 peak value is set to TCCP0, and the ch.1 offset value is set to TCCP1.

Writing of TCSA0.STOP=0 and TCSA0.SCLR=1 is performed. The FRT-ch.0 counter value (=TCDT0) is initialized to 0x0000, and the FRT-ch.1 counter value (=TCDT1) is initialized to the offset value (=TCCP1). The count operation is started simultaneously for ch.0 and ch.1.

Operation is performed in the above-described normal up/down-count mode for the ch.0 counter value. Counting is started from the offset value (=TCCP1) for the ch.1 counter value and then incremented to the peak + offset value (=TCCP0+TCCP1). Then, the value decrements to the offset value (=TCCP1). Following this, the count operation is repeated. The FRT count cycle is TCCP0 × 2 × count clock cycle for both ch.0 and ch.1.

During a count operation, writing of TCSA0.STOP=0 and TCSA0.SCLR=1 can be performed to simultaneously initialize the ch.0 count value to 0x0000 and initialize the ch.1 count value to the offset value (=TCCP1) and to continue the subsequent count operation. After initialization, count is restarted in the up direction.

Writing of TCSA0.STOP=1 and TCSA0.SCLR=1 can be performed to simultaneously initialize the ch.0 counter value to 0x0000 and initialize the ch.1 counter value to the offset value (=TCCP1) and stop the count operation.

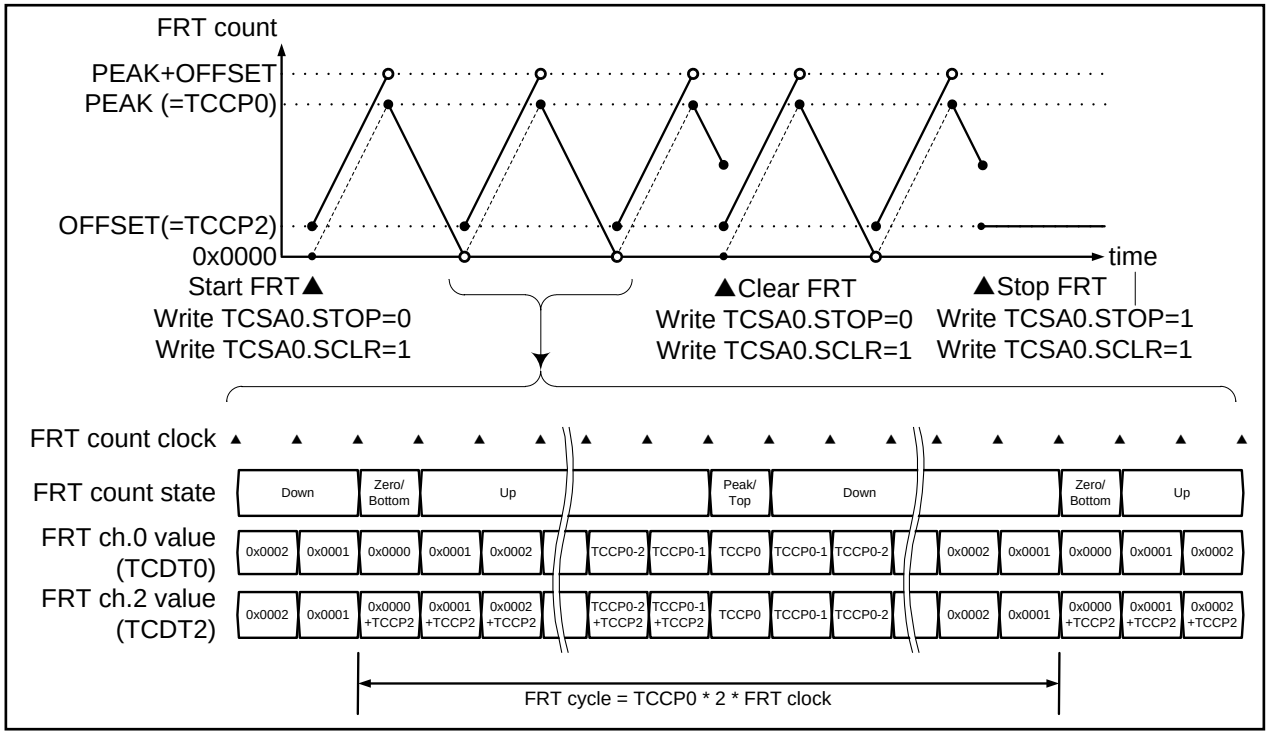
After count mode with offset is selected, when counting is started the first time, be sure to always write TCSA0.SCLR=1 for the first time. Writing this value initializes the counter values for both ch.0 and ch.1.

When TCSD.OFMD1=1, the ch.1 control registers (TCSA1 and TCSC1) are not used. Both ch.0 and ch.1 are controlled simultaneously by the ch.0 control registers (TCSA0 and TCSC0).

4.1.2.7 Offset Up/Down-count Mode Operation (ch.2)

This section describes FRT-ch.2. The FRT count operation for FRT-ch.2 up/down-count mode with offset is shown in Figure 4-6. The solid lines in the figure indicate ch.2 count operations, and the dashed lines indicate ch.0 count operations. To make the figure easier to read, the change when the counter value was cleared is not connected by a line.

Figure 4-6 FRT Operation in Up/down-count Mode with Offset (ch.2)



The count mode operation and control procedure are described below.

FRT-ch.0 is set to normal up/down-count mode, and FRT-ch.2 is set to up/down-count mode with offset. (TCSA0.MODE=1 and TCSD.OFMD2=1)

The ch.0 peak value is set to TCCP0, and the ch.2 offset value is set to TCCP2.

Writing of TCSA0.STOP=0 and TCSA0.SCLR=1 is performed. The FRT-ch.0 counter value (=TCDT0) is initialized to 0x0000, and the FRT-ch.2 counter value (=TCDT2) is initialized to the offset value (=TCCP1). The count operation is started simultaneously for ch.0 and ch.2.

Counter operation is performed in the above-described normal up/down-count mode for ch.0. The dashed line in the figure is omitted for the location where ch.0 and ch.2 have the same count value. Counting is started from the offset value (=TCCP2) for the ch.2 counter value and then incremented to the peak + offset value - 1 (=TCCP0+TCCP2 - 1). Then, the count operation counts to the peak value (TCCP0) and decrements to 0x0001. Next, the value counts to the offset value (=TCCP2). Following this, the count operation is repeated. This operation is indicated by black dots and white dots in the top section of the figure. The FRT count value is shown in the bottom section of the figure. When the ch.0 count value is in the peak state or countdown state, the offset value is not added to the ch.2 count value. The FRT count cycle is TCCP0 × 2 × count clock cycle for both ch.0 and ch.2.

During count operation, writing of TCSA0.STOP=0 and TCSA0.SCLR=1 can be performed to simultaneously initialize the ch.0 count value to 0x0000 and initialize the ch.2 count value to the offset value (=TCCP2) and to continue the subsequent count operation. After initialization, count is restarted in the up direction.

Writing of TCSA0.STOP=1 and TCSA0.SCLR=1 can be performed to simultaneously initialize the ch.0 counter value to 0x0000 and initialize the ch.2 counter value to the offset value (=TCCP2) and stop the count operation.

After count mode with offset is selected, when counting is started the first time, be sure to always write TCSA0.SCLR=1 for the first time. Writing this value initializes the counter values for both ch.0 and ch.2.

When TCSD.OFMD2=1, the ch.2 control registers (TCSA2 and TCSC2) are not used. Both ch.0 and ch.2 are controlled simultaneously by the ch.0 control registers (TCSA0 and TCSC0).

4.1.2.8 FRT Count Status

The FRT count value and FRT count status are included in the bottom section of Figure 4-1, Figure 4-2, Figure 4-3, Figure 4-4, Figure 4-5, and Figure 4-6. The FRT count status and count value are input to OCU, ICU, and ADCMP connected to FRT. Each block performs output signal changes, buffer transfer operation, and other operations based on these inputs. The FRT count statuses are defined as shown below. Refer to the sections describing the OCU and ADCMP operations.

FRT count value is 0x0000 or offset value: Zero/Bottom status

FRT counter value is at the peak value or peak+offset value: Peak/Top status

FRT counter value is being incremented: Up status

FRT counter value is being decremented: Down status

4.1.3 TCCP Register Function

4.1.3.1 TCCP Register Function

The TCCP register is a 16-bit register that sets the FRT peak value (count cycle) and offset value. During an FRT count operation, writing can be performed to the TCCP register to change the peak value and offset value. The FRT peak value that is set to the TCCP register is used to determine the FRT count cycle as shown below.

- In up-count mode: FRT count cycle = (TCCP+1) × FRT count clock cycle
- In up/down-count mode: FRT count cycle = TCCP × 2 × FRT count clock cycle

The TCCP register has a buffer function. When the FRT peak value is set to the TCCP register, the TCSA.BUFE register setting can be used to select enable or disable for the buffer register function.

When the buffer register function is enabled (TCSA.BUFE=1), the peak value written to the TCCP register from the CPU is first stored to the TCCP buffer register. Then, zero detection of the FRT is used to transfer the value from the TCCP buffer register to the TCCP register.

When the buffer register function is disabled (TCSA.BUFE=0), the peak value written to the TCCP register from the CPU is immediately transferred to the TCCP register.

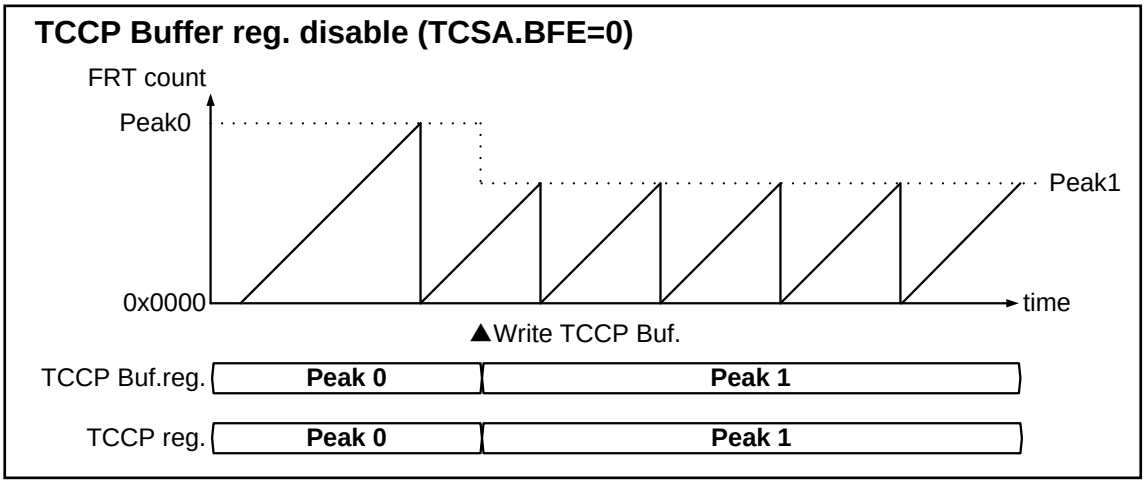
When count mode with offset is selected in the FRT, and an FRT offset value is set to the TCCP register, the buffer register function is constantly disabled. In this case, the offset value written to the TCCP register from the CPU is immediately transferred to the TCCP register. However, even if the offset value was changed, the offset value of the FRT counter value is not immediately changed, and the updated value is applied starting from the next cycle.

If data is read from the TCCP register, values are read from the TCCP register, not from the TCCP buffer register. While the buffer function is enabled, the value before transfer is read until the transfer is completed.

4.1.3.2 Changing the Peak Value Setting (Normal Up-count Mode)

Figure 4-7 shows the operation waveform when the peak value is updated while the TCCP register buffer function is disabled in normal up-count mode.

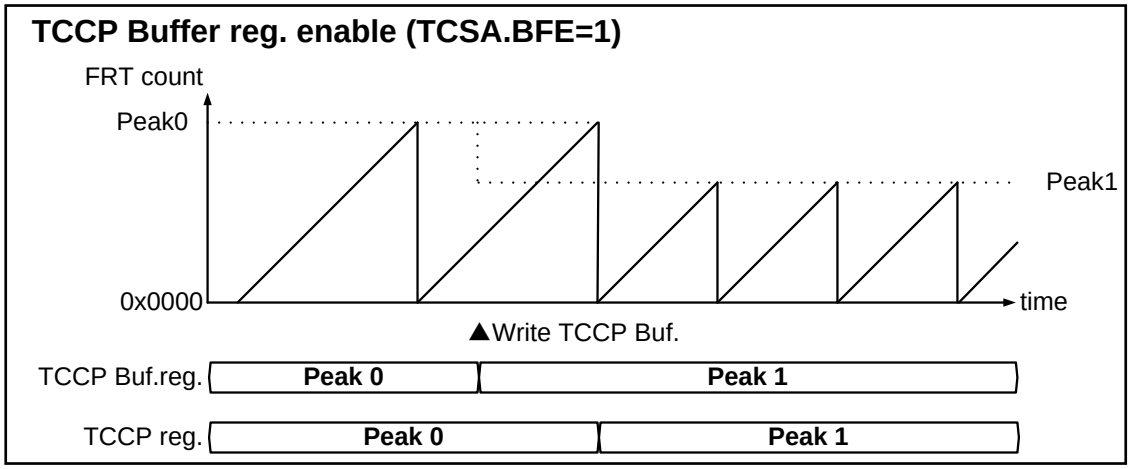
Figure 4-7 Changing the Cycle in Normal Up-count Mode



When the buffer function is disabled, the value in the buffer register is immediately applied to the TCCP register. The FRT cycle can be changed from the FRT cycle where writing was performed. In this case, writing a value smaller than the FRT count value at that time performs a count-up operation of the FRT count value to 0xFFFF, and so careful attention is necessary.

Figure 4-8 shows the operation waveform when the peak value is updated while the TCCP register buffer function is enabled in normal up-count mode.

Figure 4-8 Changing the Cycle in Normal Up-count Mode

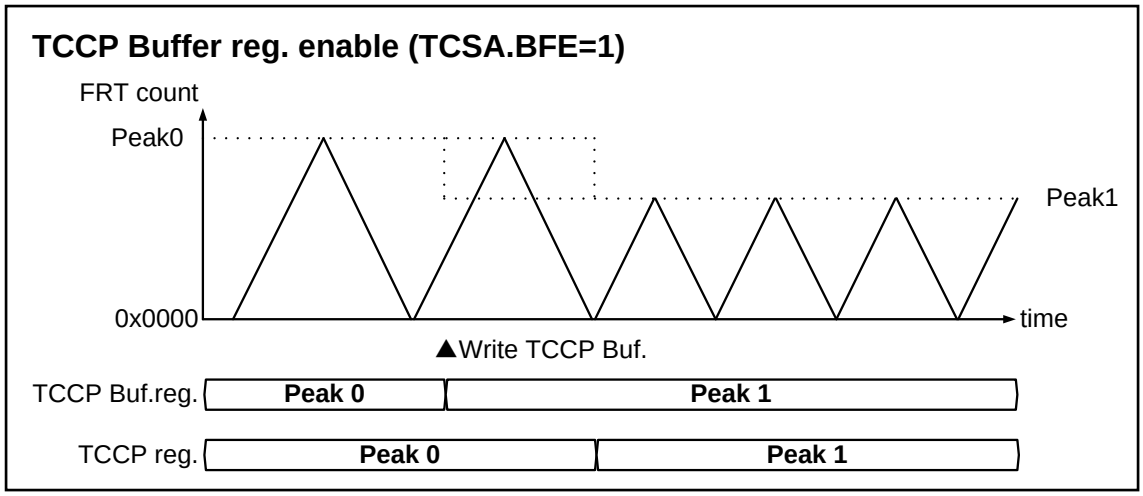


When the buffer function is enabled, after the value is written to the buffer register, the value is transferred to the TCCP register when the next Zero/Bottom is detected. The FRT count cycle is changed starting from the next FRT cycle where writing was performed.

4.1.3.3 Changing the Peak Value Setting (Normal Up/Down-count Mode)

Figure 4-9 shows the operation waveform when the buffer function is enabled in normal up/down-count mode.

Figure 4-9 Changing the Cycle in Normal Up/Down-count Mode

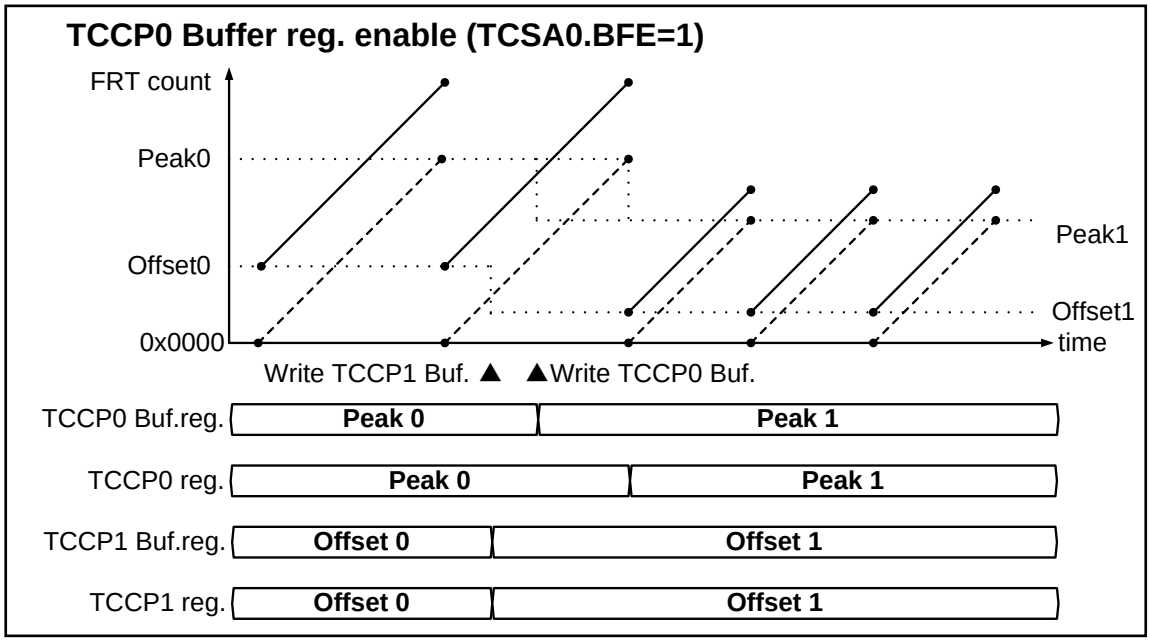


In normal up/down-count mode, the TCCP register of the peak value setting is used by selecting buffer function enabled. The value that was written to the buffer register is transferred to the TCCP register when the next Zero/Bottom is detected. The FRT count cycle is changed starting from the next FRT cycle where writing was performed.

4.1.3.4 Changing the Offset Value Setting (ch.1 and ch.2 Up-count with Offset)

Figure 4-10 shows the operation waveform when both the peak value and offset value are changed in ch.1 up-count mode with offset.

Figure 4-10 Changing the Cycle and Offset in Up-count Mode with Offset



The solid lines in the figure indicate ch.1 count operations, and the dashed lines indicate ch.0 count operations. To make the figure easier to read, the change from the ch.0 peak to zero and the change from the ch.1 peak+offset to the offset are not connected by a line. In this figure, the TCSA0.BUFE=1 setting indicates when the buffer function of the peak value for TCCP0 is enabled.

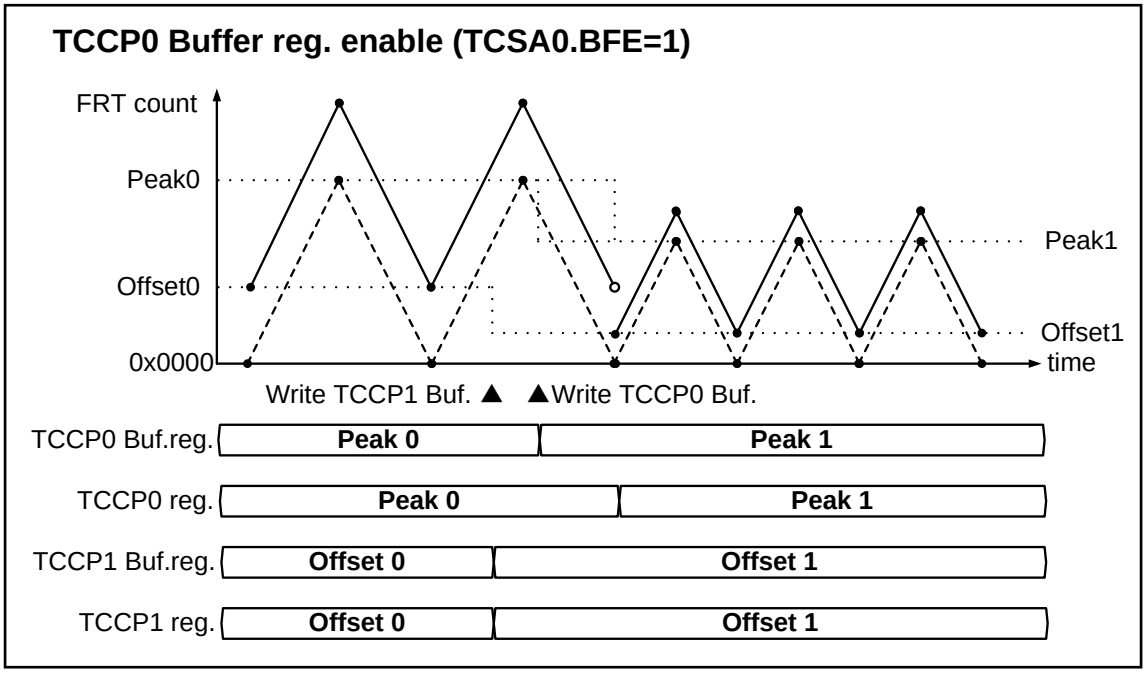
In the ch.1 counter of up-count mode with offset, the ch.0 counter value is in the peak value status, or in the case of initialization, the TCCP1 register value is referenced, and the register value is applied to the ch.1 counter value as the offset value. In the case of other statuses, the ch.1 counter performs count operation by incrementing the current counter value. As a result, if the TCCP1 register was overwritten during the count operation, the offset value is applied starting from the next FRT cycle. The buffer function of the TCCP1 register where the offset is stored is disabled, but the ch.1 counter offset value does not change during the FRT cycle.

Operation when up-count mode with offset is selected in ch.2 is also identical.

4.1.3.5 Changing the Offset Value Setting (ch.1 Up/down-count with Offset)

Figure 4-11 shows the operation waveform when both the peak value and offset value are changed in ch.1 up/down-count mode with offset.

Figure 4-11 Change Operation for Cycle and Offset in Up/down-count Mode with Offset (ch.1)



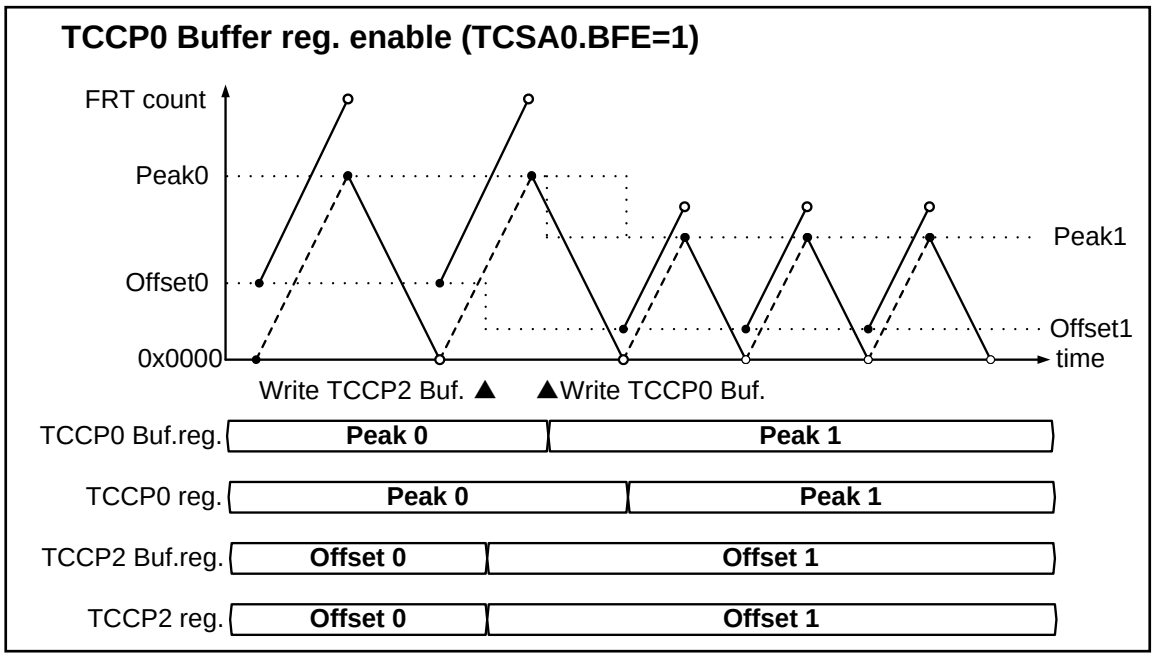
The solid lines in the figure indicate ch.1 count operations, and the dashed lines indicate ch.0 count operations. In this figure, the TCSA0.BUFE=1 setting indicates when the buffer function of the peak value for TCCP0 is enabled.

In the ch.1 counter of up/down-count mode with offset, the ch.0 counter value is in the 0x0000 status, or in the case of initialization, the TCCP1 register value is referenced, and the register value is applied to the ch.1 counter value as the offset value. In the case of other statuses, the counter performs count operation by incrementing or decrementing the current counter value. As a result, if the TCCP1 register was overwritten during the count operation, the offset value is applied starting from the next cycle. The buffer function of the TCCP1 register where the offset is stored is disabled, but the ch.1 counter offset value does not change during the FRT cycle. The changed new offset value is applied to the ch.1 count value starting from when the ch.0 counter value becomes 0x0000. This operation is shown by the white dots on the solid lines indicating ch.1 count operations in the figure.

4.1.3.6 Changing the Offset Value Setting (ch.2 Up/down-count with Offset)

Figure 4-12 shows the operation waveform when both the peak value and offset value are changed in ch.2 up/down-count mode with offset.

Figure 4-12 Change Operation for Cycle and Offset in Up/down-count Mode with Offset (ch.2)



The solid lines in the figure indicate ch.2 count operations, and the dashed lines indicate ch.0 count operations. In this figure, the TCSA0.BUFE=1 setting indicates when the buffer function of the peak value for TCCP0 is enabled.

In the ch.2 counter of up/down-count mode with offset, the ch.0 counter value is in the 0x0000 status, or in the case of initialization, the TCCP2 register is referenced, and the register value is applied to the ch.2 counter value as the offset value. In the case of other statuses, the TCCP2 register is not referenced. As a result, if the TCCP2 register was overwritten during the count operation, the offset value is applied starting from the next cycle. The buffer function of the TCCP2 register where the offset is stored is disabled, but the ch.2 counter offset value does not change during the FRT cycle. The changed new offset value is applied to the ch.2 count value starting from when the ch.0 counter value becomes 0x0000.

4.1.4 FRT Interrupt Operation

4.1.4.1 Zero Detection and Peak Detection Event Register Operation

The TCSA.IRQZF bit is an event detection register for notifying the CPU when a count operation is performed while the FRT is in the Zero/Bottom status. If an interrupt is allowed by TCSA.IRQZE=1, the CPU can receive zero detection interrupts. The TCSA.IRQZF bit can be cleared by writing "0" from the CPU.

The TCSA.ICLR bit is an event detection register for notifying the CPU when a count operation is performed while the FRT is in the Peak/Top status. If an interrupt is allowed by TCSA.ICRE =1, the CPU can receive zero detection interrupts. The TCSA.ICLR bit can be cleared by writing "0" from the CPU.

See "4.10 Treatment of Event Detect Register and Interrupt".

These event detection registers are not set and do not generate unneeded interrupts in the following cases.

- When FRT is not performing a count operation
- When performing the count operation for the first time after the bus is reset or after TCSA.SCLR=1 is written
- When the zero interrupt mask count is not 0 (TCSC.MSZC≠0000), IRQZF is not set.
- When the peak interrupt mask count is not 0, (TCSC.MSPC≠0000), ICLR is not set.
- If TCSD.OFMD1=1, TCSA1.IRQZF and TCSA1.ICLR are fixed at 0 and are not set.
- If TCSD.OFMD2=1, TCSA2.IRQZF and TCSA2.ICLR are fixed at 0 and are not set.

If count mode with offset is selected, TCSA0.IRQZF and TCSA0.ICLR for ch.0 only are set. The IRQZF and ICLR for ch.1 and ch.2 are not set, and no interrupt is generated.

4.1.4.2 Operation of Interrupt Mask Counters

Four-bit Zero value detection mask counters are used in FRTs to reduce (mask) the number of times the Zero detection register (IRQZF) is set, at a constant rate. The Zero value detection mask counter (MSZC[3:0]) performs a down count to reload the MSZI[3:0] value as the initial value. Zero detection flags are set when MSZC is 0. The relationship between the MSZI setting values and Zero value detection interrupt mask count is shown in Table 4-5.

Table 4-5 TCSC.MSZI Setting Values and Zero Value Detection Interrupt Mask Count

MSZI Setting	Function
0	IRQZF is always set (not masked) for every FRT count at “0x0000”.
1	IRQZF is set once for every 2 FRT counts at 0x0000 (skipping 1 count).
• • •	Omitted
15	IRQZF is set once for every 16 FRT counts at 0x0000 (skipping 15 counts).

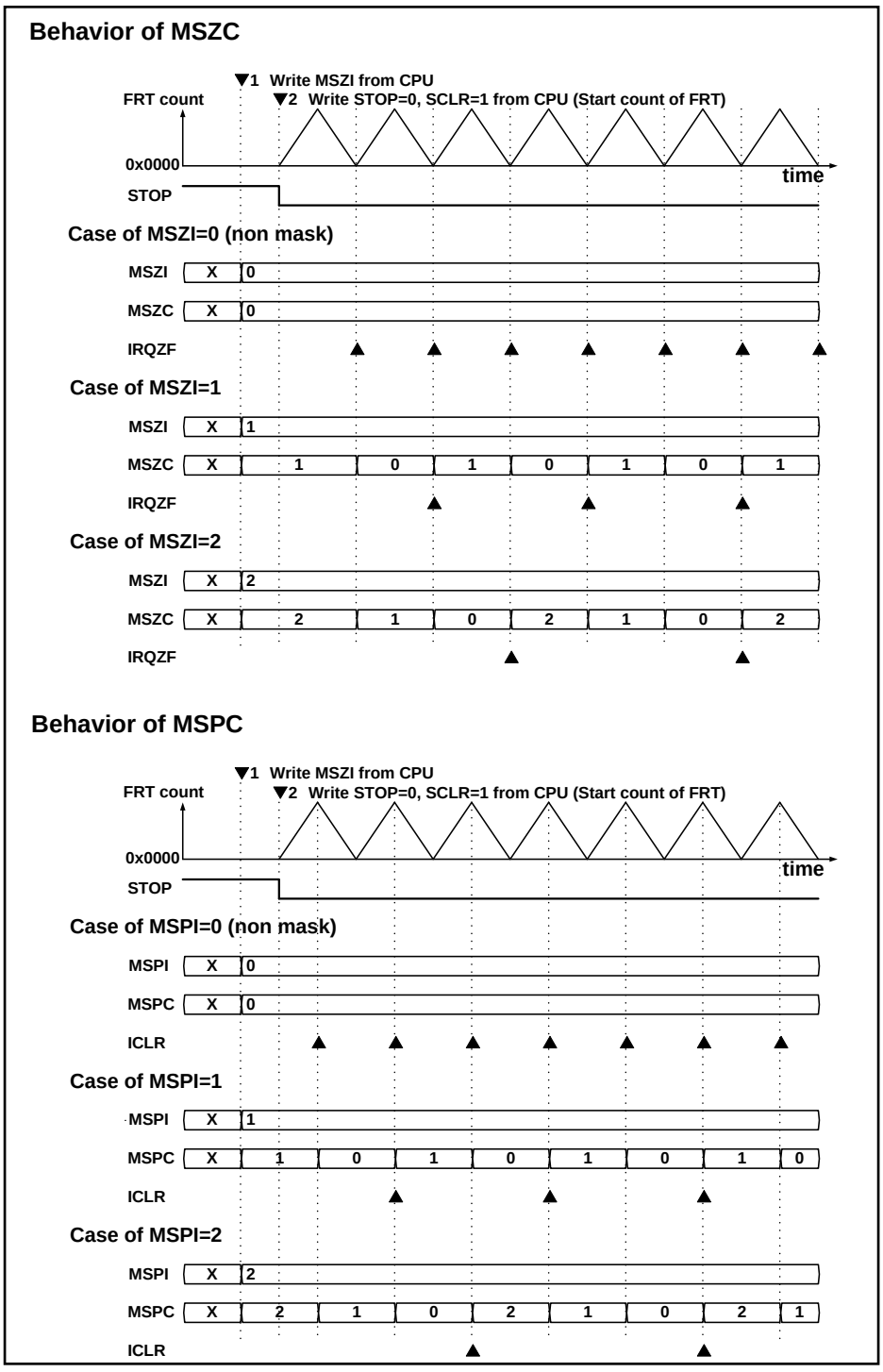
Four-bit Peak value detection mask counters are used in FRTs to reduce (mask) the number of times the Zero detection register (ICLR) is set, at a constant rate. The Peak value detection mask counter (MSPC[3:0]) performs a down count to reload the MSPI[3:0] value as the initial value. Peak detection flags are set when MSPC is "0". The relationship between the MSPI setting values and peak value detection interrupt mask count is shown in Table 4-6.

Table 4-6 TCSC.MSPI Setting Values and Peak Value Detection Interrupt Mask Count

MSPI Setting	Function
0	ICLR is always set (not masked) for every FRT =Peak count.
1	ICLR is set once for every 2 FRT=Peak counts (skipping 1 count).
• • •	Omitted
15	ICLR is set once for every 16 FRT=Peak counts (skipping 15 counts).

Figure 4-13 shows examples of Zero value detection mask counter and Peak value detection mask counter operations.

Figure 4-13 Example 1: Operation of Interrupt Mask Counter



This figure shows operational examples for cases where, starting from the top, MSZI is 0, 1 and 2, and cases where MSPI is 0, 1 and 2. Points with ▲ show the times when the IRQZF or ICLR is set.

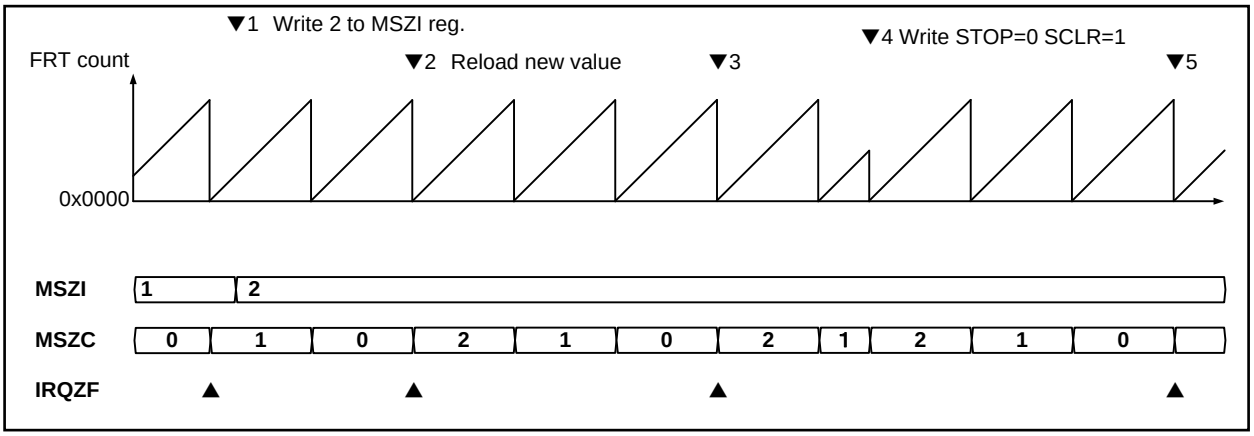
Initial value (written to MSZI and MSPI) is set at time ▼1. When writing to MSZI and MSPI while FRT counting is stopped (STOP=1), values are immediately reflected in the internal counters (MSZC, MSPC).

The FRT starts counting at time ▼2 (writing STOP=0 and SCLR=1). This timing is for the first FRT count operation from 0x0000 to 0x0001 after a bus reset or writing SCLR=1, so that the IRQZF is not set independently of the MSZC value at this time. Each counter down counts at time FRT=0x0000 and FRT=TCCP after that.

When writing to MSZI or MSPI while the FRT is counting (STOP=0), only the initial value setting is written, it is not reflected in the counter values (MSZC, MSPC). When 1 is written to SCLR, the initial values of MSZI and MSPI are reloaded into the mask counter.

Figure 4-14 shows an operational example.

Figure 4-14 Example 2: Operation of Interrupt Mask Counter



The value for MSZI is rewritten from 1 to 2 at time ▼1 while the FRT is counting (STOP=0). In this case, the new MSZI setting is reloaded at time ▼2. The generation of interrupts by the IRQZF changes at time ▼3.
1 is written to SCLR at time ▼4. The MSZI value is reloaded into MSZC. The next IRQZF interrupt is generated at time ▼5. At time ▼4 in the figure, 1 is written to SCLR, and the first FRT count operation from 0x0000 to 0x0001 is performed. IRQZF is not set independently of the MSZC value at this time.

In cases where both Zero detection interrupt and Peak detection interrupt masks are used, pay attention to the rewrite time when MSZI or MSPI is rewritten while FRT is running. Both mask counters may not be synchronized.

When count mode with offset is selected, TCSC0.MSZC and TCSC0.MSPC of ch.0 only are down-counted. The MSZC counter and MSPC counter of ch.1 and ch.2 are fixed at 0 and do not down-count.

The OCU and ADCMP connected to FRT perform buffer transfer operations, AD start, and other operations linked to the FRT interrupt mask counter. If the FRT where connection by OCU and ADCMP is selected is in count mode with offset (ch.1 and ch.2), the FRT interrupt mask counter value is connected to the ch.0 interrupt mask counter value that is operating synchronously. As a result, buffer transfer and AD start linked to the interrupt mask counter can be performed even if the FRT in count mode with offset is connected.

4.2 Description of OCU Operation

OCU operation is described below.

4.2.1 OCU Control Register

For a list of OCU control register functions and timings when the setting may be changed, see Table 4-7. Basic OCU settings are made when OCU channel operation is prohibited. When channel operation is permitted (OCSA.CST0=1, OCSA.CST1=1), output signals (RT(0), RT(1)) and interrupt flags (OCSA.IOP0, OCSA.IOP1) are changed in accordance with the control register specification based on the counter value of the connected FRT.

Table 4-7 OCU Control Registers

Register ch.(1)	Register ch.(0)	Function	Valid Timing for Updating
OCSA:CST1	OCSA:CST0	Selection of operation prohibition/permission	Any time after initial setting
OCFS:FSO1	OCFS:FSO0	Selection of connected FRT (*1)	Any time before OCU is permitted working. Don't update it after OCU is permitted working
OCSD:OCCP1BUFE OCSD:OPBM1	OCSD:OCCP0BUFE OCSD:OPBM0	Selection of OCCP buffer existence/absence and transmission parameters	
OCSD:OCSE1BUFE OCSD.OEBM1	OCSD:OCSE0BUFE OCSD.OEBM0	Selection of OCSE buffer existence/absence and transmission parameters	
OCSB:FM4 common use for ch.(1) and ch.(0) (*2)		Selection of FM4 mode/FM3 conversion mode	
OCSB:CMOD common use for ch.(1) and ch.(0)		Selection of operational content of FM3 conversion mode	
OCSC:MOD(1)	OCSC:MOD(0)		
OCSD.OFEX1	OCSD.OFEX0	Specification of operational content in FM4 mode	
OCSE(1)[31:0]	OCSE(0)[15:0]	Specification of operational content in FM4 mode	Any time before OCU is permitted working. After OCU is permitted working, it is available to update it if OCSE buffer function is valid. Don't update it when OCSE buffer function is invalid after OCU is permitted working.
OCSB:OTD1	OCSB:OTD0	Setting of initial level and status read out of RT(0) output pin, RT(1) output pin	Update it as an initial level of output before OCU is permitted working. After OCU is permitted working, updating is ignored.
OCSA:IOP1	OCSA:IOP0	Read or clear match detection register	Any time after initial setting
OCSA:IOE1	OCSA:IOE0	Selection of interrupt permission/prohibition	
OCCP(1)	OCCP(0)	Specification of OCU compare value	

*1: The content of OCU operation differs depending on the value of the operation mode (TCSA.MODE) of the FRT selected for connection.

*2: For details of operation when OCSB.FM4=0 (FM3 compatible mode), see 4.3 OCU FM3 Family Product-compatible Operation

4.2.2 Independent Channel Operation

OCU has two type of operation. (i.e. 'Independent Channel Operation' and 'Channel-Linked Operation') OCU of Independent Channel Operation will output waveform from ch.(0) and ch.(1) with the value of OCCP(0) and OCCP(1) respectively. OCU of Channel-Linked Operation will output waveform from ch.(1) with the valud of OCCP(0) and OCCP(1).

The output waveform generating operation when OCU-ch(0) and OCU-ch(1) operate independently is described below.

4.2.2.1 List of Setting Examples

A list of initial set values for setting example 1 to setting example 8 is shown Table 4-8 and Table 4-9.

Table 4-8 OCU ch.0 Setting Examples

Setting Description	Setting Register	Setting Example 1	Setting Example 2	Setting Example 3	Setting Example 4
FRT Mode	TCSA0:MODE	0	1	1	1
FRT Selection	OCFS10:FSO0	0000	0000	0000	0000
OCCP0 Buffer function	OCSD10:OCCP0BUFE OCSD10.OPBM0	00 0	01 0	01 0	11 0
OCSE0 Buffer function	OCSD10:OCSE0BUFE OCSD10.OEBM0	00 0	00 0	00 0	00 0
ch.0 working condition	OCSB10.FM4 OCSE0[15:0] OCSD10.OFEX0	1 0x0FFF 0	1 0x852D 0	1 0x4A1D 0	1 0x95A0 0
Interrupt	OCSA10:IOE0	As required	As required	As required	As required
Output level	OCSB10:OTD0 OCCP0	Specify an initial value	Specify an initial value	Specify an initial value	Specify an initial value

Table 4-9 OCU ch.1 Setting Examples

Setting Description	Setting Register	Setting Example 5	Setting Example 6	Setting Example 7	Setting Example 8	Setting Example 9
FRT Mode	TCSD.OFMD1 TCSD.OFMD2 TCSA0:MODE TCSA1.MODE TCSA2.MODE	- - 0 - -	- - 1 - -	- - 1 - -	- - 1 - -	1 1 0 0 0
FRT Selection	OCFS10:FSO1	0000	0000	0000	0000	0010
OCCP0 Buffer function	OCSD10:OCCP1BUFE OCSD10.OPBM1	00 0	01 0	01 0	11 0	11 0
OCSE0 Buffer function	OCSD10:OCSE1BUFE OCSD10.OEBM1	00 0	00 0	00 0	00 0	00 0
ch.0 working condition	OCSB10.FM4 OCSE1[15:0] OCSE1[31:0] OCSD10.OFEX1	1 0x0FFF 0x0FF0 0	1 0x852D 0x8520 0	1 0x4A1D 0x4A10 0	1 0x95A0 0x95A0 0	1 0x95A0 0x95A0 1
Interrupt	OCSA10:IOE1	As required	As required	As required	As required	As required
Output level	OCSB10:OTD1 OCCP1	Specify an initial value	Specify an initial value	Specify an initial value	Specify an initial value	Specify an initial value

4.2.2.2 Operation for Setting Example 1

The RT0 and IOP0 operations at control timings shown in setting example 1 are shown in Table 4-10. The output waveform chart is shown in Figure 4-15. The OCCP0 buffer is omitted from the charts. The ▲ mark indicates IOP0 set timings. The FRT operates in the up-down count mode. The value from the CPU written in the OCCP0 buffer is immediately sent to the OCCP0 register. In this setting example, whenever the FRT and OCCP0 match, the RT0 output level is inverted and an interrupt can be generated.

At timings▼1, ▼2, ▼3, ▼5, ▼6 in the charts, the control parameters for each parameter number column in the table have been satisfied. Parameter 4 has been satisfied for other timings. RT0 signal output and IOP0 operate in accordance with the respective specifications. Since the FRT is operated in the up-count mode, parameters 7 and 8 have not been satisfied.

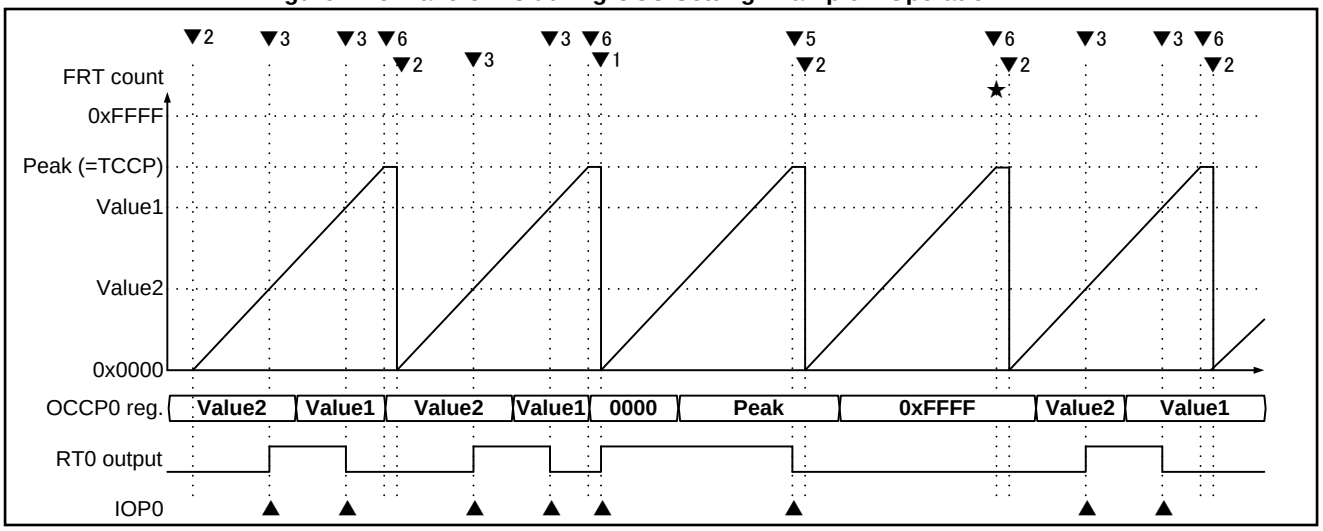
Because timing ★ in the charts operates the FRT in the up-count mode (TCSA.MODE=0), OCCP0=0xFFFF is not treated as a peak match. Operation is in accordance with parameter 6. Match is detected at (TCCP=0xFFFF).

In this setting example, when OCCP0 is included in the following range, the output signal is not changed. The peak value < OCCP0 ≤ 0xFFFF.

Table 4-10 Content of Operation for OCU Setting Example 1

Control Parameter			Setting Example 1 OCSE0=0x0FFF	
FRT Value	**OCCP0 Comparison Result**	**Parameter Number**	**RT0 Operation**	**IOP0 Operation**
Zero/Bottom	Match	1	Reverse	Set
	Mismatch	2	Hold	Hold
Up	Match	3	Reverse	Set
	Mismatch	4	Hold	Hold
Peak	Match	5	Reverse	Set
	Mismatch	6	Hold	Hold
Down	Match	7	Reverse	Set
	Mismatch	8	Hold	Hold

Figure 4-15 Waveforms during OCU Setting Example 1 Operation



4.2.2.3 Operation for Setting Example 2

RT0, IOP0 operations at the control timings in setting example 2 are shown in Table 4-11. The output waveform chart is shown in Figure 4-16. The ▲ mark indicates IOP0 set timings. The FRT operates in the up-down count mode. The write value for OCCP0 from the CPU is provisionally stored in the buffer register and sent to the OCCP0 register when the FRT is 0x0000. New data sent is targeted for comparison from FRT=0x0000. In this setting example, symmetrical Active-High waveform centered on the FRT peak value can be output. In addition, specification of 0x0000 in OCCP0 results in unprocessed (High) output until a value other than 0x0000 is specified.

At timings ▼1, ▼2, ▼3, ▼5, ▼6 and ▼7 in the chart, the control parameters for each parameter number column in the table have been satisfied. At other timings, parameter 4 or 8 have been satisfied. RT0 signal output and IOP0 operate in accordance with the respective specifications.

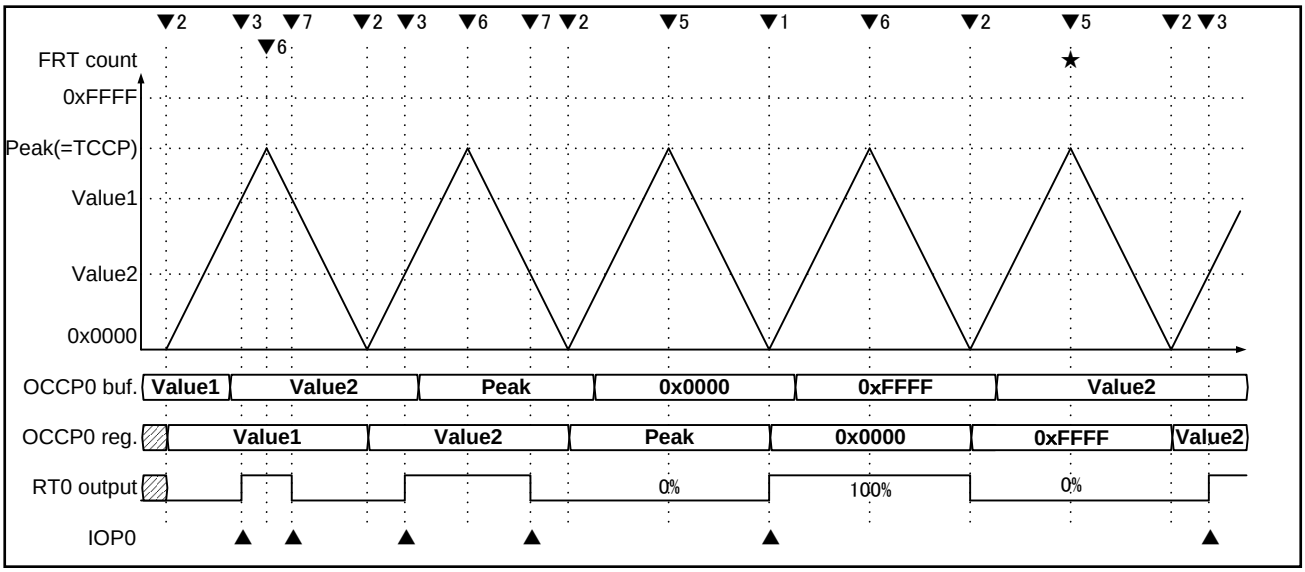
Because timing ★ in the charts operates the FRT in the up-down count mode (TCSA.MODE=1), OCCP0=0xFFFF is treated as a peak match. Operation is in accordance with parameter 5.

In this setting example, when OCCP0 is included in the following range, the output signal is not changed. The peak value ≤ OCCP0 < 0xFFFF.

Table 4-11 Content of Operation for OCU Setting Example 2

Control Parameter			Setting Example 2 OCSE0=0x852D	
FRT Value	**OCCP0 Comparison Result**	**Parameter Number**	**RT0 Operation**	**IOP0 Operation**
Zero/Bottom	Match	1	Set	Set
	Mismatch	2	Reset	Hold
Up	Match	3	Set	Set
	Mismatch	4	Hold	Hold
Peak	Match	5	Hold	Hold
	Mismatch	6	Hold	Hold
Down	Match	7	Reset	Set
	Mismatch	8	Hold	Hold

Figure 4-16 Waveforms during OCU Setting Example 2 Operation



4.2.2.4 Operation for Setting Example 3

RT0, IOP0 operations at the control timings in setting example 3 are shown in Table 4-12. The output waveform chart is shown in Figure 4-17. The ▲ mark indicates IOP0 set timings. The FRT operates in the up-down count mode. The write value for OCCP0 from the CPU is provisionally stored in the buffer register and sent to the OCCP0 register when the FRT is 0x0000. New data sent is targeted for comparison from FRT=0x0000. In this setting example, symmetrical Active-Low waveform centered on the FRT peak value can be output. In addition, specification of 0x0000 in OCCP0 results in unprocessed (Low) output until a value other than 0x0000 is specified.

At timings ▼1, ▼2, ▼3, ▼5, ▼6 and ▼7 in the chart, the control parameters for each parameter number column in the table have been satisfied. At other timings, parameter 4 or 8 have been satisfied. RT(0) signal output and IOP0 operate in accordance with the respective specifications.

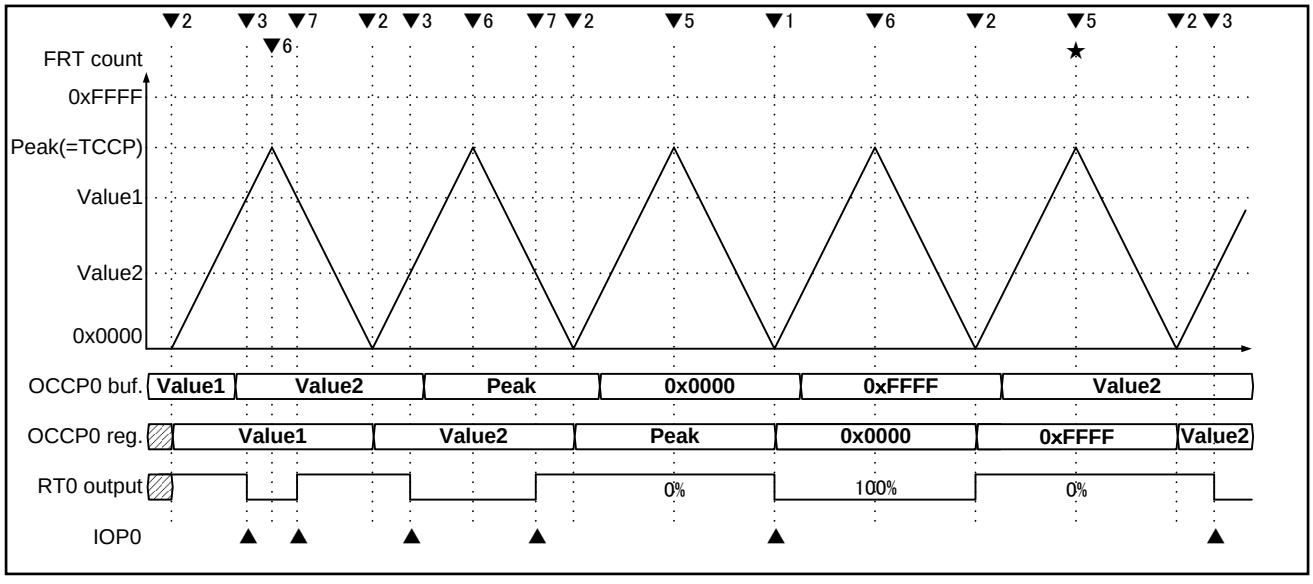
Because timing ★ in the charts operates the FRT in the up-down count mode (TCSA.MODE=1), OCCP0=0xFFFF is treated as a peak match. Operation is in accordance with parameter 5.

In this setting when OCCP0 is included in the following range, the output signal is not changed. The peak value ≤ OCCP0 < 0xFFFFd.

Table 4-12 Content of Operation for OCU Setting Example 3

Control Parameter			Setting Example 3 OCSE0=0x4A1D	
FRT Value	**OCCP0 Comparison Result**	**Parameter Number**	**RT0 Operation**	**IOP0 Operation**
Zero/Bottom	Match	1	Reset	Set
	Mismatch	2	Set	Hold
Up	Match	3	Reset	Set
	Mismatch	4	Hold	Hold
Peak	Match	5	Hold	Hold
	Mismatch	6	Hold	Hold
Down	Match	7	Set	Set
	Mismatch	8	Hold	Hold

Figure 4-17 Waveforms during OCU Setting Example 3 Operation



4.2.2.5 Operation for Setting Example 4

RT0, IOP0 operations at the control timings in setting example 4 are shown in Table 4-13. The output waveform chart is shown in Figure 4-18. The buffer register is omitted from the charts. The FRT operates in the up-down count mode. The write value for OCCP0 from the CPU is provisionally stored in the buffer register and sent to the OCCP0 register when the FRT is 0x0000 and at peak value . New data sent is targeted for comparison from FRT=0x0000, Peak. In this setting example, asymmetrical Active-High waveform centered on the FRT peak value can be output. In addition, specification of 0x0000, peak value (or 0xFFFF) in OCCP0 results in unprocessed output. IOP0 is normally not set.

At timings ▼1, ▼2, ▼3, ▼5, ▼6 and ▼7 in the chart, the control parameters for each parameter number column in the table have been satisfied. At other timings, parameter 4 or 8 have been satisfied. RT(0) signal output operate in accordance with the respective specifications.

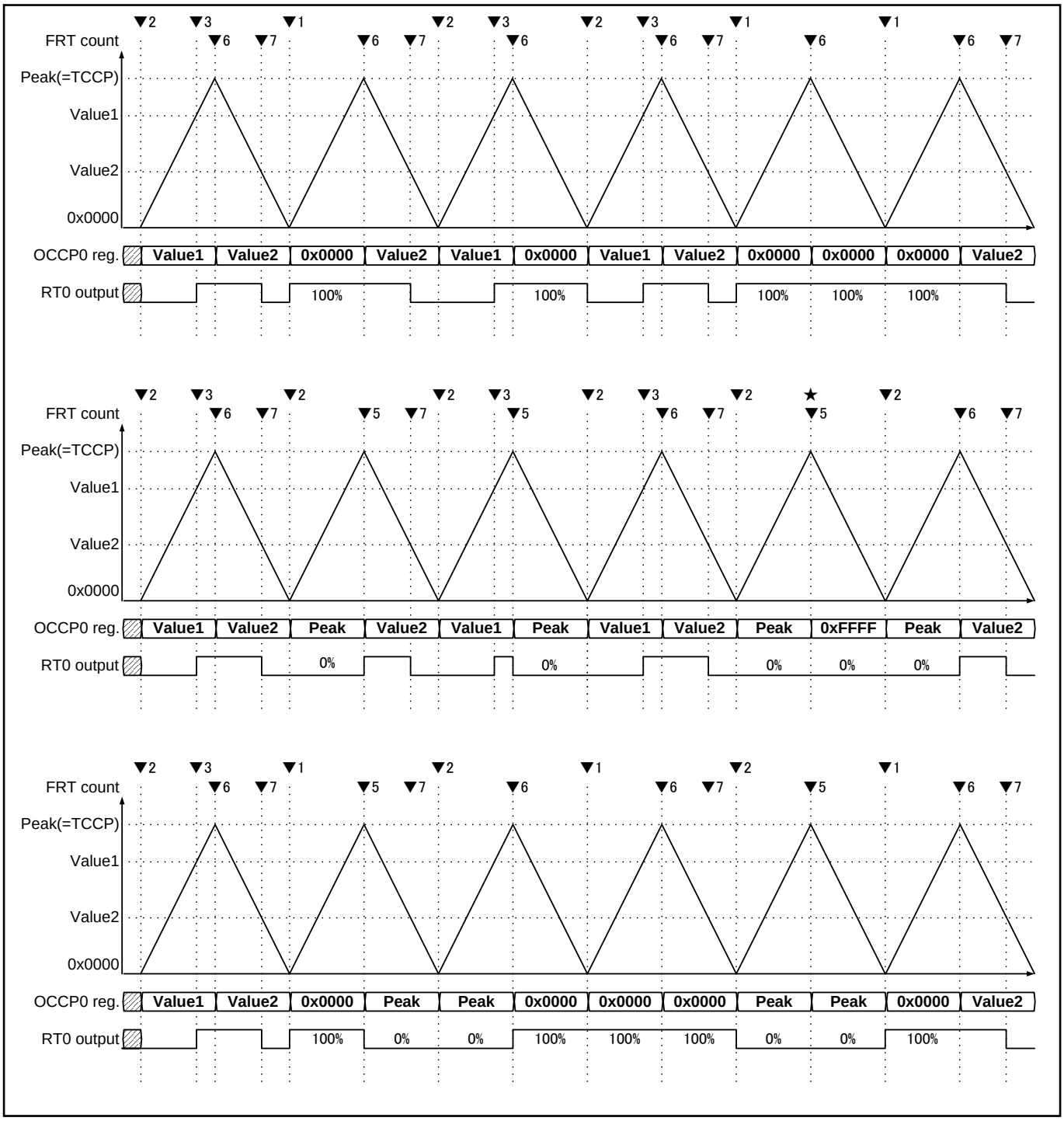
Because timing ★ in the charts operates the FRT in the up-down count mode, OCCP0=0xFFFF is treated as a peak match. Operation is in accordance with parameter 5.

In this setting example, when OCCP0 is included in the following range, the output signal is not changed. The peak value < OCCP0 < 0xFFFF.

Table 4-13 Content of Operation for OCU Setting Example 4

Control Parameter			Setting Example 4 OCSE0=0x95A0	
FRT Value	**OCCP0 Comparison Result**	**Parameter Number**	**RT0 operation**	**IOP0 operation**
Zero/Bottom	Match	1	Set	Hold
	Mismatch	2	Reset	Hold
Up	Match	3	Set	Hold
	Mismatch	4	Hold	Hold
Peak	Match	5	Reset	Hold
	Mismatch	6	Set	Hold
Down	Match	7	Reset	Hold
	Mismatch	8	Hold	Hold

Figure 4-18 Waveforms during OCU Setting Example 4 Operation



4.2.2.6 Conditions for Independent Operation of OCU-ch.(1)

The effects of OCCP(0) value can be eliminated from the change conditions of Ch.(1) RT(1) output signal by specifying the same 12-bit value in bit[31:20] and bit[15:4] in the OCSE(1) register and bit[19:16] =0000. This is because RT(1) change parameters are exactly the same when the OCCP(0) and FRT comparison results match/mismatch the OCCP(1) comparison result. In this setting example, OCUs can be used separately and independently with ch.(0) controlled by OCCP(0) and ch.(1) by OCCP(1). When this parameter is not satisfied, the ch.(1) RT(1) output signal does not operate independently due the possible effect of the OCCP(0) value in some way.

4.2.2.7 Operation for Setting Examples 5, 6, 7, 8

In setting examples 5, 6, 7 and 8, the same 12-bit value is specified in bit[31:20] and bit[15:4] of the OCSE1 register and bit[19:16] =0000 is specified. ch.(1) can be used independently irrespective of the ch.(0)setting.

RT1 and IOP1 operations at each control timing in setting examples 5, 6, 7, 8 are shown in Table 4-14. In setting example 5, 6, 7, 8 operations, the OCCP0 register, RT0 output signal and IOP0 register in setting examples 1, 2, 3 and 4 are replaced by the OCCP1 register, RT1 output signal and IOP1 register. The description of output waveform and operation example is omitted.

Table 4-14 Content of Operation for OCU Setting Examples 5, 6, 7, 8

Control Parameters		Setting Example 5 OCSE1[31:0] =0x0FF00FFF		Setting Example 6 OCSE1[31:0] =0x8520852D		Setting Example 7 OCSE1[31:0] =0x4A104A1D		Setting Example 8 OCSE1[31:0] =0x95A095A0	
FRT Value	OCCP1 Comparison Result	RT1 Operation	IOP1 Operation	RT1 Operation	IOP1 Operation	RT1 Operation	IOP1 Operation	RT1 Operation	IOP1 Operation
Zero/Bottom	Match	Reverse	Set	Set	Set	Reset	Set	Set	Hold
	Mismatch	Hold	Hold	Reset	Hold	Set	Hold	Reset	Hold
Up	Match	Reverse	Set	Set	Set	Reset	Set	Set	Hold
	Mismatch	Hold	Hold	Hold	Hold	Hold	Hold	Hold	Hold
Peak	Match	Reverse	Set	Hold	Hold	Hold	Hold	Reset	Hold
	Mismatch	Hold	Hold	Hold	Hold	Hold	Hold	Set	Hold
Down	Match	Reverse	Set	Reset	Set	Set	Set	Reset	Hold
	Mismatch	Hold	Hold	Hold	Hold	Hold	Hold	Hold	Hold

4.2.2.8 Operation for Setting Examples 9

In setting example 9, FRT-ch.2 where up/down-count operation with offset is performed is connected to OCU-ch.1, and the OCSD.OFEX1=1 setting is used to extend the OCCP1 compare match conditions. RT1 and IOP1 operation at the control timing shown in setting example 9 are shown in Table 4-15. The output waveform figure is shown in Figure 4-19.

In this setting example, the up/down-count operation with offset for FRT-ch.2 is connected to the OCU. In the figure, the FRT-ch.2 count operation is indicated by solid lines. FRT-ch.0 (normal up-count operation), which performs the count operation simultaneously, and FRT-ch.1 (up/down-count operation with offset) are indicated by dashed lines. The OCSD.OFEX1=1 setting is used to extend the comparison determination conditions for the Zero/Bottom status and Peak/Top status in the OCCP1 comparison results field in Table 4-15. The FRT, which is the OCCP1 comparison target, is the FRT-ch.2 value.

The OCCP buffer register is omitted from the figure. The writing value from the CPU to OCCP1 is first stored in the buffer register, and it is transferred to the OCCP1 register at both the Zero/Bottom and Peak/Top of FRT. The transferred new data is the comparison target immediately after transfer.

In this setting example, the RT1 change position of OCU can be output by the Active-High waveform specified separately at the FRT up side and down side. Also, RT dead timer mode is set at the later stage WFG, and the FRT offset value and WFG dead time are set to the same value. The WFG RTO0 and RTO1 output are included together in the figure.

In the case of this setting example, the RTO0 and RTO1 output change positions can be aligned with the timing where the OCCP1 value matches FRT ch.0 and ch.1 within the range of dead time (offset) <= OCCP1 < Peak. Also, a solid high is output at the OCCP1=0x0000 setting. A solid low is output at the (Peak value + Dead time) <= OCCP1 setting.

At the timing of ▼1 to ▼3 and ▼5 to ▼7 in the figure, the control conditions for the respective condition number fields in the table are satisfied. At other timings, condition 4 or condition 8 is satisfied. The RT(1) signal output operates based on the specified conditions.

Table 4-15 Content of Operation for OCU Setting Example 9

Control condition			Setting example 9 OCSE1[31:0]=0x95A095A0 OCSD10.OFEX1=1	
FRT Value	**OCCP1 Comparison Result**	**Condition Number**	**RT1 Operation**	**IOP1 Operation**
Zero/Bottom	OCCP1 <= FRT ch.2	1	Set	Hold
	OCCP1 > FRT ch.2	2	Reset	Hold
Up	OCCP1 == FRT ch.2 (Match)	3	Set	Hold
	OCCP1 != FRT ch.2 (Mismatch)	4	Hold	Hold
Peak/Top	OCCP1 >= FRT	5	Reset	Hold
	OCCP < FRT	6	Set	Hold
Down	OCCP1 == FRT ch.2 (Match)	7	Reset	Hold
	OCCP1 != FRT ch.2 (Mismatch)	8	Hold	Hold

Figure 4-19 Operation Waveform 1 for OCU Setting Example 9

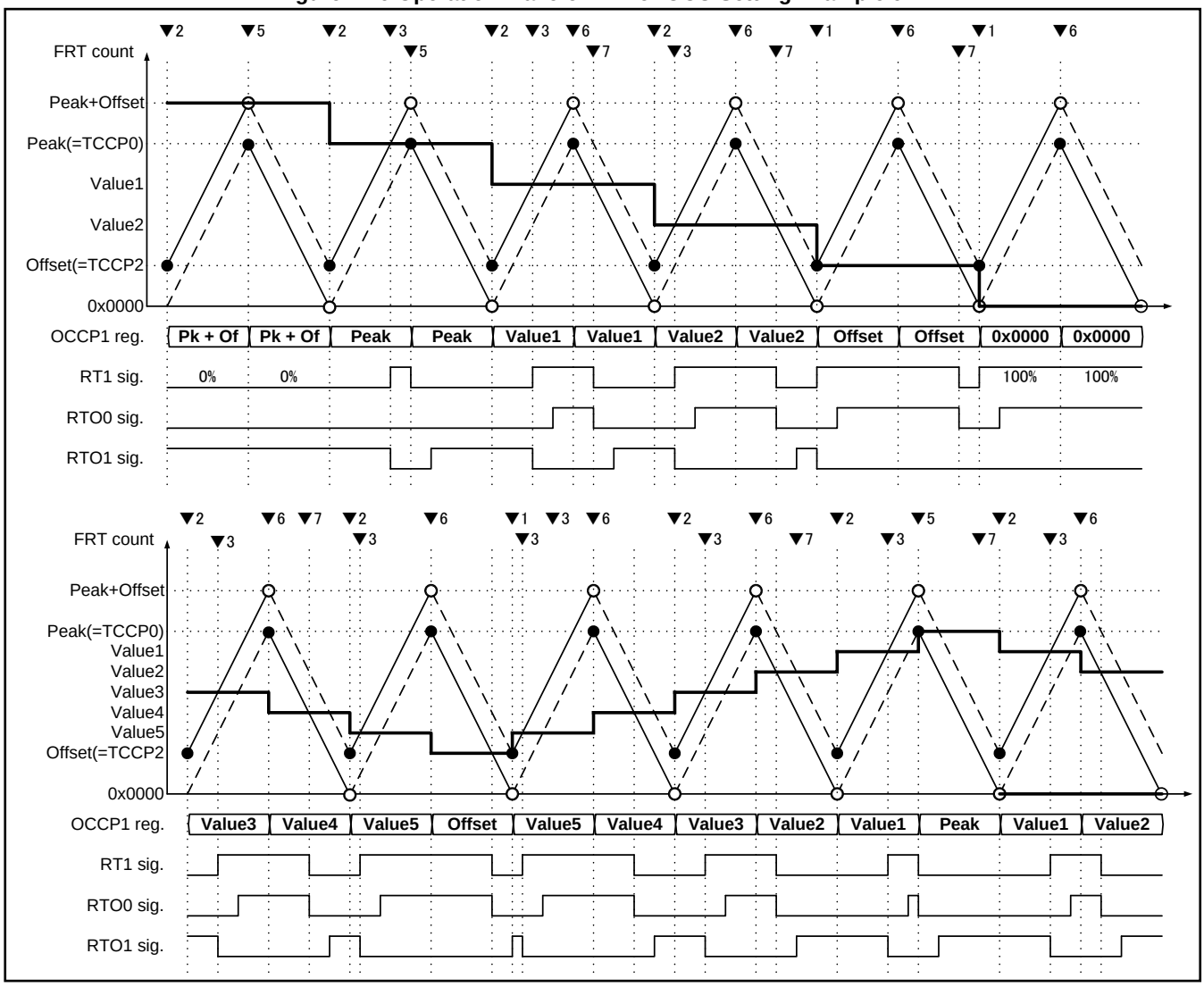


Figure 4-20 shows an example of an operation waveform when OCCP1 is set (Value 3 in the figure) within the range of 0x0000 < OCCP1 < Dead time. In this case, the RTO1 signal is changed to Low at the timing of ▼1. The RTO0 signal is changed to High at the timing of ▼2.

Figure 4-20 Operation Waveform 2 for OCU Setting Example 9

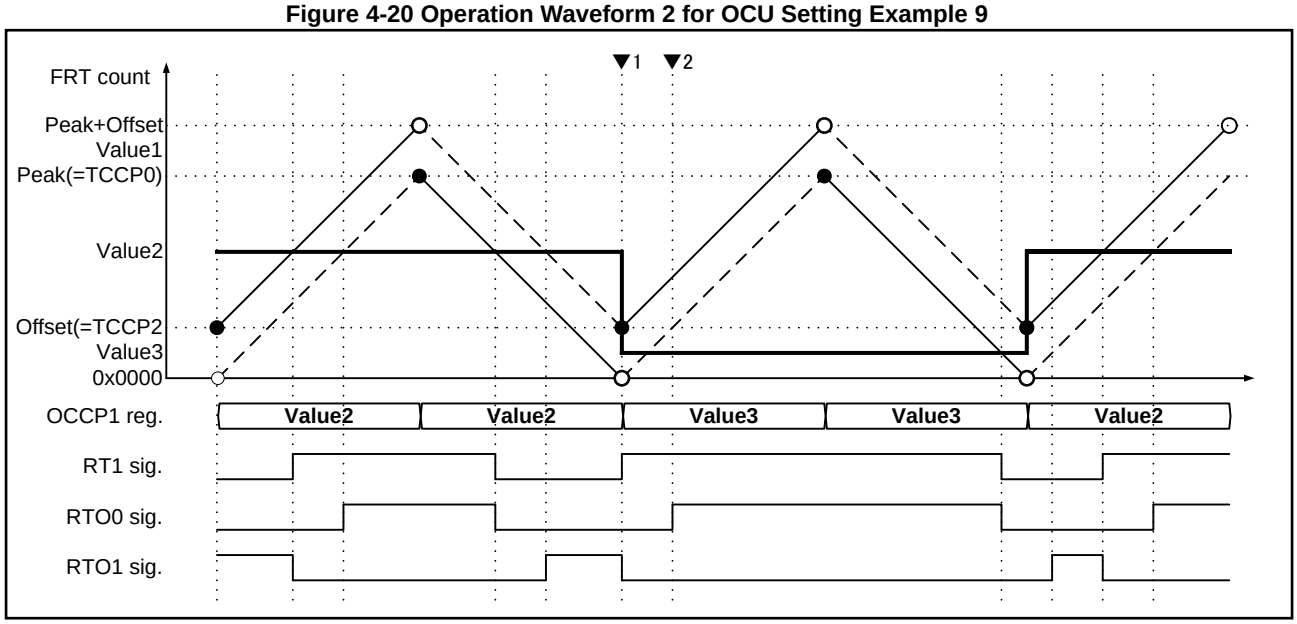
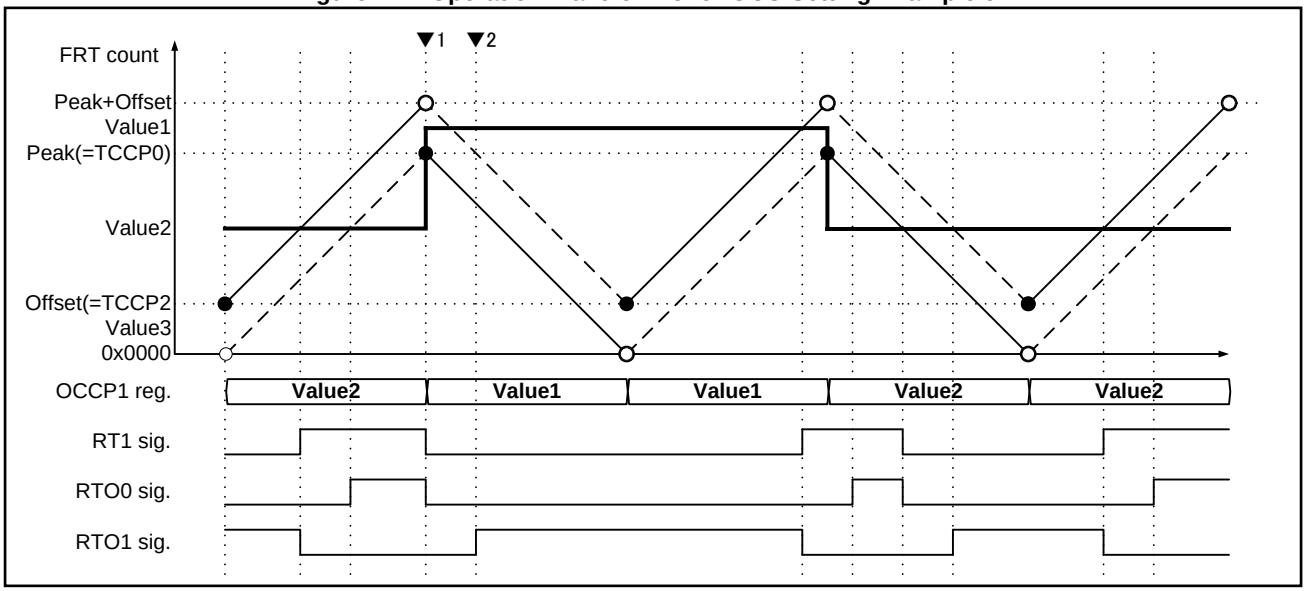


Figure 4-21 shows an example of an operation waveform when OCCP1 is set (Value 1 in the figure) within the range of Peak < OCCP1 < (Peak + Dead timer). In this case, the RTO0 signal is changed to Low at the timing of ▼1. The RTO1 signal is changed to High at the timing of ▼2.

Figure 4-21 Operation Waveform 3 for OCU Setting Example 9



4.2.3 Channel-linked Operation

This section describes output waveform generation operation during linked operation of OCU-ch(0) and OCU-ch(1). During linked operation, the two values OCCP(0) and OCCP(1) are used to control the RT(1) output signal on the ch.(1) side. Linked operation of the RT(0) signal on the ch.(0) side is not possible.

For linked operation, ch.(0) and ch.(0) must be connected to the same FRT. The same settings does not need to be made for the buffer-send specification. Zero-send can be specified for ch.(0) and Peak-send for ch.(1).

Interrupt cannot be generated upon detection of a match between OCCP(0) and the FRT in ch.(1). To set IOP0 by a match between OCCP(0) and the FRT, ch.(0) operation permission as CST0=1 must be set. To use the RT(1) output signal only without using the RT(0) output signal and IOP0, CST0=1 need not be set.

4.2.3.1 List of Setting Examples

A list of initial set values for setting examples 9 and 10 is shown in Table 4-16.

Table 4-16 Setting Examples for OCU ch.0 and ch.1 Linked Operation

Setting Description	Setting Register	Setting Example 10	Setting Example 11
FRT Mode	TCSA0:MODE	0	1
FRT Selection	OCFS10:FSO0 OCFS10:FSO1	0000 0000	0000 0000
OCCP0、OCCP1 Buffer function	OCSD10:OCCP0BUFE OCSD10.OPBM0 OCSD10:OCCP1BUFE OCSD10.OPBM1	01 0 01 0	01 0 01 0
OCSE0、OCSE1 Buffer function	OCSD10:OCSE0BUFE OCSD10.OEBM0 OCSD10:OCSE1BUFE OCSD10.OEBM1	00 0 00 0	00 0 00 0
FM4mode selection	OCSB10.FM4	1	1
ch.0 working condition	OCSE0 [15:0] OCSD10.OFEX0	0x000F 0	0x0000 0
ch.1 working condition	OCSE1[15:0] OCSE1[31:16] OCSD10.OFEX1	0x0FFF 0xFFFF 0	0x98A0 0x55A4 0
Interrupt	OCSA10:IOE0 OCSA10:IOE1	As required	As required
Output level	OCSB10:OTD0 OCSB10:OTD1 OCCP0 OCCP1	Specify an initial value	Specify an initial value

4.2.3.2 Operation for Setting Example 10

RT1, IOP1, RT0, IOP0 operations at the control timings in setting example 10 are shown in Table 4-17. The output waveform chart is shown in Figure 4-22. The ▲ mark indicates IOP0, IOP1 set timings.

The FRT operates in the up-count mode. The write values for OCCP0 and OCCP1 buffers from the CPU are provisionally stored in the buffer registers and sent to each register when the FRT is 0x0000. New data sent is targeted for comparison from FRT=0x0000. In this setting example, RT1 output is inverted when either OCCP0 or OCCP1 match. IOP1 is set when OCCP1 and the FRT match and IOP0 when OCCP0 and the FRT match. In this example, to set IOP0, CST0=1 must be set and ch.0 linked operation enabled.

At timings ▼1, ▼2, ▼3, ▼5, ▼6 in the chart, the parameters shown in the control parameter number column in the table have been satisfied. At other timings, parameter 4 has been satisfied. RT0 signal output and IOP0 operate in accordance with the respective specifications. Because the FRT operates in the up- count mode, parameters 7 and 8 are not satisfied.

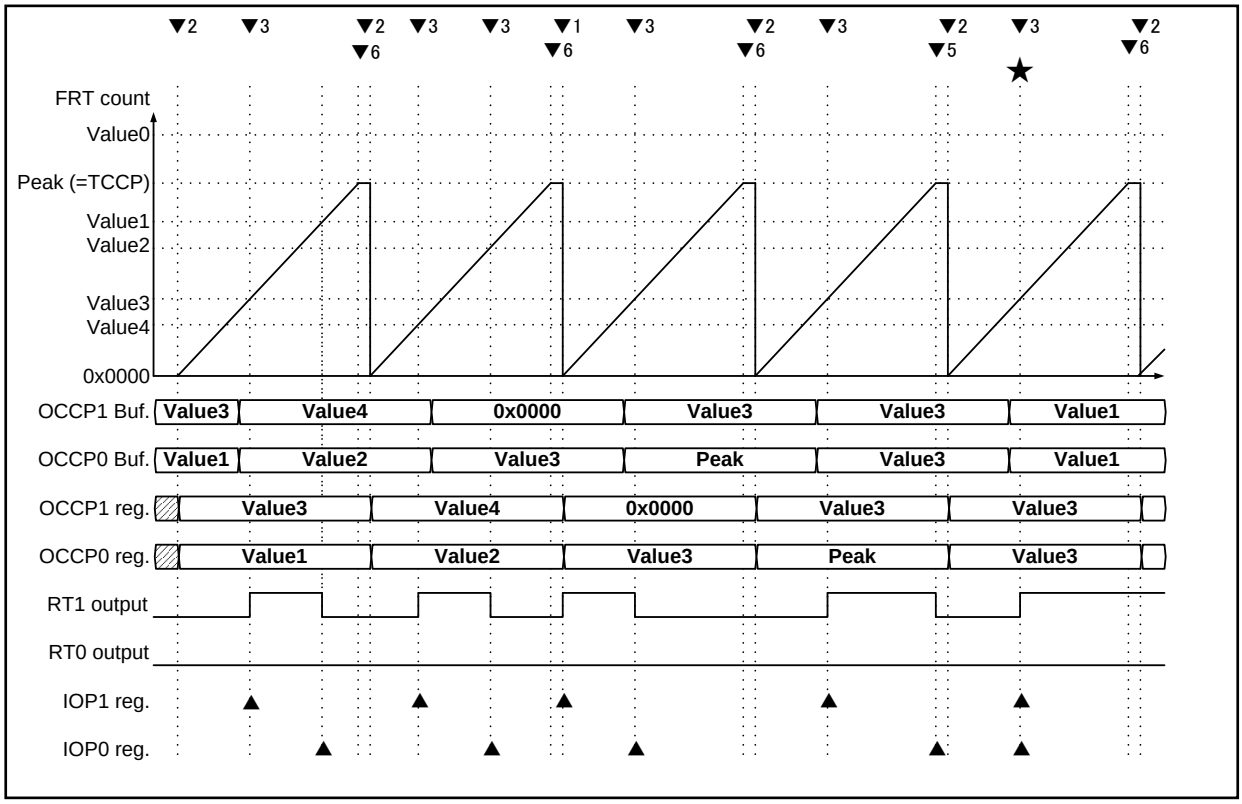
In this setting example, output level is inverted when match is simultaneously detected for OCCP0 and OCCP1 (timing ★) Operation can be changed when match is simultaneously detected for OCCP0 and OCCP1 by setting change for OCSE1 register.

In this setting example, when OCCP is included in the following range, the output signal is not changed.. The peak value < OCCP ≤ 0xFFFF..

Table 4-17 Content of OCU Operation in Setting Example 10

Control Parameter				Setting Example 10 OCSE1=0xFFFF0FFF, OCSE0=0x000F			
FRT Value	**OCCP1 Comparison Result**	**OCCP0 Comparison Result**	**Parameter Number**	**RT1 Operation**	**IOP1 Operation**	**RT0 Operation**	**IOP0 Operation**
Zero/Bottom	Match	Match	1	Reverse	Set	Hold	Set
	Match	Mismatch		Reverse			Hold
	Mismatch	Match		Reverse	Hold		Set
	Mismatch	Mismatch	2	Hold			Hold
Up	Match	Match	3	Reverse	Set		Set
	Match	Mismatch		Reverse			Hold
	Mismatch	Match		Reverse	Hold		Set
	Mismatch	Mismatch	4	Hold			Hold
Peak	Match	Match	5	Reverse	Set		Set
	Match	Mismatch		Reverse			Hold
	Mismatch	Match		Reverse	Hold		Set
	Mismatch	Mismatch	6	Hold			Hold
Down	Match	Match	7	Reverse	Set		Set
	Match	Mismatch		Reverse			Hold
	Mismatch	Match		Reverse	Hold		Set
	Mismatch	Mismatch	8	Hold			Hold

Figure 4-22 Waveforms during OCU Setting Example 9 Operation



4.2.3.3 Operation for Setting Example 11

RT1, IOP1, RT0 and IOP0 operations at the control timings in setting example 11 are shown in Table 4-18. The output waveform chart is shown in Figure 4-23.

In setting example 11, an asymmetrical Active-High waveform is output centered on the same FRT peak value as in setting examples 4 and 8. In addition, when 0x0000, peak value (or 0xFFFF) are specified for OCCP0, OCCP1, unprocessed output is implemented. Unlike setting examples 4 and 8, the two values OCCP0 and OCCP1 are used.

In setting example 11, when the FRT is 0x0000 in the up-count mode, the OCCP1 value is ignored and RT1 output changed only when OCCP0 and the FRT match. When the FRT is at peak in the down-count mode, the OCCP0 value is ignored and RT1 output changed only when OCCP1 and the FRT match. As shown in the comments column in the table, this kind of operation can be implemented by specifying the same OCCP match/mismatch parameter settings for the OCCP on the side where comparison results are ignored.

In this setting example, RT1 change timing can be specified by OCCP0 in the first half of the FRT count and by OCCP1 in the second half. Control by from the CPU can be implemented only when a zero detection interrupt from the FRT is generated. Unlike setting examples 4 and 8, the CPU interrupt processing count can be reduced.

The FRT operates in the up-down count mode. The OCCP0, OCCP1 write values from the CPU are temporarily stored in buffer registers and sent to the OCCP0 and OCCP1 registers upon FRT zero detection. New data sent is targeted for comparison from FRT=0x0000. Since the RT0 output signal and IOP0 are not set in the example, CST0=1 need not be specified.

At timings ▼1, ▼2, ▼3, ▼5, ▼6, ▼7in the chart, the control parameters for each parameter number column in the table have been satisfied. At other timings, either parameter 4 or 8 has been satisfied. RT1 signal output operates in accordance with the respective specifications.

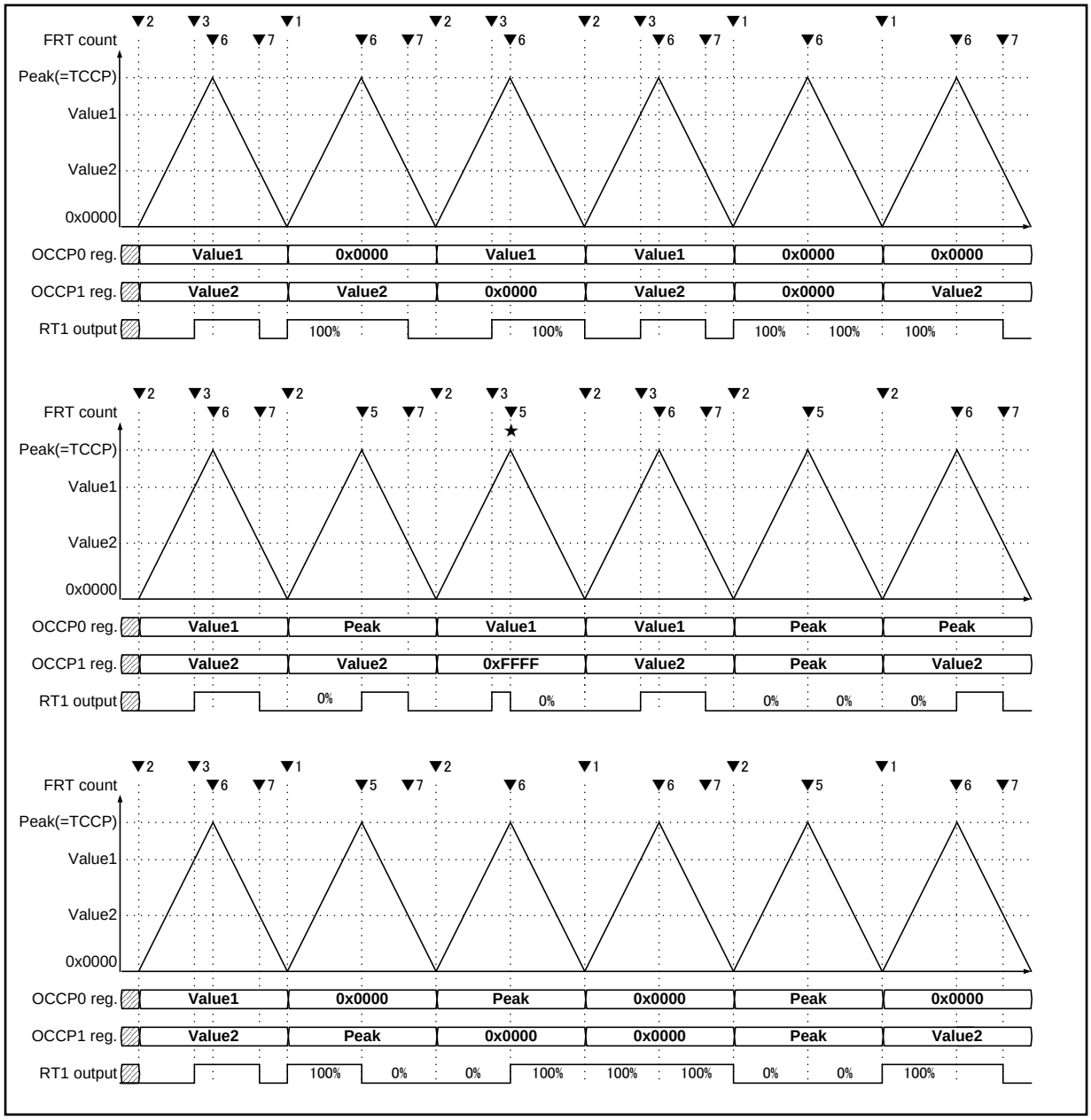
Because the FRT operates in the up-down count mode at timing ★ in the figure, OCCP1=0xFFFF is handled as the peak. Parameter 5 operation is implemented.

In this setting example, when OCCP is included in the following range, the output signal is not changed. The peak value < OCCP0 < 0xFFFF.

Table 4-18 Content of Operation in OCU Setting Example 11

Control Parameters				Setting Example 11 OCSE1=0x55A498A0, OCSE0=0x0000				
FRT Value	OCCP1 Comparison Result	OCCP0 Comparison Result	Parameter Number	RT1 Operation	IOP1 Operation	Comments	RT0 Operation	IOP0 Operation
0x0000	Ignored	Match	1	Set	Hold	Bit[27:26]=Bit[31:30]	Hold	Hold
		Mismatch	2	Reset		Bit[11:10]=Bit[15:14]		
Up		Match	3	Set		Bit[25:24]=Bit[19:18]		
		Mismatch	4	Hold		Bit[9:8]=00(Hold)		
Peak	Match	Ignored	5	Reset		Bit[23:22]=Bit[7:6]		
	Mismatch		6	Set		Bit[29:28]=Bit[13:12]		
Down	Match		7	Reset		Bit[21:20]=Bit[5:4]		
	Mismatch		8	Hold		Bit[17:16]=00(Hold)		

Figure 4-23 Waveforms during OCU Setting Example 10 Operation



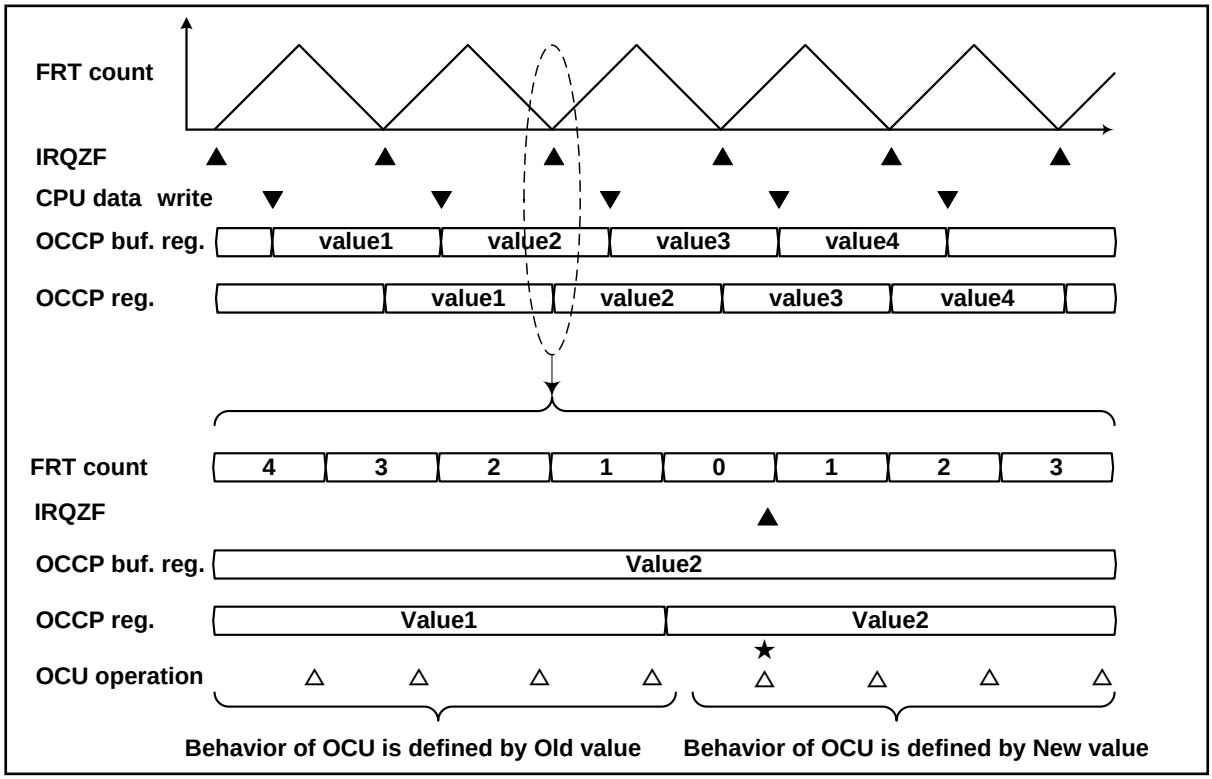
4.2.4 OCU Buffer Data Transfer

The OCCP register and OCSE register have a buffer function. When the buffer function is enabled, data written to OCCP and OCSE from the CPU during the count operation by FRT is written to the buffer register. Then, the data is transferred to the respective registers at the specified transfer timing.

When FRT interrupt mask linked transfer is off, the buffer transfer is performed at the specified FRT count status. There is no effect by the FRT interrupt mask counter.

An operation example when the OCCP buffer function is enabled, Zero/Bottom transfer is performed, and (OCSD.OCCPBUFE=01) FRT interrupt mask linked transfer is off (OCSD.OPBM=0) is shown in Figure 4-24.

Figure 4-24 OCU Buffer Data Transfer (Interrupt Mask Link Off)



The top section in the figure shows the entire view, and the bottom section shows an enlarged view of the transfer operation section. FRT performs the count operation in up/down-count mode. A zero detection interrupt is generated from FRT at the timing indicated by ▲. At the timing of ▼, the OCCP buffer register is overwritten from the CPU. The written data is stored in the OCCP buffer register. Then, whenever the FRT zero is detected, the transfer operation to the OCCP register is performed, and an interrupt is generated.

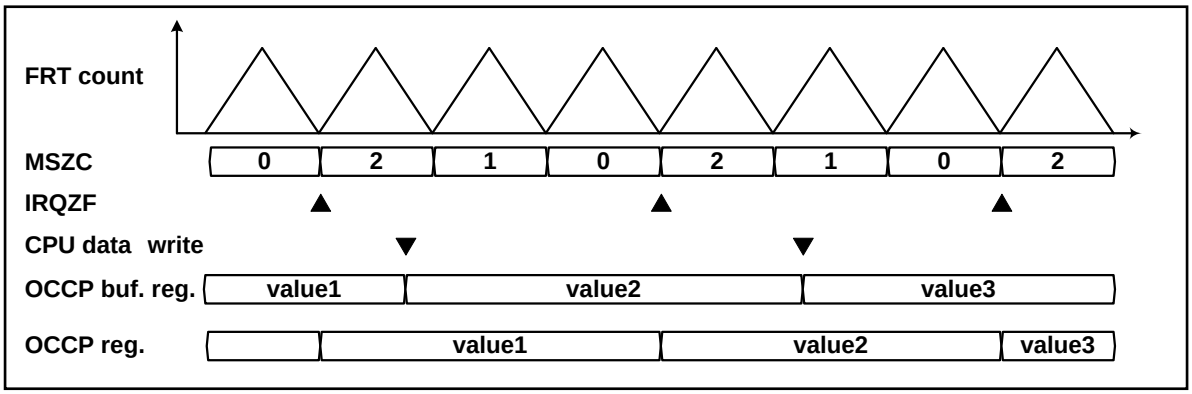
OCU performs the operation to change the RT output signal and IOP register based on the specified OCCP register setting at the timing of △. OCU operation from the timing of ★ (FRT=0x0000) is performed based on the new data after OCCP transfer. OCU operation before this timing is performed based on the old data before OCCP transfer. In this way, the OCU uses the transferred data starting from the transfer timing.

The figure shows an example of OCCP Zero/Bottom transfer, but the OCSE buffer transfer operation and Peak/Top transfer also perform the same operation. In all of these cases, the transferred data is used starting from the transfer timing.

When FRT interrupt mask linked transfer is turned on (OCSD.OPBM=1), buffer transfer is performed when the connected FRT is the specified count status and the FRT interrupt mask counter is 0.

An operation example when the OCCP buffer function is enabled, Zero/Bottom transfer is performed, and (OCSD.OCCPBUFE=01) FRT interrupt mask linked transfer is on (OCSD.OPBM=1) is shown in Figure 4-25.

Figure 4-25 OCU Buffer Transfer (Interrupt Mask Link On)



FRT performs the count operation in up/down-count mode. The zero detection interrupt mask counter (MSZC) counts down from 2 to 0. A zero detection interrupt is generated from FRT at the timing indicated by ▲. At the timing of ▼, the OCCP buffer register is overwritten from the CPU. The written data is stored in the OCCP buffer register. Then, whenever the FRT zero is detected while the zero detection interrupt mask counter is 0, the transfer operation to the OCCP register is performed, and an interrupt is generated.

Like the bottom section of Figure 4-24, the transferred data is used for operation from the time of the FRT count. As described above, the number of OCCP buffer transfer operations can be reduced by linking with the FRT interrupt mask counter.

If the connected FRT is count mode with offset (ch.1 or ch.2), this FRT interrupt mask counter value is fixed at 0. However, the interrupt mask counter value used in determination of the buffer transfer conditions uses the interrupt mask counter value of the FRT-ch.0 where the count is operating in synchronization with this FRT. As a result, the buffer transfer operation can be performed by linking with the FRT interrupt mask counter even if the connected FRT is in count mode with offset.

Note:

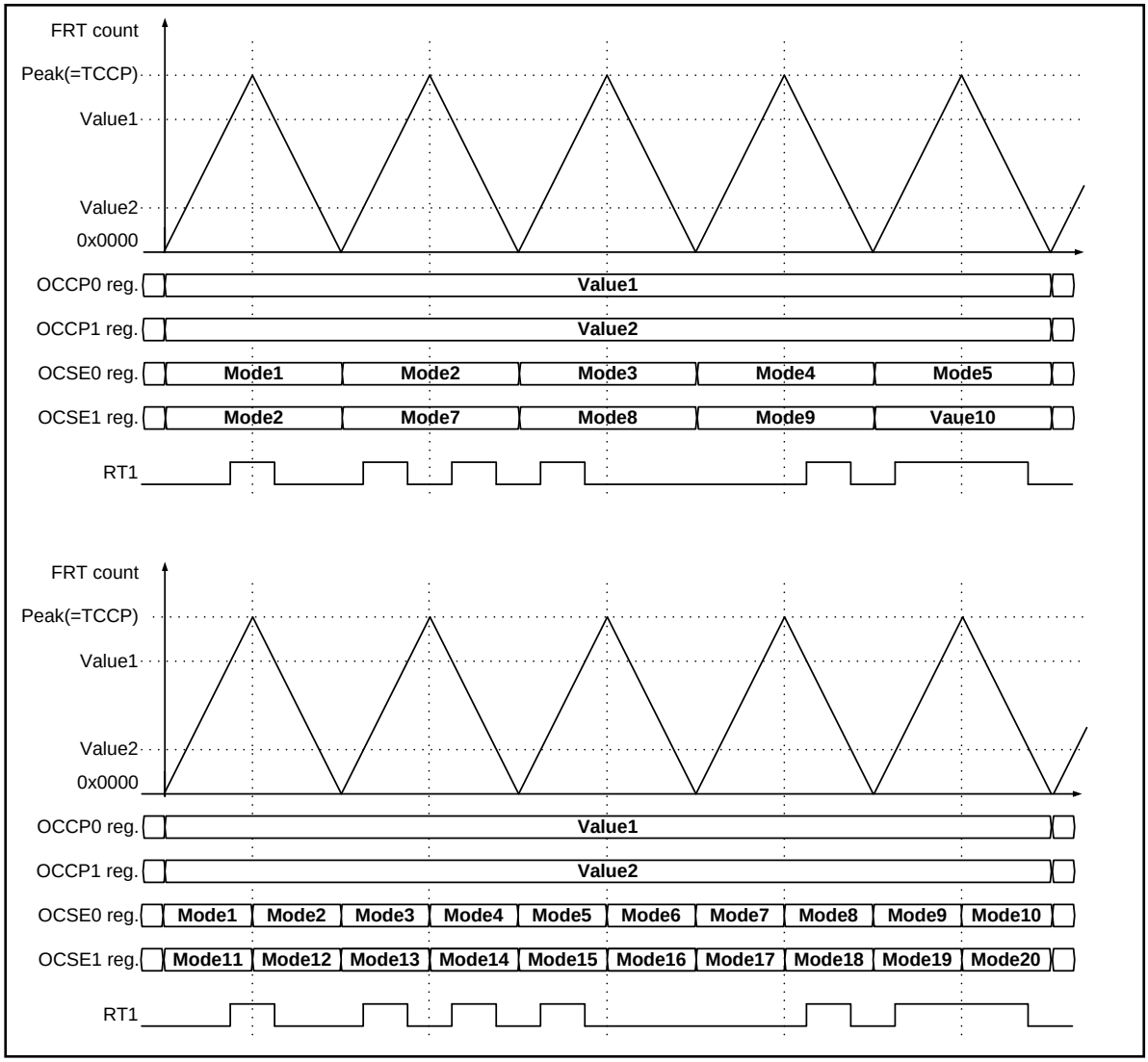
- *The buffer transfer function linked to the FRT interrupt mask counter is available in TYPE3-M4 products and later only. It cannot be used in TYPE1-M4 and TYPE2-M4 products.*

4.2.5 OCSE Buffer Function

OCSE registers are furnished with a buffer function. The OCSE register buffer function can be used to change the RT(0) and RT(1) output signal change parameters to synchronize with FRT zero detection and peak detection during FRT operation. Use of the OCCP(0) and OCCP (1) buffer functions in combination with the value comparison link function enables generation of various PWM waveforms.

Figure 4-26 shows an example where the output waveform is generated by not changing the register values of OCCP(1) and OCCP(2), rewriting only values in OCSE register and changing output modes.

Figure 4-26 OCU OCSE Register Buffer Function



4.3 OCU FM3 Family Product-compatible Operation

OCU FM3 Family product-compatible operation is described below.

4.3.1 OCU FM3 Family Product-compatible Operation

When the OCU is set to OCSB.FM4=0, the operation mode is selected by the value set in the OCSB.CMOD register and the OCSC.MOD register. The value set in the OCSE register is ignored. Set register values and OCU ch.(0), OCU ch(1) operation modes are shown in Table 4-19. Operation in each of the modes is identical to that in setting examples described in 4.1 Descriptions of FRT Operation The existence/absence of OCCP register buffer functions and send timing specifications are not compatible with FM3 Family products. Even if OCSB.FM4=0, the setting is made by the OCSD register during initial settings.

Table 4-19 FM3 Family Product-compatible Operation

Register Settings				Content of Operation in the Selected Operation Mode	
TCSA: MODE ch.(1) (*1)	**TCSA: MODE ch.(0) (*2)**	**OCSB: CMOD (*3)**	**OCSC: MOD (*4)**	**CH(1) Operation Mode**	**CH(0) Operation Mode**
0	0	0	00	Up-count mode (1 change) (OCU setting mode 5 operation)	Up-count mode (1 change) (OCU setting mode 1 operation)
0	0	1	00	Up-count mode (2 changes) (OCU setting mode 5 or 9 operation) (*5)	Up-count mode (1 change) (OCU setting mode 1 operation)
0	1	0	01	Up-count mode (1 change) (OCU setting mode 5 operation)	Up-down count mode (Active High) (OCU setting mode 2 operation)(*6)
1	0	0	10	Up-down count mode (Active High) (OCU setting mode 6 operation)(*6)	Up-count mode (1 change) (OCU setting mode 1 operation)
1	0	1	10	Up-down count mode (Active Low) (OCU setting mode 7 operation)(*6)	Up-count mode (1 change) (OCU setting mode 1 operation)
1	1	0	11	Up-down count mode (Active High) (OCU setting mode 6 operation)(*6)	Up-down count mode (Active High) (OCU setting mode 2 operation)(*6)
1	1	1	11	Up-down count mode (Active Low) (OCU setting mode 7 operation)(*6)	Up-down count mode (Active Low) (OCU setting mode 3 operation)(*6)

*1: TCSA:MODE ch.(1) shows the TCSA:MODE value of the FRT connected to OCU ch.(1).

*2: TCSA:MODE ch.(0) shows the TCSA*MODE value of the FRT connected to OCU ch.(0).

*3: OCSB:CMOD shows the OCSB10:CMOD value for ch.1-ch.0, the OCSB32:CMOD value for ch.3-ch.2 and the OCSB54:CMOD value for ch.5-ch.4.

*4: OCSC:MOD shows the OCSC:MOD[1:0] value for ch.1-ch.0, the OCSC:MOD[3:2] value for ch.3-ch.2 and the OCSC:MOD[5:4] value for ch.5-ch.4.

*5: When OCSA.CST0=0, RT(1) output and IOP1 operation is in accordance with OCU setting example 5. WhenOCSA.CST0=1, RT(1) output and IOP1 operation is in accordance with OCU setting example 10. ch.(0) and ch(1) are connected to the same FRT.

*6: OCSD register specification should be used to enable the OCCP buffer function and zero value-send. If the buffer function is disabled or peak value-send is specified, FM3 Family product compatible operation will not be executed.

*7: Compatible operation will not be executed with combinations of TCSA.MODE, OCSB:CMOD, OCSC:MOD[5:0] other than the above.

4.4 Description of WFG Operation

This section explains the output waveform of WFG in each mode.

4.4.1 WFG Control Register

The WFG control registers are shown in Table 4-20. An overview of the register functions and setting timing are also provided in this table.

Table 4-20 WFG Control Registers

Setting Register	Register Function	Register Change Timing
WFSA:DCK WFSA:TMD WFSA:GTEN WFSA:PSEL WFSA:PGEN WFSA:DMOD	Sets clock frequency division ratio Selects WFG operation mode Selects CH_GATE signal output conditions Selects CH_PPG signal input source Selects CH_PPG signal input apply conditions Selects RTO output signal polarity	Set before OCU and PPG operation allowed. Changing of the settings is prohibited after changing to an operation allowed status.
WFTA, WFTB	Sets WFG timer time	Any user-selected timing
WFTF	Sets pulse counter value	

WFG operates according to the setting of WFSA register. Complete initial setting before RT0 and RT1 signals from OCU which are input signals of WFG, and the PPG signal from PPG are input (before operation of OCU and PPG is enabled). If operation mode is selected by WFSA register, the initial output level of RTO0 to RTO5 output signal and GATE signal are determined.

4.4.2 List of CH_GATE Signal Output Details

Table 4-21 shows a list of WFG operation modes, CH_GATE signal output details by register settings.

Table 4-21 List of Details of CH_GATE Signal Output Details

Operation Mode	WFSA: TMD[2:0]	WFSA: GTEN[1:0]	CH_GATE Signal Output
Through mode	000	don't care	Always outputs Low-level signals
RT-PPG mode	001	00	Always outputs Low-level signals
		01	Outputs RT(0) signal
		10	Outputs RT(1) signal
		11	Outputs the logic OR signal of RT (1) signal and RT (0) signal.
Timer-PPG mode	010	00	Always outputs Low-level signals
		01	Outputs WFG timer active flag 0
		10	Outputs WFG timer active flag 1
		11	Outputs the logical OR signal of WFG timer active flag 1 and WFG timer active flag 0.
RT-dead timer mode	100	don't care	Always outputs Low-level signals
RT-dead timer filter mode	101	don't care	Always outputs Low-level signals
PPG-dead timer filter mode	110	00	Always outputs Low-level signals
		01	Outputs RT(0) signal
		10	Outputs RT(1) signal
		11	Outputs the logical OR signal of RT (1) signal and RT (0) signal.
PPG-dead timer mode	111	00	Always outputs Low-level signals
		01	Outputs RT(0) signal
		10	Outputs RT(1) signal
		11	Outputs the logical OR signal of RT (1) signal and RT (0) signal.

*: The CH_GATE signals in the table refer to CH10_GATE, CH32_GATE and CH54_GATE before being selected by WFSA:PSEL[1:0], as shown in Figure 3-4, Figure 4-57, Figure 4-58 Diagram of PPG Selection Circuit Configuration.

4.4.3 List of RTO0 to RTO5 Signal Output Details

Table 4-22 shows a list of WFG operation modes, register settings, RTO (1) signal, and RTO (0) signal output details.

Table 4-22 List of Output Details of RTO Pin

Operation Mode	WFSA: TMD [2:0]	WFSA: PGEN [1:0]	Output RTO (1) Signal	Output RTO (0) Signal
Through mode	000	00	Outputs RT (1) signal	Outputs RT (0) signal
		01	Outputs RT (1) signal	Outputs CH_PPG signal
		10	Outputs CH_PPG signal	Outputs RT (0) signal
		11	Outputs CH_PPG signal	Outputs CH_PPG signal
RT-PPG mode	001	00	Outputs RT(1) signal	Outputs RT (0) signal
		01	Outputs RT(1) signal	Outputs the logic AND signal of RT (0) signal and CH_PPG signal.
		10	Outputs the logic AND signal of RT (1) signal and CH_PPG signal.	Outputs RT (0) signal
		11	Outputs the logic AND signal of RT (1) signal and CH_PPG signal.	Outputs the logic AND signal of RT (0) signal and CH_PPG signal.
Timer-PPG mode	010	00	Output WFG timer active flag 1	Outputs WFG timer active flag 0
		01	Output WFG timer active flag 1	Outputs the logic AND signal of WFG timer active flag 0 and CH_PPG signal.
		10	Outputs the logic AND signal of WFG timer active flag 1 and CH_PPG signal.	Outputs WFG timer active flag 0
		11	Outputs the logic AND signal of WFG timer active flag 1 and CH_PPG signal.	Outputs the logic AND signal of WFG timer active flag 0 and CH_PPG signal.
RT-dead timer mode	100	don't care	Starts WFG timer from RT (1) signal and outputs the generated non-overlap signal.	
RT-dead timer filter mode	101	don't care	Performs pulse width filtering process via pulse counter to RT (1) signal. Starts WFG timer from the processed signal, and outputs the generated non-overlap signal.	
PPG-dead timer filter mode	110	don't care	Performs pulse width filtering process via pulse counter to CH_PPG signal. Starts WFG timer from the processed signal, and outputs the generated non-overlap signal.	
PPG-dead timer mode	111	don't care	Starts WFG timer from CH_PPG signal and outputs the generated non-overlap signal.	

*: The CH_PPG signals in the table refer to CH10_PPG, CH32_PPG and CH54_PPG selected by WFSA:PSEL[1:0], as shown in Figure 3-4, Figure 4-57, Figure 4-58 Diagram of PPG Selection Circuit.

The WFSA.DMOD[1:0] setting can be used to change the output polarity of the RTO(0) and RTO(1) signals in Table 4-22 as shown below regardless of the other WFSA register settings.

In the case of WFSA.DMOD[1:0] =00, RTO(0) and RTO(1) signals are output with normal polarity.
In the case of WFSA.DMOD[1:0] =01, RTO(0) and RTO(1) signals are output with reversed polarity.
In the case of WFSA.DMOD[1:0] =10, RTO(0) signal is output with reversed polarity, and RTO(1) signal is output with normal polarity.
In the case of WFSA.DMOD[1:0] =11, RTO(1) signal is output with reversed polarity, and RTO(0) signal is output with normal polarity.

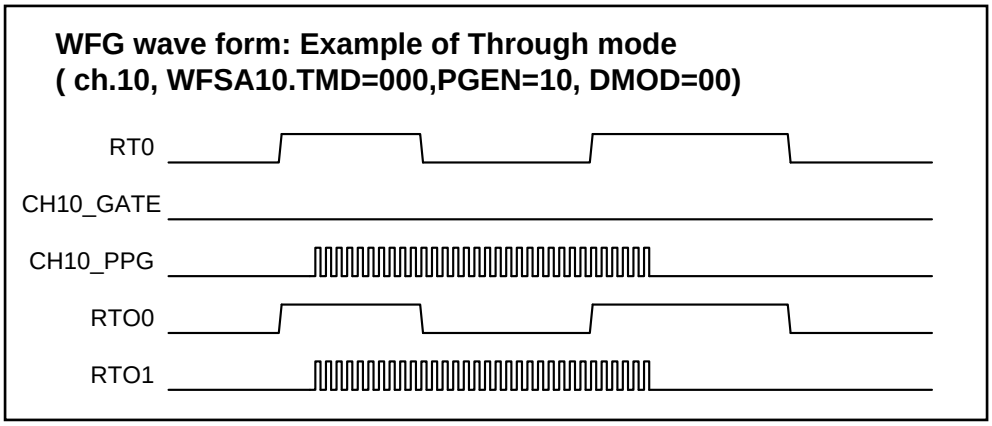
4.4.4 Through Mode

The operation in Through Mode (WFSA.TMD=000) is as follows

In this mode, the output of the CH_GATE signal is always fixed to the Low level. The RTO(1) and RTO(0) signals output the RT(1), RT(0), and CH_PPG signals through without change by PGEN[1:0] setting.

Figure 4-27 shows the example of the operation waveform in Through mode of WFG ch.10. In this example, the RT0 input signal and the CH10_PPG input signal are output through to RTO0 and RTO1 output signal, respectively. PPG timer unit can start outputting without the use of the GATE signal in this mode.

Figure 4-27 Example of Operation Waveform in WFG-Through Mode



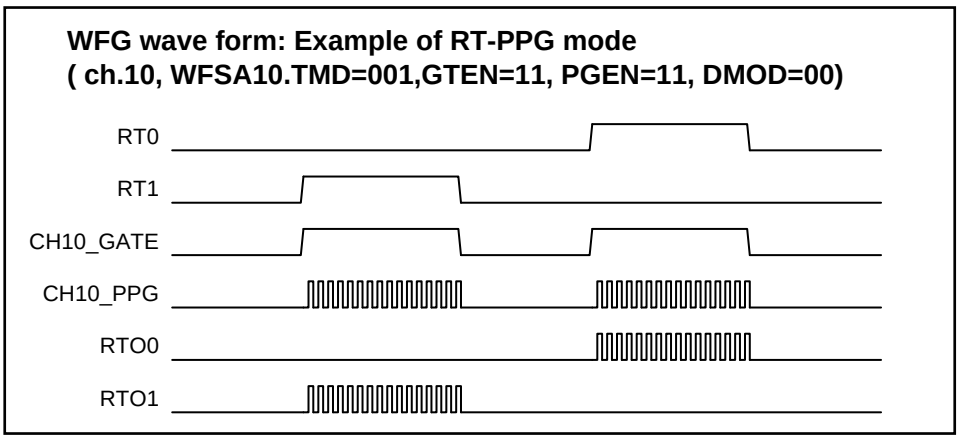
4.4.5 RT-PPG Mode

The operation in RT-PPG mode (WFSA.TMD=001) is as follows.

In this mode, the CH_GATE signal outputs the RT(1) signal, RT(0) signal or the logic OR signal of each signal by GTEN[1:0] setting. The RTO(1) and RTO(0) signals select and output the RT(1) signal, RT(0) signal, and the logic AND signal of CH_PPG signal by PGEN[1:0] setting.

Figure 4-28 shows an example of the operation waveform in RT-PPG mode of WFG ch.10. In this example, the CH10_GATE signal is generated from the logic OR signal of RT1 input and RT0 input to start PPG-ch.0. The CH10_PPG input signal, RT0 input and RT1 input undergo logic AND operation, is superimposed on RTO0 and RTO1 to output.

Figure 4-28 Example of Operation Waveform in WFG-RT-PPG Mode



4.4.6 Timer-PPG Mode

The operation in Timer-PPG mode(WFSA.TMD=010) is as follows.

Each channel of WFG has two flags: WFG timer active flag0 and WFG timer active flag1. This mode outputs a waveform using these flags.

When this mode is selected by rewriting to the WFSA.TMD register, WFG timer active flag0,1 are reset to 0 (Low level). When this mode is selected, irrespective of the input level of the RT(0) , RT(1) , and CH_PPG signals, the output level of RTO(0) and the RTO(1) is Low level.

When the rising edge of RT(0) signal is detected, WFG timer active flag 0 is to set to 1 and loads the initial value from the WFTA register and starts Down-count operation.

When the rising edge of RT(1) signal is detected, WFG timer active flag 1 is to set to 1 and loads the initial value from the WFTB register and starts Down-count operation.

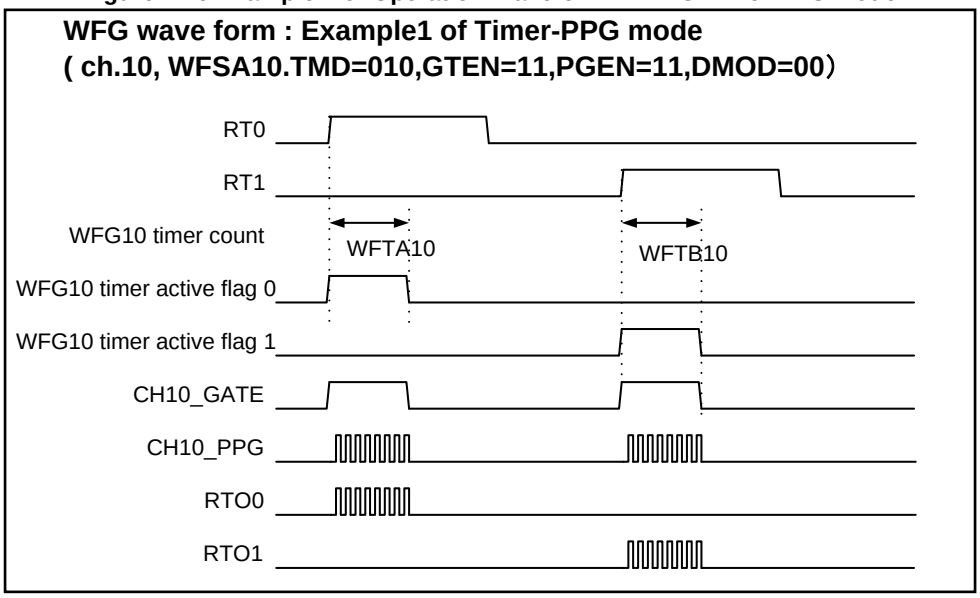
When the rising edge of RT(0) and RT(1) signals are detected at the same time, both of the WFG timer active flags are set to 1 and loads the initial value from the WFTA register and starts Down-count operation.

After counting, WFG timer resets both of the WFG timer active flags to 0. Therefore, irrespective of the pulse width of the RT(0) and RT(1) signals, the WFG timer flags0, 1 are set for the setting time of the WFG timer from the rising edge of each signal.

The CH_GATE signal selects and outputs WFG timer active flag 0, WFG timer active flag 1, or the logical OR signal of each signal by GTEN[1:0] setting. The RTO(1) and RTO(0) signals select and output either these two active flags or the logic AND signal of CH_PPG signal by PGEN[1:0] setting.

Figure 4-29 and Figure 4-30 show examples 1, and 2 of the operation waveform in Timer PPG mode of WFG ch.10.

Figure 4-29 Example 1 of Operation Waveform in WFG-Timer PPG Mode



In Figure 4-29, the rising of RT0 input and RT1 input starts WFG timer, and WFG10 timer active flag 0, and 1 are set to WFTA10 time and WFTB10 time respectively. These two logical OR signals generate CH10_GATE signal and start PPG ch.0. CH10_PPG input signal makes WFG10 timer active flag 0 and 1 to undergo the logical AND operation to output the RTO0 and RTO1. During timer operation, CH10_PPG input signal is superimposed on RTO0 and RTO1 to output.

Figure 4-30 is the example which sets up the time setting value of WFG timer (WFTA10, WFTB10) as longer than the pulse length of RT0 and RT1. Though RT0 signal and RT1 signal input the same signal as shown in Figure 4-29, it is indicated that the different output from that is shown in Figure 4-29 is achieved by timer setting value.

Figure 4-30 Example 2 of Operation Waveform in WFG-Timer PPG Mode

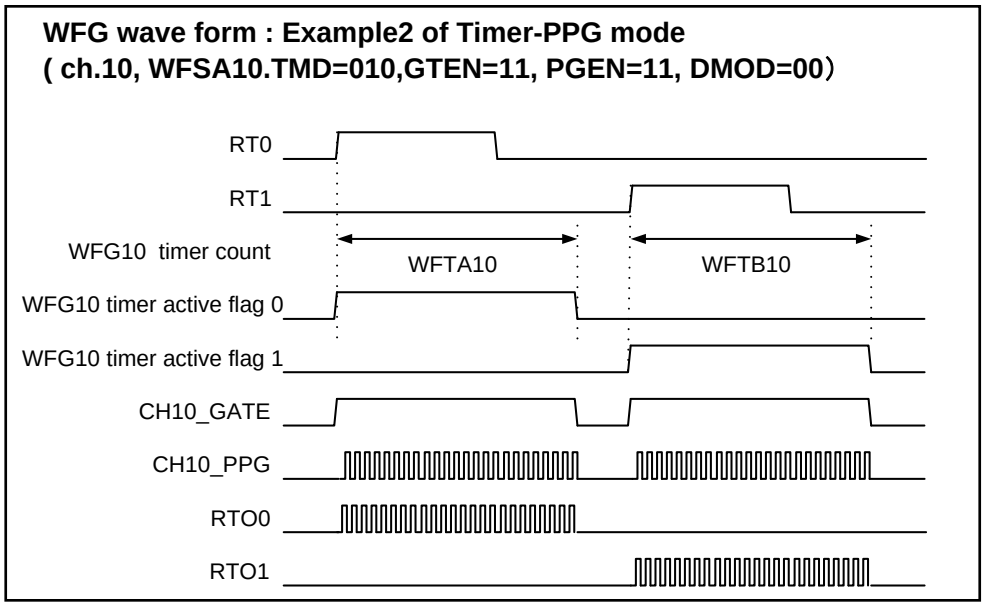


Figure 4-31 shows Example 3 of the operation waveform in Timer PPG mode of WFG ch.10.

Figure 4-31 Example 3 of Operation Waveform in WFG-Timer PPG Mode

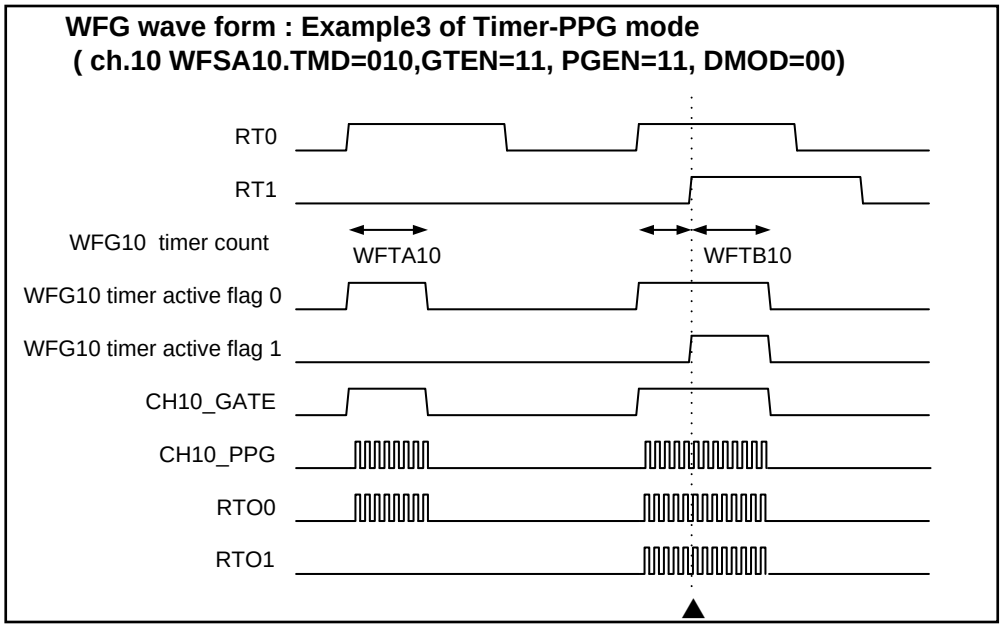


Figure 4-31 shows an exceptional case. The following operation is performed at the point indicated by ▲ in Figure 4-31. WFG timer active flag0 is set at the rising edge of the RT0 signal and WFG timer is in counting operation. In the meantime, the rising edge of the RT1 signal is detected and WFG10 timer

active flag1 is set. In this case, WFG timer reloads the initial value (WFTB10 register value) and performs the operation that will restart the timer count. Each WFG10 timer active flag 0 and flag 1 are reset, when the counting by WFG timer is completed. For this reason, the period in which WFG10 timer active flag0 is set becomes longer than the timer setting (WFTA10 register value), as shown in the Figure 4-31. Therefore, the output of the waveform shown in the Figure 4-31 can be achieved for RTO0 and RTO1.

4.4.7 RT-dead Timer Mode

The operation in RT-dead timer mode (WFSA.TMD=100) is as follows.

In this mode, the RTO(1) and RTO(0) signals output the non-overlap signal that has the dead time set by WFTA,WFTB register based on RT(1) signal. This mode assumes that the output polarity of OCU's RT(1) output is Active High. The output of the CH_GATE signal is always fixed to the Low level. In this mode, the value of the WFTF register, the RT(0) signal, and the CH_PPG signal are not used.

When this mode is selected by rewriting to the WFSA.TMD register, the RTO(0) signal is set to the same output level as for the RT(1) signal and the RTO(1) signal is set to the output level that is opposite from that of RT(1) signal.

If the rising edge of RT(1) signal is detected, RTO(1) signal output becomes Low level. WFG timer loads the value from WFTB register and starts counting the time. After counting, RTO(0) signal becomes High level.

When the falling edge of RT (1) signal is detected, RTO(0) signal output becomes Low level. WFG timer loads the value from WFTA register and starts counting the time. After counting RTO(1) signal becomes High level.

By WFTA register and WFTB register, the dead time of rising and falling side can be specified respectively.

Figure 4-32 shows Example 1 of the operation waveform in RT-dead timer mode of WFG ch.10.

Figure 4-32 Example 1 of Operation Waveform in WFG-RT-dead Timer Mode

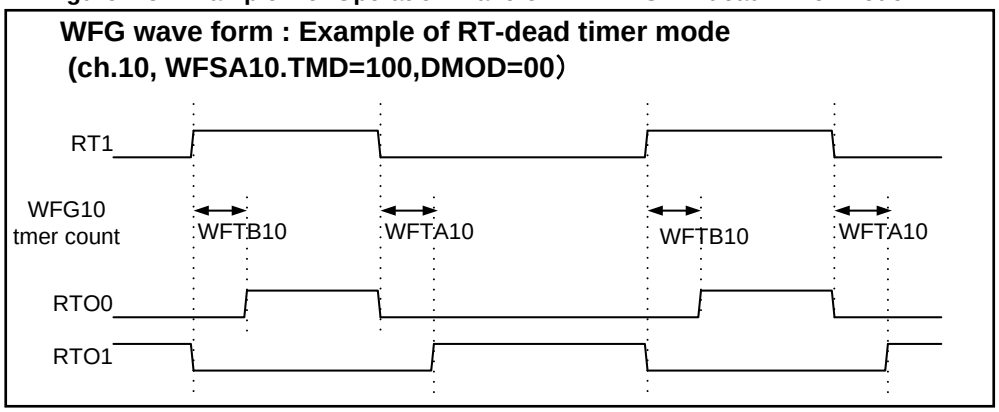
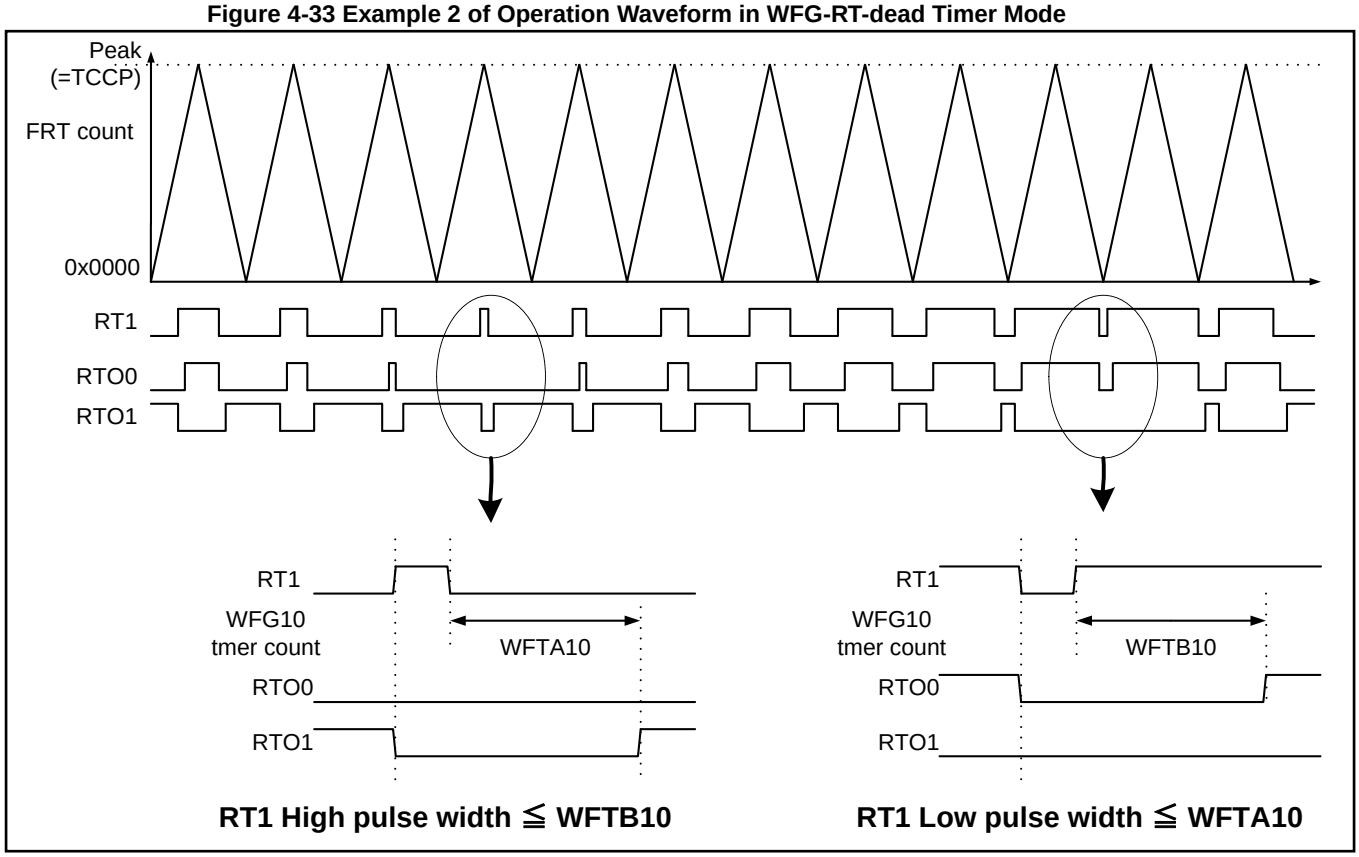


Figure 4-33 shows example 2 of the operation waveform in RT-dead timer mode of WFG ch.10.

When the High pulse width of the OCU's RT1 input signal is shorter than dead time set by WFTB10, only the RTO(1) output signal becomes Low level. RTO1 output signal becomes High level after rising of RT1 input signal and WFTA10 time. In this case, the signal waveform in which High level does not exist is output to RTO0 output signal.

When the Low pulse width of the RT1 input signal is shorter than dead time set by WFTA10, only the RTO(0) output signal becomes Low level. RTO0 output signal becomes High level after rising of RT1 input signal and WFTB10 time. In this case, the signal waveform in which High level does not exist is output to RTO1 output signal.

Figure 4-33 Example 2 of Operation Waveform in WFG-RT-dead Timer Mode



4.4.8 RT-dead Timer Filter Mode

Operation in RT-dead timer filter mode (WFSA.TMD=101) is as follows.

Using the pulse counter in WFG first, RT-dead timer filter mode filters RT(1) input signal which pulse length is shorter than WFTF register rated value. In the case that the pulse width of RT(1) input signal is longer than WFTF time, RT(1) input signal generates the filter signal which is delayed WFTF time. From this filter signal, non-overlap signal that maintains the dead time set by WFTA register and WFTB register is output to RTO(1) and RTO(0). The output of the CH_GATE signal is always fixed to the Low level. In this mode, the RT(0) signal and the CH_PPG signal are not used. This mode assumes that the output polarity of OCU's RT(1) output is Active High.

When this mode is selected by rewriting to the WFSA.TMD register, the RTO(0) signal is set to the same output level as for the RT(1) signal and the RTO(1) signal is set to the output level that is opposite from that of RT(1) signal.

When the rising edge of RT(1) signal is detected, the pulse counter loads the value from WFTF register and starts counting the High pulse width of RT(1) signal. In the case that the High pulse width is longer than WFTF time, RTO(1) signal output becomes Low level after WFTF time. WFG timer loads the value from WFTB register and starts counting the time. After counting, RTO(0) signal becomes High level.

When the falling edge of RT(1) signal is detected, the pulse counter loads the value from WFTF register and starts counting the Low pulse width of RT(1) signal. In the case that the Low pulse width is longer than WFTF time, RTO(0) signal output becomes Low level after WFTF time. WFG timer loads the value from WFTA register and starts counting the time. After counting, RTO(1) signal becomes High level.

In the case that the pulse width of RT(1) signal is shorter than WFTF time, the output of RTO(0) and RTO(1) do not change. And the dead time by the side of rising and falling can be specified respectively by WFTA register and WFTB register.

Figure 4-34 shows the example 1 of operation waveform in RT-dead timer filter mode of WFG ch.10.

Figure 4-34 Example 1 of Operation Waveform in RT-dead Timer Filter Mode

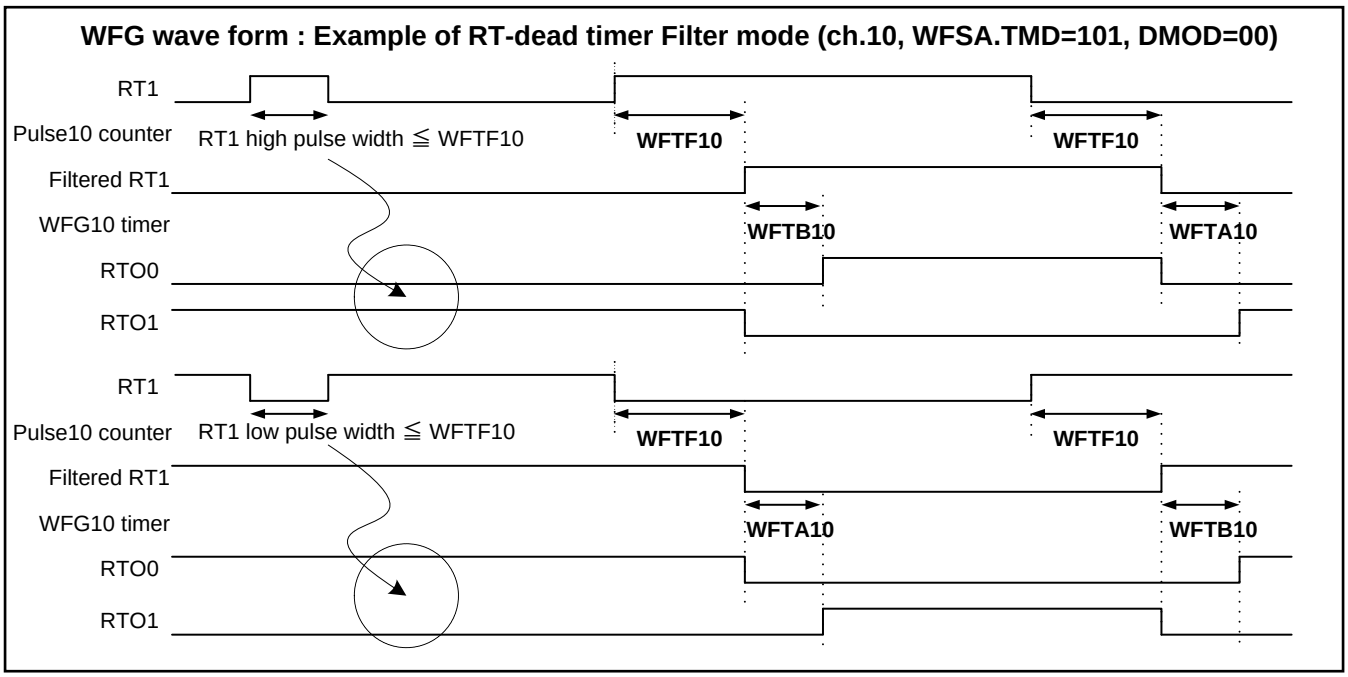
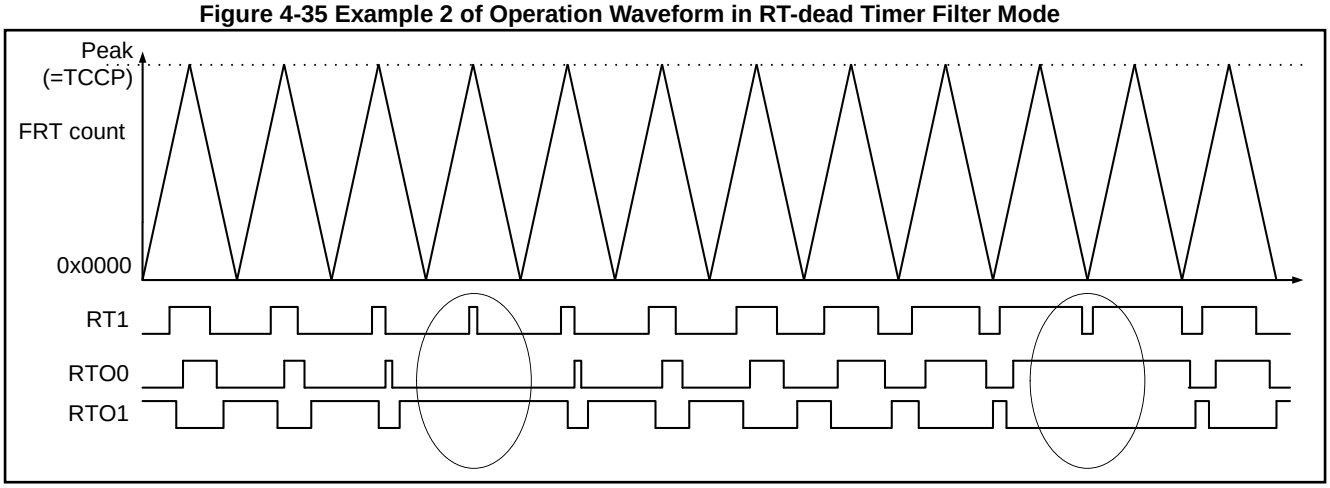


Figure 4-35 shows the example 2 of operation waveform in RT-dead timer filter mode. In the case that the pulse width of RT1 signal is shorter than WFTF10 time, RT1 signal is filtered and RTO0 output signal and RTO1 output signal do not change. In the case of the conditions of WFTF10≥WFTA10 and WFTF10 ≥WFTB10, output signal shown in the Figure 4-35 can be achieved for RTO0 and RTO1.

Figure 4-35 Example 2 of Operation Waveform in RT-dead Timer Filter Mode



4.4.9 PPG-Dead Timer Mode

The operation in PPG-dead timer mode (WFSA.TMD=111) is as follows.

In this mode, the RTO(1) and RTO(0) signals output the non-overlap signal that has the dead time set by WFTA,WFTB register based onCH_PPG signal. The CH_GATE signal selects and outputs the RT(1) signal, RT(0) signal or logic OR signal of each signal by GTEN[1:0] setting. The RT(0) and RT(1) signals are used only for the output of the CH_GATE signal. The value of the WFTF register is not used. This mode assumes that the output polarity of PPG output is Active High.

When this mode is selected by rewriting to the WFSA.TMD register, the RTO(0) signal is set to the same output level as for the CH_PPG signal and the RTO(1) signal is set to the output level that is opposite from that of CH_PPG signal.

When the rising edge of CH_PPG signal is detected, RTO(1) signal output become Low level. WFG timer loads the value from WFTB register and starts counting the time. After counting, RTO(0) signal becomes High level.

When the falling edge of the CH_PPG signal is detected, the RTO(0) signal output becomes Low level. WFG timer loads the value from the WFTA register and starts counting the time. After counting, RTO(1) signal becomes High level.

By the WFTA register and the WFTB register, the dead time of rising and falling side can be specified respectively.

Figure 4-36 shows example 1 of the operation waveform in PPG-dead timer mode of WFG ch.10.

Figure 4-36 Example 1 of Operation Waveform in WFG-PPG Dead Timer Mode

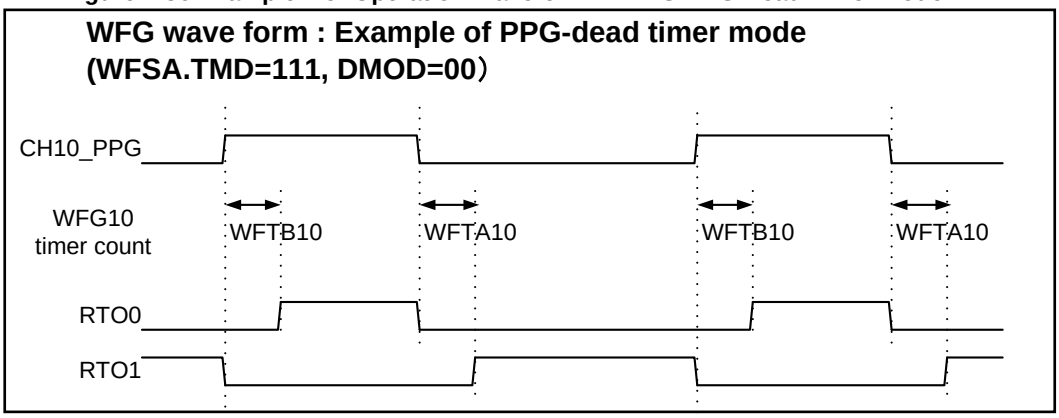
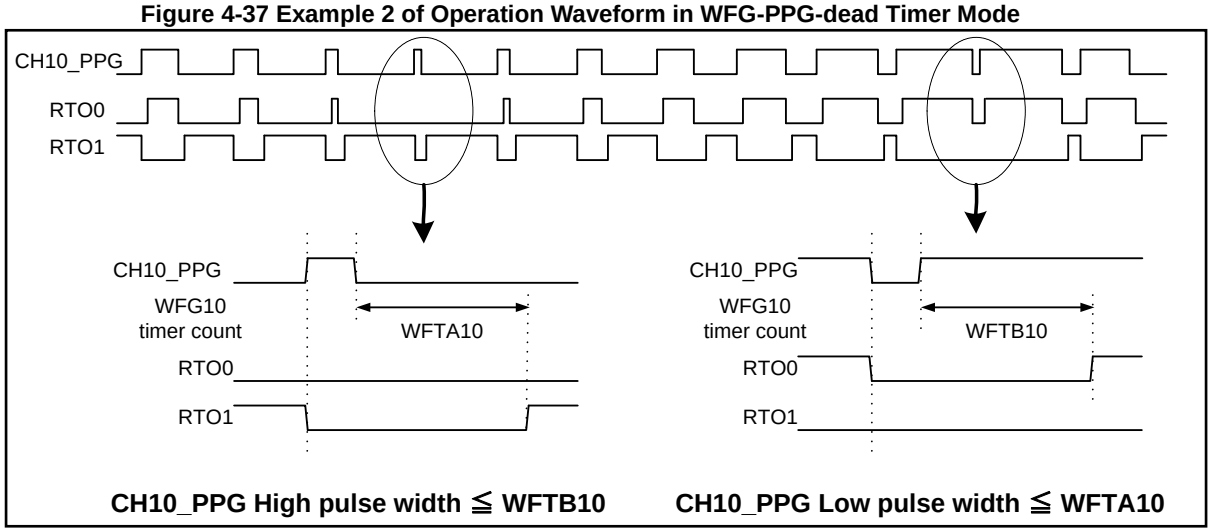


Figure 4-37 shows the example 2 of operation waveform in PPG-dead timer mode of WFG ch.10.

When the High pulse width of the CH10_PPG input signal is shorter than dead time set by WFTB10, only the RTO1 output signal becomes Low level. RTO1 output signal becomes High level after the rising of CH10_PPG input signal and WFTA10 time. In this case, the signal waveform in which High level does not exist is output to RTO0 output signal.

When the Low pulse width of the CH10_PPG input signal is shorter than the dead time set by the WFTA10, only the RTO0 output signal becomes Low level. RTO0 output signal becomes High level after the rising of CH10_PPG input signal and WFTB10 time. In this case, the signal waveform in which High level does not exist is output to RTO1 output signal.

Figure 4-37 Example 2 of Operation Waveform in WFG-PPG-dead Timer Mode



4.4.10 PPG-Dead Timer Filter Mode

The operation in PPG dead timer filter mode (WFSA.TMD=110) is as follows.

Using the pulse counter in WFG first, PPG dead timer filter mode filters CH_PPG input signal which pulse length is shorter than WFTF register rated value. In the case that the pulse width of CH_PPG input signal is longer than WFTF time, CH_PPG input signal generates the filter signal which is delayed WFTF time. From this filter signal, non-overlap signal that maintains the dead time set by WFTA register and WFTB register is output to RTO(1) and RTO(0). The CH_GATE signal selects and outputs the RT(1) signal, RT(0) signal or the logical OR signal of each signal by GTEN[1:0] setting. In this mode, the RT(0) signal and the RT(1) signal are only used for the output of CH_GATE signal. This mode assumes that the output polarity of PPG output is Active High.

When this mode is selected by rewriting to the WFSA.TMD register, the RTO(0) signal is set to the same output level as for the CH_PPG signal and the RTO(1) signal is set to the output level that is opposite from that of CH_PPG signal.

When the rising edge of the CH_PPG signal is detected, the pulse counter loads the value from the WFTF register and starts counting High pulse width of CH_PPG signal. In the case that High pulse width is longer than WFTF time, the RTO(1) signal output becomes Low level after WFTF time. WFG timer loads the value from the WFTB register and starts counting the time. After counting, RTO(0) signal becomes High level.

When the falling edge of the CH_PPG signal is detected, the pulse counter loads the value from the WFTF register and starts counting Low pulse width of CH_PPG signal. In the case that Low pulse width is longer than WFTF time, the RTO(0) signal output becomes Low level after WFTF time. WFG timer loads the value from the WFTA register and starts counting the time. After counting, RTO(1) signal becomes High level.

When the pulse width of the CH_PPG signal is shorter than WFTF time, RTO(0) and a RTO(1) output do not change. And the dead time of rising and falling side can be specified by the WFTA register and WFTB register, respectively.

Figure 4-38 shows the example 1 of operation waveform in PPG-dead timer filter mode of WFG ch.10.

Figure 4-38 Example 1 of Operation Waveform in WFG PPG-Dead Timer Filter Mode

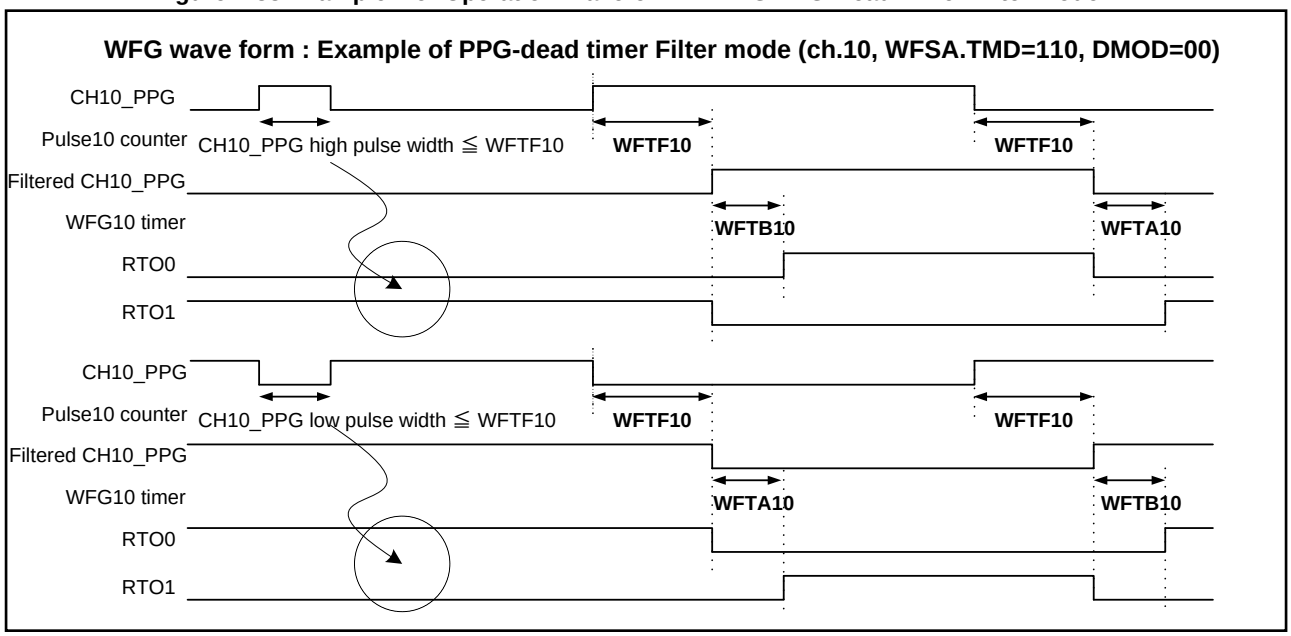
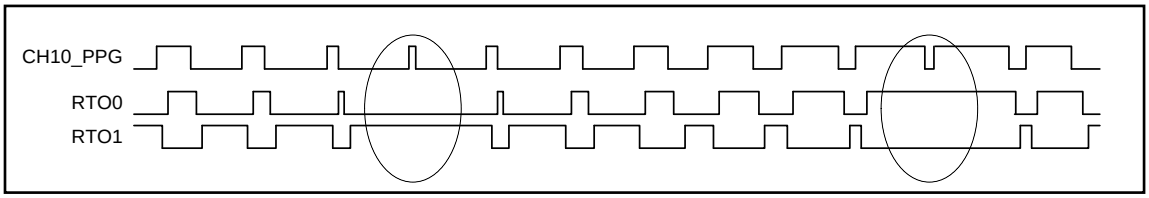


Figure 4-39 shows the example 2 of operation in PPG-dead timer filter mode of WFG ch.10. In the case that the pulse width of CH10_PPG signal is shorter than WFTF10 time, CH10_PPG signal is filtered and RTO0 output signal and RTO1 output signal do not change. In the case of the conditions of WFTF10≥WFTA10 and WFTF10 ≥WFTB10, output signal shown in the Figure 4-39 can be achieved for RTO0 and RTO1.

Figure 4-39 Example 2 of Operation Waveform in WFG PPG-Dead Timer Filter Mode

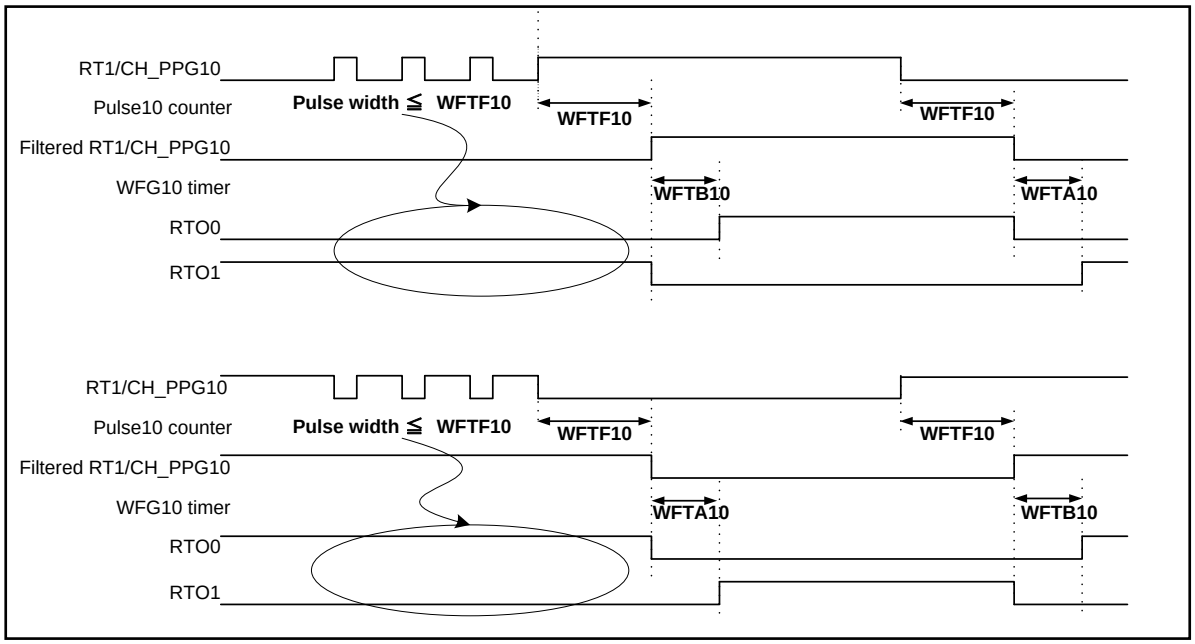


4.4.11 Supplemental Explanation on Filtering Operation of Pulse Counter

The following is the supplemental explanation on filtering operation of pulse counter use in RT dead timer filter mode or PPG dead timer filter mode.

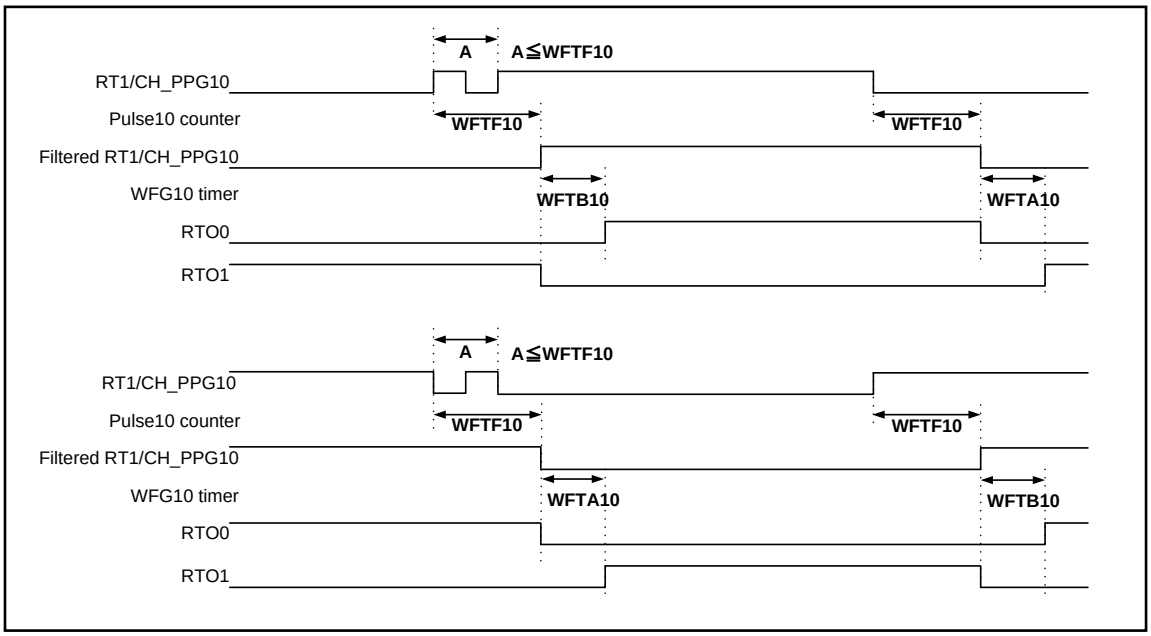
Figure 4-40 shows the operation waveform of products after TYPE2-M4 products. When the pulse width of input signal waveform of RT(1) signal or CH_PPG signal in these products is WFTF time or less, the input signal is ignored and the output signals of RTO(0) and RTO(1) are not changed. When the pulse width of input signal waveform is WFTF time or more, the output signals of RTO(0) and RTO(1) are changed after WFTF time.

Figure 4-40 RT/PPG Dead Timer Filter Mode Operation Wave Form (Products after TYPE2-M4 Products)



For TYPE1-M4 products, the level changing count of RT(1) signal or CH_PPG signal input signal waveform must be two times or less in WFTF time. When the level is changed three times or more in WFTF time, the filtering operation may not be executed. Figure 4-41 shows the operation waveform when three times or more of level change are generated,

Figure 4-41 RT/PPG Dead Timer/Filtering Mode Operation Waveform (TYPE1-M4 Products)



4.4.12 Output Polarity Revered by WESA.DMOD

The WFSA.DMOD[1:0] setting can be used to change the output polarity of the RTO(0) and RTO(1) signals in Table 4-23 as shown below regardless of the other WFSA register settings.

In the case of WFSA.DMOD[1:0] =00, RTO(0) and RTO(1) signals are output with normal polarity.

In the case of WFSA.DMOD[1:0] =01, RTO(0) and RTO(1) signals are output with reversed polarity.

In the case of WFSA.DMOD[1:0] =10, RTO(0) signal is output with reversed polarity, and RTO(1) signal is output with normal polarity.

In the case of WFSA.DMOD[1:0] =11, RTO(1) signal is output with reversed polarity, and RTO(0) signal is output with normal polarity.

For the output waveform examples, see Figure 4-42 and Figure 4-43.

Figure 4-42 Example 1 of Output Reversed Waveform with DMOD

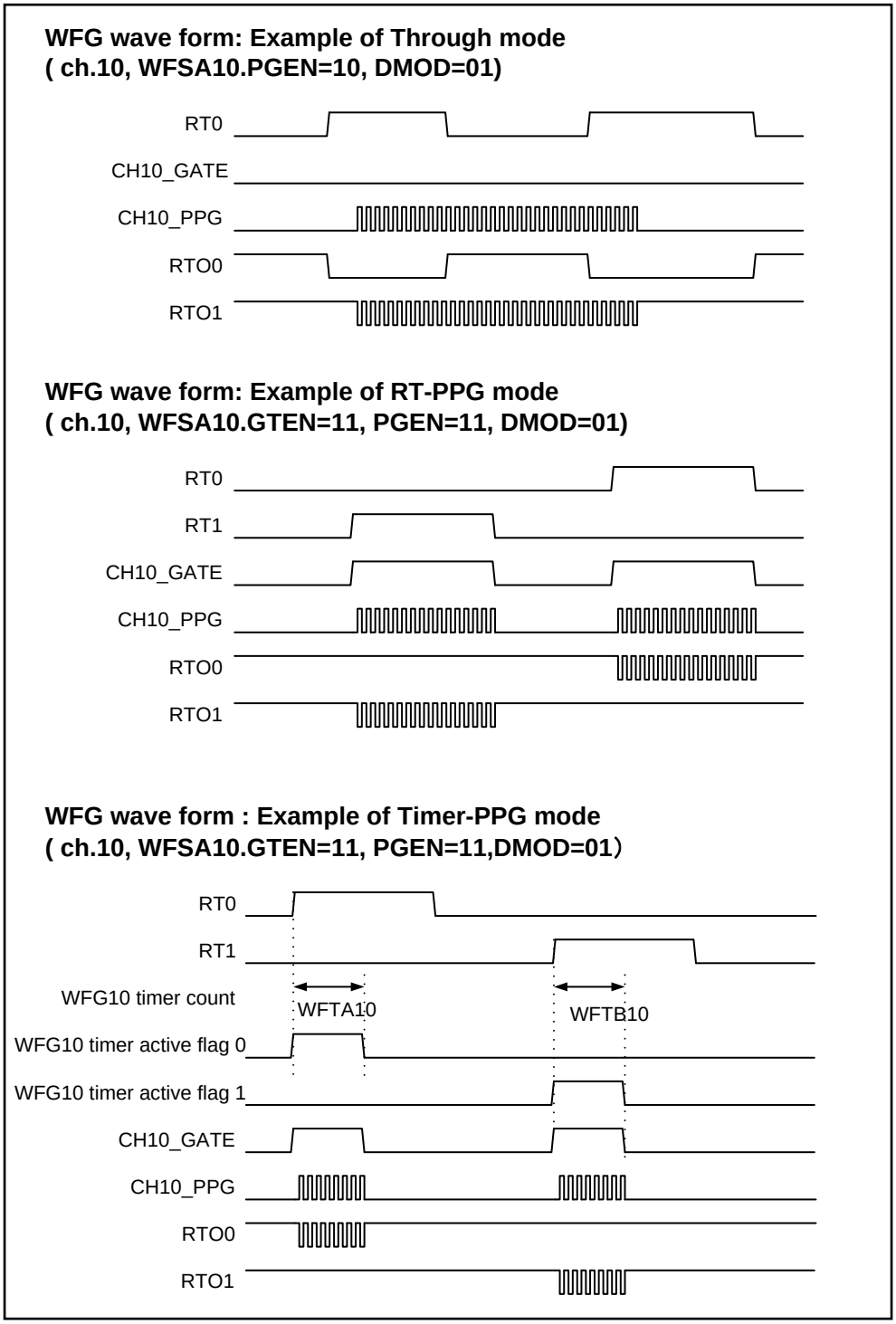
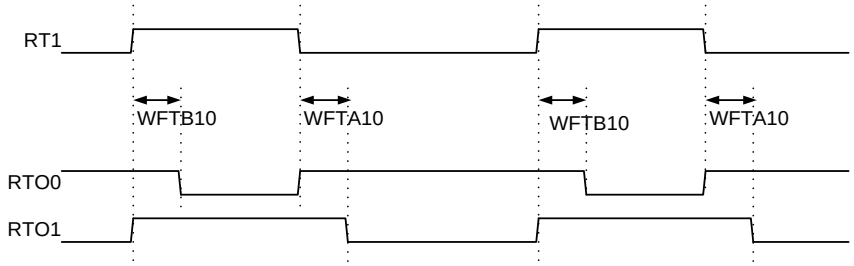
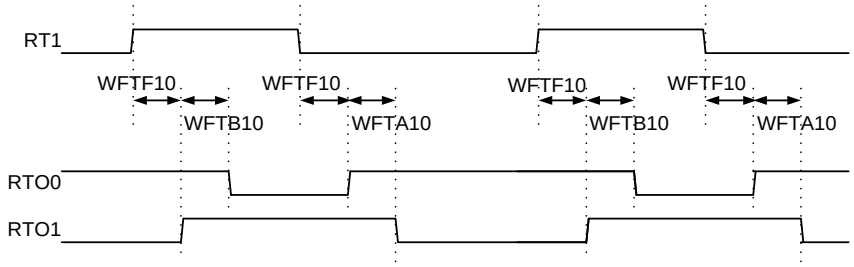


Figure 4-43 Example 2 of Output Reversed Waveform with DMOD

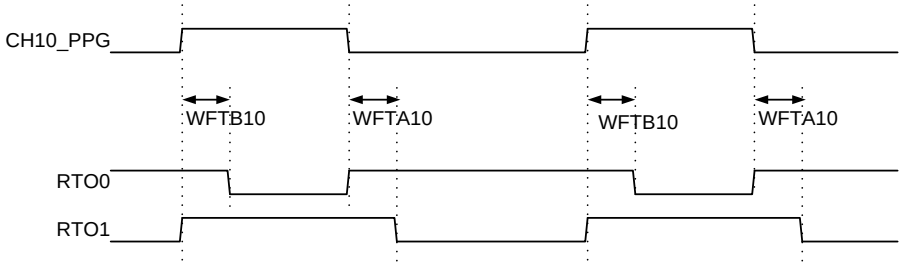
WFG wave form : Example of RT-dead timer mode (ch.10, WFSA10.TMD=100,DMOD=01）



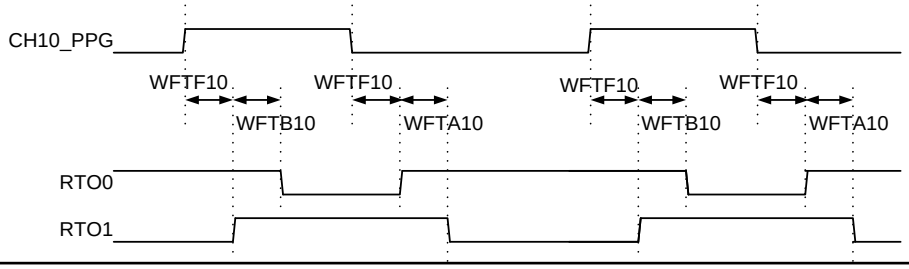
WFG wave form : Example of RT-dead timer Filter mode (ch.10, WFSA.TMD=101, DMOD=01)



WFG wave form : Example of PPG-dead timer mode (ch.10, WFSA10.TMD=111,DMOD=01）



WFG wave form : Example of PPG-dead timer Filter mode (ch.10, WFSA.TMD=110, DMOD=01)

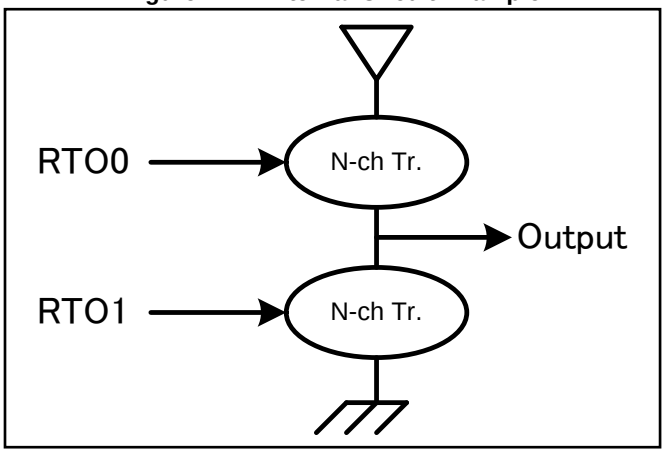


In RT dead timer mode, RT dead timer filter mode, PPG dead timer mode, or PPG dead timer filter mode (WFSA.TMD=100, 101, 110, 111), DMOD=00,01 is used when using IGBT, N-Ch driver × 2, or other same-polarity driver. DMOD=10,11 is used when using MOSFET(N-Ch＋P-Ch) or other drivers with different polarity. Check and set the specifications for the driver that is connected.

Notes:

- *When an external circuit is connected like that shown in Figure 4-44, and if RT dead timer mode (WFSA.TMD=100), DMOD=10, or other incorrect settings are made, a short-circuit will occur between the power supply and GND.*
- *Be aware that the range that this register function is enabled is different from the FM3 Family products.*

Figure 4-44 External Circuit Example



4.5 WFG FM3 Family Product-compatible Operation

This section explains WFG FM3 Family product-compatible operation.

4.5.1 WFG Operation Compatible with FM3 Family Products

When using WFG compatible with FM3 series products, be careful of the following points.

- Timer PPG mode, RT-dead timer mode, PPG dead timer mode

The register which performs an operating time setup of WFG timer (WFTM register with FM3 Family products) is divided into two, WFTA register and WFTB register with FM4 Family products, and which has come to be able to perform separate specification. By specifying the same value as that of the existing WFTM register to both WFTA register and WFTB, compatible operation with FM3 Family products becomes available.

- Reload timer function

The register, which sets counting time, used for reload timer function (WFTM register for FM3 Family products) has been changed to the WFTF register with FM4 series products. By specifying the same value as that of the existing WFTM register to WFTF register, compatible operation with FM3 Family products becomes available.

- Polar reversal function by DMOD

With FM3 Family products, the polar reversal function of the RTO output signal by WFSA.DMOD is effective only in the RT-dead timer mode and the PPG dead timer mode, and the value from WFSA.DMOD register is disregarded in other modes. With FM4 Family products, irrespective of the value of WFSA.TMD, polar reversal function of the RTO output signal by WFSA.DMOD is effective. If the setting is WFSA.DMOD=00, compatible operation with FM3 Family products becomes available.

4.6 Description of ADCMP Operation

This section explains ADCMP operation.

4.6.1 ADCMP Control Register

Table 4-23 shows the list of each control register function of ADCMP and the timing of the setting change possible. A basic setting of ADCMP is performed while forbidding the operation of each channel of ADCMP. Each channel outputs ADC start signal according to the specification of control register on the basis of the counter value of FRT to connect, if operation is enabled (by setting one of the ACSD register, ZE, UE, PE, or DE to 1).

Table 4-23 Control Register of ADMP

Setting Register	Register Function	Register Change Timing
ACSD.ZE ACSD.UE ACSD.PE ACSD.DE	Selects operation enabled or disabled All registers are 0: Operation prohibited status Any register is 1: Operation allowed status	Any user-selected timing after the initial settings are completed
ACFS.FSA	Selects FRT to connect	Set before operation allowed. Changing of the settings is prohibited after changing to operation allowed status
ACSC.BUFE	Selects ACMP buffer functional existence/absence and transmission conditions	
ACSC.ADSEL	Selects the output destination ADC of start signal	
ACSD.AMOD	Selects normal mode / offset mode	Set before operation allowed. Changing of the settings is prohibited after changing to operation allowed status (*1)
ACSD.OCUS	Selects starting source of OCU at the time of offset mode	
ACMP	Specifies compare value and offset value of ADCMP	Any user-selected timing
ACMC:MZCE ACMC:MPCE ACMC:AMC	Specifies ADCMP mask counter compare value	

*1: At the time of writing access to AMOD, OCUS, it is no problem to rewrite the setting value as well as disabling the operation of ACSD.ZE, UE, PE, and DE of operation.

By selecting the value of ACSC.ADSEL of two or more channels to the same output destination, ADCMP can instruct the same ADC to start up at two or more ADC starting timing.

4.6.2 Normal Mode Operation

In the case of ACSD.AMOD=0, ADCMP can be operated in normal mode. As shown in Table 4-24, the ADC start signal output conditions are determined by the ZE, UE, PE, and DE values of the ACSD register, the status of the FRT connected to ADCMP, connected FRT and ACMP register comparison results, and ACMC determination results. The X in the table indicates that the conditions are ignored. The FRT status to be output can be selected by specifying ZE, UE, PE, or DE of the ACSD register.

Table 4-24 AD Start Signal Output Conditions in ADCMP Normal Mode

ACSD register Value				Connected FRT Status	Connected FRT and ACMP Comparison Results	ACMC Match Determination Results	ADC Start Signal
ZE	UE	PE	DE				
1	X	X	X	Zero/Bottom	Match	Match	Output
X	1	X	X	Up	Match	Match	
X	X	1	X	Peak/Top	Match	Match	
X	X	X	1	Down	Match	Match	
When the above conditions do not apply							Not output

- In contrast to OCU, in normal mode, the ACMP＝0xFFFF value is not treated as a detected match when the connected FRT is in the peak/stop status.
- For details on ACMC match determination, see ADCMP Mask Compare Value Storage Register (ACMC).

4.6.2.1 List of the Setting Examples

Normal mode setting examples and operation are described below. The setting values used in setting examples 1 to 5 are shown in the table below.

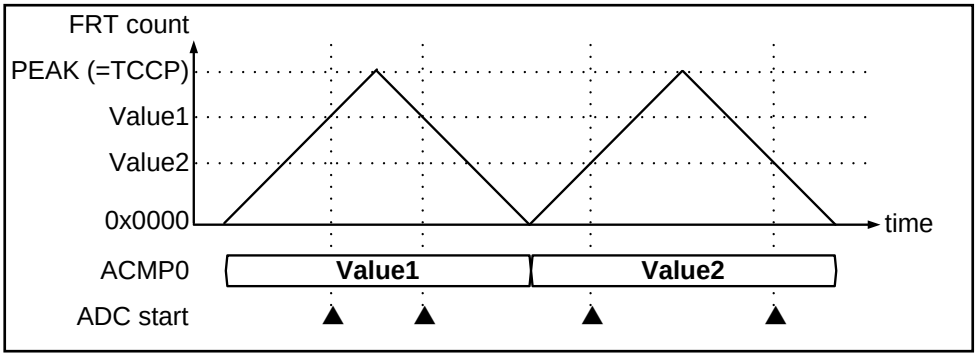
Table 4-25 ADCMP Normal Mode Setting Examples

Setting Register	Setting Example 1	Setting Example 2	Setting Example 3	Setting Example 4	Setting Example 5
ACFS10.FSA0(Selected ch.0 connection to FRT)	Arbitrary	Arbitrary	Arbitrary	Arbitrary	Arbitrary
ACFS10.FSA1(Selected ch.1 connection to FRT)	-	-	-	FRT same as ch.0	FRT same as ch.0
TCSA.MODE(Selected FRT operation mode)	1	1	1	1	1
ACSA.CE10 (Selected FM3 compatibility mode)	00	00	00	00	00
ACSC0.BUFE(Selected buffer function of ch.0) ACSC0:APBM	01 0	01 0	01 0	01 0	01 0
ACSC1.BUFE(Selected buffer function of ch.1) ACSC1:APBM	- -	- -	- -	01 0	01 0
ACSC0.ADSEL(Selected output destination ADC of ch.0)	Arbitrary	Arbitrary	Arbitrary	Arbitrary	Arbitrary
ACSC1.ADSEL(Selected output destination ADC of ch.1)	-	-	-	ADC same as ch.0	ADC same as ch.0
ACSCD0.AMOD ACSCD0.OCUS ACSCD0.ZE, UE, PE, DE (Selected operation mode of ch.0)	0 0 1111	0 0 1100	0 0 0011	0 0 1100	0 0 1100
ACSCD1.AMOD ACSCD1.OCUS ACSCD1.ZE, UE, PE, DE (Selected operation mode of ch.1)	- - -	- - -	- - -	0 0 0011	0 0 1100
ACMP0(Specified compare value of ch.0)	Initial value specified	Initial value specified	Initial value specified	Initial value specified	Initial value specified
ACMP1(Specified compare value of ch.1)	-	-	-	Initial value specified	Initial value specified
ACMC0 (Specified ch.0 mask compare)	0x00	0x00	0x00	0x00	0x00
ACMC1 (Specified ch.1 mask compare)				0x00	0x00

4.6.2.2 Operation of the Setting Example 1

The setting example 1 is an example of using only ch.0 of ADCMP. The setting of ch.1 is arbitrary. ch.0 enables AD conversion start signal under the condition of FRT-Zero, UP, Peak, Down. As shown in Figure 4-45, AD conversion start signal is output at the time of match detection of FRT and ACMP0 (▲mark shows ADC start timing).

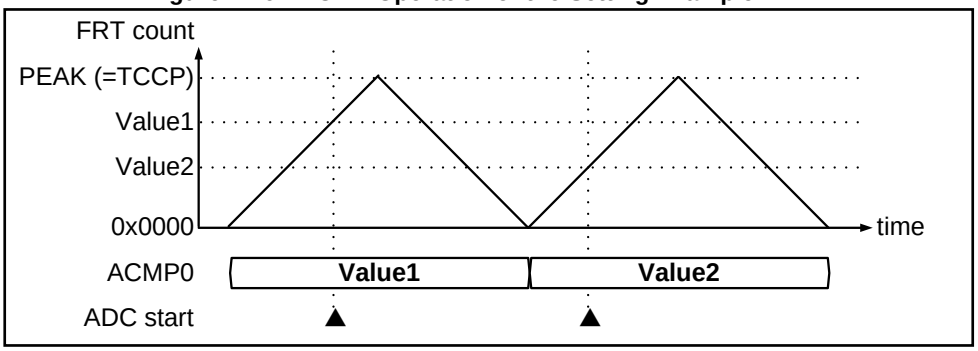
Figure 4-45 ADCMP Operation of the Setting Example 1



4.6.2.3 Operation of the Setting Example 2

The setting example 2 is an example of using only ch.0 of ADCMP. The setting of ch.1 is arbitrary. ch.0 enables AD conversion start signal under the condition of FRT-Zero and UP. As shown in Figure 4-46, AD conversion start signal is output at the time of match detection of FRT and ACMP0.

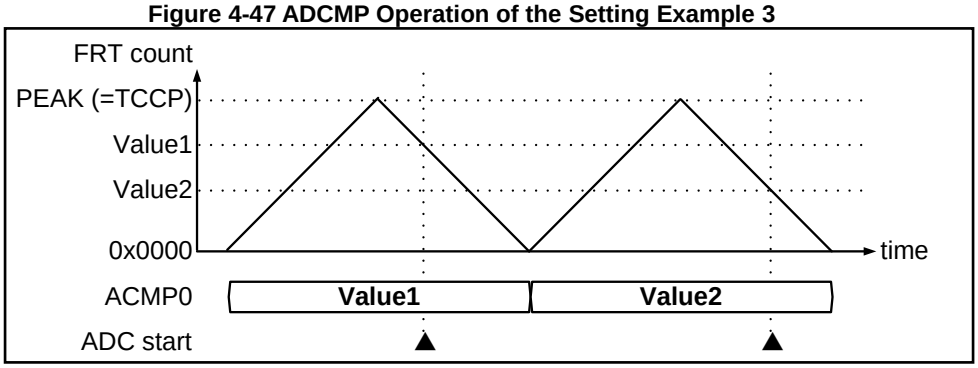
Figure 4-46 ADCMP Operation of the Setting Example 2



4.6.2.4 Operation of the Setting Example 3

The setting example 3 is an example of using only ch.0 of ADCMP. The setting of ch.1 is arbitrary. ch.0 enables AD conversion start signal under the condition of FRT- Peak and Down. As shown in Figure 4-47, AD conversion start signal is output at the time of match detection of FRT and ACMP0.

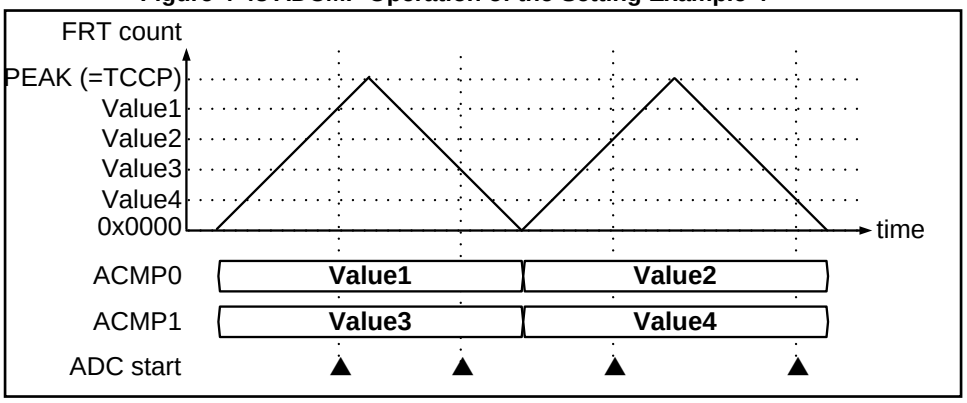
Figure 4-47 ADCMP Operation of the Setting Example 3



4.6.2.5 Operation of the Setting Example 4

The setting example 4 is an example of using together two channels, ch.0 and ch.1 of ADCMP. ch.0 enables AD conversion start signal under the condition of FRT- Zero and Up. ch.1 enables AD conversion start signal under the condition of FRT- Peak and Down. The start signal of ch.0 and ch.1 undergo logic OR operation. As shown in Figure 4-48, AD conversion start signal is output at the time of match detection of FRT and ACMP0, and match detection of FRT and ACMP1.

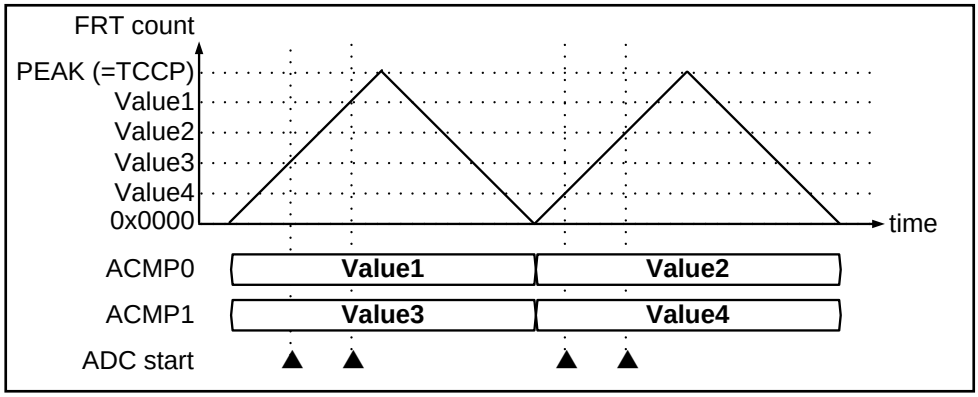
Figure 4-48 ADCMP Operation of the Setting Example 4



4.6.2.6 Operation of the Setting Example 5

The setting example 5 is an example of using together two channels, ch.0 and ch.1 of ADCMP. ch.0 enables AD conversion start signal under the condition of FRT-Zero and UP. ch.1 enables AD conversion start signal under the condition of FRT-Zero and UP. The start signal of ch.0 and ch.1 undergo logic OR operation. As shown in Figure 4-49, AD conversion start signal is output at the time of match detection of FRT and ACMP0, and match detection of FRT and ACMP1.

Figure 4-49 ADCMP Operation of the Setting Example 5



4.6.3 Offset Mode Operation

In the case of ACSD.AMOD=1, ADCMP can be operated in offset mode. In the case of offset mode, the value of ACMP is loaded to an offset starting down counter at the time of match detection of selected OCCP and FRT. After an offset starting down counter performs count operation specified by ACMP, an ADC start signal is output. The offset time from match detection of OCCP to ADC starting is as follows.
Offset time = ACMP value × free-run timer clock cycle
OCCP register of a starting source can be selected with ACSD.OCS values. The selected OCCP is differed by ADCMP channel numbers. For selected OCCP, see Table 4-26.

Table 4-26 OCCP Registers Selected by OCUS

ADCMPChannel No.	At OCUS=0	At OCUS=1
ADCMP ch.0	OCCP0	OCCP1
ADCMP ch.1	OCCP0	OCCP1
ADCMP ch.2	OCCP2	OCCP3
ADCMP ch.3	OCCP2	OCCP3
ADCMP ch.4	OCCP4	OCCP5
ADCMP ch.5	OCCP4	OCCP5

As shown in Table 4-27, the conditions where the ACMP value is loaded to the offset start down-counter and the down-count is started are determined by the ZE, UE, PE, and DE values of the ACSD register, FRT status connected to ADCMP, comparison results between the FRT and OCCP of the selected OCU, and the ACMC determination results. The X in the table indicates that the conditions are ignored. The FRT status where the count is started can be selected by specifying ZE, UE, PE, or DE of the ACSD register.

Table 4-27 Down-count Start Conditions in ADCMP Offset Mode

ACSD Register Value				Connected FRT Status	OCU Comparison Results	ACMC Match Determination Results	Down-count
ZE	UE	PE	DE				
1	X	X	X	Zero/Bottom	Match	Match	Start
X	1	X	X	Up	Match	Match	
X	X	1	X	Peak/Top	Match	Match	
X	X	X	1	Down	Match	Match	
When the above conditions do not apply							Does not start

- In the determination conditions of the OCU comparison results, when the OCCP(0) register is selected, the conditions in Table 3-6 OCCP(0) and FRT match determination conditions apply. When the OCCP(1) register is selected, the conditions in Table 3-10 OCCP(1) and FRT match determination conditions apply.
- For details on ACMC match determination, see ADCMP Mask Compare Value Storage Register (ACMC).

If the start conditions for the down-counter are met during the countdown of the offset time, the down-counter reloads the ACMP and restarts the down-count. Also, the down-counter is reset if 0 is written to all of ACSD:ZE, UE, PE, and DE, or if AMOD=0 is written.
The FRT-ch.0 that operates can be selected by setting count mode with offset for the FRT connected to OCU and normal count mode for the FRT connected to ADCMP.

4.6.3.1 List of the Examples of the Setting

Offset mode setting examples and operation are described below. The setting values used in setting examples 6 and 7 are shown in Table 4-28.

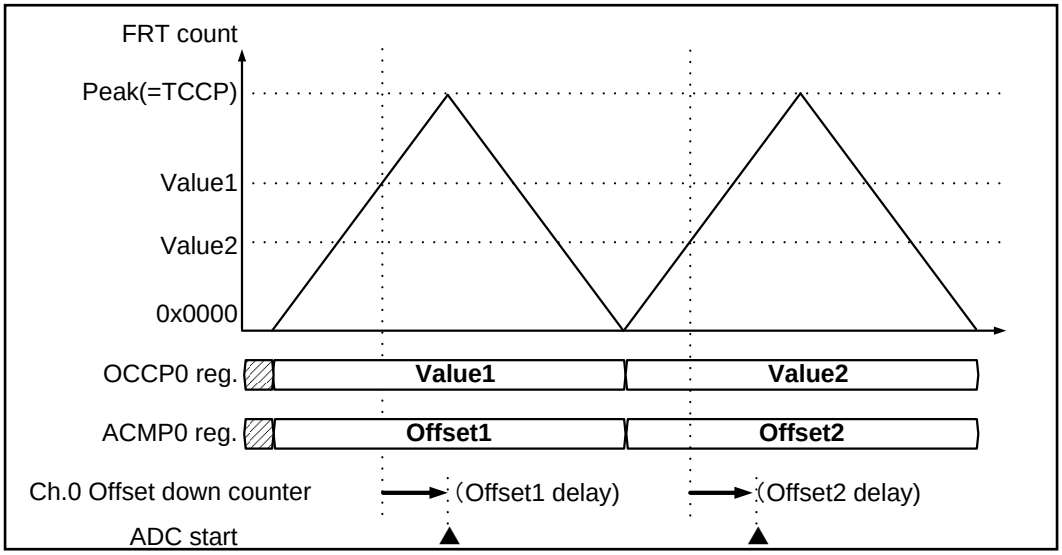
Table 4-28 ADCMP Offset Mode Setting Examples

Setting Register	Setting Example 6	Setting Example 7
ACFS10.FSA0 (Selected ch.0 connection to FRT)	Arbitrary	Arbitrary
ACFS10.FSA1 (Selected ch.1 connection to FRT)	-	FRT as same as ADCMP-ch.0
TCSA.MODE (Selected operation mode of FRT)	1	1
OCFS10:FSO0 (Selected OCU-ch.0 connection to FRT)	FRT as same as ADCMP-ch.0	FRT as same as ADCMP-ch.0
ACSA.CE10 (Selected FM3 compatibility mode)	00	00
ACSC0.BUFE (Selected buffer function of ch.0) ACSC0:APBM	01 0	01 0
ACSC1.BUFE (Selected buffer function of ch.1) ACSC1:APBM	-	01 0
ACSC0.ADSEL (Selected ADC output destination of ch.0)	Arbitrary	Arbitrary
ACSC1.ADSEL (Selected ADC output destination of ch.1)	-	ADC as same as ADCMP-ch.0
ACSCD0.AMOD ACSCD0.OCUS ACSCD0.ZE, UE, PE, DE (Selected operation mode of ch.0)	1 0 1100	1 0 1100
ACSCD1.AMOD ACSCD1.OCUS ACSCD1.ZE, UE, PE, DE (Selected operation mode of ch.1)	- - -	1 0 1100
ACMP0 (Specified ch.0 offset value)	Initial value specified	Initial value specified
ACMP1 (Specified ch.1 offset value)	-	Initial value specified
ACMC0 (Specified ch.0 mask compare)	0x00	0x00
ACMC1 (Specified ch.1 mask compare)		0x00

4.6.3.2 Operation of the Setting Example 6

The setting example 6 is an example of using only ch.0 of ADCMP. The setting of ch.1 is arbitrary. Offset starting is permitted under the condition of FRT-Zero and UP. As shown in Figure 4-50, the value of ACMP0 is loaded to Down counter at the time of match detection of FRT and OCCP0, and AD conversion start signal is output after the designated time.

Figure 4-50 ADCMP Operation of the Setting Example 6

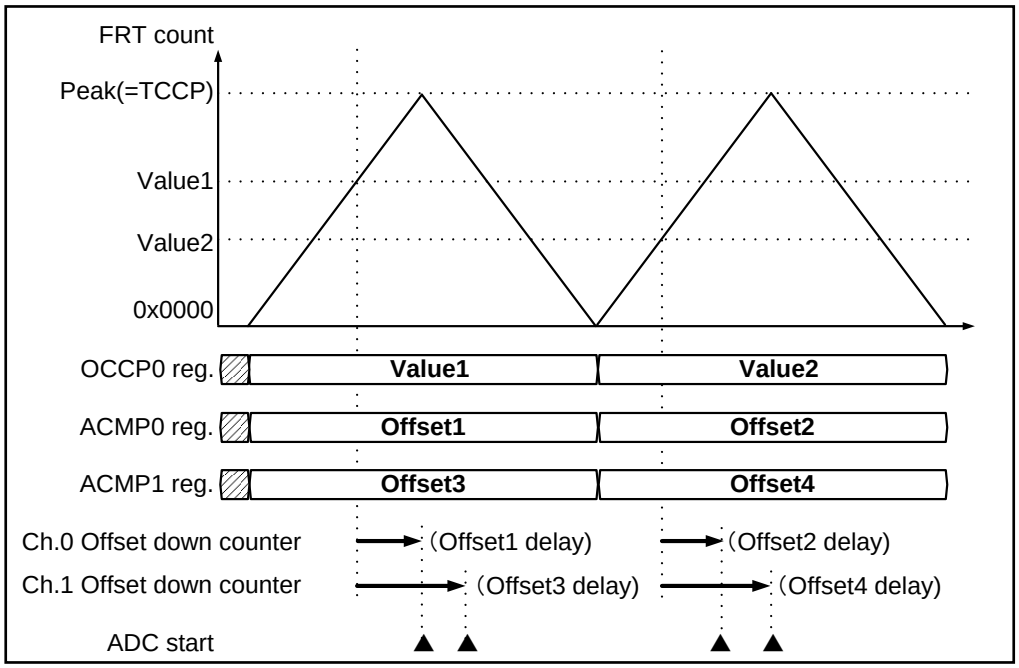


If match detection of OCCP occurs during count operation of Down counter, Down counter reloads the value from ACMP and restarts counting operation. For this reason, if the interval of match detection of starting source of OCCP is shorter than the specified offset time, AD conversion start signal may not be output.

4.6.3.3 Operation of the Setting Example 7

The setting example 7 is an example of using together two channels, ch.0 and ch.1 of ADCMP. ch.0 enables offset starting under the condition of FRT-Zero and UP. ch.1 enables offset starting under the condition of FRT-Zero and UP. As shown in Figure 4-51, the value from ACMP0 and ACMP1 are loaded to Down counter respectively at the time of match detection of FRT and OCCP0. After the designated time, the start signal of ch.0 and ch.1 undergo logical OR operation and AD conversion start signal is output.

Figure 4-51 ADCMP Operation of the Setting Example 7



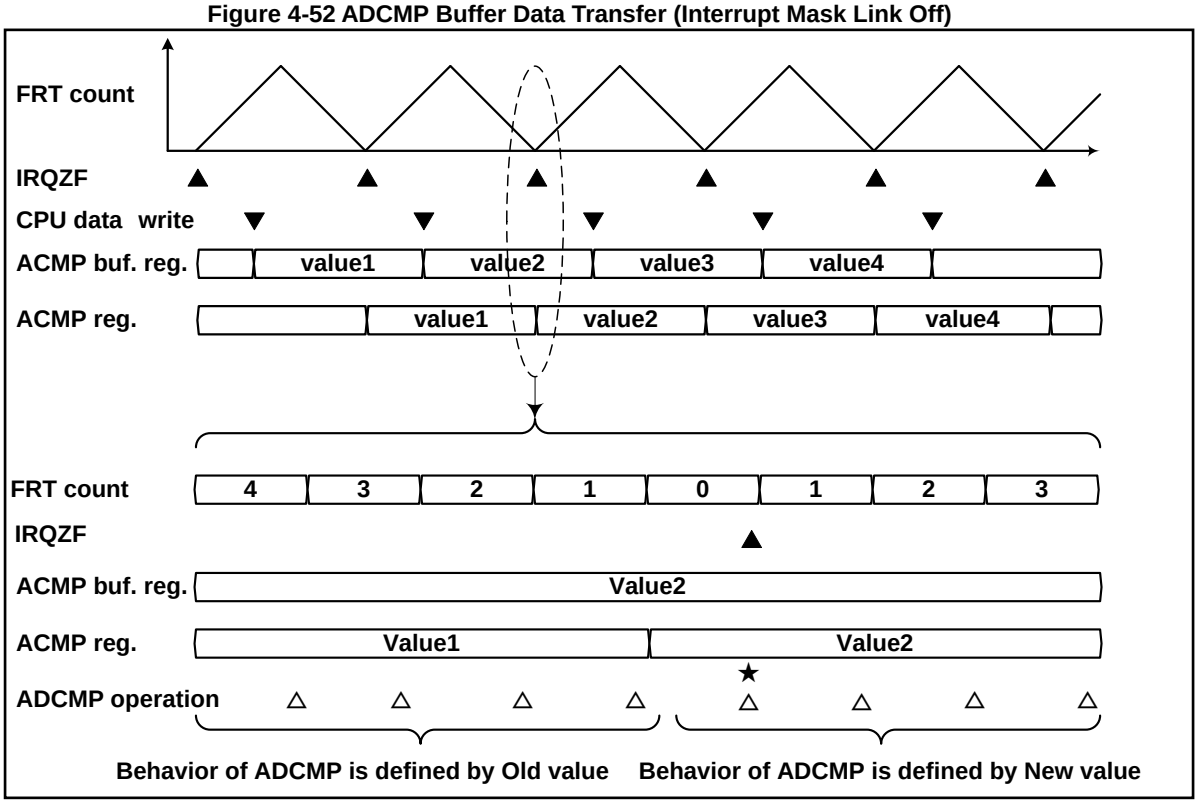
4.6.4 ADCMP Buffer Transfer

The ACMP register and ACMC register have a buffer function. When the buffer function is enabled, data written to ACMP and ACMC from the CPU during the count operation by FRT are written to the buffer register. Then, data is transferred to the respective registers at the specified transfer timing.

When FRT interrupt mask linked transfer is off, the buffer transfer is performed at the specified FRT count status. There is no effect by the FRT interrupt mask counter.

An operation example when the ACMP buffer function is enabled, Zero/Bottom transfer is performed, and (ACSC.BUFE=01) FRT interrupt mask linked transfer is off (ACSC.APBM=0) is shown in Figure 4-52.

Figure 4-52 ADCMP Buffer Data Transfer (Interrupt Mask Link Off)



The top section in the figure shows the entire view, and the bottom section shows an enlarged view of the transfer operation section. FRT performs the count operation in up/down-count mode. A zero detection interrupt is generated from FRT at the timing indicated by ▲. At the timing of ▼, the ACMP buffer register is overwritten from the CPU. The written data is stored in the ACMP buffer register. Then, whenever the FRT zero is detected, the transfer operation to the ACMP register is performed, and an interrupt is generated.

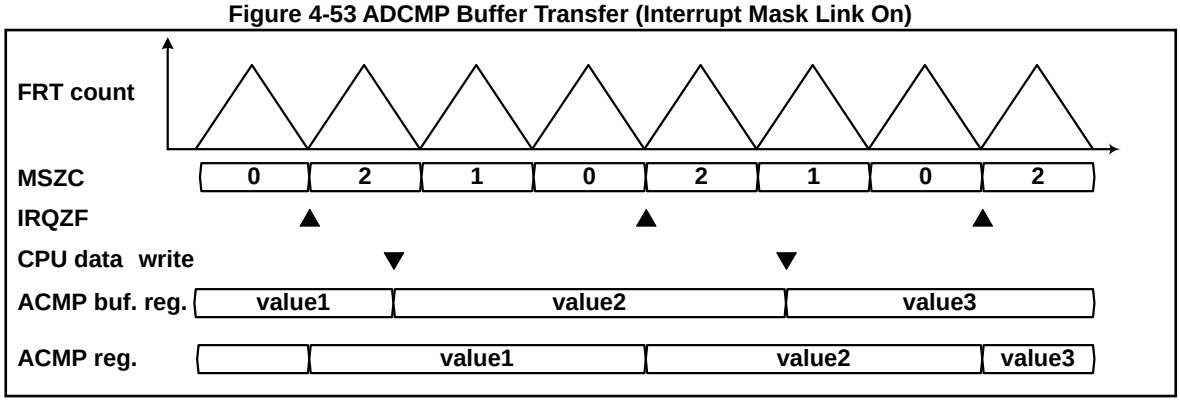
ADCMP performs operation based on the specified ACMP register setting at the timing of △. ADCMP operation from the timing of ★ (FRT=0x0000) is performed based on the new data after ACMP transfer. ADCMP operation before this timing is performed based on the old data before ACMP transfer. In this way, the ADCMP uses the transferred data starting from the transfer timing.

The figure shows an example of ACMP Zero/Bottom transfer, but the ACMC buffer transfer operation and Peak/Top transfer also perform the same operation. In all of these cases, the transferred data is used starting from the transfer timing.

When FRT interrupt mask linked transfer is turned on (ACSC.APBM=1), buffer transfer is performed when the connected FRT is the specified count status and the FRT interrupt mask counter is 0.

An operation example when the ACMP buffer function is enabled, Zero/Bottom transfer is performed, and (ACSC.BUFE=01) FRT interrupt mask linked transfer is on (ACSC.APBM=1) is shown in Figure 4-53.

Figure 4-53 ADCMP Buffer Transfer (Interrupt Mask Link On)



FRT performs the count operation in up/down-count mode. The zero detection interrupt mask counter (MSZC) counts down from 2 to 0. A zero detection interrupt is generated from FRT at the timing indicated by ▲. At the timing of ▼, the ACMP buffer register is overwritten from the CPU. The written data is stored in the ACMP buffer register. Then, whenever the FRT zero is detected while the zero detection interrupt mask counter is 0, the transfer operation to the ACMP register is performed, and an interrupt is generated.

Like the bottom section of Figure 4-52, the transferred data is used for operation from the time of the FRT count. As described above, the number of ACMP buffer transfer operations can be reduced by linking with the FRT interrupt mask counter.

If the connected FRT is count mode with offset (ch.1 or ch.2), this FRT interrupt mask counter value is fixed at 0. However, the interrupt mask counter value used in determination of the buffer transfer conditions uses the interrupt mask counter value of the FRT-ch.0 where the count is operating in synchronization with this FRT. As a result, the buffer transfer operation can be performed by linking with the FRT interrupt mask counter even if the connected FRT is in count mode with offset.

Note:

- *The buffer transfer function linked to the FRT interrupt mask counter is available in TYPE3-M4 products and later only. It cannot be used in TYPE1-M4 and TYPE2-M4 products.*

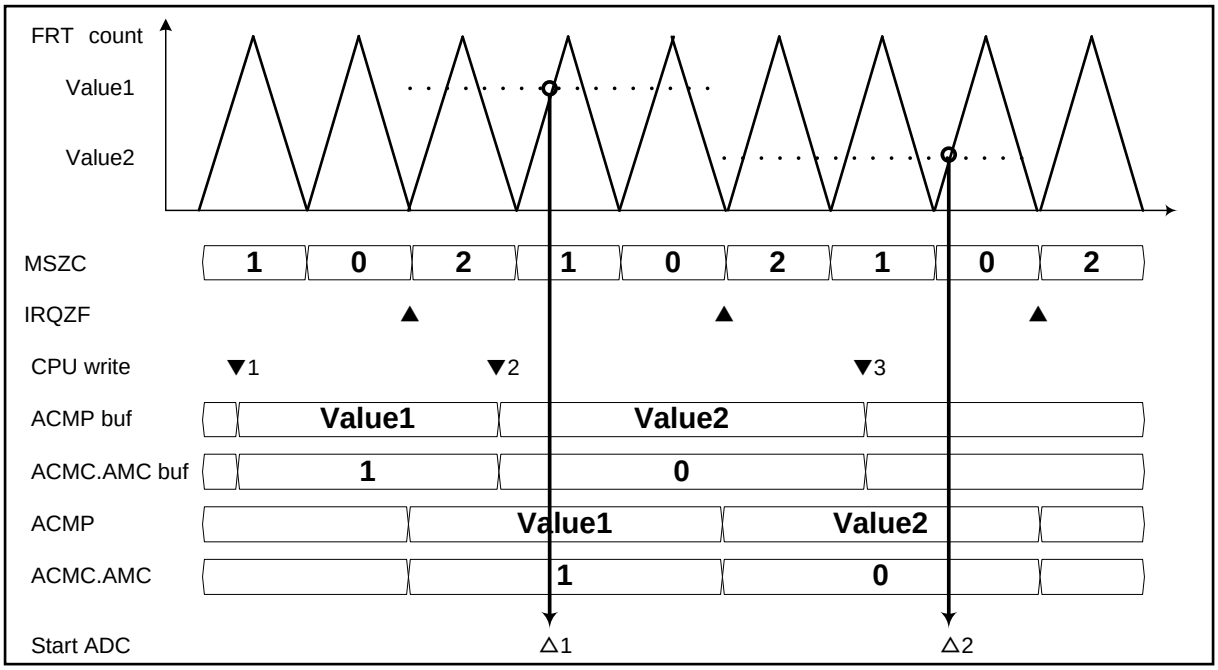
4.6.5 ADC Start Linked with FRT Interrupt Mask Counter

Matched output of the ACMC register can be used to perform ADC start linked with the FRT interrupt mask counter. An operation example in ADCMP normal mode is shown in Figure 4-54. The explanation below is based on the following settings.

ACSC register: BUFE=01, APBM=1

ACSD register: AMOD=0, ZE=0, UE=1, PE=0, DE=0

Figure 4-54 ADC Start Linked with FRT Interrupt Mask Counter



FRT performs the count operation in up/down-count mode. The zero detection interrupt mask counter (MSZC) counts down from 2 to 0. A zero detection interrupt is generated from FRT at the timing indicated by ▲.

At the timing of ▼1, Value 1 is written to the ACMP buffer register. At the same time, MZCE=1, MPCE=0, and AMC=0001 are written to the ACMC buffer register. Then, the transfer operation to the ACMP register and ACMC register is performed at the timing of ▲. Because MSZC=AMC=1 and FRT=ACMP=Value 1, ADC is started at the timing of △1.

At the timing of ▼2, Value 2 is written to the ACMP buffer register. At the same time, MZCE=1, MPCE=0, and AMC=0000 are written to the ACMC buffer register. Then, the transfer operation to the ACMP register and ACMC register is performed at the timing of ▲. Because MSZC=AMC=0 and FRT=ACMP=Value 2, ADC is started at the timing of △2.

In this way, the ACMC register setting is used to enable ADC start linked to the FRT interrupt mask counter. In the same way as ADCMP offset mode, the offset start down-counter can be started.

If the ACMC register value does not need to be changed as needed, overwriting the setting is not necessary. The setting value at ACMC register initialization is applied.

Notes:

- *The ADC start function linked to the FRT interrupt mask counter is available in TYPE3-M4 products and later only. It cannot be used in TYPE1-M4 and TYPE2-M4 products.*
- *The ADC start function linked to the FRT interrupt mask counter can be used when utilizing the ACSD register to output an ADC start signal. It cannot be used for FM3 compatibility start utilizing the ACSA register.*

4.7 ADCMP FM3 Family Product-compatible Operation

This section explains ADCMP operation compatible with FM3 Family products.

ADCMP Operation Compatible with FM3 Family Products

ADCMP performs compatible operation with FM3 Family products by using ACSA.CE10, CE32, CE54, and ACSA.SEL10, SEL32 and SEL54. In this case, ch. (0) and ch. (1) of ADCMP are used in pairs. The list of the register setting value and ch. (0) and OCU ch (1) of ADCMP in each operation mode are shown in Table 4-29. The selected operation performs the same operation as each setting example of ADCMP shown in 4.6 Description of ADCMP Operation.

Table 4-29 ADCMP Start-up Compatible with FM3 Family

ACSA.CE10 ACSA.CE32 ACSA.CE54	ACSA.SEL10 ACSA.SEL32 ACSA.SEL54	Operation Mode Selected
00	-	Operation disabled state
01	00	ch. (0) operates the setting example 1 of ADCMP. ch. (1) cannot be used.
01	01	ch. (0) operates the setting example 2 of ADCMP. ch. (1) cannot be used.
01	10	ch. (0) operates the setting example 3 of ADCMP. ch. (1) cannot be used.
01	11	ch. (0) and ch. (1) operate the setting example 4 of ADCMP. Sets the compare value in FRT-Zero and UP to ACMP (0) of ch. (0). Sets the compare value in FRT-Peak and Down to ACMP (1) of ch. (1). The connection FRT of ch. (0) and ch. (1) and the output destination ADC are set to be the same setting.
The value other than the above	-	Operation disabled state

When using ADCMP compatible with FM3 Family products, FRT connected to ADCMP to connect to except FRT-ch.0, and the buffer function and transfer timing specification of ACMP register, and selected specification of the output destination ADC are not compatible with FM3 Family products about the register specification method. Select and specify the specification by FSAC register and ACSC register before enabling ADCMP to start up.

The name of register which stores compare value differ between FM3 Family products and FM4 Family products. The correspondence table of ADCMP compare register between FM3 Family and FM4 Family is shown below.

Table 4-30 Correspondence Table of ADCMP Compare Register Name between FM3 Family and FM4 Family Products

Register Name of FM3 Family Products	Register Name of FM4 Family Products
ACCP0	ACMP0
ACCPDN0	ACMP1
ACCP1	ACMP2
ACCPDN1	ACMP3
ACCP2	ACMP4
ACCPDN2	ACMP5

4.8 FRT Selection of OCU, ICU, and ADCMP

OCU, ICU and ADCMP are configured to be able to select FRT for other multifunction timer units. This section explains FRT connection between multifunction timer units and the selection method.

4.8.1 Product Mounting Two MFT's

Figure 4-55 shows a diagram of FRT connected between multifunction timer units for a product mounting 2 multifunction timer units.

Figure 4-55 Diagram of FRT Connected between Multifunction Timer Units (For Product Mounting 2 Multifunction Timer Units)

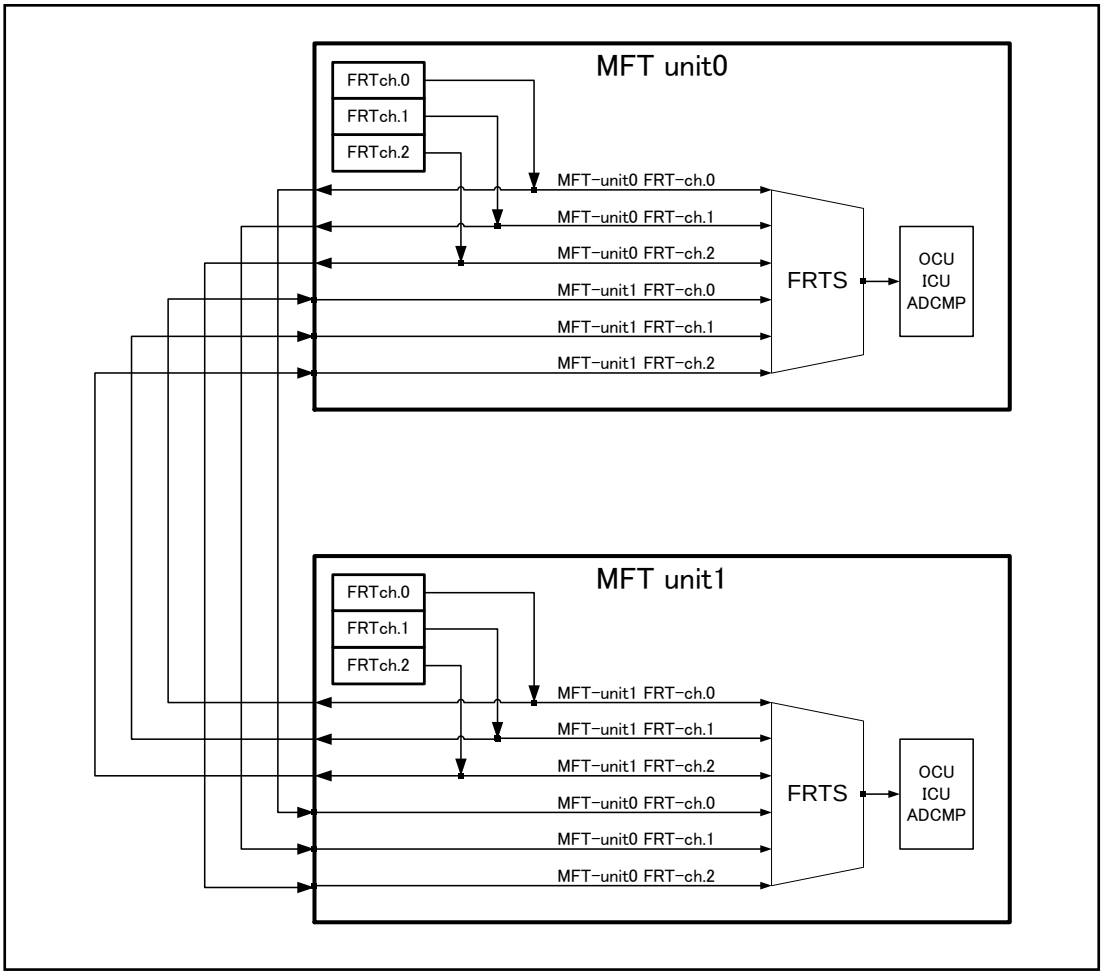


Table 4-31 and Table 4-32 show the OCFS, ICFS, and ACFS register setting values for the MFT-unit0 and MFT-unit1 installed multifunction timer units and the FRT selected for connection. The settings for each register are listed in the table. TP3 fields marked by (★) can be used for TYPE3-M4 products and later only. This setting is prohibited in TYPE1-M4 and TYPE2-M4 products.

Table 4-31 OCFS, ICFS, ACFS Register Settings for MFT unit0 (For Product Mounting 2 Multifunction Timer Units)

Name of Register		Setting	TP3	Function
OCFS ICFS ACFS	FSO0[3:0] FSI0[3:0] FSA0[3:0] ch.(0) side	0000		Connects FRT ch.0 of MFT unit0 to OCU/ICU/ADCMP ch.(0) of MFT unit0.
		0001		Connects FRT ch.1 of MFT unit0 to OCU/ICU/ADCMP ch.(0) of MFT unit0.
		0010		Connects FRT ch.2 of MFT unit0 to OCU/ICU/ADCMP ch.(0) of MFT unit0.
		0011		Connects FRT ch.0 of MFT unit1 to OCU/ICU/ADCMP ch.(0) of MFT unit0.
		0100		Connects FRT ch.1 of MFT unit1 to OCU/ICU/ADCMP ch.(0) of MFT unit0.
		0101	★	Connects FRT ch.2 of MFT unit1 to OCU/ICU/ADCMP ch.(0) of MFT unit0.
		Other		Setting prohibited
	FSO1[3:0] FSI1[3:0] FSA1[3:0] ch.(1) side	0000		Connects FRT ch.0 of MFT unit0 to OCU/ICU/ADCMP ch.(1) of MFT unit0.
		0001		Connects FRT ch.1 of MFT unit0 to OCU/ICU/ADCMP ch.(1) of MFT unit0.
		0010		Connects FRT ch.2 of MFT unit0 to OCU/ICU/ADCMP ch.(1) of MFT unit0.
		0011		Connects FRT ch.0 of MFT unit1 to OCU/ICU/ADCMP ch.(1) of MFT unit0.
		0100		Connects FRT ch.1 of MFT unit1 to OCU/ICU/ADCMP ch.(1) of MFT unit0.
		0101	★	Connects FRT ch.2 of MFT unit1 to OCU/ICU/ADCMP ch.(1) of MFT unit0.
		Other		Setting prohibited

Table 4-32 OCFS, ACFS and ICFS Register Settings for MFT unit1 (For Product Mounting 2 Multifunction Timer Units)

Name of Register		Setting	TP3	Function
OCFS ICFS ACFS	FSO0[3:0] FSI0[3:0] FSA0[3:0] ch.(0) side	0000		Connects FRT ch.0 of MFT unit1 to OCU/ICU/ADCMP ch.(0) of MFT unit1.
		0001		Connects FRT ch.1 of MFT unit1 to OCU/ICU/ADCMP ch.(0) of MFT unit1.
		0010		Connects FRT ch.2 of MFT unit1 to OCU/ICU/ADCMP ch.(0) of MFT unit1.
		0011		Connects FRT ch.0 of MFT unit0 to OCU/ICU/ADCMP ch.(0) of MFT unit1.
		0100		Connects FRT ch.1 of MFT unit0 to OCU/ICU/ADCMP ch.(0) of MFT unit1.
		0101	★	Connects FRT ch.2 of MFT unit0 to OCU/ICU/ADCMP ch.(0) of MFT unit1.
		Other		Setting prohibited
	FSO1[3:0] FSI1[3:0] FSA1[3:0] ch.(1) side	0000		Connects FRT ch.0 of MFT unit1 to OCU/ICU/ADCMP ch.(1) of MFT unit1.
		0001		Connects FRT ch.1 of MFT unit1 to OCU/ICU/ADCMP ch.(1) of MFT unit1.
		0010		Connects FRT ch.2 of MFT unit1 to OCU/ICU/ADCMP ch.(1) of MFT unit1.
		0011		Connects FRT ch.0 of MFT unit0 to OCU/ICU/ADCMP ch.(1) of MFT unit1.
		0100		Connects FRT ch.1 of MFT unit0 to OCU/ICU/ADCMP ch.(1) of MFT unit1.
		0101	★	Connects FRT ch.2 of MFT unit0 to OCU/ICU/ADCMP ch.(1) of MFT unit1.
		Other		Setting prohibited

4.8.2 Product Mounting Three MFT's (other than TYPE6-M4)

Figure 4-56 shows a diagram of FRT connected between multifunction timer units for a product mounting 3 multifunction timer units.

Figure 4-56 Diagram of FRT Connected between Multifunction Timer Units (for Product Mounting 3 Multifunction Timer Units)

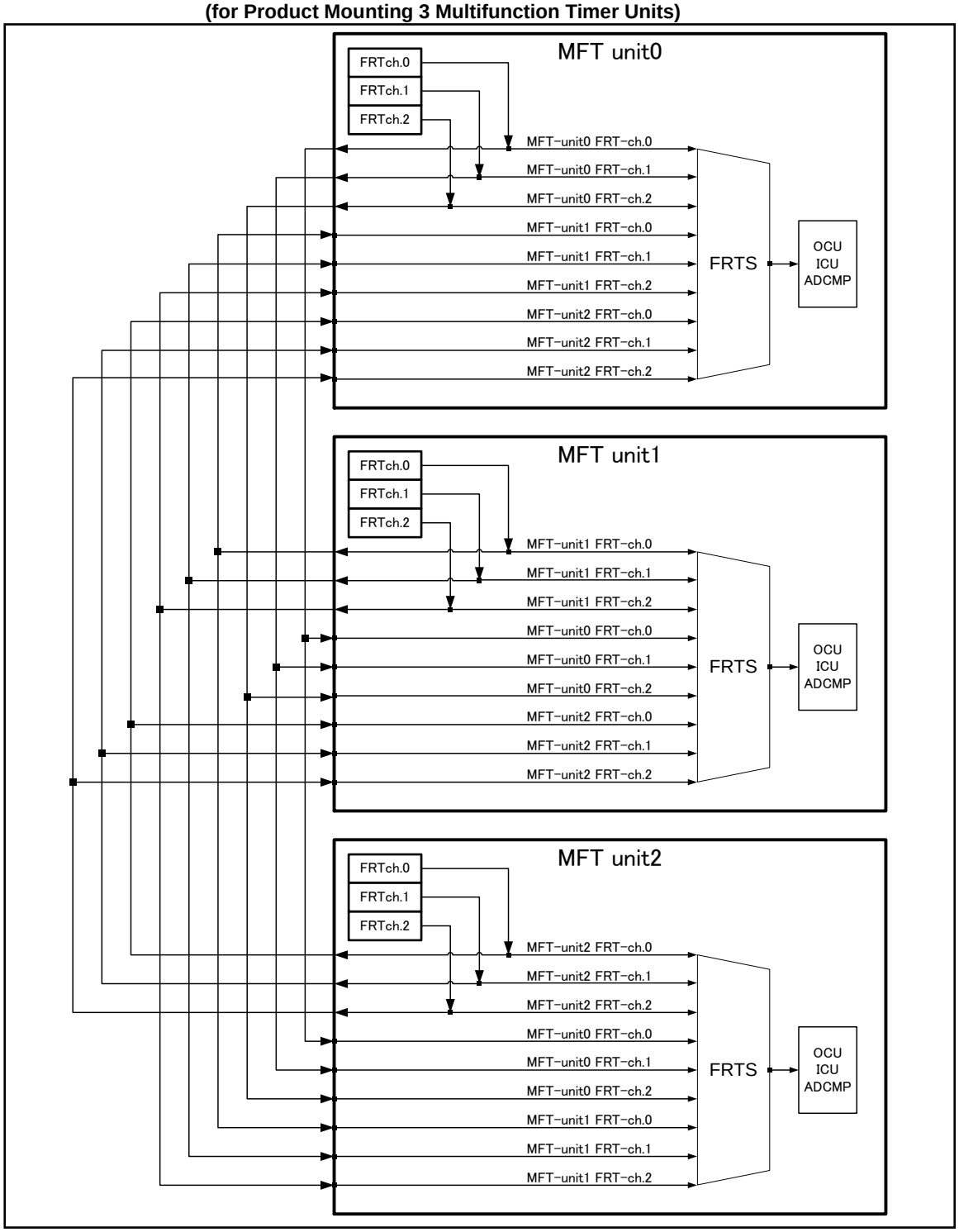


Table 4-33, Table 4-34 and Table 4-35 show the OCFS, ICFS, and ACFS register setting values for the MFT-unit0, MFT-unit1, and MFT-unit2 installed multifunction timer units and the FRT selected for connection. The settings for each register are listed in the table. TP3 fields marked by (★) can be used for TYPE3-M4 products and later only. This setting is prohibited in TYPE1-M4 and TYPE2-M4 products.

Table 4-33 OCFS, ICFS, ACFS Register Settings for MFT unit0 (for Product Mounting 3 Multifunction Timer Units)

Register Name		Setting	TP3	Function
OCFS ICFS ACFS	FSO0[3:0] FSI0[3:0] FSA0[3:0] ch.(0) side	0000		Connects FRT ch.0 of MFT unit0 to OCU/ICU/ADCMP ch.(0) of MFT unit0.
		0001		Connects FRT ch.1 of MFT unit0 to OCU/ICU/ADCMP ch.(0) of MFT unit0.
		0010		Connects FRT ch.2 of MFT unit0 to OCU/ICU/ADCMP ch.(0) of MFT unit0.
		0011		Connects FRT ch.0 of MFT unit1 to OCU/ICU/ADCMP ch.(0) of MFT unit0.
		0100		Connects FRT ch.0 of MFT unit2 to OCU/ICU/ADCMP ch.(0) of MFT unit0.
		0101	★	Connects FRT ch.1 of MFT unit1 to OCU/ICU/ADCMP ch.(0) of MFT unit0.
		0110	★	Connects FRT ch.1 of MFT unit2 to OCU/ICU/ADCMP ch.(0) of MFT unit0.
		0111	★	Connects FRT ch.2 of MFT unit1 to OCU/ICU/ADCMP ch.(0) of MFT unit0.
		1000	★	Connects FRT ch.2 of MFT unit2 to OCU/ICU/ADCMP ch.(0) of MFT unit0.
		Other		Setting prohibited
	FSO1[3:0] FSI1[3:0] FSA1[3:0] ch.(1) side	0000		Connects FRT ch.0 of MFT unit0 to OCU/ICU/ADCMP ch.(1) of MFT unit0.
		0001		Connects FRT ch.1 of MFT unit0 to OCU/ICU/ADCMP ch.(1) of MFT unit0.
		0010		Connects FRT ch.2 of MFT unit0 to OCU/ICU/ADCMP ch.(1) of MFT unit0.
		0011		Connects FRT ch.0 of MFT unit1 to OCU/ICU/ADCMP ch.(1) of MFT unit0.
		0100		Connects FRT ch.0 of MFT unit2 to OCU/ICU/ADCMP ch.(1) of MFT unit0.
		0101	★	Connects FRT ch.1 of MFT unit1 to OCU/ICU/ADCMP ch.(1) of MFT unit0.
		0110	★	Connects FRT ch.1 of MFT unit2 to OCU/ICU/ADCMP ch.(1) of MFT unit0.
		0111	★	Connects FRT ch.2 of MFT unit1 to OCU/ICU/ADCMP ch.(1) of MFT unit0.
		1000	★	Connects FRT ch.2 of MFT unit2 to OCU/ICU/ADCMP ch.(1) of MFT unit0.
		Other		Setting prohibited

Table 4-34 OCFS, ICFS, ACFS Register Settings for MFT unit1 (for Product Mounting 3 Multifunction Timer Units)

Register Name		Setting	TP3	Function
OCFS ICFS ACFS	FSO[3:0] FSI0[3:0] FSA0[3:0] ch.(0) side	0000		Connects FRT ch.0 of MFT unit1 to OCU/ICU/ADCMP ch.(0) of MFT unit1.
		0001		Connects FRT ch.1 of MFT unit1 to OCU/ICU/ADCMP ch.(0) of MFT unit1.
		0010		Connects FRT ch.2 of MFT unit1 to OCU/ICU/ADCMP ch.(0) of MFT unit1.
		0011		Connects FRT ch.0 of MFT unit0 to OCU/ICU/ADCMP ch.(0) of MFT unit1.
		0100		Connects FRT ch.0 of MFT unit2 to OCU/ICU/ADCMP ch.(0) of MFT unit1.
		0101	★	Connects FRT ch.1 of MFT unit0 to OCU/ICU/ADCMP ch.(0) of MFT unit1.
		0110	★	Connects FRT ch.1 of MFT unit2 to OCU/ICU/ADCMP ch.(0) of MFT unit1.
		0111	★	Connects FRT ch.2 of MFT unit0 to OCU/ICU/ADCMP ch.(0) of MFT unit1.
		1000	★	Connects FRT ch.2 of MFT unit2 to OCU/ICU/ADCMP ch.(0) of MFT unit1.
		Other		Setting prohibited
	FSO1[3:0] FSI1[3:0] FSA1[3:0] ch.(1) side	0000		Connects FRT ch.0 of MFT unit1 to OCU/ICU/ADCMP ch.(1) of MFT unit1.
		0001		Connects FRT ch.1 of MFT unit1 to OCU/ICU/ADCMP ch.(1) of MFT unit1.
		0010		Connects FRT ch.2 of MFT unit1 to OCU/ICU/ADCMP ch.(1) of MFT unit1.
		0011		Connects FRT ch.0 of MFT unit0 to OCU/ICU/ADCMP ch.(1) of MFT unit1.
		0100		Connects FRT ch.0 of MFT unit2 to OCU/ICU/ADCMP ch.(1) of MFT unit1.
		0101	★	Connects FRT ch.1 of MFT unit0 to OCU/ICU/ADCMP ch.(1) of MFT unit1.
		0110	★	Connects FRT ch.1 of MFT unit2 to OCU/ICU/ADCMP ch.(1) of MFT unit1.
		0111	★	Connects FRT ch.2 of MFT unit0 to OCU/ICU/ADCMP ch.(1) of MFT unit1.
		1000	★	Connects FRT ch.2 of MFT unit2 to OCU/ICU/ADCMP ch.(1) of MFT unit1.
		Other		Setting prohibited

Table 4-35 OCFS, ICFS, ACFS Register Settings for MFT unit2 (for Product Mounting 3 Multifunction Timer Units)

Register Name		Setting	TP3	Function
OCFS ICFS ACFS	FSO[3:0] FSI0[3:0] FSA0[3:0] ch.(0) side	0000		Connects FRT ch.0 of MFT unit2 to OCU/ICU/ADCMP ch.(0) of MFT unit2.
		0001		Connects FRT ch.1 of MFT unit2 to OCU/ICU/ADCMP ch.(0) of MFT unit2.
		0010		Connects FRT ch.2 of MFT unit2 to OCU/ICU/ADCMP ch.(0) of MFT unit2.
		0011		Connects FRT ch.0 of MFT unit0 to OCU/ICU/ADCMP ch.(0) of MFT unit2.
		0100		Connects FRT ch.0 of MFT unit1 to OCU/ICU/ADCMP ch.(0) of MFT unit2.
		0101	★	Connects FRT ch.1 of MFT unit0 to OCU/ICU/ADCMP ch.(0) of MFT unit2.
		0110	★	Connects FRT ch.1 of MFT unit1 to OCU/ICU/ADCMP ch.(0) of MFT unit2.
		0111	★	Connects FRT ch.2 of MFT unit0 to OCU/ICU/ADCMP ch.(0) of MFT unit2.
		1000	★	Connects FRT ch.2 of MFT unit1 to OCU/ICU/ADCMP ch.(0) of MFT unit2.
		Other		Setting prohibited
	FSO1[3:0] FSI1[3:0] FSA1[3:0] ch.(1) side	0000		Connects FRT ch.0 of MFT unit2 to OCU/ICU/ADCMP ch.(1) of MFT unit2.
		0001		Connects FRT ch.1 of MFT unit2 to OCU/ICU/ADCMP ch.(1) of MFT unit2.
		0010		Connects FRT ch.2 of MFT unit2 to OCU/ICU/ADCMP ch.(1) of MFT unit2.
		0011		Connects FRT ch.0 of MFT unit0 to OCU/ICU/ADCMP ch.(1) of MFT unit2.
		0100		Connects FRT ch.0 of MFT unit1 to OCU/ICU/ADCMP ch.(1) of MFT unit2.
		0101	★	Connects FRT ch.1 of MFT unit0 to OCU/ICU/ADCMP ch.(1) of MFT unit2.
		0110	★	Connects FRT ch.1 of MFT unit1 to OCU/ICU/ADCMP ch.(1) of MFT unit2.
		0111	★	Connects FRT ch.2 of MFT unit0 to OCU/ICU/ADCMP ch.(1) of MFT unit2.
		1000	★	Connects FRT ch.2 of MFT unit1 to OCU/ICU/ADCMP ch.(1) of MFT unit2.
		Other		Setting prohibited

4.8.3 Product Mounting Three MFT's (TYPE6-M4 product)

Figure 4-57 shows a diagram of the FRT connected between multifunction timer units for a product mounting 3 multifunction timer units (TYPE6-M4 product).

Figure 4-57 Diagram of FRT Connected between Multifunction Timer Units (for Product Mounting 3 Multifunction Timer Units)

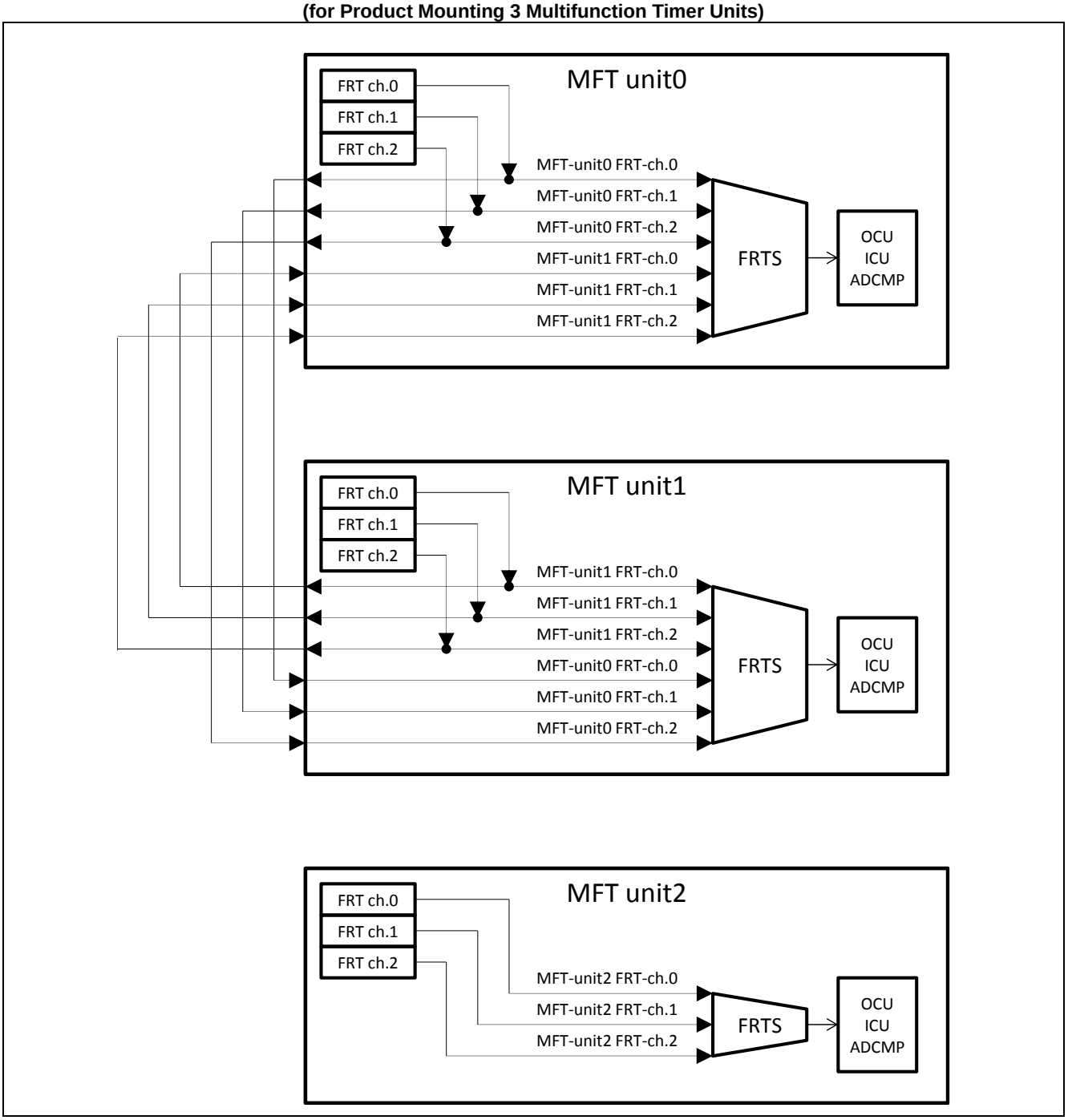


Table 4-36, Table 4-37, and Table 4-38 show the OCFS, ICFS, and ACFS register setting values for the MFT-unit0, MFT-unit1, and MFT-unit2 installed multifunction timer units and the FRT selected for connection. The settings for each register are listed in the table.

Table 4-36 OCFS, ICFS, ACFS Register Settings for MFT unit0 (TYPE6-M4 product)

Register Name		Setting	Function
OCFS ICFS ACFS	FSO0[3:0] FSI0[3:0] FSA0[3:0] ch.(0) side	0000	Connects FRT ch.0 of MFT unit0 to OCU/ICU/ADCMP ch.(0) of MFT unit0.
		0001	Connects FRT ch.1 of MFT unit0 to OCU/ICU/ADCMP ch.(0) of MFT unit0.
		0010	Connects FRT ch.2 of MFT unit0 to OCU/ICU/ADCMP ch.(0) of MFT unit0.
		0011	Connects FRT ch.0 of MFT unit1 to OCU/ICU/ADCMP ch.(0) of MFT unit0.
		0100	Connects FRT ch.1 of MFT unit1 to OCU/ICU/ADCMP ch.(0) of MFT unit0.
		0101	Connects FRT ch.2 of MFT unit1 to OCU/ICU/ADCMP ch.(0) of MFT unit0.
		Other	Setting prohibited
	FSO1[3:0] FSI1[3:0] FSA1[3:0] ch.(1) side	0000	Connects FRT ch.0 of MFT unit0 to OCU/ICU/ADCMP ch.(1) of MFT unit0.
		0001	Connects FRT ch.1 of MFT unit0 to OCU/ICU/ADCMP ch.(1) of MFT unit0.
		0010	Connects FRT ch.2 of MFT unit0 to OCU/ICU/ADCMP ch.(1) of MFT unit0.
		0011	Connects FRT ch.0 of MFT unit1 to OCU/ICU/ADCMP ch.(1) of MFT unit0.
		0100	Connects FRT ch.1 of MFT unit1 to OCU/ICU/ADCMP ch.(1) of MFT unit0.
		0101	Connects FRT ch.2 of MFT unit1 to OCU/ICU/ADCMP ch.(1) of MFT unit0.
		Other	Setting prohibited

Table 4-37 OCFS, ICFS, ACFS Register Settings for MFT unit1 (TYPE6-M4 product)

Register Name		Setting	Function
OCFS ICFS ACFS	FSO0[3:0] FSI0[3:0] FSA0[3:0] ch.(0) side	0000	Connects FRT ch.0 of MFT unit1 to OCU/ICU/ADCMP ch.(0) of MFT unit1.
		0001	Connects FRT ch.1 of MFT unit1 to OCU/ICU/ADCMP ch.(0) of MFT unit1.
		0010	Connects FRT ch.2 of MFT unit1 to OCU/ICU/ADCMP ch.(0) of MFT unit1.
		0011	Connects FRT ch.0 of MFT unit0 to OCU/ICU/ADCMP ch.(0) of MFT unit1.
		0100	Connects FRT ch.1 of MFT unit0 to OCU/ICU/ADCMP ch.(0) of MFT unit1.
		0101	Connects FRT ch.2 of MFT unit0 to OCU/ICU/ADCMP ch.(0) of MFT unit1.
		Other	Setting prohibited
	FSO1[3:0] FSI1[3:0] FSA1[3:0] ch.(1) side	0000	Connects FRT ch.0 of MFT unit1 to OCU/ICU/ADCMP ch.(1) of MFT unit1.
		0001	Connects FRT ch.1 of MFT unit1 to OCU/ICU/ADCMP ch.(1) of MFT unit1.
		0010	Connects FRT ch.2 of MFT unit1 to OCU/ICU/ADCMP ch.(1) of MFT unit1.
		0011	Connects FRT ch.0 of MFT unit0 to OCU/ICU/ADCMP ch.(1) of MFT unit1.
		0100	Connects FRT ch.1 of MFT unit0 to OCU/ICU/ADCMP ch.(1) of MFT unit1.
		0101	Connects FRT ch.2 of MFT unit0 to OCU/ICU/ADCMP ch.(1) of MFT unit1.
		Other	Setting prohibited

Table 4-38 OCFS, ICFS, ACFS Register Settings for MFT unit2 (TYPE6-M4 product)

Register Name		Setting	Function
OCFS ICFS ACFS	FSO0[3:0] FSI0[3:0] FSA0[3:0] ch.(0) side	0000	Connects FRT ch.0 of MFT unit2 to OCU/ICU/ADCMP ch.(0) of MFT unit2.
		0001	Connects FRT ch.1 of MFT unit2 to OCU/ICU/ADCMP ch.(0) of MFT unit2.
		0010	Connects FRT ch.2 of MFT unit2 to OCU/ICU/ADCMP ch.(0) of MFT unit2.
		Other	Setting prohibited
	FSO1[3:0] FSI1[3:0] FSA1[3:0] ch.(1) side	0000	Connects FRT ch.0 of MFT unit2 to OCU/ICU/ADCMP ch.(1) of MFT unit2.
		0001	Connects FRT ch.1 of MFT unit2 to OCU/ICU/ADCMP ch.(1) of MFT unit2.
		0010	Connects FRT ch.2 of MFT unit2 to OCU/ICU/ADCMP ch.(1) of MFT unit2.
		Other	Setting prohibited

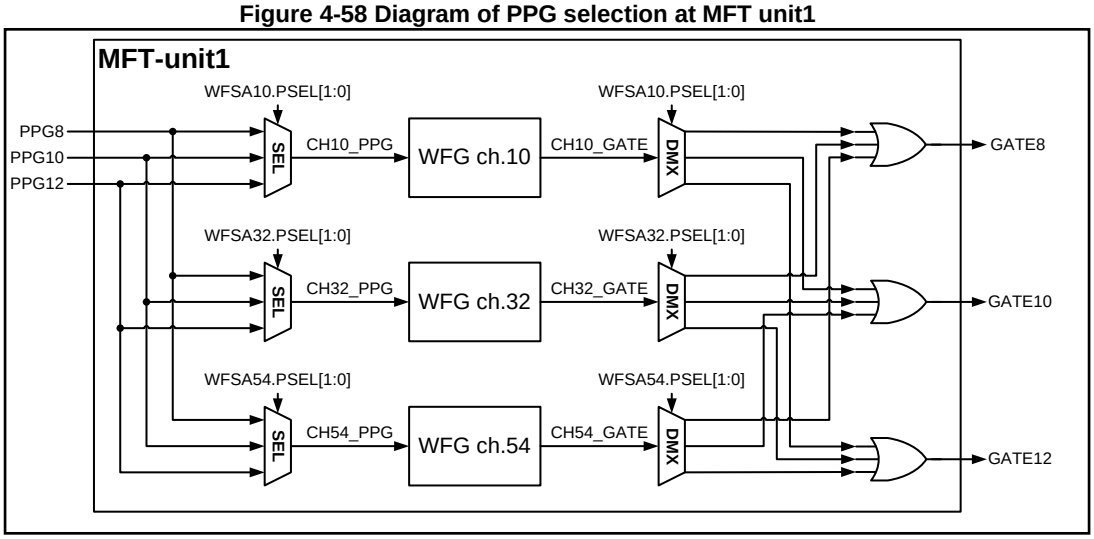
4.9 PPG Timer Unit Connected to WFG

The PPG timer unit to be connected to WFG varies depending on the multifunction timer unit used. This section explains the connection of the PPG timer unit and the selection method.

4.9.1 MFT unit1

PPG timer unit ch.8, ch.10 and ch.12 are connected to WFG of MFT unit1, as shown in Figure 4-58.

Figure 4-58 Diagram of PPG selection at MFT unit1



In case of WFG in MFT unit1, the following is selected by the setting of the PSEL[1:0].

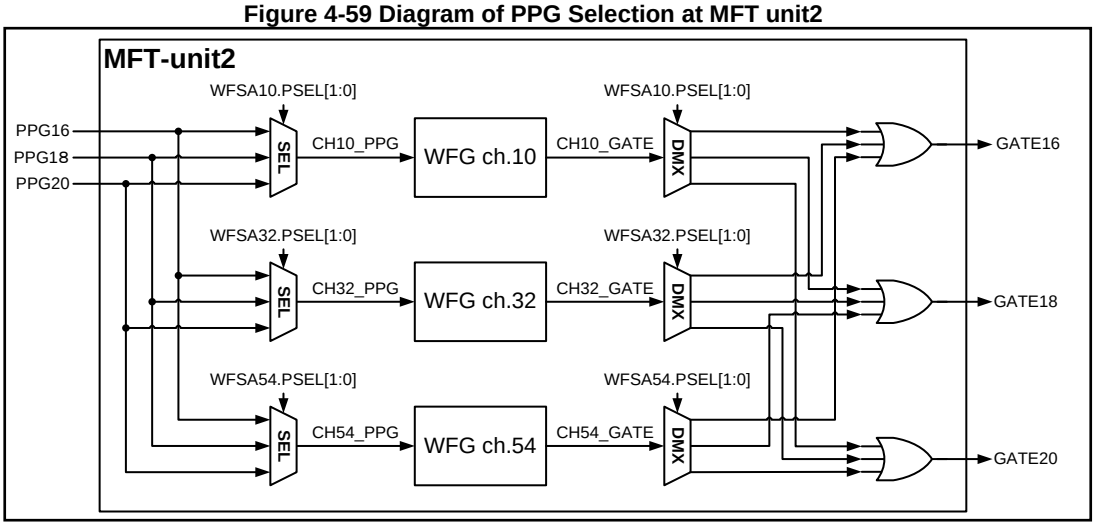
[bit9:8] PSEL[1:0]

Process	bit9:8	Function
Write	00	Sets the output destination of the GATE signal to PPG timer unit ch.8. Sets the input source of the PPG signal to PPG timer unit ch.8.
	01	Sets the output destination of the GATE signal to PPG timer unit ch.10. Sets the input source of the PPG signal to PPG timer unit ch.10.
	10	Sets the output destination of the GATE signal to PPG timer unit ch.12. Sets the input source of the PPG signal to PPG timer unit ch.12.
	11	Setting is prohibited.
Read	-	Reads the register setting.

4.9.2 MFT unit2

PPG timer unit ch.16, ch.18 and ch.20 are connected to WFG of MFT unit2, as shown in Figure 4-59.

Figure 4-59 Diagram of PPG Selection at MFT unit2



In case of WFG in MFT unit2, the following is selected by the setting of the PSEL[1:0].

[bit9:8] PSEL[1:0]

Process	bit9:8	Function
Write	00	Sets the output destination of the GATE signal to PPG timer unit ch.16. Sets the input source of the PPG signal to PPG timer unit ch.16.
	01	Sets the output destination of the GATE signal to PPG timer unit ch.18. Sets the input source of the PPG signal to PPG timer unit ch.18.
	10	Sets the output destination of the GATE signal to PPG timer unit ch.20. Sets the input source of the PPG signal to PPG timer unit ch.20.
	11	Setting is prohibited.
Read	-	Reads the register setting.

4.10 Treatment of Event Detect Register and Interrupt

This section provides notes on the event detect register in the multifunction timer unit, the operation and control of interrupt-related circuits.

4.10.1 List of Event Detection Registers and Interrupt Enable Registers

For the list of event detection registers, interrupt enable/mask registers, and interrupt signals, see Table 4-39.

Table 4-39 List of Event Detect Registers and Interrupt Enable/Mask Registers

Block	Target Event	Event Detection Register	Interrupt Enable/Mask Register	Interrupt Signal Name	Class
FRT ch.0	FRT0 == 0x0000 detect	TCSA0:IRQZF	TCSA0:IRQZE	Zero value detect interrupt	1
FRT ch.1	FRT1 == 0x0000 detect	TCSA1:IRQZF	TCSA1:IRQZE	Zero value detect interrupt	1
FRT ch.2	FRT2 == 0x0000 detect	TCSA2:IRQZF	TCSA2:IRQZE	Zero value detect interrupt	1
FRT ch.0	FRT0 == TCCP0 detect	TCSA0:ICLR	TCSA0:ICRE	Peak value detect interrupt	1
FRT ch.1	FRT1 == TCCP1 detect	TCSA1:ICLR	TCSA1:ICRE	Peak value detect interrupt	1
FRT ch.2	FRT2 == TCCP2 detect	TCSA2:ICLR	TCSA2:ICRE	Peak value detect interrupt	1
OCU ch.0	FRT == OCCP0 detect	OCSA10:IOP0	OCSA10:IOE0	Match detect interrupt	1
OCU ch.1	FRT == OCCP1 detect	OCSA10:IOP1	OCSA10:IOE1	Match detection interrupt	1
OCU ch.2	FRT == OCCP2 detection	OCSA32:IOP0	OCSA32:IOE0	Match detection interrupt	1
OCU ch.3	FRT == OCCP3 detection	OCSA32:IOP1	OCSA32:IOE1	Match detection interrupt	1
OCU ch.4	FRT == OCCP4 detect	OCSA54:IOP0	OCSA54:IOE0	Match detect interrupt	1
OCU ch.5	FRT == OCCP5 detect	OCSA54:IOP1	OCSA54:IOE1	Match detect interrupt	1
ICU ch.0	Valid edge detect	ICSA10:ICP0	ICSA10:ICE0	Input signal edge detect interrupt	1
ICU ch.1	Valid edge detect	ICSA10:ICP1	ICSA10:ICE1	Input signal edge detect interrupt	1
ICU ch.2	Valid edge detect	ICSA32:ICP0	ICSA32:ICE0	Input signal edge detect interrupt	1
ICU ch.3	Valid edge detect	ICSA32:ICP1	ICSA32:ICE1	Input signal edge detect interrupt	1
NZCL	Motor emergency stop signal input (Digital path)	WFIR:DTIFA	NZCL:DIMA	DTIF interrupt	2
NZCL	Motor emergency stop signal input (Analog path)	WFIR:DTIFB	NZCL:DIMB		2
WFG ch.10	Timer count end	WFIR:TMIF10	NZCL:WIM10	WFG10 reload timer interrupt	2
WFG ch.32	Timer count end	WFIR:TMIF32	NZCL:WIM32	WFG32 reload timer interrupt	2
WFG ch.54	Timer count end	WFIR:TMIF54	NZCL:WIM54	WFG54 reload timer interrupt	2

4.10.2 Configuration of Circuit

In Table 4-39, for the configuration of generating circuit of event detection register, interrupt enable register, and interrupt signal for Class 1 see Figure 4-60; for Class 2 see Figure 4-61.

Figure 4-60 Configuration of Interrupt Signal Generation Circuit (Class 1)

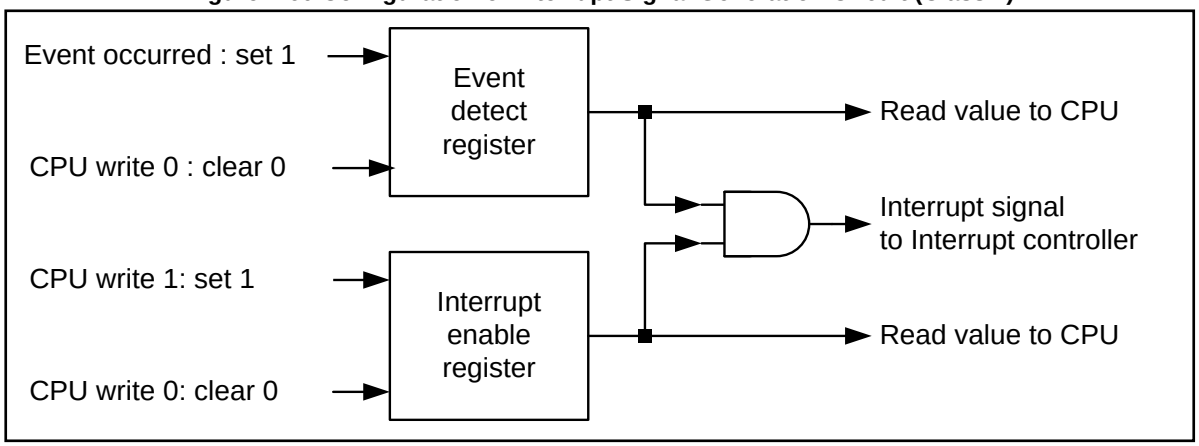
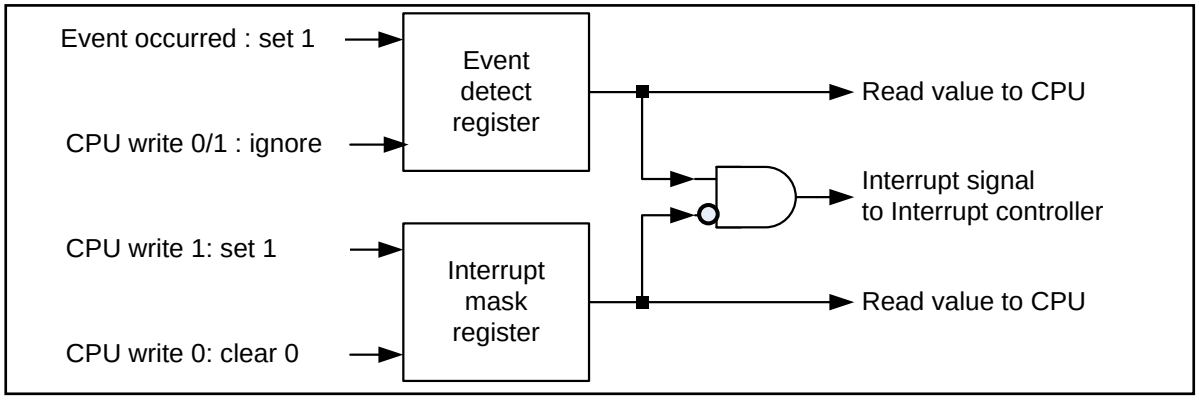


Figure 4-61 Configuration of Interrupt Signal Generation Circuit (Class 2)



■ Event detect register

Each function block has an event detect register to notify CPU that a specific event (e.g. detection of the rising edge of the input signal at ICU) has occurred. This register indicates 0 when the relevant event has not occurred. It is set to 1, when the event occurs.

■ Interrupt enable register/interrupt mask register

There is an interrupt enable register to specify whether or not to notify CPU of the above event as an interrupt. For Class 1, interrupt enable register is described, and for Class 2, interrupt mask register is described. As shown in the Figure 4-60 and Figure 4-61, the logical AND of the values in the event detect register and the interrupt enable register (interrupt mask register) is connected to the interrupt controller (NVIC) as an interrupt signal.

■ Writing to and reading from each register

The event detect register can be read from CPU at any time, regardless of the value in the interrupt enable register (interrupt mask register). It can be cleared, but cannot be set.

The interrupt enable register (or interrupt mask register) allows any value to be set from CPU and always can be read. A value is not rewritten by MFT.

- Operation when the interrupt is disabled

  When the interrupt enable register is set to 0 or the interrupt mask register is set to 1, the interrupt is enabled.

  Even when an event occurs and 1 is set to the event detect register, an interrupt signal is not asserted and no interrupt occurs. In this case, the occurrence of the event can be recognized by reading from the event detect register regularly via CPU.

- Operation when the interrupt is enabled

  When the interrupt enable register is set to 1 or the interrupt mask register is set to 0, the interrupt is disabled.

  When an event occurs and 1 is set to the event detect register, the interrupt signal is asserted and an interrupt occurs. CPU can recognize the occurrence of the event by the interrupt.

- Clearing Event Detect Register in Class 1

  Generally, the event detect register cannot be cleared automatically. In order to recognize the occurrence of the next event after 1 is set to the event detect register, the event detect register must be cleared via CPU beforehand. If it is not cleared via CPU, CPU cannot recognize the occurrence of the succeeding events.

- Returning from Interrupt Processing

  When an interrupt is processed using an interrupt signal, it is necessary to clear the event detect register when returning from the interrupt processing, deassert the interrupt signal, and then return from the interrupt. Returning from an interrupt without deasserting the interrupt signal will result in the same interrupt process taking place again with no way out of that process.

4.10.3 Notes When Event Detect Register of Class 1 is Cleared

The write value and read value of the event detect register in Class 1 have the following meanings:

- Writing 0: Clears the register.
- Writing 1: Does nothing.
- Reading 0: No event occurred.
- Reading 1: Event occurred

Because the event detect register in Class 1 is in the configuration described above, when a value is read from the event detect register via CPU, the value cannot be normally written back. This is due to the following reason. When 0 is successfully read from the event detect register at a certain point, it indicates that the event has yet to occur at that point. Next, writing the value back to the event detect register without change (i.e. writing 0) means instructing the event detect register to be cleared. If an event occurs during the period from the reading via CPU to the writing the value back, the register will be cleared, preventing that event from being recognized. For the above reason, when writing to the event detect register, "1" must be always written (i.e. doing nothing), unless the register is intended to be cleared. An example is provided below.

The ICSA10 register is in the following configuration based on the 8-bit register.

bit	7	6	5	4	3	2	1	0
field	ICP1	ICP0	ICE1	ICE0	EG1[1:0]		EG0[1:0]	

The ICP1 and ICP0 registers are event detect registers that notify CPU of an event upon edge detection of input signal at ICU-ch.1 and ICU-ch.0, respectively. If 01111111 is read from these registers at a certain point, for example, it indicates that a valid edge is detected (ICP0=1) at ch.0 and no valid edge is detected (ICP1=0) at ch.1

Then, write 0 back to bit6 in order to clear the ICP0 register. At that point, it is not possible to set the value in the ICP0 register to 0 and write 00111111 back due to the reason explained above. It is because information about any possible detection of an event at ch.1 will be cleared during the period from reading from the register to writing the value back. Therefore, in order to clear the ICP0 register, it is necessary to write 10111111 back with bit6=0 and bit7=1.

4.10.4 Read Value Mask Function at RMW (Read Modify Write) Access

Since the above procedure is complicated, a masking function is provided to mask the read value of the event detect register to 1 at RMW access for the value to be written back.

In this model, RMW access occurs, when write access is made to the bit-banding alias area. Write access to the bit-banding alias area is the RMW access used to read all of the register bits in the address area where the target bit exists, rewrite only the target bit and write all the register bits back.

In the example of the ICSA10 register provided earlier, assume that the value 01111111 is read at a certain point. To write 0 to bit6 so that the ICP0 register will be cleared, write access to the normal address area requires bit7=1 and bit6=0 to be written as described above. However, if 0 is written to bit6 by write access to the bit-banding alias area, the hardware performs the following operation:

- It reads the value in the ICSA10 register.
- At this point, the ICP1 and ICP0 registers return a read value masked to 1 because of the RMW access. In other words, the value to be read is 11111111.
- Write back the value 10111111 to the ICSA10 register, where only the value of bit6 (ICP0) has been replaced with 0.

Bit7 cannot be cleared because the device operates as described above. How to write back the value of bit6 is described in this example. In case of writing back the values of bit7 and bit5 to bit0, the read values of bit7 and bit6 are masked to 1 also; therefore, it is unnecessary to consider the writing back value. For this reason, this configuration allows rewriting the register without considering the writing back value to the event detect register in case of writing access to the bit-banding alias area.

* Read access to the bit-banding alias area is not RMW access; therefore the value of the event detect register is unmasked when reading.

4.10.5 Clearing Event Detect Register in Class 2

To clear the event detect register in Class 2, write 1 to the clear register in a different register. The written value to the event detect register is ignored. So, the RMW access is not required.

5. Multifunction Timer Control Examples

This section presents explanations based on control examples and setting procedures for the multifunction timer.

5.1. Multifunction Timer Control Example 1
5.2. Multifunction Timer Control Example 2

5.1 Multifunction Timer Control Example 1

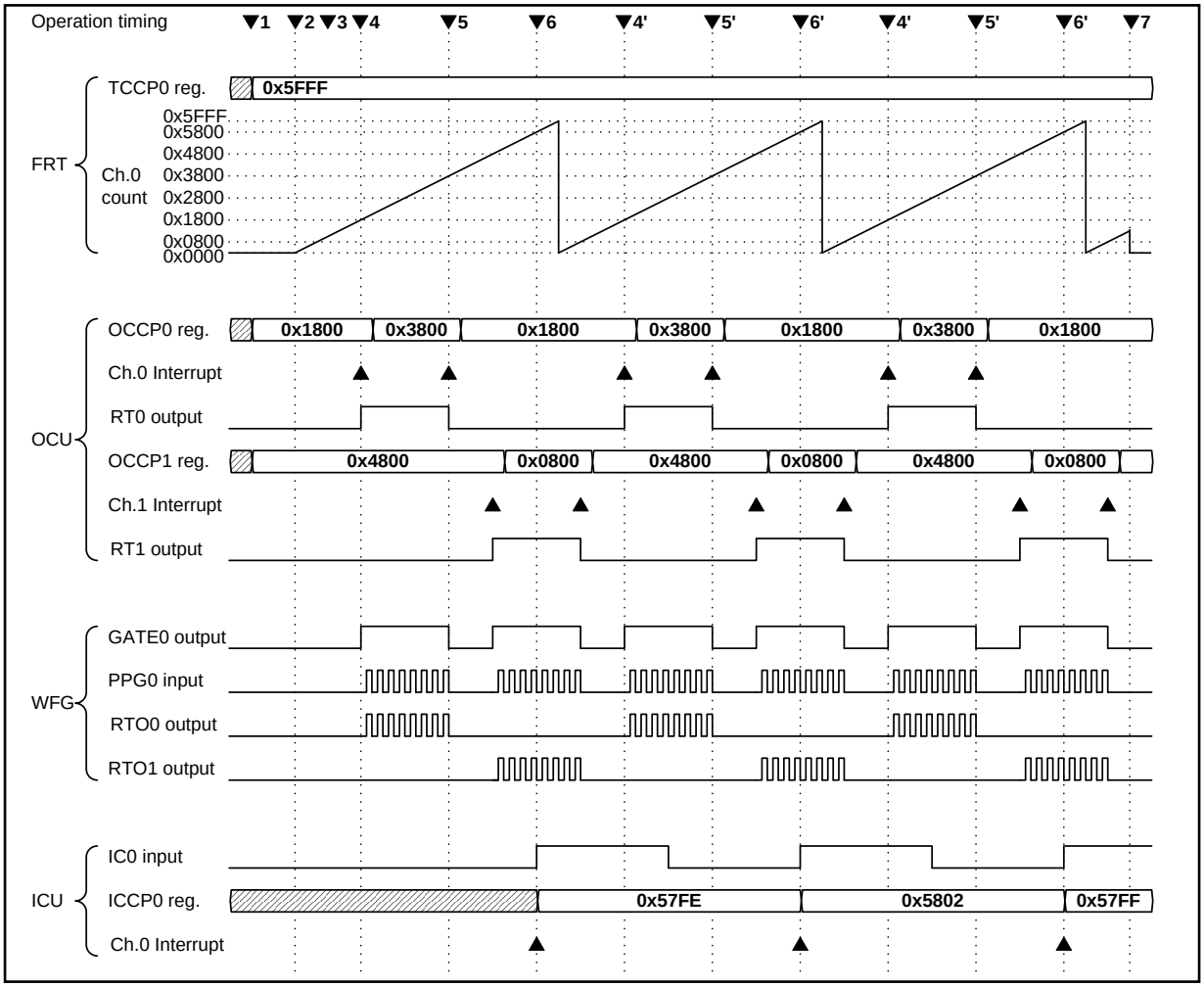
Multifunction Timer Control Example 1 presents cases where the function blocks are operated in the modes shown below.

FRT:	Up-count mode without interrupt
OCU:	RT output reversal and interrupt generated when FRT and OCCP match (Same as OCU Setting Examples 1 and 5)
WFG:	RT-PPG mode, GATE signal generation, PPG signal superimposing
ICU:	Rising edge detection mode, with interrupt

5.1.1 Timechart

The main registers for the MFT blocks and input/output signal timecharts are shown in Figure 5-1.

Figure 5-1 Timechart of Main Registers and Input/Output Signals for Each Block



The figure above shows the operation timing, FRT operation, OCU operation, WFG operation, and ICU operation from top to bottom. The cases shown in Operation timing 1 to 7 describe what is controlled by the CPU and the operation of each function block. Specific examples of CPU register settings are shown for each timing. For details of the register settings, see 3 Registers of the Multifunction Timer. In addition to the above, it should also be noted that the LSI I/O port block, interrupt control block, and PPG must be set separately.

5.1.2 FRT and OCU Settings and Operation

- Operation timing 1

  The FRT-ch.0 initial settings (up-count mode) are made (TCSA0 register write).

  The FRT-ch.0 count cycle is set (TCCP0 register write). In this example, 0x5FFF is set. The FRT count cycle is 78.6432 ms when the prescaler is set to 1/128 and PCLK is set to 40 MHz.

  The OCU-ch.0 and ch.1 initial settings are set. Operation is set in OCU Setting Examples 1 and 5 in 4.1 Descriptions of FRT Operation (RT output reversal and interrupt generated each time that FRT and OCCP match). Also, the initial output level of the OCU-ch.0 and ch.1 output signals (RT0, RT1) is specified (Register writes for OCFS10, OCSA10, OCSB10, OCSD10, OCSE0, and OCSE1).

  The initial value is set for the time at which the OCU-ch.0 output signal (RT0) (OCCP0 register write) is changed. In this example, 0x1800 is set. The written value is written to the buffer register and then transferred to the OCCP0 register.

  The initial value is set for the time at which the OCU-ch.1 output signal (RT1) is changed. (OCCP1 register write) In this example, 0x4800 is set. The written value is written to the buffer register and then transferred to the OCCP1 register.

- Operation timing 2

  A command is issued to FRT-ch.0 to start the count operation (TCSA0 register write).

  As shown in Figure 5-1, FRT-ch.0 starts counting from 0x0000 and continues the up-count operation until the TCCP value (=0x5FFF) is reached. Then, the value returns to 0x0000, and the count operation continues.

- Operation timing 3

  An operation allows command is issued to OCU-ch.0 and ch.1 (OCSA10 register write).

- Operation timing 4

  When OCU-ch.0 detects that the FRT counter value has reached 0x1800 and matches the OCCP0 setting value, the output signal (RT0) changes from the Low level to the High level. It also generates an interrupt to the CPU.

  The CPU determines that an interrupt has been generated from OCU-ch.0 because 1 has been set to the match detection flag of OCU-ch.0 (OCSA10 register read). The timing of changing the OCU-ch.0 output signal (RT0) is updated to "0x3800" (OCCP0 register write). The CPU clears the match detection flag and returns from the interrupt (OCSA10 register write).

- Operation timing 5

  When OCU-ch.0 detects that the FRT counter value matches the OCCP0 setting value, the output signal (RT0) changes from the High level to the Low level. It also generates an interrupt to the CPU.

  The CPU determines that an interrupt has been generated from OCU-ch.0 (OCSA10 register read). The OCCP0 register of OCU-ch.0 is updated to 0x1800 (OCCP0 register write). The CPU clears the match detection flag and returns from the interrupt (OCSA10 register write).

- Operation timing 4’ and 5’

  After this, the operations in 4 and 5 are repeated so that the RT0 output signal shown in Figure 5-1 is obtained. For the RT1 output signal, the OCCP1 register value is also updated in the same way whenever an interrupt is generated.

5.1.3 WFG Settings and Operation

- Operation timing 1

RT-PPG mode operation is set to WFG-ch.10 (WFSA10 register write).

- Operation timing 2

WFG asserts the GATE0 signal when the RT0 signal from OCU-ch.0 is changed to the High level, and a start instruction is issued to PPG-ch.0. When the GATE0 signal is asserted, PPG-ch.0 starts output of the PPG0 signal. WFG superimposes and outputs the PPG signal to RTO0 while the RT0 signal remains at the High level.

- Operation timing 5

When the RT0 signal is changed to the Low level, WFG deasserts the GATE0 signal, and a stop instruction is issued to PPG-ch.0. PPG-ch.0 sets the PPG signal to the Low level and stops the output. WFG sets the RTO0 signal to the Low level and stops the output.

WFG performs the same operation to the RT1 signal from OCU-ch.1 and superimposes and outputs the PPG0 signal to RTO1. The WFG function can be used to output the DC chopper control waveform to RTO0 and RTO1 as shown in Figure 5-1.

5.1.4 ICU Settings and Operation

- Operation timing 1

The ICU-ch.0 initial settings are made. The rising edge detection operation of the input signal is set (ICFS10, ICSA10 register write).

- Operation timing 6

When a rising edge is detected in the input signal (IC0), ICU-ch.0 stores the FRT's count value in the ICCP0 register. It also generates an interrupt to the CPU.

The CPU determines that an interrupt has been generated from ICU-ch.0 because "1" has been set to the valid edge detection register of ICU-ch.0 (ICSA10 register read). The CPU captures the position of the rising edge of the signal (ICCP0 register read). The CPU clears the valid edge detection register(ICP0) and returns from the interrupt (ICSA10 register write).

5.1.5 Completion of Process

- Operation timing 7

The process in Operation timing 7 shows the procedure for completing output of the PWM signal from the CPU.

Operation of OCU-ch.0 and ch.1 is prohibited, and the OCU-ch.0 and ch.1 output signal (RT0, RT1) levels are set (OCSA10, OCSB10 register write).

Operation of ICU-ch.0 is prohibited (ICSA10 register write).

When the output of OCU stops, WFG does not allow changing of the output signal.

A count operation stop instruction is issued to FRT-ch.0 (TCSA0 register write).

5.1.6 Other Channel Processes

The example above describes operation with two channels of OCU, one channel of WFG, and one channel of ICU. However, if OCU-6ch, WFG-3ch, and ICU-3ch are connected to the same FRT to perform linked control, three-phase motor control can be achieved.

5.1.7 Details of Register Setting Values

Details of the register setting values for Multifunction Timer Control Example 1 are shown in Table 5-1 to Table 5-4.

The meanings of the abbreviations used in the AC fields and Value fields in Table 5-1 to Table 5-4 are shown below.

AC (Access)	WW	Word write access
	HW	Half-word write access
	BW	Byte write access
	HR	Half-word read access
	BR	Byte read access
Value	Numerical value	Indicates the value of the bit field.
	NM	Indicates either writing the same value as the register value that is already set or reading from the register to write back the original value (No Modify).
	1(RMW)	Indicates writing of 1 if register clear is not intended. If updating by RMW access (see 4.10 Treatment of Event Detect Register and Interrupt), this indicates that the read value can be written back.
	Other	Indicates the setting bits of other channels and no relation to this explanatory example.
	DC	Indicates that the read value has no relation (Don't Care).

Table 5-1 Control Example 1 Register Settings 1

Timing	Register	AC	Bit Field	Value	Setting Description
1	TCSA0	HW	CLK[3:0]	0111	Clock division prescaler setting: 1/128
			SCLR	0	Soft clear: Nothing is performed
			MODE	0	Count mode setting: Up-count mode
			STOP	1	FRT count operation: Count stop
			BFE	1	TCCP buffer function: Enable
			ICRE	0	Peak value detection interrupt: Prohibit
			ICLR	0	Peak value detection: Clear
			Reserved	000	-
			IRQZE	0	Zero value detection interrupt: Prohibit
			IRQZF	0	Zero value detection: Clear
			ECKE	0	Selection of clock used: Internal clock
	TCCP0	HW	TCCP	0x5FFF	Sets the FRT cycle
	OCFS10	BW	FSO0[3:0]	0000	FRT connected to ch.0: FRT ch.0
			FSO1[3:0]	0000	FRT connected to ch.1: FRT ch.0
	OCSA10	BW	CST0	0	ch.0 operation state: Operation prohibit
			CST1	0	ch.1 operation state: Operation prohibit
			Reserved	00	ch.1 OCCP buffer function: Disable
			IOE0	1	ch.0 interrupt: Allow
			IOE1	1	ch.1 interrupt: Allow
			IOP0	0	ch.0 match detection: Clear
			IOP1	0	ch.1 match detection: Clear
	OCSB10	BW	OTD0	0	RT0 output level initial setting: Low
			OTD1	0	RT1 output level initial setting: Low
			Reserved	00	-
			CMOD	0	Operation mode: Specifies FM4 mode
			Reserved	00	-
			FM4	1	Operation mode: Specifies FM4 mode
	OCSD10	HW	OCCP0BUFE[1:0]	00	ch.0 OCCP buffer function: Disable
			OCCP1BUFE[1:0]	00	ch.1 OCCP buffer function: Disable
			OCSE0BUFE[1:0]	00	ch.0 OCSE buffer transfer: Disable
			OCSE1BUFE[1:0]	00	ch.1 OCSE buffer transfer: Disable
			OPBM0	0	ch.0 OCCP buffer interrupt mask link transfer: Off
			OPBM1	0	ch.1 OCCP buffer interrupt mask link transfer: Off
			OEBM0	0	ch.0 OCSE buffer interrupt mask link transfer: Off
			OEBM1	0	ch.1 OCSE buffer interrupt mask link transfer: Off
			OFEX0	0	ch.0 matched condition extension: Off
			OFEX1	0	ch.0 matched condition extension: Off
			Reserved	00	-
	OCSE0	HW	OCSE0[15:0]	0x0FFF	Specifies ch.0 operation: See OCU Setting Example 1.
	OCSE1	WW	OCSE1[31:0]	0x0FF00FFF	Specifies ch.1 operation: See OCU Setting Example 5.
	OCCP0	HW	OCCP	0x1800	Specifies ch.0 change timing
	OCCP1	HW	OCCP	0x4800	Specifies ch.1 change timing

Table 5-2 Control Example 1 Register Settings 2

Timing	Register	AC	Bit Field	Value	Setting Description
1	WFSA10	HW	DCK[2:0]	000	Clock division prescaler setting: 1/1 (setting disabled)
			TMD[2:0]	001	Operation mode: Selects RT-PPG mode
			GTEN[1:0]	11	Gate: GATE0 = RT0 | RT1
			PSEL[1:0]	00	Connecting PPG: PPG0
			PGEN[1:0]	11	PPG: RTO0=RT0&PPG0, RTO1=RT1&PPG0
			DMOD[1:0]	00	Output polarity: Positive polarity
			Reserved	00	-
	ICFS10	BW	FSI0[3:0]	0000	FRT connected to ch.0: FRT ch.0
			FSI1[3:0]	Other	-
	ICSA10	BW	EG0[1:0]	01	ch.0 operation state: Operation enabled, rising edge
			EG1[1:0]	Other	-
			ICE0	1	ch.0 interrupt: Allow
			ICE1	Other	-
			ICP0	0	ch.0 edge detection: Clear
			ICP1	Other	-
2	TCSA0	HW	CLK[3:0]	NM	Clock division prescaler setting:
			SCLR	NM	Soft clear:
			MODE	NM	Count mode setting:
			STOP	0	FRT count operation: Counting is started
			BFE	NM	TCCP buffer function:
			ICRE	NM	Peak value detection interrupt:
			ICLR	1(RMW)	Peak value detection: Nothing is performed
			Reserved	NM	-
			IRQZE	NM	Zero value detection interrupt:
			IRQZF	1(RMW)	Zero value detection: Nothing is performed
			ECKE	NM	Selection of clock used:
3	OCSA10	BW	CST0	1	ch.0 operation state: Operation allowed
			CST1	1	ch.1 operation state: Operation allowed
			Reserved	00	
			IOE0	NM	ch.0 interrupt:
			IOE1	NM	ch.1 interrupt:
			IOP0	1	ch.0 match detection: Nothing is performed
			IOP1	1	ch.1 match detection: Nothing is performed

Table 5-3 Control Example 1 Register Settings 3

Timing	Register	AC	Bit Field	Value	Setting Description
4	OCSA10	BR	CST0	DC	ch.0 operation state:
			CST1	DC	ch.1 operation state:
			Reserved	DC	
			IOE0	DC	ch.0 interrupt:
			IOE1	DC	ch.1 interrupt:
			IOP0	1	ch.0 match detection: Match detected
			IOP1	0	ch.1 match detection: Match not detected
	OCCP0	HW	OCCP0	0x3800	Specifies ch.0 change timing
	OCSA10	BW	CST0	NM	ch.0 operation state:
			CST1	NM	ch.1 operation state:
			Reserved	NM	
			IOE0	NM	ch.0 interrupt:
			IOE1	NM	ch.1 interrupt:
			IOP0	0	ch.0 match detection: Flag cleared
			IOP1	1(RMW)	ch.1 match detection: Nothing is performed
5	OCSA10	BR	CST0	DC	ch.0 operation state:
			CST1	DC	ch.1 operation state:
			Reserved	DC	
			IOE0	DC	ch.0 interrupt:
			IOE1	DC	ch.1 interrupt:
			IOP0	1	ch.0 match detection: Match detected
			IOP1	0	ch.1 match detection: Match not detected
	OCCP0	HW	OCCP0	0x1800	Specifies ch.0 change timing
	OCSA10	BW	CST0	NM	ch.0 operation state:
			CST1	NM	ch.1 operation state:
			Reserved	DC	
			IOE0	NM	ch.0 interrupt:
			IOE1	NM	ch.1 interrupt:
			IOP0	0	ch.0 match detection: Flag cleared
			IOP1	1(RMW)	ch.1 match detection: Nothing is performed

Table 5-4 Control Example 1 Register Settings 4

Timing	Register	AC	Bit Field	Value	Setting Description
6	ICSA10	BR	EG0[1:0]	DC	ch.0 operation state:
			EG1[1:0]	DC	ch.1 operation state:
			ICE0	DC	ch.0 interrupt:
			ICE1	DC	ch.1 interrupt:
			ICP0	1	ch.0 edge detection: Edge detected
			ICP1	0	ch.1 edge detection: Edge not detected
	ICCP0	HR	ICCP0	0x57FE	ch.0 capture value is captured
	ICSA10	BW	EG0[1:0]	NM	ch.0 operation state:
			EG1[1:0]	NM	ch.1 operation state:
			ICE0	NM	ch.0 interrupt:
			ICE1	NM	ch.1 interrupt:
			ICP0	0	ch.0 edge detection: Clear
			ICP1	1(RMW)	ch.1 edge detection: Nothing is performed
7	OCSA10	BW	CST0	0	ch.0 operation state: Prohibit
			CST1	0	ch.1 operation state: Prohibit
			Reserved	NM	
			IOE0	NM	ch.0 interrupt:
			IOE1	NM	ch.1 interrupt:
			IOP0	1	ch.0 match detection: Nothing is performed
			IOP1	1	ch.1 match detection: Nothing is performed
	OCSB10	BW	OTD0	0	RT0 output level: Low
			OTD1	0	RT1 output level: Low
			Reserved	NM	-
			CMOD	NM	Operation mode:
			Reserved	NM	
			FM4	NM	Operation mode
	ICSA10	BW	EG0[1:0]	00	ch.0 operation state: Operation prohibit
			EG1[1:0]	00	ch.1 operation state: Operation prohibit
			ICE0	NM	ch.0 interrupt:
			ICE1	NM	ch.1 interrupt:
			ICP0	1	ch.0 edge detection: Nothing is performed
			ICP1	1	ch.1 edge detection: Nothing is performed
	TCSA0	HW	CLK[3:0]	NM	Clock division prescaler setting:
			SCLR	1	Soft clear: FRT initialization
			MODE	NM	Count mode setting:
			STOP	1	FRT count operation: Counting is stopped
			BFE	NM	TCCP buffer function:
			ICRE	NM	Peak value detection interrupt:
			ICLR	1	Peak value detection: Nothing is performed
			Reserved	NM	-
			IRQZE	NM	Zero value detection interrupt
			IRQZF	1	Zero value detection: Nothing is performed
			ECKE	NM	Selection of clock used:

5.2 Multifunction Timer Control Example 2

Multifunction Timer Control Example 2 presents cases where the function blocks are operated in the modes shown below.

FRT:	Normal Up/Down-count mode, with zero detection interrupt
OCU:	Active high waveform output where change position is identical on the FRT up side and down side (Same as OCU Setting Example 6)
WFG:	RT-dead timer mode
ADCMP:	Conversion start command at match condition during Up-counting (Same as ADCMP Setting Example 2)

5.2.1 Timechart

The main registers for the MFT blocks and input/output signal timecharts are shown in Figure 5-2.

Figure 5-2 Timechart of Main Registers and Input/Output Signals for Each Block

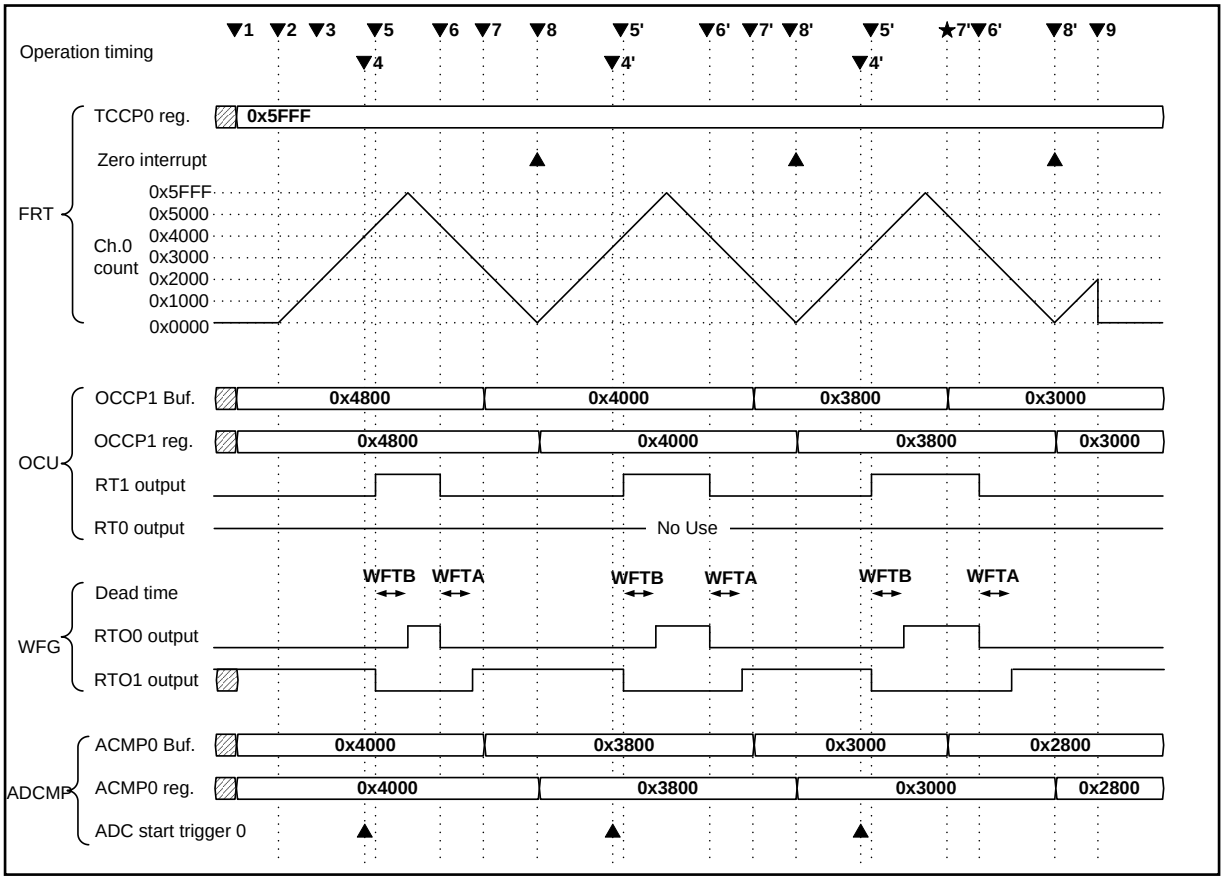


Figure 5-2 shows the operation timing, FRT operation, OCU operation, WFG operation, and ADCMP operation from top to bottom. The cases shown in Operation timing 1 to 9 describe what is controlled by the CPU and the operation of each function block. Specific examples of CPU register settings are shown for each timing. For details of the register settings, see 3 Registers of the Multifunction Timer. In addition to the above, it should also be noted that the LSI I/O port block, interrupt control block, and ADC must be set separately.

5.2.2 FRT, OCU, and ADCMP Settings and Operation

- Operation timing 1

The FRT-ch.0 initial settings (normal up/down-count mode) are set (TCSA0 register write).

The FRT-ch.0 peak value (count cycle) is set (TCCP0 register write). In this example, "0x5FFF" is set. The FRT count cycle is 4.915 ms when the prescaler is set to 1/4 and PCLK is set to 40MHz.

The OCU-ch.1 initial settings are set. Operation is set in OCU Setting Example 6 in “4.2 Description of OCU Operation” (Active high waveform output where the OCU RT1 change position is identical on the FRT up side and down side). Also, the initial output level of the OCU-ch.1 output signal (RT1) is specified (Register writes for OCFS10, OCSA10, OCSB10, OCSD10 and OCSE1).

The initial value is set for the time at which the OCU-ch.1 output signal (RT1) (OCCP1 register write) is changed. In this example, 0x4800 is set. The written value is written to the buffer register and then transferred to the OCCP1 register.

The ADCMP-ch.0 initial settings are set. Operation is set in ADCMP Setting Example 2 in “4.6 Description of ADCMP Operation”. (ADC conversion start command by match detection during FRT count-up) (ACFS10, ACSC0 register write).

The initial value is set for the time for starting ADCMP-ch.0 (ACMP0 register write). In this example, "0x4000" is set. The written value is written to the buffer register and then transferred to the ACMP0 register.

- Operation timing 2

A command is issued to FRT-ch.0 to start the count operation (TCSA0 register write).

As shown in Figure 5-2, FRT-ch.0 starts counting from 0x0000 and continues the up-count operation until the TCCP value (=0x5FFF) is reached. Then, the count direction is switched, and the down-count operation is performed until 0x0000 is reached. After that, this count operation continues.

- Operation timing 3

An operation allow command is issued to OCU-ch.1 (OCSA10 register write).

An operation allow command is issued to ADCMP-ch.0 (ACSD0 register write).

- Operation timing 4

When ADCMP -ch.0 detects that the FRT counter value has reached 0x4000 during the count-up and matches the ACMP0 setting value, the ADC start signal is output.

- Operation timing 5

When OCU-ch.1 detects that the FRT counter value has reached 0x4800 during the count-up and matches the OCCP1 setting value, the output signal (RT1) changes from the Low level to the High level.

- Operation timing 6

When OCU-ch.1 detects that the FRT counter value has reached 0x4800 during the count-down and matches the OCCP1 setting value, the output signal (RT1) changes from the High level to the Low level.

- Operation timing 7

The CPU sets the time at which the output signal (RT1) for OCU-ch.1 is changed in the next FRT cycle and sets the time for starting ADCMP-ch.0 (OCCP1 and ACMP0 register write). Because the OCCP1 and ACMP0 buffer functions are enabled and the zero value detection transfer mode is selected, the written value is first stored in the buffer register. Then, when the FRT counter value reaches the Zero value (Operation timing 8), the buffer register value is transferred to the OCCP1 and ACMP0 registers and is applied to the OCU output and ADC start signal output. For this reason, even if writing is performed before Operation timing 5 as shown in the timing for ★ in the figure, it does not affect the time for changing the output signal (RT1).

- Operation timing 8

When the count value reaches 0x0000 from 0x0001 in the count operation, FRT-ch.0 generates a Zero value interrupt to the CPU (An interrupt is not generated at Operation timing 2 immediately after FRT is started up).

The CPU determines that an interrupt has been generated from FRT-ch.0 because 1 has been set to the Zero value detection register of FRT-ch.0 (TCSA0 register read). The CPU clears the Zero value detection register and returns from the interrupt (TCSA0 register write).

- Operation timing 4' to 8'

After this, as shown in the figure, the operations in 4 to 8 are repeated so that an active high waveform output is obtained where the OCU RT1 change position is identical on the FRT up side and down side.

5.2.3 WFG Settings and Operation

- Operation timing 1

The RT-dead timer mode initial settings for WFG-ch.10 are set (WFSA10 register write). When this mode is set for WFG, the WFG output signal (RTO0) is output at the same level as the OCU-ch.1 output signal (RT1), but the WFG output signal (RTO1) is output at the opposite level.

The dead time is set to WFG-ch.10 (WFTA and WFTB register write). In this example, "0x0010" is set, and the inserted dead time is 0.8μs when the WFG prescaler is set to 1/2 and PCLK is set to 40MHz.

- Operation timing 4

When the RT1 signal changes from the Low level to the High level, the RTO1 signal changes from the High level to the Low level. After the dead time specified by the WFTB register, the RTO0 signal changes from the Low level to the High level.

- Operation timing 5

When the RT1 signal changes from the High level to the Low level, the RTO0 signal changes from the High level to the Low level. After the dead time specified by the WFTA register, the RTO1 signal changes from the Low level to the High level.

5.2.4 Completion of Process

- Operation timing 9

The process in Operation timing 9 shows the procedure for completing output of the PWM signal.

Operation of OCU-ch.1 is prohibited, and the OCU-ch.1 output signal (RT1) level is set (OCSA10, OCSB10 register write).

Operation of ADCMP-ch.0 is prohibited (ACSD0 register write).

When the output of OCU stops, WFG does not allow changing of the output signal.

A count operation stop instruction is issued to FRT-ch.0 (TCSA0 register write).

The example above describes operation with one channel of OCU, one channel of WFG, and one channel of ADCMP. However, if OCU-3ch, WFG-3ch, and ADCMP-3ch are connected to the same FRT to perform linked control, three-phase motor control can be achieved.

5.2.5 Details of Register Setting Values

Details of the register setting values for Multifunction Timer Control Example 2 are shown in

Table 5-5 to Table 5-8.

The meanings of the abbreviations used in the AC fields and Value fields for each table are identical to those for Control Example 1.

Table 5-5 Control Example 2 Register Settings 1

Timing	Register	AC	Bit Field	Value	Setting Description
1	TCSA0	HW	CLK[3:0]	0010	Clock division prescaler setting: 1/4
			SCLR	0	Soft clear: Nothing is performed
			MODE	1	Count mode: Up/down count mode
			STOP	1	FRT count operation: Counting is stopped
			BFE	1	TCCP buffer function: Enable
			ICRE	0	Peak value detection interrupt: Prohibit
			ICLR	0	Peak value detection: Clear
			Reserved	000	-
			IRQZE	1	Zero value detection interrupt: Enable
			IRQZF	0	Zero value detection: Clear
			ECKE	0	Selection of clock used: Internal clock
	TCCP0	HW	TCCP	0x5FFF	Sets FRT cycle.
	OCFS10	BW	FSO0[3:0]	Other	FRT connected to ch.0:
			FSO1[3:0]	0000	FRT connected to ch.1: FRT ch.0
	OCSA10	BW	CST0	Other	ch.0 operation state:
			CST1	0	ch.1 operation state: Operation prohibit
			Reserved	00	
			IOE0	Other	ch.0 interrupt:
			IOE1	0	ch.1 interrupt: Prohibit
			IOP0	Other	ch.0 match detection:
			IOP1	0	ch.1 match detection: Clear
	OCSB10	BW	OTD0	Other	RT0 output level:
			OTD1	0	RT1 output level: Low
			Reserved	00	-
			CMOD	0	Operation mode: Specifies FM4 mode
			Reserved	00	-
			FM4	1	Operation mode: Specifies FM4 mode-
	OCSD10	HW	OCCP0BUFE[1:0]	Other	ch.0 OCCP buffer function
			OCCP1BUFE[1:0]	01	ch.1 OCCP buffer function: Enable, zero transfer
			OCSE0BUFE[1:0]	Other	ch.0 OCSE buffer transfer:
			OCSE1BUFE[1:0]	00	ch.1 OCSE buffer transfer: Disable
			OPBM0	Other	ch.0 OCCP buffer interrupt mask link transfer:
			OPBM1	0	ch.1 OCCP buffer interrupt mask link transfer: Off
			OEBM0	Other	ch.0 OCSE buffer interrupt mask link transfer:
			OEBM1	0	ch.1 OCSE buffer interrupt mask link transfer: Off
			OFEX0	Other	ch.0 matched condition extension:
			OFEX1	0	ch.0 matched condition extension:Off
			Reserved	00	-
	OCSE1	WW	OCSE1[31:0]	0x8520852D	Specifies ch.1 operation: See OCU Setting Example 5.
	OCCP1	HW	OCCP	0x4800	Specifies ch.1 change timing
	ACFS10	BW	FSA0[3:0]	0000	FRT connected to ch.0: FRT ch.0
			FSA0[3:0]	Other	FRT connected to ch.1:
	ACSC0	BW	BUFE[1:0]	01	ch.0 ACMP buffer function: Enable, zero transfer
			ADSEL[2:0]	000	ch.0 ADC selection: start trigger0
			APBM	0	ch.0 ACMP buffer interrupt mask link transfer: Off
			Reserved	00	
	ACMP0	HW	ACMP0[15:0]	0x4000	Specifies ch.0 start timing

Table 5-6 Control Example 2 Register Settings 2

Timing	Register	AC	Bit Field	Value	Setting Description
1	WFSA10	HW	DCK[2:0]	001	Clock division prescaler setting: 1/2
			TMD[2:0]	100	Operation mode: Selects RT-dead timer mode
			GTEN[1:0]	00	Gate signal generation: Setting disabled
			PSEL[1:0]	00	Connecting PPG : Setting disabled
			PGEN[1:0]	00	Applying PPG setting: Setting disabled
			DMOD[1:0]	00	Output polarity: Positive polarity
			Reserved	00	-
	WFTA10	HW	WFTA	0x0010	Sets the dead time value
	WFTB10	HW	WFTB	0x0010	Sets the dead time value
2	TCSA0	HW	CLK[3:0]	NM	Clock division prescaler setting:
			SCLR	NM	Soft clear:
			MODE	NM	Count mode setting:
			STOP	0	FRT count operation: Counting is started
			BFE	NM	TCCP buffer function:
			ICRE	NM	Peak value detection interrupt:
			ICLR	1(RMW)	Peak value detection: Nothing is performed
			Reserved	NM	-
			IRQZE	NM	Zero value detection interrupt
			IRQZF	1(RMW)	Zero value detection: Nothing is performed
			ECKE	NM	Selection of clock used:
3	OCSA10	BW	CST0	NM	ch.0 operation state:
			CST1	1	ch.1 operation state: Operation allowed
			BDIS0	NM	ch.0 OCCP buffer function:
			BDIS1	NM	ch.1 OCCP buffer function:
			IOE0	NM	ch.0 interrupt:
			IOE1	NM	ch.1 interrupt:
			IOP0	1	ch.0 match detection: Nothing is performed
			IOP1	1	ch.1 match detection: Nothing is performed
	ACSD0	BW	AMOD	0	ch.0 operation mode: Normal mode
			OCUS	0	OCCP selection at offset: Disable setting
			Reserved	0	
			DE	0	Start at ch.0 FRT=Down: Operation prohibited
			PE	0	Start at ch.0 FRT= Peak: Operation prohibited
			UE	1	Start at ch.0 FRT=Up: Operation allowed
			ZE	1	Start at ch.0 FRT=0x0000: Operation allowed
7	OCCP1	HW	OCCP1	0x4000	Specifies ch.1 change timing
	ACMP0	HW	ACMP0	0x3800	Specifies ch.0 start timing

Table 5-7 Control Example 2 Register Settings 3

Timing	Target Block	Register	AC	Bit Field	Value	Setting Description
8	FRT	TCSA0	HR	CLK[3:0]	DC	Clock division prescaler setting:
				SCLR	DC	Soft clear:
				MODE	DC	Count mode setting:
				STOP	DC	FRT count operation:
				BFE	DC	TCCP buffer function:
				ICRE	DC	Peak value detection interrupt:
				ICLR	DC	Peak value detection:
				Reserved	DC	-
				IRQZE	DC	Zero value detection interrupt
				IRQZF	1	Zero value detection: Zero value detection
				ECKE	DC	Selection of clock used:
		TCSA0	HW	CLK[3:0]	NM	Clock division prescaler setting:
				SCLR	NM	Soft clear:
				MODE	NM	Count mode setting:
				STOP	NM	FRT count operation:
				BFE	NM	TCCP buffer function:
				ICRE	NM	Peak value detection interrupt:
				ICLR	1(RMW)	Peak value detection: Nothing is performed
				Reserved	NM	-
				IRQZE	NM	Zero value detection interrupt
				IRQZF	0	Zero value detection: Flag cleared
				ECKE	NM	Selection of clock used:

Table 5-8 Control Example 2 Register Settings 4

Timing	Register	AC	Bit Field	Value	Setting Description
9	OCSA10	BW	CST0	NM	ch.0 operation state:
			CST1	0	ch.1 operation state: Prohibit
			Reserved	NM	
			IOE0	NM	ch.0 interrupt:
			IOE1	NM	ch.1 interrupt:
			IOP0	1	ch.0 match detection: Nothing is performed
			IOP1	1	ch.1 match detection: Nothing is performed
	OCSB10	BW	OTD0	NM	RT0 output level:
			OTD1	0	RT1 output level: Low
			Reserved	NM	-
			CMOD	NM	Operation mode:
			Reserved	NM	:
			FM4	NM	Operation mode
	ACSD0	BW	AMOD	NM	ch.0 operation mode:
			OCUS	NM	OCCP selection at offset:
			Reserved	NM	
			DE	0	Start at ch.0 FRT=Down: Prohibit
			PE	0	Start at ch.0 FRT=Peak: Prohibit
			UE	0	Start at ch.0 FRT=Up: Prohibit
			ZE	0	Start at ch.0 FRT=0x0000: Prohibit
	TCSA0	HW	CLK[3:0]	NM	Clock division prescaler setting:
			SCLR	1	Soft clear: FRT initialization
			MODE	NM	Count mode setting:
			STOP	1	FRT count operation: Counting is stopped
			BFE	NM	TCCP buffer function:
			ICRE	NM	Peak value detection interrupt:
			ICLR	1	Peak value detection: Nothing is performed
			Reserved	NM	-
			IRQZE	NM	Zero value detection interrupt
			IRQZF	1	Zero value detection: Nothing is performed
			ECKE	NM	Selection of clock used:

6. Detailed Timing of the Multifunction Timer Input/Output Signals

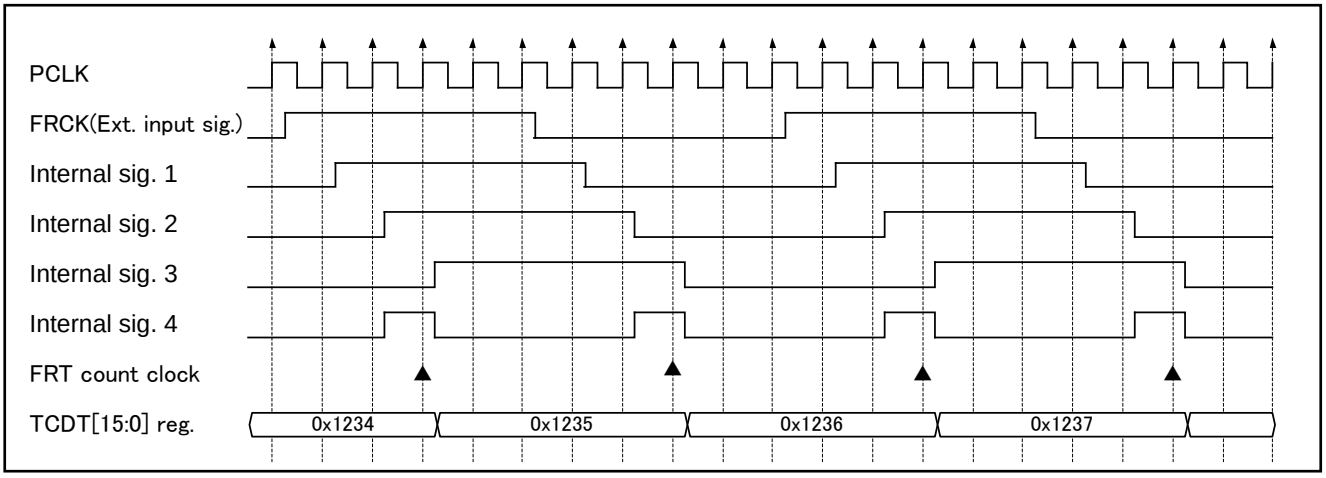
The detailed timing charts for the multifunction timer input/output signals are shown below.

6.1. FRT Operation Detailed Timing When Using External Input Clock
6.2. OCU and WFG Operation Detailed Timing
6.3. ADCMP Operation Detailed Timing
6.4. ICU Operation Detailed Timing
6.5. DTTIX Input Detailed Timing

6.1 FRT Operation Detailed Timing When Using External Input Clock

The timing chart for the FRT count operation when using an external input clock (FRCK) is shown in Figure 6-1.

Figure 6-1 FRT Operation Timing Chart (When Using External Input Clock)



6.2 OCU and WFG Operation Detailed Timing

The OCU and WFG operation timing charts are shown in Figure 6-2 and Figure 6-3. The IOP register, RTx output signal, and WFG RTOx output signal changes when a match is detected in OCU are shown.

Figure 6-2 is an example when through mode (WFSA.TMD=000) is selected by the WFG. The FRT performs count operation using the PCLK frequency-dividing clock. The figure is an example of four frequency divisions (TCSA.CLK[3:0]=0010).

The WFG RTOx signal is changed from the OCU RTx signal after one cycle by PCLK. The RTOx signal is an external output terminal for the microcontroller. Delays are generated based on the load capacity of the external output terminal.

Figure 6-2 OCU-WFG Operation Timing Chart (WFG Through Mode)

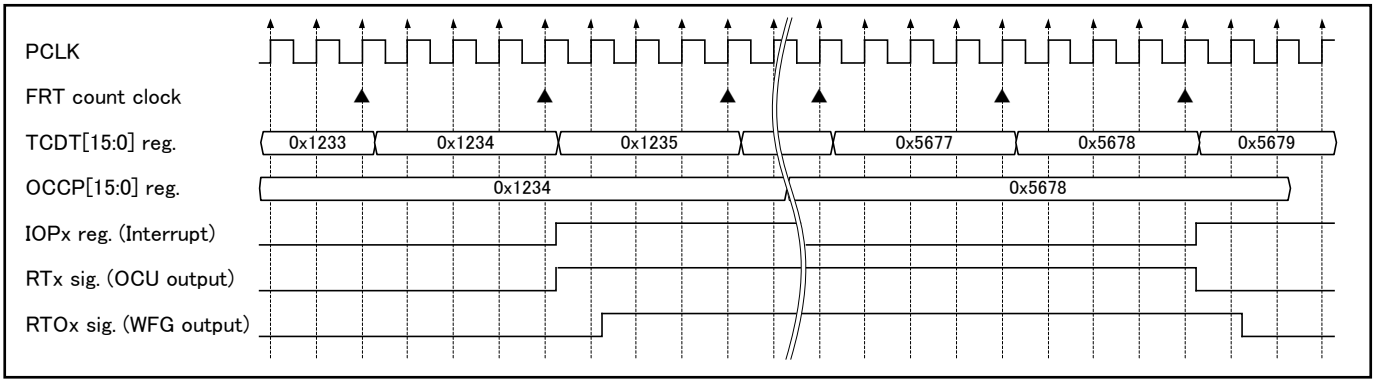
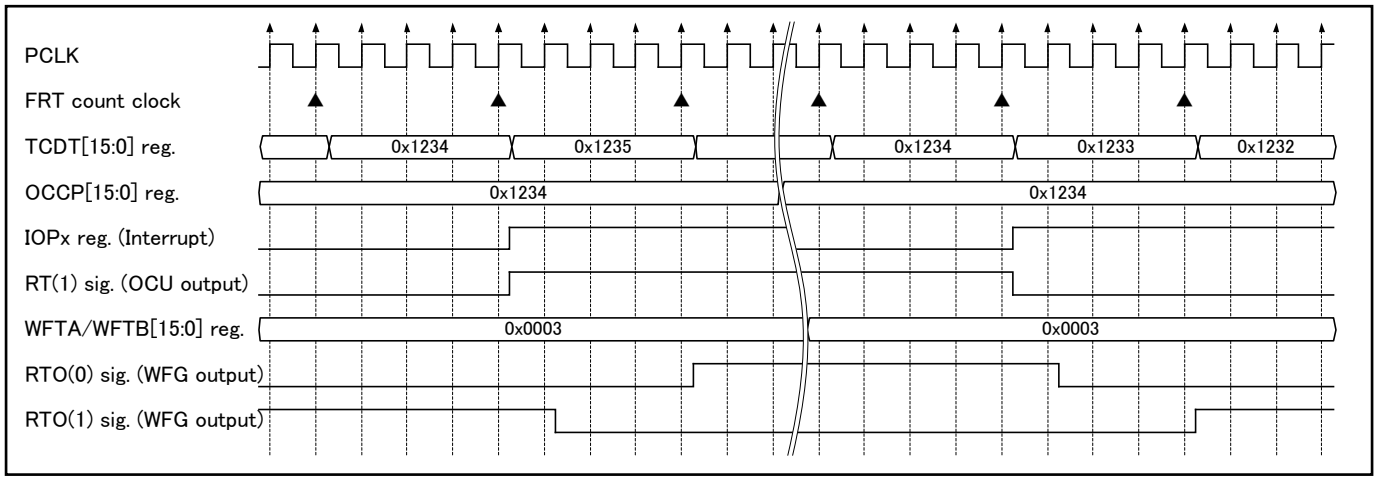


Figure 6-3 shows an example when RT dead timer mode (WFSA.TMD=100) is selected by the WFG. This shown an example where WFTA/WFTB=0x0003 and WFSA.DCK=000 are specified, and a dead time of 3*PCLK is inserted.

If the dead time is not inserted, the RTO(0) and RTO(1) of the WFG are changed from the OCU RT(1) signal after one cycle by PCLK. If a dead time is inserted, after one cycle by PCLK, the output is changed after the specified dead time.

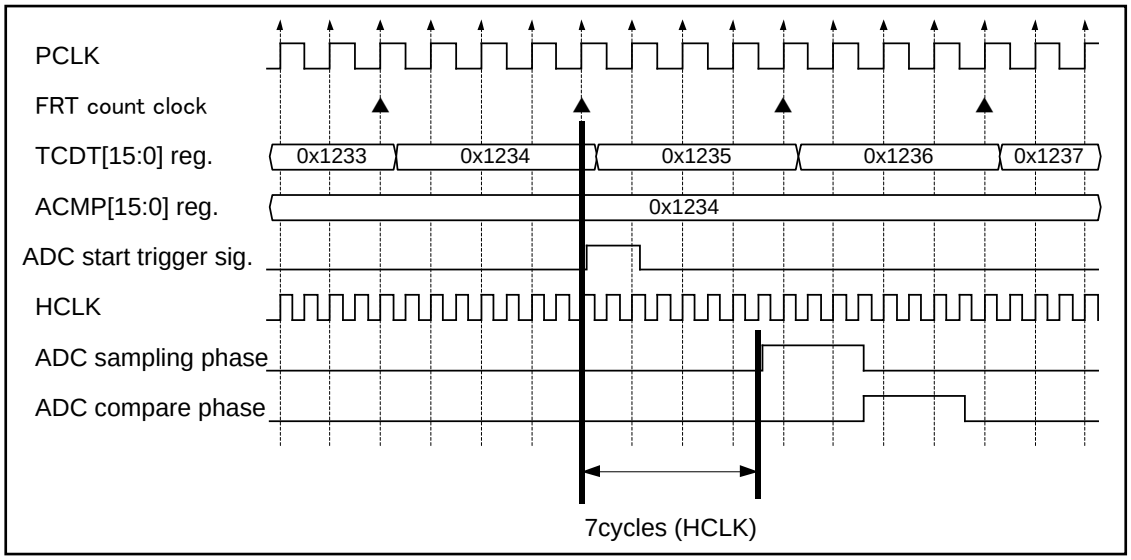
Figure 6-3 OCU-WFG Operation Timing Chart (WFG RT Dead Timer Mode)



6.3 ADCMP Operation Detailed Timing

The ADCMP operation timing chart is shown in Figure 6-4. The operation timing from FRT counter match detection to the beginning of ADC startup in ADCMP is shown. Time for a total of seven cycles in HCLK is required from FRT count clock match detection to ADC conversion start. The ADC sampling time and compare time are specified by making settings at the ADC side.

Figure 6-4 ADCMP Operation Timing Chart



6.4 ICU Operation Detailed Timing

The ICU operation timing charts are shown in Figure 6-5 and

Figure 6-6. These charts contain the operation where the FRT count value is captured by the ICCP register and the operation where the ICP register (interrupt flag) is set from the signal change of the external input terminal (ICx). The capture timing is determined by the change timing of the input signal only and is not affected by the FRT count clock.

Figure 6-5 ICU Operation Timing Chart (Input Signal Rising)

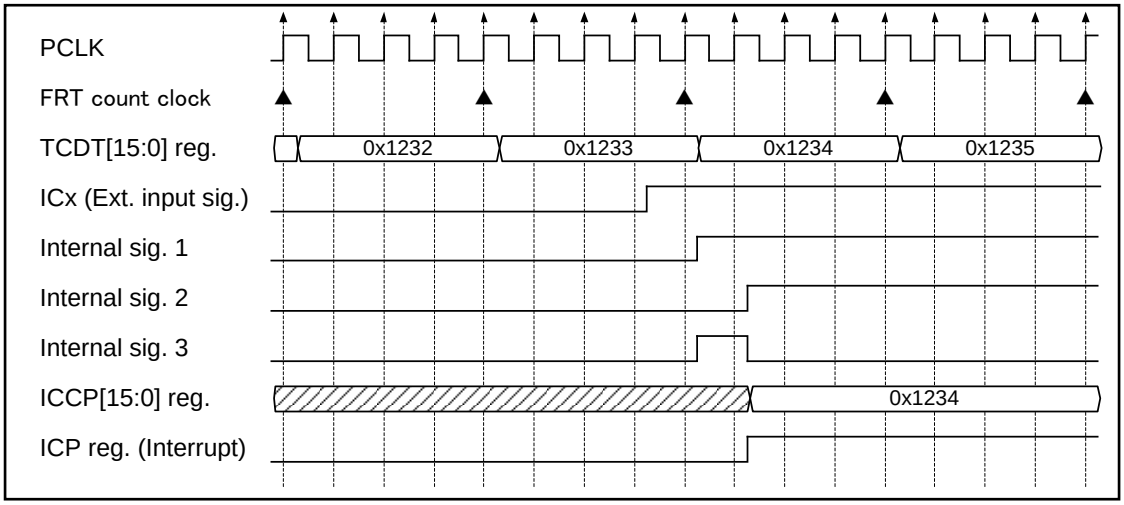
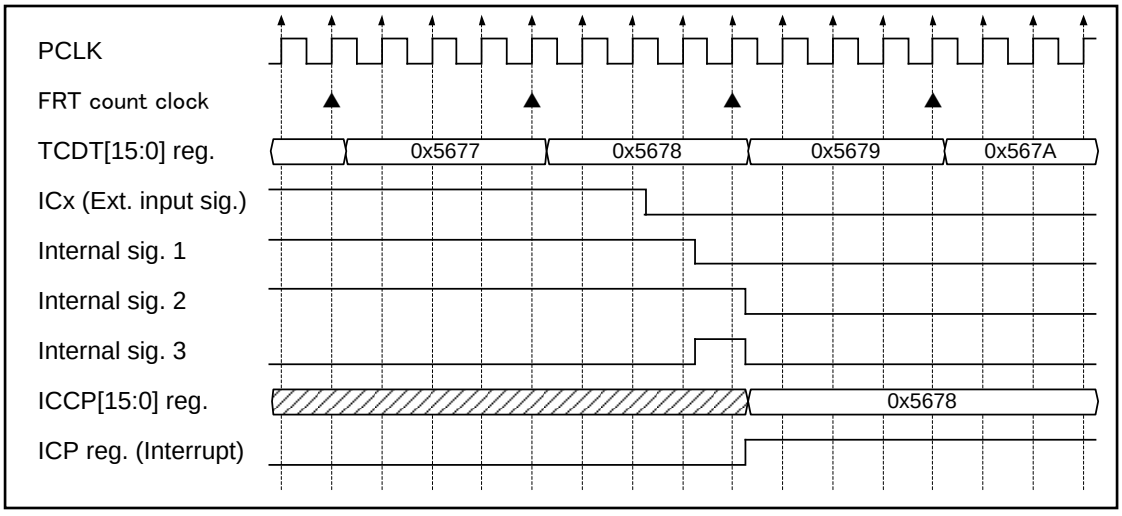


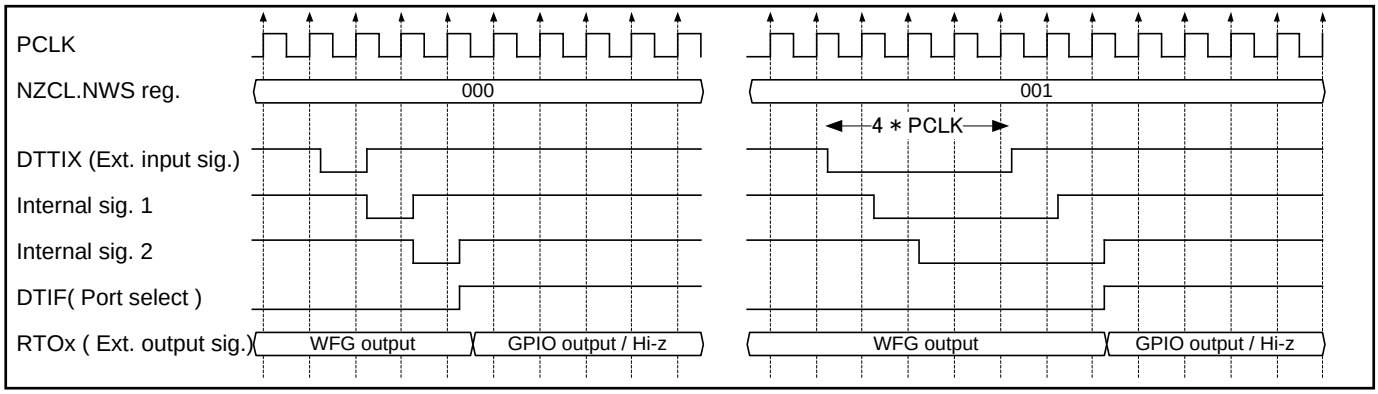
Figure 6-6 ICU Operation Timing Chart (Input Signal Falling)



6.5 DTTIX Input Detailed Timing

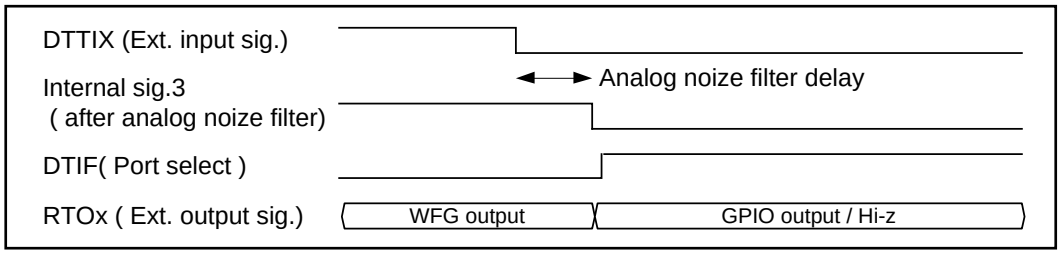
The timing chart from the DTTIX signal until the I/O port output is changed by passing through the digital noise filter is shown in Figure 6-7.

Figure 6-7 DTTIX-DTIF Timing Chart (Passing Through Digital Noise Filter)



The timing chart from the DTTIX signal until the I/O port output is changed by the DTIF interrupt by passing through an analog noise filter is shown in Figure 6-8.

Figure 6-8 DTTIX-DTIF Timing Chart (Passing Through Analog Noise Filter)



CHAPTER 7-1: PPG Configuration

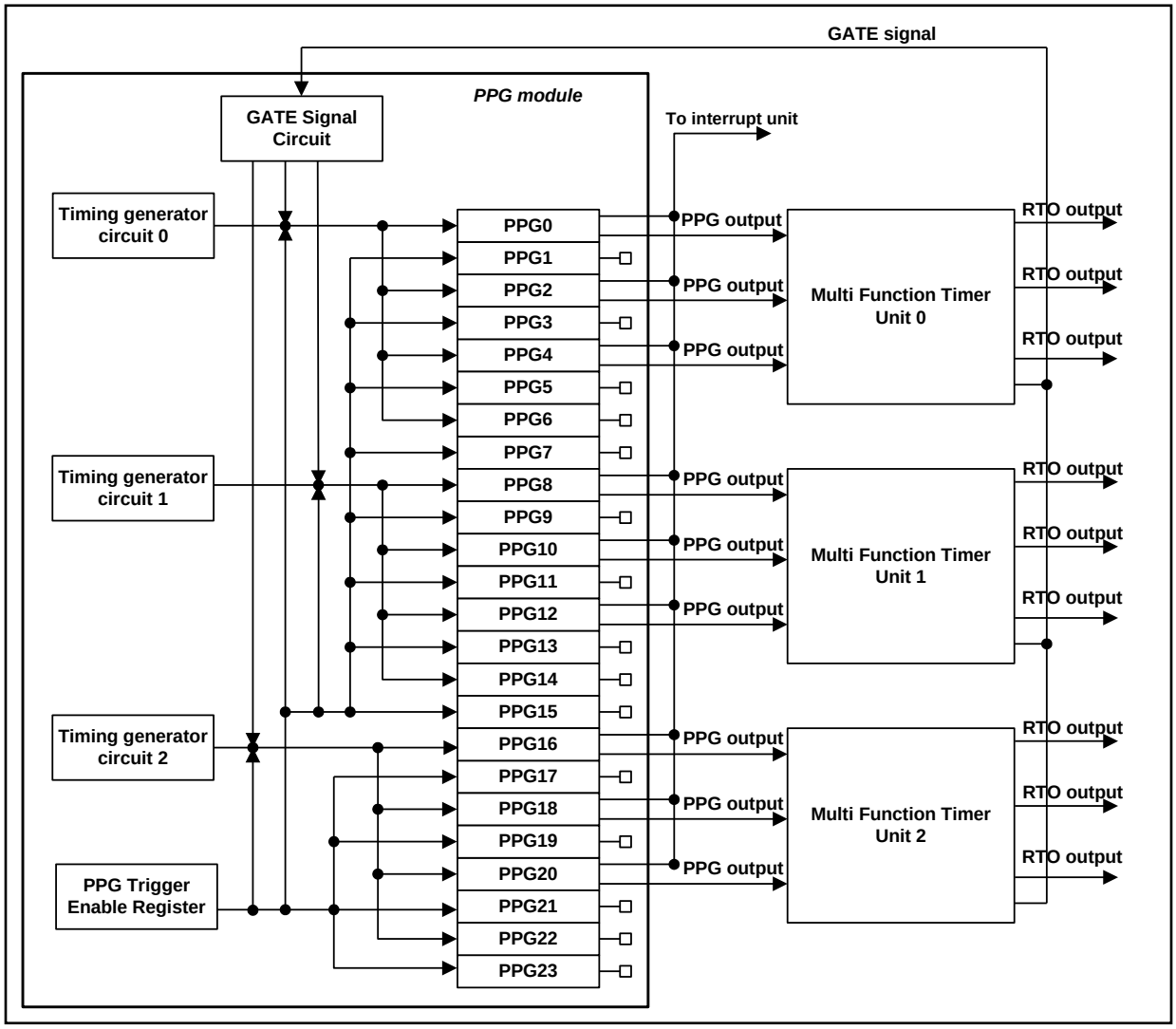
This chapter explains the PPG configuration.

1. Configuration

1. Configuration

This section explains the PPG configuration.

The following shows the PPG configuration.



Note:

- *The number of MFT, Timing generators, and PPG varies with the products. For details, see the Data Sheet of the product you are using.*

PPG Connection

- PPG output is transferred from the output RTO pin of the multifunction timer via the multifunction timer module.
- PPG output and PPG interrupt are connected only to the PPG0, PPG2, PPG4, PPG8, PPG10, PPG12, PPG16, PPG18 and PPG20. Therefore, no output is obtained from other PPG channels.
- A PPG start factor can be set to a PPG channel with no output connected, but no output is obtained from such a PPG channel.
- Furthermore, any PPG operation mode (8-bit, 8+8-bit, 16-bit, or 16+16-bit mode) can be selected, but no output is obtained from a PPG channel with no output connected.

Differences between Timing Generators 0, 1 and 2

- Timing generator 0
  - Compare Register: COMP0/COMP2/COMP4/COMP6
  - PPG channel to be triggered: ch.0/ch.2/ch.4/ch.6
- Timing generator 1
  - Compare Register: COMP1/COMP3/COMP5/COMP7
  - PPG channel to be triggered: ch.8/ch.10/ch.12/ch.14
- Timing generator 2
  - Compare Register: COMP8/COMP10/COMP12/COMP14
  - PPG channel to be triggered: ch.16/ch.18/ch.20/ch.22

Setting the EDGE bit in the PPG GATE Function Control Register

The EDGE bit in the PPG GATE Function Control Register can be set only to EDGE=0.

Note:

- *Started only at the rising edge of the GATE signal.*

Combinations of Operation Modes and PPG Channels with Output Enabled

PPG Channel	8-bit Mode	8+8-bit Mode	16-bit Mode	16+16-bit Mode
PPG ch.0	PPG0 output	PPG0 output	PPG0 output	PPG0 output
PPG ch.1	Not available	PPG0 prescaler		
PPG ch.2	PPG2 output	PPG2 output	PPG2 output	PPG0 prescaler
PPG ch.3	Not available	PPG2 prescaler		
PPG ch.4	PPG4 output	PPG4 output	PPG4 output	PPG4 output
PPG ch.5	Not available	PPG4 prescaler		
PPG ch.6	Not available	Not available	Not available	PPG4 prescaler
PPG ch.7	Not available	Not available		
PPG ch.8	PPG8 output	PPG8 output	PPG8 output	PPG8 output
PPG ch.9	Not available	PPG8 prescaler		
PPG ch.10	PPG10 output	PPG10 output	PPG10 output	PPG8 prescaler
PPG ch.11	Not available	PPG10 prescaler		
PPG ch.12	PPG12 output	PPG12 output	PPG12 output	PPG12 output
PPG ch.13	Not available	PPG12 prescaler		
PPG ch.14	Not available	Not available	Not available	PPG12 prescaler
PPG ch.15	Not available	Not available		
PPG ch.16	PPG16 output	PPG16 output	PPG16 output	PPG16 output
PPG ch.17	Not available	PPG16 prescaler		
PPG ch.18	PPG18 output	PPG18 output	PPG18 output	PPG16 prescaler
PPG ch.19	Not available	PPG18 prescaler		
PPG ch.20	PPG20 output	PPG20 output	PPG20 output	PPG20 output
PPG ch.21	Not available	PPG20 prescaler		
PPG ch.22	Not available	Not available	Not available	PPG20 prescaler
PPG ch.23	Not available	Not available		

CHAPTER 7-2: PPG

This chapter explains the PPG function.

1. Overview
2. Configuration and Block Diagrams of the PPG
3. Operations of the PPG
4. PPG Setup Procedure
5. PPG Registers
6. Notes on using PPG

1. Overview

This section gives an overview of the PPG function.

The Programmable Pulse Generator (PPG) module can perform pulse output of arbitrary cycle and duty ratio controlled by timer operation.

Features of the PPG Module

- 8-bit PPG operation mode is supported.
- 16-bit PPG operation mode is supported.
- 8+8-bit PPG operation mode is supported.
- 16+16-bit PPG operation mode is supported.
- The output level for the PPG can be inverted, including the initial output level during PPG stop.
- An arbitrary PPG cycle can be selected by selecting the PPG count clock.
- The PPG can output a pulse wave with an arbitrary duty ratio by making the register setting. This module can also be used in conjunction with an external circuit to form a D/A converter.
- If interrupt enable is set, an interrupt can be generated when the PPG output is changed (when the count for reload value ends, and an underflow occurs).

PPG Start Trigger Method

PPG start trigger can be selected from following three methods.

- Start triggered by PPG start trigger register writing
- Start triggered by the Timing Generator Circuit
- Start triggered by GATE signal from the multifunction timer

* Besides the above start methods, start by the IGBT mode can also be selected. For details, see the chapter on PPG IGBT mode.

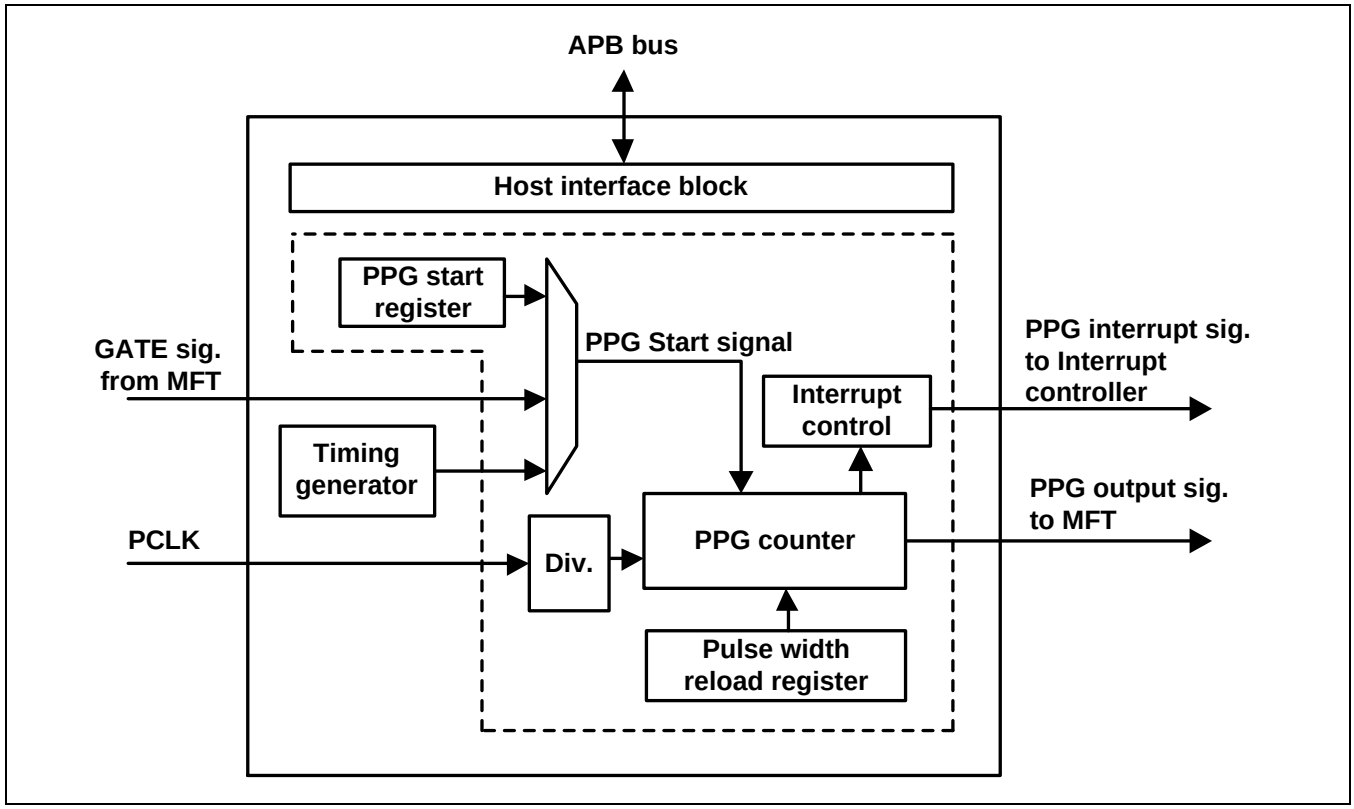
2. Configuration and Block Diagrams of the PPG

This section shows the block diagrams of PPG.

2.1 PPG Circuit Block Diagram

Figure 2-1 shows the block diagram of the PPG.

Figure 2-1 PPG Block Diagram



The PPG module consists of the following functional blocks.

Host Interface Block

This performs function control of each PPG block based on instructions from the CPU.

PPG Start Register

This register directly generates PPG start signals by register writing from the CPU.

Timing Generator

This is a circuit for starting multiple PPGs individually at the specified timing. PPG start signals are generated separately for multiple PPGs at the timing that was set by the internal compare registers. Internal configuration block diagrams are shown in Figure 3-14, Figure 3-15, and Figure 3-16.

PPG Start Signal Selector

The PPG start signal is selected by specifying the control register value. PPG start from PPG start register, PPG start from timing generator, or PPG start by GATE signal from multifunction timer (MFT) can be selected.

PCLK Divider

The PPG operates using the peripheral clock signal (PCLK) as a reference clock. The count clock used by the PPG counter is generated by the PCLK frequency divider. The pulse width of the output signal from PPG is specified based on the PCLK cycle.

PPG Counter and Pulse Width Reload Register

The Low pulse width and High pulse width of the PPG output signal is specified in the reload register from the CPU. The PPG counter performs a count operation of the specified pulse width and changes the PPG output signal.

Interrupt Control Circuit

The PPG interrupt signal is generated and output when the PPG output signal is changed.

In Figure 2-1, the section enclosed by the dashed lines indicates that multiple PPG channels are installed. Also, the connection topology of the PPG channel and the number of available channels change based on the selected PPG operation mode. The channel connection diagrams for each operation mode are shown in Figure 3-1, Figure 3-3, Figure 3-4, and Figure 3-5.

Among the PPG output signals obtained by PPG timer operation, some channel outputs can be output to external terminals by passing through a multifunction timer. Also, some PPG interrupt outputs are connected to interrupt controllers for enabling execution of interrupt processes.

For details on the PPG output terminal that is output to external terminals by passing through a multifunction timer and on PPG interrupts connected to an interrupt controller, see the chapter PPG configuration.

3. Operations of the PPG

This section shows the operation of PPG.

3.1. PPG Circuit Operations
3.2. Timing Generator Circuit Operations

3.1 PPG Circuit Operations

The PPG module can output pulse signals having arbitrary cycle and duty ratio.
The pulse output can be controlled based on the timer operation.

3.1.1 PPG Operations

This explains operation of the PPG timer circuit. The configuration in 8-bit PPG operation mode is shown in Figure 3-1. The input/output signal waveform is shown in Figure 3-12.

Figure 3-1 Configuration in 8-bit PPG Mode

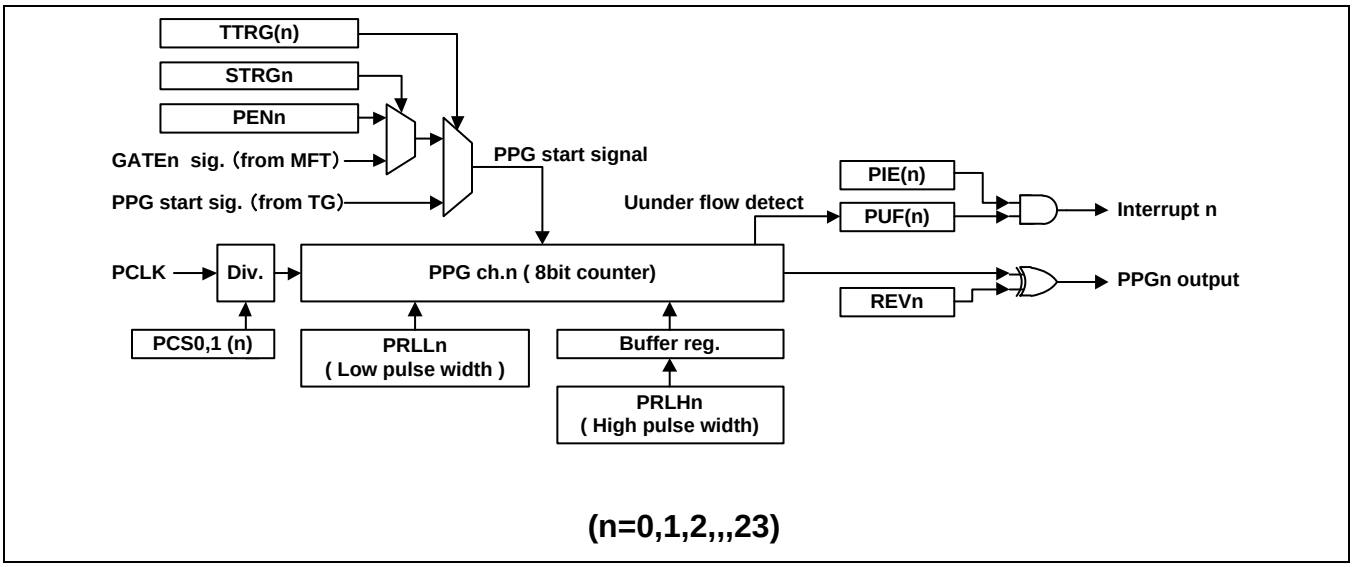
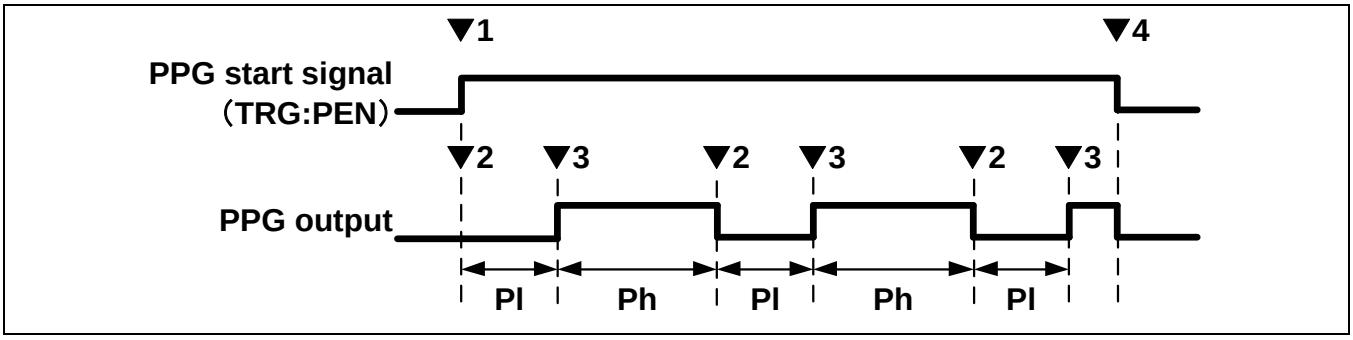


Figure 3-2 PPG Input/output Signal Waveform



The ▼1 to ▼4 in the text below indicate the timing shown in Figure 3-2. This section explains operation when the start method by writing the PPG start register (TRG:PEN) is specified and the positive polarity (REVC:REV=0) is specified.

The initial level of PPG output is Low. The PPG starts operation by asserting the start signal. At the timing in ▼1, "1" is written to the PPG start register (TRG:PEN) from the CPU, and the PPG start signal is asserted. During the period that the PPG start signal is asserted, the PPG timer circuit continues to repeat the operations of ▼2 and ▼3 below.

At the timing of ▼2, the PPG output is set to the Low level. Also, the Low width value is loaded to the PPG counter from the Low width setting reload register (PRLL), and the countdown is started. A wait is performed until the time specified in the Low width has elapsed.

At the timing of ▼3, the PPG output is set to the High level. Also, the High width value is loaded to the PPG counter from the High width setting reload register (PRLH), and the countdown is started. A wait is performed until the time specified in the High width has elapsed.

This operation generates output waveforms having the specified Low width and High width. In Figure 3-2, the Low width (Pl) and High width (Ph) of the output pulse can be specified as shown below.

T (count clock cycle) = Count clock cycle selected by the PPGC: PCS1 and PCS0 registers
Pl (PPG output Low width) = T x (PRLL register value + 1)
Ph (PPG output High width) = T x (PRLH register value + 1)

At the timing in ▼4, "0" is written to the PPG start register (TRG:PEN) from the CPU, and the start signal is negated. The PPG timer circuit stops the count operation. Even if the count operation is in progress, output is set to the Low level.

3.1.2 PPG Operation Modes

The PPG has an 8-bit length counter for each channel. Multiple PPG channels can be connected to enable generation of output pulses with longer count lengths. The PPG operation modes below can be used.

8-bit PPG Operation Mode

Figure 3-1 shows the channel connection diagram for this operation mode. In this mode, operation is performed as an 8-bit length counter PPG independently for each channel. The output pulse width can be specified as an 8-bit length value.

16-bit PPG Operation Mode

Figure 3-13 shows the channel connection diagram for this operation mode. In this mode, two channels are connected to perform operation as a 16-bit length counter PPG. The output pulse width can be specified as a 16-bit length value.

8+8-bit PPG Operation Mode

Figure 3-14 shows the channel connection diagram for this operation mode. Two channels are used. One of the PPGs operates as a prescaler. (This is referred to as the "prescaler side" below) The other PPG operates using the prescaler side output as an operation clock. (This is referred to as the "PPG output side" below.) In this mode, operation is performed by specifying the output pulse width as an 8-bit length value separately for the prescaler side and PPG output side. The counter on the PPG output side performs the count operation at both the rising and falling edges of the prescaler side output signal.

16+16-bit PPG Operation Mode

Figure 3-15 shows the channel connection diagram for this operation mode. Four channels are used. Two channels are connected respectively to perform operation as a 16-bit length counter. One PPG operates as the prescaler side. The other PPG operates as the PPG output side using the prescaler side output as an operation clock. In this mode, operation is performed by specifying the output pulse width as a 16-bit length value separately for the prescaler side and PPG output side. The counter on the PPG output side performs the count operation at both the rising and falling edges of the prescaler side output signal.

Figure 3-3 Configuration in 16-bit PPG Mode

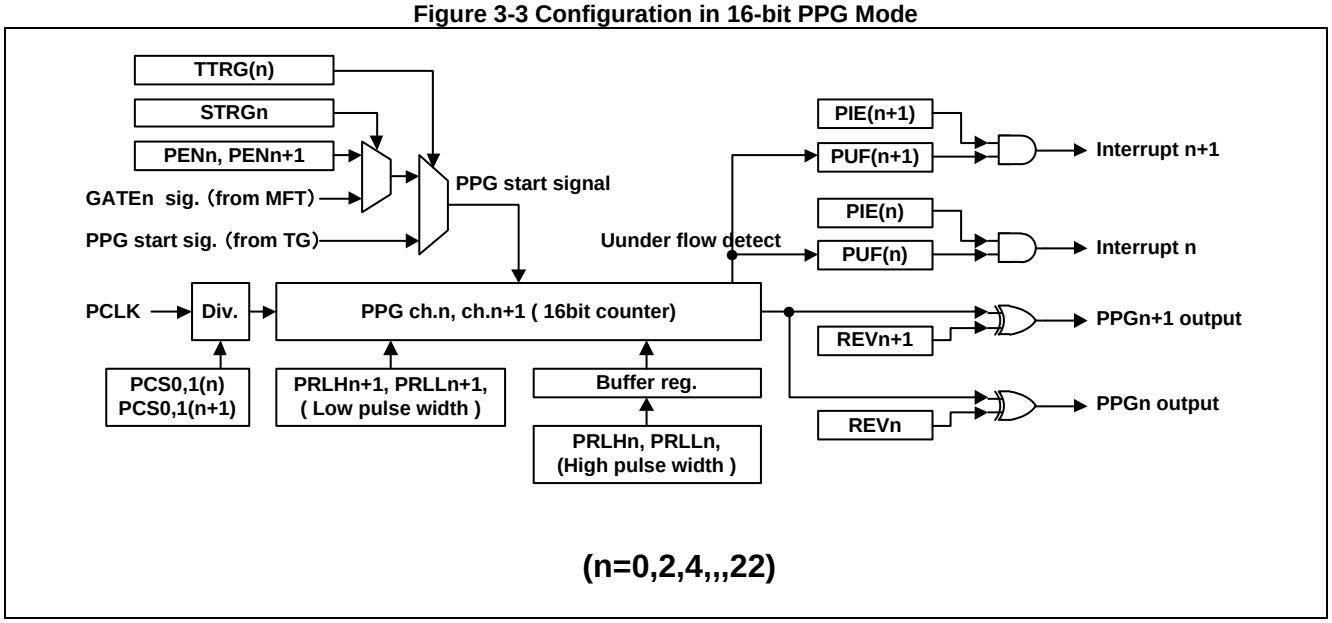


Figure 3-4 Configuration in 8+8-bit PPG Mode

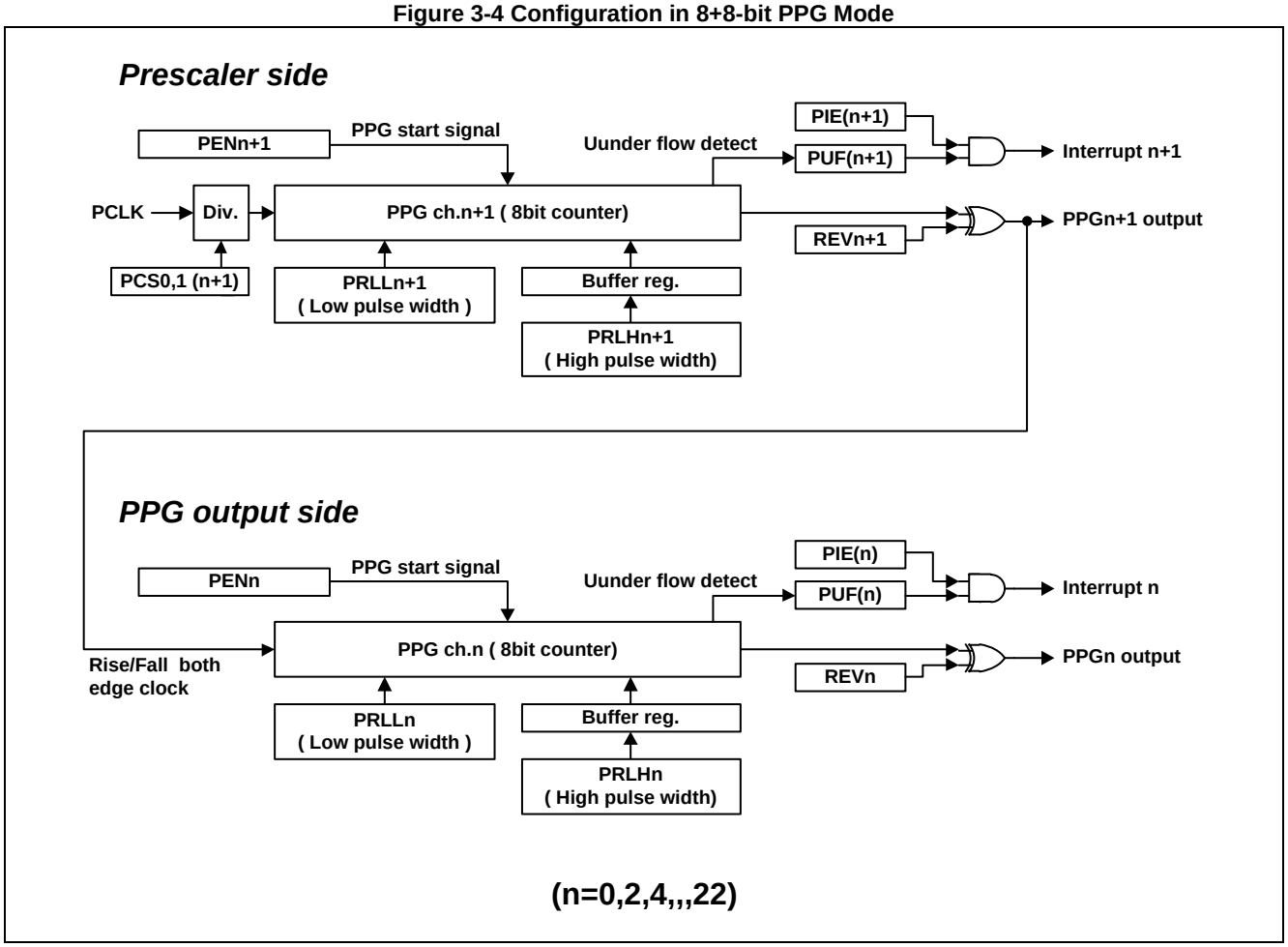
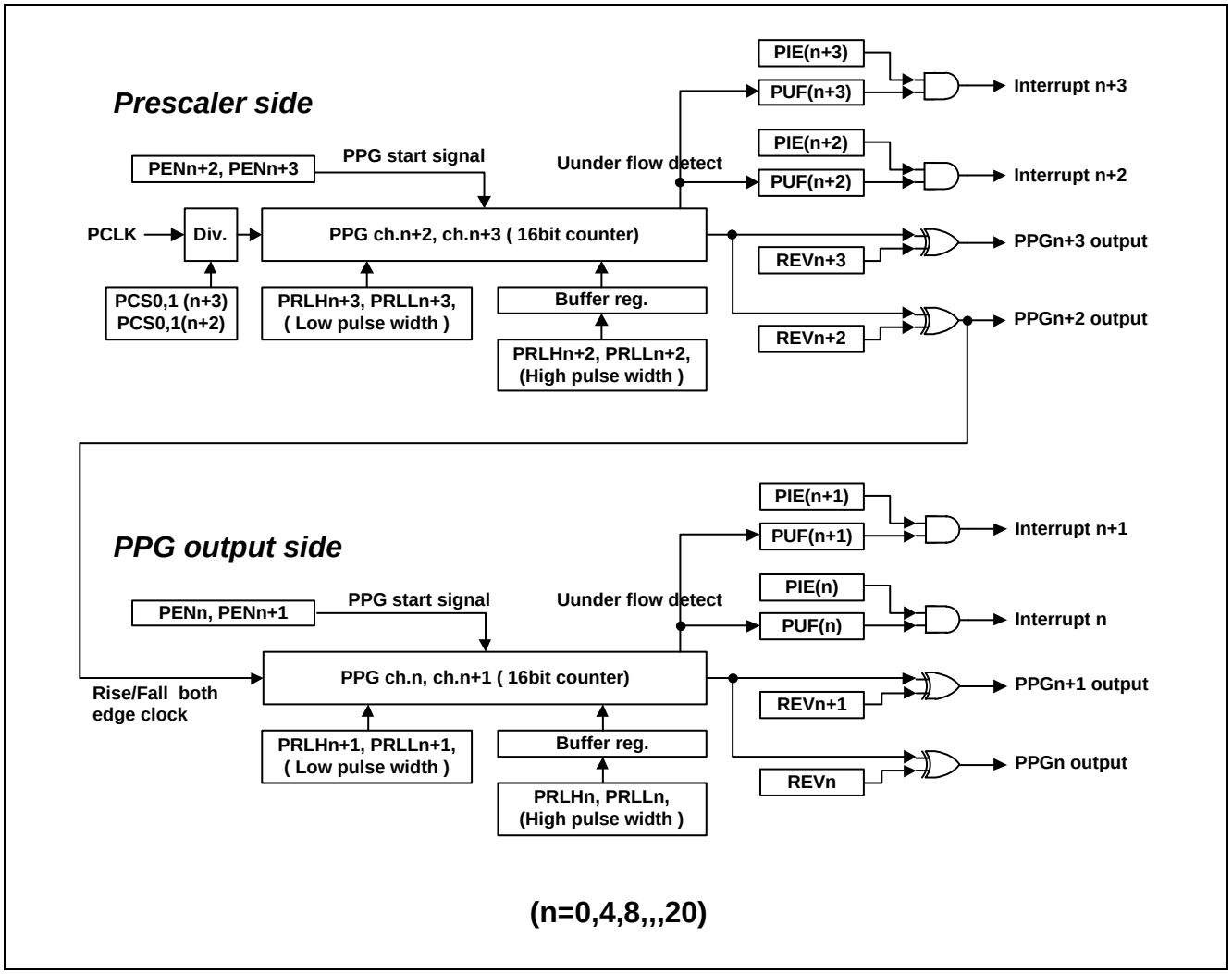


Figure 3-5 Configuration in 16+16-bit PPG Mode



3.1.3 Selecting the PPG Operation Mode

The PPGC:MD[1:0] register setting can be used to select the operation mode for each PPG channel. The operation mode for each channel (channel connection, used as prescaler side, used as PPG output side) is uniquely determined by this register setting.

The PPGCn:MD[1:0] register exists only for registers where n is even. The operation mode for both channel n (even numbers) and channel n+1 (odd numbers) is determined by specifying the PPGCn:MD[1:0] register. For 16+16-bit PPG mode, both the PPGCn:MD[1:0] register and PPGCn+2:MD[1:0] register are set to "11".

Table 3-1 shows a list of PPG operation modes which are selected based on the PPGCn:MD[1:0] register value and PPGCn+2:MD[1:0] register value.

The index n indicating the register number and channel number in Table 3-1 stands for n=0, 4, 8, 12, 16, and 20. The same combination can be specified for ch.0 to ch.3, ch.4 to ch.7, ch.8 to ch.11, ch.12 to ch.15, ch.16 to ch.19, and ch.20 to ch.23.

The operation mode is selected before starting the PPG. During PPG operation, the operation mode cannot be changed.

Table 3-1 Selecting PPG Operation Mode

Register Setting				Selected Operation Mode			
PPGCn		PPGCn+2		Ch.n+0	Ch.n+1	Ch.n+2	Ch.n+3
MD1	MD0	MD1	MD0				
0	0	0	0	8 PPG : ☆ ◎	8 PPG : ★ ◎	8 PPG : ☆ ◎	8 PPG : ★ ◎
0	0	0	1	8 PPG : ☆ ◎	8 PPG : ★ ◎	8+8 out : ★ ● ←	8+8 pre: ★ ◎
0	0	1	0	8 PPG : ☆ ◎	8 PPG : ★ ◎	16 PPG : ☆○	
0	0	1	1	Setting is prohibited.			
0	1	0	0	8+8 out: ★ ● ←	8+8 pre: ★◎	8 PPG : ☆◎	8 PPG : ★ ◎
0	1	0	1	8+8 out: ★ ● ←	8+8 pre: ★◎	8+8 out : ★ ● ←	8+8 pre: ★ ◎
0	1	1	0	8+8 out: ★ ● ←	8+8 pre: ★◎	16 PPG : ☆○	
0	1	1	1	Setting is prohibited.			
1	0	0	0	16 PPG : ☆ ○		8 PPG : ☆ ◎	8 PPG : ★ ◎
1	0	0	1	16 PPG : ☆ ○		8+8 out : ★ ● ←	8+8 pre: ★ ◎
1	0	1	0	16 PPG : ☆ ○		16 PPG : ☆ ○	
1	0	1	1	Setting is prohibited.			
1	1	0	0				
1	1	0	1				
1	1	1	0				
1	1	1	1	16+16 out: ★ ● ←		16+16 pre: ★ ○	

Details of Table 3-1 are described below.

8 PPG : Indicates that 8-bit PPG operation mode is selected.

16 PPG : Indicates that 16-bit PPG operation mode is selected.
Two channels are connected, and 16-bit length counter operation is performed.

8+8 pre : Indicates that 8+8-bit PPG operation mode is selected.
Indicates that prescaler side operation is performed.
Arrows in the table indicate the output direction of the prescaler clock.

8+8 out : Indicates that 8+8-bit PPG operation mode is selected.
Indicates that PPG output side operation is performed.

16+16 pre : Indicates that 16+16-bit PPG operation mode is selected.
Two channels are connected, and 16-bit length counter operation is performed.
Indicates that prescaler side operation is performed.
Arrows in the table indicate the output direction of the prescaler clock.

16 + 16 out : Indicates that 16+16-bit PPG operation mode is selected.
Two channels are connected, and 16-bit length counter operation is performed.
Indicates that PPG output side operation is performed.

☆ mark, ★ mark : Indicates the available start methods. This is described in the section on selecting the PPG start method.

◎ mark, ○ mark, ● mark : Indicates the available count clocks. This is described in the section on selecting the count clock.

3.1.4 Selecting the PPG Start Method

The PPG can be started by one of the three methods below.

- Direct writing from the CPU to the PPG start register (TRG:PEN) is used to start PPG
- GATE signal from a multifunction timer is used to start the PPG
- PPG start signal of a timing generator is used to start the PPG

Besides the above start methods, start method by IGBT mode can also be selected. For details, see the chapter on PPG IGBT mode.

For the operation modes indicated by the ☆ mark in Table 3-1, the PPG start method can be selected from the above three. For the operation modes indicated by the ★ mark, only the start method of direct writing to the PPG start register (TRG:PEN) can be used. The PPG start method is selected by the GATEC:STRG and PPGC:TTRG registers. This setting is used to connect the corresponding start signal to the PPG. The register settings, PPG operation modes, and selected PPG start signals are shown in Table 3-2. The GATEC:STRGn and PPGCn:TTRG registers exist only when n is an even number. The start methods for both channel n (even numbers) and channel n+1 (odd numbers) are determined by specifying the registers.

Table 3-2 Selecting the PPG Start Method

Register Setting		PPG Operation Mode	PPG Start Signal	Additional Notes
GATEC: STRGn	PPGCn: TTRG			
0	0	8-bit	PPG start register (TRG:PEN)	
		16-bit		1
		8+8-bit		1
		16+16-bit		1, 2
1	0	8-bit	GATE signal from multifunction timer	3
		16-bit		4
		8+8-bit	Setting prohibited	7
		16+16-bit		7
X	1	8-bit	Start signal from timing generator	5
		16-bit		6
		8+8-bit	Setting prohibited	7
		16+16-bit		7

Additional Notes:

1. For operation modes that use multiple PPG channels (8+8-bit, 16-bit, and 16+16-bit) and the start method of writing the PPG start register (TRG:PEN), "1" is written simultaneously to the TRG:PEN registers of all channels being used to start the PPG. Also, "0" is written simultaneously to the TRG:PEN registers to stop the PPG. The count cycle may be shifted if values are not written simultaneously.
2. In 16+16-bit PPG operation mode, set both the n channel and n+2 channel registers to "0" for the GATEC:STRGn and PPGCn:TTRG registers.
3. In this case, the GATE signal from the multifunction timer is connected to even channels only. Odd channels connect TRG:PEN.
4. In this case, GATE signals from the multifunction timer are connected to both even and odd channels.
5. In this case, the start signal from the timing generator is connected to even channels only. Odd channels connect TRG:PEN.

6. In this case, the start signals from the timing generator are connected to both the even and odd channels.
7. In the case of 8+8-bit mode and 16+16-bit mode, the start by writing the PPG start register (TRG:PEN) only can be selected.

3.1.5 Selecting the Count Clock

The count clock for each PPG channel can be selected from four frequency dividing ratios by using the PCLK frequency divider. Table 3-3 shows the register settings and selected count clock.

Table 3-3 Count Clock Selection Table

PPGC:PCS1	PPGC:PCS0	Count Clock Operation
0	0	Count clock performs 1 count for every PCLK
0	1	Count clock performs 1 count for every 4 PCLK cycles
1	0	Count clock performs 1 count for every 16 PCLK cycles
1	1	Count clock performs 1 count for every 64 PCLK cycles

In Table 3-1, the count clock can be selected using the PPGC:PCS1 and PCS0 registers for operation modes indicated by the ◎mark and ○ mark. For the operation modes indicated by the ○ mark, the count clock selection settings for the even channel side and odd channel side (PSC1, PSC0) must always be set to the same value. For the operation modes indicated by the ● mark, both edges of the prescaler side output are used for the count clock. The PSC1 and PSC0 register settings for these channels are ignored.

3.1.6 Specifying the Reload Register and Pulse Width

The pulse width of the PPG output signal is specified by the reload registers (PRLH and PRLL). The pulse width can be changed during PPG operation. Both the High width and Low width are specified. The pulse width that is output is a value found by multiplying the count clock cycle by a value that is +1 added to the value written to the reload register. If PPG channels are connected to form a 16-bit length, the 8-bit reload register that specifies the pulse width is also connected for specifying a 16-bit length value. For details, see 5-10 PPG reload registers n (PRLHn and PRLLn n=0 to 23). The relationship between the setting examples and output pulse widths are shown in Table 3-4.

Table 3-4 Examples of Reload Register Setting Values

PPG Bit Width	Reload Register Value	Output Pulse Width
8-bit	0x00	1 x Count clock cycle
	0x01	2 x Count clock cycle
	0xFF	256 x Count clock cycle
16-bit	0x0000	1 x Count clock cycle
	0x0001	2 x Count clock cycle
	0x00FF	256 x Count clock cycle
	0x0100	257 x Count clock cycle
	0xFFFF	65536 x Count clock cycle

3.1.7 Buffer Function of High Width Setting Reload Register

The High width setting reload register includes a buffer function. Operation of the buffer function is shown in Figure 3-6.

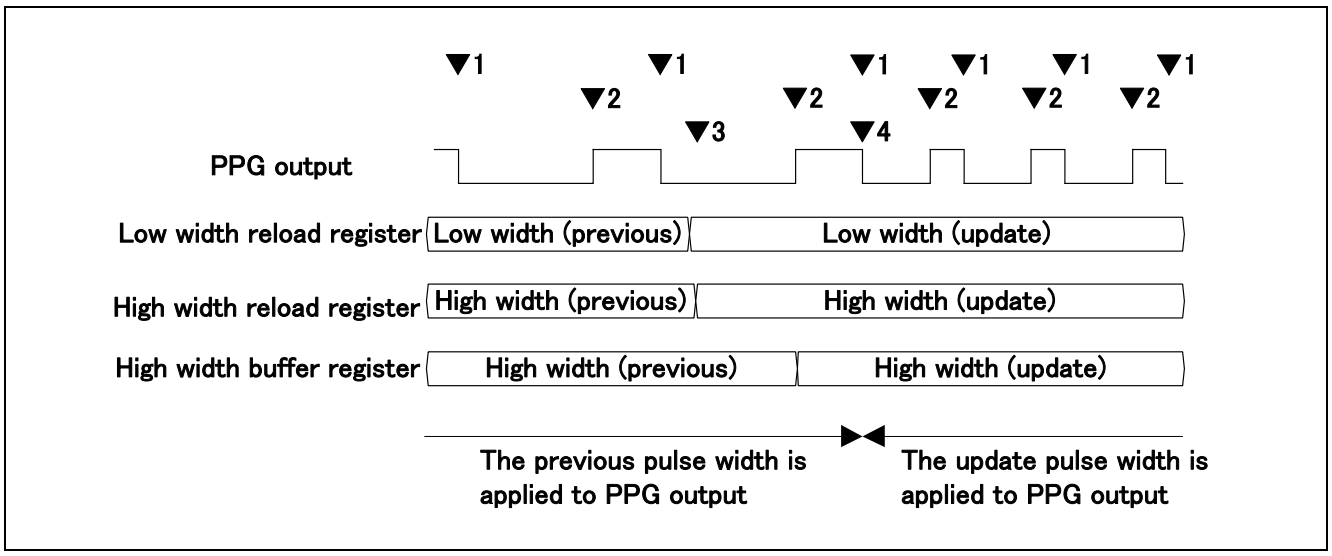
When the PPG output signal changes from High to Low (▼1 in the figure), the PPG counter imports the setting value of the Low width from the reload register. When the PPG output signal changes from Low to High (▼2 in figure), the PPG counter imports the setting value of the High width from the buffer register.

At the timing of ▼3, if the Low width setting value and High width setting value are changed from the CPU, the High width setting before the update is stored to the buffer register. At the next ▼2 timing, the PPG counter imports the High width setting value before the update from the buffer register and applies it to the output pulse width.

For this reason, until the timing at ▼4, the Low width and High width setting values before the update are applied in the PPG output. At the timing of ▼4, the Low width and High width setting values after the update are applied in the PPG output.

When the output pulse width settings are updated, a combination of the Low width and High width settings can be maintained.

Figure 3-6 High Width Setting Buffer Register Function



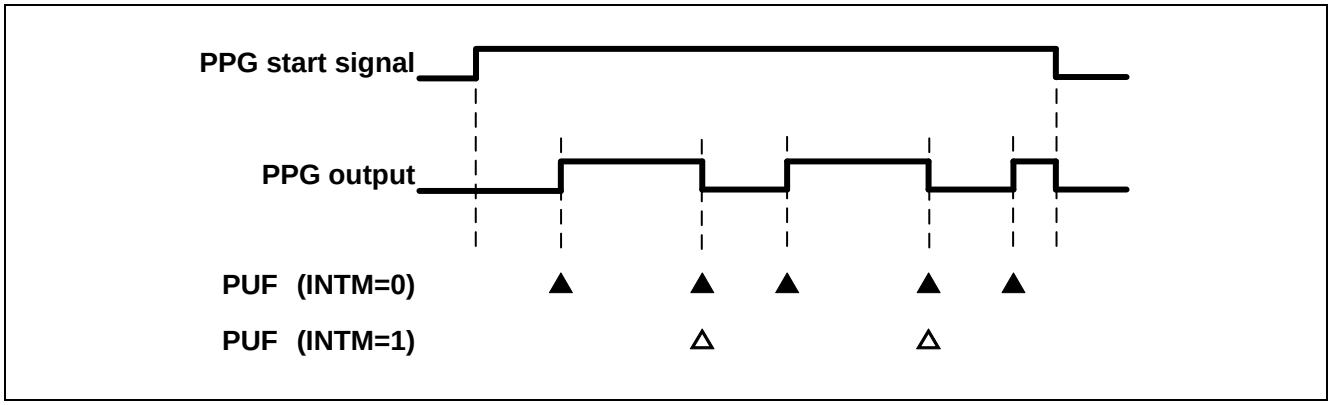
3.1.8 Interrupts

When the PPG changes the output signal (when the reload value count is ended and an underflow has occurred), 1 is set to the PUF of the PPG operation mode control register (PPGC). The selections below are performed using PPGCn: INTM.

- When PPGC:INTM=0, the setting is made when both the Low pulse and the High pulse end.
- When PPGC:INTM=1, the setting is made when the High pulse ends.

Figure 3-7 shows the PUF setting timing selection based on the INTM value. The PUF setting timing when INTM=0 (indicated by ▲) and when INTM=1 (indicated by △) is shown.

Figure 3-7 PUF Setting Timing Selection Based on INTM



If the PPG channels are connected to perform operation using a 16-bit length, the PUF for both the even and odd channels are set simultaneously.

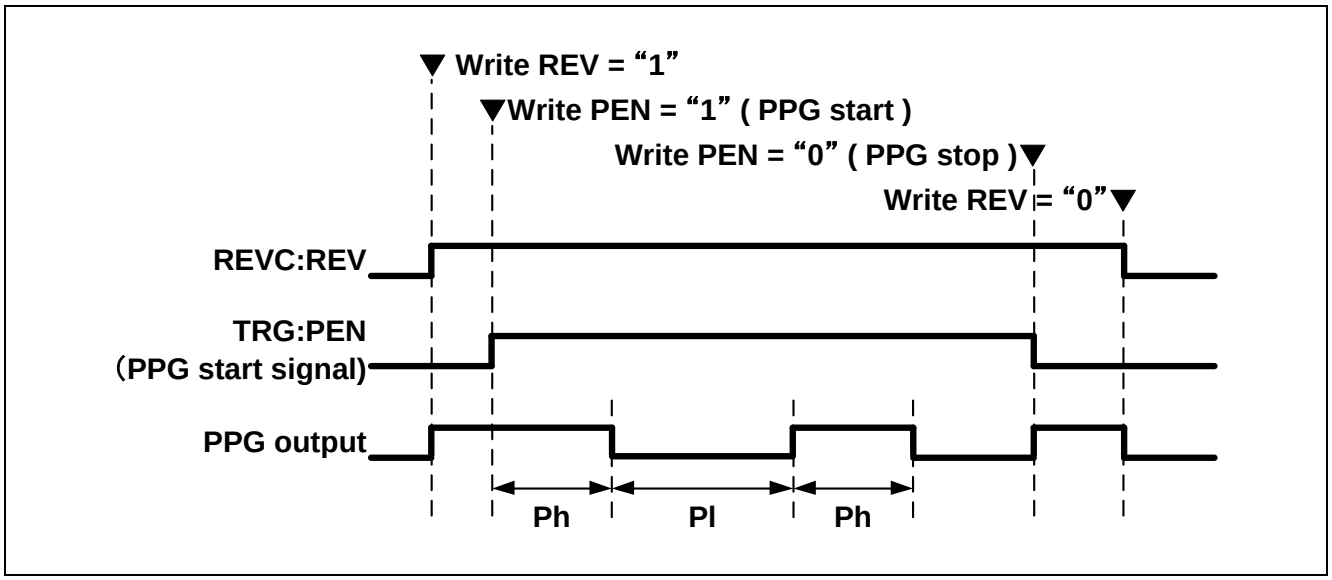
The PUFs that are set from PPG can be cleared by writing "0" to PUF from the CPU.

If interrupt enable is set by the PPG operation mode control register (PIE=1), PUF can be used to assert the interrupt signal.

3.1.9 Polarity Reversal by REVn Register

The polarity of the PPG output signal can be reversed using the REVC:REV register setting. Figure 3-8 shows the output waveform for REV=1 and the 8-bit PPG operation mode.

Figure 3-8 Output Waveform When REVn = 1



The connection diagrams of Figure 3-1, Figure 3-13, Figure 3-14, and Figure 3-15 show configurations where the PPG output is reversed by the REV register value directly. For this reason, when REV=1, the followings are performed.

- The output level before operation start of the PPG output and output level after operation stop are reversed to the High level.
- The Low-High of the output pulse is reversed, and the relationship of the Low width setting and High width setting of the reload register is reversed.
- PUF is set when PPGC:INTM=1 and when the Low pulse ends.
- In 8+8-bit PPG operation mode and 16+16-bit PPG operation mode, the operation clock supplied to the PPG output side from the prescaler side is reversed.

In Figure 3-8, the Low width (Pl) and High width (Ph) for the output pulse can be specified as shown below.

T (Count clock cycle) = Count clock cycle selected by PPGC:PCS1 and PCS0 registers
Pl (PPG output Low width) = T x (PRLH register value + 1)
Ph (PPG output High width) = T x (PRLL register value + 1)

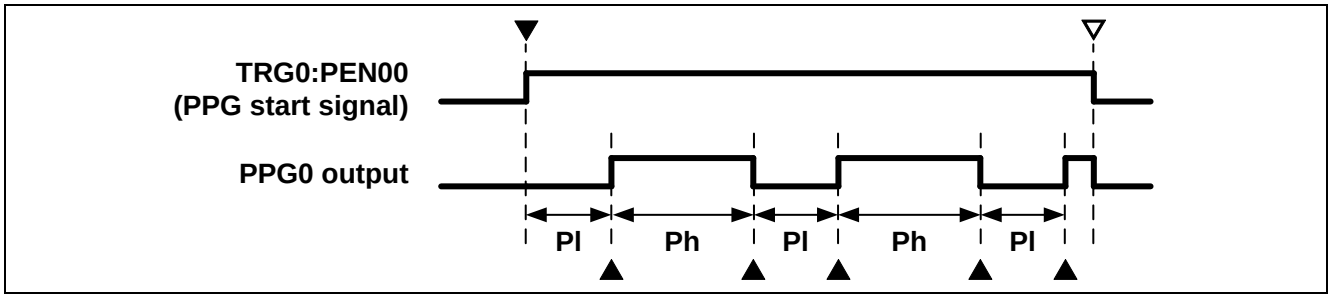
3.1.10 8-bit PPG Operation Mode Example

This section shows an operation example of 8-bit PPG operation mode using PPG-ch.0. Table 3-5 shows the register initial settings used in this operation example. Figure 3-12 shows the output waveforms of this operation example.

Table 3-5 8-bit PPG Operation Mode Register Setting Example

Register Name	Bit Write Value	Setting Description	Remarks
PPGC0	TTRG=0 MD1,MD0=00 PCS1,PCS0=01 INTM=0 PUF=0 PIE=0	Start by TRG0:PEN00 8-bit PPG operation mode PCLK/4 is selected for count clock PUF interrupt flag is set for both Low and High PUF flag is initialized Generation of interrupts is prohibited	See Note 1.
GATEC0	STRG0=0 STRG2=X	Start by TRG0:PEN00 This is no relation setting for other PPG channel.	
REVC0	REV00=0 REV01 to 15=X	PPG0 is output at positive polarity This is no relation setting for other PPG channel.	

Figure 3-9 Example of 8-bit PPG Operation Mode Output Waveform



The symbols in Figure 3-9 have the meanings shown below.

▼ PPG operation start (See Note 2.)
▽ PPG operation stop (See Note 3.)
▲ PPGC0:PUF setting timing (See Note 4.)
Pl PPG0 output Low width
Ph PPG0 output High width

The Low width (Pl) and High width (Ph) of the PPG0 output can be specified as shown below.

T (Count clock cycle) = PCLK cycle x 4 (See Note 1.)
Pl (PPG0 output Low width) = T x (PRLL0 register value + 1)
Ph (PPG0 output High width) = T x (PRLH0 register value + 1)

Additional Notes:

1. *T (Count clock cycle) is determined by the clock cycle selected by the count clock selection registers (PPGC0:PCS1,PCS0) of PPG0.*
2. *When 1 is written to TRG0:PEN00, the PPG start signal is asserted, and the PPG starts operation.*
3. *When 0 is written to TRG0:PEN00, the PPG start signal is negated, and the PPG stops operation.*
4. *Based on the specified PPGC0:INTM=0, PPGC0:PUF is set at the timing indicated by ▲.*

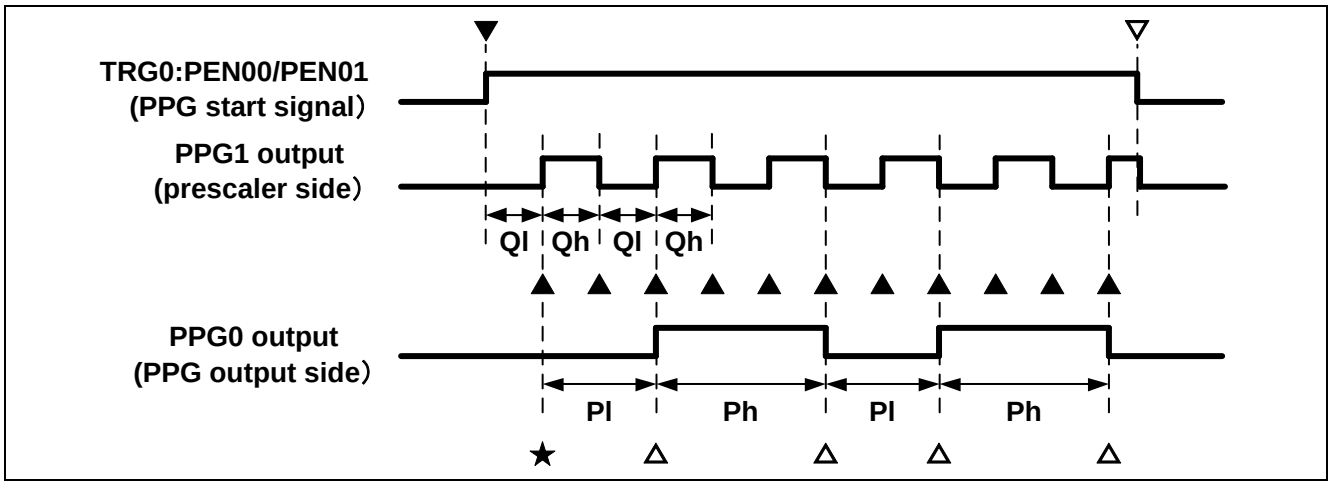
3.1.11 8+8-bit PPG Operation Mode Example

This section shows an operation example of 8+8-bit PPG operation mode using PPG-ch.0 and ch.1. Table 3-6 shows the register settings used in this operation example. Figure 3-10 shows the output waveform of this operation example.

Table 3-6 8+8-bit PPG Operation Mode Register Setting Example

Register Name	Bit Write Value	Setting Description	Remarks
PPGC0	TTRG=0 MD1,MD0=01 PCS1,PCS0=00 INTM=0 PUF=0 PIE=0	Start by TRG0:PEN00/PEN01 8+8-bit PPG operation mode Setting is ignored PUF interrupt flag is set for both Low and High PUF flag is initialized Generation of interrupts is prohibited	See Note 2.
PPGC1	PCS1,PCS0=01 INTM=0 PUF=0 PIE=0	PCLK/4 is selected for count clock PUF interrupt flag is set for both Low and High PUF flag is initialized Generation of interrupts is prohibited	See Note 1.
GATEC0	STRG0=0 STRG2=X	Start by TRG0:PEN00/PEN01 This is no relation setting for other PPG channel.	
REVC0	REV00=0 REV01=0 REV02 to 15=X	PPG0 (PPG output side) is output at positive polarity PPG1 (prescaler side) is output at positive polarity This is no relation setting for other PPG channel.	See Note 9. See Note 9.

Figure 3-10 8+8-bit PPG Operation Mode Output Waveform Example



The symbols in Figure 3-10 have the meanings shown below.

▼	PPG operation start (See Note 3.)
▽	PPG operation stop (See Note 4.)
▲	PPGC1:PUF setting timing (prescaler side, see Note 5.)
▵	PPGC0:PUF setting timing (PPG output side, see Note 6.)
★	PPG output side count operation start timing (See Note 7.)
Ql	PPG1 output (prescaler side) Low pulse width
Qh	PPG1 output (prescaler side) High pulse width
Pl	PPG0 output (PPG output side) Low pulse width
Ph	PPG0 output (PPG output side) High pulse width

The Low width (Ql) and High width (Qh) of the PPG1 output (prescaler side) and the Low width (Pl) and High width (Ph) of the PPG0 output (PPG output side) can be specified as shown below.

T (Prescaler side clock cycle)	= PCLK cycle x 4 (See Note 1.)
Ql (PPG1 output pulse Low width)	= T x (PRLL1 register value + 1)
Qh (PPG1 output pulse High width)	= T x (PRLH1 register value + 1)
Qa (PPG output side clock cycle)	= (Ql + Qh)/2 (Ql and Qh average value: See Note 8.)
Pl (PPG0 output pulse Low width)	= Qa x (PRLL0 register value + 1)
Ph (PPG0 output pulse High width)	= Qa x (PRLH0 register value + 1)

Additional Notes:

1. *T (Prescaler side clock cycle) is determined by the clock cycle selected by the count clock selection registers (PPGC1:PCS1 and PCS0) of PPG1 (Prescaler side).*
2. *The values of the count clock selection registers (PPGC0:PCS1 and PCS0) of PPG0 (PPG output side) are ignored.*
3. *When 11 is written simultaneously to TRG0:PEN00 and PEN01, the PPG start signal is asserted, and the PPG starts operation. If 11 is not written simultaneously, the count cycle may be shifted.*
4. *When "00" is written simultaneously to TRG0:PEN00 and PEN01, the PPG start signal is negated, and the PPG stops operation. If "00" is not written simultaneously, the count cycle may be shifted.*
5. *Based on the specified PPGC1:INTM=0, PPGC1:PUF is set at the timing indicated by ▲. (Prescaler side)*
6. *Based on the specified PPGC0:INTM=0, PPGC0:PUF is set at the timing indicated by ▵. (PPG output side)*
7. *PPG0 (PPG output side) starts counting from the position of ★ after Ql has elapsed after the start instruction in ▼. The PPG output side imports the output pulse width from the reload register at the timing in ★. After the ▼start instruction, if the output pulse width setting on the PPG output side was overwritten before the timing at ★, the setting for the output pulse width before that time is not applied.*
8. *The PPG0 (PPG output side) count operation is performed at both the PPG1 (prescaler side) output rising and falling edges. For this reason, in the above equation, Qa is the average value of Ql and Qh. It is recommended that the same value be used for the Low pulse width and High pulse width at the prescaler side. Be careful because, if the values for the Low pulse width and High pulse width at the prescaler side are different, when the pulse count on the PPG output side is odd, the output pulse width on the PPG output side will not match the above equation.*
9. *The PPG0 (PPG output side) output signal and PPG1 (Prescaler side) output signal can be reversed using the REVC0:REV00 and REV01 registers.*

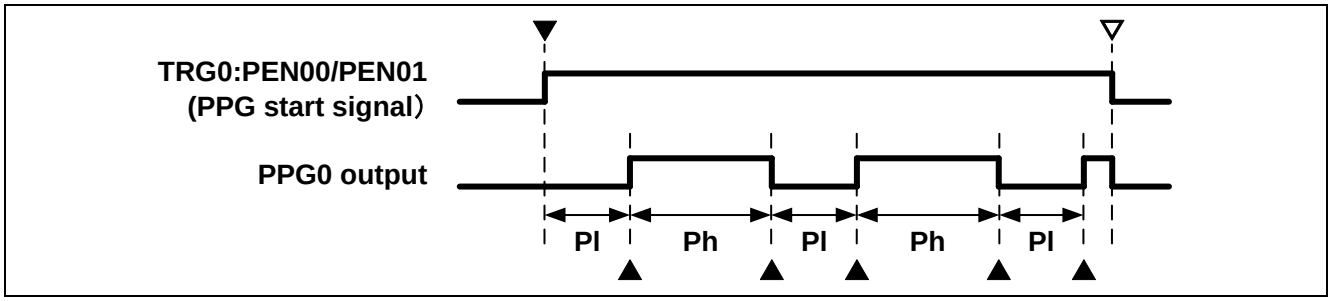
3.1.12 16-bit PPG Operation Mode Example

This section shows an operation example of 16-bit PPG operation mode using PPG-ch.0 and ch.1. Table 3-7 shows the register settings used in this operation example. Figure 3-11 shows the output waveform of this operation example.

Table 3-7 16-bit PPG Operation Mode Register Setting Example

Register Name	Bit Write Value	Setting Description	Remarks
PPGC0	TTRG=0 MD1,MD0=10 PCS1,PCS0=01 INTM=0 PUF=0 PIE=0	Start by TRG0:PEN00/PEN01 16-bit PPG operation mode PCLK/4 is selected for count clock PUF interrupt flag is set for both Low and High PUF flag is initialized Generation of interrupts is prohibited	See Note 1.
PPGC1	PCS1,PCS0=01 INTM=0 PUF=0 PIE=0	PCLK/4 is selected for count clock PUF interrupt flag is set for both Low and High PUF flag is initialized Generation of interrupts is prohibited	See Note 1.
GATEC0	STRG0=0 STRG2=X	Start by TRG0:PEN00/PEN01 This is no relation setting for other PPG channel.	
REVC0	REV00=0 REV01=0 REV02 to 15=X	PPG0 is output at positive polarity PPG1 is output at positive polarity This is no relation setting for other PPG channel.	See Note 5.

Figure 3-11 16-bit PPG Operation Mode Output Waveform Example



The symbols in Figure 3-11 have the meanings shown below.

▼ PPG operation start (See Note 2.)
▽ PPG operation stop (See Note 3.)
▲ PPGC0:PUF and PPGC1:PUF setting timing (See Note 4.)
Pl PPG0 output Low pulse width
Ph PPG0 output High pulse width

The Low width (Pl) and High width (Ph) of the PPG0 output can be specified as shown below.

T (Count clock cycle) = PCLK cycle x 4 (See Note 4.)
Pl (PPG0 output pulse Low width) =T x (PRLH1 register value x 256 + PRLL1 register value + 1)
Ph (PPG0 output pulse High width) =T x (PRLH0 register value x 256 + PRLL0 register value + 1)

Additional Notes:

1. *The values for the PPG0 and PPG1 count clock selection registers (PPGC0:PCS1 and PCS0) and (PPGC1:PCS1 and PCS0) must be the same. T (Count clock cycle) is determined by this value.*
2. *When 11 is written simultaneously to TRG0:PEN00 and PEN01, the PPG start signal is asserted, and the PPG starts operation. If 11 is not written simultaneously, the count cycle may be shifted.*
3. *When 00 is written simultaneously to TRG0:PEN00 and PEN01, the PPG start signal is negated, and the PPG stops operation. If 00 is not written simultaneously, the count cycle may be shifted.*
4. *Based on the specified PPGC0:INTM=0, PPGC0:PUF is set at the timing indicated by ▲. Based on the specified PPGC1:INTM=0, PPGC1:PUF is set at the timing indicated by ▲. In this case, both flags are set simultaneously.*
5. *Although it is omitted in the figure, when REVC0:REV00=0 and REVC0:REV01=0 are specified, the same output waveform as the PPG0 output is obtained for PPG1 output.*

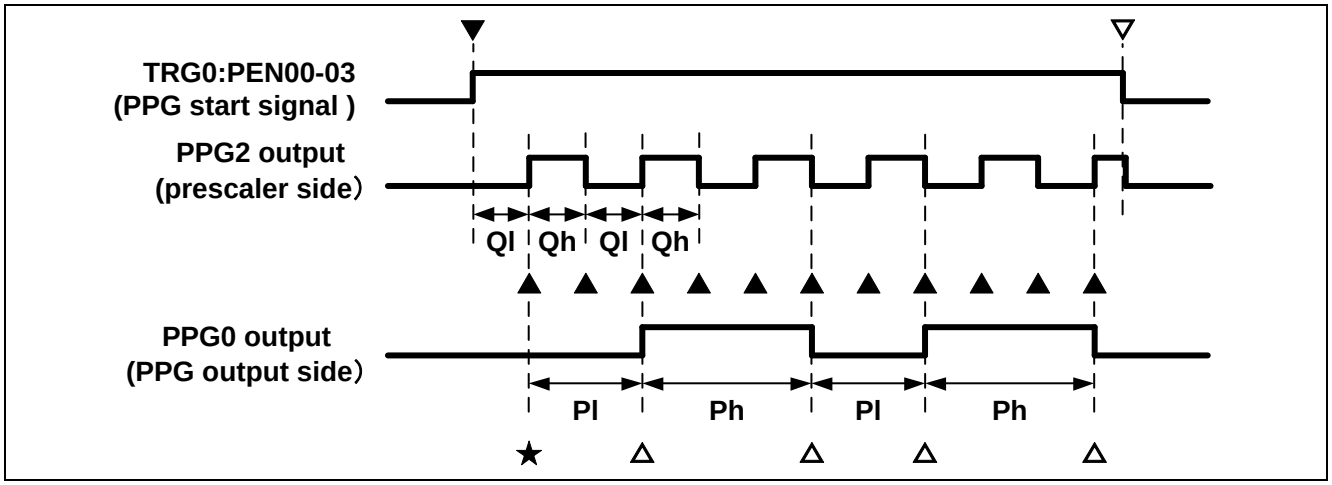
3.1.13 16+16-bit PPG Operation Mode Example

This section shows an operation example of 16+16-bit PPG operation mode using PPG-ch.0, ch.1, ch.2, and ch.3. Table 3-8 shows the register settings used in this operation example. Figure 3-12 shows the output waveform of this operation example.

Table 3-8 16+16-bit PPG Operation Mode Register Setting Example

Register Name	Bit Write Value	Setting Description	Remarks
PPGC0	TTRG=0 MD1,MD0=11 PCS1,PCS0=00 INTM=0 PUF=0 PIE=0	Start by TRG0:PEN00/PEN01/PEN02/PEN03 16+16-bit PPG operation mode Setting is ignored PUF interrupt flag is set for both Low and High PUF flag is initialized Generation of interrupts is prohibited	See Note 2.
PPGC1	PCS1,PCS0=00 INTM=0 PUF=0 PIE=0	Setting is ignored PUF interrupt flag is set for both Low and High PUF flag is initialized Generation of interrupts is prohibited	See Note 2.
PPGC2	TTRG=0 MD1,MD0=11 PCS1,PCS0=01 INTM=0 PUF=0 PIE=0	Start by TRG0:PEN00/PEN01/PEN02/PEN03 16+16-bit PPG operation mode PCLK/4 is selected for count clock PUF interrupt flag is set for both Low and High PUF flag is initialized Generation of interrupts is prohibited	See Note 1.
PPGC3	PCS1,PCS0=01 INTM=0 PUF=0 PIE=0	PCLK/4 is selected for count clock PUF interrupt flag is set for both Low and High PUF flag is initialized Generation of interrupts is prohibited	See Note 1.
GATEC0	STRG0=0 STRG2=0	Start by TRG0:PEN00/PEN01/PEN02/PEN03 Start by TRG0:PEN00/PEN01/PEN02/PEN03	
REVC0	REV00=0 REV01=0 REV02=0 REV03=0 REV04 to 15=X	PPG0 and PPG1 (PPG output side) are output at positive polarity PPG2 and PPG3 (prescaler side) are output at positive polarity This is no relation setting for other PPG channel.	See Note 9. See Note 9.

Figure 3-12 16+16-bit PPG Operation Mode Output Waveform Example



The symbols in Figure 3-12 have the meanings shown below.

▼	PPG operation start (See Note 3.)
▽	PPG operation stop (See Note 4.)
▲	PPGC2:PUF and PPGC3:PUF setting timing (prescaler side, See Note 5.)
△	PPGC0:PUF and PPGC1:PUF setting timing (PPG output side, see Note 6.)
★	PPG output side count operation start timing (See Note 7.)
Ql	PPG2 output (prescaler side) Low pulse width
Qh	PPG2 output (prescaler side) High pulse width
Pl	PPG0 output (PPG output side) Low pulse width
Ph	PPG0 output (PPG output side) High pulse width

The Low width (Ql) and High width (Qh) of the PPG2 output (prescaler side) and the Low width (Pl) and High width (Ph) of the PPG0 output (PPG output side) can be specified as shown below.

T (Prescaler side clock cycle)	= PCLK cycle x 4 (See Note 1.)
Ql (PPG2 output pulse Low width)	= T x (PRLH3 register value x 256 + PRLL3 register value + 1)
Qh (PPG2 output pulse High width)	= T x (PRLH2 register value x 256 + PRLL2 register value + 1)
Qa (PPG output side clock cycle)	= (Ql + Qh)/2 (Ql and Qh average value: See Note 8.)
Pl (PPG0 output pulse Low width)	= Qa x (PRLH1 register value x 256 + PRLL1 register value + 1)
Ph (PPG0 output pulse High width)	= Qa x (PRLH0 register value x 256 + PRLL0 register value + 1)

Additional Notes:

1. *T (Prescaler side clock cycle) is determined by the count clock cycle selected by the count clock selection registers (PPGC2:PCS1, PCS0 and PPGC3:PCS1, PCS0) of PPG2 and PPG3 (16-bit prescaler side). PCS1 and PCS0 of PPGC2 and PPGC3 must always be set to the same value.*
2. *The values of the count clock selection registers (PPGC0:PCS1, PCS0 and PPGC1:PCS1, PCS0) of PPG0 and PPG1 (16-bit PPG output side) are ignored.*
3. *When 1111 is written simultaneously to TRG0:PEN00 to PEN03, the PPG start signal is asserted, and the PPG starts operation. If 1111 is not written simultaneously, the count cycle may be shifted.*
4. *When "0000" is written simultaneously to TRG0:PEN00 to PEN03, the PPG start signal is negated, and the PPG stops operation. If 0000 is not written simultaneously, the count cycle may be shifted.*

5. *Based on the specified PPGC2:INTM=0, PPGC2:PUF is set at the timing indicated by ▲. Based on the specified PPGC3:INTM=0, PPGC3:PUF is set at the timing indicated by ▲. In this case, both flags are set simultaneously.*
6. *Based on the specified PPGC0:INTM=0, PPGC0:PUF is set at the timing indicated by ⊿. Based on the specified PPGC1:INTM=0, PPGC1:PUF is set at the timing indicated by ⊿. In this case, both flags are set simultaneously.*
7. *PPG0 (PPG output side) starts counting from the position of ★ after Ql has elapsed after the start instruction in ▼. The PPG output side imports the output pulse width from the reload register at the timing in ★. After the ▼ start instruction, if the output pulse width setting on the PPG output side was overwritten before the timing at ★, the setting for the output pulse width before that time is not applied.*
8. *The PPG0 (PPG output side) count operation is performed at both the PPG2 (prescaler side) output rising and falling edges. For this reason, in the above equation, Qa is the average value of Ql and Qh. It is recommended that the same value be used for the Low pulse width and High pulse width at the prescaler side. Be careful because, if the values for the Low pulse width and High pulse width at the prescaler side are different, when the pulse count on the PPG output side is odd, the output pulse width on the PPG output side will not match the above equation.*
9. *Although it is omitted from the figure, when REVC0:REV00 to REV03=0000, the same output waveform as PPG0 output is obtained for PPG1 output, and the same output waveform as PPG2 output is obtained for PPG3 output.*

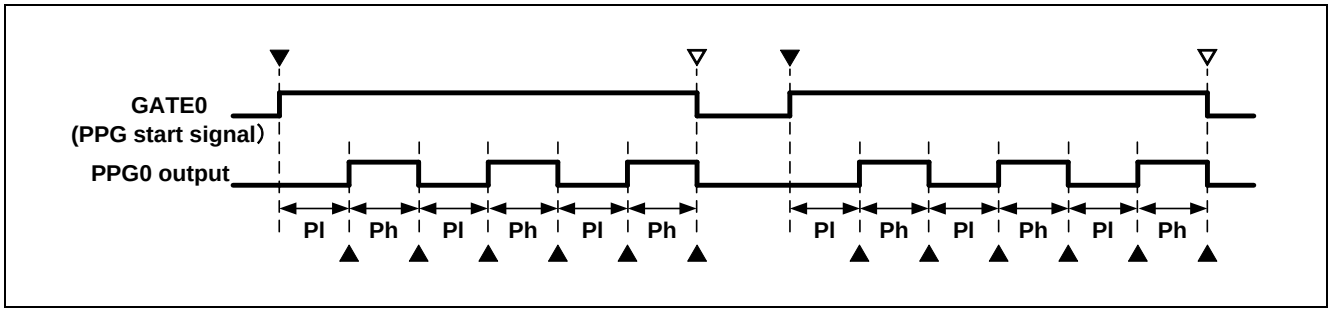
3.1.14 Example of PPG Operation by GATE Signals from Multifunction Timer

This section shows an operation example of PPG start by GATE signals from a multifunctional timer (in the case of 16-bit PPG operation mode using PPG-ch.0 and ch.1). Table 3-9 shows the register settings used in this operation example. Figure 3-13 shows the output waveform of this operation example.

Table 3-9 Register Setting Example of Start from Multifunction Timer (16-bit PPG Operation Mode)

Register Name	Bit Write Value	Setting Description	Remarks
PPGC0	TTRG=0 MD1,MD0=10 PCS1,PCS0=01 INTM=0 PUF=0 PIE=0	Start by GATE signal from multifunction timer 16-bit PPG operation mode PCLK/4 is selected for count clock PUF interrupt flag is set for both Low and High PUF flag is initialized Generation of interrupts is prohibited	
PPGC1	PCS1,PCS0=01 INTM=0 PUF=0 PIE=0	PCLK/4 is selected for count clock PUF interrupt flag is set for both Low and High PUF flag is initialized Generation of interrupts is prohibited	
GATEC0	STRG0=1 STRG2=X	Start by GATE signal from multifunction timer This is no relation setting for other PPG channel.	
REVC0	REV00=0 REV01=0 REV02 to 15=X	PPG0 is output at positive polarity PPG1 is output at positive polarity This is no relation setting for other PPG channel.	

Figure 3-13 Example of PPG Operation by GATE Signal from Multifunction Timer



The symbols in Figure 3-13 have the meanings shown below.

▼ PPG operation start (Asserting GATE0 signal from multifunction timer)
▽ PPG operation stop (Negating GATE0 signal from multifunction timer)
▲ PPGC0:PUF and PPGC1:PUF setting timing
Pl PPG0 output Low pulse width
Ph PPG0 output High pulse width

The Low width (Pl) and High width (Ph) of the PPG0 output can be specified as shown below.

T (Count clock cycle) = PCLK cycle x 4 (based on selected clock)
Pl (PPG0 output pulse Low width) = T x (PRLH1 register value x 256 + PRLL1 register value + 1)
Ph (PPG0 output pulse High width) = T x (PRLH0 register value x 256 + PRLL0 register value + 1)

3.2 Timing Generator Circuit Operations

The timing generator circuit is used for individually starting multiple PPGs at a specified timing. The PPG timer start signal is generated and output when the 8-bit upcounter and compare registers are compared and match.

3.2.1 Timing Generator Configuration

The timing generator consists of a prescaler, 8-bit upcounter, and four compare registers. Four PPG start signals are output per timing generator unit.

The block diagrams for timing generators 0, 1, and 2 are shown in Figure 3-14, Figure 3-15, and Figure 3-16, respectively.

Figure 3-14 Timing Generator Circuit 0 Block Diagram

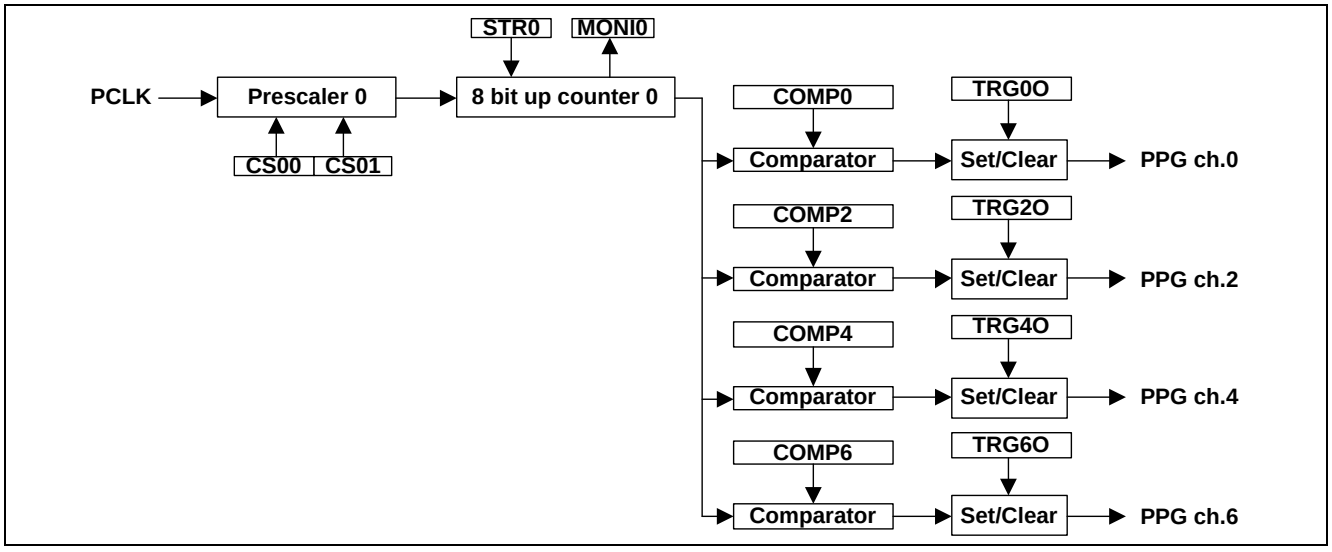


Figure 3-15 Timing Generator Circuit 1 Block Diagram

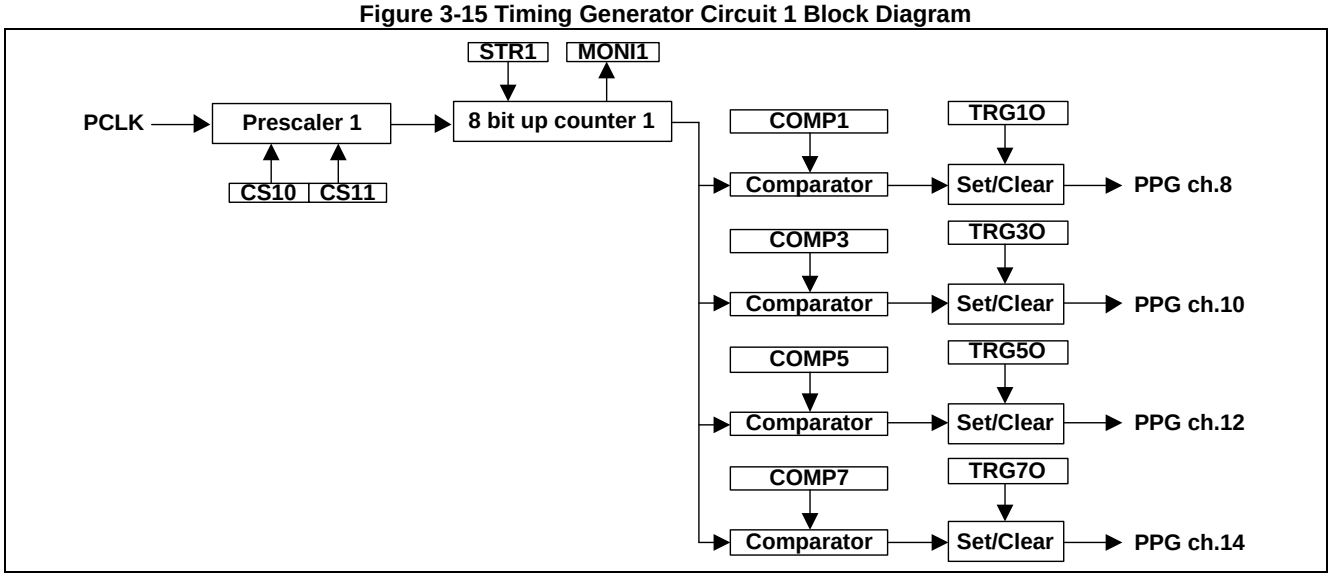
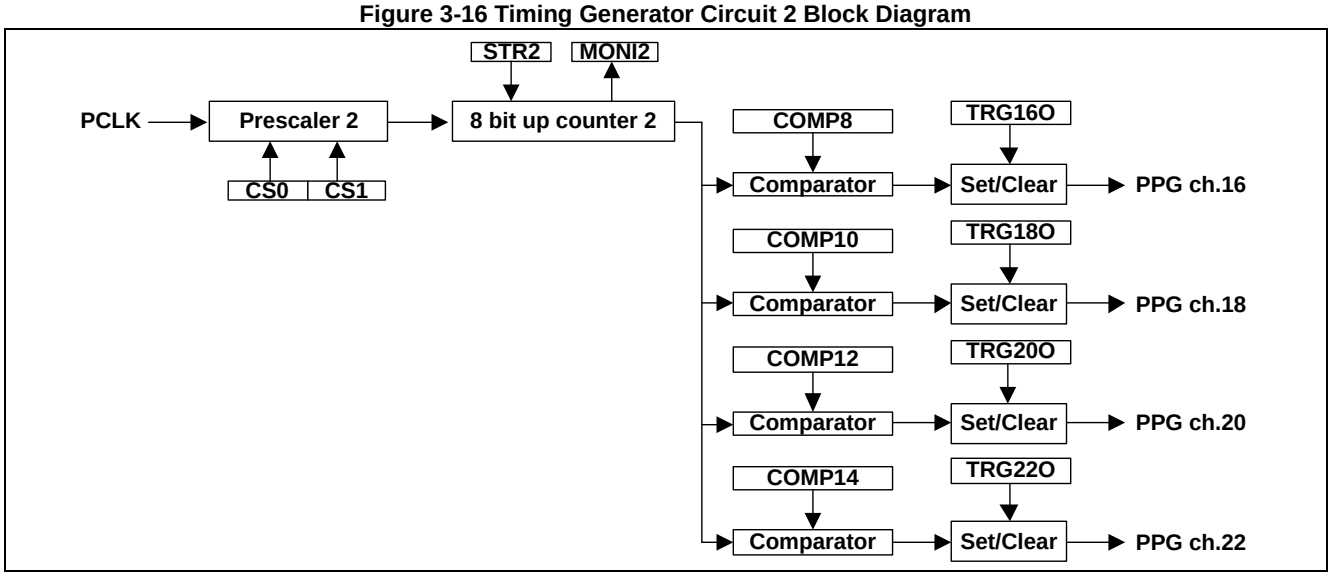


Figure 3-16 Timing Generator Circuit 2 Block Diagram



The blocks making up the timing generator circuit are described below.

- The prescaler can be used to select from four types of 8-bit upcounter operation clocks (PCLK/2, PCLK/8, PCLK/32, and PCLK/64).
- The 8-bit upcounter starts the count operation by writing TTCRx:STR="1".
- The 8-bit upcounter operation status can be read from the TTCRx:MONI bit.
- The four compare registers (COMPx) support the four respective PPG channels and set the start timing for each.
- If the count value of the 8-bit upcounter and compare register value both match, the respective PPG start signal is asserted.
- Writing TTCRx:TRGx0="0" negates the PPG start signal.
- Writing TTCRx:TRGx0="1" does not negate the PPG start signal.
- Once the 8-bit upcounter has counted up to 0xFF, the count operation is stopped.

The PPG start signal that is output from the timing generator is connected to the PPG even channels. The correspondence of the COMP register numbers, TTCRx:TRGxO register numbers, and the PPG channel numbers is different. Pay careful attention to the numbers when setting the registers. Table 3-10 shows the correspondence of the timing generator numbers, COMP register numbers, TTCRx:TRGxO register numbers, and PPG channel numbers.

Table 3-10 Correspondence between Timing Generator Register Numbers and PPG Channels

Timing Generator	COMP Register	TRGxO Register	Connected PPG Channel Number
Timing generator 0	COMP0	TTCR0:TRG0O	PPG ch.0
	COMP2	TTCR0:TRG2O	PPG ch.2
	COMP4	TTCR0:TRG4O	PPG ch.4
	COMP6	TTCR0:TRG6O	PPG ch.6
Timing generator 1	COMP1	TTCR1:TRG1O	PPG ch.8
	COMP3	TTCR1:TRG3O	PPG ch.10
	COMP5	TTCR1:TRG5O	PPG ch.12
	COMP7	TTCR1:TRG7O	PPG ch.14
Timing generator 2	COMP8	TTCR2:TRG16O	PPG ch.16
	COMP10	TTCR2:TRG18O	PPG ch.18
	COMP12	TTCR2:TRG20O	PPG ch.20
	COMP14	TTCR2:TRG22O	PPG ch.22

3.2.2 Timing Generator Operation Example

This section shows an operation example for PPG ch.2, ch.4, ch.6, and ch.8 start by timing generator 0. Table 3-11 shows an example of the initial register settings, and Figure 3-17 shows an example of the input/output signal waveform.

Table 3-11 Register Settings when Startinged by Timing Generator (16-bit PPG Operation Mode)

Register Name	Bit Write Value	Setting Description	Remarks
PPGC0 PPGC2 PPGC4 PPGC6	TTRG=1 MD1,MD0=10 PCS1,PCS0=01 INTM=0 PUF=0 PIE=0	Start by timing generator 16-bit PPG operation mode PCLK/4 is selected for count clock PUF interrupt flag is set for both Low and High PUF flag is initialized Generation of interrupts is prohibited	
PPGC1 PPGC3 PPGC5 PPGC7	PCS1,PCS0=01 INTM=0 PUF=0 PIE=0	PCLK/4 is selected for count clock PUF interrupt flag is set for both Low and High PUF flag is initialized Generation of interrupts is prohibited	
TTCR0	STR0=0 MONI0=0 CS01,CS00=00 TRG0O=0 TRG2O=0 TRG4O=0 TRG6O=0	Counter operation does not start (initial setting) Write value is ignored PCLK/2 is selected for 8-bit upcounter clock Start signal initialization for PPG ch.0 Start signal initialization for PPG ch.2 Start signal initialization for PPG ch.4 Start signal initialization for PPG ch.6	
REVC0	REV00-PPG07 REV08~15=X	PPG0 to PPG7 are output at positive polarity This is no relation setting for other PPG channel.	
COMP0	COMP0=0x40	Specifies output start timing of PPG0/PPG1	
COMP2	COMP2=0x80	Specifies output start timing of PPG2/PPG3	
COMP4	COMP4=0xC0	Specifies output start timing of PPG4/PPG5	
COMP6	COMP6=0xF0	Specifies output start timing of PPG6/PPG7	

The controlled content from the CPU and PPG operation at the timing of ▼ 1 to ▼6 shown in Figure 3-17 are described in detail below.

▼1 timing:
As shown in Table 3-11, the PPG and timing generator initial settings are performed. Because the initial settings cannot be performed during operation of the 8-bit upcounter, the initial settings are performed after reading the TTCR0:MONI0 register to confirm that the counter has stopped operation. When PPGC0, 2, 4, 6:TTRG=1 is specified, start from the timing generator is selected. The clock used by the 8-bit upcounter is selected by the TTCR0:CS01 and CS00 registers. The start timing of each PPG is specified by the COMP0, 2, 4, and 6 registers. If the PPG start signal is not asserted, COMPx=0x00 is specified.

▼2 timing:
Writing of TTCR0:STR0="1" is performed. The 8-bit upcounter starts the count operation. The TTCR0:MONI0 register is used to read the count operation status of the 8-bit upcounter. During the count operation, 1 is read. While the count operation is stopped, 0 is read.

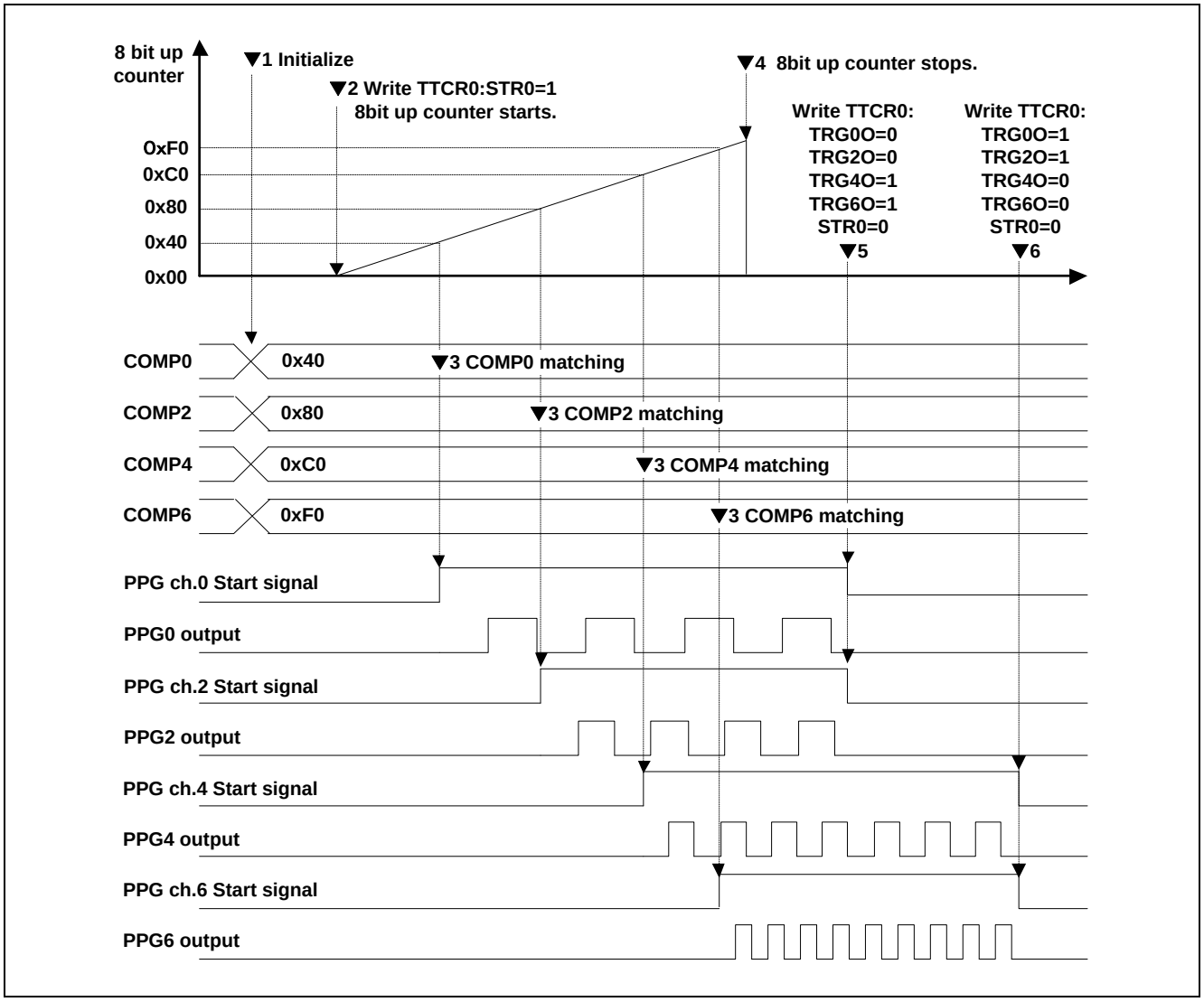
▼3 timing:
When the counter value of the 8-bit upcounter matches the value for COMP0, COMP2, COMP4, or COMP6, the PPG start signal from the timing generator for the respective channel is asserted. Each PPG starts output when the respective start signal is asserted.

▼4 timing:
The 8-bit upcounter stops once it has counted up to 0xFF.

▼5 timing:
Writing is performed for TRG0O=TRG2O=0, TRG4O=TRG6O=1, and STR0=0. Instructions are issued to PPG0 and PPG2 to stop operation and issued to PPG4 and PPG6 to continue operation. STR0=0 is written so that the 8-bit upcounter does not restart.

▼6 timing:
Writing is performed for TRG0O=TRG2O=1, TRG4O=TRG6O=0, and STR0=0, and a stop instruction is issued to PPG4 and PPG6.

Figure 3-17 Example of PPG Start Operation by Timing Generator 0



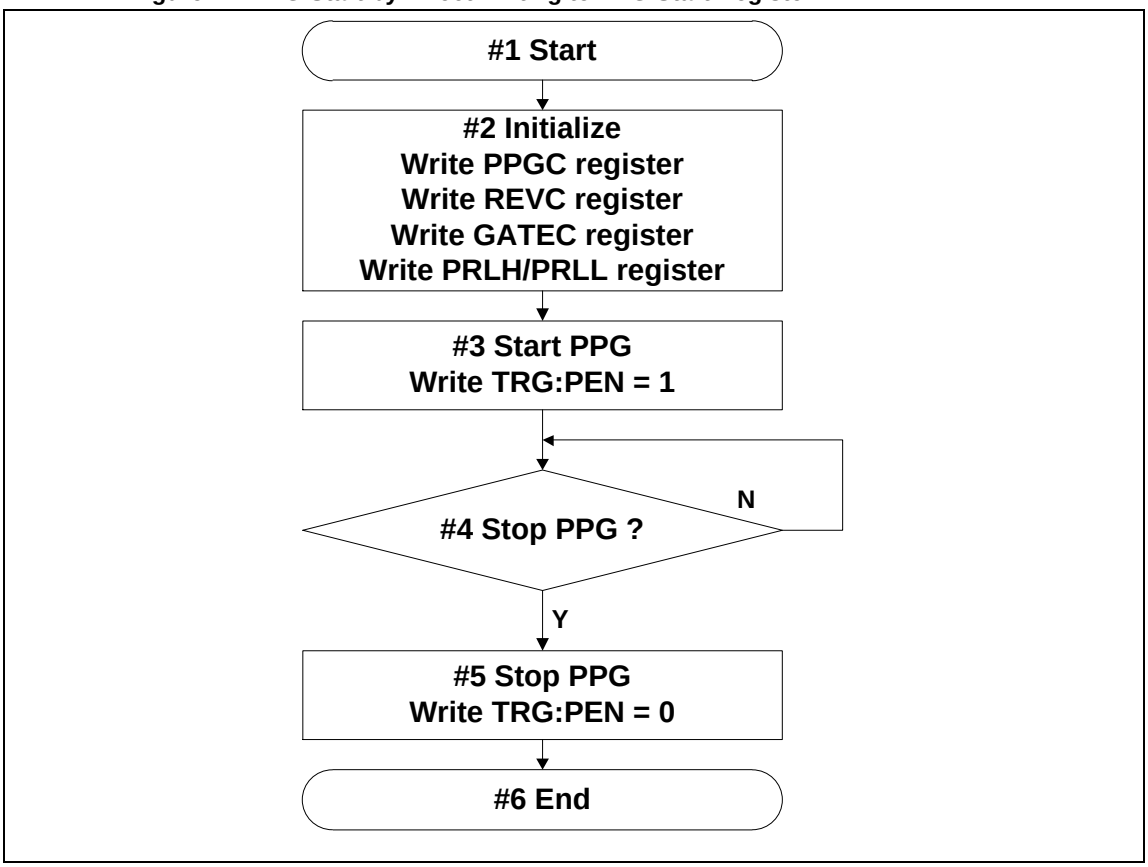
4. PPG Setup Procedure

This section gives a procedure for setting the PPG.

4.1 Example of PPG Start by Writing to PPG Start Register

Figure 4-1 shows an example of the setting procedure when the option PPG start by writing directly to the PPG start register (TRG:PEN) is selected. The numbers in the figure correspond to the numbers in the explanation below.

Figure 4-1 PPG Start by Direct Writing to PPG Start Register

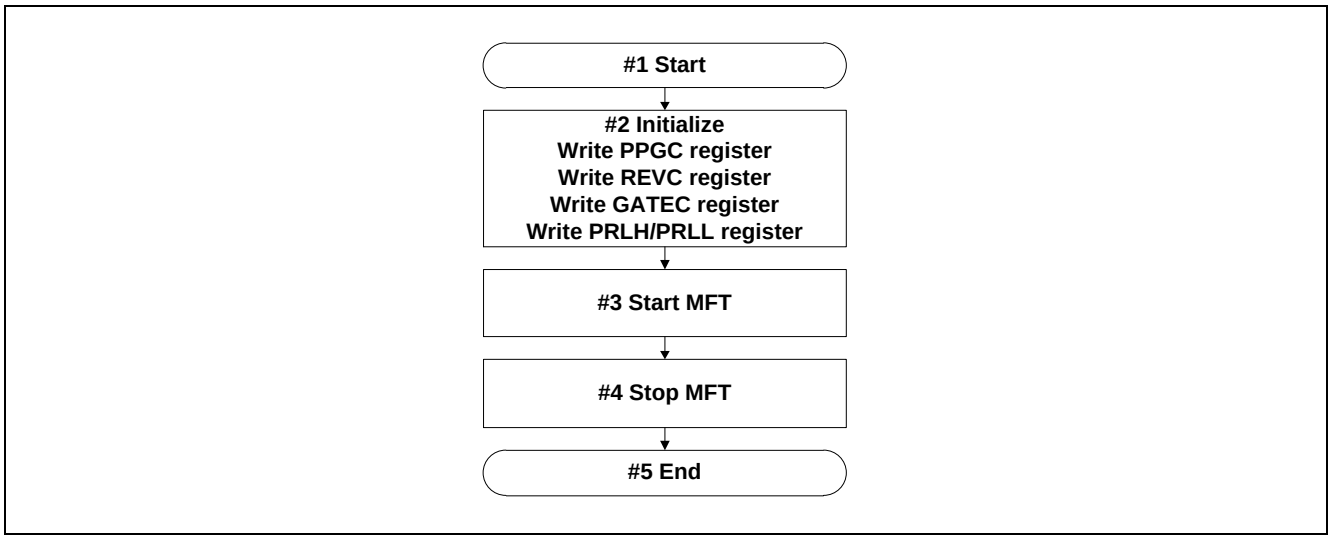


#1 The example setting procedure starts.
#2 Each register initializes. The settings PPGC:TTRG=0 and GATEC:STRG=0 are made to select PPG start by direct writing to the PPG start register (TRG:PEN). For the initial setting values of each register, see Table 3-5, Table 3-6, Table 3-7, and Table 3-8.
#3 1 is written to the PPG start register (TRG:PEN), and an instruction is issued to start PPG output.
#4 After PPG output starts, output continues until a command is issued to stop the start operation. When the start operation is stopped, proceed to #5.
#5 0 is written to the PPG start register (TRG:PEN), and an instruction is issued to stop PPG output.
#6 The setting procedure ends.

4.2 Example of PPG Start by GATE Signal from Multifunction Timer

Figure 4-2 shows the setting procedure when the option PPG start by GATE signal from multifunction timer (MFT) is selected. The numbers in the figure correspond to the numbers in the explanation below.

Figure 4-2 PPG Start by GATE Signal from Multifunction Timer



#1 The setting procedure starts.

#2 Each register initializes. The settings PPGC:TTRG=0 and GATEC:STRG=1 are made to select start by GATE signal from multifunction timer. For the initial settings of each register, see Table 3-9.

#3 Operation of the multifunction timer starts. Control is performed so that PPG output is started and stopped based on asserting and negating of the GATE signals supplied from the multifunction timer.

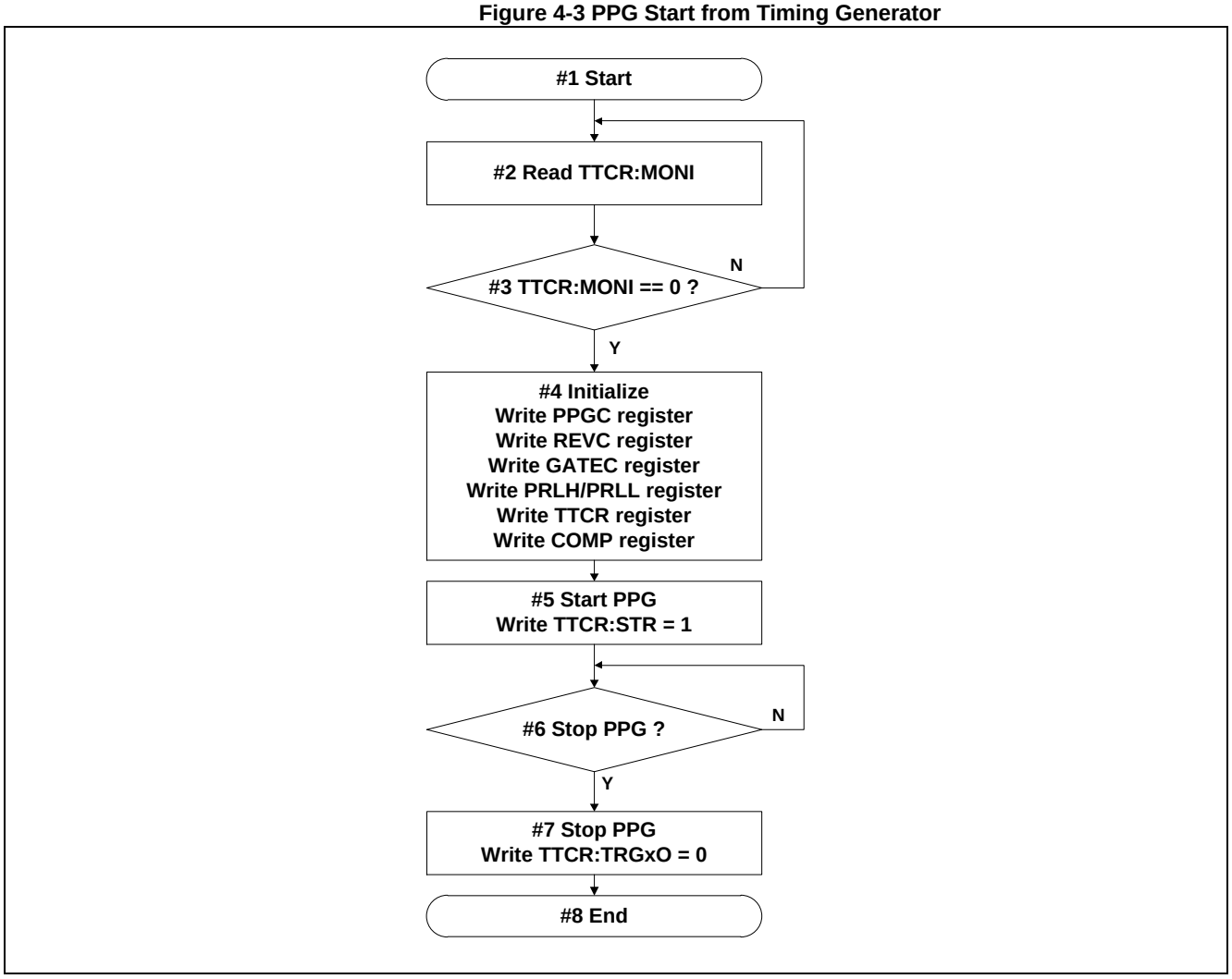
#4 Operation of the multifunction timer stops. When operation stops, perform control at the multifunction timer side so that the GATE signal ends in the negated state. When the GATE signal is in the negated state, the PPG stops any further output.

#5 The setting procedure ends.

4.3 Example of PPG Start by Timing Generator

Figure 4-3 shows the setting procedure when the option PPG start by timing generator is selected. The numbers in the figure correspond to the numbers in the explanation below.

Figure 4-3 PPG Start from Timing Generator



#1 The setting procedure starts.

#2, #3 If performing PPG start by a timing generator, initialization cannot be performed during the count operation of the 8-bit upcounter, and so reading of TTCR:MONI is performed to confirm that the count operation has stopped before proceeding to #4.

#4 Each register initializes. The setting PPGC:TTRG=1 is made to select start by timing generator. For the initial settings of each register, see Table 3-11.

#5 1 is written to TTCR:STR, and an instruction is issued to start the count of the 8-bit upcounter. When the setting value of the COMP register matches the value of the 8-bit upcounter, the PPG start signal is asserted, and PPG output is started.

#6 After PPG is started, output continues until a command is issued to stop the start operation. When the start operation is stopped, proceed to #7.

#7 0 is written to the TTCR:TRGxO register, and an instruction is issued to stop PPG output. The corresponding PPG start signal is negated, and PPG output is stopped.

#8 The setting procedure ends.

5. PPG Registers

This section explains the registers of PPG.
Table 5-1 lists the PPG registers.

Table 5-1 PPG Register List

Abbreviation	Register Name	Reference
TTCR0	Timing Generator PPG Start Trigger Control register 0	5.1
TTCR1	Timing Generator PPG Start Trigger Control register 1	5.2
TTCR2	Timing Generator PPG Start Trigger Control register 2	5.3
COMP0	Timing Generator PPG Compare register 0	5.4
COMP1	Timing Generator PPG Compare register 1	
COMP2	Timing Generator PPG Compare register 2	
COMP3	Timing Generator PPG Compare register 3	
COMP4	Timing Generator PPG Compare register 4	
COMP5	Timing Generator PPG Compare register 5	
COMP6	Timing Generator PPG Compare register 6	
COMP7	Timing Generator PPG Compare register 7	
COMP8	Timing Generator PPG Compare register 8	
COMP10	Timing Generator PPG Compare register 10	
COMP12	Timing Generator PPG Compare register 12	
COMP14	Timing Generator PPG Compare register 14	
TRG0	PPG Start register 0	5.5
TRG1	PPG Start register 1	5.6
REVC0	Output Reverse register 0	5.7
REVC1	Output Reverse register 1	5.8
PPGC0	PPG Operation Mode Control register 0	5.9
PPGC1	PPG Operation Mode Control register 1	
PPGC2	PPG Operation Mode Control register 2	
PPGC3	PPG Operation Mode Control register 3	
PPGC4	PPG Operation Mode Control register 4	
PPGC5	PPG Operation Mode Control register 5	
PPGC6	PPG Operation Mode Control register 6	
PPGC7	PPG Operation Mode Control register 7	
PPGC8	PPG Operation Mode Control register 8	
PPGC9	PPG Operation Mode Control register 9	
PPGC10	PPG Operation Mode Control register 10	
PPGC11	PPG Operation Mode Control register 11	
PPGC12	PPG Operation Mode Control register 12	
PPGC13	PPG Operation Mode Control register 13	
PPGC14	PPG Operation Mode Control register 14	
PPGC15	PPG Operation Mode Control register 15	
PPGC16	PPG Operation Mode Control register 16	
PPGC17	PPG Operation Mode Control register 17	
PPGC18	PPG Operation Mode Control register 18	
PPGC19	PPG Operation Mode Control register 19	
PPGC20	PPG Operation Mode Control register 20	
PPGC21	PPG Operation Mode Control register 21	
PPGC22	PPG Operation Mode Control register 22	
PPGC23	PPG Operation Mode Control register 23	

Abbreviation	Register Name	Reference
PRLH0	PPG Reload register H0	5.10
PRLL0	PPG Reload register L0	
PRLH1	PPG Reload register H1	
PRLL1	PPG Reload register L1	
PRLH2	PPG Reload register H2	
PRLL2	PPG Reload register L2	
PRLH3	PPG Reload register H3	
PRLL3	PPG Reload register L3	
PRLH4	PPG Reload register H4	
PRLL4	PPG Reload register L4	
PRLH5	PPG Reload register H5	
PRLL5	PPG Reload register L5	
PRLH6	PPG Reload register H6	
PRLL6	PPG Reload register L6	
PRLH7	PPG Reload register H7	
PRLL7	PPG Reload register L7	
PRLH8	PPG Reload register H8	
PRLL8	PPG Reload register L8	
PRLH9	PPG Reload register H9	
PRLL9	PPG Reload register L9	
PRLH10	PPG Reload register H10	
PRLL10	PPG Reload register L10	
PRLH11	PPG Reload register H11	
PRLL11	PPG Reload register L11	
PRLH12	PPG Reload register H12	
PRLL12	PPG Reload register L12	
PRLH13	PPG Reload register H13	
PRLL13	PPG Reload register L13	
PRLH14	PPG Reload register H14	
PRLL14	PPG Reload register L14	
PRLH15	PPG Reload register H15	
PRLL15	PPG Reload register L15	
PRLH16	PPG Reload register H16	
PRLL16	PPG Reload register L16	
PRLH17	PPG Reload register H17	
PRLL17	PPG Reload register L17	
PRLH18	PPG Reload register H18	
PRLL18	PPG Reload register L18	
PRLH19	PPG Reload register H19	
PRLL19	PPG Reload register L19	
PRLH20	PPG Reload register H20	
PRLL20	PPG Reload register L20	
PRLH21	PPG Reload register H21	
PRLL21	PPG Reload register L21	
PRLH22	PPG Reload register H22	
PRLL22	PPG Reload register L22	
PRLH23	PPG Reload register H23	
PRLL23	PPG Reload register L23	

Abbreviation	Register Name	Reference
GATEC0	Gate Function Control register 0	5.11
GATEC4	Gate Function Control register 4	
GATEC8	Gate Function Control register 8	
GATEC12	Gate Function Control register 12	
GATEC16	Gate Function Control register 16	
GATEC20	Gate Function Control register 20	

5.1 Timing Generator PPG Start Trigger Control Register 0 (TTCR0)

The TTCR0 register controls Timing Generator 0.

Register configuration

bit	15	14	13	12	11	10	9	8
Field	TRG6O	TRG4O	TRG2O	TRG0O	CS01	CS00	MONI0	STR0
Attribute	W	W	W	W	R/W	R/W	R	W
Initial value	-	-	-	-	0	0	0	-

Register functions

[bit15:12] TRG6O, TRG4O, TRG2O, TRG0O: PPG trigger stop bits

These bits can be used to negate the PPG start signal generated by the timing generator 0.

bit	Function
Reading	1 is always read.
Writing 0	PPG start signal from timing generator is negated, and PPG output is stopped.
Writing 1	No effect on the operation

[bit11:10] CS01, CS00: 8-bit UP counter clock select bits

These bits set an operation clock of the 8-bit UP counter.

bit11	bit10	Function
0	0	PCLK/2 [Initial value]
0	1	PCLK/8
1	0	PCLK/32
1	1	PCLK/64

[bit9] MONI0: 8-bit UP counter operation state monitor bit

This bit indicates the operation state of the 8-bit UP counter.

bit	Function
Reading 0	The 8-bit UP counter for comparison is stopped. [Initial value]
Reading 1	The 8-bit UP counter for comparison is operating.
Writing	No effect on the operation

[bit8] STR0: 8-bit UP counter operation enable bit

This bit issues an instruction to start operation of the 8-bit upcounter.

bit	Function
Reading	0 is always read.
Writing 0	No effect on the operation
Writing 1	Starts the 8-bit UP counter.

Notes:

- *In certain cases, the number of the TRGxO bit and the number of the PPG channel being controlled may be different. See Table 3-10.*
- *If the PPG start signal is asserted based on a match with the compare register and writing of TRGxO=0 occurs at the same time, the PPG start signal negate is given priority.*
- *If writing of TRGxO=0 is performed before the PPG start signal is asserted based on a match with the compare register, there is no effect on operation.*
- *After counting is started, the 8-bit upcounter stops once it has counted up to 0xFF. Once the count has started, to start the count again from 0x00, issue a count start instruction after first confirming that the count operation has stopped using the MONI0 bit.*
- *Change the value of the CS01 and CS00 bits is prohibited during operation of the 8-bit upcounter.*

5.2 Timing Generator PPG Start Trigger Control Register 1 (TTCR1)

The TTCR1 register controls a start of Timing Generator1.

Register configuration

bit	15	14	13	12	11	10	9	8
Field	TRG7O	TRG5O	TRG3O	TRG1O	CS11	CS10	MONI1	STR1
Attribute	W	W	W	W	R/W	R/W	R	W
Initial value	-	-	-	-	0	0	0	-

Register functions

[bit15:12] TRG7O, TRG5O, TRG3O, TRG1O: PPG trigger stop bits

These bits are used to negate the PPG start signal generated by the timing generator.

bit	Function
Reading	1 is always read.
Writing 0	PPG start signal from timing generator is negated, and PPG output is stopped.
Writing 1	No effect on the operation

[bit11:10] CS11, CS10: 8-bit UP counter clock select bits

These bits set an operation clock of 8-bit UP counter.

bit11	bit10	Function
0	0	PCLK/2 [Initial value]
0	1	PCLK/8
1	0	PCLK/32
1	1	PCLK/64

[bit9] MONI1: 8-bit UP counter operation state monitor bit

This bit indicates the operation state of 8-bit UP counter.

bit	Function
Reading 0	The 8-bit UP counter is stopped. [Initial value]
Reading 1	The 8-bit UP counter is operating.
Writing	No effect on the operation

[bit8] STR1: 8-bit UP counter operation enable bit

This bit enables the operation of 8-bit UP counter.

bit	Function
Reading	0 is always read.
Writing 0	No effect on the operation
Writing 1	Starts the 8-bit UP counter.

Note:

- *See notes in Timing generator PPG start trigger control register 0 (TTCR0). These notes also apply to the TTCR1 register in the same way.*

5.3 Timing Generator PPG Start Trigger Control Register 2 (TTCR2)

The TTCR2 register controls a start of Timing generator2.

Register configuration

bit	15	14	13	12	11	10	9	8
Field	TRG22O	TRG20O	TRG18O	TRG16O	CS21	CS20	MONI2	STR2
Attribute	W	W	W	W	R/W	R/W	R	W
Initial value	-	-	-	-	0	0	0	-

Register functions

[bit15:12] TRG22O, TRG20O, TRG18O, TRG16O: PPG trigger stop bits

These bits are used to negate the PPG start signal generated by the timing generator.

Bit	Function
Reading	1 is always read.
Writing 0	PPG start signal from timing generator is negated, and PPG output is stopped.
Writing 1	No effect on the operation

[bit11:10] CS21, CS20: 8-bit UP counter clock select bits

These bits set an operation clock of 8-bit UP counter.

bit11	bit10	Function
0	0	PCLK/2 [Initial value]
0	1	PCLK/8
1	0	PCLK/32
1	1	PCLK/64

[bit9] MONI2: 8-bit UP counter operation state monitor bit

This bit indicates the operation state of 8-bit UP counter.

bit	Function
Reading 0	The 8-bit UP counter is stopped. [Initial value]
Reading 1	The 8-bit UP counter is operating.
Writing	No effect on the operation

[bit8] STR2: 8-bit Counter Operation Enable bit

This bit issues an instruction to start operation of the 8-bit upcounter.

bit	Function
Reading	0 is always read.
Writing 0	No effect on the operation
Writing 1	Starts the 8-bit UP counter.

Note:

- *See notes in Timing generator PPG start trigger control register 0 (TTCR0). These notes also apply to the TTCR2 register in the same way.*

5.4 Timing Generator PPG Compare Register "n" (COMPn, where n=0 to 14)

The COMPn register sets a Compare value of the Timing Generator.

Register configuration

bit	15/7	14/6	13/5	12/4	11/3	10/2	9/1	8/0
Field	COMPn							
Attribute	R/W							
Initial value	0x00							

Register functions

[bit15:8, or bit7:0] COMP14 to COMP0: Compare Register channels 14 to 0

These bits can be used to set the PPG compare register value when started by a timing generator.

bit15:8, or bit7:0	Function
Reading	Reads the Compare value. Initial value is 0x00.
Writing	Writes a Compare value.

Notes:

- *This register is an 8-bit compare register, and one register is provided for each PPG start signal. In certain cases, the number of this register and the number of the PPG channel being controlled may be different. See Table 3-10.*
- *When this register value matches the value of the 8-bit upcounter, a start signal is asserted for the corresponding PPG.*
- *When this register value is 0x00, no comparison or matching is made with the 8-bit upcounter value, and the PPG start signal is not asserted.*
- *Writing of this register is prohibited during operation of the 8-bit upcounter.*

5.5 PPG Start Register 0 (TRG0)

The TRG0 register is a PPG start register that directly starts PPG0 to PPG15.

Register configuration

bit	15	14	13	12	11	10	9	8
Field	PEN15	PEN14	PEN13	PEN12	PEN11	PEN10	PEN09	PEN08
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Field	PEN07	PEN06	PEN05	PEN04	PEN03	PEN02	PEN01	PEN00
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Register functions

[bit15:0] PEN15 to PEN00: PPG Start Trigger Register

This is the PPG start register for directly starting each PPG channel. When 1 is written, the PPG start signal is asserted, and the PPG is started. When "0" is written, the PPG start signal is negated, and the PPG is stopped. Simultaneous PPG start and simultaneous PPG stop are possible by simultaneous writing to multiple channels.

bit15:0	Function
0	PPG start signal is negated, and PPG operation is stopped. (Initial value)
1	PPG start signal is asserted, and PPG operation is started.

Notes:

- *The PEN bit number n (n=0, 1, 2, ..., 15) corresponds to the channel number of each PPG.*
- *If PPG start by PEN register is selected by the specified values for the PPGC:TTRG register and GATEC:STRG register, PPG can be started and stopped from the PEN register.*
- *If PPG start by PEN register is not selected, the PEN register value is ignored. See Table 3-2.*
- *For operation modes that use multiple PPG channels (8+8-bit, 16-bit, and 16+16-bit) and the start method of writing the PPG start register (TRG:PEN), 1 is written simultaneously to the TRG:PEN registers of all channels being used to start the PPG. Also, 0 is written simultaneously to the TRG:PEN registers to stop the PPG. The count cycle may be shifted if values are not written simultaneously.*

5.6 PPG Start Register 1 (TRG1)

The TRG1 register is a PPG start register that directly starts PPG16 to PPG23.

Register configuration

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute					-			
Initial value					-			

bit	7	6	5	4	3	2	1	0
Field	PEN23	PEN22	PEN21	PEN20	PEN19	PEN18	PEN17	PEN16
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Register functions

[bit7:0] PEN23 to PEN16: PPG Start Trigger Register

This is the PPG start register for directly starting each PPG channel. When 1 is written, the PPG start signal is asserted, and the PPG is started. When 0 is written, the PPG start signal is negated, and the PPG is stopped. Simultaneous PPG start and simultaneous PPG stop are possible by simultaneous writing to multiple channels.

bit7:0	Function
0	PPG start signal is negated, and PPG operation is stopped. (Initial value)
1	PPG start signal is asserted, and PPG operation is started.

Note:

- *The PEN bit number n (n=16, 17, ..., 23) corresponds to the channel number of each PPG. See the notes in "PPG start register 0 (TRG0)". These notes also apply to the TRG1 register in the same way.*

5.7 Output Reverse Register 0 (REVC0)

The REVC0 register sets an output polarity of PPG0 to PPG15 output signal.

Register configuration

bit	15	14	13	12	11	10	9	8
Field	REV15	REV14	REV13	REV12	REV11	REV10	REV09	REV08
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Field	REV07	REV06	REV05	REV04	REV03	REV02	REV01	REV00
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Register functions

[bit15:0] REV15 to REV00: PPG Output Reverse Enable bits

These bits set the polarity of each PPG channel output signal.

bit	Function
0	Normal output (LOW output when PPG is not operating) [Initial value]
1	Reverse the output. (HIGH output when PPG is stopped)

Notes:

- *The REV bit number n (n=0, 1, 2, ..., 15) corresponds to the channel number of each PPG.*
- *The connection diagrams of Figure 3-1, Figure 3-3, Figure 3-4, and Figure 3-5 show configurations where the PPG output is reversed by the REV register value directly. For this reason, when REV=1, the followings are performed.*
  - *The output level before operation start of the PPG output and the output level after operation stop are reversed to the High level.*
  - *The Low-High of the output pulse is reversed, and the relationship of the Low width setting and High width setting of the reload resistor is reversed.*
  - *PUF is set when PPGC:INTM=1 and when the Low pulse ends.*
  - *In 8+8-bit PPG operation mode and 16+16-bit PPG operation mode, the operation clock supplied to the PPG output side from the prescaler side is reversed.*

5.8 Output Reverse Register 1 (REVC1)

The REVC1 register sets an output polarity of PPG16 to PPG23 output signal.

Register configuration

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	-							

Bit	7	6	5	4	3	2	1	0
Field	REV23	REV22	REV21	REV20	REV19	REV18	REV17	REV16
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Register functions

[bit7:0] REV23 to REV16: PPG Output Reverse Enable bits

These bits set the polarity of each PPG channel output signal.

bit	Function
0	Normal output (LOW output when PPG is not operating) [Initial value]
1	Invert the output. (HIGH output when PPG is stopped)

Notes:

- *The REV bit number n (n=16, 17, ..., 23) corresponds to the channel number of each PPG. The (n=16, 17, 18, ..., 23) of the REVn register corresponds to the channel number of each PPG.*
- *See the notes in the "Output reversal register 0 (REVC0)". These notes also apply to the REV1 register in the same way.*

5.9 PPG Operation Mode Control Register n (PPGCn n=0 to 23)

The PPGCn register sets the PPG interrupts, operation mode, clock selection, and other settings.

PPGC Register configuration list

bit 15 8	7 0	Initial Value	Attribute	Correspoding PPG
PPGC0	PPGC1	0x0000	R/W	PPG0, PPG1
PPGC2	PPGC3	0x0000	R/W	PPG2, PPG3
PPGC4	PPGC5	0x0000	R/W	PPG4, PPG5
PPGC6	PPGC7	0x0000	R/W	PPG6, PPG7
PPGC8	PPGC9	0x0000	R/W	PPG8, PPG9
PPGC10	PPGC11	0x0000	R/W	PPG10, PPG11
PPGC12	PPGC13	0x0000	R/W	PPG12, PPG13
PPGC14	PPGC15	0x0000	R/W	PPG14, PPG15
PPGC16	PPGC17	0x0000	R/W	PPG16, PPG17
PPGC18	PPGC19	0x0000	R/W	PPG18, PPG19
PPGC20	PPGC21	0x0000	R/W	PPG20, PPG21
PPGC22	PPGC23	0x0000	R/W	PPG22, PPG23

Notes:

- *The PPGC register number n (n=0, 1, 2, ..., 23) corresponds to the channel number of the PPG being controlled.*
- *This register is located on the upper side (bit[15:8]) when n is even.*
- *This register is located on the lower side (bit[7:0]) when n is odd.*
- *The register configuration is different for the upper side and lower side. There is a control bit that exists only on the even channel side.*

PPGCn register configuration (when n is even)

Bit	15	14	13	12	11	10	9	8
Field	PIE	PUF	INTM	PCS1	PCS0	MD1	MD0	TTRG

PPGCn register configuration (when n is odd)

bit	7	6	5	4	3	2	1	0
Field	PIE	PUF	INTM	PCS1	PCS0	Reserved		

Register functions

[bit15/bit7] PIE: PPG Interrupt Enable bit

This bit is used to select enable/disable for PPG interrupts. When interrupt enable is set, PUF can be used to assert the interrupt signal. As shown in the connection diagrams in Figure 3-1, Figure 3-3, Figure 3-4, and Figure 3-5, the interrupt output signal is the logical AND signal of the PUF value and PIE value.

bit	Function
Writing 0	Disables an interrupt. [Initial value]
Writing 1	Enables an interrupt.
Reading	Reading setting value

[bit14/bit6] PUF: PPG Counter Underflow bit

This bit is used to notify the CPU when a PPG output pulse change event occurs. It is set to 1 by the underflow of the PPG counter. It can be cleared by setting to 0 from the CPU.

bit	Function
Reading 0	No underflow of PPG Counter has been detected. [Initial value]
Reading 1	An underflow of PPG Counter has been detected.
Writing 0	Clears the PUF flag.
Writing 1	No effect on the operation

The PPG counter changes the output pulse when the down-count for the specified pulse width value ends and an underflow occurs. PUF is set to 1 by this counter underflow. PUF is an event register that notifies the CPU when an output pulse change event occurs. The selection below is performed by setting PPGCn:INTM.

- When PPGCn:INTM=0, the settings are made by the underflow when the Low pulse width count is ended and by the underflow when the High pulse width count is ended.
- When PPGCn:INTM=1, the setting is made by the underflow when the High pulse width count is ended.

If the PPG channels are connected and operated at a length of 16 bits, the PUFs for both the even and odd channels are set simultaneously.

The PUF that is set from the PPG can be cleared by writing 0 from the CPU to the PUF. Once a PUF is set, it is not cleared from the PPG. To enable the CPU to recognize an output pulse change event, the PUF must be cleared from the CPU whenever the PUF is set.

The PUF is cleared by writing 0. As a result, if writing access to the PPGCn register is performed without clearing the PUF, write 1 to the PUF. When reading during read modify write access, 1 is read regardless of the PUF value.

[bit13/bit5] INTM: Interrupt Mode Select bit

This bit sets the interrupt mode.

bit	Function
Writing 0	The PUF bit is set to 1 at the underflow when the Low pulse width count is ended and at underflow when the High pulse width count is ended. (Initial value)
Writing 1	The PUF bit is set to 1 at the underflow when the High pulse width count is ended.
Reading	Reading setting value

[bit12:11/bit4:3] PCS1, PCS0: PPG DOWN Counter Operation Clock Select bits

These bits set an operation clock of PPG's DOWN counter.

See the "Count clock selection".

bit12	bit11	Function
0	0	PCLK [Initial value]
0	1	PCLK/4
1	0	PCLK/16
1	1	PCLK/64

[bit10:9] MD1, MD0: PPG Operation Mode Set bits

These bits set the PPG operation mode.

These bits are found in even channels (n=0, 2, 4, ..., 22) only. By setting these bits, the operation modes for both the PPG even channels (n) and odd channels (n+1) are specified.

When 16+16-bit PPG operation mode is set, 4 channels are used. The PPGCm:MD1,MD0 = PPGCm+2:MD1,MD = 11 (m=0, 4, 8, 12, 16, 20) setting is performed.

See Selecting the PPG operation mode.

bit10	bit9	Function
0	0	Both even channels (n) and odd channels (n+1) are set to 8-bit PPG operation mode. (Initial value)
0	1	This sets to 8+8-bit PPG operation mode. Even channels (n) are set to the 8-bit PPG output side. Odd channels (n+1) are set to the 8-bit prescaler side.
1	0	The even (n) and odd (n+1) channels are connected and set to 16-bit PPG operation mode.
1	1	This sets to 16+16-bit PPG operation mode. This connects PPGm and PPGm+1 and sets to the 16-bit PPG output side. This connects PPGm+2 and PPGm+3 and sets to the 16-bit prescaler side.

[bit8] TTRG: PPG start trigger signal select bit

This bit is used to select the PPG start signal. This bit is found in even channels only. The PPG start signals for both even and odd channels are selected by a combination of this bit setting and the GATECx:STRGn register setting. The available start signals vary depending on the selected PPG operation mode.
See Selecting the PPG start method.

bit	Function
0	Selects start from PPG start register (TRG:PEN) or start by GATE signal from multifunction timer. (Initial value)
1	Selects start signal from timing generator.

[bit2:0] Reserved : Reserved bits

000 is read from these bits.

Set these bits to 000 when writing.

5.10 PPG Reload Registers n (PRLHn, PRLLn n=0 to 23)

The PRLHn and PRLLn registers set the PPG output pulse width.

PRLHn/PRLLn Register configuration list

bit 15 to 8	bit 7 to 0	Initial value	Attribute
PRLH0	PRLL0	0xXXXX	R/W
PRLH1	PRLL1	0xXXXX	R/W
PRLH2	PRLL2	0xXXXX	R/W
PRLH3	PRLL3	0xXXXX	R/W
PRLH4	PRLL4	0xXXXX	R/W
PRLH5	PRLL5	0xXXXX	R/W
PRLH6	PRLL6	0xXXXX	R/W
PRLH7	PRLL7	0xXXXX	R/W
PRLH8	PRLL8	0xXXXX	R/W
PRLH9	PRLL9	0xXXXX	R/W
PRLH10	PRLL10	0xXXXX	R/W
PRLH11	PRLL11	0xXXXX	R/W
PRLH12	PRLL12	0xXXXX	R/W
PRLH13	PRLL13	0xXXXX	R/W
PRLH14	PRLL14	0xXXXX	R/W
PRLH15	PRLL15	0xXXXX	R/W
PRLH16	PRLL16	0xXXXX	R/W
PRLH17	PRLL17	0xXXXX	R/W
PRLH18	PRLL18	0xXXXX	R/W
PRLH19	PRLL19	0xXXXX	R/W
PRLH20	PRLL20	0xXXXX	R/W
PRLH21	PRLL21	0xXXXX	R/W
PRLH22	PRLL22	0xXXXX	R/W
PRLH23	PRLL23	0xXXXX	R/W

Register configuration

bit	15 to 8	7 to 0
Field	PRLHn	PRLLn
Attribute	R/W	R/W
Initial value	0xXX	0xXX

Register functions

[bit15:8] PRLH: PPG Reload Register HIGH Set bits

These bits specify the PPG pulse width.

bit	Function
During writing	Any value can be written.
During reading	The register value is read. The initial value is undefined.

[bit7:0] PRLL: PPG Reload Register LOW Set bits

These bits specify the PPG pulse width.

bit	Function
During writing	Any value can be written.
During reading	The register value is read. The initial value is undefined.

This register specifies the width of the PPG output pulse. The pulse width can be changed during PPG operation. Both the High width and Low width are specified. The pulse width that is output is found by multiplying the count clock cycle by the written value with +1 added. If the PPG channels are connected to make a 16-bit length, the reload registers are also connected to specify a value that is 16 bits in length. When High width is set, the buffer register function is enabled. See Specifying the reload register and pulse width and Buffer function of high width setting reload register.

The setting content is determined uniquely by the PPG operation mode. The channel number 0 to 3 settings are shown below. The settings for channel numbers 4 and higher use the same combinations.

8-bit operation mode combination

PRLH0	PRLL0
The high width(8bit) of PPG0	The low width(8bit) of PPG0
PRLH1	PRLL1
The high width(8bit) of PPG1.	The low width(8bit) of PPG1
PRLH2	PRLL2
The high width(8bit) of PPG2	The low width(8bit) of PPG2
PRLH3	PRLL3
The high width(8bit) of PPG3	The low width(8bit) of PPG3

8+8-bit operation mode combination

PRLH0	PRLL0
The high width(8bit) of PPG0(PPG output side)	The low width(8bit) of PPG0(PPG output side)
PRLH1	PRLL1
The high width(8bit) of PPG1(prescaler side)	The low width(8bit) of PPG1(prescaler side)
PRLH2	PRLL2
The high width(8bit) of PPG2(PPG output side)	The low width(8bit) of PPG2(PPG output side)
PRLH3	PRLL3
The high width(8bit) of PPG3(prescaler side)	The low width(8bit) of PPG2(prescaler side)

16-bit operation mode combination

PRLH0	PRLL0
The high width(16bit) of PPG0/PPG1	
PRLH1	PRLL1
The low width(16bit) of PPG0/PPG1	
PRLH2	PRLL2
The high width(16bit) of PPG2/PPG3	
PRLH3	PRLL3
The low width(16bit) of PPG2/PPG3	

16+16-bit operation mode combination

PRLH0	PRLL0

The high width(16bit) of PPG0/PPG1(PPG output side)

PRLH1	PRLL1

The low width(16bit) of PPG0/PPG1(PPG output side)

PRLH2	PRLL2

The high width(16bit) of PPG2/PPG3 (prescaler side)

PRLH3	PRLL3

The low width(16bit) of PPG2/PPG3 (prescaler side)

5.11 Gate Function Control Registers n (GATEC0/GATEC4/GATEC8/GATEC12/GATEC16/ GATEC20)

The GATEC registers specify the start of the PPG using a GATE signal sent from the multifunction timer.

GATEC Register configuration list

bit 15 8	7 0	Initial value	Attribute	Corresponding PPG
Reserved	GATEC0	0x00	R/W	PPG2, PPG0
Reserved	GATEC4	0x00	R/W	PPG6, PPG4
Reserved	GATEC8	0x00	R/W	PPG10, PPG8
Reserved	GATEC12	0x00	R/W	PPG14, PPG12
Reserved	GATEC16	0x00	R/W	PPG18, PPG16
Reserved	GATEC20	0x00	R/W	PPG22, PPG20

GATECn Register configuration (n=0, 4, 8, 12, 16 or 20)

bit	7	6	5	4	3	2	1	0
Field	Reserved		STRGn+2	EDGEn+2	Reserved		STRGn	EDGEn
Attribute	-		R/W	R/W	-		R/W	R/W
Initial value	-		0	0	-		0	0

Register functions

[bit7:6] Reserved: Reserved bits

00 is read from these bits.

Set these bits to 00 when writing.

[bit5] STRGn+2: Select trigger bit n+2 (n=0, 4, 8, 12, 16 or 20)

This bit is used to select the PPG start signal. The start signals for both PPGn+3 and PPGn+2 are selected by a combination of this bit and the PPGCn+2:TTRG: register. See Selecting the PPG start method.

bit	Function
0	Selects start from PPG start register (TRGx:PEN). (Initial value)
1	Selects start from GATE signal from multifunction timer.

[bit4] EDGEn+2: Start Effective Level Select bit "n+2" (where, n=0, 4, 8, 12, 16 or 20)

This register is used by writing 0. A value of 0 is read.

[bit3:2] Reserved: Reserved bits

00 is read from these bits.

Set these bits to 00 when writing.

[bit1] STRGn: Select trigger bit "n" (where, n=0, 4, 8, 12, 16 or 20)

This bit is used to select the PPG start signal. The start signals for both PPGn+1 and PPGn are selected by a combination of this bit and the PPGCn:TTRG: register. See "Selecting the PPG start method".

bit	Function
0	Selects start from PPG start register (TRGx:PEN). (Initial value)
1	Selects start from GATE signal from multifunction timer.

[bit0] EDGEn: Start Effective Level Select bit "n" (where, n=0, 4, 8, 12, 16 or 20)

This register is used by writing 0. A value of 0 is read.

6. Notes on using PPG

This section gives detail about using the PPG.

PPG Output Operations

When the PPG is operating, the pulse output waveform of LOW level period and HIGH level period are continuously output.
Once the pulse output has started, the PPG does not stop the output until PPG operation is stopped.

A reset signal must be entered or the PPG stop setting must be set to stop the operation.
The following explains PPG stop conditions.

- Start triggered by the Timing Generator Circuit

  Start signal is negated by writing PPGC:TRGxO=0

- Start triggered by GATE signal from the multifunction timer

  GATE signal from multifunction timer is negated

- Start triggered by PPG start register (TRG) writing

  Start signal is negated by writing TRG:PEN=0

PPG Operation Mode Setting

The PPG operation mode is determined by setting the MD[1:0] bit of each PPGC register.
Be sure to always select the PPG operation mode before starting PPG.

Other Module Settings

PPG pulses are output via the I/O port of the multifunction timer. The multifunction timer settings are explained in Chapter Multifunction Timer. For details on waveform output to I/O ports, see Chapter I/O Ports in the Peripheral Manual. Also, for details on interrupts, see Chapter Interrupts in the Peripheral Manual.

PPG Output Signal and Interrupt Signal

Among the PPG output signals obtained by PPG timer operation, some channel outputs can be output to external terminals by passing through a multifunction timer. Also, some PPG interrupt outputs can be connected to interrupt controllers for performing interrupt processes.

See the chapter "PPG configuration" for details on the PPG output terminals that are output to external terminals by passing through a multifunction timer and PPG interrupts connected to interrupt controllers.

CHAPTER 8-1: Quadrature Position/Revolution Counter

This chapter explains the functions and operations of the Quadrature Position/Revolution Counter (QPRC).

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1. Overview
2. Configuration
3. Operations
4. Registers

1. Overview

The Quadrature Position/Revolution Counter is used to measure the position of the Position Encoder. Also, it can be used as an up/down counter depending on the setting. The Quadrature Position/Revolution Counter contains a 16-bit position counter, a 16-bit revolution counter, two 16-bit compare registers, a control register, and its control circuit.

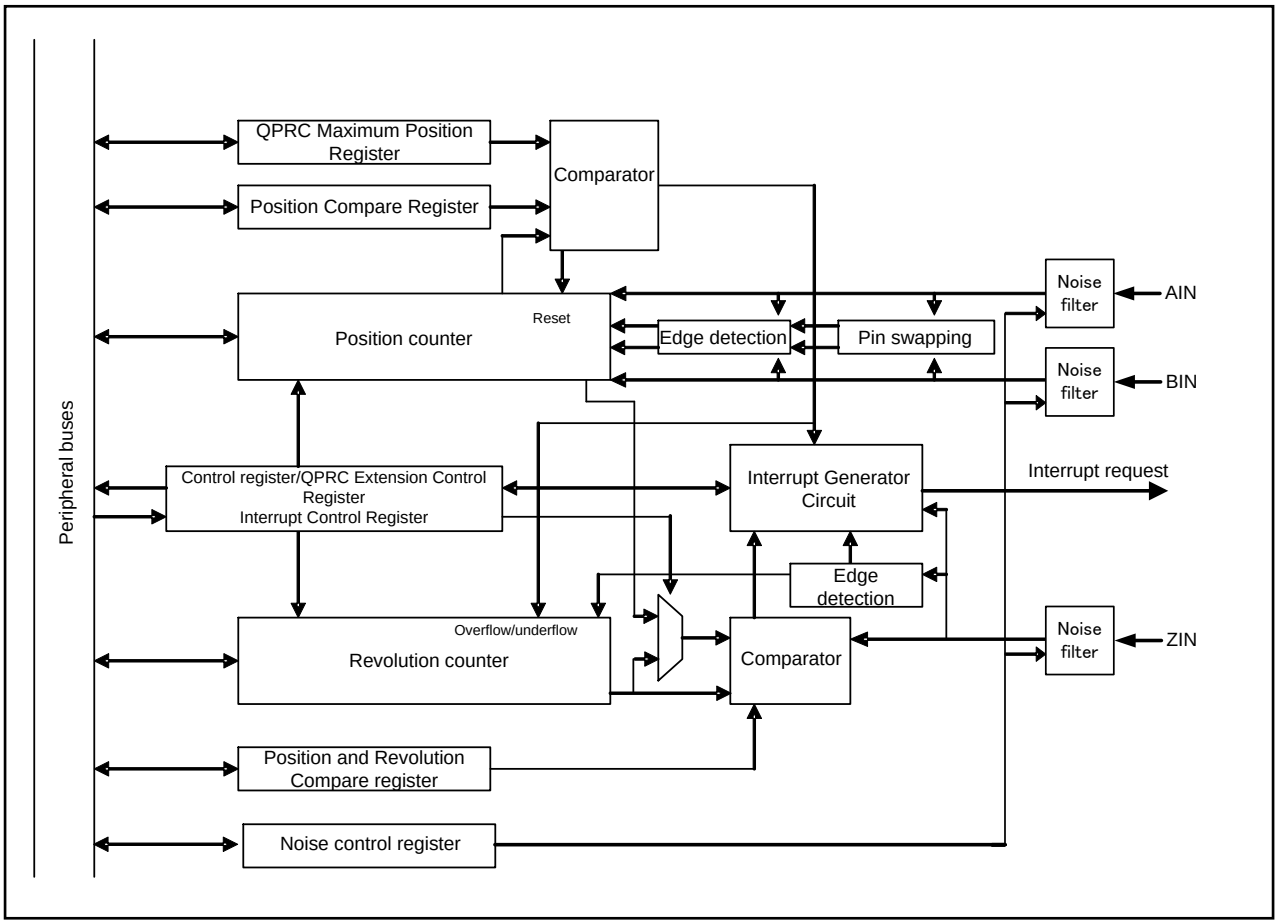
Features of Quadrature Position/Revolution Counter

- The position counter can be operated in one of the following three counting modes:
  - PC_Mode1: Up/down count mode
  - PC_Mode2: Phase difference count mode (supporting the 1-time, 2-time and 4-time frequency multiplication)
  - PC_Mode3: Count mode with direction
- The revolution counter can be operated in one of the following three counting modes:
  - RC_Mode1: The revolution counter can count up or down at a ZIN active edge only.
  - RC_Mode2: The revolution counter can count up or down with an output value of position counter only.
  - RC_Mode3: The revolution counter can count up or down both with an output value of position counter and a signal at a ZIN active edge.
- A signal edge detection can be set for detecting an input event from three AIN, BIN, and ZIN external pins
  - Detection of falling edge
  - Detection of rising edge
  - Detection of both rising and falling edges
- Noise filter for three external pins (AIN, BIN and ZIN)
  - Noise removal width setting available (Maximum: 256 cycles of PCLK)
  - Input reversing function
  - Input masking function
- The following two functions can be selected for input in the ZIN pin
  - Counter clear function
  - Gate function
- An interrupt request can be generated if:
  - The position counter value matches the Position Compare register,
  - The position counter value matches the Position and Revolution Compare register value, or the revolution counter value matches the Position and Revolution Compare register value,
  - The position counter underflows,
  - The position counter overflows (that is, the position counter value matches the value of the QPRC Maximum Position register),
  - The position counter is reset at a ZIN active edge,
  - The counting of position counter is inverted,
  - The position counter matches the Position Compare register value, and the revolution counter matches the Position and Revolution Compare register value, or
  - An outrange revolution counter value is detected.
- The following useful functions are provided for counting
  - Swap function of AIN and BIN external pins
  - Mask reset function of the position counter
  - Count direction check function during position counter operation or during overflow/underflow occurrence

2. Configuration

The following shows the configuration of Quadrature Position/Revolution Counter.

Figure 2-1 Block Diagram of Quadrature Position/Revolution Counter



3. Operations

This section explains the operation of Quadrature Position/Revolution Counter.

Operation of Position Counter

The position counter receives an input signal from AIN or BIN external pin as an event of count clock, and increments or decrements the counter. As listed in Table 3-1, the position counter can select a counting mode by setting of the position counter mode bits (QCR:PCM[1:0]) of a control register. The counting conditions depend on the selected count mode.

The position counter is counted up or down in the following ZIN conditions only.

- If the ZIN function is set to the count clear function (QCR:CGSC=0)
- If the ZIN function is set to the Gate function (QCR:CGSC=1), the ZIN low-level detection (QCR:CGE[1:0]=01) is set, and the ZIN is low level
- If the ZIN function is set to the Gate function (QCR:CGSC=1), the ZIN high-level detection (QCR:CGE[1:0]=10) is set, and the ZIN is high level

If the ZIN function is set to the Gate function (QCR:CGSC=1) and if a level other than ZIN high- or low-level detection (QCR:CGE[1:0]=00 or 11) is set, the position counter is not counted up or down.

Also, if the AIN and BIN configurations are swapped by SWAP bits of a control register, the AIN and BIN pins are swapped and the position counter is counted up or down.
For example, if PC_Mode1 (QCR:PCM[1:0]=01) and AES[1:0]=10 (rising edge) and BES[1:0]=01 (falling edge) are set, the following occurs.

- If QCR:SWAP=0 and when a rising edge of AIN signal is detected, the position counter is counted up. When a falling edge of BIN signal is detected, the position counter is counted down.
- If QCR.SWAP=1, the position counter is counted down at a falling edge of AIN signal but it is counted up at a rising edge of BIN signal.

Table 3-1 Counting Conditions of AIN and BIN Pin Position Counter

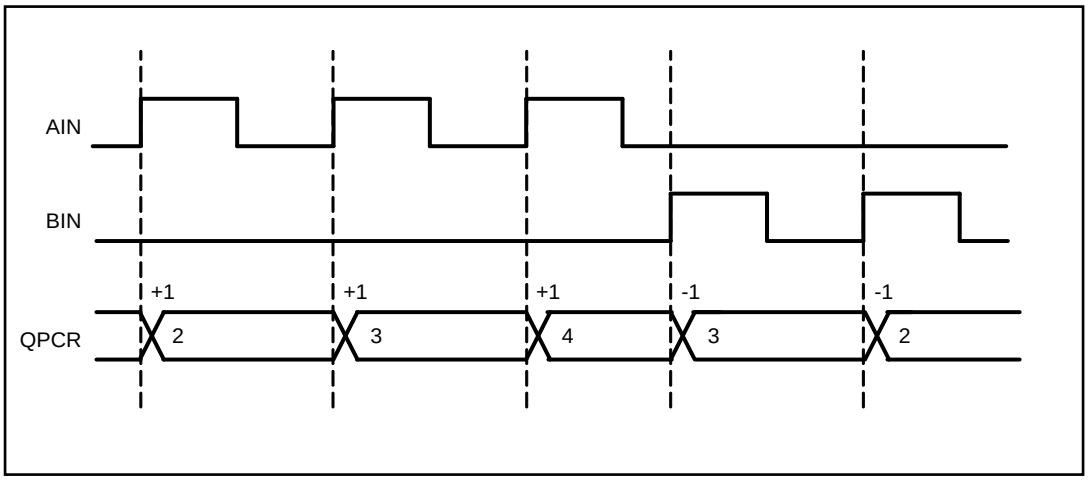
Position Count Mode (PC_MODE)	AIN Counting Conditions	BIN Counting Conditions
Count disable PC_Mode0:QCR:PCM[1:0]=00	Position counter disable	Position counter disable
Up/down counting PC_Mode1: QCR:PCM[1:0]=01	AIN Active edge	BIN Active edge
Phase difference count PC_Mode2:QCR:PCM[1:0]=10	AIN Active edge or high/low level	High/low level or BIN active edge
Counting with direction PC_Mode3:QCR:PCM[1:0]=11	High/low level	BIN Active edge

Note:

- *The active edge of AIN signal and the active edge of BIN signal mean a rising edge, a falling edge, or both of edges set by the AIN Detection Edge Select bits (QCR:AES[1:0]=01 or 10 or 11) or by the BIN Detection Edge Select bits (QCR:BES[1:0]=01 or 10 or 11).*

- PC_Mode1: Up/down count mode
  - An external signal entered from AIN or BIN external pin is received as the counting clock, and the position counter is counted up or down.
  - In this mode, the position counter is counted up when an active edge of AIN signal is detected. When an active edge of BIN signal is detected, the position counter is counted down.

Figure 3-1 Operations in Up/down Count Mode (QCR:AES[1:0]=10, QCR:BES[1:0]=10, QCR:SWAP=0)



- PC_Mode2: Phase difference count mode (supporting the 1-time, 2-time and 4-time frequency multiplication)
  - This mode is useful for counting the difference between phases A and B of encoder output signal. If the phase-A and phase-B outputs are respectively connected to the AIN and BIN pins and if phase A is leading phase B, the counter is counted up. If delayed, the counter is counted down.
  - In this mode, when an active edge of AIN signal is detected, the BIN signal level is checked and the position counter counts it. In the opposite case, the position counter also counts it.
  - Counting in the 4-time or 2-time frequency multiplication can be made by setting the AES and BES bits of QPRC Control register (QCR). The counting in these frequency multiplication modes allows more accurate position measurement as its counting resolution is very high.
  - A behavior of 1-time frequency multiplication is different by TYPE. TYPE3-M4, TYPE4-M4, TYPE5-M4 can be selected both edge count for 1-time frequency multiplication phase difference count mode by setting of PEC bit.

Table 3-2 AES and BES Bit Settings in Frequency Multiplication Mode

Frequency Multiplication Mode	AES[1:0] Setting	BES[1:0] Setting
1-time frequency multiplication mode	01	00
	10	00
	00	01
	00	10
2-time frequency multiplication mode	11	00
	00	11
4-time frequency multiplication mode	11	11

Table 3-3 Counting in 1-time Frequency Multiplication Phase Difference Count Mode(Rise Edge)
(TYPE1-M4, TYPE2-M4, TYPE6-M4 : QCR:AES[1:0]=10, QCR:BES[1:0]=00, QCR:SWAP=0)
(TYPE3-M4, TYPE4-M4, TYPE5-M4: QECR:PEC=0, QCR:AES[1:0]=10, QCR:BES[1:0]=00, QCR:SWAP=0)

Edge Detection Pin	Detection Edge	Level Check Pin	Input Level	Counting Direction	Figure 3-2Figure 3-4 Timing
AIN	Rising edge	BIN	Low	Up	(1)
	Rising edge		High	Down	(2)
	Falling edge		Low	Keep	(3)
	Falling edge		High	Keep	(4)

Figure 3-2 Counting in 1-time Frequency Multiplication Phase Difference Count Mode(Rise Edge)
(TYPE1-M4, TYPE2-M4, TYPE6-M4: QCR:AES[1:0]=10, QCR:BES[1:0]=00, QCR:SWAP=0)
(TYPE3-M4, TYPE4-M4, TYPE5-M4: QECR:PEC=0, QCR:AES[1:0]=10, QCR:BES[1:0]=00, QCR:SWAP=0)

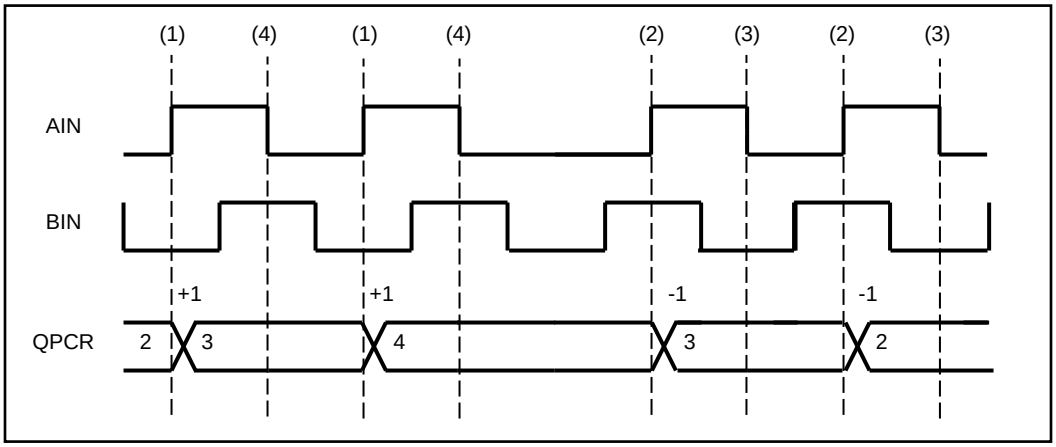


Table 3-4 Counting in 1-time Frequency Multiplication Phase Difference Count Mode(Both Edge)
(TYPE3-M4, TYPE4-M4, TYPE5-M4: QECR:PEC=1, QCR:AES[1:0]=10, QCR:BES[1:0]=00, QCR:SWAP=0)

Edge Detection Pin	Detection Edge	Level Check Pin	Input Level	Counting Direction	Figure 3-3 Timing
AIN	Rising edge	BIN	Low	Up	(1)
	Rising edge		High	Keep	(2)
	Falling edge		Low	Down	(3)
	Falling edge		High	Keep	(4)

Figure 3-3 Counting in 1-time Frequency Multiplication Phase Difference Count Mode(Both Edge)
(TYPE3-M4, TYPE4-M4, TYPE5-M4: QECR:PEC=1, QCR:AES[1:0]=10, QCR:BES[1:0]=00, QCR:SWAP=0)

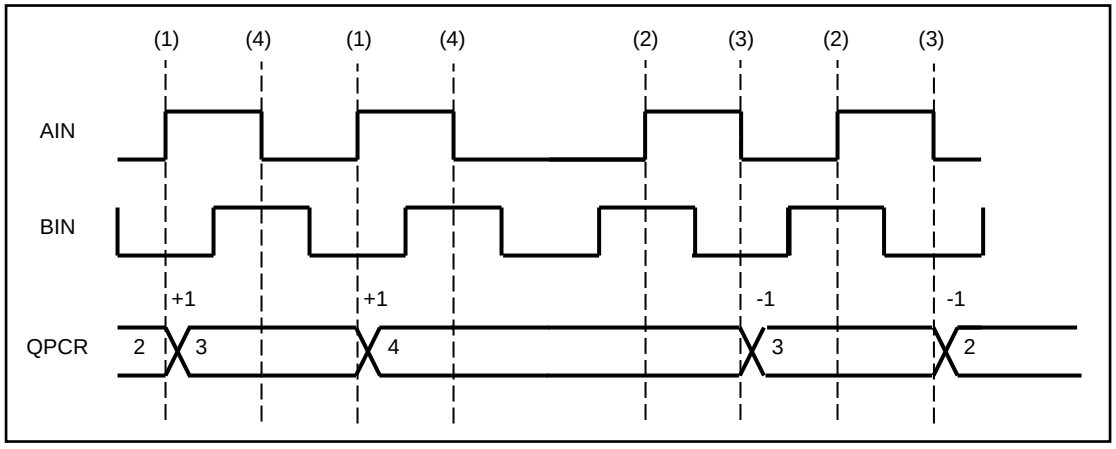


Table 3-5 Counting in 2-time Frequency Multiplication Phase Difference Count Mode (QCR:AES[1:0]=00, QCR:BES[1:0]=11, QCR:SWAP=0)

Edge Detection Pin	Detection Edge	Level Check Pin	Input Level	Counting Direction	Figure 3-4 Timing
BIN	Rising edge	AIN	High	Up	(1)
	Rising edge		Low	Down	(2)
	Falling edge		High	Down	(3)
	Falling edge		Low	Up	(4)

Figure 3-4 Operation in 2-time Frequency Multiplication Phase Difference Count Mode (QCR:AES[1:0]=00, QCR:BES[1:0]=11, QCR:SWAP=0)

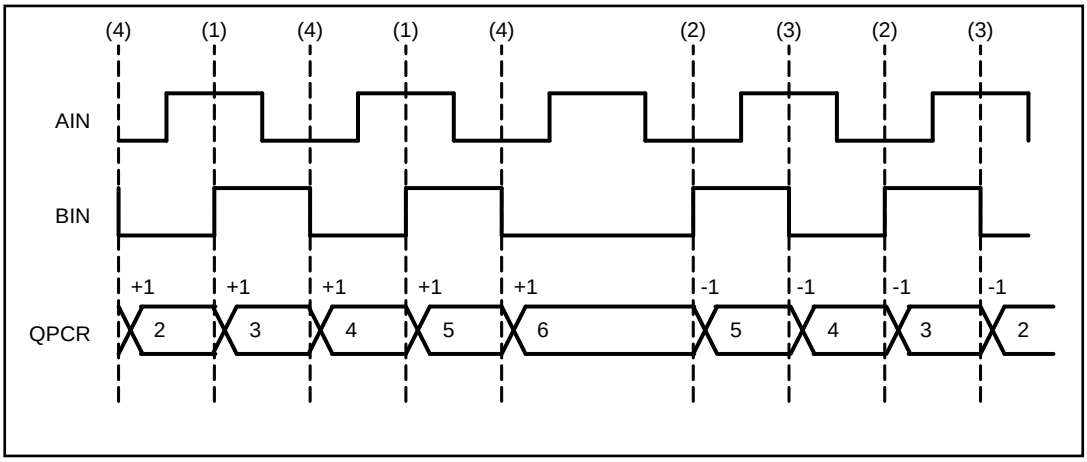
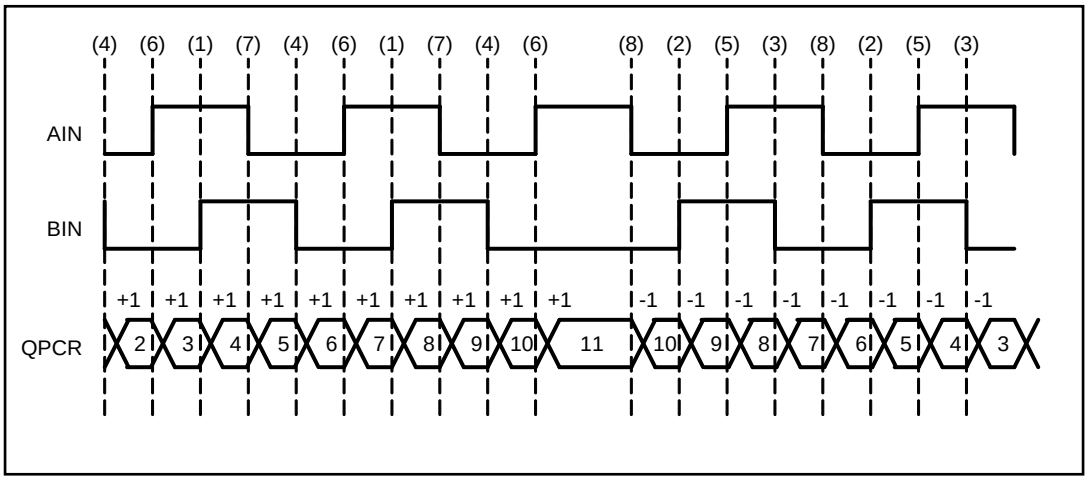


Table 3-6 Counting in 4-time Frequency Multiplication Phase Difference Count Mode (QCR:AES[1:0]=11, QCR:BES[1:0]=11)

Edge Detection Pin	Detection Edge	Level Check Pin	Input Level	Counting Direction	Figure 3-5 Timing
BIN	Rising edge	AIN	High	Up	(1)
	Rising edge		Low	Down	(2)
	Falling edge		High	Down	(3)
	Falling edge		Low	Up	(4)
AIN	Rising edge	BIN	High	Down	(5)
	Rising edge		Low	Up	(6)
	Falling edge		High	Up	(7)
	Falling edge		Low	Down	(8)

Figure 3-5 Operation in 4-time Frequency Multiplication Phase Difference Count Mode (QCR:AES[1:0]=11, QCR:BES[1:0]=11, QCR:SWAP=0)

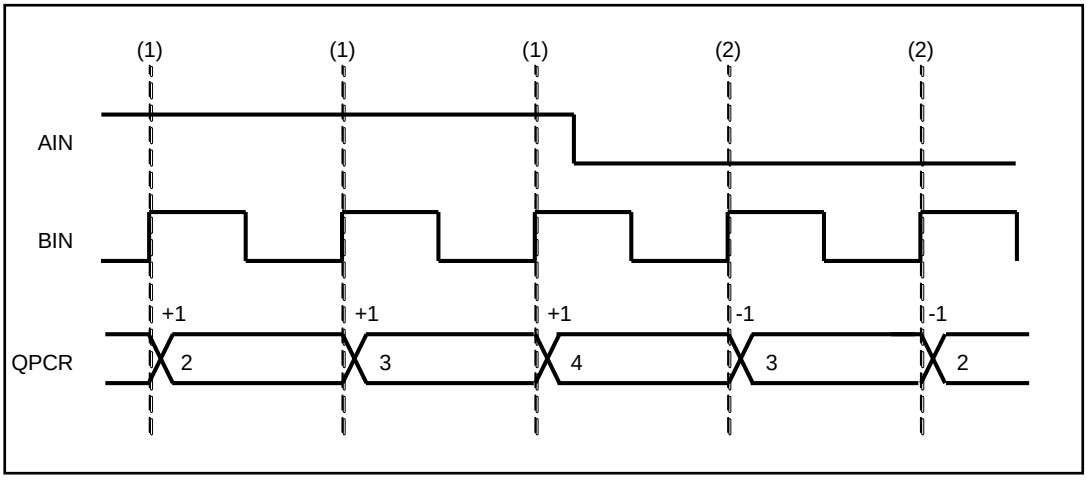


- PC_Mode3: Count mode with direction
  - A signal entered from the BIN external pin is received as the counting clock, and an input level of the signal entered form the AIN external pin is used for count direction control for counter up/down counting.
  - In this mode, when an active edge of BIN signal is detected, the AIN signal level is checked and the position counter counted up or down. A rising edge, a falling edge, or both can be set as the active edge.

Table 3-7 Counting in the Direction Control Counting Mode

Edge Detection Pin	Detection Edge	Level Check Pin	Input Level	Counting Direction	Figure 3-6 Timing
BIN	Active edge	AIN	High	Up	(1)
	Active edge		Low	Down	(2)

Figure 3-6 Operation in the Direction Control Counting Mode (QCR:AES[1:0]=00, QCR:BES[1:0]=10, QCR:SWAP=0)



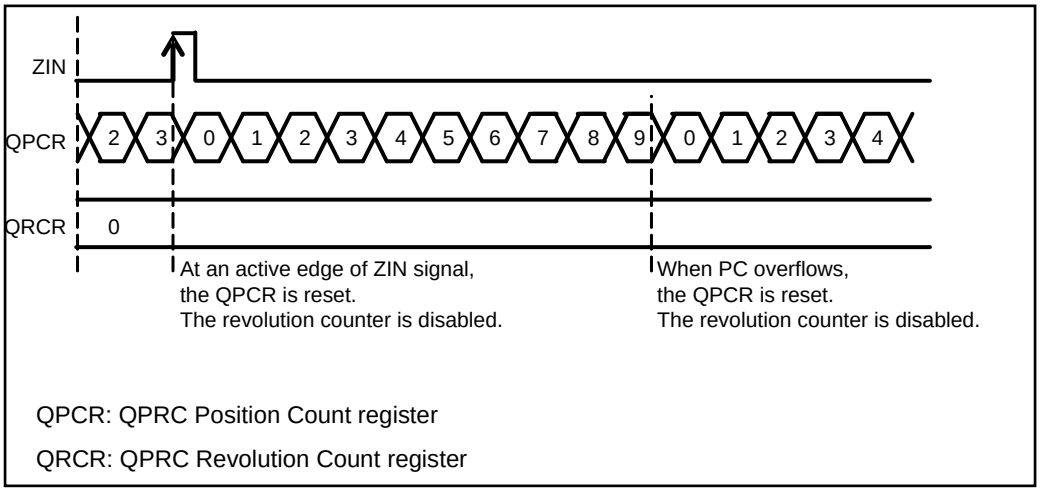
Operation of Revolution Counter

When the revolution counter receives an input from the ZIN pin (having the counter clear function) or an output of position counter (underflow or overflow), it is counted up or down. A rising edge, a falling edge, or both can be set as the active edge of ZIN signal.

The counting conditions of revolution counter depend on the selected mode as follows.

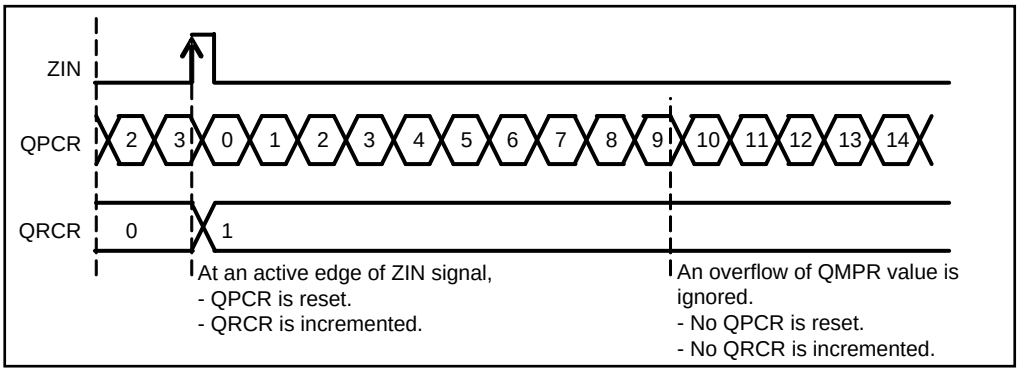
- RC_Mode0 (QCR:RCM[1:0]=00)
  - The revolution counter is disabled.
  - When the ZIN signal is used for counter clear function (QCR:CGSC=0), the active edge of ZIN signal is reset. Also, the position counter is reset when this counter overflows.

Figure 3-7 RC_Mode0 Operation (QPRC Maximum Position Register QMPR=9, QCR:CGSC=0)



- RC_Mode1 (QCR:RCM[1:0]=01)
  - When ZIN signal is used for the counter clear function (QCR:CGSC=0), the revolution counter is operated only at an active edge of ZIN signal (but an input from the position counter is ignored).
  - When an active edge of ZIN signal is detected during incrementing of position counter (QICR:DIRPC=0), the revolution counter is counted up. When an active edge of ZIN is detected during decrementing of position counter (QICR:DIRPC=1), it is counted down.
  - When the ZIN signal is used for counter clear function (QCR:CGSC=0), the position counter is reset only at an active edge of ZIN signal.
  - The position counter is not reset even when an overflow of position counter is detected. When an overflow of position counter is detected, the position counter is counted up and the overflow flag (QICR:OFDF) is set to 1.

Figure 3-8 RC_Mode1 Operation (QPRC Maximum Position Register QMPR=9, QCR:CGSC=0)



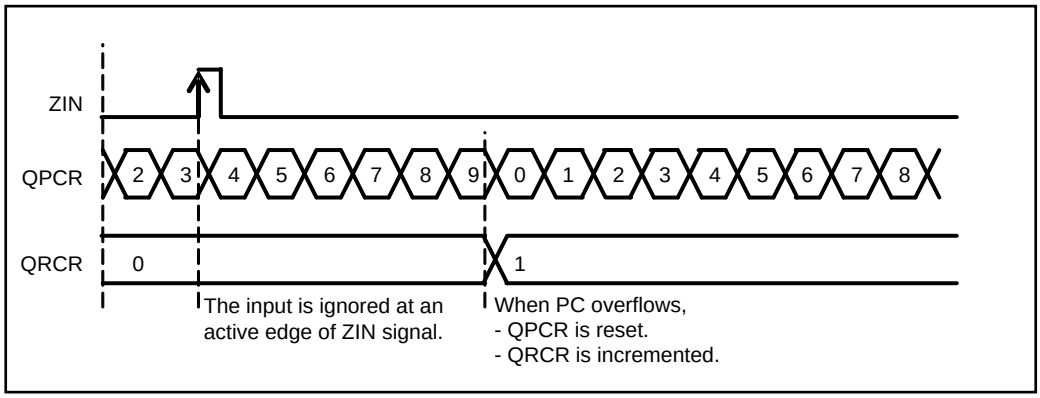
Notes:

- *When an active edge of a ZIN signal and an active edge that counts down the position counter are detected at the same time during incrementing of the position counter (QICR:DIRPC=0), the revolution counter is counted down.*
- *When an active edge of a ZIN signal and an active edge that counts up the position counter are detected at the same time during decrementing of the position counter (QICR:DIRPC=1), the revolution counter is counted up.*
- *When an active edge of a ZIN signal, an active edge of an AIN signal, and an active edge of a BIN signal are detected at the same time, the revolution counter is counted up or down in accordance with the last position counter direction bit (QICR:DIRPC).*

■ RC_Mode2 (QCR:RCM[1:0]=10)

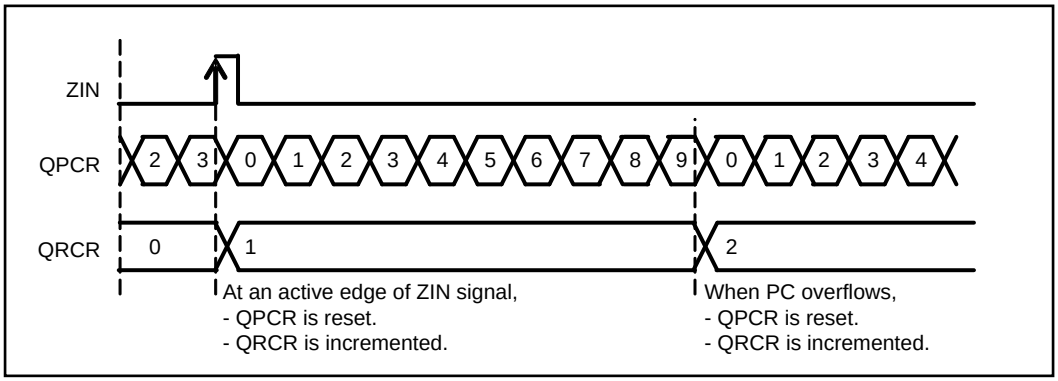
- The revolution counter is counted up or down only by the output value of position counter.
- The position counter is reset only when an overflow of position counter is detected (but an event of a ZIN signal is ignored).
- When an overflow of position counter is detected in any of 3 position counter modes (PC_Mode1, PC_Mode2 and PC_Mode3), the revolution counter is counted up. When an underflow of the position counter is detected, the revolution counter is counted down.

Figure 3-9 RC_Mode2 Operation (QPRC Maximum Position Register QMPR=9)



- RC_Mode3 (QCR:RCM[1:0]=11)
  - *In this mode, the revolution counter is counted up or down with an output value from the position counter or at an active edge of a ZIN when the ZIN is used as the counter clear function (QCR:CGSC=0).*
  - *When an active edge of a ZIN signal is detected during incrementing of position counter (QICR:DIRPC=0) or when an overflow of the position counter is detected, the revolution counter is counted up.*
  - *When an active edge of a ZIN signal is detected during decrementing of position counter (QICR:DIRPC=1) or when an underflow of the position counter is detected, the revolution counter is counted down.*
  - *When the ZIN signal is used for the counter clear function (QCR:CGSC=0), the position counter is reset at an active edge of the ZIN signal or at detection of the position counter overflow.*

Figure 3-10 RC_Mode3 Operation (QPRC Maximum Position Register QMPR=9, QCR:CGSC=0)



Notes:

- *When an active edge of a ZIN signal and an active edge that counts down the position counter are detected at the same time during incrementing of the position counter (QICR:DIRPC=0), the revolution counter is counted down.*
- *When an active edge of a ZIN signal and an active edge that counts up the position counter are detected at the same time during decrementing of the position counter (QICR:DIRPC=1), the revolution counter is counted up.*
- *When an active edge of ZIN signal, an active edge of an AIN signal, and an active edge of a BIN signal are detected at the same time, the revolution counter is counted up or down in accordance with the last position counter direction bit (QICR:DIRPC).*

Absolute Value of Positions

In RC_Mode2 and 3 modes (when the revolution counter operates with an output of position counter), each position has the following absolute value.

QPRC Position Count register (QPCR) + QPRC Revolution Count register (QRCR) × (QPRC Maximum Position register (QMPR) +1)

Example: Time measurement

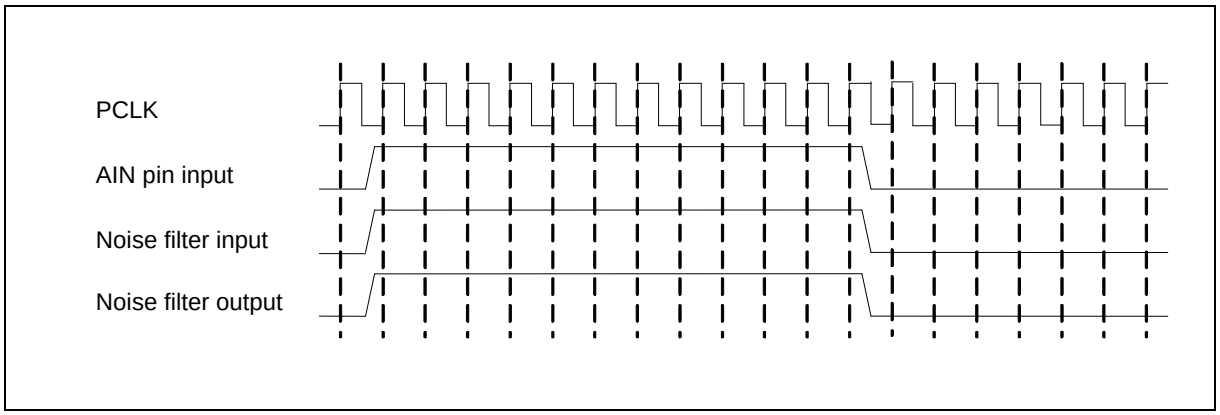
The revolution counter counts the hours, and the position counter counts the minutes.
If QMPR=59, QPCR=20, and QRCR=5

Time = 20 + 5 × (59 + 1)
= 320 minutes. This is the absolute value in position counter units (minutes).

Noise Filter Operation

When the noise filter operates (AINNWS[2:0]!=0b000), the input signal of the AIN pin (for BIN and ZIN pins, the following explanation can be also applied. In that case, AIN should be replaced with BIN or ZIN.) is input to the noise filter after being synchronized with PCLK×2 clock. Figure 3-11 shows the waveform when the noise filter does not operate(AINNWS[2:0]=0b000). The signal from the AIN pin is output to the noise filter output without operation. At this time, AINLV and AINMD functions also become invalid.

Figure 3-11 Noise Filter Operation Explanation (1)



For the example of the noise filter being valid, the operation of the case where the noise filter width is set to four cycle width of a PCLK cycle (AINNWS[2:0]=0b001) is explained. The delay between the AIN pin input and noise filter output is 5 to 6 cycles of PCLK.

If the reversed value of the output value is input to the noise filter input for four cycles or more continuously, the noise filter output is reversed. Figure 3-12 shows that example.

Figure 3-12 Noise Filter Operation Explanation (2)

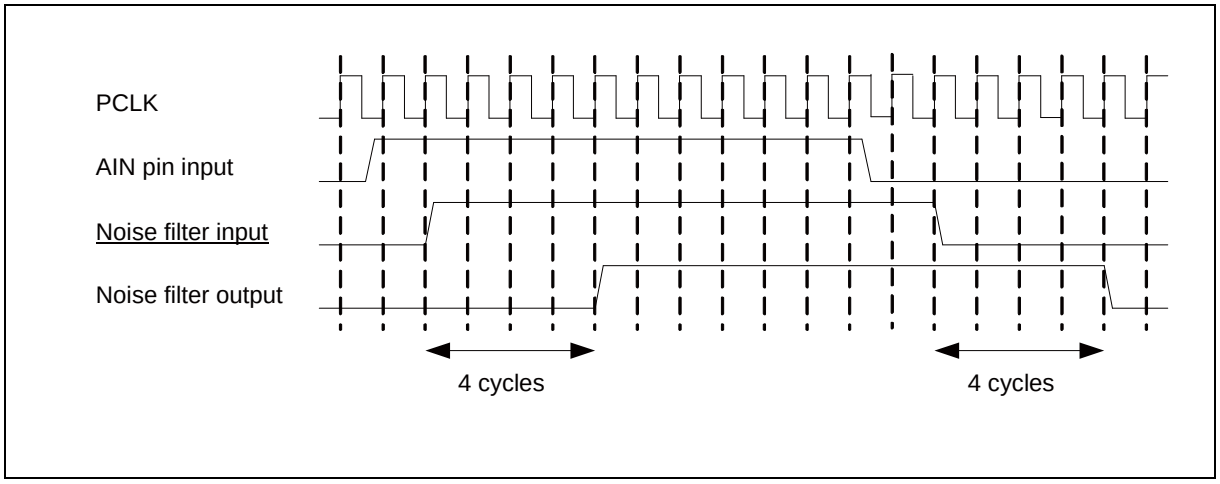
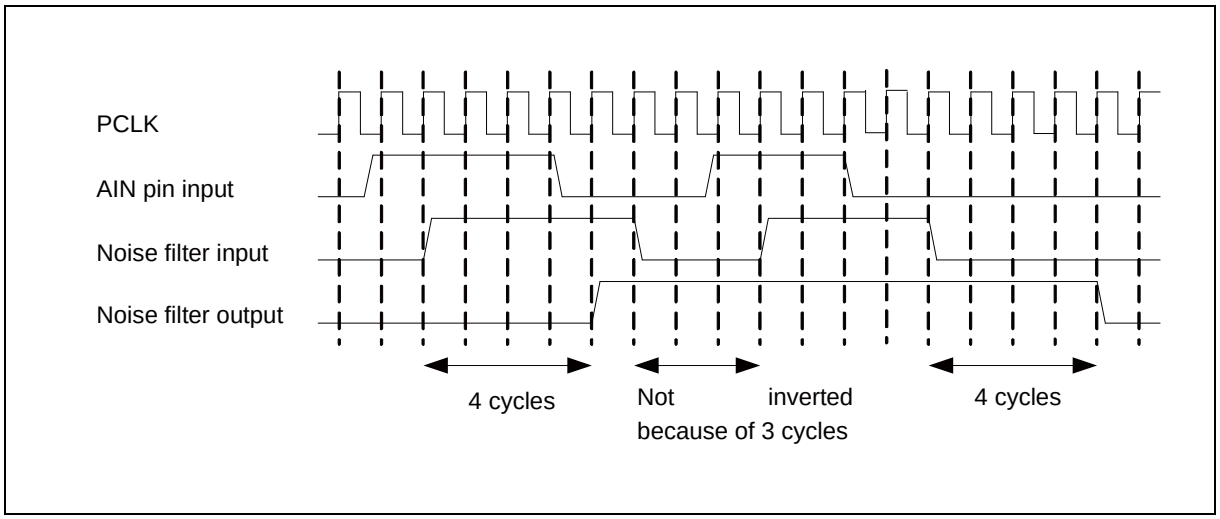


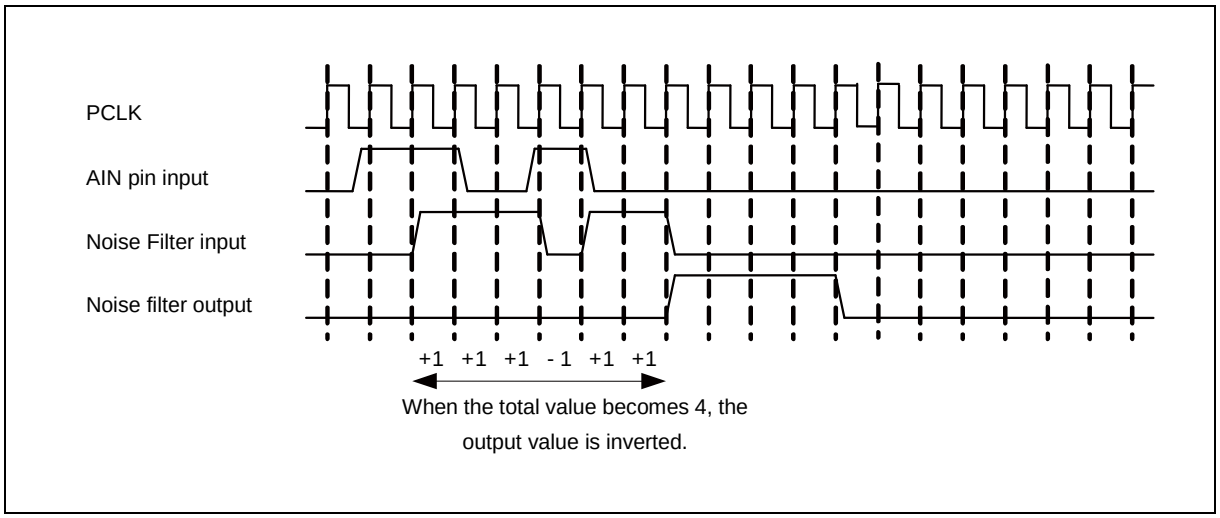
Figure 3-13 shows the waveform when the inversed input value is input for three cycles.

Figure 3-13 Noise Filter Operation Explanation (3)



Decremented by 1 when a value is the inverted input value and decremented by 1 when a value is the same as the input value, the output value is inverted when the total value is 4. Figure 3-14 shows the waveform example.

Figure 3-14 Noise Filter Operation Explanation (4)



For the set values of AINNWS[2:0] and the maximum cycle counts of the delay between AIN and noise filter output, see Table 3-8. The delay includes the input Synchronizer delay of 1 to 2 cycles.

Table 3-8 Register Settings and Delay Cycle Count

AINNWS[2:0]	Delay PCLK Cycle Count
000	0
001	5 to 6
010	9 to 10
011	17 to 18
100	33 to 34
101	65 to 66
110	129 to 130
111	257 to 258

Quadrature Position/Revolution Counter Interrupts

Table 3-9 defines the conditions where an interrupt request of the Quadrature Position/Revolution Counter can generate.

Table 3-9 Generation Conditions of Quadrature Position/Revolution Counter Interrupt Requests

Interrupt Request	Interrupt Request Flag	Interrupt Request is Enabled if	Interrupt Request is Cleared if
Count inversion interrupt request	QICR:CDCF=1	QICR:CDCIE=1	QICR:CDCF is set to 0.
Zero index interrupt request	QICR:ZIIF=1	QICR:OUZIE=1	QICR:ZIIF is set to 0.
Overflow interrupt request	QICR:OFDF=1		QICR:OFDF is set to 0.
Underflow interrupt request	QICR:UFDF=1		QICR:UFDF is set to 0.
PC and RC match interrupt request	QICR:QPRCMF=1	QICR:QPRCMIE=1	QICR:QPRCMF is set to 0.
PC match interrupt request	QICR:QPCMF=1	QICR:QPCMIE=1	QICR:QPCMF is set to 0.
PC match and RC match interrupt request	QICR:QPCNRCMF=1	QICR:QPCNRCMIE=1	QICR:QPCNRCMF is set to 0.
Outrange interrupt request	QECR:ORNGF=1	QICR:ORNGIE=1	QECR:QRNGF is set to 0.

QICR: QPRC Interrupt Control register
QECR: QPRC Extension Control register

Operation Example of the QPRC Maximum Position Register (QMPR) Interrupt

The QPRC Maximum Position register (QMPR) value is used as the reload data to the position counter when an overflow or underflow of the position counter is detected.

When the position counter value matches the QPRC Maximum Position register (QMPR) value, the operation of the revolution counter depends on the selected mode as follows:

- When the position counter is counted up in RC_Mode0 (QCR:RCM[1:0]=00), RC_Mode2 (QCR:RCM[1:0]=10) or RC_Mode3 (QCR:RCM[1:0]=11), the overflow flag (QICR:OFDF) is set to 1 and the position counter is reset.
- When the position counter is counted up in RC_Mode1 (QCR:RCM[1:0]=01), the overflow flag (QICR:OFDF) is set to 1. During this time, the position counter is not reset but is counted up.

The following gives an operation example where the QPRC Maximum Position register (QMPR) is used in RC_Mode2 (QCR:RCM[1:0]=10).

During counting up

When the position counter maximum value overflows to 0x0000, the revolution counter is counted up. During this time, the overflow flag (QICRL:OFDF) is set to 1.

Example: If the QPRC Maximum Position register (QMPR) is set to 18

Position counter	15	16	17	18	0	1	2
Revolution counter	1	1	1	1	2	2	2

During counting down

When an underflow is detected (a value lower than 0x0000 is detected) and when the value of Quad Counter Maximum Position Counter register (QMPR) is reloaded to the position counter, the revolution counter is counted down. During this time, the underflow flag (QICRL:UFDF) is set to 1.

Example: If the QPRC Maximum Position register (QMPR) is set to 5

Position counter	4	3	2	1	0	5	4	3	2	1	0	5
Revolution counter	1	1	1	1	1	0	0	0	0	0	0	0xFFFF

Note:

- *The counting direction of position counter depends on the AIN and BIN external input signals only.*

Position Counter Reset Mask Function

The position counter reset mask function can be used only when RC_Mode0 (QCR:RCM[1:0]=00) or RC_Mode3 (QCR:RCM[1:0]=11) is selected. This function operates regardless of setting of the position counter mode (PC_Mode1, PC_Mode2 or PC_Mode3).

The position counter reset mask function is executed in the following sequence.

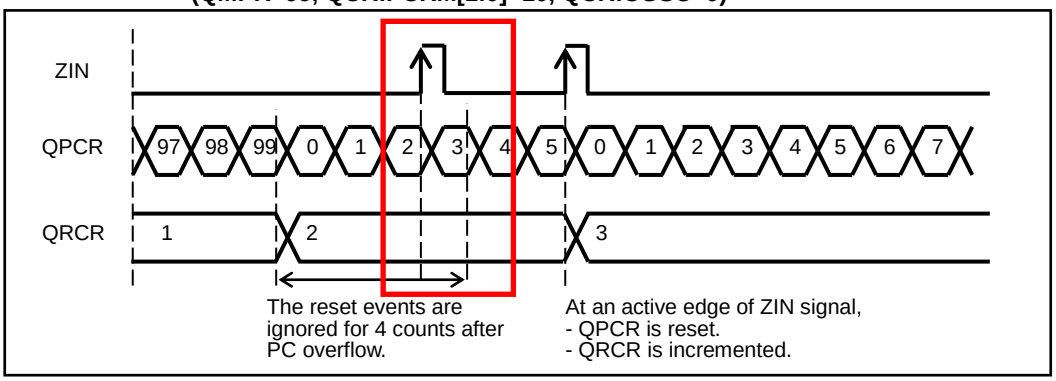
1. When an active event of ZIN signal, an overflow of position counter, or an underflow of position counter is detected, a value being set by the position counter reset mask bits (QCR:PCRM[1:0]) is set to the mask counter (*1).
2. When the position counter is counted up or down in the same counting direction, the mask counter (*1) is counted down.
   The position counter is reset only when the mask counter (*1) is set to 0x0. Also, the revolution counter is not counted up or down.
   When a count inversion of the position counter is detected, the mask counter (*1) is set to 0x0.
3. If the mask counter (*1) is set to 0x0, the position counter is set to 0x0000 when an active edge of the ZIN signal or an overflow of the position counter is detected.

*1: The number of times to mask both the reset of the position counter and the counting up/down of the revolution counter is counted. The masking continues until this counter value reaches 0x0.

The following gives an operation example where the position counter reset mask function is used in RC_Mode3 (QCR:RCM[1:0]=11).

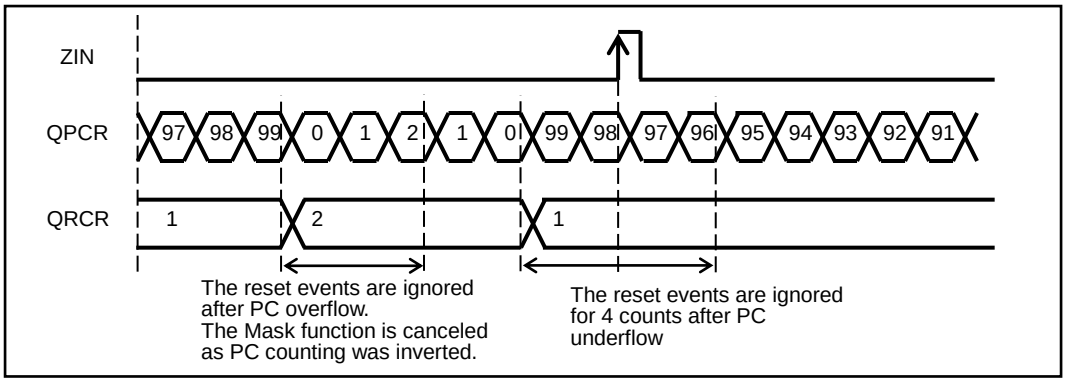
Example 1:
Active edge(s) of the ZIN signal are ignored for four (4) counts(QPCR=0-3) of the position counter after an occurrence of the position counter overflow.

Figure 3-15 Position Counter Reset Mask Operation Example 1 (QMPR=99, QCR:PCRM[1:0]=10, QCR:CGSC=0)



Example 2:
Active edge(s) of the ZIN signal are ignored for four (4) counts(QPCR=99-96) of the position counter after an occurrence of the position counter underflow following count inversion of the position counter.

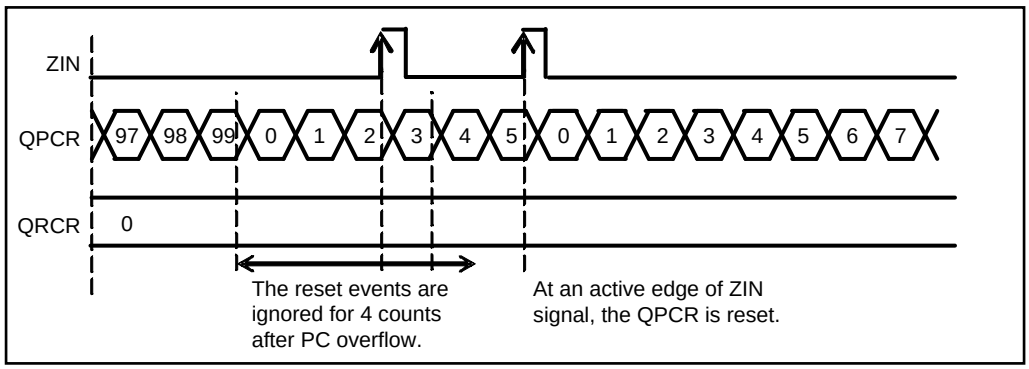
Figure 3-16 Position Counter Reset Mask Operation Example 2 (QMPR=99, QCR:PCRM[1:0]=10, QCR:CGSC=0)



The following gives an operation example where the position counter reset mask function is used in RC_Mode0 (QCR:RCM[1:0]=00).

Example 3:
Active edge(s) of the ZIN signal are ignored for four (4) counts(QPCR=0-3) of the position counter after an occurrence of the position counter overflow if the revolution counter is disabled.

Figure 3-17 Position Counter Reset Mask Operation Example 3 (QMPR=99, QCR:PCRM[1:0]=10, QCR:CGSC=0)



Notes:

- *While the position counter reset mask function is operating, the mask function is released and the position counter can be reset in the following conditions.*
- *When the position counter mode bit (QCR:PCM[1:0]) is changed*
- *When the revolution counter mode bit (QCR:RCM[1:0]) is changed*
- *When the direction of the position counter is changed*
- *Even if an overflow or underflow of the position counter occurs without inversion of the position counter while the position counter reset mask function is operating in RC_Mode0 (QCR:RCM[1:0]=00) or RC_Mode3 (QCR:RCM[1:0]="11"), the revolution counter is not counted up or down. However, if an overflow occurs, the position counter becomes 0. If an underflow occurs, the QMPR is reloaded to the position counter. The overflow interrupt request flag bit (QICR:OFDF) or the underflow interrupt request flag bit (QICR:UFDF) is set to 1.*

4. Registers

This section explains the configuration and functions of the registers used for the Quadrature Position/Revolution Counter (QPRC).

List of Quadrature Position/Revolution Counter Registers

Abbreviation	Register Name	Reference
QPCR	QPRC Position Count register	4.1
QRCR	QPRC Revolution Count register	4.2
QPCCR	QPRC Position Counter Compare register	4.3
QPRCR	QPRC Position and Revolution Counter Compare register	4.4
QCR	QPRC Control register	4.5
QECR	QPRC Extension Control register	4.6
QICRL	Low-Order Bytes of QPRC Interrupt Control register	4.7
QICRH	High-Order Bytes of QPRC Interrupt Control register	4.8
QMPR	QPRC Maximum Position register	4.9
NTCTLA	Control register of Noise Filter for AIN Input	4.10
NFCTLB	Control register of Noise Filter for BIN Input	4.11
NFCTLZ	Control register of Noise Filter for ZIN Input	4.12

4.1 QPRC Position Count Register (QPCR)

The QPRC Position Count register (QPCR) indicates the position counter.

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	QPCR[15:0]															
Attribute	R/W															
Initial value	0x0000															

[bit15:0] QPCR:

Reading this register reads out the current value of the position counter. While the position counter stops counting (QCR:PSTP=1), the count value can be written to this register. Also, write access is ignored while the counter is counting (QCR:PSTP=0),

This register is set to 0x0000 in one of the following conditions.

- Reset
- A ZIN active edge is detected in the following conditions.
  - The ZIN function is set to the counter clear function (QCR:CGSC=0) in RC_Mode1 (QCR:RCM[1:0]=01).
  - After the position counter has been incremented or decremented by the mask set value when the count inversion of the position counter is not detected where the ZIN function is set to the counter clear function (QCR:CGSC=0) and the reset mask function of the position counter is valid (QCR:PCRM[1:0]=01 or 10 or 11) in RC_Mode0 (QCR:RCM[1:0]=00) or RC_Mode3 (QCR:RCM[1:0]=11)
  - The ZIN function is set to the counter clear function (QCR:CGSC=0) and the reset mask function of the position counter is invalid (QCR:PCRM[1:0]=00) in RC_Mode0(QCR:RCM[1:0]=00) or RC_Mode3(QCR:RCM[1:0]=11).
- A position counter overflow is detected in the following conditions.
  - RC_Mode2(QCR:RCM[1:0]=10)
  - After the position counter has been incremented or decremented by the mask set value when the count inversion of the position counter is not detected where the ZIN function is set to the counter clear function (QCR:CGSC=0) and the reset mask function of the position counter is valid (QCR:PCRM[1:0]=01 or 10 or 11) in RC_Mode0 (QCR:RCM[1:0]=00) or RC_Mode3 (QCR:RCM[1:0]=11)
  - The ZIN function is set to the counter clear function (QCR:CGSC=0) and the reset mask function of the position counter is invalid (QCR:PCRM[1:0]=00) in RC_Mode0(QCR:RCM[1:0]=00) or RC_Mode3(QCR:RCM[1:0]=11).
- 0x0000 is written to this QPCR while the position counter is under suspension (QCR:PSTP=1).

The value of the QPRC Maximum Position register (QMPR) is set to this register in the following condition.

- A position counter underflow is detected.

Notes:

- *Do not access the QPRC Position Count register (QPCR) with a byte access instruction.*
- *After the count value was written to the QPRC Position Count register (QPCR) while the position counter was under suspension (QCR:PSTP=1) in RC_Mode0 (QCR:RCM[1:0]=00), RC_Mode1 (QCR:RCM[1:0]=01), or RC_Mode3(QCR:RCM[1:0]=11), if a ZIN active edge is detected with the count function (QCR:CGSC=0), the QPRC Position Count register (QPCR) will be set to 0x0000. To write the count value to the QPRC Position Count register (QPCR), disable the ZIN detection edge (QCR:CGE[1:0]=00) before writing it to the QPCR.*

4.2 QPRC Revolution Count Register (QRCR)

The QPRC Revolution Count register (QRCR) indicates the revolution counter.

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	QRCR[15:0]															
Attribute	R/W															
Initial value	0x0000															

[bit15:0] QRCR[15:0]:

Reading this register reads out the current value of the revolution counter. While the revolution counter stops counting (QCR:RCM[1:0]=00), the count value can be written to this register. Also, write access is ignored while the counter is counting (QCR:RCM[1:0]≠00)

This register is set to 0x0000 in one of the following conditions.

- Reset
- 0x0000 is written to this register while the revolution counter is under suspension (QCR:RCM[1:0]=00).

Notes:

- *Do not access the QPRC Revolution Count register (QRCR) with a byte access instruction.*
- *As the direction of the position counter is not detected in PC_Mode0 (QCR:PCM[1:0]=00), the last position counter direction bit (QICR:DIRPC) becomes indefinite. Therefore, if the mode is changed from PC_Mode0 (QCR:PCM[1:0]=00) to another mode, when a ZIN active edge is detected before an AIN/BIN active edge is detected, the following operations apply.*
- *The position counter is reset if the mode is RC_Mode0 (QCR:RCM[1:0]=00), RC_Mode1 (QCR:RCM[1:0]=01), or RC_Mode3 (QCR:RCM[1:0]=11)*
- *The revolution counter is not counted up or down*

4.3 QPRC Position Counter Compare Register (QPCCR)

The QPRC Position Counter Compare register (QPCCR) is used to compare with the count value of the position counter.

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	QPCCR[15:0]															
Attribute	R/W															
Initial value	0x0000															

[bit15:0] QPCCR[15:0]:

If the value of this register matches that of the position counter, the QPRC position counter comparison match flag (QICR:QPCMF) is set to 1. This Compare register can be used only to compare with the count value of the position counter.

Note:

- *Do not access the QPRC Position Counter Compare register (QPCCR) with a byte access instruction.*

4.4 QPRC Position and Revolution Counter Compare Register (QPRCR)

The QPRC Position and Revolution Counter Compare register (QPRCR) is used to compare with the selected count value of the position or revolution counter.

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	QPRCR[15:0]															
Attribute	R/W															
Initial value	0x0000															

[bit15:0] QPRCR[15:0]:

Use the RSEL bit of the QPRC Control register (QCR) to select the position counter or revolution counter to be compared with. If the value of this register matches that of the position or revolution counter, the QPRC position and revolution counter comparison match flag (QICR:QPRCMF) is set to 1.

Note:

- *Do not access the QPRC Position and Revolution Counter Compare register (QPRCR) with a byte access instruction.*

4.5 QPRC Control Register (QCR)

The QPRC Control register (QCR) is used to specify the operation mode of the position counter or 16-bit revolution counter. It is also used to start or stop each counter.

Low-Order Bytes of QPRC Control Register (QCRL)

bit	7	6	5	4	3	2	1	0
Field	SWAP	RSEL	CGSC	PSTP	RCM1	RCM0	PCM1	PCM0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7] SWAP: Swap bit

This bit is used to swap the connections of the AIN input and BIN input to the position counter.

When this bit is set to 0, the AIN pin is used for the AIN input of the position counter, and the BIN pin is used for the BIN input of the position counter. When this bit is set to 1, the AIN pin is used for the BIN input of the position counter, and the BIN pin is used for the AIN input of the position counter.

Bit	Description
0	No swap
1	Swaps AIN and BIN inputs.

Note:

- *Change the swap bit (SWAP) when the position counter is disabled (PCM[1:0]=00).*

[bit6] RSEL: Register function selection bit

This bit is used to select the position counter or revolution counter to be compared with the QPRC position and revolution counter compare register.

Bit	Description
0	Compares the value of the QPRC Position and Revolution Counter Compare register (QPRCR) with that of the position counter.
1	Compares the value of the QPRC Position and Revolution Counter Compare register (QPRCR) with that of the revolution counter.

Note:

- *When the value of the position counter matches that of the QPRC Position Counter Compare register (QPCCR) and also the value of the revolution counter matches that of the QPRC Position and Revolution Counter Compare register (QPRCR), the PC match and RC match interrupt request flag bit (QICR: QPCNRCMF) is set to 1 regardless of the setting of this bit.*

[bit5] CGSC: Count clear or gate selection bit

This bit is used to select the function of the ZIN external pin.

When the counter clear function is enabled (QGSC=0), the ZIN pin clears the position counter if the revolution count mode is set to RC_Mode0 (RCM[1:0]=00), RC_Mode1 (RCM[1:0]=01), or RC_Mode3 (RCM[1:0]=11). The CGE1 and CGE0 bits of the QCR register clear the position counter by selecting a valid edge of the ZIN pin and detecting the selected edge.

When the gate function is enabled (QGSC=1), the ZIN pin controls the count operation of the position counter. The CGE1 and CGE0 bits of the QCR register count the position counter at the valid level of the ZIN pin.

Bit	Description
0	Counter clear function
1	Gate function

[bit4] PSTP: Position counter stop bit

This bit is used to stop the position counter.

Bit	Description
0	Enables count operation.
1	Stops count operation.

[bit3:2] RCM1, RCM0: Revolution counter mode bits

These bits are used to select the count mode of the revolution counter and the reset mode of the position counter. For the effect on the position counter, see Operation of Revolution Counter.

bit3	bit2	Description
0	0	Disables the revolution counter (RC_Mode0).
0	1	The revolution counter is counted up or down only with a ZIN active edge (RC_Mode1).
1	0	The revolution counter is counted up or down only when overflow or underflow is detected in the position counter that matches QMPR (RC_Mode2).
1	1	The revolution counter is counted up or down in two cases: a position counter overflow or underflow is detected and a ZIN active edge is detected (RC_Mode3).

[bit1:0] PCM1, PCM0: Position counter mode bits

These bits are used to select the count mode of the position counter.

bit1	bit0	Description
0	0	Disables the position counter (PC_Mode0) to stop it.
0	1	Up-down count mode (PC_Mode1) Increments the value with an AIN active edge and decrements it with a BIN active edge.
1	0	Phase difference count mode (PC_Mode2) Counts up if AIN is leading BIN and down if BIN is leading AIN.
1	1	Directional count mode (PC_Mode3) Counts up or down with the BIN active edge and AIN level.

Note:

As the direction of the position counter is not detected in PC_Mode0 (PCM[1:0]=00), the last position counter direction bit (QICR:DIRPC) becomes indefinite. Therefore, if the mode is changed from PC_Mode0 (PCM[1:0]=00) to another mode, when a ZIN active edge is detected before an AIN/BIN active edge is detected, the following operations apply.

- *The position counter is reset if the mode is RC_Mode0 (RCM[1:0]="00"), RC_Mode1 (RCM[1:0]=01), or RC_Mode3 (RCM[1:0]=11)*
- *The revolution counter is not counted up or down*

High-Order Bytes of the QPRC Control Register (QCRH)

bit	15	14	13	12	11	10	9	8
Field	CGE1	CGE0	BES1	BES0	AES1	AES0	PCRM1	PCRM0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit15:14] CGE1, CGE0: Detection edge selection bits

These bits are used to select the detection edge when the ZIN external pin is used for the counter clear function (CGSC=0). They are also used to select the detection level when the ZIN external pin is used for the gate function (CGSC=1).

bit15	bit14	ZIN used for counter clear function (CGSC=0)	ZIN used for gate function (CGSC=1)
0	0	Disables edge detection.	Disables level detection.
0	1	Detects a falling edge.	Detects level L.
1	0	Detects a rising edge.	Detects level H.
1	1	Detects a rising or falling edge.	Disables level detection.

[bit13:12] BES1, BES0: BIN detection edge selection bits

These bits are used to select the detection edge of the BIN external pin.

bit13	bit12	Description
0	0	Disables edge detection.
0	1	Detects a falling edge.
1	0	Detects a rising edge.
1	1	Detects rising and falling edges.

[bit11:10] AES1, AES0: AIN detection edge selection bits

These bits are used to select the detection edge of the AIN external pin.

bit11	bit10	Description
0	0	Disables edge detection.
0	1	Detects a falling edge.
1	0	Detects a rising edge.
1	1	Detects rising and falling edges.

[bit9:8] PCRM1, PCRM0: Position counter reset mask bits

These bits are used to specify the period (mask time) to ignore the events shown below after detecting a position counter overflow or underflow or detecting a ZIN active edge.

- Position counter resetting
- Revolution counter increment or decrement

This mask function is released when the count direction of the position counter is changed, and restarts when a position counter overflow or underflow is detected or a ZIN active edge is detected.

bit9	bit8	Description
0	0	No reset mask
0	1	The position counter reset or a revolution counter count-up or -down events are ignored until the position counter changes twice.
1	0	The position counter reset or a revolution counter count-up or -down events are ignored until the position counter changes four times.
1	1	The position counter reset or a revolution counter count-up or -down events are ignored until the position counter changes eight times.

Notes:

- *The position counter reset mask function is available only in RC_Mode0 (RCM[1:0]=00) and RC_Mode3 (RCM[1:0]=11). This function operates regardless of the setting of the position counter mode (PC_Mode1, PC_Mode2, or PC_Mode3).*
- *While the position counter reset mask function is operating, the mask function is released and the position counter can be reset in the following conditions.*
- *When the position counter mode bit (PCM[1:0]) is changed*
- *When the revolution counter mode bit (RCM[1:0]) is changed*
- *When the direction of the position counter is changed*

4.6 QPRC Extension Control Register (QECR)

The QPRC Extension Control register (QECR) is used to select that the revolution counter is inside the count range, indicate that the revolution counter is outside the count range, or control whether or not to generate an interrupt when the revolution counter gets out of the range.

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Reserved												PEC	ORNGIE	ORNGF	ORNGMD
Attribute	-												R/W	R/W	R/W	R/W
Initial value	000000000000												0	0	0	0

[bit15:4] Reserved bits

Always write 0 to these bits. The read value is 0.

[bit3] PEC: Phase edge change bit

This bit is used to change the operating edge in 1-time frequency multiplication of PC_Mode2. This bit has effect in 1-time frequency multiplication of PC_Mode2 only: otherwise it has no effect.

This bit does not exist in TYPE1-M4, TYPE2-M4, TYPE6-M4 products.

bit	Description
0	The QPCR is counted up or down by the same edge (rising edge or falling edge).
1	The QPCR is counted up or down by both edge (rising edge and falling edge).

[bit2] ORNGIE: Outrange interrupt enable bit

This bit is used to control whether or not to issue an interrupt notification to the CPU when the outrange interrupt request flag (ORNGF) is set to 1. When this bit is set to 1, an interrupt is generated if the value of the revolution counter gets out of the range (ORNGF=1).

Bit	Description
0	Interrupt disabled
1	Interrupt enabled

[bit1] ORNGF: Outrange interrupt request flag bit

This flag indicates that the revolution counter is outside the count range.

If a positive number is selected as the outrange mode of the revolution counter (ORNGMD=0), this flag is set to 1 when the revolution counter changes from 0x0001 to 0x0000 after counting down or when it changes from 0xFFFE to 0xFFFF after counting up.

If the 8K value is selected as the outrange mode of the revolution counter (ORNGMD=1), this flag is set to 1 when the revolution counter changes from 0x8001 to 0x8000 after counting down or when it changes from 0x7FFE to 0x7FFF after counting up.

This flag can be cleared to 0 only in write mode. Writng 1 has no effect.

1 is read by the read-modify-write access operation.

Bit	Description	
	Read	Write
0	Out of range is not detected.	Clears this bit.
1	Out of range is detected.	No effect.

[bit0] ORNGMD: Outrange mode selection bit

This bit defines the outrange mode of the revolution counter.

Bit	Description
0	Selects a positive number (in the range from 0x0000 to 0xFFFF).
1	Selects the 8K value (in the range from 0x0000 to 0x7FFF).

4.7 Low-Order Bytes of the QPRC Interrupt Control Register (QICRL)

The Low-Order Bytes of the QPRC Interrupt Control register (QICRL) are used to control a position counter overflow or underflow interrupt, zero index interrupt, QPRC position counter comparison match interrupt, or QPRC position and revolution counter comparison match interrupt.

bit	7	6	5	4	3	2	1	0
Field	ZIIF	OFDF	UFDF	OUZIE	QPRCMF	QPRCMIE	QPCMF	QPCMIE
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit7] ZIIF: Zero index interrupt request flag bit

This flag is set to 1 when the position counter is reset by the ZIN input.

This flag can only be cleared to 0 in write mode. Setting 1 has no effect.

1 is read by the read-modify-write access operation.

bit	Description	
	Read	Write
0	Does not detect zero index.	Clears this bit.
1	Detects zero index.	No effect.

Note:

- *The zero index interrupt request flag bit (ZIIF) is not set to 1 even if ZIN is used as the gate function (QCR:CGSC=1) or the position counter is reset in RC_Mode2 (QCR:RCM[1:0]=10).*

[bit6] OFDF: Overflow interrupt request flag bit

This flag indicates that a position counter overflow occurs. When the set value of the QPRC Maximum Position register (QMPR) matches the value of the position counter and the position counter is counted up, this bit is set to 1.

This flag can be cleared to 0 only in write mode. Writng 1 has no effect.

1 is read by the read-modify-write access operation.

bit	Description	
	Read	Write
0	Does not detect overflow.	Clears this bit.
1	Detects overflow.	No effect.

[bit5] UFDF: Underflow interrupt request flag bit

This flag indicates that a position counter underflow occurs. When the position counter is 0x0000 and the position counter is counted down, this bit is set to 1.

This flag can be cleared to 0 only in write mode. Writng 1 has no effect.

"1" is read by the read-modify-write access operation.

bit	Description	
	Read	Write
0	Does not detect underflow.	Clears this bit.
1	Detects underflow.	No effect.

[bit4] OUZIE: Overflow, underflow, or zero index interrupt enable bit

This bit is used to control whether or not to issue an interrupt notification to the CPU when the overflow interrupt request flag bit (OFDF), underflow interrupt request flag bit (UFDF), or zero index interrupt request flag bit (ZIIF) is set to 1. When this bit is set to 1, an interrupt is generated if overflow is detected (OFDF=1), underflow is detected (UFDF=1), or zero index is detected (ZIIF=1).

bit	Description
0	Interrupt disabled
1	Interrupt enabled

[bit3] QPRCMF: PC and RC match interrupt request flag bit

This flag indicates whether the value of the position counter matches that of the QPRC Position and Revolution Counter Compare register (QPRCR) or the value of the revolution counter (QRCR) matches that of the QPRC Position and Revolution Counter Compare register (QPRCR).

When the comparison between the position counter and QPRC Position and Revolution Counter Compare register (QPRCR) is selected (QCR:RSEL=0), this flag is set to 1 if the value of the position counter matches that of the QPRC Position and Revolution Counter Compare register (QPRCR).

When the comparison between the revolution counter and QPRC Position and Revolution Counter Compare register (QPRCR) is selected (QCR:RSEL=1), this flag is set to 1 if the value of the revolution counter matches that of the QPRC Position and Revolution Counter Compare register (QPRCR).

This flag can only be cleared to 0 in write mode. Setting 1 has no effect.

1 is read by the read-modify-write access operation.

Bit	Description	
	Read	Write
0	Does not detect comparison match with the QPRCR value.	Clears this bit.
1	Detects a comparison match with the QPRCR value.	No effect.

Notes:

- *If the register function selection bit (QCR:RSEL) is set to 0, the PC and RC match interrupt request flag bit (QPRCMF) is set to 1 immediately when one of the following conditions is satisfied.*
- *The mode is changed to PC_Mode1 (QCR:PCM[1:0]=01), PC_Mode2 (QCR:PCM[1:0]=10), or PC_Mode3 (QCR:PCM[1:0]=11) when the position counter is disabled (QCR:PCM[1:0]=00) and the value of the position counter matches that of the QPRC Position and Revolution Counter Compare register (QPRCR).*
- *The value of the position counter matches that of the QPRC Position and Revolution Counter Compare register (QPRCR) when data is written to the QPRC Position Count register (QPCR) or QPRC Position and Revolution Counter Compare register (QPRCR) in PC_Mode1 (QCR:PCM[1:0]=01), PC_Mode2 (QCR:PCM[1:0]=10), or PC_Mode3 (QCR:PCM[1:0]=11).*

- *If the register function selection bit (QCR:RSEL) is set to 1, the PC and RC match interrupt request flag bit (QPRCMF) is set to 1 immediately when one of the following conditions is satisfied.*
- *The value of the revolution counter matches that of the QPRC Position and Revolution Counter Compare Register (QPRCR) by writing data to the QPRC Position and Revolution Counter Compare Register (QPRCR) when the mode is RC_Mode1 (QCR:RCM[1:0]=01), RC_Mode2 (QCR:RCM[1:0]=10), or RC_Mode3 (QCR:RCM[1:0]=11).*
- *The value of the revolution counter matches that of the QPRC Position and Revolution Counter Compare register (QPRCR) by changing the mode from RC_Mode0 (QCR:RCM[1:0]=00) to another mode.*
- *When the register function selection bit (QCR:RSEL) is changed, the PC and RC match interrupt request flag bit (QPRCMF) is set to 1 immediately if one of the following conditions is satisfied.*
- *The value of the revolution counter matches that of the QPRC Position and Revolution Counter Compare register (QPRCR) when the register function selection bit (QCR:RSEL) is changed from 0 to 1 in the mode other than RC_Mode0 (QCR.RCM[1:0]=00).*
- *The value of the position counter matches that of the QPRC Position and Revolution Counter Compare register (QPRCR) when the register function selection bit (QCR:RSEL) is changed from 1 to 0 in the mode other than RC_Mode0 (QCR.RCM[1:0]=00).*

[bit2] QPRCMIE: PC and RC match interrupt enable bit

This bit is used to control whether or not to issue an interrupt notification to the CPU when the PC and RC match interrupt request flag (QPRCMF) is set to 1. When this bit is set to 1, an interrupt is generated if the value of the position or revolution counter matches that of the QPRC Position and Revolution Counter Compare register (QPRCR) (QPRCMF=1).

bit	Description
0	Interrupt disabled
1	Interrupt enabled

[bit1] QPCMF: PC match interrupt request flag bit

This flag indicates whether or not the value of the position counter matches that of the QPRC Position Counter Compare register (QPCCR).

This flag is set to 1 if the value of the position counter matches that of the QPRC Position Counter Compare register (QPCCR).

This flag can be cleared to 0 only in write mode. Writing 1 has no effect.

1 is read by the read-modify-write access operation.

Bit	Description	
	Read	Write
0	Does not detect comparison match with the QPCCR value.	Clears this bit.
1	Detects a comparison match with the QPCCR value.	No effect.

Notes:

The PC match interrupt request flag bit (QPCMF) is set to 1 immediately when one of the following conditions is satisfied.

- *The mode is changed to PC_Mode1 (QCR:PCM[1:0]=01), PC_Mode2 (QCR:PCM[1:0]=10), or PC_Mode3 (QCR:PCM[1:0]=11) when the position counter is disabled (QCR:PCM[1:0]=00) and the value of the position counter matches that of the QPRC Position Counter Compare register (QPCCR).*
- *The value of the position counter matches that of the QPRC Position Counter Compare register (QPCCR) by writing to the QPRC Position Count register (QPCR) when the position counter stop bit (QCR:PSTP) is 1 and when the mode is PC_Mode1 (QCR:PCM[1:0]=01), PC_Mode2 (QCR:PCM[1:0]=10), or PC_Mode3 (QCR:PCM[1:0]=11).*
- *The value of the position counter matches that of the QPRC Position Counter Compare register (QPCCR) by writing to the QPRC Position Counter Compare register (QPCCR) when the mode is PC_Mode1 (QCR:PCM[1:0]=01), PC_Mode2 (QCR:PCM[1:0]=10), or PC_Mode3 (QCR:PCM[1:0]=11).*

[bit0] QPCMIE: PC match interrupt enable bit

This bit is used to control whether or not to issue an interrupt notification to the CPU when the PC match interrupt request flag (QPCMF) is set to 1.

When this bit is set to 1, an interrupt is generated if the value of the position counter matches that of the QPRC Position Counter Compare register (QPCCR) (QPCMF=1).

Bit	Description
0	Interrupt disabled
1	Interrupt enabled

4.8 High-Order Bytes of QPRC Interrupt Control Register (QICRH)

The High-Order Bytes of QPRC Interrupt Control register (QICRH) are used to control a match between the position counter and QPCCR, a match between the revolution counter and QPRCR, and a count inversion interrupt. They are also used to indicate the direction of the position counter when the last underflow or overflow interrupt was detected or the last value of the position counter was changed.

bit	15	14	13	12	11	10	9	8
Field	Reserved		QPCNRCMF	QPCNRCMIE	DIROU	DIRPC	CDCF	CDCIE
Attribute	-		R/W	R/W	R	R	R/W	R/W
Initial value	00		0	0	0	0	0	0

[bit15:14] Reserved : Reserved bits

Always write 0 to these bits. The read value is 0.

[bit13] QPCNRCMF: PC match and RC match interrupt request flag bit

This flag indicates whether or not the value of the position counter matches that of the QPRC Position Counter Compare register (QPCCR) and the value of the revolution counter matches that of the QPRC Position and Revolution Counter Compare register (QPRCR).

This flag is set to 1 when the value of the position counter matches that of the QPRC Position Counter Compare register (QPCCR) (QPCMF=1) and the value of the revolution counter matches that of the QPRC Position and Revolution Counter Compare register (QPRCR).

This flag can only be cleared to 0 in write mode. Setting 1 has no effect.

1 is read by the read-modify-write access operation.

Bit	Description	
	Read	Write
0	Does not detect match.	Clears this bit.
1	Detects a match.	No effect.

Notes:

- *The PC match and RC match interrupt request flag bit (QPCNRCMF) is set to 1 immediately when one of the following conditions is satisfied.*
- *The mode is changed to PC_Mode1 (QCR:PCM[1:0]=01), PC_Mode2 (QCR:PCM[1:0]=10), or PC_Mode3 (QCR:PCM[1:0]=11) when the position counter is disabled (QCR:PCM[1:0]=00) and the revolution counter is in the mode other than RC_Mode0(QCR:RCM[1:0]=00) while the value of the position counter matches that of the QPRC Position Counter Compare register (QPCCR) and the value of the revolution counter matches that of the QPRC Position and Revolution Counter Compare register (QPRCR).*
- *The value of the position counter matches that of the QPRC Position Counter Compare register (QPCCR) when data is written to the QPRC Position Count register (QPCR) or QPRC Position Counter Compare Register (QPCCR) where the value of the revolution counter matches that of the QPRC Position & Revolution Counter Compare register (QPRCR) when the mode is PC_Mode1 (QCR:PCM[1:0]=01), PC_Mode2 (QCR:PCM[1:0]=10), or PC_Mode3 (QCR:PCM[1:0]=11) and the revolution counter is in the mode other than RC_Mode0 (QCR:RCM[1:0]=00).*
- *The value of the revolution counter matches that of the QPRC Position and Revolution Counter Compare register (QPRCR) when the data is written to the QPRC Position and Revolution Counter Compare register (QPRCR) in the mode other than RC_Mode0 (QCR:RCM[1:0]=00) where the specified value matches that of the QPRC Position Count register (QPCR) or QPRC Position Counter Compare register (QPCCR) in PC_Mode1 (QCR:PCM[1:0]=01), PC_Mode2 (QCR:PCM[1:0]=10), or PC_Mode3 (QCR:PCM[1:0]=11).*
- *The value of the revolution counter matches that of the QPRC Position and Revolution Counter Compare register (QPRCR) when the mode is changed from RC_Mode0 (QCR:RCM[1:0]=00) to another mode where the specified value matches that of the QPRC Position Count register (QPCR) or QPRC Position Counter Compare register (QPCCR) in PC_Mode1 (QCR:PCM[1:0]=01), PC_Mode2 (QCR:PCM[1:0]=10), or PC_Mode3 (QCR:PCM[1:0]=11).*
- *This bit is set to 1 when the value of the position counter matches that of the QPRC Position Counter Compare register (QPCCR) and the value of the revolution counter matches that of the QPRC Position and Revolution Counter Compare register (QPRCR) regardless of the setting of the register function selection bit (QCR:RSEL).*

[bit12] QPCNRCMIE: PC match and RC match interrupt enable bit

This bit is used to control whether or not to issue an interrupt notification to the CPU when the PC match and RC match interrupt request flag (QPCNRCMF) is set to 1.

When this bit is set to 1, an interrupt is generated if the value of the position counter matches that of the QPRC Position Counter Compare register (QPCCR) and the value of the revolution counter matches that of the QPRC Position and Revolution Counter Compare register (QPRCR) (QPCNRCMF=1).

bit	Description
0	Interrupt disabled
1	Interrupt enabled

[bit11] DIROU: Last position counter flow direction bit

This bit indicates the direction of the position counter when the last position counter overflow or underflow was detected.

bit	Description
0	The position counter was incremented.
1	The position counter was decremented.

[bit10] DIRPC: Last position counter direction bit

This bit indicates the count direction when the position counter was last changed.

Bit	Description
0	The position counter was incremented.
1	The position counter was decremented.

Note:

As the direction of the position counter is not detected in PC_Mode0 (QCR:PCM[1:0]=00), the last position counter direction bit (QICR:DIRPC) becomes indefinite. Therefore, if the mode is changed from PC_Mode0 (QCR:PCM[1:0]=00) to another mode, when a ZIN active edge is detected before an AIN/BIN active edge is detected, the following operations apply.

- *The position counter is reset if the mode is RC_Mode0 (QCR:RCM[1:0]=00), RC_Mode1 (QCR:RCM[1:0]=01), or RC_Mode3 (QCR:RCM[1:0]=11)*
- *The revolution counter is not counted up or down*

[bit9] CDCF: Count inversion interrupt request flag bit

This bit indicates whether or not the position counter inverted the count direction.

This bit is set to 1 when the position counter inverts the count direction. Inverting the count direction means that the counter counts down at the next counting after counting up, or the counter counts up at the next counting after counting down.
This flag can be cleared to 0 only in write mode. Writing 1 has no effect.
1 is read by the read-modify-write access operation.

Bit	Description	
	Read	Write
0	Does not invert the count direction of the position counter.	Clears this bit.
1	Inverts the count direction of the position counter at least once.	No effect.

Note:

- *As the direction of the position counter is not detected in PC_Mode0 (QCR:PCM[1:0]=00), the last position counter direction bit (QICR:DIRPC) becomes indefinite. Therefore, after the mode is changed from PC_Mode0 (QCR:PCM[1:0]=00) to another mode, even if an AIN/BIN active edge is detected and the direction of the position counter is inverted, the count inversion interrupt request flag bit (QICR:CDCF) is not set to 1.*

[bit8] CDCIE: Count inversion interrupt enable bit

This bit is used to control whether or not to issue an interrupt notification to the CPU when the count inversion interrupt request flag (CDCF) is set to 1.

When this bit is set to 1, an interrupt is generated if the count direction of the position counter is inverted (CDCF=1).

Bit	Description
0	Interrupt disabled
1	Interrupt enabled

4.9 QPRC Maximum Position Register (QMPR)

The QPRC Maximum Position register (QMPR) is used to specify the maximum value of the position counter.

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	QMPR[15:0]															
Attribute	R/W															
Initial value	0xFFFF															

[bit15:0] QMPR:

When the set value of the QPRC Maximum Position register (QMPR) matches the value of the position counter and the position counter is counted up, a position counter overflow is detected (QICR:OFDF=1). The set value of the QPRC Maximum Position register (QMPR) is reloaded to the position counter if a position counter underflow is detected (QICR:UFDF=1).

Note:

- *Do not access the QPRC Maximum Position register (QMPR) with a byte access instruction.*

4.10 AIN Noise Control Register (NFCTLA)

The AIN Noise Control register (NFCTLA) is used to specify the operation of the AIN external pin.

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Reserved										AINMD	AINLV	Reserved	AINNWS[2:0]		
Attribute	-										R/W	R/W	-	R/W		
Initial value											0	0		000		

[bit15:6]Reserved: Reserved bits

Writing has no effect. The read value is indefinite.

[bit5]AINMD: Mask bit

This bit is used to mask the AIN external pin.

Bit	Description
0	Enables AIN input.
1	Masks AIN input.

[bit4]AINLV: Input invert bit

This bit is used to invert the input level of AIN external pin.

Bit	Description
0	Does not invert the AIN input level.
1	Inverts the AIN input level.

[bit3]Reserved: Reserved bit

Writing has no effect. The read value is indefinite.

[bit2:0] AINNWS[2:0]: Noise filter width select bits

These bits are used to specify the filter width of the AIN External pin digital noise filter.

bit2	bit1	bit0	Description
0	0	0	No noise filter operation
0	0	1	Specifies four PCLK cycles as noise filter width.
0	1	0	Specifies eight PCLK cycles as noise filter width.
0	1	1	Specifies 16 PCLK cycles as noise filter width.
1	0	0	Specifies 32 PCLK cycles as noise filter width.
1	0	1	Specifies 64 PCLK cycles as noise filter width.
1	1	0	Specifies 128 PCLK cycles as noise filter width.
1	1	1	Specifies 256 PCLK cycles as noise filter width.

4.11 BIN Noise Control Register (NFCTLB)

The BIN noise control register (NFCTLB) is used to specify the operation of the BIN external pin.

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Reserved										BINMD	BINLV	Reserved	BINNWS[2:0]		
Attribute	-										R/W	R/W	-	R/W		
Initial value											0	0		000		

[bit15:6] Reserved: Reserved bits

Writing has no effect. The read value is indefinite.

[bit5] BINMD: Mask bit

This bit is used to mask the BIN external pin.

bit	Description
0	Enables BIN input.
1	Masks BIN input.

[bit4] BINLV: Input invert bit

This bit is used to invert the input level of the BIN external pin.

bit	Description
0	Does not invert the BIN input level.
1	Inverts the BIN input level.

[bit3] Reserved: Reserved bit

Writing has no effect. The read value is indefinite.

[bit2:0] BINNWS[2:0]: Noise filter width select bits

These bits are used to specify the filter width of BIN External pin digital noise filter.

bit2	bit1	bit0	Description
0	0	0	No noise filter operation
0	0	1	Specifies four PCLK cycles as noise filter width.
0	1	0	Specifies eight PCLK cycles as noise filter width.
0	1	1	Specifies 16 PCLK cycles as noise filter width.
1	0	0	Specifies 32 PCLK cycles as noise filter width.
1	0	1	Specifies 64 PCLK cycles as noise filter width.
1	1	0	Specifies 128 PCLK cycles as noise filter width.
1	1	1	Specifies 256 PCLK cycles as noise filter width.

4.12 ZIN Noise Control Register (NFRCTLZ)

The ZIN noise control register (NFRCTLZ) is used to specify the operation of the ZIN external pin.

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Reserved										ZINMD	ZINLV	Reserved	ZINNWS[2:0]		
Attribute	-										R/W	R/W	-	R/W		
Initial value											0	0		000		

[bit15:6] Reserved: Reserved bits

Writing has no effect. The read value is indefinite.

[bit5] ZINMD: Mask bit

This bit is used to mask the ZIN external pin.

Bit	Description
0	Enables ZIN input.
1	Masks ZIN input.

[bit4] ZINLV: Input invert bit

This bit is used to invert the input level of the ZIN external pin.

Bit	Description
0	Does not invert the ZIN input level.
1	Inverts the ZIN input level.

[bit3] Reserved: Reserved bit

Writing has no effect. The read value is indefinite.

[bit2:0] ZINNWS[2:0]: Noise filter width select bit

These bits are used to specify the filter width of the ZIN External pin digital noise filter.

bit2	bit1	bit0	Description
0	0	0	No noise filter operation
0	0	1	Specifies four PCLK cycles as noise filter width.
0	1	0	Specifies eight PCLK cycles as noise filter width.
0	1	1	Specifies 16 PCLK cycles as noise filter width.
1	0	0	Specifies 32 PCLK cycles as noise filter width.
1	0	1	Specifies 64 PCLK cycles as noise filter width.
1	1	0	Specifies 128 PCLK cycles as noise filter width.
1	1	1	Specifies 256 PCLK cycles as noise filter width.

CHAPTER 8-2: Quad Counter Position Rotation Count Display Function

This chapter describes the quad counter position rotation count dispay function (integrated in the products after TYPE2).

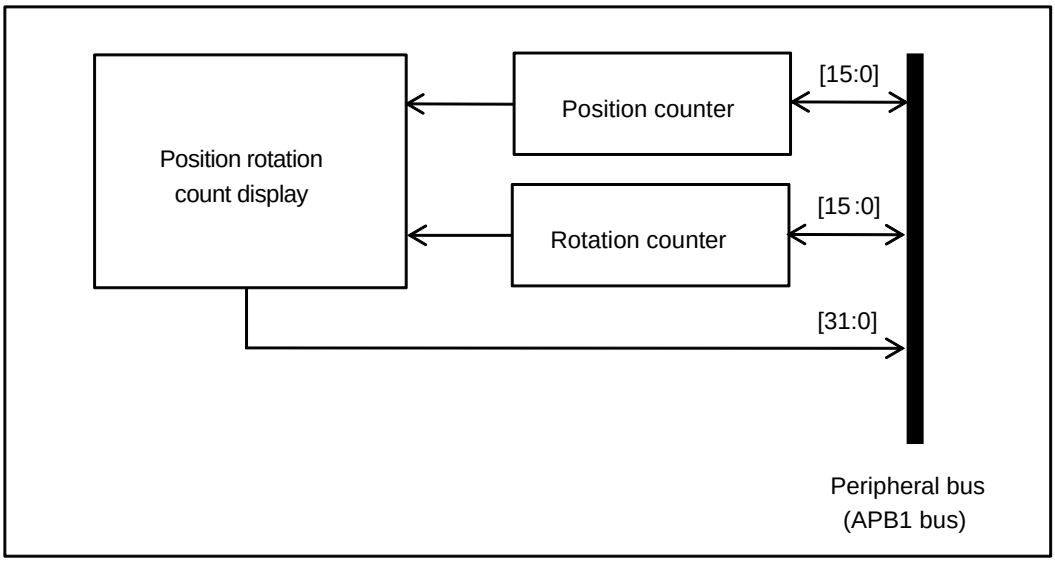
1. Overview and Configuration
2. Register

1. Overview and Configuration

This section describes the overview of the quad counter position rotation count display function.

The products after TYPE2 have functions that can read the value of the quad counter position count register (QPCR) and the value of the quad counter rotation count register (QRCR) simultaneously.

Figure 1-1 Block Diagram of Quad Counter Position Rotation Count Register



2. Register

This section describes the register of the quad counter position rotation count display function.

Register Abbreviation	Register Name	Reference
QPRCRR	Quad Counter Position Rotation Count Register	2.1

2.1 Quad Counter Position Rotation Count Register (QPRCRR)

The values of the quad counter position count register (QPCR) and quad counter rotation count register (QRCR) are displayed.

Register configuration

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Field	QRCRR [15:0]															
Attribute	R															
Initial value	0x0000															

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	QPCRR [15:0]															
Attribute	R															
Initial value	0x0000															

Register function

[bit31:16] QRCRR: Quad counter rotation count display bit

This is a mirror register that can read the same value as the quad counter rotation count register (QRCR). Writing is disabled.

[bit15:0] QPCRR: Quad counter position count display bit

This is a mirror register that can read the same value as the quad counter position count register (QPCR). Writing is disabled.

By using this register, the values of the quad counter position count register (QPCR) and quad counter rotation count register (QRCR) can be read simultaneously.

Appendixes

This chapter shows the register map, list of notes, limitations and product type list.

A. Register Map

B. List of Notes

C. Major Changes

A. Register Map

This chapter shows the register map.

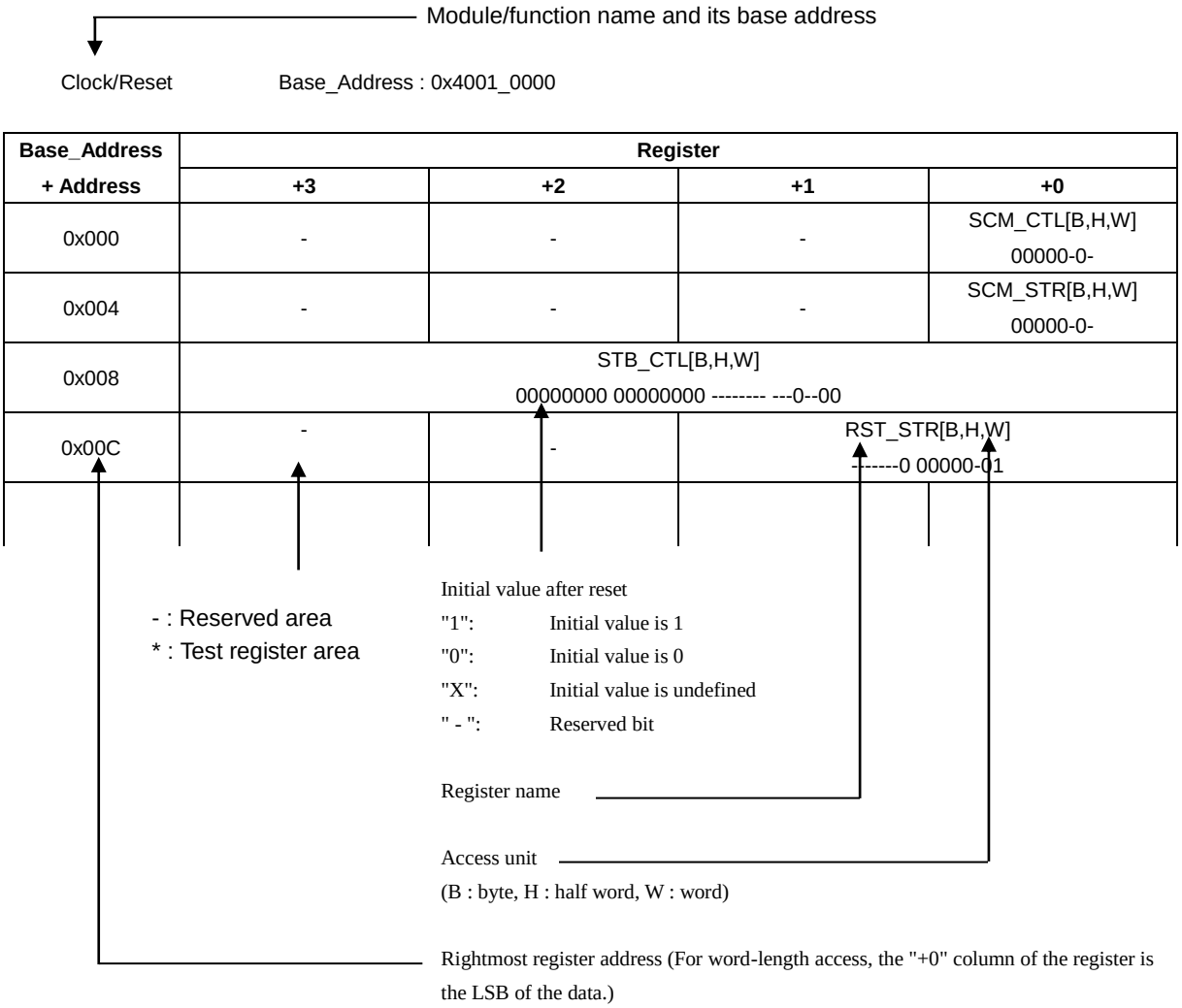
1. **Register Map**
   - 1.1 FLASH_IF
   - 1.2 Unique ID
   - 1.3 ECC Capture Address
   - 1.4 Clock/Reset
   - 1.5 HW WDT
   - 1.6 SW WDT
   - 1.7 Dual_Timer
   - 1.8 MFT
   - 1.9 PPG
   - 1.10 Base Timer
   - 1.11 IO Selector for Base Timer
   - 1.12 QPRC
   - 1.13 QPRC NF
   - 1.14 A/DC
   - 1.15 CR Trim
   - 1.16 EXTI
   - 1.17 INT-Req. READ
   - 1.18 D/AC
   - 1.19 HDMI-CEC
   - 1.20 GPIO
   - 1.21 LVD
   - 1.22 DS_Mode
   - 1.23 USB Clock
   - 1.24 CAN_Prescaler
   - 1.25 MFS
   - 1.26 CRC
   - 1.27 Watch Counter
   - 1.28 RTC
   - 1.29 Low-speed CR Prescaler
   - 1.30 Peripheral Clock Gating
   - 1.31 Smart Card Interface
   - 1.32 MFSI2S
   - 1.33 I2S Prescaler
   - 1.34 GDC_Prescaler
   - 1.35 EXT-Bus I/F
   - 1.36 USB

1.37 DMAC
1.38 DSTC
1.39 CAN
1.40 Ethernet-MAC
1.41 Ethernet-Control
1.42 I2S
1.43 SD-Card
1.44 CAN FD
1.45 Programmable-CRC
1.46 WorkFlash_IF
1.47 High-Speed Quad SPI Controller
1.48 HyperBus Interface
1.49 GDC Sub System Controller
1.50 GDC Sub System SDRAM Controller

1. Register Map

Register map is shown on the table every module/function.

[How to read the each table]



Notes:

- *The register table is represented in the little-endian.*
- *When performing a data access, the addresses should be as below according to the access size.*
- *Word access: Address should be multiples of 4 (least significant 2 bits should be 0x00)*
- *Half word access: Address should be multiples of 2 (least significant bit should be 0x0)*
- *Byte access: -*
- *Do not access the test register area.*
- *Do not access the area that is not written in the register table.*
- *When the register is accessed by larger unit than register size, for the reserved area to access at the same time, the read value is undefined, and writing is invalid.*

1.1 FLASH_IF

1.1.1 TYPE1-M4, TYPE2-M4 Products

FLASH_IF Base_Address : 0x4000_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	FASZR[B,H,W]			
0x004	FRWTR[B,H,W]			
0x008	FSTR[B,H,W]			
0x00C	*			
0x010	FSYNDN[B,H,W]			
0x014	FBFCR[B,H,W]			
0x018 - 0x01C	-	-	-	-
0x020	FICR[B,H,W]			
0x024	FISR[B,H,W]			
0x028	FICLR[B,H,W]			
0x02C - 0x0FC	-	-	-	-
0x100	CRTRMM[B,H,W]			
0x104 - 0x1FC	-	-	-	-

Note:

- *For details of Flash I/F registers, see Flash Programming Manual of the product used.*

1.1.2 TYPE3-M4 Product

FLASH_IF Base_Address : 0x4000_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	FASZR[B,H,W]			
0x004	FRWTR[B,H,W]			
0x008	FSTR[B,H,W]			
0x00C	*			
0x010	FSYNDN[B,H,W]			
0x014	FBFCR[B,H,W]			
0x018 - 0x01C	-	-	-	-
0x020	FICR[B,H,W]			
0x024	FISR[B,H,W]			
0x028	FICLR[B,H,W]			
0x02C	-	-	-	-
0x030	DFCTRLR[W]			
0x034 - 0x0FC	-	-	-	-
0x100	CRTRMM[B,H,W]			
0x104 - 0x10C	-	-	-	-
0x110	FGPDM1[B,H,W]			
0x114	FGPDM2[B,H,W]			
0x118	FGPDM3[B,H,W]			
0x11C	FGPDM4[B,H,W]			
0x120 - 0x1FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x400	DFASZR[B,H,W]			
0x404	DFRWTR[B,H,W]			
0x408	DFSTR[B,H,W]			
0x40C - 0x4FC	-	-	-	-

Note:

- *For details of Flash I/F registers, see Flash Programming Manual of the product used.*

1.1.3 TYPE4-M4, TYPE5-M4, TYPE6-M4 Products

FLASH_IF Base_Address : 0x4000_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	FASZR[B,H,W]			
0x004	FRWTR[B,H,W]			
0x008	FSTR[B,H,W]			
0x00C	*			
0x010	FSYNDN[B,H,W]			
0x014	FBFCR[B,H,W]			
0x018 - 0x01C	-	-	-	-
0x020	FICR[B,H,W]			
0x024	FISR[B,H,W]			
0x028	FICLR[B,H,W]			
0x02C - 0x0FC	-	-	-	-
0x100	CRTRMM[B,H,W]			
0x104 - 0x10C	-	-	-	-
0x110	FGPDM1[B,H,W]			
0x114	FGPDM2[B,H,W]			
0x118	FGPDM3[B,H,W]			
0x11C	FGPDM4[B,H,W]			
0x120 - 0x1FC	-			

Note:

- *For details of Flash I/F registers, see Flash Programming Manual of the product used.*

1.2 Unique ID

Unique ID Base_Address : 0x4000_0200

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	UIDR0[W] XXXXXXXX XXXXXXXX XXXXXXXX XXXX----			
0x004	UIDR1[W]			
	-------- -------- ---XXXXX XXXXXXXX			
0x008 - 0xDFC	-	-	-	-

1.3 ECC Capture Address

ECC Capture Address Base_Address : 0x4000_0300

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	FERRAD[W] -------- -XXXXXXX XXXXXXXX XXXXXXXX			
0x004 - 0xFFC	-	-	-	-

1.4 Clock/Reset

1.4.1 TYPE1-M4, TYPE2-M4 Products

Clock/Reset Base_Address : 0x4001_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	SCM_CTL[W] 00000-0-
0x004	-	-	-	SCM_STR[W] 00000-0-
0x008	STB_CTL[W] 00000000 00000000 -------- ---0-000			
0x00C	-	-	RST_STR[W] -------0 0000--01	
0x010	-	-	-	BSC_PSR[W] -----000
0x014	-	-	-	APBC0_PSR[W] ------00
0x018	-	-	-	APBC1_PSR[W] 1--0--00
0x01C	-	-	-	APBC2_PSR[W] 1--0--00
0x020	-	-	-	SWC_PSR[W] ------00
0x024 – 0x027	-	-	-	-
0x028	-	-	-	TTC_PSR[W] ------00
0x02C – 0x02F	-	-	-	-
0x030	-	-	-	CSW_TMR[W] 00000000
0x034	-	-	-	PSW_TMR[W] ---0-000
0x038	-	-	-	PLL_CTL1[W] 00000000
0x03C	-	-	-	PLL_CTL2[W] --000000
0x040	-	-	CSV_CTL[W] -111--00 ------11	
0x044	-	-	-	CSV_STR[W] ------00
0x048	-	-	FCSWH_CTL[W] 11111111 11111111	
0x04C	-	-	FCSWL_CTL[W] 00000000 00000000	

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
0x050	-	-	FCSWD_CTL[W] 00000000 00000000	
0x054	-	-	-	DBWDT_CTL[W] 0-0-----
0x058	-	-	-	*
0x05C - 0x05F	-	-	-	-
0x060	-	-	-	INT_ENR[W] --0--000
0x064	-	-	-	INT_STR[W] --0–000
0x068	-	-	-	INT_CLR[W] --0--000
0x06C – 0xFFC	-	-	-	-

1.4.2 TYPE3-M4, TYPE4-M4, TYPE5-M4, TYPE6-M4 Products

Clock/Reset Base_Address : 0x4001_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	SCM_CTL[W] 00000-0-
0x004	-	-	-	SCM_STR[W] 00000-0-
0x008	STB_CTL[W] 00000000 00000000 -------- ---0-000			
0x00C	-	-	RST_STR[W] -------0 0000--01	
0x010	-	-	-	BSC_PSR[W] -----000
0x014	-	-	-	APBC0_PSR[W] ------00
0x018	-	-	-	APBC1_PSR[W] 1--0--00
0x01C	-	-	-	APBC2_PSR[W] 1--0--00
0x020	-	-	-	SWC_PSR[W] ------00
0x024 – 0x027	-	-	-	-
0x028	-	-	-	TTC_PSR[W] ------00
0x02C – 0x02F	-	-	-	-
0x030	-	-	-	CSW_TMR[W] 00000000
0x034	-	-	-	PSW_TMR[W] ---0-000
0x038	-	-	-	PLL_CTL1[W] 00000000
0x03C	-	-	-	PLL_CTL2[W] --000000
0x040	-	-	CSV_CTL[W] -111--00 ------11	
0x044	-	-	-	CSV_STR[W] ------00
0x048	-	-	FCSWH_CTL[W] 11111111 11111111	
0x04C	-	-	FCSWL_CTL[W] 00000000 00000000	

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
0x050	-	-	FCSWD_CTL[W] 00000000 00000000	
0x054	-	-	-	DBWDT_CTL[W] 0-0-----
0x058	-	-	-	*
0x05C - 0x05F	-	-	-	-
0x060	-	-	-	INT_ENR[W] --0--000
0x064	-	-	-	INT_STR[W] --0–000
0x068	-	-	-	INT_CLR[W] --0--000
0x06C – 0x070	-	-	-	-
0x074	PLLCG_CTL[W] -------- 11111111 00000000 00----00			
0x078 – 0xFFC	-	-	-	-

1.5 HW WDT

HW WDT Base_Address : 0x4001_1000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	WDG_LDR[W] 00000000 00000000 11111111 11111111			
0x004	WDG_VLR[W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x008	-	-	-	WDG_CTL[W] ------11
0x00C	-	-	-	WDG_ICL[W] XXXXXXXX
0x010	-	-	-	WDG_RIS[W] -------0
0x014	*			
0x018 – 0xBFC	-	-	-	-
0xC00	WDG_LCK[W] 00000000 00000000 00000000 00000001			
0xC04 – 0xFFC	-	-	-	-

1.6 SW WDT

SW WDT Base_Address : 0x4001_2000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	WdogLoad[W] 11111111 11111111 11111111 11111111			
0x004	WdogValue[W] 11111111 11111111 11111111 11111111			
0x008	-	-	-	WdogControl[W] ---00000
0x00C	WdogIntClr[W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x010	-	-	-	WdogRIS[W] -------0
0x014	*			
0x018	-	-	-	WdogSPMC[W] -------0
0x01C – 0xBFC	-	-	-	-
0xC00	WdogLock[W] 00000000 00000000 00000000 00000000			
0xC04 - 0xDFC	-	-	-	-
0xF00 - 0xF04	*			
0xF08 - 0xFDF	-	-	-	-
0xFE0 - 0xFFC	*			

1.7 Dual_Timer

Dual_Timer Base_Address : 0x4001_5000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	Timer1Load[W] 00000000 00000000 00000000 00000000			
0x004	Timer1Value[W] 11111111 11111111 11111111 11111111			
0x008	Timer1Control[W] -------- -------- -------- 00100000			
0x00C	Timer1IntClr[W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x010	Timer1RIS[W] -------- -------- -------- -------0			
0x014	Timer1MIS[W] -------- -------- -------- -------0			
0x018	Timer1BGLoad[W] 00000000 00000000 00000000 00000000			
0x020	Timer2Load[W] 00000000 00000000 00000000 00000000			
0x024	Timer2Value[W] 11111111 11111111 11111111 11111111			
0x028	Timer2Control[W] -------- -------- -------- 00100000			
0x02C	Timer2IntClr[W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x030	Timer2RIS[W] -------- -------- -------- -------0			
0x034	Timer2MIS[W] -------- -------- -------- -------0			
0x038	Timer2BGLoad[W] 00000000 00000000 00000000 00000000			
0x040 - 0xFFC	-	-	-	-

1.8 MFT

1.8.1 TYPE1-M4, TYPE2-M4 Products

MFT unit0 Base_Address : 0x4002_0000

MFT unit1 Base_Address : 0x4002_1000

MFT unit2 Base_Address : 0x4002_2000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x100	OCCP0[H,W] 00000000 00000000		-	-
0x104	OCCP1[H,W] 00000000 00000000		-	-
0x108	OCCP2[H,W] 00000000 00000000		-	-
0x10C	OCCP3[H,W] 00000000 00000000		-	-
0x110	OCCP4[H,W] 00000000 00000000		-	-
0x114	OCCP5[H,W] 00000000 00000000		-	-
0x118	-	OCSD10[B,H,W] 00000000	OCSB10[B,H,W] 00000000	OCSA10[B,H,W] 00000000
0x11C	-	OCSD32[B,H,W] 00000000	OCSB32[B,H,W] 00000000	OCSA32[B,H,W] 00000000
0x120	-	OCSD54[B,H,W] 00000000	OCSB54[B,H,W] 00000000	OCSA54[B,H,W] 00000000
0x124	-	-	OCSC[B,H,W] --000000	-
0x128	-	-	OCSE0[B,H,W] 00000000 00000000	
0x12C	OCSE1[B,H,W] 00000000 00000000 00000000 00000000			
0x130	-	-	OCSE2[B,H,W] 00000000 00000000	
0x134	OCSE3[B,H,W] 00000000 00000000 00000000 00000000			
0x138	-	-	OCSE4[B,H,W] 00000000 00000000	
0x13C	OCSE5[B,H,W] 00000000 00000000 00000000 00000000			
0x140	TCCP0[H,W] 11111111 11111111		-	-
0x144	TCDT0[H,W] 00000000 00000000		-	-
0x148	TCSC0[H,W] 00000000 00000000		TCSA0[B,H,W] 00000000 01000000	
0x14C	TCCP1[H,W] 11111111 11111111		-	-

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
0x150	TCDT1[H,W] 00000000 00000000		-	-
0x154	TCSC1[H,W] 00000000 00000000		TCSA1[B,H,W] 00000000 01000000	
0x158	TCCP2[H,W] 11111111 11111111		-	-
0x15C	TCDT2[H,W] 00000000 00000000		-	-
0x160	TCSC2[H,W] 00000000 00000000		TCSA2[B,H,W] 00000000 01000000	
0x164	TCAL[W] 00000000 00000000 11111111 11111111 *1			
	-	-	-	- *2
	*1 MFT unit0 *2 MFT unit1,unit2			
0x168	-	OCFS54[B,H,W] 00000000	OCFS32[B,H,W] 00000000	OCFS10[B,H,W] 00000000
0x16C	-	-	ICFS32[B,H,W] 00000000	ICFS10[B,H,W] 00000000
0x170	-	ACFS54[B,H,W] 00000000	ACFS32[B,H,W] 00000000	ACFS10[B,H,W] 00000000
0x174	ICCP0[H,W] 00000000 00000000		-	-
0x178	ICCP1[H,W] 00000000 00000000		-	-
0x17C	ICCP2[H,W] 00000000 00000000		-	-
0x180	ICCP3[H,W] 00000000 00000000		-	-
0x184	-	-	ICSB10[B,H,W] ------00	ICSA10[B,H,W] 00000000
0x188			ICSB32[B,H,W] ------00	ICSA32[B,H,W] 00000000
0x18C	WFTF10[H,W] 00000000 00000000		-	-
0x190	WFTB10[H,W] 00000000 00000000		WFTA10[H,W] 00000000 00000000	
0x194	WFTF32[H,W] 00000000 00000000		-	-
0x198	WFTB32[H,W] 00000000 00000000		WFTA32[H,W] 00000000 00000000	
0x19C	WFTF54[H,W] 00000000 00000000		-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x1A0	WFTB54[H,W] 00000000 00000000		WFTA54[H,W] 00000000 00000000	
0x1A4	-		-	WFSA10[B,H,W] --000000 000000
0x1A8	-		-	WFSA32[B,H,W] --000000 000000
0x1AC	-		-	WFSA54[B,H,W] --000000 000000
0x1B0	-		-	WFIR[H,W] 00000000 00000000
0x1B4	-		-	NZCL[H,W] 00000000 00000000
0x1B8	ACMP0[H,W] 00000000 00000000		-	-
0x1BC	ACMP1[H,W] 00000000 00000000		-	-
0x1C0	ACMP2[H,W] 00000000 00000000		-	-
0x1C4	ACMP3[H,W] 00000000 00000000		-	-
0x1C8	ACMP4[H,W] 00000000 00000000		-	-
0x1CC	ACMP5[H,W] 00000000 00000000		-	-
0x1D0	-	-	ACSA[B,H,W] 00000000 00000000	
0x1D4	-	-	ACSD0[B,H,W] 00000000	ACSC0[B,H,W] 00000000
0x1D8	-	-	ACSD1[B,H,W] 00000000	ACSC1[B,H,W] 00000000
0x1DC	-	-	ACSD2[B,H,W] 00000000	ACSC2[B,H,W] 00000000
0x1E0	-	-	ACSD3[B,H,W] 00000000	ACSC3[B,H,W] 00000000
0x1E4	-	-	ACSD4[B,H,W] 00000000	ACSC4[B,H,W] 00000000
0x1E8	-	-	ACSD5[B,H,W] 00000000	ACSC5[B,H,W] 00000000
0x1EC-0xFFC	-	-	-	-

1.8.2 TYPE3-M4, TYPE4-M4, TYPE5-M4, TYPE6-M4 Products

MFT unit0 **Base_Address : 0x4002_0000**

MFT unit1 **Base_Address : 0x4002_1000**

MFT unit2 **Base_Address : 0x4002_2000**

Base_Address + Address	Register			
	+3	+2	+1	+0
0x100	OCCP0[H,W] 00000000 00000000		-	-
0x104	OCCP1[H,W] 00000000 00000000		-	-
0x108	OCCP2[H,W] 00000000 00000000		-	-
0x10C	OCCP3[H,W] 00000000 00000000		-	-
0x110	OCCP4[H,W] 00000000 00000000		-	-
0x114	OCCP5[H,W] 00000000 00000000		-	-
0x118	OCSD10[B,H,W] --000000 00000000		OCSB10[B,H,W] 00000000	OCSA10[B,H,W] 00000000
0x11C	OCSD32[B,H,W] --000000 00000000		OCSB32[B,H,W] 00000000	OCSA32[B,H,W] 00000000
0x120	OCSD54[B,H,W] --000000 00000000		OCSB54[B,H,W] 00000000	OCSA54[B,H,W] 00000000
0x124	-	-	OCSC[B,H,W] --000000	-
0x128	-	-	OCSE0[B,H,W] 00000000 00000000	
0x12C	OCSE1[B,H,W] 00000000 00000000 00000000 00000000			
0x130	-	-	OCSE2[B,H,W] 00000000 00000000	
0x134	OCSE3[B,H,W] 00000000 00000000 00000000 00000000			
0x138	-	-	OCSE4[B,H,W] 00000000 00000000	
0x13C	OCSE5[B,H,W] 00000000 00000000 00000000 00000000			
0x140	TCCP0[H,W] 11111111 11111111		-	-
0x144	TCDT0[H,W] 00000000 00000000		-	-
0x148	TCSC0[H,W] 00000000 00000000		TCSA0[B,H,W] 00000000 01000000	
0x14C	TCCP1[H,W] 11111111 11111111		-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x150	TCDT1[H,W] 00000000 00000000		-	-
0x154	TCSC1[H,W] 00000000 00000000		TCSA1[B,H,W] 00000000 01000000	
0x158	TCCP2[H,W] 11111111 11111111		-	-
0x15C	TCDT2[H,W] 00000000 00000000		-	-
0x160	TCSC2[H,W] 00000000 00000000		TCSA2[B,H,W] 00000000 01000000	
0x164	TCAL[W] 00000000 00000000 11111111 11111111 *1			
	-	-	-	- *2
	*1 MFT unit0 *2 MFT unit1,unit2			
0x168	-	OCFS54[B,H,W] 00000000	OCFS32[B,H,W] 00000000	OCFS10[B,H,W] 00000000
0x16C	-	-	ICFS32[B,H,W] 00000000	ICFS10[B,H,W] 00000000
0x170	-	ACFS54[B,H,W] 00000000	ACFS32[B,H,W] 00000000	ACFS10[B,H,W] 00000000
0x174	ICCP0[H,W] 00000000 00000000		-	-
0x178	ICCP1[H,W] 00000000 00000000		-	-
0x17C	ICCP2[H,W] 00000000 00000000		-	-
0x180	ICCP3[H,W] 00000000 00000000		-	-
0x184	-	-	ICSB10[B,H,W] ------00	ICSA10[B,H,W] 00000000
0x188			ICSB32[B,H,W] ------00	ICSA32[B,H,W] 00000000
0x18C	WFTF10[H,W] 00000000 00000000		-	-
0x190	WFTB10[H,W] 00000000 00000000		WFTA10[H,W] 00000000 00000000	
0x194	WFTF32[H,W] 00000000 00000000		-	-
0x198	WFTB32[H,W] 00000000 00000000		WFTA32[H,W] 00000000 00000000	
0x19C	WFTF54[H,W] 00000000 00000000		-	-

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
0x1A0	WFTB54[H,W] 00000000 00000000		WFTA54[H,W] 00000000 00000000	
0x1A4	-	-	WFSA10[B,H,W] --000000 000000	
0x1A8	-	-	WFSA32[B,H,W] --000000 000000	
0x1AC	-	-	WFSA54[B,H,W] --000000 000000	
0x1B0	-	-	WFIR[H,W] 00000000 00000000	
0x1B4	-	-	NZCL[H,W] 00000000 00000000	
0x1B8	ACMP0[H,W] 00000000 00000000		-	-
0x1BC	ACMP1[H,W] 00000000 00000000		-	-
0x1C0	ACMP2[H,W] 00000000 00000000		-	-
0x1C4	ACMP3[H,W] 00000000 00000000		-	-
0x1C8	ACMP4[H,W] 00000000 00000000		-	-
0x1CC	ACMP5[H,W] 00000000 00000000		-	-
0x1D0	-	-	ACSA[B,H,W] 00000000 00000000	
0x1D4	-	ACMC0[B,H,W] 00--0000	ACSD0[B,H,W] 00000000	ACSC0[B,H,W] 00000000
0x1D8	-	ACMC1[B,H,W] 00--0000	ACSD1[B,H,W] 00000000	ACSC1[B,H,W] 00000000
0x1DC	-	ACMC2[B,H,W] 00--0000	ACSD2[B,H,W] 00000000	ACSC2[B,H,W] 00000000
0x1E0	-	ACMC3[B,H,W] 00--0000	ACSD3[B,H,W] 00000000	ACSC3[B,H,W] 00000000
0x1E4	-	ACMC4[B,H,W] 00--0000	ACSD4[B,H,W] 00000000	ACSC4[B,H,W] 00000000
0x1E8	-	ACMC5[B,H,W] 00--0000	ACSD5[B,H,W] 00000000	ACSC5[B,H,W] 00000000
0x1EC	-	-	-	TCSD[B,H,W] ------00
0x1F0-0xFFC	-	-	-	-

1.9 PPG

PPG Base_Address : 0x4002_4000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	TTCR0 [B,H,W] 11110000	-
0x004	-	-	-	*
0x008	-	-	COMP0 [B,H,W] 00000000	-
0x00C	-	-	-	COMP2 [B,H,W] 00000000
0x010	-	-	COMP4 [B,H,W] 00000000	-
0x014	-	-	-	COMP6 [B,H,W] 00000000
0x018 - 0x01C	-	-	-	-
0x020	-	-	TTCR1 [B,H,W] 11110000	-
0x024	-	-	-	*
0x028	-	-	COMP1 [B,H,W] 00000000	-
0x02C	-	-	-	COMP3 [B,H,W] 00000000
0x030	-	-	COMP5 [B,H,W] 00000000	-
0x034	-	-	-	COMP7 [B,H,W] 00000000
0x038 - 0x03C	-	-	-	-
0x040	-	-	TTCR2 [B,H,W] 11110000	-
0x044	-	-	-	*
0x048	-	-	COMP8 [B,H,W] 00000000	-
0x04C	-	-	-	COMP10 [B,H,W] 00000000
0x050	-	-	COMP12 [B,H,W] 00000000	-
0x054	-	-	-	COMP14 [B,H,W] 00000000
0x058 - 0x0FC	-	-	-	-
0x100	-	-	TRG0 [B,H,W] 00000000 00000000	
0x104	-	-	REVC0 [B,H,W] 00000000 00000000	
0x108 - 0x13C	-	-	-	-
0x140	-	-	TRG1 [B,H,W] -------- 00000000	
0x144	-	-	REVC1 [B,H,W] -------- 00000000	
0x148 - 0x1FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x200	-	-	PPGC0 [B,H,W] 00000000	PPGC1 [B,H,W] 00000000
0x204	-	-	PPGC2 [B,H,W] 00000000	PPGC3 [B,H,W] 00000000
0x208	-	-	PRLH0 [B,H,W] XXXXXXXX	PRLL0 [B,H,W] XXXXXXXX
0x20C	-	-	PRLH1 [B,H,W] XXXXXXXX	PRLL1 [B,H,W] XXXXXXXX
0x210	-	-	PRLH2 [B,H,W] XXXXXXXX	PRLL2 [B,H,W] XXXXXXXX
0x214	-	-	PRLH3 [B,H,W] XXXXXXXX	PRLL3 [B,H,W] XXXXXXXX
0x218	-	-	-	GATEC0 [B,H,W] --00---00
0x21C - 0x23C	-	-	-	-
0x240	-	-	PPGC4 [B,H,W] 00000000	PPGC5 [B,H,W] 00000000
0x244	-	-	PPGC6 [B,H,W] 00000000	PPGC7 [B,H,W] 00000000
0x248	-	-	PRLH4 [B,H,W] XXXXXXXX	PRLL4 [B.H.W] XXXXXXXX
0x24C	-	-	PRLH5 [B,H,W] XXXXXXXX	PRLL5 [B,H,W] XXXXXXXX
0x250	-	-	PRLH6 [B,H,W] XXXXXXXX	PRLL6 [B,H,W] XXXXXXXX
0x254	-	-	PRLH7 [B,H,W] XXXXXXXX	PRLL7 [B,H,W] XXXXXXXX
0x258	-	-	-	GATEC4 [B,H,W] ------00
0x25C - 0x27C	-	-	-	-
0x280	-	-	PPGC8 [B,H,W] 00000000	PPGC9 [B,H,W] 00000000
0x284	-	-	PPGC10 [B,H,W] 00000000	PPGC11 [B,H,W] 00000000
0x288	-	-	PRLH8 [B,H,W] XXXXXXXX	PRLL8 [B,H,W] XXXXXXXX
0x28C	-	-	PRLH9 [B,H,W] XXXXXXXX	PRLL9 [B,H,W] XXXXXXXX
0x290	-	-	PRLH10 [B,H,W] XXXXXXXX	PRLL10 [B,H,W] XXXXXXXX
0x294	-	-	PRLH11 [B,H,W] XXXXXXXX	PRLL11 [B,H,W] XXXXXXXX
0x298	-	-	-	GATEC8 [B,H,W] --00--00
0x29C - 0x2BC	-	-	-	-
0x2C0	-	-	PPGC12 [B,H,W] 00000000	PPGC13 [B,H,W] 00000000
0x2C4	-	-	PPGC14 [B,H,W] 00000000	PPGC15 [B,H,W] 00000000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x2C8	-	-	PRLH12 [B,H,W] XXXXXXXX	PRLL12 [B,H,W] XXXXXXXX
0x2CC	-	-	PRLH13 [B,H,W] XXXXXXXX	PRLL13 [B,H,W] XXXXXXXX
0x2D0	-	-	PRLH14 [B,H,W] XXXXXXXX	PRLL14 [B,H,W] XXXXXXXX
0x2D4	-	-	PRLH15 [B,H,W] XXXXXXXX	PRLL15 [B,H,W] XXXXXXXX
0x2D8	-	-	-	GATEC12 [B,H,W] ------00
0x2DC - 0x2FC	-	-	-	-
0x300	-	-	PPGC16 [B,H,W] 00000000	PPGC17 [B,H,W] 00000000
0x304	-	-	PPGC18 [B,H,W] 00000000	PPGC19 [B,H,W] 00000000
0x308	-	-	PRLH16 [B,H,W] XXXXXXXX	PRLL16 [B,H,W] XXXXXXXX
0x30C	-	-	PRLH17 [B,H,W] XXXXXXXX	PRLL17 [B,H,W] XXXXXXXX
0x310	-	-	PRLH18 [B,H,W] XXXXXXXX	PRLL18 [B,H,W] XXXXXXXX
0x314	-	-	PRLH19 [B,H,W] XXXXXXXX	PRLL19 [B,H,W] XXXXXXXX
0x318	-	-	-	GATEC16 [B,H,W] --00---00
0x31C - 0x33C	-	-	-	-
0x340	-	-	PPGC20 [B,H,W] 00000000	PPGC21 [B,H,W] 00000000
0x344	-	-	PPGC22 [B,H,W] 00000000	PPGC23 [B,H,W] 00000000
0x348	-	-	PRLH20 [B,H,W] XXXXXXXX	PRLL20 [B.H.W] XXXXXXXX
0x34C	-	-	PRLH21 [B,H,W] XXXXXXXX	PRLL21 [B,H,W] XXXXXXXX
0x350	-	-	PRLH22 [B,H,W] XXXXXXXX	PRLL22 [B,H,W] XXXXXXXX
0x354	-	-	PRLH23 [B,H,W] XXXXXXXX	PRLL23 [B,H,W] XXXXXXXX
0x358	-	-	-	GATEC20 [B,H,W] ------00
0x35C - 0x37C	-	-	-	-
0x380	-	-	-	-
0x384 - 0xFFC	-	-	-	-

1.10 Base Timer

Base Timer ch.0 Base Address : 0x4002_5000
Base Timer ch.1 Base Address : 0x4002_5040
Base Timer ch.2 Base Address : 0x4002_5080
Base Timer ch.3 Base Address : 0x4002_50C0
Base Timer ch.4 Base Address : 0x4002_5200
Base Timer ch.5 Base Address : 0x4002_5240
Base Timer ch.6 Base Address : 0x4002_5280
Base Timer ch.7 Base Address : 0x4002_52C0
Base Timer ch.8 Base Address : 0x4002_5400
Base Timer ch.9 Base Address : 0x4002_5440
Base Timer ch.10 Base Address : 0x4002_5480
Base Timer ch.11 Base Address : 0x4002_54C0
Base Timer ch.12 Base Address : 0x4002_5600
Base Timer ch.13 Base Address : 0x4002_5640
Base Timer ch.14 Base Address : 0x4002_5680
Base Timer ch.15 Base Address : 0x4002_56C0

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	PCSR/PRLL [H,W] XXXXXXXX XXXXXXXX	
0x004	-	-	PDUT/PRLH/DTBF [H,W] XXXXXXXX XXXXXXXX	
0x008	-	-	TMR [H,W] 00000000 00000000	
0x00C	-	-	TMCR [B,H,W] -0000000 00000000	
0x010	-	-	TMCR2 [B,H,W] 0------0	STC [B,H,W] 0000-000
0x014 - 0x03C	-	-	-	-

1.11 IO Selector for Base Timer

IO Selector for ch.0-ch.3 (Base Timer) Base Address : 0x4002_5100

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	BTSEL0123 [B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

IO Selector for ch.4-ch.7(Base Timer)Base Address : 0x4002_5300

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	BTSEL4567 [B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

IO Selector for ch.8-ch.11(Base Timer) Base Address : 0x4002_5500

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	BTSEL89AB [B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

IO Selector for ch.12-ch.15(Base Timer) Base Address : 0x4002_5700

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	BTSELCDEF [B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

Software-based Simultaneous Startup(Base Timer) Base Address : 0x4002_5F00

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000 - 0x0FB	-	-	-	-
0x0FC	-	-	BTSSSR [B,H,W] XXXXXXXX XXXXXXXX	

1.12 QPRC

1.12.1 TYPE1-M4, TYPE2-M4, TYPE6-M4 Products

QPRC ch.0 **Base Address : 0x4002_6000**

QPRC ch.1 **Base Address : 0x4002_6040**

QPRC ch.2 **Base Address : 0x4002_6080**

QPRC ch.3 **Base Address : 0x4002_60C0**

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0000	-	-	QPCR [H,W] 00000000 00000000	
0x0004	-	-	QRCR [H,W] 00000000 00000000	
0x0008	-	-	QPCCR [H,W] 00000000 00000000	
0x000C	-	-	QPRCR [H,W] 00000000 00000000	
0x0010	-	-	QMPR [H,W] 11111111 11111111	
0x0014	-	-	QICRH [B,H,W] --000000	QICRL [B,H,W] 00000000
0x0018	-	-	QCRH [B,H,W] 00000000	QCRL [B,H,W] 00000000
0x001C	-	-	QECR [B,H,W] -------- -----000	
0x0020 - 0x003B	-	-	-	-
0x003C	QPCRR[B,H,W] 00000000 00000000		QRCRR[B,H,W] 00000000 00000000	

1.12.2 TYPE3-M4, TYPE4-M4, TYPE5-M4 Products

QPRC ch.0 **Base Address : 0x4002_6000**

QPRC ch.1 **Base Address : 0x4002_6040**

QPRC ch.2 **Base Address : 0x4002_6080**

QPRC ch.3 **Base Address : 0x4002_60C0**

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0000	-	-	QPCR [H,W] 00000000 00000000	
0x0004	-	-	QRCR [H,W] 00000000 00000000	
0x0008	-	-	QPCCR [H,W] 00000000 00000000	
0x000C	-	-	QPRCR [H,W] 00000000 00000000	
0x0010	-	-	QMPR [H,W] 11111111 11111111	
0x0014	-	-	QICRH [B,H,W] --000000	QICRL [B,H,W] 00000000
0x0018	-	-	QCRH [B,H,W] 00000000	QCRL [B,H,W] 00000000
0x001C	-	-	QECR [B,H,W] -------- ----0000	
0x0020 - 0x003B	-	-	-	-
0x003C	QPCRR[B,H,W] 00000000 00000000		QRCRR[B,H,W] 00000000 00000000	

1.13 QPRC NF

QPRC ch.0 NF Base Address : 0x4002_6100

QPRC ch.1 NF Base Address : 0x4002_6110

QPRC ch.2 NF Base Address : 0x4002_6120

QPRC ch.3 NF Base Address : 0x4002_6130

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0000	-	-	-	NFCTLA[B,H,W] --00-000
0x0004	-	-	-	NFCTLB[B,H,W] --00-000
0x0008	-	-	-	NFCTLZ[B,H,W] --00-000
0x000C	-	-	-	-

1.14 A/DC

12bit A/DC unit0 Base_Address : 0x4002_7000

12bit A/DC unit1 Base_Address : 0x4002_7100

12bit A/DC unit2 Base_Address : 0x4002_7200

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	ADCR[B,H,W] 000-0000	ADSR[B,H,W] 00---000
0x004	-	-	-	*
0x008	-	-	SCCR[B,H,W] 1000-000	SFNS[B,H,W] ----0000
0x00C	SCFD[B,H,W] XXXXXXXX XXXX---- ---1--XX ---XXXXX			
0x010	-	-	SCIS3[B,H,W] 00000000	SCIS2[B,H,W] 00000000
0x014	-	-	SCIS1[B,H,W] 00000000	SCIS0[B,H,W] 00000000
0x018	-	-	PCCR[B,H,W] 10000000	PFNS[B,H,W] --XX--00
0x01C	PCFD[B,H,W] XXXXXXXX XXXX---- ---1-XXX ---XXXXX			
0x020	-	-	-	PCIS[B,H,W] 00000000
0x024	CMPD[B,H,W] 00000000 00------		-	CMPCR[B,H,W] 00000000
0x028	-	-	ADSS3[B,H,W] 00000000	ADSS2[B,H,W] 00000000
0x02C	-	-	ADSS1[B,H,W] 00000000	ADSS0[B,H,W] 00000000
0x030	-	-	ADST0[B,H,W] 00010000	ADST1[B,H,W] 00010000
0x034	-	-	-	ADCT[B,H,W] 00000111
0x038	-	-	SCTSL[B,H,W] ----0000	PRTSL[B,H,W] ----0000
0x03C	-	-	ADCEN[B,H,W] 11111111 ------00	
0x040	CALSR[B,H,W] -------- -------- -------0 00000000			
0x044	-	-	-	WCMRCIF[B,H,W] 00000000
0x048	-	-	-	WCMRCOT [B,H,W] 00000000
0x04C	-	-	WCMPSR[B,H,W] 00000000	WCMPCR[B,H,W] 00100000
0x050	WCMPDH[B,H,W] 00000000 00000000		WCMPDL[B,H,W] 00000000 00000000	
0x040 - 0x0FC	-	-	-	-

1.15 CR Trim

CR Trim Base_Address : 0x4002_E000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	MCR_PSR[B,H,W] -----001
0x004	-	-	MCR_FTRM[B,H,W] ------01 11101111	
0x008	-	-	-	MCR_TTRM[B,H,W] ---10000
0x00C	MCR_RLR[W] 00000000 00000000 00000000 00000001			
0x010 - 0x0FC	-	-	-	-

1.16 EXTI

1.16.1 TYPE1-M4, TYPE2-M4, TYPE3-M4, TYPE4-M4 Products

EXTI Base_Address : 0x4003_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	ENIR[B,H,W] 00000000 00000000 00000000 00000000			
0x004	EIRR[B,H,W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x008	EICL[B,H,W] 11111111 11111111 11111111 11111111			
0x00C	ELVR[B,H,W] 00000000 00000000 00000000 00000000			
0x010	ELVR1[B,H,W] 00000000 00000000 00000000 00000000			
0x014	-	-	-	NMIRR[B,H,W] -------0
0x018	-	-	-	NMICL[B,H,W] -------1
0x01C	-	-	-	-
0x020 - 0x0FC	-	-	-	-

1.16.2 TYPE5-M4, TYPE6-M4 Products

EXTI Base_Address : 0x4003_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	ENIR[B,H,W] 00000000 00000000 00000000 00000000			
0x004	EIRR[B,H,W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x008	EICL[B,H,W] 11111111 11111111 11111111 11111111			
0x00C	ELVR[B,H,W] 00000000 00000000 00000000 00000000			
0x010	ELVR1[B,H,W] 00000000 00000000 00000000 00000000			
0x014	-	-	-	NMIRR[B,H,W] -------0
0x018	-	-	-	NMICL[B,H,W] -------1
0x01C	ELVR2[B,H,W] 00000000 00000000 00000000 00000000			
0x020 - 0x0FC	-	-	-	-

1.17 INT-Req. READ

1.17.1 TYPE1-M4, TYPE2-M4, TYPE6-M4 Products

INT-Req. READ Base_Address : 0x4003_1000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	DRQSEL[B,H,W] 00000000 00000000 00000000 00000000			
0x004 – 0x00C	-			
0x010	-	-	-	ODDPKS[B] ---00000
0x014	-	-	-	-
0x018	-	*	-	*
0x01C – 0x10C	-	-	-	-
0x110	IRQ003SEL[B,H,W] -------- 00000000 -------- 00000000			
0x114	IRQ004SEL[B,H,W] -------- 00000000 -------- 00000000			
0x118	IRQ005SEL[B,H,W] -------- 00000000 -------- 00000000			
0x11C	IRQ006SEL[B,H,W] -------- 00000000 -------- 00000000			
0x120	IRQ007SEL[B,H,W] -------- 00000000 -------- 00000000			
0x124	IRQ008SEL[B,H,W] -------- 00000000 -------- 00000000			
0x128	IRQ009SEL[B,H,W] -------- 00000000 -------- 00000000			
0x12C	IRQ010SEL[B,H,W] -------- 00000000 -------- 00000000			
0x130 – 0x1FC	-	-	-	-
0x200	EXC02MON[B,H,W] -------- -------- -------- ------00			
0x204	IRQ000MON[B,H,W] -------- -------- -------- -------0			
0x208	IRQ001MON[B,H,W] -------- -------- -------- -------0			
0x20C	IRQ002MON[B,H,W] -------- -------- -------- -------0			
0x210	IRQ003MON[B,H,W] -------- -------- -------- 00000000			
0x214	IRQ004MON[B,H,W] -------- -------- -------- 00000000			
0x218	IRQ005MON[B,H,W] -------- -------- -------- 00000000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x21C	IRQ006MON[B,H,W] -------- -------- -------- 00000000			
0x220	IRQ007MON[B,H,W] -------- -------- -------- 00000000			
0x224	IRQ008MON[B,H,W] -------- -------- -------- 00000000			
0x228	IRQ009MON[B,H,W] -------- -------- -------- 00000000			
0x22C	IRQ010MON[B,H,W] -------- -------- -------- 00000000			
0x230	IRQ011MON[B,H,W] -------- -------- -------- -------0			
0x234	IRQ012MON[B,H,W] -------- -------- -------- -------0			
0x238	IRQ013MON[B,H,W] -------- -------- -------- -------0			
0x23C	IRQ014MON[B,H,W] -------- -------- -------- -------0			
0x240	IRQ015MON[B,H,W] -------- -------- -------- -------0			
0x244	IRQ016MON[B,H,W] -------- -------- -------- -------0			
0x248	IRQ017MON[B,H,W] -------- -------- -------- -------0			
0x24C	IRQ018MON[B,H,W] -------- -------- -------- -------0			
0x250	IRQ019MON[B,H,W] -------- -------- -------- --000000			
0x254	IRQ020MON[B,H,W] -------- -------- -------- --000000			
0x258	IRQ021MON[B,H,W] -------- -------- -------- ----0000			
0x25C	IRQ022MON[B,H,W] -------- -------- -------- ----0000			
0x260	IRQ023MON[B,H,W] -------- -------- -------- ----0000			
0x264	IRQ024MON[B,H,W] -------- -------- -------- -----000			
0x268	IRQ025MON[B,H,W] -------- -------- -------- -----000			
0x26C	IRQ026MON[B,H,W] -------- -------- -------- ----0000			
0x270	IRQ027MON[B,H,W] -------- -------- -------- --000000			
0x274	IRQ028MON[B,H,W] -------- -------- -------- -----000			
0x278	IRQ029MON[B,H,W] -------- -------- -------- -----000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x27C	IRQ030MON[B,H,W] -------- -------- -------- ----0000			
0x280	IRQ031MON[B,H,W] -------- -------- -------- --000000			
0x284	IRQ032MON[B,H,W] -------- -------- -------- -----000			
0x288	IRQ033MON[B,H,W] -------- -------- -------- -----000			
0x28C	IRQ034MON[B,H,W] -------- -------- -------- ---00000			
0x290	IRQ035MON[B,H,W] -------- -------- -------- --000000			
0x294	IRQ036MON[B,H,W] -------- -------- -------- -----000			
0x298	IRQ037MON[B,H,W] -------- -------- -------- -----000			
0x29C	IRQ038MON[B,H,W] -------- -------- -------- -----000			
0x2A0	IRQ039MON[B,H,W] -------- -------- -------- ------00			
0x2A4	IRQ040MON[B,H,W] -------- -------- -------- ------00			
0x2A8	IRQ041MON[B,H,W] -------- -------- -------- ------00			
0x2AC	IRQ042MON[B,H,W] -------- -------- -------- ------00			
0x2B0	IRQ043MON[B,H,W] -------- -------- -------- ------00			
0x2B4	IRQ044MON[B,H,W] -------- -------- -------- ------00			
0x2B8	IRQ045MON[B,H,W] -------- -------- -------- ------00			
0x2BC	IRQ046MON[B,H,W] -------- -------- -------- ------00			
0x2C0	IRQ047MON[B,H,W] -------- -------- -------- ------00			
0x2C4	IRQ048MON[B,H,W] -------- -------- -------- -------0			
0x2C8	IRQ049MON[B,H,W] -------- -------- -------- -------0			
0x2CC	IRQ050MON[B,H,W] -------- -------- -------- -------0			
0x2D0	IRQ051MON[B,H,W] -------- -------- -------- -------0			
0x2D4	IRQ052MON[B,H,W] -------- -------- -------- -------0			
0x2D8	IRQ053MON[B,H,W] -------- -------- -------- -------0			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x2DC	IRQ054MON[B,H,W] -------- -------- -------- -------0			
0x2E0	IRQ055MON[B,H,W] -------- -------- -------- -------0			
0x2E4	IRQ056MON[B,H,W] -------- -------- -------- -------0			
0x2E8	IRQ057MON[B,H,W] -------- -------- -------- -------0			
0x2EC	IRQ058MON[B,H,W] -------- -------- -------- -------0			
0x2F0	IRQ059MON[B,H,W] -------- -------- -------- ----0000			
0x2F4	IRQ060MON[B,H,W] -------- -------- -------- -------0			
0x2F8	IRQ061MON[B,H,W] -------- -------- -------- ------00			
0x2FC	IRQ062MON[B,H,W] -------- -------- -------- -------0			
0x300	IRQ063MON[B,H,W] -------- -------- -------- ------00			
0x304	IRQ064MON[B,H,W] -------- -------- -------- -------0			
0x308	IRQ065MON[B,H,W] -------- -------- -------- ------00			
0x30C	IRQ066MON[B,H,W] -------- -------- -------- -------0			
0x310	IRQ067MON[B,H,W] -------- -------- -------- ------00			
0x314	IRQ068MON[B,H,W] -------- -------- -------- -------0			
0x318	IRQ069MON[B,H,W] -------- -------- -------- ------00			
0x31C	IRQ070MON[B,H,W] -------- -------- -------- -------0			
0x320	IRQ071MON[B,H,W] -------- -------- -------- ------00			
0x324	IRQ072MON[B,H,W] -------- -------- -------- -------0			
0x328	IRQ073MON[B,H,W] -------- -------- -------- ------00			
0x32C	IRQ074MON[B,H,W] -------- -------- -------- -------0			
0x330	IRQ075MON[B,H,W] -------- -------- -------- ------00			
0x334	IRQ076MON[B,H,W] -------- -------- -------- ---00000			
0x338	IRQ077MON[B,H,W] -------- -------- -------- ---00000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x33C	IRQ078MON[B,H,W] -------- -------- -------- ---00000			
0x340	IRQ079MON[B,H,W] -------- -------- -------- --000000			
0x344	IRQ080MON[B,H,W] -------- -------- -------- -------0			
0x348	IRQ081MON[B,H,W] -------- -------- -------- -------0			
0x34C	IRQ082MON[B,H,W] -------- -------- -------- -----000			
0x350	IRQ083MON[B,H,W] -------- -------- -------- -------0			
0x354	IRQ084MON[B,H,W] -------- -------- -------- -------0			
0x358	IRQ085MON[B,H,W] -------- -------- -------- -------0			
0x35C	IRQ086MON[B,H,W] -------- -------- -------- -------0			
0x360	IRQ087MON[B,H,W] -------- -------- -------- -------0			
0x364	IRQ088MON[B,H,W] -------- -------- -------- -------0			
0x368	IRQ089MON[B,H,W] -------- -------- -------- -------0			
0x36C	IRQ090MON[B,H,W] -------- -------- -------- -------0			
0x370	IRQ091MON[B,H,W] -------- -------- -------- ------00			
0x374	IRQ092MON[B,H,W] -------- -------- -------- ----0000			
0x378	IRQ093MON[B,H,W] -------- -------- -------- ----0000			
0x37C	IRQ094MON[B,H,W] -------- -------- -------- ----0000			
0x380	IRQ095MON[B,H,W] -------- -------- -------- ----0000			
0x384	IRQ096MON[B,H,W] -------- -------- -------- --000000			
0x388	IRQ097MON[B,H,W] -------- -------- -------- --000000			
0x38C	IRQ098MON[B,H,W] -------- -------- -------- ------00			
0x390	IRQ099MON[B,H,W] -------- -------- -------- ------00			
0x394	IRQ100MON[B,H,W] -------- -------- -------- ------00			
0x398	IRQ101MON[B,H,W] -------- -------- -------- ------00			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x39C	IRQ102MON[B,H,W] -------- -------- -------- ------00			
0x3A0	IRQ103MON[B,H,W] -------- -------- -------- -------0			
0x3A4	IRQ104MON[B,H,W] -------- -------- -------- ------00			
0x3A8	IRQ105MON[B,H,W] -------- -------- -------- -------0			
0x3AC	IRQ106MON[B,H,W] -------- -------- -------- ------00			
0x3B0	IRQ107MON[B,H,W] -------- -------- -------- -------0			
0x3B4	IRQ108MON[B,H,W] -------- -------- -------- ------00			
0x3B8	IRQ109MON[B,H,W] -------- -------- -------- -------0			
0x3BC	IRQ110MON[B,H,W] -------- -------- -------- ------00			
0x3C0	IRQ111MON[B,H,W] -------- -------- -------- ---00000			
0x3C4	-	-	-	-
0x3C8	IRQ113MON[B,H,W] -------- -------- -------- ---00000			
0x3CC	IRQ114MON[B,H,W] -------- -------- -------- --000000			
0x3D0 – 0x3D8	-	-	-	-
0x3DC	IRQ118MON[B,H,W] -------- -------- -------- ------00			
0x3E0	IRQ119MON[B,H,W] -------- -------- -------- -------0			
0x3E4	IRQ120MON[B,H,W] -------- -------- -------- -------0			
0x3E8	IRQ121MON[B,H,W] -------- -------- -------- ------00			
0x3EC	IRQ122MON[B,H,W] -------- -------- -------- -------0			
0x3F0	IRQ123MON[B,H,W] -------- -------- -------- ------00			
0x3F4	IRQ124MON[B,H,W] -------- -------- -------- -------0			
0x3F8	IRQ125MON[B,H,W] -------- -------- -------- ------00			
0x3FC	IRQ126MON[B,H,W] -------- -------- -------- -------0			
0x400	IRQ127MON[B,H,W] -------- -------- -------- ------00			
0x404 – 0xFFC	-	-	-	-

1.17.2 TYPE3-M4, TYPE5-M4 Product

INT-Req. READ Base_Address : 0x4003_1000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	DRQSEL[B,H,W] 00000000 00000000 00000000 00000000			
0x004 – 0x00C	-			
0x010	-	-	-	ODDPKS[B] ---00000
0x014	-	-	-	ODDPKS1[B] --00000
0x018	-	*	-	*
0x01C – 0x10C	-	-	-	-
0x110	IRQ003SEL[B,H,W] -------- 00000000 -------- 00000000			
0x114	IRQ004SEL[B,H,W] -------- 00000000 -------- 00000000			
0x118	IRQ005SEL[B,H,W] -------- 00000000 -------- 00000000			
0x11C	IRQ006SEL[B,H,W] -------- 00000000 -------- 00000000			
0x120	IRQ007SEL[B,H,W] -------- 00000000 -------- 00000000			
0x124	IRQ008SEL[B,H,W] -------- 00000000 -------- 00000000			
0x128	IRQ009SEL[B,H,W] -------- 00000000 -------- 00000000			
0x12C	IRQ010SEL[B,H,W] -------- 00000000 -------- 00000000			
0x130 – 0x1FC	-	-	-	-
0x200	EXC02MON[B,H,W] -------- -------- -------- ------00			
0x204	IRQ000MON[B,H,W] -------- -------- -------- -------0			
0x208	IRQ001MON[B,H,W] -------- -------- -------- -------0			
0x20C	IRQ002MON[B,H,W] -------- -------- -------- -------0			
0x210	IRQ003MON[B,H,W] -------- -------- -------- 00000000			
0x214	IRQ004MON[B,H,W] -------- -------- -------- 00000000			
0x218	IRQ005MON[B,H,W] -------- -------- -------- 00000000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x21C	IRQ006MON[B,H,W] -------- -------- -------- 00000000			
0x220	IRQ007MON[B,H,W] -------- -------- -------- 00000000			
0x224	IRQ008MON[B,H,W] -------- -------- -------- 00000000			
0x228	IRQ009MON[B,H,W] -------- -------- -------- 00000000			
0x22C	IRQ010MON[B,H,W] -------- -------- -------- 00000000			
0x230	IRQ011MON[B,H,W] -------- -------- -------- -------0			
0x234	IRQ012MON[B,H,W] -------- -------- -------- -------0			
0x238	IRQ013MON[B,H,W] -------- -------- -------- -------0			
0x23C	IRQ014MON[B,H,W] -------- -------- -------- -------0			
0x240	IRQ015MON[B,H,W] -------- -------- -------- -------0			
0x244	IRQ016MON[B,H,W] -------- -------- -------- -------0			
0x248	IRQ017MON[B,H,W] -------- -------- -------- -------0			
0x24C	IRQ018MON[B,H,W] -------- -------- -------- -------0			
0x250	IRQ019MON[B,H,W] -------- -------- -------- --000000			
0x254	IRQ020MON[B,H,W] -------- -------- -------- --000000			
0x258	IRQ021MON[B,H,W] -------- -------- -------- ----0000			
0x25C	IRQ022MON[B,H,W] -------- -------- -------- ----0000			
0x260	IRQ023MON[B,H,W] -------- -------- -------- ----0000			
0x264	IRQ024MON[B,H,W] -------- -------- -------- -----000			
0x268	IRQ025MON[B,H,W] -------- -------- -------- -----000			
0x26C	IRQ026MON[B,H,W] -------- -------- -------- ----0000			
0x270	IRQ027MON[B,H,W] -------- -------- -------- --000000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x274	IRQ028MON[B,H,W] -------- -------- -------- -----000			
0x278	IRQ029MON[B,H,W] -------- -------- -------- -----000			
0x27C	IRQ030MON[B,H,W] -------- -------- -------- ----0000			
0x280	IRQ031MON[B,H,W] -------- -------- -------- --000000			
0x284	IRQ032MON[B,H,W] -------- -------- -------- -----000			
0x288	IRQ033MON[B,H,W] -------- -------- -------- -----000			
0x28C	IRQ034MON[B,H,W] -------- -------- -------- ---00000			
0x290	IRQ035MON[B,H,W] -------- -------- -------- --000000			
0x294	IRQ036MON[B,H,W] -------- -------- -------- -----000			
0x298	IRQ037MON[B,H,W] -------- -------- -------- -----000			
0x29C	IRQ038MON[B,H,W] -------- -------- -------- -----000			
0x2A0	IRQ039MON[B,H,W] -------- -------- -------- ------00			
0x2A4	IRQ040MON[B,H,W] -------- -------- -------- ------00			
0x2A8	IRQ041MON[B,H,W] -------- -------- -------- ------00			
0x2AC	IRQ042MON[B,H,W] -------- -------- -------- ------00			
0x2B0	IRQ043MON[B,H,W] -------- -------- -------- ------00			
0x2B4	IRQ044MON[B,H,W] -------- -------- -------- ------00			
0x2B8	IRQ045MON[B,H,W] -------- -------- -------- ------00			
0x2BC	IRQ046MON[B,H,W] -------- -------- -------- ------00			
0x2C0	IRQ047MON[B,H,W] -------- -------- -------- ------00			
0x2C4	IRQ048MON[B,H,W] -------- -------- -------- -------0			
0x2C8	IRQ049MON[B,H,W] -------- -------- -------- -------0			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x2CC	IRQ050MON[B,H,W] -------- -------- -------- -------0			
0x2D0	IRQ051MON[B,H,W] -------- -------- -------- -------0			
0x2D4	IRQ052MON[B,H,W] -------- -------- -------- -------0			
0x2D8	IRQ053MON[B,H,W] -------- -------- -------- -------0			
0x2DC	IRQ054MON[B,H,W] -------- -------- -------- -------0			
0x2E0	IRQ055MON[B,H,W] -------- -------- -------- -------0			
0x2E4	IRQ056MON[B,H,W] -------- -------- -------- -------0			
0x2E8	IRQ057MON[B,H,W] -------- -------- -------- -------0			
0x2EC	IRQ058MON[B,H,W] -------- -------- -------- -------0			
0x2F0	IRQ059MON[B,H,W] -------- -------- -------- ---00000			
0x2F4	IRQ060MON[B,H,W] -------- -------- -------- -------0			
0x2F8	IRQ061MON[B,H,W] -------- -------- -------- ------00			
0x2FC	IRQ062MON[B,H,W] -------- -------- -------- -------0			
0x300	IRQ063MON[B,H,W] -------- -------- -------- ------00			
0x304	IRQ064MON[B,H,W] -------- -------- -------- -------0			
0x308	IRQ065MON[B,H,W] -------- -------- -------- ------00			
0x30C	IRQ066MON[B,H,W] -------- -------- -------- -------0			
0x310	IRQ067MON[B,H,W] -------- -------- -------- ------00			
0x314	IRQ068MON[B,H,W] -------- -------- -------- -------0			
0x318	IRQ069MON[B,H,W] -------- -------- -------- ------00			
0x31C	IRQ070MON[B,H,W] -------- -------- -------- -------0			
0x320	IRQ071MON[B,H,W] -------- -------- -------- ------00			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x324	IRQ072MON[B,H,W] -------- -------- -------- -------0			
0x328	IRQ073MON[B,H,W] -------- -------- -------- ------00			
0x32C	IRQ074MON[B,H,W] -------- -------- -------- -------0			
0x330	IRQ075MON[B,H,W] -------- -------- -------- ------00			
0x334	IRQ076MON[B,H,W] -------- -------- -------- ---00000			
0x338	IRQ077MON[B,H,W] -------- -------- -------- ---00000			
0x33C	IRQ078MON[B,H,W] -------- -------- -------- ---00000			
0x340	IRQ079MON[B,H,W] -------- -------- -------- --000000			
0x344	IRQ080MON[B,H,W] -------- -------- -------- -------0			
0x348	IRQ081MON[B,H,W] -------- -------- -------- ---00000			
0x34C	IRQ082MON[B,H,W] -------- -------- -------- -----000			
0x350	IRQ083MON[B,H,W] -------- -------- -------- -------0			
0x354	IRQ084MON[B,H,W] -------- -------- -------- -------0			
0x358	IRQ085MON[B,H,W] -------- -------- -------- -------0			
0x35C	IRQ086MON[B,H,W] -------- -------- -------- -------0			
0x360	IRQ087MON[B,H,W] -------- -------- -------- -------0			
0x364	IRQ088MON[B,H,W] -------- -------- -------- -------0			
0x368	IRQ089MON[B,H,W] -------- -------- -------- -------0			
0x36C	IRQ090MON[B,H,W] -------- -------- -------- -------0			
0x370	IRQ091MON[B,H,W] -------- -------- -------- ------00			
0x374	IRQ092MON[B,H,W] -------- -------- -------- ----0000			
0x378	IRQ093MON[B,H,W] -------- -------- -------- ----0000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x37C	IRQ094MON[B,H,W] -------- -------- -------- ----0000			
0x380	IRQ095MON[B,H,W] -------- -------- -------- ----0000			
0x384	IRQ096MON[B,H,W] -------- -------- -------- --000000			
0x388	IRQ097MON[B,H,W] -------- -------- -------- --000000			
0x38C	IRQ098MON[B,H,W] -------- -------- -------- ------00			
0x390	IRQ099MON[B,H,W] -------- -------- -------- ------00			
0x394	IRQ100MON[B,H,W] -------- -------- -------- ------00			
0x398	IRQ101MON[B,H,W] -------- -------- -------- ------00			
0x39C	IRQ102MON[B,H,W] -------- -------- -------- ------00			
0x3A0	IRQ103MON[B,H,W] -------- -------- -------- -------0			
0x3A4	IRQ104MON[B,H,W] -------- -------- -------- ------00			
0x3A8	IRQ105MON[B,H,W] -------- -------- -------- -------0			
0x3AC	IRQ106MON[B,H,W] -------- -------- -------- ------00			
0x3B0	IRQ107MON[B,H,W] -------- -------- -------- -------0			
0x3B4	IRQ108MON[B,H,W] -------- -------- -------- ------00			
0x3B8	IRQ109MON[B,H,W] -------- -------- -------- -------0			
0x3BC	IRQ110MON[B,H,W] -------- -------- -------- ------00			
0x3C0	IRQ111MON[B,H,W] -------- -------- -------- ---00000			
0x3C4	IRQ112MON[B,H,W] -------- -------- -------- --000000			
0x3C8	IRQ113MON[B,H,W] -------- -------- -------- --000000			
0x3CC	IRQ114MON[B,H,W] -------- -------- -------- -0000000			
0x3D0	IRQ115MON[B,H,W] -------- -------- -------- -----000			

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
0x3D4	IRQ116MON[B,H,W] -------- -------- -------- --------			
0x3D8	IRQ117MON[B,H,W] -------- -------- -------- ------00			
0x3DC	IRQ118MON[B,H,W] -------- -------- -------- ------00			
0x3E0	IRQ119MON[B,H,W] -------- -------- -------- -------0			
0x3E4	IRQ120MON[B,H,W] -------- -------- -------- -------0			
0x3E8	IRQ121MON[B,H,W] -------- -------- -------- ------00			
0x3EC	IRQ122MON[B,H,W] -------- -------- -------- -------0			
0x3F0	IRQ123MON[B,H,W] -------- -------- -------- ------00			
0x3F4	IRQ124MON[B,H,W] -------- -------- -------- -------0			
0x3F8	IRQ125MON[B,H,W] -------- -------- -------- ------00			
0x3FC	IRQ126MON[B,H,W] -------- -------- -------- -------0			
0x400	IRQ127MON[B,H,W] -------- -------- -------- ------00			
0x404 – 0xFFC	-	-	-	-

1.17.3 TYPE4-M4 Product

INT-Req. READ Base_Address : 0x4003_1000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	DRQSEL[B,H,W] 00000000 00000000 00000000 00000000			
0x004 – 0x00C	-			
0x010	-	-	-	ODDPKS[B] ---00000
0x014	-	-	-	ODDPKS1[B] --00000
0x018	-	*	-	*
0x01C – 0x10C	-	-	-	-
0x110	IRQ003SEL[B,H,W] 00000000 00000000 -------- 00000000			
0x114	IRQ004SEL[B,H,W] 00000000 00000000 -------- 00000000			
0x118	IRQ005SEL[B,H,W] 00000000 00000000 -------- 00000000			
0x11C	IRQ006SEL[B,H,W] 00000000 00000000 -------- 00000000			
0x120	IRQ007SEL[B,H,W] 00000000 00000000 -------- 00000000			
0x124	IRQ008SEL[B,H,W] 00000000 00000000 -------- 00000000			
0x128	IRQ009SEL[B,H,W] 00000000 00000000 -------- 00000000			
0x12C	IRQ010SEL[B,H,W] 00000000 00000000 -------- 00000000			
0x130 – 0x1FC	-	-	-	-
0x200	EXC02MON[B,H,W] -------- -------- -------- ------00			
0x204	IRQ000MON[B,H,W] -------- -------- -------- -------0			
0x208	IRQ001MON[B,H,W] -------- -------- -------- -------0			
0x20C	IRQ002MON[B,H,W] -------- -------- -------- -------0			
0x210	IRQ003MON[B,H,W] -------- -------- -------- 00000000			
0x214	IRQ004MON[B,H,W] -------- -------- -------- 00000000			
0x218	IRQ005MON[B,H,W] -------- -------- -------- 00000000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x21C	IRQ006MON[B,H,W] -------- -------- -------- 00000000			
0x220	IRQ007MON[B,H,W] -------- -------- -------- 00000000			
0x224	IRQ008MON[B,H,W] -------- -------- -------- 00000000			
0x228	IRQ009MON[B,H,W] -------- -------- -------- 00000000			
0x22C	IRQ010MON[B,H,W] -------- -------- -------- 00000000			
0x230	IRQ011MON[B,H,W] -------- -------- -------- -------0			
0x234	IRQ012MON[B,H,W] -------- -------- -------- -------0			
0x238	IRQ013MON[B,H,W] -------- -------- -------- -------0			
0x23C	IRQ014MON[B,H,W] -------- -------- -------- -------0			
0x240	IRQ015MON[B,H,W] -------- -------- -------- -------0			
0x244	IRQ016MON[B,H,W] -------- -------- -------- -------0			
0x248	IRQ017MON[B,H,W] -------- -------- -------- -------0			
0x24C	IRQ018MON[B,H,W] -------- -------- -------- -------0			
0x250	IRQ019MON[B,H,W] -------- -------- -------- --000000			
0x254	IRQ020MON[B,H,W] -------- -------- -------- --000000			
0x258	IRQ021MON[B,H,W] -------- -------- -------- ----0000			
0x25C	IRQ022MON[B,H,W] -------- -------- -------- ----0000			
0x260	IRQ023MON[B,H,W] -------- -------- -------- ----0000			
0x264	IRQ024MON[B,H,W] -------- -------- -------- -----000			
0x268	IRQ025MON[B,H,W] -------- -------- -------- -----000			
0x26C	IRQ026MON[B,H,W] -------- -------- -------- ----0000			
0x270	IRQ027MON[B,H,W] -------- -------- -------- --000000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x274	IRQ028MON[B,H,W] -------- -------- -------- -----000			
0x278	IRQ029MON[B,H,W] -------- -------- -------- -----000			
0x27C	IRQ030MON[B,H,W] -------- -------- -------- ----0000			
0x280	IRQ031MON[B,H,W] -------- -------- -------- --000000			
0x284	IRQ032MON[B,H,W] -------- -------- -------- -----000			
0x288	IRQ033MON[B,H,W] -------- -------- -------- -----000			
0x28C	IRQ034MON[B,H,W] -------- -------- -------- ---00000			
0x290	IRQ035MON[B,H,W] -------- -------- -------- --000000			
0x294	IRQ036MON[B,H,W] -------- -------- -------- -----000			
0x298	IRQ037MON[B,H,W] -------- -------- -------- -----000			
0x29C	IRQ038MON[B,H,W] -------- -------- -------- -----000			
0x2A0	IRQ039MON[B,H,W] -------- -------- -------- ------00			
0x2A4	IRQ040MON[B,H,W] -------- -------- -------- ------00			
0x2A8	IRQ041MON[B,H,W] -------- -------- -------- ------00			
0x2AC	IRQ042MON[B,H,W] -------- -------- -------- ------00			
0x2B0	IRQ043MON[B,H,W] -------- -------- -------- ------00			
0x2B4	IRQ044MON[B,H,W] -------- -------- -------- ------00			
0x2B8	IRQ045MON[B,H,W] -------- -------- -------- ------00			
0x2BC	IRQ046MON[B,H,W] -------- -------- -------- ------00			
0x2C0	IRQ047MON[B,H,W] -------- -------- -------- ------00			
0x2C4	IRQ048MON[B,H,W] -------- -------- -------- -------0			
0x2C8	IRQ049MON[B,H,W] -------- -------- -------- ------00			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x2CC	IRQ050MON[B,H,W] -------- -------- -------- -------0			
0x2D0	IRQ051MON[B,H,W] -------- -------- -------- -------0			
0x2D4	IRQ052MON[B,H,W] -------- -------- -------- -------0			
0x2D8	IRQ053MON[B,H,W] -------- -------- -------- -------0			
0x2DC	IRQ054MON[B,H,W] -------- -------- -------- -------0			
0x2E0	IRQ055MON[B,H,W] -------- -------- -------- -------0			
0x2E4	IRQ056MON[B,H,W] -------- -------- -------- -------0			
0x2E8	IRQ057MON[B,H,W] -------- -------- -------- -------0			
0x2EC	IRQ058MON[B,H,W] -------- -------- -------- -------0			
0x2F0	IRQ059MON[B,H,W] -------- -------- -------- --000000			
0x2F4	IRQ060MON[B,H,W] -------- -------- -------- -------0			
0x2F8	IRQ061MON[B,H,W] -------- -------- -------- ------00			
0x2FC	IRQ062MON[B,H,W] -------- -------- -------- -------0			
0x300	IRQ063MON[B,H,W] -------- -------- -------- ------00			
0x304	IRQ064MON[B,H,W] -------- -------- -------- -------0			
0x308	IRQ065MON[B,H,W] -------- -------- -------- ------00			
0x30C	IRQ066MON[B,H,W] -------- -------- -------- -------0			
0x310	IRQ067MON[B,H,W] -------- -------- -------- ------00			
0x314	IRQ068MON[B,H,W] -------- -------- -------- -------0			
0x318	IRQ069MON[B,H,W] -------- -------- -------- ------00			
0x31C	IRQ070MON[B,H,W] -------- -------- -------- -------0			
0x320	IRQ071MON[B,H,W] -------- -------- -------- ------00			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x324	IRQ072MON[B,H,W] -------- -------- -------- -------0			
0x328	IRQ073MON[B,H,W] -------- -------- -------- ------00			
0x32C	IRQ074MON[B,H,W] -------- -------- -------- -------0			
0x330	IRQ075MON[B,H,W] -------- -------- -------- ------00			
0x334	IRQ076MON[B,H,W] -------- -------- -------- ---00000			
0x338	IRQ077MON[B,H,W] -------- -------- -------- ---00000			
0x33C	IRQ078MON[B,H,W] -------- -------- -------- ---00000			
0x340	IRQ079MON[B,H,W] -------- -------- -------- --000000			
0x344	IRQ080MON[B,H,W] -------- -------- -------- -------0			
0x348	IRQ081MON[B,H,W] -------- -------- -------- ---00000			
0x34C	IRQ082MON[B,H,W] -------- -------- -------- -----000			
0x350	IRQ083MON[B,H,W] -------- -------- -------- -------0			
0x354	IRQ084MON[B,H,W] -------- -------- -------- -------0			
0x358	IRQ085MON[B,H,W] -------- -------- -------- -------0			
0x35C	IRQ086MON[B,H,W] -------- -------- -------- -------0			
0x360	IRQ087MON[B,H,W] -------- -------- -------- -------0			
0x364	IRQ088MON[B,H,W] -------- -------- -------- -------0			
0x368	IRQ089MON[B,H,W] -------- -------- -------- -------0			
0x36C	IRQ090MON[B,H,W] -------- -------- -------- -------0			
0x370	IRQ091MON[B,H,W] -------- -------- -------- ------00			
0x374	IRQ092MON[B,H,W] -------- -------- -------0 ----0000			
0x378	IRQ093MON[B,H,W] -------- -------- -------0 ----0000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x37C	IRQ094MON[B,H,W] -------- -------- -------0 ----0000			
0x380	IRQ095MON[B,H,W] -------- -------- -------0 ----0000			
0x384	IRQ096MON[B,H,W] -------- -------- -------0 --000000			
0x388	IRQ097MON[B,H,W] -------- -------- -------0 --000000			
0x38C	IRQ098MON[B,H,W] -------- -------- -------0 ------00			
0x390	IRQ099MON[B,H,W] -------- -------- -------0 ------00			
0x394	IRQ100MON[B,H,W] -------- -------- -------0 ------00			
0x398	IRQ101MON[B,H,W] -------- -------- -------0 ------00			
0x39C	IRQ102MON[B,H,W] -------- -------- -------0 ------00			
0x3A0	IRQ103MON[B,H,W] -------- -------- -------0 -------0			
0x3A4	IRQ104MON[B,H,W] -------- -------- -------0 ------00			
0x3A8	IRQ105MON[B,H,W] -------- -------- -------0 -------0			
0x3AC	IRQ106MON[B,H,W] -------- -------- -------0 ------00			
0x3B0	IRQ107MON[B,H,W] -------- -------- -------0 -------0			
0x3B4	IRQ108MON[B,H,W] -------- -------- -------0 ------00			
0x3B8	IRQ109MON[B,H,W] -------- -------- -------0 -------0			
0x3BC	IRQ110MON[B,H,W] -------- -------- -------0 ------00			
0x3C0	IRQ111MON[B,H,W] -------- -------- -------- ---00000			
0x3C4	IRQ112MON[B,H,W] -------- -------- ------00 00000000			
0x3C8	IRQ113MON[B,H,W] -------- -------- -------- --000000			
0x3CC	IRQ114MON[B,H,W] -------- -------- -------- -0000000			
0x3D0	IRQ115MON[B,H,W] -------- -------- -------- -----000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x3D4	IRQ116MON[B,H,W] -------- -------- -------- --------			
0x3D8	IRQ117MON[B,H,W] -------- -------- -------- -----000			
0x3DC	IRQ118MON[B,H,W] -------- -------- -------- ------00			
0x3E0	IRQ119MON[B,H,W] -------- -------- -------- -------0			
0x3E4	IRQ120MON[B,H,W] -------- -------- -------0 -------0			
0x3E8	IRQ121MON[B,H,W] -------- -------- -------0 ------00			
0x3EC	IRQ122MON[B,H,W] -------- -------- -------0 -------0			
0x3F0	IRQ123MON[B,H,W] -------- -------- -------0 ------00			
0x3F4	IRQ124MON[B,H,W] -------- -------- -------- -------0			
0x3F8	IRQ125MON[B,H,W] -------- -------- -------- ------00			
0x3FC	IRQ126MON[B,H,W] -------- -------- -------- -------0			
0x400	IRQ127MON[B,H,W] -------- -------- -------- ------00			
0x404 – 0xFFC	-	-	-	-

1.18 D/AC

12bit D/AC unit0 Base_Address : 0x4003_3000

12bit D/AC unit1 Base_Address : 0x4003_3008

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	DACR[B,H,W] --00--00
0x004	-	-	DADR[H,W] ----XXXX XXXXXXXX	
0x010 – 0xFFC	-	-	-	-

1.19 HDMI-CEC

HDMI-CEC/Remote Control Receiver ch.0 Base_Address : 0x4003_4000

HDMI-CEC/Remote Control Receiver ch.1 Base_Address : 0x4003_4100

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	TXCTRL[B,H,W] --0000-0
0x004	-	-	-	TXDATA[B,H,W] 00000000
0x008	-	-	-	TXSTS[B,H,W] --00---0
0x00C	-	-	-	SFREE[B,H,W] ----0000
0x010 – 0x03C	-	-	-	-
0x040	-	-	RCCR[B,H,W] 0---0000	RCST[B,H,W] 00000000
0x044	-	-	RCSHW[B,H,W] 00000000	RCDAHW[B,H,W] 00000000
0x048	-	-	RCDBHW[B,H,W] 00000000	-
0x04C	-	-	RCADR1[B,H,W] ---00000	RCADR2[B,H,W] ---00000
0x050	-	-	RCDTHH[B,H,W] 00000000	RCDTHL[B,H,W] 00000000
0x054	-	-	RCDTLH[B,H,W] 00000000	RCDTLL[B,H,W] 00000000
0x058	-	-	RCCKD[B,H,W] ---00000 00000000	
0x05C	-	-	RCRC[B,H,W] ---0---0	RCRHW[B,H,W] 00000000
0x060	-	-	RCLE[B,H,W] 00000-00	-
0x064	-	-	RCLELW[B,H,W] 00000000	RCLESW[B,H,W] 00000000
0x068 – 0x0FC	-	-	-	-

1.20 GPIO

1.20.1 TYPE1-M4, TYPE2-M4, TYPE6-M4 Products

GPIO Base_Address : 0x4006_F000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	PFR0[B,H,W] ---- ---- ---- ---- 0000 0000 0001 1111			
0x004	PFR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x008	PFR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x00C	PFR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x010	PFR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x014	PFR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x018	PFR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x01C	PFR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x020	PFR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x024	PFR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x028	PFRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x02C	PFRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x030	PFRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x034	PFRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x038	PFRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x03C	PFRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x040 - 0x0FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x100	PCR0[B,H,W] ---- ---- ---- ---- 0000 0000 0001 1111			
0x104	PCR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x108	PCR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x10C	PCR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x110	PCR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x114	PCR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x118	PCR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x11C	PCR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x120	-			
0x124	PCR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x128	PCRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x12C	PCRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x130	PCRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x134	PCRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x138	PCRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x13C	PCRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x140 - 0x1FC	-	-	-	-

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
0x200	DDR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x204	DDR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x208	DDR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x20C	DDR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x210	DDR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x214	DDR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x218	DDR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x21C	DDR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x220	DDR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x224	DDR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x228	DDRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x22C	DDRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x230	DDRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x234	DDRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x238	DDRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x23C	DDRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x240 - 0x2FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x300	PDIR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x304	PDIR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x308	PDIR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x30C	PDIR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x310	PDIR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x314	PDIR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x318	PDIR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x31C	PDIR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x320	PDIR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x324	PDIR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x328	PDIRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x32C	PDIRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x330	PDIRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x334	PDIRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x338	PDIRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x33C	PDIRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x340 - 0x3FC	-	-	-	-

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
0x400	PDOR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x404	PDOR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x408	PDOR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x40C	PDOR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x410	PDOR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x414	PDOR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x418	PDOR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x41C	PDOR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x420	PDOR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x424	PDOR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x428	PDORA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x42C	PDORB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x430	PDORC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x434	PDORD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x438	PDORE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x43C	PDORF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x440 - 0x4FC	-	-	-	-
0x500	ADE[B,H,W] 1111 1111 1111 1111 1111 1111 1111 1111			
0x504 - 0x57C	-	-	-	-
0x580	SPSR[B,H,W] ---- ---- ---- ---- ---- ---- --00 01--			
0x584 - 0x5FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x600	EPFR00[B,H,W] ---- --00 ---- --11 --0- --0- 0000 --00			
0x604	EPFR01[B,H,W] 0000 0000 0000 0000 ---0 0000 0000 0000			
0x608	EPFR02[B,H,W] 0000 0000 0000 0000 ---0 0000 0000 0000			
0x60C	EPFR03[B,H,W] 0000 0000 0000 0000 ---0 0000 0000 0000			
0x610	EPFR04[B,H,W] --00 0000 --00 00-- --00 0000 -000 00--			
0x614	EPFR05[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x618	EPFR06[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x61C	EPFR07[B,H,W] 0000 0000 0000 0000 0000 0000 0000 ----			
0x620	EPFR08[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x624	EPFR09[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x628	EPFR10[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x62C	EPFR11[B,H,W] ---- --00 0000 0000 0000 0000 0000 0000			
0x630	EPFR12[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x634	EPFR13[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x638	EPFR14[B,H,W] --00 0000 0000 00-- ---- ---- --00 0000			
0x63C	EPFR15[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x640	EPFR16[B,H,W] --00 0000 0000 0000 0000 0000 0000 0000			
0x644	EPFR17[B,H,W] ---- 0000 0000 0000 0000 0000 0000 ----			
0x648	EPFR18[B,H,W] --00 0000 0000 0000 00-- --00 0000 ----			
0x64C	EPFR19[B,H,W] ---- ---- ---- ---- ---- ---- ---- ----			
0x650	EPFR20[B,H,W] ---- ---0 0000 0000 0000 0000 0000 0000			
0x654 – 0x6FC	-	-	-	-

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
0x700	PZR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x704	PZR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x708	PZR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x70C	PZR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x710	PZR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x714	PZR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x718	PZR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x71C	PZR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x720	PZR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x724	PZR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x728	PZRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x72C	PZRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x730	PZRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x734	PZRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x738	PZRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x73C	PZRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x740 - 0xEFC	-	-	-	-
0xF00 – 0xF04	*			
0xF08 – 0xFDC	-	-	-	-
0xFE0	*			
0xFE4 - 0xFFC	-	-	-	-

1.20.2 TYPE3-M4 Product

GPIO Base_Address : 0x4006_F000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	PFR0[B,H,W] ---- ---- ---- ---- 0000 0000 0001 1111			
0x004	PFR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x008	PFR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x00C	PFR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x010	PFR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x014	PFR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x018	PFR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x01C	PFR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x020	PFR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x024	PFR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x028	PFRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x02C	PFRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x030	PFRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x034	PFRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x038	PFRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x03C	PFRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x040 - 0x0FC	-	-	-	-

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
0x100	PCR0[B,H,W] ---- ---- ---- ---- 0000 0000 0001 1111			
0x104	PCR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x108	PCR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x10C	PCR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x110	PCR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x114	PCR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x118	PCR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x11C	PCR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x120	-			
0x124	PCR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x128	PCRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x12C	PCRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x130	PCRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x134	PCRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x138	PCRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x13C	PCRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x140 - 0x1FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x200	DDR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x204	DDR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x208	DDR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x20C	DDR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x210	DDR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x214	DDR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x218	DDR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x21C	DDR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x220	DDR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x224	DDR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x228	DDRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x22C	DDRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x230	DDRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x234	DDRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x238	DDRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x23C	DDRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x240 - 0x2FC	-	-	-	-

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
0x300	PDIR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x304	PDIR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x308	PDIR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x30C	PDIR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x310	PDIR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x314	PDIR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x318	PDIR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x31C	PDIR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x320	PDIR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x324	PDIR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x328	PDIRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x32C	PDIRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x330	PDIRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x334	PDIRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x338	PDIRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x33C	PDIRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x340 - 0x3FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x400	PDOR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x404	PDOR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x408	PDOR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x40C	PDOR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x410	PDOR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x414	PDOR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x418	PDOR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x41C	PDOR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x420	PDOR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x424	PDOR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x428	PDORA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x42C	PDORB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x430	PDORC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x434	PDORD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x438	PDORE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x43C	PDORF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x440 - 0x4FC	-	-	-	-
0x500	ADE[B,H,W] 1111 1111 1111 1111 1111 1111 1111 1111			
0x504 - 0x57C	-	-	-	-
0x580	SPSR[B,H,W] ---- ---- ---- ---- ---- ---- --00 01--			
0x584 - 0x5FC	-	-	-	-

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
0x600	EPFR00[B,H,W] ---- 0000 ---- --11 --0- --0- 0000 –00			
0x604	EPFR01[B,H,W] 0000 0000 0000 0000 ---0 0000 0000 0000			
0x608	EPFR02[B,H,W] 0000 0000 0000 0000 ---0 0000 0000 0000			
0x60C	EPFR03[B,H,W] 0000 0000 0000 0000 ---0 0000 0000 0000			
0x610	EPFR04[B,H,W] --00 0000 --00 00-- --00 0000 -000 00--			
0x614	EPFR05[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x618	EPFR06[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x61C	EPFR07[B,H,W] 0000 0000 0000 0000 0000 0000 0000 ----			
0x620	EPFR08[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x624	EPFR09[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x628	EPFR10[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x62C	EPFR11[B,H,W] ---- --00 0000 0000 0000 0000 0000 0000			
0x630	EPFR12[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x634	EPFR13[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x638	EPFR14[B,H,W] --00 0000 0000 00-- ---- ---- --00 0000			
0x63C	EPFR15[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x640	EPFR16[B,H,W] --00 0000 0000 0000 0000 0000 0000 0000			
0x644	EPFR17[B,H,W] ---- 0000 0000 0000 0000 0000 0000 ----			
0x648	EPFR18[B,H,W] --00 0000 0000 0000 00-- --00 0000 0000			
0x64C	EPFR19[B,H,W] ---- ---- ---- ---- ---- ---- ---- ----			
0x650	EPFR20[B,H,W] ---- ---0 0000 0000 0000 0000 0000 0000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x654	EPFR21[B,H,W] ---- ---- ---- ---- ---- ---- ---- ----			
0x658	EPFR22[B,H,W] ---- ---- ---- ---- ---- ---- ---- ----			
0x65C	EPFR23[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x660	EPFR24[B,H,W] ---- ---- ---- ---- ---- 0000 0000 0000			
0x664	EPFR25[B,H,W] ---- ---- ---- ---- ---- ---- ---- 0000			
0x668	EPFR26[B,H,W] ---- ---- ---- --00 0000 0000 0000 0000			
0x66C – 0x6FC	-	-	-	-

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
0x700	PZR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x704	PZR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x708	PZR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x70C	PZR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x710	PZR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x714	PZR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x718	PZR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x71C	PZR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x720	PZR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x724	PZR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x728	PZRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x72C	PZRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x730	PZRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x734	PZRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x738	PZRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x73C	PZRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x740	PDSR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x744	PDSR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x748	PDSR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x74C	PDSR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x750	PDSR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x754	PDSR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x758	PDSR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x75C	PDSR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x760	PDSR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x764	PDSR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x768	PDSRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x76C	PDSRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x770	PDSRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x774	PDSRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x778	PDSRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x77C	PDSRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x780 - 0xEFC	-	-	-	-
0xF00 – 0xF04	*			
0xF08 – 0xFDC	-	-	-	-
0xFE0	*			
0xFE4 - 0xFFC	-	-	-	-

1.20.3 TYPE4-M4 Product

GPIO Base_Address : 0x4006_F000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	PFR0[B,H,W] ---- ---- ---- ---- 0000 0000 0001 1111			
0x004	PFR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x008	PFR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x00C	PFR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x010	PFR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x014	PFR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x018	PFR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x01C	PFR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x020	PFR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x024	PFR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x028	PFRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x02C	PFRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x030	PFRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x034	PFRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x038	PFRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x03C	PFRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x040 - 0x0FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x100	PCR0[B,H,W] ---- ---- ---- ---- 0000 0000 0001 1111			
0x104	PCR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x108	PCR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x10C	PCR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x110	PCR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x114	PCR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x118	PCR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x11C	PCR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x120	-			
0x124	PCR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x128	PCRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x12C	PCRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x130	PCRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x134	PCRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x138	PCRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x13C	PCRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x140 - 0x1FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x200	DDR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x204	DDR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x208	DDR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x20C	DDR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x210	DDR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x214	DDR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x218	DDR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x21C	DDR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x220	DDR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x224	DDR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x228	DDRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x22C	DDRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x230	DDRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x234	DDRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x238	DDRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x23C	DDRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x240 - 0x2FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x300	PDIR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x304	PDIR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x308	PDIR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x30C	PDIR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x310	PDIR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x314	PDIR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x318	PDIR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x31C	PDIR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x320	PDIR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x324	PDIR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x328	PDIRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x32C	PDIRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x330	PDIRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x334	PDIRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x338	PDIRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x33C	PDIRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x340 - 0x3FC	-	-	-	-

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
0x400	PDOR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x404	PDOR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x408	PDOR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x40C	PDOR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x410	PDOR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x414	PDOR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x418	PDOR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x41C	PDOR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x420	PDOR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x424	PDOR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x428	PDORA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x42C	PDORB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x430	PDORC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x434	PDORD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x438	PDORE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x43C	PDORF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x440 - 0x4FC	-	-	-	-
0x500	ADE[B,H,W] 1111 1111 1111 1111 1111 1111 1111 1111			
0x504 - 0x57C	-	-	-	-
0x580	SPSR[B,H,W] ---- ---- ---- ---- ---- ---- --00 01--			
0x584 - 0x5FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x600	EPFR00[B,H,W] ---- 0000 ---- --11 --0- --0- 0000 –00			
0x604	EPFR01[B,H,W] 0000 0000 0000 0000 ---0 0000 0000 0000			
0x608	EPFR02[B,H,W] 0000 0000 0000 0000 ---0 0000 0000 0000			
0x60C	EPFR03[B,H,W] 0000 0000 0000 0000 ---0 0000 0000 0000			
0x610	EPFR04[B,H,W] --00 0000 --00 00-- --00 0000 -000 00--			
0x614	EPFR05[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x618	EPFR06[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x61C	EPFR07[B,H,W] 0000 0000 0000 0000 0000 0000 0000 ----			
0x620	EPFR08[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x624	EPFR09[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x628	EPFR10[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x62C	EPFR11[B,H,W] ---- --00 0000 0000 0000 0000 0000 0000			
0x630	EPFR12[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x634	EPFR13[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x638	EPFR14[B,H,W] --00 0000 0000 00-- ---- ---- --00 0000			
0x63C	EPFR15[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x640	EPFR16[B,H,W] --00 0000 0000 0000 0000 0000 0000 0000			
0x644	EPFR17[B,H,W] ---- 0000 0000 0000 0000 0000 0000 ----			
0x648	EPFR18[B,H,W] --00 0000 0000 0000 00-- --00 0000 0000			
0x64C	EPFR19[B,H,W] ---- ---- ---- ---- ---- ---- ---- ----			
0x650	EPFR20[B,H,W] ---- ---0 0000 0000 0000 0000 0000 0000			

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
0x654	EPFR21[B,H,W] ---- ---- ---- ---- ---- ---- ---- ----			
0x658	EPFR22[B,H,W] ---- ---- ---- ---- ---- ---- ---- ----			
0x65C	EPFR23[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x660	EPFR24[B,H,W] ---- 0000 0000 0000 ---- 0000 0000 0000			
0x664	EPFR25[B,H,W] ---- ---- ---- ---- ---- ---- ---- 0000			
0x668	EPFR26[B,H,W] ---- ---- ---- --00 0000 0000 0000 0000			
0x66C	EPFR27[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x670	EPFR28[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x674	EPFR29[B,H,W] 0000 0000 0000 00-- 0000 0000 0000 0000			
0x67C	EPFR30[B,H,W] ---- --00 0000 0000 ---- 0000 0000 0000			
0x680 – 0x6FC	-	-	-	-
0x700	PZR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x704	PZR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x708	PZR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x70C	PZR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x710	PZR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x714	PZR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x718	PZR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x71C	PZR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x720	PZR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x724	PZR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x728	PZRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x72C	PZRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x730	PZRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x734	PZRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x738	PZRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x73C	PZRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x740 - 0xEFC	-	-	-	-
0xF00 – 0xF04	*			
0xF08 – 0xFDC	-	-	-	-
0xFE0	*			
0xFE4 - 0xFFC	-	-	-	-

1.20.4 TYPE5-M4 Product

GPIO Base_Address : 0x4006_F000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	PFR0[B,H,W] ---- ---- ---- ---- 0000 0000 0001 1111			
0x004	PFR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x008	PFR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x00C	PFR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x010	PFR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x014	PFR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x018	PFR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x01C	PFR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x020	PFR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x024	PFR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x028	PFRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x02C	PFRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x030	PFRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x034	PFRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x038	PFRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x03C	PFRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x040 - 0x0FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x100	PCR0[B,H,W] ---- ---- ---- ---- 0000 0000 0001 1111			
0x104	PCR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x108	PCR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x10C	PCR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x110	PCR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x114	PCR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x118	PCR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x11C	PCR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x120	-			
0x124	PCR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x128	PCRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x12C	PCRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x130	PCRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x134	PCRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x138	PCRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x13C	PCRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x140 - 0x1FC	-	-	-	-

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
0x200	DDR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x204	DDR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x208	DDR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x20C	DDR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x210	DDR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x214	DDR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x218	DDR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x21C	DDR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x220	DDR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x224	DDR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x228	DDRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x22C	DDRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x230	DDRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x234	DDRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x238	DDRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x23C	DDRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x240 - 0x2FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x300	PDIR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x304	PDIR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x308	PDIR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x30C	PDIR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x310	PDIR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x314	PDIR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x318	PDIR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x31C	PDIR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x320	PDIR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x324	PDIR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x328	PDIRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x32C	PDIRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x330	PDIRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x334	PDIRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x338	PDIRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x33C	PDIRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x340 - 0x3FC	-	-	-	-

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
0x400	PDOR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x404	PDOR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x408	PDOR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x40C	PDOR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x410	PDOR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x414	PDOR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x418	PDOR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x41C	PDOR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x420	PDOR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x424	PDOR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x428	PDORA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x42C	PDORB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x430	PDORC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x434	PDORD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x438	PDORE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x43C	PDORF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x440 - 0x4FC	-	-	-	-
0x500	ADE[B,H,W] 1111 1111 1111 1111 1111 1111 1111 1111			
0x504 - 0x57C	-	-	-	-
0x580	SPSR[B,H,W] ---- ---- ---- ---- ---- ---- --00 01--			
0x584 - 0x5FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x600	EPFR00[B,H,W] ---- 0000 ---- --11 --0- --0- 0000 –00			
0x604	EPFR01[B,H,W] 0000 0000 0000 0000 ---0 0000 0000 0000			
0x608	EPFR02[B,H,W] 0000 0000 0000 0000 ---0 0000 0000 0000			
0x60C	EPFR03[B,H,W] ---- ---- ---- ---- ---- ---- ---- ----			
0x610	EPFR04[B,H,W] --00 0000 --00 00-- --00 0000 -000 00--			
0x614	EPFR05[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x618	EPFR06[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x61C	EPFR07[B,H,W] 0000 0000 0000 0000 0000 0000 0000 ----			
0x620	EPFR08[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x624	EPFR09[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x628	EPFR10[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x62C	EPFR11[B,H,W] ---- --00 0000 0000 0000 0000 0000 0000			
0x630	EPFR12[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x634	EPFR13[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x638	EPFR14[B,H,W] --00 0000 0000 00-- ---- ---- --00 0000			
0x63C	EPFR15[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x640	EPFR16[B,H,W] --00 0000 0000 0000 0000 0000 0000 0000			
0x644	EPFR17[B,H,W] ---- ---- ---- ---- ---- ---- ---- ----			
0x648	EPFR18[B,H,W] --00 0000 0000 0000 00-- --00 0000 0000			
0x64C	EPFR19[B,H,W] ---- ---- ---- ---- ---- ---- ---- ----			
0x650	EPFR20[B,H,W] ---- ---0 0000 0000 0000 0000 0000 0000			

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
0x654	EPFR21[B,H,W] ---- ---- ---- ---- ---- ---- ---- ----			
0x658	EPFR22[B,H,W] ---- ---- ---- ---- ---- ---- ---- ----			
0x65C	EPFR23[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x660	EPFR24[B,H,W] ---- ---- ---- ---- ---- 0000 0000 0000			
0x664	EPFR25[B,H,W] ---- ---- ---- ---- ---- ---- ---- 0000			
0x668	EPFR26[B,H,W] ---- ---- ---- --00 0000 0000 0000 0000			
0x66C – 0x680	-	-	-	-
0x684	EPFR33[B,H,W] ---- 0000 0000 0000 ---- 0000 0000 0000			
0x688	-	-	-	-
0x68C	EPFR35[B,H,W] ---- 0000 0000 0000 ---- ---- ---- ----			
0x690 – 0x6FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x700	PZR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x704	PZR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x708	PZR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x70C	PZR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x710	PZR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x714	PZR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x718	PZR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x71C	PZR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x720	PZR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x724	PZR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x728	PZRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x72C	PZRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x730	PZRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x734	PZRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x738	PZRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x73C	PZRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x740	PDSR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x744	PDSR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x748	PDSR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x74C	PDSR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x750	PDSR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x754	PDSR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
0x758	PDSR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x75C	PDSR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x760	PDSR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x764	PDSR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x768	PDSRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x76C	PDSRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x770	PDSRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x774	PDSRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x778	PDSRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x77C	PDSRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x780 - 0xEFC	-	-	-	-
0xF00 – 0xF04	*			
0xF08 – 0xFDC	-	-	-	-
0xFE0	*			
0xFE4 - 0xFFC	-	-	-	-

1.21 LVD

LVD Base_Address : 0x4003_5000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	LVD_CTL[B,H,W] 000111--
0x004	-	-	-	LVD_STR[B,H,W] 0-------
0x008	-	-	-	LVD_CLR[B,H,W] 1-------
0x00C	LVD_RLR[W] 00000000 00000000 00000000 00000001			
0x010	-	-	-	LVD_STR2 [B,H,W] 0-------
0x014 - 0x0FC	-	-	-	-

1.22 DS_Mode

DS_Mode Base_Address : 0x4003_5100

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	*
0x004	-	-	-	RCK_CTL[B,H,W] ------01
0x008 - 0x6FC	-	-	-	-
0x700	-	-	-	PMD_CTL[B,H,W] -------0
0x704	-	-	-	WRFSR[B,H,W] ------00
0x708	-	-	WIFSR[B,H,W] ------00 00000000	
0x70C	-	-	WIER[B,H,W] ------00 00000-00	
0x710	-	-	-	WILVR[B,H,W] ---00000
0x714	-	-	-	DSRAMR[B,H,W] ------00
0x718 - 0x7FC	-	-	-	-
0x800	BUR04[B,H,W] 00000000	BUR03[B,H,W] 00000000	BUR02[B,H,W] 00000000	BUR01[B,H,W] 00000000
0x804	BUR08[B,H,W] 00000000	BUR07[B,H,W] 00000000	BUR06[B,H,W] 00000000	BUR05[B,H,W] 00000000
0x808	BUR012[B,H,W] 00000000	BUR11[B,H,W] 00000000	BUR10[B,H,W] 00000000	BUR09[B,H,W] 00000000
0x80C	BUR16[B,H,W] 00000000	BUR15[B,H,W] 00000000	BUR14[B,H,W] 00000000	BUR13[B,H,W] 00000000
0x810 - 0xEFC	-	-	-	-

1.23 USB Clock

USB Clock Base_Address : 0x4003_6000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	UCCR[B,H,W] -0000000
0x004	-	-	-	UPCR1[B,H,W] ------00
0x008	-	-	-	UPCR2[B,H,W] -----000
0x00C	-	-	-	UPCR3[B,H,W] ---00000
0x010	-	-	-	UPCR4[B,H,W] -0111011
0x014	-	-	-	UP_STR[B,H,W] -------0
0x018	-	-	-	UPINT_ENR[B,H,W] -------0
0x01C	-	-	-	UPINT_CLR[B,H,W] -------0
0x020	-	-	-	UPINT_STR[B,H,W] -------0
0x024	-	-	-	UPCR5[B,H,W] ----0100
0x028	-	-	-	UPCR6[B,H,W] ----0010
0x02C	-	-	-	UPCR7[B,H,W] -------0
0x030	-	-	-	USBEN0[B,H,W] -------0
0x034	-	-	-	USBEN1[B,H,W] -------0
0x038 - 0x0FC	-	-	-	-

1.24 CAN_Prescaler

CAN_Prescaler Base_Address : 0x4003_7000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	CANPRE[B,H,W] ----1011
0x004 - 0xFFC	-	-	-	-

1.25 MFS

MFS ch.0 Base_Address : 0x4003_8000

MFS ch.1 Base_Address : 0x4003_8100

MFS ch.2 Base_Address : 0x4003_8200

MFS ch.3 Base_Address : 0x4003_8300

MFS ch.4 Base_Address : 0x4003_8400

MFS ch.5 Base_Address : 0x4003_8500

MFS ch.6 Base_Address : 0x4003_8600

MFS ch.7 Base_Address : 0x4003_8700

MFS ch.8 Base_Address : 0x4003_8800

MFS ch.9 Base_Address : 0x4003_8900

MFS ch.10Base_Address : 0x4003_8A00

MFS ch.11Base_Address : 0x4003_8B00

MFS ch.12Base_Address : 0x4003_8C00

MFS ch.13Base_Address : 0x4003_8D00

MFS ch.14Base_Address : 0x4003_8E00

MFS ch.15Base_Address : 0x4003_8F00

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	SCR / IBCR[B,H,W] 0--00000	SMR[B,H,W] 000-00-0
0x004	-	-	SSR[B,H,W] 0-000011	ESCR / IBSR[B,H,W] 00000000
0x008	-	-	RDR/TDR[H,W] 00000000 00000000	
	(*1) RDR/TDR[H,W] 00000000 00000000 00000000 00000000			

A. Register Map

Base_Address + Address	Register			
	+3	+3	+3	+3
0x00C	-	-	BGR1[B,H,W] 00000000	BGR0[B,H,W] 00000000
0x010	-	-	ISMK[B,H,W] --------	ISBA[B,H,W] --------
0x014	-	-	FCR1[B,H,W] ---00100	FCR0[B,H,W] -0000000
0x018	-	-	FBYTE2[B,H,W] 00000000	FBYTE1[B,H,W] 00000000
0x01C	-	-	SCSTR1/ EIBCR[B,H,W] 00000000	SCSTR0/ NFCR[B,H,W] 00000000
0x020	-	-	SCSTR3[B,H,W] 00000000	SCSTR2[B,H,W] 00000000
0x024	-	-	SACSR1[B,H,W] 00000000	SACSR0[B,H,W] 00000000
0x028	-	-	STMR1[B,H,W] 00000000	STMR0[B,H,W] 00000000
0x02C	-	-	STMCR1[B,H,W] 00000000	STMCR0[B,H,W] 00000000
0x030	-	-	SCSCR1[B,H,W] 00000000	SCSCR0[B,H,W] 00100000
0x034	-	-	SCSFR1[B,H,W] 10000000	SCSFR0[B,H,W] 10000000
0x038	-	-	-	SCSFR2[B,H,W] 10000000
0x03C	-	-	TBYTE1[B,H,W] 00000000	TBYTE0[B,H,W] 00000000
0x040	-	-	TBYTE3[B,H,W] 00000000	TBYTE2[B,H,W] 00000000
0x0144 - 0x1FC	-	-	-	-

Note:

- *(*1): RDR/TDR register's higher 16 bits can be accessed by word operation in I2S mode.*

1.26 CRC

CRC Base_Address : 0x4003_9000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	-	-	CRCCR[B,H,W] -0000000
0x004	CRCINIT[B,H,W] 11111111 11111111 11111111 11111111			
0x008	CRCIN[B,H,W] 00000000 00000000 00000000 00000000			
0x00C	CRCR[B,H,W] 11111111 11111111 11111111 11111111			

1.27 Watch Counter

Watch Counter Base_Address : 0x4003_A000

Base_Address	Register			
+ Address	+3	+2	+1	+0
0x000	-	WCCR[B,H,W] 00--0000	WCRL[B,H,W] --000000	WCRD[B,H,W] --000000
0x004 - 0x00C	-	-	-	-
0x010	-	-	CLK_SEL[B,H,W] -----000 ------00	
0x014	-	-	-	CLK_EN[B,H,W] ------00
0x018 - 0xFFC	-	-	-	-

1.28 RTC

1.28.1 TYPE1-M4, TYPE2-M4, TYPE3-M4, TYPE6-M4 Products

RTC Base_Address : 0x4003_B000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x100	-	-	-	WTCR10[B,H,W] 00000000
0x104	-	-	-	WTCR11[B,H,W] ---00000
0x108	-	-	-	WTCR12[B,H,W] 00000000
0x10C	-	-	-	WTCR13[B,H,W] 00000000
0x110	-	-	-	WTCR20[B,H,W] --000000
0x114	-	-	-	WTCR21[B,H,W] -----000
0x118	-	-	-	*
0x11C	-	-	-	WTSR[B,H,W] -0000000
0x120	-	-	-	WTMIR[B,H,W] -0000000
0x124	-	-	-	WTHR[B,H,W] --000000
0x128	-	-	-	WTDR[B,H,W] --000000
0x12C	-	-	-	WTDW[B,H,W] -----000
0x130	-	-	-	WTMOR[B,H,W] ---00000
0x134	-	-	-	WTYR[B,H,W] 00000000
0x138	-	-	-	ALMIR[B,H,W] -0000000
0x13C	-	-	-	ALHR[B,H,W] --000000
0x140	-	-	-	ALDR[B,H,W] --000000
0x144	-	-	-	ALMOR[B,H,W] ---00000
0x148	-	-	-	ALYR[B,H,W] 00000000
0x14C	-	-	-	WTTR0[B,H,W] 00000000
0x150	-	-	-	WTTR1[B,H,W] 00000000
0x154	-	-	-	WTTR2[B,H,W] ------00

Base_Address + Address	Register			
	+3	+2	+1	+0
0x158	-	-	-	WTCAL0[B,H,W] 00000000
0x15C	-	-	-	WTCAL1[B,H,W] ------00
0x160	-	-	-	WTCALEN[B,H,W] -------0
0x164	-	-	-	WTDIV[B,H,W] ----0000
0x168	-	-	-	WTDIVEN[B,H,W] ------00
0x16C	-	-	-	WTCALPRD[B,H,W] --010011
0x170	-	-	-	WTCOSEL[B,H,W] -------0
0x174	-	-	-	VB_CLKDIV[B,H,W] 00000111
0x178	-	-	-	WTOSCCNT[B,H,W] ------01
0x17C	-	-	-	CCS[B,H,W] 00001000
0x180	-	-	-	CCB[B,H,W] 00010000
0x184	-	-	-	*
0x188	-	-	-	BOOST[B,H,W] ------11
0x18C	-	-	-	EWKUP[B,H,W] -------0
0x190	-	-	-	VDET[B,H,W] 00------
0x194	-	-	-	*
0x198	-	-	-	HIBRST[B,H,W] -------0
0x19C	-	-	-	VBPFR[B,H,W] --011100
0x1A0	-	-	-	VBPCR[B,H,W] ----0000
0x1A4	-	-	-	VBDDR[B,H,W] ----XXXX
0x1A8	-	-	-	VBDIR[B,H,W] ----0000
0x1AC	-	-	-	VBDOR[B,H,W] ----1111
0x0B0	-	-	-	VBPZR[B,H,W] ------11
0x1B4-1FF	-	-	-	-

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
0x200	BREG03[B,H,W] 00000000	BREG02[B,H,W] 00000000	BREG01[B,H,W] 00000000	BREG00[B,H,W] 00000000
0x204	BREG07[B,H,W] 00000000	BREG06[B,H,W] 00000000	BREG05[B,H,W] 00000000	BREG04[B,H,W] 00000000
0x208	BREG0B[B,H,W] 00000000	BREG0A[B,H,W] 00000000	BREG09[B,H,W] 00000000	BREG08[B,H,W] 00000000
0x20C	BREG0F[B,H,W] 00000000	BREG0E[B,H,W] 00000000	BREG0D[B,H,W] 00000000	BREG0C[B,H,W] 00000000
0x210	BREG13[B,H,W] 00000000	BREG12[B,H,W] 00000000	BREG11[B,H,W] 00000000	BREG10[B,H,W] 00000000
0x214	BREG17[B,H,W] 00000000	BREG16[B,H,W] 00000000	BREG15[B,H,W] 00000000	BREG14[B,H,W] 00000000
0x218	BREG1B[B,H,W] 00000000	BREG1A[B,H,W] 00000000	BREG19[B,H,W] 00000000	BREG18[B,H,W] 00000000
0x21C	BREG1F[B,H,W] 00000000	BREG1E[B,H,W] 00000000	BREG1D[B,H,W] 00000000	BREG1C[B,H,W] 00000000
0x220	BREG23[B,H,W] 00000000	BREG22[B,H,W] 00000000	BREG21[B,H,W] 00000000	BREG20[B,H,W] 00000000
0x224	BREG27[B,H,W] 00000000	BREG26[B,H,W] 00000000	BREG25[B,H,W] 00000000	BREG24[B,H,W] 00000000
0x228	BREG2B[B,H,W] 00000000	BREG2A[B,H,W] 00000000	BREG29[B,H,W] 00000000	BREG28[B,H,W] 00000000
0x22C	BREG2F[B,H,W] 00000000	BREG2E[B,H,W] 00000000	BREG2D[B,H,W] 00000000	BREG2C[B,H,W] 00000000
0x230	BREG33[B,H,W] 00000000	BREG32[B,H,W] 00000000	BREG31[B,H,W] 00000000	BREG30[B,H,W] 00000000
0x234	BREG37[B,H,W] 00000000	BREG36[B,H,W] 00000000	BREG35[B,H,W] 00000000	BREG34[B,H,W] 00000000
0x238	BREG3B[B,H,W] 00000000	BREG3A[B,H,W] 00000000	BREG39[B,H,W] 00000000	BREG38[B,H,W] 00000000
0x23C	BREG3F[B,H,W] 00000000	BREG3E[B,H,W] 00000000	BREG3D[B,H,W] 00000000	BREG3C[B,H,W] 00000000
0x240	BREG43[B,H,W] 00000000	BREG42[B,H,W] 00000000	BREG41[B,H,W] 00000000	BREG40[B,H,W] 00000000
0x244	BREG47[B,H,W] 00000000	BREG46[B,H,W] 00000000	BREG45[B,H,W] 00000000	BREG44[B,H,W] 00000000
0x248	BREG4B[B,H,W] 00000000	BREG4A[B,H,W] 00000000	BREG49[B,H,W] 00000000	BREG48[B,H,W] 00000000
0x24C	BREG4F[B,H,W] 00000000	BREG4E[B,H,W] 00000000	BREG4D[B,H,W] 00000000	BREG4C[B,H,W] 00000000
0x250	BREG53[B,H,W] 00000000	BREG52[B,H,W] 00000000	BREG51[B,H,W] 00000000	BREG50[B,H,W] 00000000
0x254	BREG57[B,H,W] 00000000	BREG56[B,H,W] 00000000	BREG55[B,H,W] 00000000	BREG54[B,H,W] 00000000
0x258	BREG5B[B,H,W] 00000000	BREG5A[B,H,W] 00000000	BREG59[B,H,W] 00000000	BREG58[B,H,W] 00000000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x25C	BREG5F[B,H,W] 00000000	BREG5E[B,H,W] 00000000	BREG5D[B,H,W] 00000000	BREG5C[B,H,W] 00000000
0x260	BREG63[B,H,W] 00000000	BREG62[B,H,W] 00000000	BREG61[B,H,W] 00000000	BREG60[B,H,W] 00000000
0x264	BREG67[B,H,W] 00000000	BREG66[B,H,W] 00000000	BREG65[B,H,W] 00000000	BREG64[B,H,W] 00000000
0x268	BREG6B[B,H,W] 00000000	BREG6A[B,H,W] 00000000	BREG69[B,H,W] 00000000	BREG68[B,H,W] 00000000
0x26C	BREG6F[B,H,W] 00000000	BREG6E[B,H,W] 00000000	BREG6D[B,H,W] 00000000	BREG6C[B,H,W] 00000000
0x270	BREG73[B,H,W] 00000000	BREG72[B,H,W] 00000000	BREG71[B,H,W] 00000000	BREG70[B,H,W] 00000000
0x274	BREG77[B,H,W] 00000000	BREG76[B,H,W] 00000000	BREG75[B,H,W] 00000000	BREG74[B,H,W] 00000000
0x278	BREG7B[B,H,W] 00000000	BREG7A[B,H,W] 00000000	BREG79[B,H,W] 00000000	BREG78[B,H,W] 00000000
0x27C	BREG7F[B,H,W] 00000000	BREG7E[B,H,W] 00000000	BREG7D[B,H,W] 00000000	BREG7C[B,H,W] 00000000
0x280-0xFFC	-	-	-	-

1.28.2 TYPE4-M4 Product

RTC Base_Address : 0x4003_B000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x100	-	-	-	WTCR10[B,H,W] 00000000
0x104	-	-	-	WTCR11[B,H,W] ---00000
0x108	-	-	-	WTCR12[B,H,W] 00000000
0x10C	-	-	-	WTCR13[B,H,W] 00000000
0x110	-	-	-	WTCR20[B,H,W] --000000
0x114	-	-	-	WTCR21[B,H,W] -----000
0x118	-	-	-	*
0x11C	-	-	-	WTSR[B,H,W] -0000000
0x120	-	-	-	WTMIR[B,H,W] -0000000
0x124	-	-	-	WTHR[B,H,W] --000000
0x128	-	-	-	WTDR[B,H,W] --000000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x12C	-	-	-	WTDW[B,H,W] -----000
0x130	-	-	-	WTMOR[B,H,W] ---00000
0x134	-	-	-	WTYR[B,H,W] 00000000
0x138	-	-	-	ALMIR[B,H,W] -0000000
0x13C	-	-	-	ALHR[B,H,W] --000000
0x140	-	-	-	ALDR[B,H,W] --000000
0x144	-	-	-	ALMOR[B,H,W] ---00000
0x148	-	-	-	ALYR[B,H,W] 00000000
0x14C	-	-	-	WTTR0[B,H,W] 00000000
0x150	-	-	-	WTTR1[B,H,W] 00000000
0x154	-	-	-	WTTR2[B,H,W] ------00
0x158	-	-	-	WTCAL0[B,H,W] 00000000
0x15C	-	-	-	WTCAL1[B,H,W] ------00
0x160	-	-	-	WTCALEN[B,H,W] -------0
0x164	-	-	-	WTDIV[B,H,W] ----0000
0x168	-	-	-	WTDIVEN[B,H,W] ------00
0x16C	-	-	-	WTCALPRD[B,H,W] --010011
0x170	-	-	-	WTCOSEL[B,H,W] -------0
0x174	-	-	-	VB_DIVCLK[B,H,W] 00000111
0x178	-	-	-	WTOSCCNT[B,H,W] ------01
0x17C	-	-	-	CCS[B,H,W] 11001110
0x180	-	-	-	CCB[B,H,W] 11001110
0x184	-	-	-	*

Base_Address + Address	Register			
	+3	+2	+1	+0
0x188	-	-	-	BOOST[B,H,W] ------11
0x18C	-	-	-	EWKUP[B,H,W] -------0
0x190	-	-	-	VDET[B,H,W] 00------
0x194	-	-	-	*
0x198	-	-	-	HIBRST[B,H,W] -------0
0x19C	-	-	-	VBPFR[B,H,W] --011100
0x1A0	-	-	-	VBPCR[B,H,W] ----0000
0x1A4	-	-	-	VBDDR[B,H,W] ----0000
0x1A8	-	-	-	VBDIR[B,H,W] ----XXXX
0x1AC	-	-	-	VBDOR[B,H,W] ----1111
0x1B0	-	-	-	VBPZR[B,H,W] ------11
0x1B4-1FF	-	-	-	-
0x200	BREG03[B,H,W]	BREG02[B,H,W]	BREG01[B,H,W]	BREG00[B,H,W]
	00000000	00000000	00000000	00000000
0x204	BREG07[B,H,W]	BREG06[B,H,W]	BREG05[B,H,W]	BREG04[B,H,W]
	00000000	00000000	00000000	00000000
0x208	BREG0B[B,H,W]	BREG0A[B,H,W]	BREG09[B,H,W]	BREG08[B,H,W]
	00000000	00000000	00000000	00000000
0x20C	BREG0F[B,H,W]	BREG0E[B,H,W]	BREG0D[B,H,W]	BREG0C[B,H,W]
	00000000	00000000	00000000	00000000
0x210	BREG13[B,H,W]	BREG12[B,H,W]	BREG11[B,H,W]	BREG10[B,H,W]
	00000000	00000000	00000000	00000000
0x214	BREG17[B,H,W]	BREG16[B,H,W]	BREG15[B,H,W]	BREG14[B,H,W]
	00000000	00000000	00000000	00000000
0x218	BREG1B[B,H,W]	BREG1A[B,H,W]	BREG19[B,H,W]	BREG18[B,H,W]
	00000000	00000000	00000000	00000000
0x21C	BREG1F[B,H,W]	BREG1E[B,H,W]	BREG1D[B,H,W]	BREG1C[B,H,W]
	00000000	00000000	00000000	00000000
0x220	BREG23[B,H,W]	BREG22[B,H,W]	BREG21[B,H,W]	BREG20[B,H,W]
	00000000	00000000	00000000	00000000
0x224	BREG27[B,H,W]	BREG26[B,H,W]	BREG25[B,H,W]	BREG24[B,H,W]
	00000000	00000000	00000000	00000000
0x228	BREG2B[B,H,W]	BREG2A[B,H,W]	BREG29[B,H,W]	BREG28[B,H,W]
	00000000	00000000	00000000	00000000
0x22C	BREG2F[B,H,W]	BREG2E[B,H,W]	BREG2D[B,H,W]	BREG2C[B,H,W]
	00000000	00000000	00000000	00000000
0x230	BREG33[B,H,W]	BREG32[B,H,W]	BREG31[B,H,W]	BREG30[B,H,W]

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
	00000000	00000000	00000000	00000000
0x234	BREG37[B,H,W]	BREG36[B,H,W]	BREG35[B,H,W]	BREG34[B,H,W]
	00000000	00000000	00000000	00000000
0x238	BREG3B[B,H,W]	BREG3A[B,H,W]	BREG39[B,H,W]	BREG38[B,H,W]
	00000000	00000000	00000000	00000000
0x23C	BREG3F[B,H,W]	BREG3E[B,H,W]	BREG3D[B,H,W]	BREG3C[B,H,W]
	00000000	00000000	00000000	00000000
0x240	BREG43[B,H,W]	BREG42[B,H,W]	BREG41[B,H,W]	BREG40[B,H,W]
	00000000	00000000	00000000	00000000
0x244	BREG47[B,H,W]	BREG46[B,H,W]	BREG45[B,H,W]	BREG44[B,H,W]
	00000000	00000000	00000000	00000000
0x248	BREG4B[B,H,W]	BREG4A[B,H,W]	BREG49[B,H,W]	BREG48[B,H,W]
	00000000	00000000	00000000	00000000
0x24C	BREG4F[B,H,W]	BREG4E[B,H,W]	BREG4D[B,H,W]	BREG4C[B,H,W]
	00000000	00000000	00000000	00000000
0x250	BREG53[B,H,W]	BREG52[B,H,W]	BREG51[B,H,W]	BREG50[B,H,W]
	00000000	00000000	00000000	00000000
0x254	BREG57[B,H,W]	BREG56[B,H,W]	BREG55[B,H,W]	BREG54[B,H,W]
	00000000	00000000	00000000	00000000
0x258	BREG5B[B,H,W]	BREG5A[B,H,W]	BREG59[B,H,W]	BREG58[B,H,W]
	00000000	00000000	00000000	00000000
0x25C	BREG5F[B,H,W]	BREG5E[B,H,W]	BREG5D[B,H,W]	BREG5C[B,H,W]
	00000000	00000000	00000000	00000000
0x260	BREG63[B,H,W]	BREG62[B,H,W]	BREG61[B,H,W]	BREG60[B,H,W]
	00000000	00000000	00000000	00000000
0x264	BREG67[B,H,W]	BREG66[B,H,W]	BREG65[B,H,W]	BREG64[B,H,W]
	00000000	00000000	00000000	00000000
0x268	BREG6B[B,H,W]	BREG6A[B,H,W]	BREG69[B,H,W]	BREG68[B,H,W]
	00000000	00000000	00000000	00000000
0x26C	BREG6F[B,H,W]	BREG6E[B,H,W]	BREG6D[B,H,W]	BREG6C[B,H,W]
	00000000	00000000	00000000	00000000
0x270	BREG73[B,H,W]	BREG72[B,H,W]	BREG71[B,H,W]	BREG70[B,H,W]
	00000000	00000000	00000000	00000000
0x274	BREG77[B,H,W]	BREG76[B,H,W]	BREG75[B,H,W]	BREG74[B,H,W]
	00000000	00000000	00000000	00000000
0x278	BREG7B[B,H,W]	BREG7A[B,H,W]	BREG79[B,H,W]	BREG78[B,H,W]
	00000000	00000000	00000000	00000000
0x27C	BREG7F[B,H,W]	BREG7E[B,H,W]	BREG7D[B,H,W]	BREG7C[B,H,W]
	00000000	00000000	00000000	00000000
0x280-0xFFC	-	-	-	-

1.28.3 TYPE5-M4 Product

RTC Base_Address : 0x4003_B000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	WTCR1 [B,H,W] 00000000 00000000 ---00000 -00000-0			
0x004	WTCR2[B,H,W] -------- -------- -----000 -------0			
0x008	WTBR [B,H,W] -------- 00000000 00000000 00000000			
0x00C	WTDR[B,H,W] --000000	WTHR[B,H,W] --000000	WTMIR[B,H,W] -0000000	WTSR[B,H,W] -0000000
0x010	-	WTYR[B,H,W] 00000000	WTMOR[B,H,W] ---00000	WTDW[B,H,W] -----000
0x014	ALDR[B,H,W] --000000	ALHR[B,H,W] --000000	ALMIR[B,H,W] -0000000	-
0x018	-	ALYR[B,H,W] 00000000	ALMOR[B,H,W] ---00000	-
0x01C	WTTR [B,H,W] -------- ------00 00000000 00000000			
0x020	-	-	WTCLKM[B,H,W] ------00	WTCLKS[B,H,W] -------0
0x024	-	WTCALEN[B,H,W] -------0	WTCAL[B,H,W] ------00 00000000	
0x028	-	-	WTDIVEN[B,H,W] ------00	WTDIV[B,H,W] ----0000
0x02C	-	-	-	WTCALPRD[B,H,W], --010011
0x030	-	-	-	WTCOSEL[B,H,W], -------0
0x034-0x0FF	-	-	-	-

1.29 Low-speed CR Prescaler

Low-speed CR Prescaler Base_Address : 0x4003_C000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	LCR_PRSLD[B,H,W], --000000
0x004 – 0x0FC	-	-	-	-

1.30 Peripheral Clock Gating

1.30.1 TYPE1-M1, TYPE2-M4 Products

Peripheral Clock Gating **Base_Address : 0x4003_C100**

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	CKEN0[B,H,W] ---1-1-1 ----1111 11111111 11111111			
0x004	MRST0[B,H,W] -----0-0 ----0000 00000000 00000000			
0x008 – 0x00F	-	-	-	-
0x010	CKEN1[B,H,W] -------- ----1111 ----1111 ----1111			
0x014	MRST1[B,H,W] -------- ----0000 ----0000 ----0000			
0x018 – 0x01F	-	-	-	-
0x020	CKEN2[B,H,W] -------- -------- -------0 --**--00 Products with CAN : *="1" Products without CAN : *="0"			
0x024	MRST2[B,H,W] -------- -------- -------0 --00--00			
0x028 – 0x67C	-	-	-	-

1.30.2 TYPE3-M4, TYPE4-M4 Products

Peripheral Clock Gating **Base_Address : 0x4003_C100**

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	CKEN0[B,H,W] ---1-1-1 ----1111 11111111 11111111			
0x004	MRST0[B,H,W] -----0-0 ----0000 00000000 00000000			
0x008 – 0x00F	-	-	-	-
0x010	CKEN1[B,H,W] -------- ----1111 ----1111 ----1111			
0x014	MRST1[B,H,W] -------- ----0000 ----0000 ----0000			
0x018 – 0x01F	-	-	-	-
0x020	CKEN2[B,H,W] ---0--11 ---1--00 -------0 -***--00 Products with : *="1" Products without CAN : *="0"			
0x024	MRST2[B,H,W] ---0--00 ---0--00 -------0 -000--00			
0x028 – 0x67C	-	-	-	-

1.30.3 TYPE5-M4, TYPE6-M4 Products

Peripheral Clock Gating **Base_Address : 0x4003_C100**

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	CKEN0[B,H,W] ---1-1-1 ----1111 11111111 11111111			
0x004	MRST0[B,H,W] -----0-0 ----0000 00000000 00000000			
0x008 – 0x00F	-	-	-	-
0x010	CKEN1[B,H,W] -------- ----1111 ----1111 ----1111			
0x014	MRST1[B,H,W] -------- ----0000 ----0000 ----0000			
0x018 – 0x01F	-	-	-	-
0x020	CKEN2[B,H,W] ---0--11 ---1--00 1111---0 -***--00 Products with : *="1" Products without CAN : *="0"			
0x024	MRST2[B,H,W] ---0--00 ---0--00 0000---0 -000--00			
0x028 – 0x67C	-	-	-	-

1.31 Smart Card Interface

Smart Card Interface ch.0 Base_Address : 0x4003_C900

Smart Card Interface ch.1 Base_Address : 0x4003_C980

Base_Address + Address	Register			
	+3	+2	+1	+0
0x00	-	-	GLOBALCONTROL1[H,W] -0001000 00000000	
0x04	-	-	STATUS[H,W] --000000 00000001	
0x08	-	-	PORTCONTROL[H,W] 0000--00 00-0-0-0	
0x0C	-	-	DATA[H,W] -------0 00000000	
0x10	-	-	CARDCLOCK [H,W] 00000000 00101000	
0x14	-	-	BAUDRATE[H,W] 0000001 01110100	
0x18	-	-	GUARDTIMER[H,W] -------- 00000000	
0x1C	-	-	IDLETIMER[H,W] 00000000 00000000	
0x20	-	-	GLOBALCONTROL2[H,W] -------- ----1-00	
0x24	-	-	DATA_FIFO[H,W] -------0 00000000	
0x28	-	-	FIFO_LEVEL_READ[H,W] 00000000 00000000	
0x2C	-	-	FIFO_LEVEL_WRITE[H,W] 00000000 00000000	
0x30	-	-	FIFO_MODE[H,W] 00000000 ----0000	
0x34	-	-	FIFO_CLEAR_MSB_WRITE[H,W] -------- -------0	
0x38	-	-	FIFO_CLEAR_MSB_ READ[H,W] -------- -------0	
0x3C	-	-	-	-
0x40	-	-	IRQ_STATUS[H,W] -------- 00000000	
0x44- 0x7C	-	-	-	-

1.32 MFSI2S

MFSI2S ch.A Base_Address : 0x4003_CA00

Base_Address + Address	Register			
	+3	+2	+1	+0
0x00	-	-	CNTLREG[B, H,W] -----0-0 -0000-01	
0x04	-	-	I2SCLK[B, H,W] 00------ 00000000	
0x08	-	-	I2SST[B,H,W] ------00	I2SRST[B,H,W] 00000000
0x0C- 0xFC	-	-	-	-

Note:

- *In TYPE5-M4 product, MFSI2S ch.A applies to MFS ch.1.*

1.33 I2S Prescaler

1.33.1 TYPE1-M4, TYPE2-M4, TYPE3-M4 Products

I2S_Prescaler **Base_Address : 0x4003_D000**

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	ICCR[B,H,W] -------- -------- -------- ------00			
0x004	IPCR1[B,H,W] -------- -------- -------- -------0			
0x008	IPCR2[B,H,W] -------- -------- -------- -----000			
0x00C	IPCR3[B,H,W] -------- -------- -------- ---00001			
0x010	IPCR4[B,H,W] -------- -------- -------- -0011111			
0x014	IP_STR[B,H,W] -------- -------- -------- -------0			
0x018	IPINT_ENR[B,H,W] -------- -------- -------- -------0			
0x01C	IPINT_CLR[B,H,W] -------- -------- -------- -------0			
0x020	IPINT_STR[B,H,W] -------- -------- -------- -------0			
0x024	IPCR5[B,H,W] -------- -------- -------- -0011000			
0x028 – 0xFFC	-	-	-	-

1.33.2 TYPE4-M4 Product

I2S_Prescaler **Base_Address : 0x4003_D000**

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	ICCR[B,H,W] -------- -------- -------- ------00			
0x004	IPCR1[B,H,W] -------- -------- -------- -------0			
0x008	IPCR2[B,H,W] -------- -------- -------- -----000			
0x00C	IPCR3[B,H,W] -------- -------- -------- ---00001			
0x010	IPCR4[B,H,W] -------- -------- -------- -0011111			
0x014	IP_STR[B,H,W] -------- -------- -------- -------0			
0x018	IPINT_ENR[B,H,W] -------- -------- -------- -------0			
0x01C	IPINT_CLR[B,H,W] -------- -------- -------- -------0			
0x020	IPINT_STR[B,H,W] -------- -------- -------- -------0			
0x024	IPCR5[B,H,W] -------- -------- -------- -0011000			
0x028 – 0x02C	-	-	-	-
0x030	ICCR_1[B,H,W] -------- -------- -------- -----000			
0x034	IPCR5_1[B,H,W] -------- -------- -------- -0000000			
0x038 – 0xFFC	-	-	-	-

1.34 GDC_Prescaler

GDC_Prescaler Base_Address : 0x4003_D100

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	GCCR[B,H,W] -------- -------- -------- -------0			
0x004	GPCR1[B,H,W] -------- -------- -------- ------00			
0x008	GPCR2[B,H,W] -------- -------- -------- -----000			
0x00C	GPCR3 [B,H,W] -------- -------- -------- ---00000			
0x010	GPCR4 [B,H,W] -------- -------- -------- -0000000			
0x014	GP_STR[B,H,W] -------- -------- -------- -------0			
0x018	GPINT_ENR[B,H,W] -------- -------- -------- -------0			
0x01C	GPINT_CLR[B,H,W] -------- -------- -------- -------0			
0x020	GPINT_STR[B,H,W] -------- -------- -------- -------0			
0x024	-	-	-	-
0x028	GCSR[B,H,W] -------- -------- ---0---0 ---0--00			
0x02C	GRCR[B,H,W] -------- -------- -------- -------0			
0x030	GMCR[B,H,W] -------- -------- -------- -------0			
0x034- 0xFFC	-	-	-	-

Note:

- *For the register details of GDC, refer to the Chapter:GDC.*

1.35 EXT-Bus I/F

1.35.1 TYPE1-M4 Product

EXT-Bus I/F Base_Address : 0x4003_F000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0000	MODE0[W] -------- -------- --000-00 00000000			
0x0004	MODE1[W] -------- -------- --000-00 00000000			
0x0008	MODE2[W] -------- -------- --000-00 00000000			
0x000C	MODE3[W] -------- -------- --000-00 00000000			
0x0010	MODE4[W] -------- -------- --000-00 00000001			
0x0014	MODE5[W] -------- -------- --000-00 00000000			
0x0018	MODE6[W] -------- -------- --000-00 00000000			
0x001C	MODE7[W] -------- -------- --000-00 00000000			
0x0020	TIM0[W] 00000101 01011111 11110000 00001111			
0x0024	TIM1[W] 00000101 01011111 11110000 00001111			
0x0028	TIM2[W] 00000101 01011111 11110000 00001111			
0x002C	TIM3[W] 00000101 01011111 11110000 00001111			
0x0030	TIM4[W] 00000101 01011111 11110000 00001111			
0x0034	TIM5[W] 00000101 01011111 11110000 00001111			
0x0038	TIM6[W] 00000101 01011111 11110000 00001111			
0x003C	TIM7[W] 00000101 01011111 11110000 00001111			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0040	AREA0[W] -------- -0001111 -------- 00000000			
0x0044	AREA1[W] -------- -0001111 -------- 00010000			
0x0048	AREA2[W] -------- -0001111 -------- 00100000			
0x004C	AREA3[W] -------- -0001111 -------- 00110000			
0x0050	AREA4[W] -------- -0001111 -------- 01000000			
0x0054	AREA5[W] -------- -0001111 -------- 01010000			
0x0058	AREA6[W] -------- -0001111 -------- 01100000			
0x005C	AREA7[W] -------- -0001111 -------- 01110000			
0x0060	ATIM0[W] -------- -------- ----0100 01011111			
0x0064	ATIM1[W] -------- -------- ----0100 01011111			
0x0068	ATIM2[W] -------- -------- ----0100 01011111			
0x006C	ATIM3[W] -------- -------- ----0100 01011111			
0x0070	ATIM4[W] -------- -------- ----0100 01011111			
0x0074	ATIM5[W] -------- -------- ----0100 01011111			
0x0078	ATIM6[W] -------- -------- ----0100 01011111			
0x007C	ATIM7[W] -------- -------- ----0100 01011111			
0x0080 - 0x00FC	-	-	-	-
0x0100	SDMODE[W] -------- -------0 00010011 --00-000			
0x0104	REFTIM[W] -------0 00000000 0000000000110011			
0x0108	PWRDWN[W] -------- -------- 00000000 00000000			
0x010C	SDTIM[W] ------00 01000010 00010001 0100--01			
0x0110	SDCMD[W] 0------- ---00000 00000000 00000000			
0x0114 - 0x01FC	-	-	-	-

A. Register Map

Base_Address + Address	Register			
	+3	+ 2	+1	+ 0
0x0200	MEMCERR[W] -------- -------- -------- ----0000			
0x0204 – 0x02FC	-	-	-	-
0x0300	DCLKR[W] -------- -------- -------- ---01111			
0x0304	EST -------- -------- -------- -------0			
0x0308	WEAD 00000000 00000000 000000000 00000000			
0x030C	ESCLR[W] -------- -------- -------- -------1			
0x0310	AMODE[W] -------- -------- -------- -------1			
0x031C - 0x0EFC	-	-	-	-
0x0F00 – 0x0F14	*	*	*	*
0x0F18 – 0x0FFC	-	-	-	-

1.35.2 TYPE3-M4, TYPE4-M4, TYPE5-M4, TYPE6-M4 Products

EXT-Bus I/F Base_Address : 0x4003_F000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0000	MODE0[W] -------- -------- --000-00 00000000			
0x0004	MODE1[W] -------- -------- --000-00 00000000			
0x0008	MODE2[W] -------- -------- --000-00 00000000			
0x000C	MODE3[W] -------- -------- --000-00 00000000			
0x0010	MODE4[W] -------- -------- --000-00 00000001			
0x0014	MODE5[W] -------- -------- --000-00 00000000			
0x0018	MODE6[W] -------- -------- --000-00 00000000			
0x001C	MODE7[W] -------- -------- --000-00 00000000			
0x0020	TIM0[W] 00000101 01011111 11110000 00001111			
0x0024	TIM1[W] 00000101 01011111 11110000 00001111			
0x0028	TIM2[W] 00000101 01011111 11110000 00001111			
0x002C	TIM3[W] 00000101 01011111 11110000 00001111			
0x0030	TIM4[W] 00000101 01011111 11110000 00001111			
0x0034	TIM5[W] 00000101 01011111 11110000 00001111			
0x0038	TIM6[W] 00000101 01011111 11110000 00001111			
0x003C	TIM7[W] 00000101 01011111 11110000 00001111			

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0040	AREA0[W] -------- -0001111 -------- 00000000			
0x0044	AREA1[W] -------- -0001111 -------- 00010000			
0x0048	AREA2[W] -------- -0001111 -------- 00100000			
0x004C	AREA3[W] -------- -0001111 -------- 00110000			
0x0050	AREA4[W] -------- -0001111 -------- 01000000			
0x0054	AREA5[W] -------- -0001111 -------- 01010000			
0x0058	AREA6[W] -------- -0001111 -------- 01100000			
0x005C	AREA7[W] -------- -0001111 -------- 01110000			
0x0060	ATIM0[W] -------- -------- ----0100 01011111			
0x0064	ATIM1[W] -------- -------- ----0100 01011111			
0x0068	ATIM2[W] -------- -------- ----0100 01011111			
0x006C	ATIM3[W] -------- -------- ----0100 01011111			
0x0070	ATIM4[W] -------- -------- ----0100 01011111			
0x0074	ATIM5[W] -------- -------- ----0100 01011111			
0x0078	ATIM6[W] -------- -------- ----0100 01011111			
0x007C	ATIM7[W] -------- -------- ----0100 01011111			
0x0080 - 0x00FC	-	-	-	-
0x0100	SDMODE[W] -------- -------0 00010011 --00-000			
0x0104	REFTIM[W] -------0 00000000 0000000000110011			
0x0108	PWRDWN[W] -------- -------- 00000000 00000000			
0x010C	SDTIM[W] 0-----00 01000010 00010001 0100--01			
0x0110	SDCMD[W] 0------- ---00000 00000000 00000000			
0x0114 - 0x01FC	-	-	-	-

Base_Address + Address	Register			
	+3	+ 2	+1	+ 0
0x0200	MEMCERR[W] -------- -------- -------- ----0000			
0x0204 – 0x02FC	-	-	-	-
0x0300	DCLKR[W] -------- -------- -------- ---01111			
0x0304	EST -------- -------- -------- -------0			
0x0308	WEAD 00000000 00000000 000000000 00000000			
0x030C	ESCLR[W] -------- -------- -------- -------1			
0x0310	AMODE[W] -------- -------- -------- -------1			
0x031C - 0x0EFC	-	-	-	-
0x0F00 – 0x0F14	*	*	*	*
0x0F18 – 0x0FFC	-	-	-	-

1.36 USB

USB ch.0 Base_Address : 0x4004_0000

USB ch.1 Base_Address : 0x4005_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x2100	-	-	HCNT1[B,H,W] -----001	HCNT0[B,H,W] 00000000
0x2104	-	-	HERR[B,H,W] 00000011	HIRQ[B,H,W] 0-000000
0x2108	-	-	HFCOMP[B,H,W] 00000000	HSTATE[B,H,W] --010010
0x210C	-	-	HRTIMER(1/0)[B,H,W] 00000000 00000000	
0x2110	-	-	HADR[B,H,W] -0000000	HRTIMER(2)[B,H,W] ------00
0x2114	-	-	HEOF(1/0)[B,H,W] --000000 00000000	
0x2118	-	-	HFRAME(1/0)[B,H,W] -----000 00000000	
0x211C	-	-	-	HTOKEN[B,H,W] 00000000
0x2120	-	-	UDCC[B,H,W] -------- 10100-00	
0x2124	-	-	EP0C[H,W] ------0- -1000000	
0x2128	-	-	EP1C[H,W] 01100001 00000000	
0x212C	-	-	EP2C[H,W] 0110000- -1000000	
0x2130	-	-	EP3C[H,W] 0110000- -1000000	
0x2134	-	-	EP4C[H,W] 0110000- -1000000	
0x2138	-	-	EP5C[H,W] 0110000- -1000000	
0x213C	-	-	TMSP[H,W] -----000 00000000	
0x2140	-	-	UDCIE[B,H,W] --000000	UDCS[B,H,W] --000000
0x2144	-	-	EP0IS[H,W] 10---1-- --------	
0x2148	-	-	EP0OS[H,W] 100--00- -XXXXXXX	
0x214C	-	-	EP1S[H,W] 100-000X XXXXXXXX	

Base_Address + Address	Register			
	+3	+2	+1	+0
0x2150	-	-	EP2S[H,W] 100-000- -XXXXXXX	
0x2154	-	-	EP3S[H,W] 100-000- -XXXXXXX	
0x2158	-	-	EP4S[H,W] 100-000- -XXXXXXX	
0x215C	-	-	EP5S[H,W] 100-000- -XXXXXXX	
0x2160	-	-	EP0DTH[B,H,W] XXXXXXXX	EP0DTL[B,H,W] XXXXXXXX
0x2164	-	-	EP1DTH[B,H,W] XXXXXXXX	EP1DTL[B,H,W] XXXXXXXX
0x2168	-	-	EP2DTH[B,H,W] XXXXXXXX	EP2DTL[B,H,W] XXXXXXXX
0x216C	-	-	EP3DTH[B,H,W] XXXXXXXX	EP3DTL[B,H,W] XXXXXXXX
0x2170	-	-	EP4DTH[B,H,W] XXXXXXXX	EP4DTL[B,H,W] XXXXXXXX
0x2174	-	-	EP5DTH[B,H,W] XXXXXXXX	EP5DTL[B,H,W] XXXXXXXX
0x2178 - 0x217C	-	-	-	-

1.37 DMAC

DMAC Base_Address : 0x4006_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0000	DMACR[B,H,W] 00-00000 -------- -------- --------			
0x0010	DMACA0[B,H,W] 00000000 0---0000 00000000 00000000			
0x0014	DMACB0[B,H,W] --000000 00000000 00000000 -------0			
0x0018	DMACSA0[B,H,W] 00000000 00000000 00000000 00000000			
0x001C	DMACDA0[B,H,W] 00000000 00000000 00000000 00000000			
0x0020	DMACA1[B,H,W] 00000000 0---0000 00000000 00000000			
0x0024	DMACB1[B,H,W] --000000 00000000 00000000 -------0			
0x0028	DMACSA1[B,H,W] 00000000 00000000 00000000 00000000			
0x002C	DMACDA1[B,H,W] 00000000 00000000 00000000 00000000			
0x0030	DMACA2[B,H,W] 00000000 0---0000 00000000 00000000			
0x0034	DMACB2[B,H,W] --000000 00000000 00000000 -------0			
0x0038	DMACSA2[B,H,W] 00000000 00000000 00000000 00000000			
0x003C	DMACDA2[B,H,W] 00000000 00000000 00000000 00000000			
0x0040	DMACA3[B,H,W] 00000000 0---0000 00000000 00000000			
0x0044	DMACB3[B,H,W] --000000 00000000 00000000 -------0			
0x0048	DMACSA3[B,H,W] 00000000 00000000 00000000 00000000			
0x004C	DMACDA3[B,H,W] 00000000 00000000 00000000 00000000			
0x0050	DMACA4[B,H,W] 00000000 0---0000 00000000 00000000			
0x0054	DMACB4[B,H,W] --000000 00000000 00000000 -------0			
0x0058	DMACSA4[B,H,W] 00000000 00000000 00000000 00000000			
0x005C	DMACDA4[B,H,W] 00000000 00000000 00000000 00000000			
0x0060	DMACA5[B,H,W] 00000000 0---0000 00000000 00000000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0064	DMACB5[B,H,W] --000000 00000000 00000000 -------0			
0x0068	DMACSA5[B,H,W] 00000000 00000000 00000000 00000000			
0x006C	DMACDA5[B,H,W] 00000000 00000000 00000000 00000000			
0x0070	DMACA6[B,H,W] 00000000 0---0000 00000000 00000000			
0x0074	DMACB6[B,H,W] --000000 00000000 00000000 -------0			
0x0078	DMACSA6[B,H,W] 00000000 00000000 00000000 00000000			
0x007C	DMACDA6[B,H,W] 00000000 00000000 00000000 00000000			
0x0080	DMACA7[B,H,W] 00000000 0---0000 00000000 00000000			
0x0084	DMACB7[B,H,W] --000000 00000000 00000000 -------0			
0x0088	DMACSA7[B,H,W] 00000000 00000000 00000000 00000000			
0x008C	DMACDA7[B,H,W] 00000000 00000000 00000000 00000000			
0x0090 - 0x00FC	-	-	-	-

1.38 DSTC

DSTC Base_Address : 0x4006_1000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0000	DESTP[B,H,W] 00000000 00000000 00000000 00000000			
0x0004	HWDESP[B,H,W] 00XXXXXX XXXXXX00 00000000 00000000			
0x0008	SWTR[H] 00000000 00000000		CFG[B] 01000000	CMD[B] 00000001
0x000C	MONERS[B,H,W] 00XXXXXX XXXXXX00 XXXXXXXX XXX00000			
0x0010	DREQENB[31:0] [B,H,W] 00000000 00000000 00000000 00000000			
0x0014	DREQENB[63:32] [B,H,W] 00000000 00000000 00000000 00000000			
0x0018	DREQENB[95:64] [B,H,W] 00000000 00000000 00000000 00000000			
0x001C	DREQENB[127:96] [B,H,W] 00000000 00000000 00000000 00000000			
0x0020	DREQENB[159:128] [B,H,W] 00000000 00000000 00000000 00000000			
0x0024	DREQENB[191:160] [B,H,W] 00000000 00000000 00000000 00000000			
0x0028	DREQENB[223:192] [B,H,W] 00000000 00000000 00000000 00000000			
0x002C	DREQENB[255:224] [B,H,W] 00000000 00000000 00000000 00000000			
0x0030	HWINT[31:0] [B,H,W] 00000000 00000000 00000000 00000000			
0x0034	HWINT[63:32] [B,H,W] 00000000 00000000 00000000 00000000			
0x0038	HWINT[95:64] [B,H,W] 00000000 00000000 00000000 00000000			
0x003C	HWINT[127:96] [B,H,W] 00000000 00000000 00000000 00000000			
0x0040	HWINT[159:128] [B,H,W] 00000000 00000000 00000000 00000000			
0x0044	HWINT[191:160] [B,H,W] 00000000 00000000 00000000 00000000			
0x0048	HWINT[223:192] [B,H,W] 00000000 00000000 00000000 00000000			
0x004C	HWINT[255:224] [B,H,W] 00000000 00000000 00000000 00000000			
0x0050	HWINTCLR[31:0] [B,H,W] 00000000 00000000 00000000 00000000			
0x0054	HWINTCLR[63:32] [B,H,W] 00000000 00000000 00000000 00000000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0058	HWINTCLR[95:64] [B,H,W] 00000000 00000000 00000000 00000000			
0x005C	HWINTCLR[127:96] [B,H,W] 00000000 00000000 00000000 00000000			
0x060	HWINTCLR[159:128] [B,H,W] 00000000 00000000 00000000 00000000			
0x064	HWINTCLR[191:160] [B,H,W] 00000000 00000000 00000000 00000000			
0x068	HWINTCLR[223:192] [B,H,W] 00000000 00000000 00000000 00000000			
0x06C	HWINTCLR[255:224] [B,H,W] 00000000 00000000 00000000 00000000			
0x070	DQMSK[31:0] [B,H,W] 00000000 00000000 00000000 00000000			
0x074	DQMSK[63:32] [B,H,W] 00000000 00000000 00000000 00000000			
0x078	DQMSK[95:64] [B,H,W] 00000000 00000000 00000000 00000000			
0x07C	DQMSK[127:96] [B,H,W] 00000000 00000000 00000000 00000000			
0x080	DQMSK[159:128] [B,H,W] 00000000 00000000 00000000 00000000			
0x084	DQMSK[191:160] [B,H,W] 00000000 00000000 00000000 00000000			
0x088	DQMSK[223:192] [B,H,W] 00000000 00000000 00000000 00000000			
0x08C	DQMSK[255:224] [B,H,W] 00000000 00000000 00000000 00000000			
0x090	DQMSKCLR[31:0] [B,H,W] 00000000 00000000 00000000 00000000			
0x094	DQMSKCLR[63:32] [B,H,W] 00000000 00000000 00000000 00000000			
0x098	DQMSKCLR[95:64] [B,H,W] 00000000 00000000 00000000 00000000			
0x09C	DQMSKCLR[127:96] [B,H,W] 00000000 00000000 00000000 00000000			
0x0A0	DQMSKCLR[159:128] [B,H,W] 00000000 00000000 00000000 00000000			
0x0A4	DQMSKCLR[191:160] [B,H,W] 00000000 00000000 00000000 00000000			
0x0A8	DQMSKCLR[223:192] [B,H,W] 00000000 00000000 00000000 00000000			
0x0AC	DQMSKCLR[255:224] [B,H,W] 00000000 00000000 00000000 00000000			
0x00B0 - 0x0FFC	-	-	-	-

1.39 CAN

CAN ch.0 Base_Address : 0x4006_2000

CAN ch.1 Base_Address : 0x4006_3000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0000	STATR[B,H,W] -------- 00000000		CTRLR[B,H,W] -------- 000-0001	
0x0004	BTR[B,H,W] -0100011 00000001		ERRCNT[B,H,W] 00000000 00000000	
0x0008	TESTR[B,H,W] -------- X00000--		INTR[B,H,W] 00000000 00000000	
0x000C	-	-	BRPER[B,H,W] -------- ----0000	
0x0010	IF1CMSK[B,H,W] -------- 00000000		IF1CREQ[B,H,W] 0------- 00000001	
0x0014	IF1MSK2[B,H,W] 11-11111 11111111		IF1MSK1[B,H,W] 11111111 11111111	
0x0018	IF1ARB2[B,H,W] 00000000 00000000		IF1ARB1[B,H,W] 00000000 00000000	
0x001C	-	-	IF1MCTR[B,H,W] 00000000 0---0000	
0x0020	IF1DTA2[B,H,W] 00000000 00000000		IF1DTA1[B,H,W] 00000000 00000000	
0x0024	IF1DTB2[B,H,W] 00000000 00000000		IF1DTB1[B,H,W] 00000000 00000000	
0x0028 - 0x002F	-	-	-	-
0x0030	IF1DTA1[B,H,W] 00000000 00000000		IF1DTA2[B,H,W] 00000000 00000000	
0x0034	IF1DTB1[B,H,W] 00000000 00000000		IF1DTB2[B,H,W] 00000000 00000000	
0x0038 - 0x003C	-	-	-	-
0x0040	IF2CMSK[B,H,W] -------- 00000000		IF2CREQ[B,H,W] 0------- 00000001	
0x0044	IF2MSK2[B,H,W] 11-11111 11111111		IF2MSK1[B,H,W] 11111111 11111111	
0x0048	IF2ARB2[B,H,W] 00000000 00000000		IF2ARB1[B,H,W] 00000000 00000000	
0x004C	-	-	IF2MCTR[B,H,W] 00000000 0---0000	
0x0050	IF2DTA2[B,H,W] 00000000 00000000		IF2DTA1[B,H,W] 00000000 00000000	
0x0054	IF2DTB2[B,H,W] 00000000 00000000		IF2DTB1[B,H,W] 00000000 00000000	
0x0058 - 0x005C	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0060	IF2DTA1[B,H,W] 00000000 00000000		IF2DTA2[B,H,W] 00000000 00000000	
0x0064	IF2DTB1[B,H,W] 00000000 00000000		IF2DTB2[B,H,W] 00000000 00000000	
0x0068 - 0x007C	-	-	-	-
0x0080	TREQR2[B,H,W] 00000000 00000000		TREQR1[B,H,W] 00000000 00000000	
0x0084 - 0x008F	-	-	-	-
0x0090	NEWDT2[B,H,W] 00000000 00000000		NEWDT1[B,H,W] 00000000 00000000	
0x0094 - 0x009F	-	-	-	-
0x00A0	INTPND2[B,H,W] 00000000 00000000		INTPND1[B,H,W] 00000000 00000000	
0x00A4 - 0x00AF	-	-	-	-
0x00B0	MSGVAL2[B,H,W] 00000000 00000000		MSGVAL1[B,H,W] 00000000 00000000	
0x00B4 - 0x0FFC	-	-	-	-

1.40 Ethernet-MAC

Ethernet-MAC Base_Address : 0x4006_4000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0000 – 0x1FFC	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX

Note:

- *For the register details of Ethernet-MAC block, refer to the "Ethernet part".*

1.41 Ethernet-Control

Ethernet-Control Base_Address : 0x4006_6000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000 - 0xFFC	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX

Note:

- *For the register details of Ethernet-Control block, refer to the Ethernet part.*

1.42 I2S

I2S ch.0 Base_Address : 0x4006_C000

I2S ch.1 Base_Address : 0x4006_C800

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	RXFDAT[B,H,W] 00000000 00000000 00000000 00000000			
0x004	TXFDAT[B,H,W] 00000000 00000000 00000000 00000000			
0x008	CNTREG[B,H,W] 00000000 00000000 00000000 00000000			
0x00C	MCR0REG[B,H,W] -0000000 00000000 -0000000 00000000			
0x010	MCR1REG[B,H,W] 00000000 00000000 00000000 00000000			
0x014	MCR2REG[B,H,W] 00000000 00000000 00000000 00000000			
0x018	OPRREG[B,H,W] -------0 -------0 -------- -------0			
0x01C	SRST[B,H,W] -------- -------- -------- -------0			
0x020	INTCNT[B,H,W] -1111111 --111111 ----0000 --000000			
0x024	STATUS[B,H,W] 00000000 ----0000 00000000 00000000			
0x028	DMAACT[B,H,W] -------0 -------0 -------0 -------0			
0x02C	TSTREG[B,H,W] -------- -------- -------- -------0			
0x030 - 0xFFC	-	-	-	-

1.43 SD-Card

SD-Card Base_Address : 0x4006_E000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000 – 0xFFC	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX

Note:

- *For the register details of SD-Card block, refer to the Chapter SD Card Interface.*

1.44 CAN FD

CAN FD Base_Address : 0x4007_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	CREL[B,H,W] 00110000 00010011 00000101 0000110			
0x004	ENDN[B,H,W] 10000111 01100101 01000011 00100001			
0x008	-	-	-	-
0x00C	FBTP[B,H,W] ---00000 0--00000 ----1010 -011--11			
0x010	TEST[B,H,W] -------- -------- --000000 X000----			
0x014	RWD[B,H,W] -------- -------- 00000000 00000000			
0x018	CCCR[B,H,W] -------- -------- -0000000 00000001			
0x01C	BTP[B,H,W] ------00 00000000 --001010 00110011			
0x020	TSCC[B,H,W] -------- ----0000 -------- ------00			
0x024	TSCV[B,H,W] -------- -------- 00000000 00000000			
0x028	TOCC[B,H,W] 11111111 11111111 -------- -----000			
0x02C	TOCV[B,H,W] -------- -------- 11111111 11111111			
0x030 - 0x03C	-	-	-	-
0x040	ECR[B,H,W] -------- 00000000 00000000 00000000			
0x044	PSR[B,H,W] -------- -------- --000111 00000111			
0x048 - 0x04C	-	-	-	-
0x050	IR[B,H,W] 00000000 00000000 00000000 00000000			
0x054	IE[B,H,W] 00000000 00000000 00000000 00000000			
0x058	ILS[B,H,W] 00000000 00000000 00000000 00000000			
0x05C	ILE[B,H,W] -------- -------- -------- ------00			
0x060 - 0x07C	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x080	GFC[B,H,W] -------- -------- -------- --000000			
0x084	SIDFC[B,H,W] -------- 00000000 00000000 000000--			
0x088	XIDFC[B,H,W] -------- -0000000 00000000 000000--			
0x08C	-	-	-	-
0x090	XIDAM[B,H,W] ---11111 11111111 11111111 11111111			
0x094	HPMS[B,H,W] -------- -------- 00000000 00000000			
0x098	NDAT1[B,H,W] 00000000 00000000 00000000 00000000			
0x09C	NDAT2[B,H,W] 00000000 00000000 00000000 00000000			
0x0A0	RXF0C[B,H,W] 00000000 -0000000 00000000 000000--			
0x0A4	RXF0S[B,H,W] ------00 --000000 --000000 -0000000			
0x0A8	RXF0A[B,H,W] -------- -------- -------- --000000			
0x0AC	RXBC[B,H,W] -------- -------- 00000000 000000--			
0x0B0	RXF1C[B,H,W] 00000000 -0000000 00000000 000000--			
0x0B4	RXF1S[B,H,W] 00----00 --000000 --000000 -0000000			
0x0B8	RXF1A[B,H,W] -------- -------- -------- --000000			
0x0BC	RXESC[B,H,W] -------- -------- -----000 -000-000			
0x0C0	TXBC[B,H,W] -0000000 --000000 00000000 000000--			
0x0C4	TXFQS[B,H,W] -------- --000000 ---00000 –000000			
0x0C8	TXESC[B,H,W] -------- -------- -------- -----000			
0x0CC	TXBRP[B,H,W] 00000000 00000000 00000000 00000000			
0x0D0	TXBAR[B,H,W] 00000000 00000000 00000000 00000000			
0x0D4	TXBCR[B,H,W] 00000000 00000000 00000000 00000000			
0x0D8	TXBTO[B,H,W] 00000000 00000000 00000000 00000000			
0x0DC	TXBCF[B,H,W] 00000000 00000000 00000000 00000000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0E0	TXBTIE[B,H,W] 00000000 00000000 00000000 00000000			
0x0E4	TXBCIE[B,H,W] 00000000 00000000 00000000 00000000			
0x0E8 - 0x0EC	-	-	-	-
0x0F0	TXEFC[B,H,W] --000000 --000000 00000000 000000--			
0x0F4	TXEFS[B,H,W] ------00 ---00000 ---00000 --000000			
0x0F8	TXEFA[B,H,W] -------- -------- -------- ---00000			
0x0FC - 0x1FC	-	-	-	-
0x200	FDSEAR[B,H,W] 00000000 00000000		FDESR[B,H,W] ------00	FDECR[B,H,W] ----0000
0x204	FDDEAR[B,H,W] 00000000 00000000		FDESCR[B,H,W] ------00	-
0x208	FDFECR[B,H,W] 0------- -----000 00000000 00000000			
0x20C	-	-	-	-
0x210	TSMDR[B,H,W] -------- -------0		TSCNTR[B,H,W] -------- -------0	
0x214	TSDIVR[B,H,W] -------- -------- 00000000 00000000			
0x218	TSCPCLR[B,H,W] 00000000 00000000		TSCDTR[B,H,W] 00000000 00000000	
0x21C - 0xFFC	-	-	-	-

CAN FD Message RAM

Base_Address + Address	Message RAM			
	+3	+2	+1	+0
0x8000 - 0xBFFC	Rx Buffer and FIFO Element [W] Tx Buffer Element [W] Tx Event FIFO Element [W] Standard Message ID Filter Element [W] Extended Message ID Filter Element [W]			

Note:

- *For the register details of CAN FD Message RAM block, refer to the Chapter CAN FD Controller.*

1.45 Programmable-CRC

Programmable-CRC Base_Address : 0x4008_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	CRCn_PORY[B,H,W] 00000100 11000001 00011101 10110111			
0x004	CRCn_SEED[B,H,W] 11111111 11111111 11111111 11111111			
0x008	CRCn_FXOR[B,H,W] 11111111 11111111 11111111 11111111			
0x00C	CRCn_CFG[B,H,W] 00000000 11100000 00000000 00000000			
0x010	CRCn_WR[B,H,W] 00000000 00000000 00000000 00000000			
0x014	CRCn_RD[B,H,W] 00000000 00000000 00000000 00000000			
0x018 - 0xFFC	-	-	-	-

1.46 WorkFlash_IF

WorkFlash_IF Base_Address : 0x200E_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	WFASZR[B,H,W]			
0x004	WFRWTR[B,H,W]			
0x008	WFSTR[B,H,W]			
0x00C - 0xFFF	-	-	-	-

Note:

- *For the register details of Workflash IF block, refer to the Flash Programming Manual of the product used.*

1.47 High-Speed Quad SPI Controller

1.47.1 TYPE1-M4, TYPE2-M4, TYPE3-M4 Products

High-Speed Quad SPI Controller Base_Address : 0xD000_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	HSSPIn_MCTRL[B,H,W] -------- -------- -------- --000-00			
0x004	HSSPIn_PCC0[B,H,W] -------- -1111111 00000000 00000000			
0x008	HSSPIn_PCC1[B,H,W] -------- -1111111 00000000 00000000			
0x00C	HSSPIn_PCC2[B,H,W] -------- -1111111 00000000 00000000			
0x010	HSSPIn_PCC3[B,H,W] -------- -1111111 00000000 00000000			
0x014	HSSPIn_TXF[B,H,W] -------- -------- -------- -0000000			
0x018	HSSPIn_TXE[B,H,W] -------- -------- -------- -0000000			
0x01C	HSSPIn_TXC[B,H,W] -------- -------- -------- -0000000			
0x020	HSSPIn_RXF[B,H,W] -------- -------- -------- -0000000			
0x024	HSSPIn_RXE[B,H,W] -------- -------- -------- -0000000			
0x028	HSSPIn_RXC[B,H,W] -------- -------- -------- -0000000			
0x02C	HSSPIn_FAULTF[B,H,W] -------- -------- -------- ---00000			
0x030	HSSPIn_FAULTC[B,H,W] -------- -------- -------- ---00000			
0x034	-	-	HSSPIn_DMDMAEN [B,H,W] ------00	HSSPIn_DMCFG [B,H,W] -----001
0x038	HSSPIn_DMTRP [B,H,W] ----0000	HSSPIn_DMPSEL [B,H,W] ------00	HSSPIn_DMSTOP [B,H,W] -------0	HSSPIn_DMSTART [B,H,W] -------0
0x03C	HSSPIn_DMBCS[B,H,W] 00000000 00000000		HSSPIn_DMBCC[B,H,W] 00000000 00000000	
0x040	HSSPIn_DMSTATUS[B,H,W] -------- ---00000 ---00000 ------00			
0x044	-	-	-	-
0x048	-	-	-	-
0x04C	HSSPIn_FIFOCFG[B,H,W] --------_--------_---00000_01110111			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x050	HSSPIn_TXFIFO0[B,H,W] 00000000 00000000 00000000 00000000			
0x054	HSSPIn_TXFIFO1[B,H,W] 00000000 00000000 00000000 00000000			
0x058	HSSPIn_TXFIFO2[B,H,W] 00000000 00000000 00000000 00000000			
0x05C	HSSPIn_TXFIFO3[B,H,W] 00000000 00000000 00000000 00000000			
0x060	HSSPIn_TXFIFO4[B,H,W] 00000000 00000000 00000000 00000000			
0x064	HSSPIn_TXFIFO5[B,H,W] 00000000 00000000 00000000 00000000			
0x068	HSSPIn_TXFIFO6[B,H,W] 00000000 00000000 00000000 00000000			
0x06C	HSSPIn_TXFIFO7[B,H,W] 00000000 00000000 00000000 00000000			
0x070	HSSPIn_TXFIFO8[B,H,W] 00000000 00000000 00000000 00000000			
0x074	HSSPIn_TXFIFO9[B,H,W] 00000000 00000000 00000000 00000000			
0x078	HSSPIn_TXFIFO10[B,H,W] 00000000 00000000 00000000 00000000			
0x07C	HSSPIn_TXFIFO11[B,H,W] 00000000 00000000 00000000 00000000			
0x080	HSSPIn_TXFIFO12[B,H,W] 00000000 00000000 00000000 00000000			
0x084	HSSPIn_TXFIFO13[B,H,W] 00000000 00000000 00000000 00000000			
0x088	HSSPIn_TXFIFO14[B,H,W] 00000000 00000000 00000000 00000000			
0x08C	HSSPIn_TXFIFO15[B,H,W] 00000000 00000000 00000000 00000000			
0x090	HSSPIn_RXFIFO0[B,H,W] 00000000 00000000 00000000 00000000			
0x094	HSSPIn_RXFIFO1[B,H,W] 00000000 00000000 00000000 00000000			
0x098	HSSPIn_RXFIFO2[B,H,W] 00000000 00000000 00000000 00000000			
0x09C	HSSPIn_RXFIFO3[B,H,W] 00000000 00000000 00000000 00000000			
0x0A0	HSSPIn_RXFIFO4[B,H,W] 00000000 00000000 00000000 00000000			
0x0A4	HSSPIn_RXFIFO5[B,H,W] 00000000 00000000 00000000 00000000			
0x0A8	HSSPIn_RXFIFO6[B,H,W] 00000000 00000000 00000000 00000000			
0x0AC	HSSPIn_RXFIFO7[B,H,W] 00000000 00000000 00000000 00000000			
0x0B0	HSSPIn_RXFIFO8[B,H,W] 00000000 00000000 00000000 00000000			

A. Register Map

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0B4	HSSPIn_RXFIFO9[B,H,W] 00000000 00000000 00000000 00000000			
0x0B8	HSSPIn_RXFIFO10[B,H,W] 00000000 00000000 00000000 00000000			
0x0BC	HSSPIn_RXFIFO11[B,H,W] 00000000 00000000 00000000 00000000			
0x0C0	HSSPIn_RXFIFO12[B,H,W] 00000000 00000000 00000000 00000000			
0x0C4	HSSPIn_RXFIFO13[B,H,W] 00000000 00000000 00000000 00000000			
0x0C8	HSSPIn_RXFIFO14[B,H,W] 00000000 00000000 00000000 00000000			
0x0CC	HSSPIn_RXFIFO15[B,H,W] 00000000 00000000 00000000 00000000			
0x0D0	HSSPIn_CSCFG[B,H,W] -------- ----0000 ----0000 --000000			
0x0D4	HSSPIn_CSITIME[B,H,W] -------- -------- 11111111 11111111			
0x0D8	HSSPIn_CSAEXT[B,H,W] 00000000 00000000 000----- --------			
0x0DC	HSSPIn_RDCSDC1[B,H,W] 00000000 ----0000		HSSPIn_RDCSDC0[B,H,W] 00000000 ----0000	
0x0E0	HSSPIn_RDCSDC3[B,H,W] 00000000 ----0000		HSSPIn_RDCSDC2[B,H,W] 00000000 ----0000	
0x0E4	HSSPIn_RDCSDC5[B,H,W] 00000000 ----0000		HSSPIn_RDCSDC4[B,H,W] 00000000 ----0000	
0x0E8	HSSPIn_RDCSDC7[B,H,W] 00000000 ----0000		HSSPIn_RDCSDC6[B,H,W] 00000000 ----0000	
0x0EC	HSSPIn_WRCSDC1[B,H,W] 00000000 ----0000		HSSPIn_WRCSDC0[B,H,W] 00000000 ----0000	
0x0F0	HSSPIn_WRCSDC3[B,H,W] 00000000 ----0000		HSSPIn_WRCSDC2[B,H,W] 00000000 ----0000	
0x0F4	HSSPIn_WRCSDC5[B,H,W] 00000000 ----0000		HSSPIn_WRCSDC4[B,H,W] 00000000 ----0000	
0x0F8	HSSPIn_WRCSDC7[B,H,W] 00000000 ----0000		HSSPIn_WRCSDC6[B,H,W] 00000000 ----0000	
0x0FC	HSSPIn_MID[B,H,W] 00000000 00000000 00000110 00110000			
0x100 - 0x3FC	-	-	-	-
0x400	-	-	-	QDCLKR[B,H,W] ----1111
0x404	-	-	-	DBCNT[B,H,W] ------00
0x408 - 0xFFC	-	-	-	-

1.47.2 TYPE4-M4 Product

High-Speed Quad SPI Controller Base_Address : 0xD0A0_4000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	HSSPIn_MCTRL[B,H,W] -------- -------- -------- --000-00			
0x004	HSSPIn_PCC0[B,H,W] -------- -1111111 00000000 00000000			
0x008	HSSPIn_PCC1[B,H,W] -------- -1111111 00000000 00000000			
0x00C	HSSPIn_PCC2[B,H,W] -------- -1111111 00000000 00000000			
0x010	HSSPIn_PCC3[B,H,W] -------- -1111111 00000000 00000000			
0x014	HSSPIn_TXF[B,H,W] -------- -------- -------- -0000000			
0x018	HSSPIn_TXE[B,H,W] -------- -------- -------- -0000000			
0x01C	HSSPIn_TXC[B,H,W] -------- -------- -------- -0000000			
0x020	HSSPIn_RXF[B,H,W] -------- -------- -------- -0000000			
0x024	HSSPIn_RXE[B,H,W] -------- -------- -------- -0000000			
0x028	HSSPIn_RXC[B,H,W] -------- -------- -------- -0000000			
0x02C	HSSPIn_FAULTF[B,H,W] -------- -------- -------- ---00000			
0x030	HSSPIn_FAULTC[B,H,W] -------- -------- -------- ---00000			
0x034	-	-	HSSPIn_DMDMAEN [B,H,W] ------00	HSSPIn_DMCFG [B,H,W] -----001
0x038	HSSPIn_DMTRP [B,H,W] ----0000	HSSPIn_DMPSEL [B,H,W] ------00	HSSPIn_DMSTOP [B,H,W] -------0	HSSPIn_DMSTART [B,H,W] -------0
0x03C	HSSPIn_DMBCS[B,H,W] 00000000 00000000		HSSPIn_DMBCC[B,H,W] 00000000 00000000	
0x040	HSSPIn_DMSTATUS[B,H,W] -------- ---00000 ---00000 ------00			
0x044	-	-	-	-
0x048	-	-	-	-
0x04C	HSSPIn_FIFOCFG[B,H,W] --------_--------_---00000_01110111			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x050	HSSPIn_TXFIFO0[B,H,W] 00000000 00000000 00000000 00000000			
0x054	HSSPIn_TXFIFO1[B,H,W] 00000000 00000000 00000000 00000000			
0x058	HSSPIn_TXFIFO2[B,H,W] 00000000 00000000 00000000 00000000			
0x05C	HSSPIn_TXFIFO3[B,H,W] 00000000 00000000 00000000 00000000			
0x060	HSSPIn_TXFIFO4[B,H,W] 00000000 00000000 00000000 00000000			
0x064	HSSPIn_TXFIFO5[B,H,W] 00000000 00000000 00000000 00000000			
0x068	HSSPIn_TXFIFO6[B,H,W] 00000000 00000000 00000000 00000000			
0x06C	HSSPIn_TXFIFO7[B,H,W] 00000000 00000000 00000000 00000000			
0x070	HSSPIn_TXFIFO8[B,H,W] 00000000 00000000 00000000 00000000			
0x074	HSSPIn_TXFIFO9[B,H,W] 00000000 00000000 00000000 00000000			
0x078	HSSPIn_TXFIFO10[B,H,W] 00000000 00000000 00000000 00000000			
0x07C	HSSPIn_TXFIFO11[B,H,W] 00000000 00000000 00000000 00000000			
0x080	HSSPIn_TXFIFO12[B,H,W] 00000000 00000000 00000000 00000000			
0x084	HSSPIn_TXFIFO13[B,H,W] 00000000 00000000 00000000 00000000			
0x088	HSSPIn_TXFIFO14[B,H,W] 00000000 00000000 00000000 00000000			
0x08C	HSSPIn_TXFIFO15[B,H,W] 00000000 00000000 00000000 00000000			
0x090	HSSPIn_RXFIFO0[B,H,W] 00000000 00000000 00000000 00000000			
0x094	HSSPIn_RXFIFO1[B,H,W] 00000000 00000000 00000000 00000000			
0x098	HSSPIn_RXFIFO2[B,H,W] 00000000 00000000 00000000 00000000			
0x09C	HSSPIn_RXFIFO3[B,H,W] 00000000 00000000 00000000 00000000			
0x0A0	HSSPIn_RXFIFO4[B,H,W] 00000000 00000000 00000000 00000000			
0x0A4	HSSPIn_RXFIFO5[B,H,W] 00000000 00000000 00000000 00000000			
0x0A8	HSSPIn_RXFIFO6[B,H,W] 00000000 00000000 00000000 00000000			
0x0AC	HSSPIn_RXFIFO7[B,H,W] 00000000 00000000 00000000 00000000			
0x0B0	HSSPIn_RXFIFO8[B,H,W] 00000000 00000000 00000000 00000000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0B4	HSSPIn_RXFIFO9[B,H,W] 00000000 00000000 00000000 00000000			
0x0B8	HSSPIn_RXFIFO10[B,H,W] 00000000 00000000 00000000 00000000			
0x0BC	HSSPIn_RXFIFO11[B,H,W] 00000000 00000000 00000000 00000000			
0x0C0	HSSPIn_RXFIFO12[B,H,W] 00000000 00000000 00000000 00000000			
0x0C4	HSSPIn_RXFIFO13[B,H,W] 00000000 00000000 00000000 00000000			
0x0C8	HSSPIn_RXFIFO14[B,H,W] 00000000 00000000 00000000 00000000			
0x0CC	HSSPIn_RXFIFO15[B,H,W] 00000000 00000000 00000000 00000000			
0x0D0	HSSPIn_CSCFG[B,H,W] -------- ----0000 ----0000 --000000			
0x0D4	HSSPIn_CSITIME[B,H,W] -------- -------- 11111111 11111111			
0x0D8	HSSPIn_CSAEXT[B,H,W] 00000000 00000000 000----- --------			
0x0DC	HSSPIn_RDCSDC1[B,H,W] 00000000 ----0000		HSSPIn_RDCSDC0[B,H,W] 00000000 ----0000	
0x0E0	HSSPIn_RDCSDC3[B,H,W] 00000000 ----0000		HSSPIn_RDCSDC2[B,H,W] 00000000 ----0000	
0x0E4	HSSPIn_RDCSDC5[B,H,W] 00000000 ----0000		HSSPIn_RDCSDC4[B,H,W] 00000000 ----0000	
0x0E8	HSSPIn_RDCSDC7[B,H,W] 00000000 ----0000		HSSPIn_RDCSDC6[B,H,W] 00000000 ----0000	
0x0EC	HSSPIn_WRCSDC1[B,H,W] 00000000 ----0000		HSSPIn_WRCSDC0[B,H,W] 00000000 ----0000	
0x0F0	HSSPIn_WRCSDC3[B,H,W] 00000000 ----0000		HSSPIn_WRCSDC2[B,H,W] 00000000 ----0000	
0x0F4	HSSPIn_WRCSDC5[B,H,W] 00000000 ----0000		HSSPIn_WRCSDC4[B,H,W] 00000000 ----0000	
0x0F8	HSSPIn_WRCSDC7[B,H,W] 00000000 ----0000		HSSPIn_WRCSDC6[B,H,W] 00000000 ----0000	
0x0FC	HSSPIn_MID[B,H,W] 00000000 00000000 00000110 00110000			
0x100 - 0x3FC	-	-	-	-
0x400	-	-	-	QDCLKR[B,H,W] ----1111
0x404	-	-	-	DBCNT[B,H,W] ------00
0x408 - 0xFFC	-	-	-	-

1.48 HyperBus Interface

HyperBus Interface **Base_Address : 0xD0A0_5000**

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	CSR[B,H,W] -----000 -------0 ----0000 -------0			
0x004	IEN[B,H,W] 0------- -------- -------- -------0			
0x008	ISR[B,H,W] -------- -------- -------- -------0			
0x024	-	-	-	-
0x010	MBR0[B,H,W] 00000000 00000000 00000000 00000000			
0x014	MBR1[B,H,W] 00000000 00000000 00000000 00000000			
0x018	MCR0[B,H,W] -------- ------00 -------- --00--11			
0x01C	MCR1[B,H,W] -------- ------00 -------- --00--11			
0x020	MTR0[B,H,W] 00000000 00000000 00000000 ----0000			
0x024	MTR1[B,H,W] 00000000 00000000 00000000 ----0000			
0x028	GPOR[B,H,W] -------- -------- -------- ------00			
0x02C	WPR[B,H,W] -------- -------- -------- -------0			
0x030	TEST[B,H,W] -------- -------- -------- -------0			
0x034- 0xFFC	-	-	-	-

1.49 GDC Sub System Controller

GDC Sub System Controller **Base_Address : 0xD0A0_0000**

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	LockUnlock[W] 00000000 00000000 00000000 00000000			
0x004	LockStatus[W] -------- -------- -------0 ---0---0			
0x008	*[W]			
0x00C	CnfigClockControl[W] -------- -------- -------- -----001			
0x010	VramInterruptEnable[W] -------- -------- -------- ------11			
0x014	*[W]			
0x018	VramInterruptClear[W] -------- -------- -------- ------00			
0x01C	VramInterruptStatus[W] -------- -------- -------- ------00			
0x020	ExtFlashDevSelect[W] -------- -------- -------- -------1			
0x024	VramRemapDisable[W] -------- -------- -------- -------0			
0x028	PanicSwitch[W] -------- -------- -------- -------1			
0x02C	GDC_ClockDivider[W] -------- -----100 00000000 --------			
0x030	WkupTriggerMask[W] -----000 -----000 00000000 00000000			
0x034	ClockDomainStatus[W] -------- -------- -------- ----0000			
0x038	-			
0x03C	-			
0x040	dsp_LockUnlock[W] 00000000 00000000 00000000 00000000			
0x044	dsp_LockStatus[W] -------- -------- -------0 ---0---0			
0x048	dsp0_ClockDivider[W] -------- 01000001 11100000 --------			
0x04C	dsp0_DomainControl[W] -------- -------1 -------- -------0			
0x050	dsp0_ClockShift[W] -------- -------- -------- -------1			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x054	*[W]			
0x058	dsp0_PowerEnControl[W] -------- -------- -------- -------0			
0x05C	dsp0_ClockGateModeLock[W] 00000000 00000000 00000000 00000000			
0x060	dsp0_ClockGateControl[W] -------- -------- -------- -------0			
0x064	-			
0x068	-			
0x06C	-			
0x070	-			
0x074	-			
0x078	SDRAMC_ClcokDivider[W] -------- 00000100 00000000 --------			
0x07C	SDRAMC_DomainControl[W] -------- -------1 -------- -------0			
0x080	HSSPIC_ClockDivider[W] -------- 00000100 00000000 --------			
0x084	HSSPIC_DomainControl[W] -------- -------1 -------- -------0			
0x088	RPCC_ClcokDivider[W] -------- -------- -------- -----000			
0x08C	RPCC_DomainControl[W] -------- -------1 -------- -------0			
0x090	-			
0x094	-			
0x098	-			
0x09C	-			
0x100	vram_LockUnlock[W] 00000000 00000000 00000000 00000000			
0x104	vram_LockStatus[W] -------- -------- -------0 ---0---0			
0x108	vram_sram_select[W] -------- -------- ----0000 00000000			
0x10C	*[W]			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x110	*[W]			
0x114	*[W]			
0x118	*[W]			
0x11C	*[W]			
0x120	*[W]			
0x124	*[W]			
0x128	*[W]			
0x12C	-			
0x130	-			
0x134	-			
0x138	-			
0x13C	vram_sberraddr_s0[W] 00000000 00000000 0000000 00000000			
0x140	vram_sberraddr_s1[W] 00000000 00000000 0000000 00000000			
0x144	-			
0x148	vram_arbiter_priority[W] -------- -------- -------- 00000000			
0x14C-0xFFC	-			

1.50 GDC Sub System SDRAM Controller

GDC Sub System SDRAM Controller **Base_Address : 0xD0A0_3000**

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000-0x0FF	-			
0x100	SDMODE[W] -------- -------0 00010011 --00-000			
0x104	REFTIM[W] -------0 00000000 0000000000110011			
0x108	PWRDWN[W] -------- -------- 00000000 00000000			
0x10C	SDTIM[W] 0-----00 01000010 00010001 0100--01			
0x110	SDCMD[W] 0------- ---00000 00000000 00000000			
0x114-0xFFC	-			

B. List of Notes

This section explains notes for each function.

1. Notes when High-speed CR is Used for the Master Clock

1. Notes when High-speed CR is Used for the Master Clock

This section explains notes when the high-speed CR is used for the master clock.
The frequency of the high-speed CR varies depending on the temperature and/or the power supply voltage.
The following table shows notes on each function macro when the high-speed CR is used for the master clock.
Furthermore, pay attention to notes when the high-speed CR is used as an input clock of the PLL and the master clock is selected for PLL.

■ Notes on Each Macro

Macro	Function/Mode	Notes
Internal Bus Clock	HCLK/FCLK/PCLK0/ PCLK1/PCLK2/ TPIUCLK	When the frequency of the high-speed CR is the maximum value, the setting of the internal operating clock frequency shall not exceed the upper limit specified in the "data sheet" for the product that you are using.
Timer	Multi-function Timer Base Timer Watch Timer Dual Timer Watch Dog Timer Quadrature	The frequency variation of the high-speed CR should be considered for the timer count value of each macro.
A/D Converter	Sampling Time Compare Time	Considering the frequency variation of the high-speed CR, the sampling time and the compare time of the A/D converter shall satisfy the specification specified in the "data sheet" for the product that you are using.
USB	-	As the frequency accuracy does not meet the required specification, these macros cannot be used when the high-speed CR is used for the master clock.
Ethernet-MAC		
CAN		
CAN-FD		
I^2S		
Multi-Function Serial Interface	UART	Even if the frequency of the high-speed CR is the minimum or the maximum value, the baud rate error should be considered. The baud rate error shall not exceed the limit.
	CSIO	The frequency variation of the high-speed CR should be considered for the communication of each macro.
	I2C	
	LIN	As the required frequency accuracy cannot be met, this function cannot be used as master. As a slave, the specified baud rate has more error at the maximum/minimum frequency of high-speed clock. So, if the error limit of the baud rate is exceeded, this function cannot be used.
Debug Interface	Serial Wire	As the frequency variation of the high-speed CR, the SWV(Serial Wire View) may not be used.
External Bus Interface	Clock Output	When the external bus clock output is used, the frequency variation of the high-speed CR should be considered for devices to be connected.
High-Speed Quad SPI	-	The frequency variation of the high-speed CR should be considered for devices to be connected.
SD card Interface	-	The frequency variation of the high-speed CR should be considered for devices to be connected.

Macro	Function/Mode	Notes
GDC	Panel Output High-Speed Quad SPI HyperBus Interface SDRAM Interface	The frequency variation of the high-speed CR should be considered for devices to be connected.

C. Major Changes

Spansion Publication Number: MN709-00002

Page	Section	Changes
Revision 1.0		
-	-	Initial release
Revision 2.0		
7 to 8	The target product in this manual	Added TYPE1-M4, TYPE2-M4, TYPE3-M4 products.
61 to 62	CHAPTER 2: Dual Timer 4. Setting Procedure Example	Corrected erratum of Figure4-1. Corrected erratum of Tabel4-1 and calculation.
94	CHAPTER4-1: Real-time Clock 1. Configuration of Real-time Clock	Divided explanation into TYPE1-M4~TYPE2-M4 and TYPE3-M4.
97 to 149	CHAPTER4-2: RTC count block(A)	Corrected erratum based on Rev. 1.0 CHAPTER4-2 :RTC count block. Corresponded TYPE1-M4 to TYPE2-M4.
151 to 201	CHAPTER4-3: RTC count block (B)	Added new contents for TYPE3-M4
203 to 219	CHAPTER4-4: RTC Clock Control Block (A)	Corrected Erratum based on Rev. 1.0 CHAPTER4-2: RTC Clock Control Block. Corresponded TYPE1-M4 to TYPE2-M4.
221 to 235	CHAPTER4-5: RTC Clock Control Block (B)	Added new contents for TYPE3-M4
244	CHAPTER5-1: Base Timer I/O Select Function 3.2 I/O mode	Corrected Figure 3-2 and Table 3-7.
291 to 292, 309, 325, 343	CHAPTER5-2: Base Timer	Added Note about the lower byte of TMCR and CTEN bit
334	CHAPTER5-2: Base Timer 9.4.1 PWC timer function	Corrected Erratum of operation mode.
349 to 542	CHAPTER6: Multifunction Timer	Corrected the description of "2.4 Function Differences by Product Type ".
547 to 596	CHAPTER7-2: PPG	Corrected and added the explanation.
600 to 604	CHAPTER8-1: Quadrature Position/Revolution Counter 3. Operations	Added the explanation for 1-time frequency multiplication mode.
613	3. Operations	Deleted Interrupts of position counter.
614	3. Operations	Corrected the operation example of QPRC reset mask.
617	4.1 Quad Counter Position Rotation Count Display Function (QPCR)	Added the following description. "Also, write access is ignored while the counter is counting (QCR:PSTP="0")".
618	4.2 Quad Counter Position Rotation Count Display Function (QPCR)	Added the following description. "Also, write access is ignored while the counter is counting (QCR:RCM[1:0]≠ "00")"

Page	Section	Changes
627	4.6 QPRC Extension Control Register (QECR)	Added PEC bit. Corrected Erratum of ORNGMD 8K value.
628 to 629	4.7 Low-Order Bytes of QPRC Interrupt Control Register (QICRL)	Corrected the explanation for OFDF and UFDF.
636	4.9 QPRC Maximum Position Register (QMPR)	Corrected the explanation for QMPR.
-	-	Company name and layout design change
Revision 3.0		
5	Peripheral Manual	Added "GDC Part"
9	The target products in this manual	Added TYPE4-M4
94	CHAPTER4-1:Real-time Clock	Added TYPE4-M4
98	CHAPTER4-2:RTC CountBlock(A)	Revised the following description: Every moment → Every minute
152	CHAPTER4-3:RTC CountBlock(B)	Revised the following description: Every moment → Every minute
512	CHAPTER6:Multifunction Timer	Revised Figure 4-55 Diagram of FRT Connected between Multifunction Timer Units
610, 611	CHAPTER 8-1: Quadrature Position/Revolution Counter	Added TYPE4-M4
Revision 4.0		
9	The Target Products in This Manual Table4 TYPE4-M4 Product list	Revised TYPE4-M4 Product list
96	CHAPTER 4-1: Real-time Clock 1. Configuration of Real-time Clock	Added TYPE5-M4 and TYPE6-M4
124, 175	CHAPTER 4-3:RTC Count Block(A), (B)	Revised interface circuit type of WTCR10 register in Table7-1
205 to 252	CHAPTER 4-4: RTC Count Block (C)	Added new chapter of RTC Count Block (C) for TYPE5-M4
256, 274	CHAPTER 4-6: RTC Clock Control Block (A), (B)	Revised Figure 3-1 and 3-2
287 to 304	CHAPTER 4-7: RTC Clock Control Block (C)	Added new chapter of RTC Clock Control Block (C) for TYPE5-M4
440, 593 to 595	CHAPTER 6: Multifunction Timer 2.4 Function Differences by Product Type 4.8.3 Product Mounting Three MFT's (TYPE6-M4 product)	Added TYP5-M4 and TYPE6-M4 Added new chapter of Product Mounting Three MFT's (TYPE6-M4) for TYPE6-M4
682, 706	CHAPTER 8-1: Quadrature Position/Revolution Counter 3. Operations 4.6 QECR)	Added TYPE5-M4 and TYPE6-M4

Page	Section	Changes
862	Appendixes A. Register Map 1. Register Map	Corrected Base Address of GDC Sub System SDRAM Controller

NOTE: Please see “Revision History” about later revised information.

Revision History

Document Revision History

Document Title:	32-Bit Microcontroller FM4 Family Peripheral Manual Timer Part		
Document Number:	002-04858		
Revision	**ECN No.**	**Origin of Change**	**Description of Change**
**	-	YOHO	Migrated to Cypress and assigned document number 002-04858. No change to document contents or format.
*A	5278823	YOHO	Update to Cyress template. Corrected the erratum in the following chapter. CHAPTER 1: Watchdog Timer CHAPTER 4-2: RTC Count Block(A) CHAPTER 4-3: RTC Count Block(B) CHAPTER 4-4: RTC Count Block(C) CHAPTER 4-7: RTC Clock Control Block(C) CHAPTER 6: Multifunction Timer CHAPTER 7-2: PPG CHAPTER 8-1: Quadrature Position/Revolution Counter
*B	5735275	AESATMP8	Updated logo and Copyright.
*C	6190015	NOSU	Perface Added the note to refer to datasheets for supported peripheral functions. Added Microcontroller support information. The Target Products in This Manual Modified part numbers in Table 3 ~ 6 to 8 digits description. CHAPTER 6: Multifunction Timer 3.3.16 WFG Timer Value Register (WFTA/WFTB) Fixed incorrect descriptions about WFTA and WFTB 4.4.3 List of RTO0 to RTO5 Signal Output Details Fixed incorrect operation mode for WFSA:TMD[2:0]=101 in Table 4-22.