

Hexagon Application Kit

For XMC4000 Family

CPU_45B-V1

CPU Board XMC4500 SDRAM

Board User's Manual

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Microcontroller

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Introduction

This document describes the features and hardware details of the CPU board “CPU Board XMC4500 SDRAM” (CPU_45B-V1) designed to work with Infineon’s XMC4500 Microcontroller. This board is part of Infineon’s Hexagon Application Kits. Please visit www.infineon.com/xmc-dev for more information about the Hexagon Application Kit family.

1 Overview

The CPU board CPU_45B-V1 houses the XMC4500 Microcontroller and three satellite connectors (HMI, COM, ACT) for application expansion. The board along with satellite cards (e.g. HMI_OLED-V1, COM_ETH-V1, AUT_ISO-V1 boards) demonstrates the capabilities of XMC4500.

The main use case of this board is to demonstrate the external bus unit (EBU) of the XMC4500 device including the tool chain. For this purpose a 64 Mbit SDRAM is connected to the XMC4500 and for external bus extension an asynchronous 16-bit wide bus interface is available at the COM satellite connector.

Attention: This board (CPU_45B) has not been designed to work with the “General Purpose Motor Drive Card” (MOT_GPD LV). For this purpose please use the CPU boards CPU_45A, CPU_44A or CPU_42A.

The focus is safe operation under evaluation conditions. The board is neither cost nor size optimized and does not serve as a reference design.

1.1 Key Features

The CPU_45B-V1 board is equipped with the following features

- XMC4500 (ARM® Cortex™-M4-based) Microcontroller, 1 MByte Flash, 160 kByte SRAM, LFBGA-144
- 8 MByte On-board SDRAM, 1 Mbit x 16 bits x 4 banks
- Connection to satellite cards via satellite connectors COM, HMI and ACT
- USB OTG Host/Device support via micro USB connector
- Debug options
 - On-board Debugger via the Debug USB connector
 - Cortex Debug connector 10-pin (0.05")
 - Cortex Debug+ETM connector 20-pin (0.05")
- Reset push button
- 32 MBit quad SPI flash memory
- Boot option switch
- PowerScale Connector: Ready for power consumption analysis
- Two User Buttons connected to P5.10 and P0.10
- 7 LED's
 - 3 Power indicating LED's
 - 2 User LEDs (P5.2 and P1.1)
 - 1 RESET LED
 - 1 Debug LED
- Potentiometer, connected to analog input P14.1
- Power supply
 - Via Debug USB connector
 - Via Micro-USB connector in USB device mode
 - Via satellite connector pins (COM/ACT satellites cards can supply power to CPU board)
 - RTC backup battery

1.2 Block Diagram

Figure 1 shows the functional block diagram of the CPU_45B-V1 board. For more information about the power supply please refer to chapter 2.1.

The CPU board has got the following building blocks:

- 3 Satellite Connectors (COM, HMI ACT)
- 2 User LEDs connected to GPIOs P5.2 and P1.1
- 2 User Buttons connected to GPIOs P5.10 and P0.10.
- Quad SPI flash memory (32 Mbit)
- Synchronous Dynamic RAM (SDRAM, 64Mbit)
- 2 Cortex Debug Connectors
- Variable resistor (POTI) connected to GPIO P14.1
- USB On-The-Go Connector (Micro-USB)
- On-board Debugger via USB connector (Micro-USB)

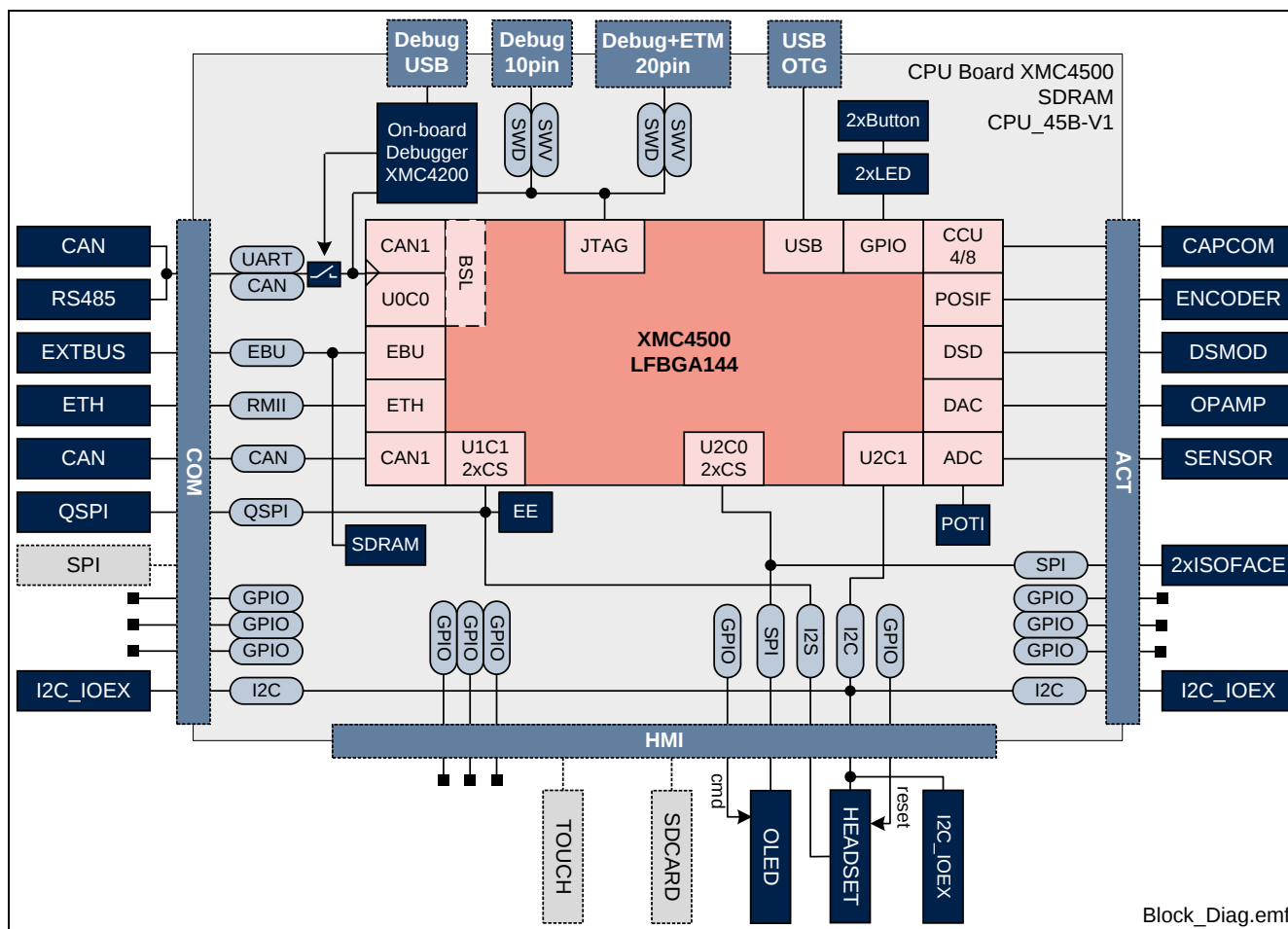


Figure 1 CPU_45B-V1 Board Block Diagram

2 Hardware Description

The following sections give a detailed description of the hardware and how it can be used.

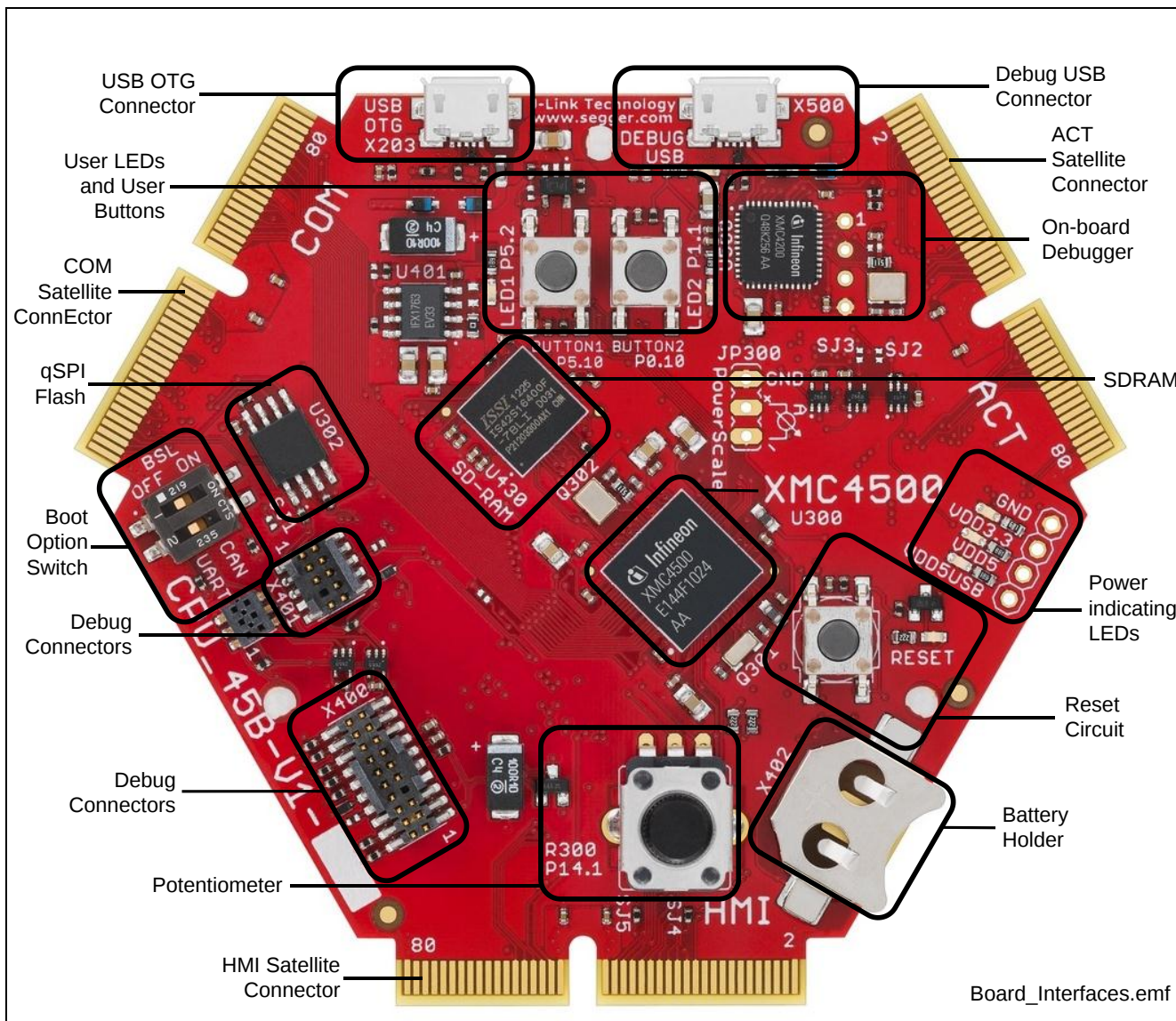


Figure 2 CPU Board XMC4500 SDRAM (CPU_45B-V1)

2.1 Power Supply

The CPU_45B-V1 board can be powered via either of the USB plugs (5 V); however, there is a current limit that can be drawn from the host PC through USB. If the CPU_45B-V1 board is used to drive other satellite cards (e.g. AUT_ISO-V1 or MOT_GPDV-V2) and the total current required exceeds 500 mA, then the board needs to be powered by a satellite card, which supports external power supply like e.g. AUT_ISO-V1, MOT_GPDV-V2, COM_ETH-V1.

The typical current drawn by the CPU board without any satellite cards connected is about 220 mA (@5V).

For powering the board through an USB interface, connect the USB cable provided with the kit to either of the Micro-USB connector on board as shown in Figure 3.

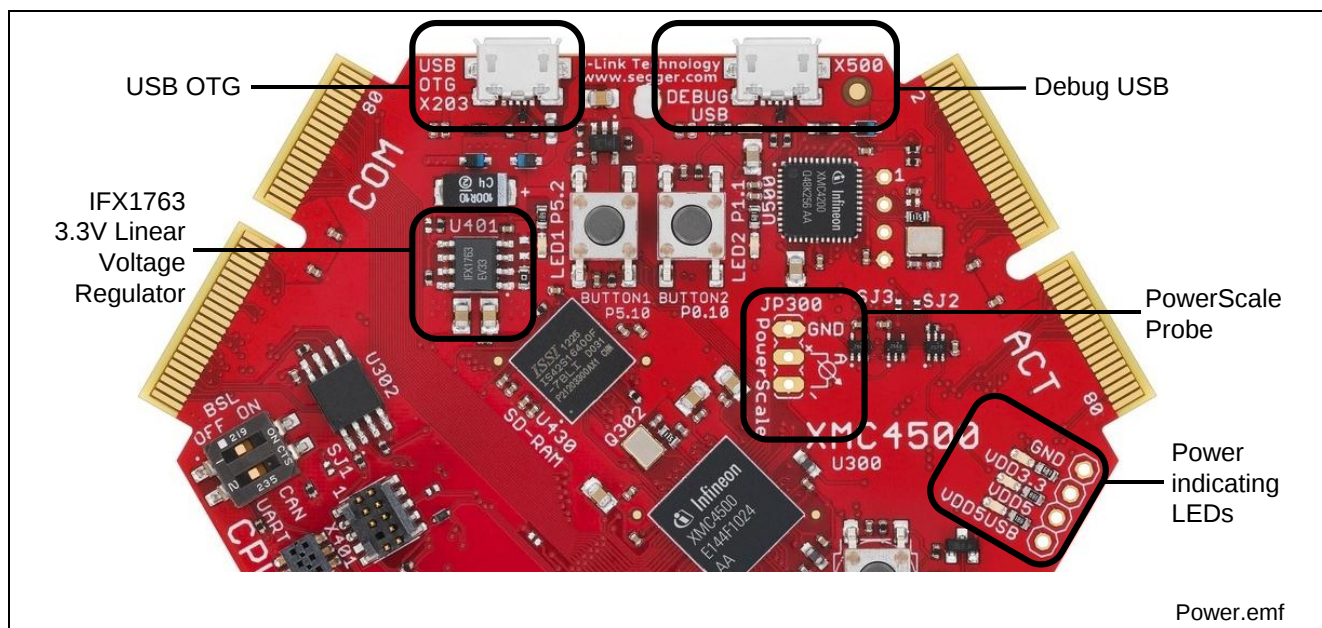


Figure 3 Powering option

To indicate the power status of CPU_45B-V1 board three power indicating LED's are provided on board (see Figure 3). The LED will be "ON" when the corresponding power rail is powered.

Table 1 Power status LEDs

LED Reference	Power Rail	Voltage	Note
V401	VDD5	5 V	Must always be “ON”
V402	VDD5USB	5 V	“ON” if powered by USB OTG connector X203 “OFF” in all other supply cases
V403	VDD3.3	3.3 V	Must always be “ON”

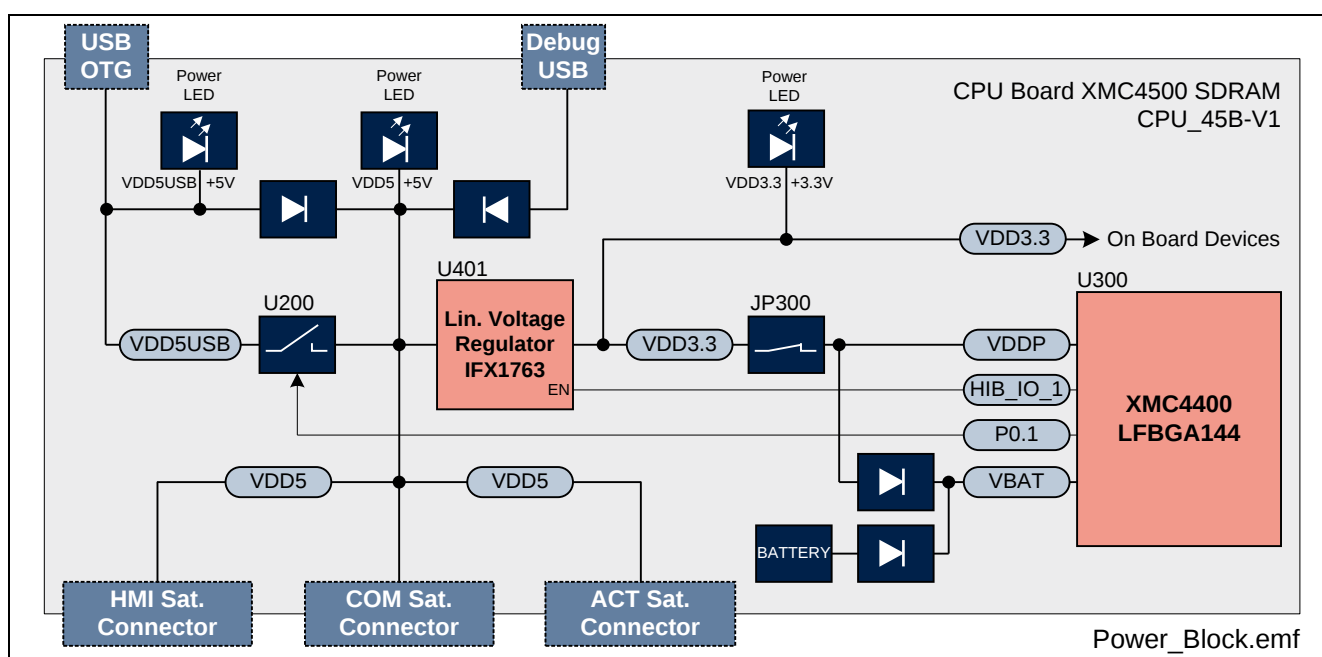


Figure 4 Block Diagram Of Power Supply

Hitex PowerScale probe is provided on the CPU_45B-V1 board to measure the power consumption of the XMC4500 device.

Table 2 **Power Measurement**

Jumper	Function	Description
JP300	PowerScale	A Hitex PowerScale probe can be connected for current sensing the VDD3.3 (CPU power source). Default: pos. 1-2 (closed) <i>Note: On the PCB there is a shorting trace between pin 1-2. This trace has to be cut first, before using PowerScale. Pin 3 is GND.</i>

2.2 Reset

A reset signal connected to the low-active PORST# pin of the target CPU (U300) can be issued by

- an on-board Reset Button (SW400, RESET)
- an on-board debug device (U500)
- an external debugger connected to either Cortex Debug connector X400 or X401

The RESET signal is routed to all satellite connectors. The reset circuit includes a red LED (V407) to indicate the reset status: The Reset LED (V407) will be "ON" during active reset state and will be "OFF" if reset is not active.

Be aware that PORST# is a bidirectional reset pin of the XMC4000 family which can also be pulled low by the XMC4000 device itself.

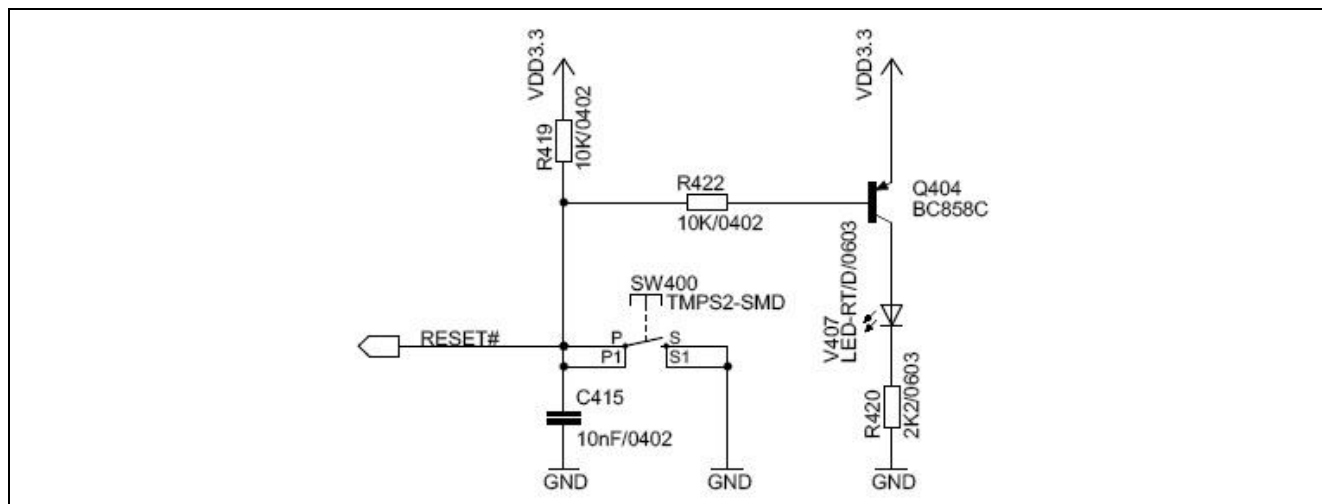


Figure 5 Reset Circuit



Figure 6 Reset LED and Reset Button

2.3 Clock Generation

An external 12 MHz crystal provides the clock signal to the XMC4500 microcontroller. The drive strength of the oscillator is set to maximum by software, in order to ensure a safe start-up of the oscillator even under worst case conditions. A serial 510 Ohm resistor will attenuate the oscillations during operations.

For the RTC clock a separate external 32.768 kHz crystal is used on board.

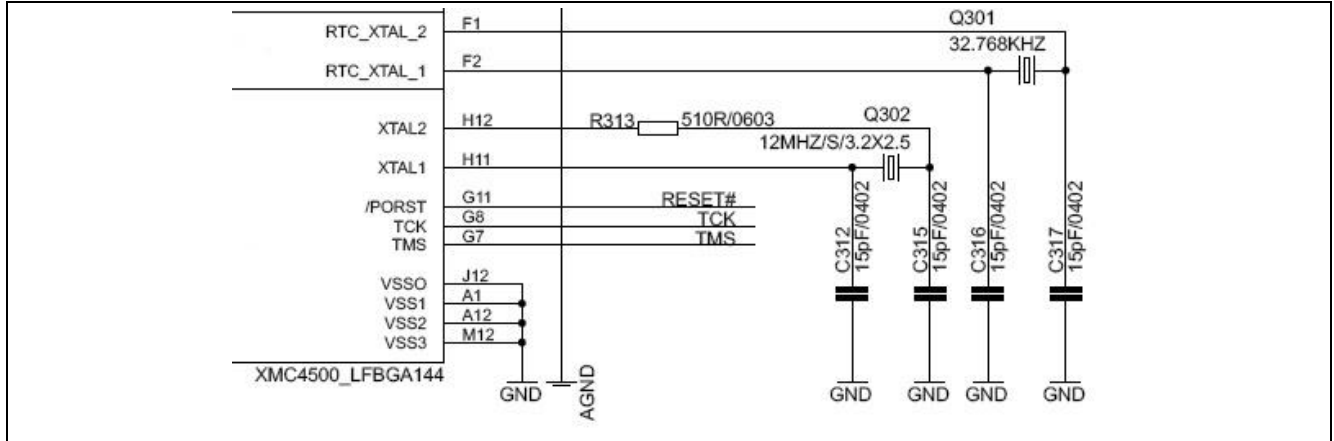


Figure 7 Clock Generation Circuit

2.4 Boot Option

During power-on-reset the XMC4500 latches the dip switch SW300 settings via the TCK and the TMS pin. Based on the values latched different boot options are possible.

Table 3 Boot Options Settings

BSL (TMS)	CAN/UART (TCK)	Boot Option
OFF (1)	UART (0)	Normal Mode (Boot from flash)
ON (0)	UART (0)	ASC BSL Enabled (Boot from UART)
OFF (1)	CAN (1)	BMI Customized Boot Enabled
ON (0)	CAN (1)	CAN BSL Enabled (Boot from CAN)

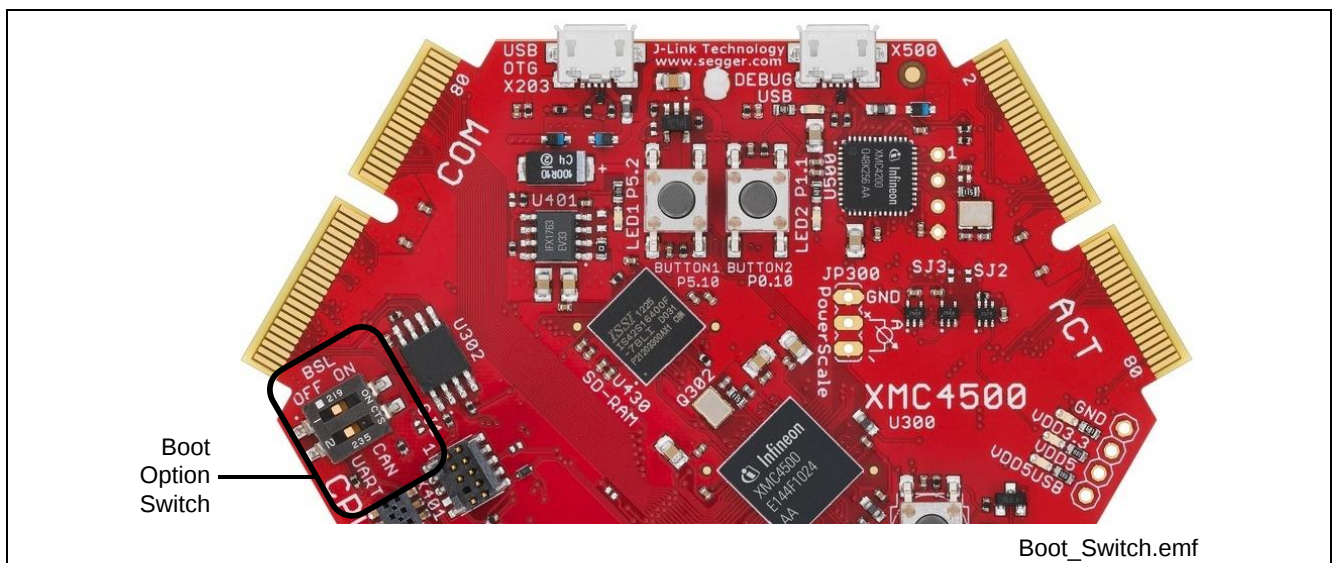


Figure 8 Boot Options Switch

2.5 Debug Interface

The CPU_45B-V1 board supports debugging via 3 different channels:

- On-board Debugger
- Cortex Debug Connector (10-pin)
- Cortex Debug+ETM Connector (20-pin)

The Hexagon Application Boards are designed to use “Serial Wire Debug” as debug interface. JTAG debug is not supported by default because the GPIO P0.7, where the required TDI function is mapped to also, is used by the on-board SDRAM device and various Actuator boards connected to the ACT satellite connector.

Attention: It is strongly recommended not to use JTAG debug mode, especially if satellites boards are connected, which uses the GPIO 0.7. For the same reason also do not use the on-board debugger in JTAG mode.

If you want to use the JTAG debug mode through the cortex debug connectors (X400, X401) anyway, enable the JTAG interface of the XMC device by assembling the pull-up resistor R427 (4k7 Ohm) and the resistor R410 (0 - 33 Ohm).

2.5.1 On-board USB Debugger

The on-board debugger [1] supports

- Serial Wire Debug
- Serial Wire Viewer [2]
- Full Duplex UART communication via a USB Virtual COM

- [1] Newer firmware versions of the on-board debugger require the latest J-Link driver (V4.62 or higher) and a Serial Port Driver (CDC driver) installed on your computer. Please check “Install J-Link Serial Port Driver” when installing the latest J-Link driver (see Figure 9)
- [2] Serial Wire Viewer operation does not work during use of the on-board SDRAM.

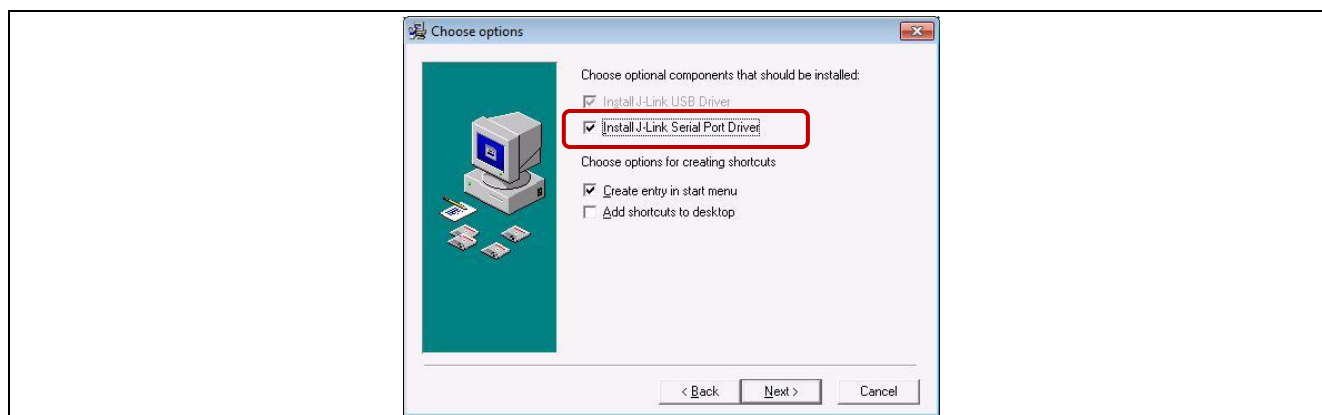


Figure 9 Installation of Serial Port Driver

The on-board debugger can be accessed through the Debug USB connector shown in Figure 10. The Debug LED V502 shows the status during debugging.

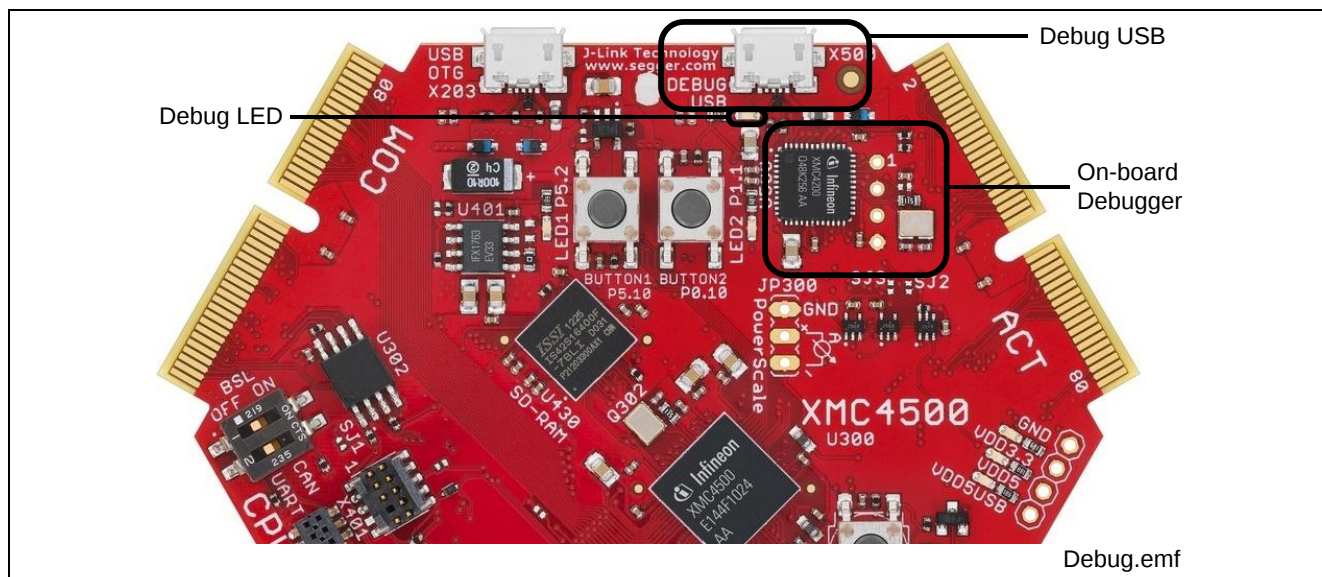


Figure 10 On-Board USB Debugger

When using an external debugger connected to the 10pin/20pin Cortex Debug Connector, the on-board debugger is switched off.

When using the USB virtual COM port function of the on-board debugger (connected to P1.4 and P1.5 of the XMC4500) the UART interface to the COM satellite is disabled through the switches U301 and U306.

2.5.2 Cortex Debug Connector (10-pin)

The CPU_45B-V1 board supports Serial Wire Debug operation through the 10-pin Cortex Debug Connector.

By default the board does not support Serial Wire Viewer operation through the 10-pin Cortex Debug Connector, because the required SWO pin mapped to P2.1 is used for the connection to the on-board SDRAM. If Serial Wire Viewer operation is required anyway the resistor R404 needs to be assembled.

JTAG operation additionally would require the TDI (P0.7) signal. By default the TDI signal is disconnected from the Cortex Debug Connectors by a not assembled resistor R410, because the pin P0.7 can be used by the on-board SDRAM, by Actuator boards connected to the ACT satellite connector and by boards connected to the COM satellite connector.

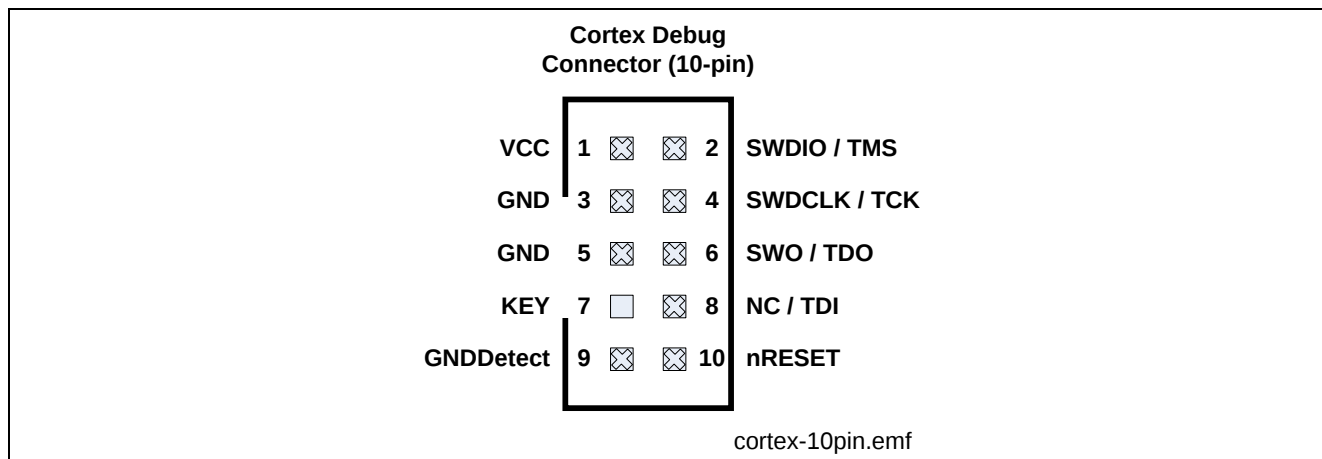


Figure 11 Cortex Debug Connector (10-pin)

Table 4 Cortex Debug Connector (10 Pin)

Pin No.	Signal Name	Serial Wire Debug	JTAG Debug
1	VCC	+3.3 V	+3.3 V
2	SWDIO / TMS	Serial Wire Data I/O	Test Mode Select
3	GND	Ground	Ground
4	SWDCLK / TCK	Serial Wire Clock	Test Clock
5	GND	Ground	Ground
6	SWO / TDO	Trace Data OUT	Test Data OUT
7	KEY	KEY	KEY
8	NC / TDI	Not connected	Test Data IN
9	GNDDetect	Ground Detect	Ground Detect
10	nRESET	Reset (Active Low)	Reset (Active Low)



Figure 12 Cortex Debug Connector (10-pin) Layout

2.5.3 Cortex Debug+ETM Connector (20-pin)

The CPU_45B-V1 board supports Serial Wire Debug operation and Instruction Trace operation through the 20-pin Cortex Debug+ETM Connector.

The board does not support Serial Wire Viewer operation through the Cortex Debug Connectors by default, because the required SWO pin mapped to P2.1 is used for the connection to the on-board SDRAM. If Serial Wire Viewer operation is required anyway the resistor R404 needs to be assembled.

JTAG operation additionally would require the TDI (P0.7) signal. By default the TDI signal is disconnected from the Cortex Debug Connectors by a not assembled resistor R410, because the pin P0.7 can be used by the on-board SDRAM, by Actuator boards connected to the ACT satellite connector and by boards connected to the COM satellite connector.

Cortex Debug+ETM Connector (20-pin)			
VCC	1		 2 SWDIO / TMS
GND	3		 4 SWDCLK / TCK
GND	5		 6 SWO / TDO / EXTa / TRACECTL (NC)
KEY	7		 8 NC/EXTb/TDI (NC)
GNDDetect	9		 10 nRESET
GND/TgtPwr+Cap	11		 12 TRACECLK
GND/TgtPwr+Cap	13		 14 TRACEDATA[0]
GND	15		 16 TRACEDATA[1]
GND	17		 18 TRACEDATA[2]
GND	19		 20 TRACEDATA[3]

cortex-20pin.emf

Figure 13 Cortex Debug+ETM Connector (20-pin)

Table 5 Cortex Debug+ETM Connector (20 Pin)

Pin No.	Signal Name	Serial Wire Debug	JTAG Debug
1	VCC	+3.3 V	+3.3 V
2	SWDIO / TMS	Serial Wire Data I/O	Test Mode Select
3	GND	Ground	Ground
4	SWDCLK / TCK	Serial Wire Clock	Test Clock
5	GND	Ground	Ground
6	SWO / TDO	Trace Data OUT	Test Data OUT
7	KEY	KEY	KEY
8	NC / TDI	Not connected	Test Data IN
9	GNDDetect	Ground Detect	Ground Detect
10	nRESET	Reset (Active Low)	Reset (Active Low)
11	GND/TgtPwr+Cap	Ground	Ground
12	TRACECLK	Trace Clock	Trace Clock
13	GND/TgtPwr+Cap	Ground	Ground
14	TRACEDATA[0]	Trace Data 0	Trace Data 0
15	GND	Ground	Ground
16	TRACEDATA[1]	Trace Data 1	Trace Data 1
17	GND	Ground	Ground
18	TRACEDATA[2]	Trace Data 2	Trace Data 2
19	GND	Ground	Ground
20	TRACEDATA[3]	Trace Data 3	Trace Data 3



Figure 14 Cortex Debug+ETM Connector (20-pin) Layout

2.7 SDRAM

The CPU_45B-V1 board has a 64 Mbit SDRAM interfaced to the XMC4500. The SDRAM interface is shown in Figure 16.

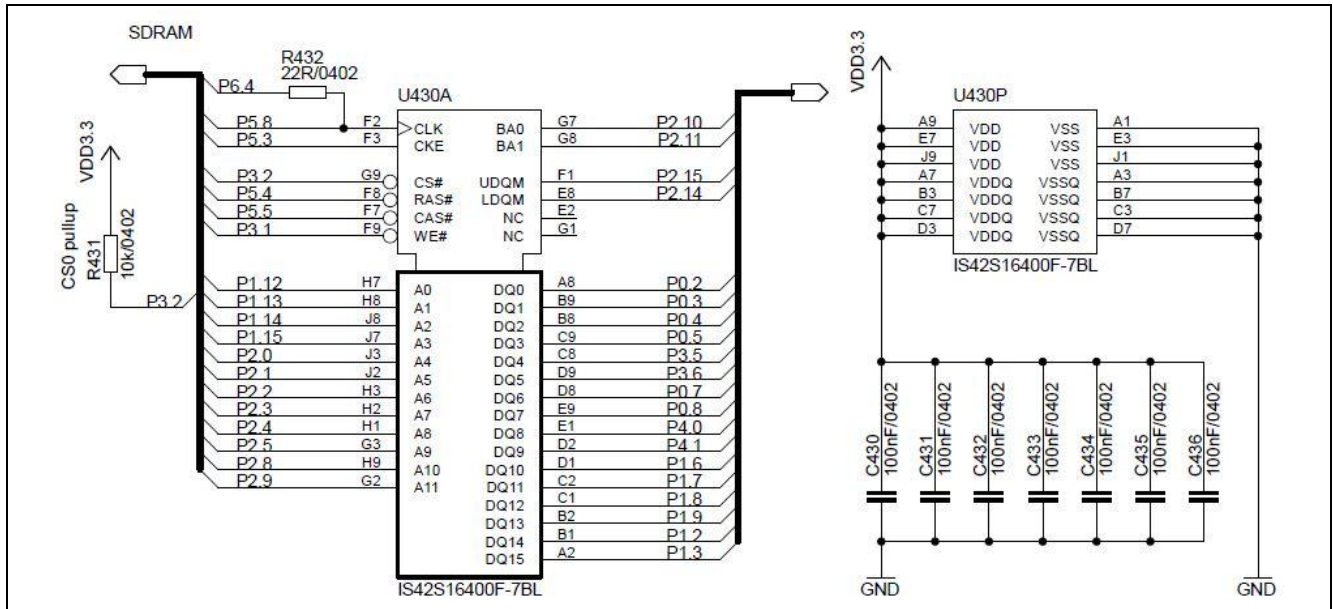


Figure 16 SDRAM Interface

2.8 USB

The XMC4500 supports USB interface in host only mode, device only mode or as an OTG Dual Role Device (DRD). In USB device mode, power is expected through VBUS (pin 1 of X203) from an external host (e.g. PC). When the current consumption of the application running on the Hexagon Application system is higher than 500 mA, power from an external source through satellite cards shall be used.

Note: Some PCs, notebooks or hubs have a weak USB supply which is not sufficient for proper supply. In this case use an external 5 Volt power supply or a powered USB hub.

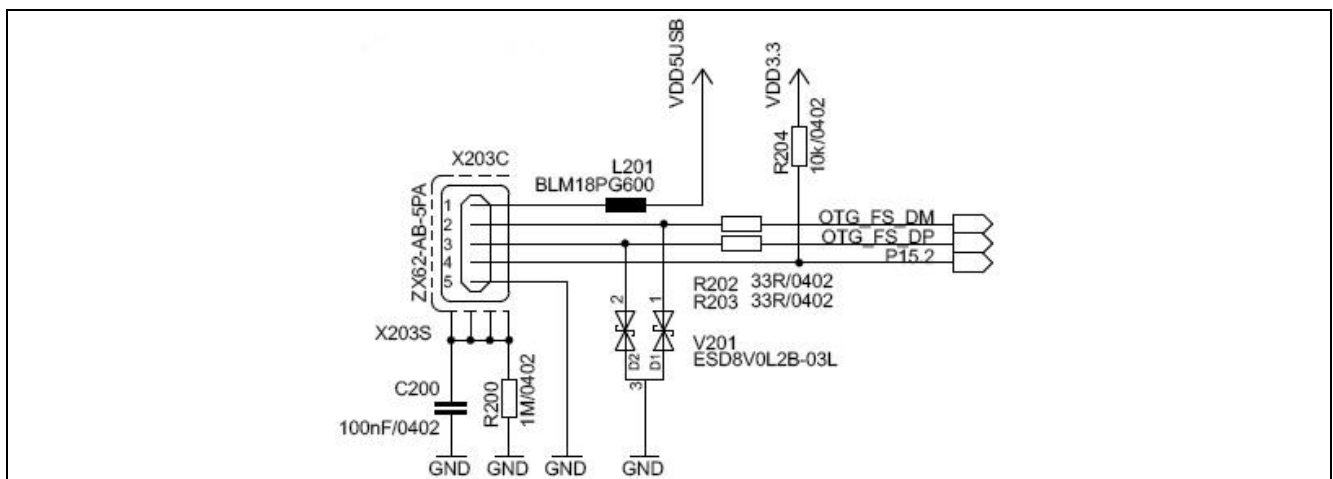


Table 7 USB micro AB connector Pinout

Pin No.	Pin Name	Pin Description
1	VBUS	5 V
2	D-	Data Minus
3	D+	Data Plus
4	ID	Identification
5	GND	Ground

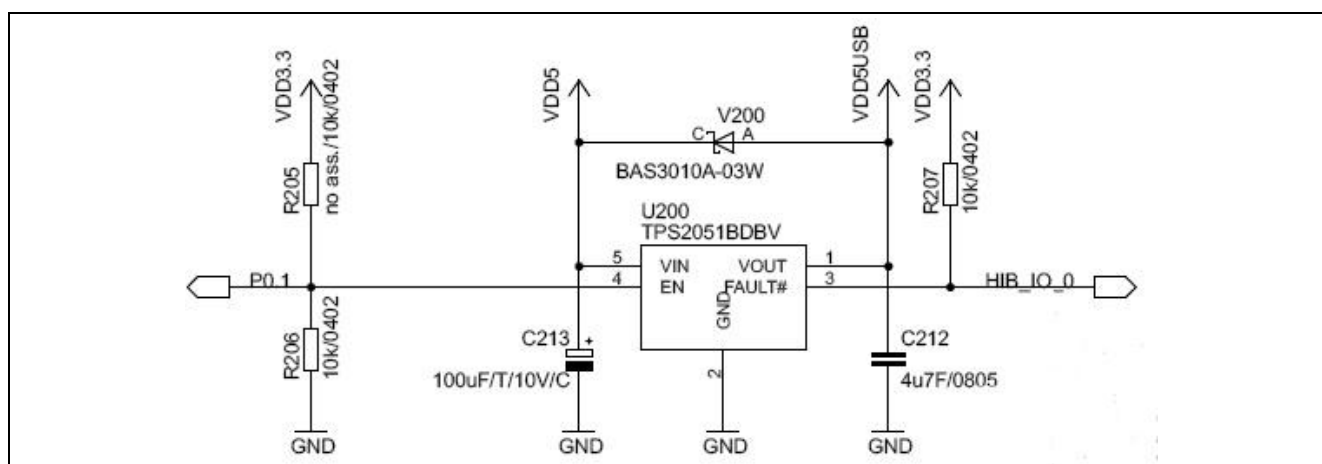


Figure 18 USB power generation - Host/OTG mode

In the host only mode and OTG mode the CPU_45B-V1 board is capable of supplying power to the connected device (e.g. USB mouse). The board has a power-switch which is controlled by the USB.BUSDRIVE signal of XMC4500. USB.BUSDRIVE is mapped to Port P0.1 (active high).

In the Host/OTG mode a low active FAULT signal indicates to XMC4500 via HIB_IO_0 signal, if more than 500 mA current is drawn by the external device. HIB_IO_0 signal is used as general purpose input pin for this implementation.

Diode V200 will allow powering the board through USB in all USB modes via e.g. a PC.

2.9 RTC

The XMC4500 CPU has two power domains, the Core Domain and Hibernate Domain.

The Core Domain (VDDP pins) is connected to the VDD3.3 rail. An on-board LDO voltage regulator generates VDD3.3 (3.3 V) from VDD5 (5 V).

The Hibernate Domain is powered via the auxiliary supply pin VBAT, which is supplied by either a 3 V coin cell (size 1216, 1220, 1225) plugged into the battery holder or 3.3 V (VDD3.3) generated by the on-board voltage regulator.



Figure 19 Battery Holder for Coin Cells

The Real Time Clock (RTC) is located in the hibernate domain. The XMC4500 uses the HIB_IO_1 signal (active low) to shutdown the external LDO voltage regulator which generates VDD3.3 (core domain). Even if the Core Domain is not powered the Hibernate Domain will operate if VBAT is available. The RTC keeps running as long as the Hibernate Domain is powered via the auxiliary supply VBAT. The RTC is capable to wake-up the whole system from Hibernate mode by setting HIB_IO_1 to high.

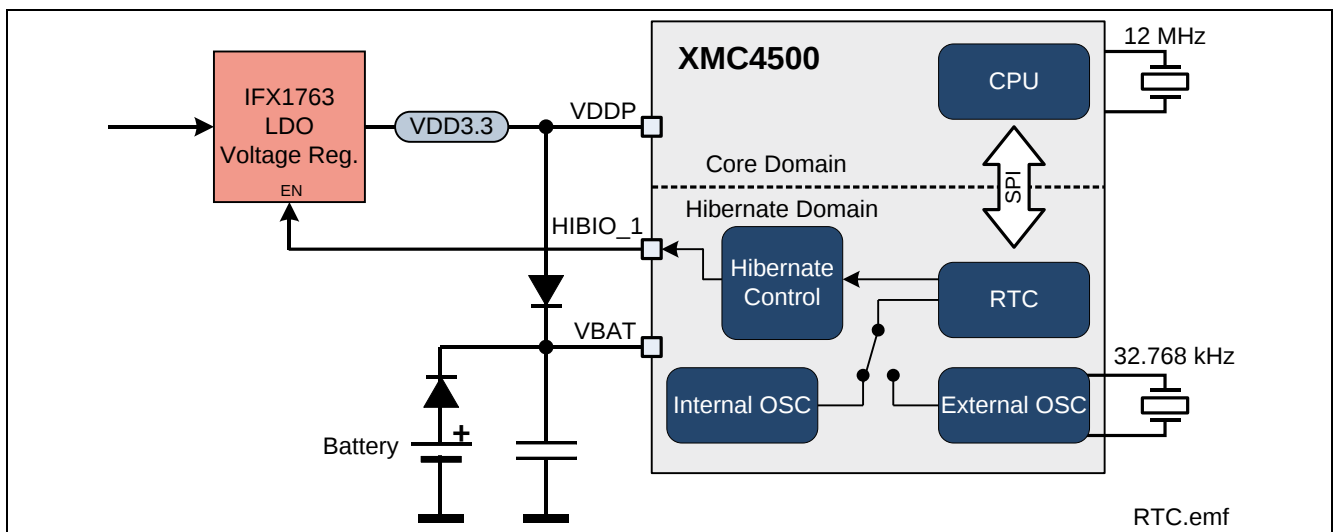


Figure 20 XMC4500 Power Domains and Real Time Clock

2.10 User LEDs and User Button

The port pins P5.2 and P1.1 of XMC4500 on the CPU_45B-V1 board are connected to the LEDs V300 and V301 respectively. More User LED's are available through the I2C GPIO expander on most of the satellite cards.

Table 8 User LEDs

LED	Connected to Port Pin
LED1 / V300	GPIO P5.2
LED2 / V301	GPIO P1.1

Two User Buttons, SW401 and SW402 are connected to P5.10 and P0.10 of XMC4500

Table 9 User Buttons

Button	Connected to Port Pin
Button1 / SW401	GPIO P5.10
Button2 / SW402	GPIO P0.10

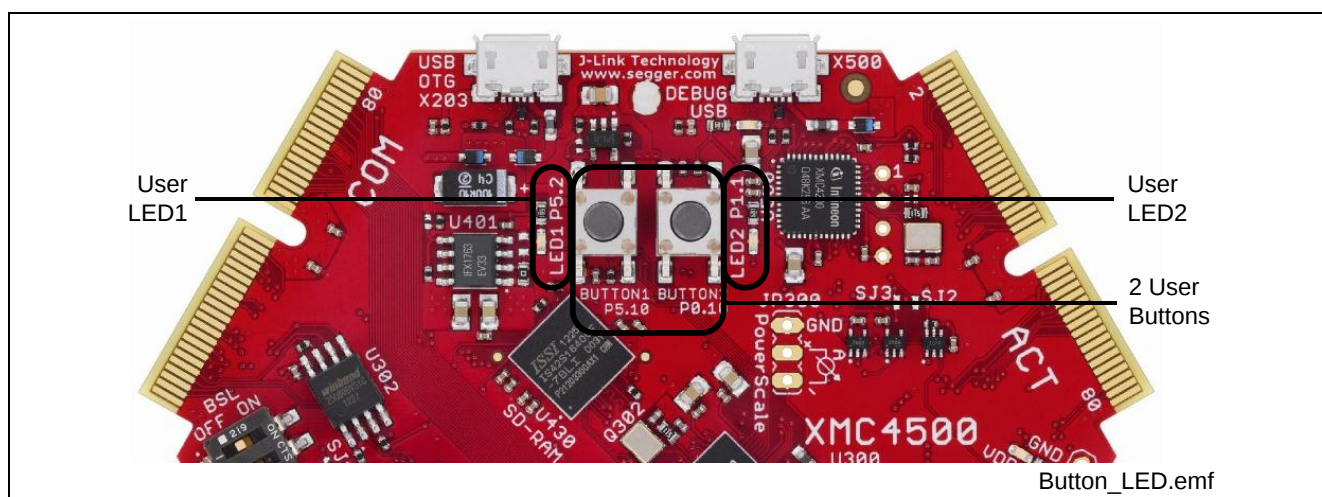


Figure 21 User LEDs and User Buttons

2.11 Potentiometer

The CPU_45B-V1 board provides a potentiometer for ease of use and testing of the on-chip analog to digital converter. The potentiometer is connected to the analog input G0_CH1 (P14.1). The analog output of the potentiometer ranges from 0 V to 3.3 V.

Table 10 Potentiometer

Potentiometer	Connected to Port Pin
R300	P14.1/ G0_CH1 (Group 0, channel 1)

2.12 Satellite Connectors

The CPU_45B-V1 board provides three satellite connectors for application expansion by satellite cards:

- COM satellite connector (Communication)
- HMI satellite connector (Human Machine Interface)
- ACT satellite connector (Actuator)

Note: Satellite cards shall be connected to their matching connectors only. (For e.g. COM satellite cards shall be connected to COM satellite connector only)

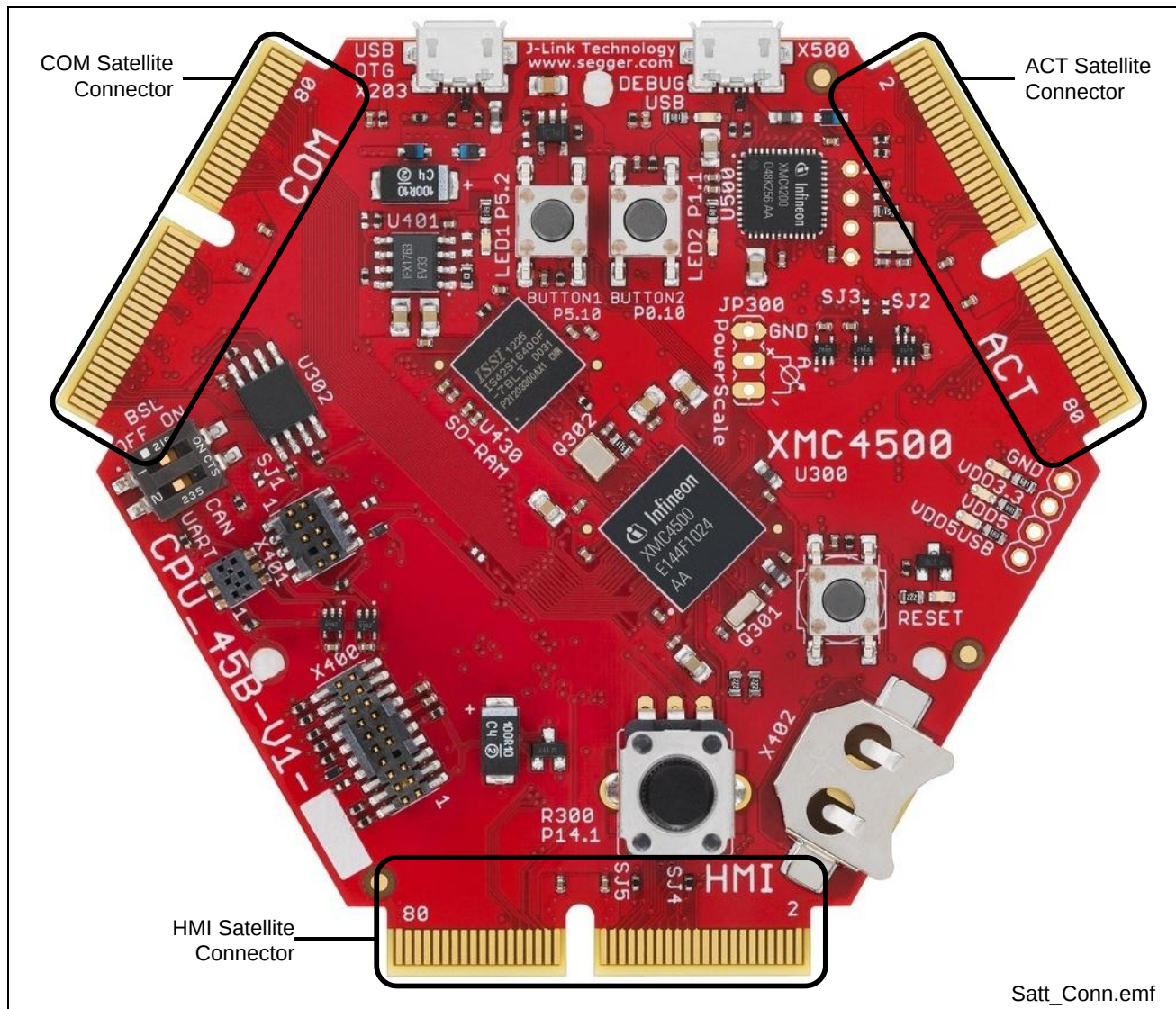


Figure 22 Satellite Connectors

2.12.1 COM Connector

The COM satellite connector on the CPU_45B-V1 board allows interface expansion through COM satellite cards (e.g. COM_ETH-V1)

CPU_45B-V1 (SDRAM)		Satellite Connector		CPU_45B-V1 (SDRAM)	
XMC Pin	XMC Function	Pin	Function	XMC Pin	XMC Function
VSS	GND	COM 1	GND	VSS	GND
P0.13	U1C1_SCLKOUT	2	qSPI_D0	P0.13	U1C1_SCLKOUT
P0.12	U1C1_SELO0	3	qSPI_D1	P0.12	U1C1_SELO0
P3.3 *	U1C1_SELO1	4	qSPI_D2	P3.3 *	U1C1_SELO1
nc	nc	5	qSPI_D3	nc	nc
nc	nc	6	RSVD	nc	nc
P5.1	ETH0_RXD1D	7	RSVD	P5.1	ETH0_RXD1D
P5.0	ETH0_RXD0D	8	ETH_RMII	P5.0	ETH0_RXD0D
P1.11	ETH0_MDC	9	ETH_RMII	P1.11	ETH0_MDC
P1.10	ETH0_MDIC	10	ETH_RMII	P1.10	ETH0_MDIC
P5.9	ETH0_TX_EN	11	ETH_RMII	P5.9	ETH0_TX_EN
nc	nc	12	ETH_RMII	nc	nc
nc	nc	13	ETH_RMII	nc	nc
P1.4 **	U0C0_D0X0B	14	ETH_RMII	P1.4 **	U0C0_D0X0B
P1.5 **	U0C0_D0X0A	15	ETH_RMII	P1.5 **	U0C0_D0X0A
nc	nc	16	ETH_RMII	nc	nc
nc	nc	17	ETH_RMII	nc	nc
nc	nc	18	ETH_RMII	nc	nc
nc	nc	19	ETH_RMII	nc	nc
P3.11/P3.12	U2C1_D0X0D/DX0D	20	ETH_RMII	P3.11/P3.12	U2C1_D0X0D/DX0D
P14.13	P14.13	21	ETH_RMII	P14.13	P14.13
P0.0	P0.0	22	ETH_RMII	P0.0	P0.0
		23	RSVD		
		24	RSVD		
		25	ASC_DIR		
		26	ASC_RXD		
		27	ASC_TXD		
		28	CAN_RXD		
		29	CAN_TXD		
		30	SPI_MSTR		
		31	SPI_MSTR		
		32	SPI_MSTR		
		33	SPI_MSTR		
		34	SPI_MSTR		
		35	SPI_MSTR		
		36	SPI_MSTR		
		37	SPI_MSTR		
		38	SPI_MSTR		
		39	SPI_MSTR		
		40	SPI_MSTR		
		41	SPI_MSTR		
		42	SPI_MSTR		
		43	SPI_MSTR		
		44	SPI_MSTR		
		45	SPI_MSTR		
		46	SPI_MSTR		
		47	SPI_MSTR		
		48	SPI_MSTR		
		49	SPI_MSTR		
		50	SPI_MSTR		
		51	SPI_MSTR		
		52	SPI_MSTR		
		53	SPI_MSTR		
		54	SPI_MSTR		
		55	SPI_MSTR		
		56	SPI_MSTR		
		57	SPI_MSTR		
		58	SPI_MSTR		
		59	SPI_MSTR		
		60	SPI_MSTR		
		61	SPI_MSTR		
		62	SPI_MSTR		
		63	SPI_MSTR		
		64	SPI_MSTR		
		65	SPI_MSTR		
		66	SPI_MSTR		
		67	SPI_MSTR		
		68	SPI_MSTR		
		69	SPI_MSTR		
		70	SPI_MSTR		
		71	SPI_MSTR		
		72	SPI_MSTR		
		73	SPI_MSTR		
		74	SPI_MSTR		
		75	SPI_MSTR		
		76	SPI_MSTR		
		77	SPI_MSTR		
		78	SPI_MSTR		
		79	SPI_MSTR		
		80	SPI_MSTR		
		COM			

Figure 23 Satellite Connector Type COM

Attention: * This pin is used as chip select signal for the on-board EEPROM and therefore disconnected by solder jumper SJ1

Attention: ** This pin is connected with the satellite connector via an analog switch

2.12.2 HMI Connector

The HMI satellite connector on the CPU_45B-V1 board allows interface expansion through HMI satellite cards.

CPU_45B-V1 (SDRAM)	CPU_45B-V1 (SDRAM)		Satellite Connector	Satellite Connector		CPU_45B-V1 (SDRAM)	CPU_45B-V1 (SDRAM)	
	XMC Pin	XMC Function		Function	Pin		XMC Function	XMC Pin
	VSS	GND	HMI	GND	1	HMI	GND	VSS
	nc	nc		MMC_CLK	2		MMC_CLK	GND
	nc	nc		MMC_DATA1	3		MMC_DATA1	MMC_nRST
	nc	nc		MMC_DATA3	4		MMC_DATA3	MMC_DATA0
	nc	nc		MMC_DATA5	5		MMC_DATA5	MMC_DATA2
	nc	nc		MMC_DATA7	6		MMC_DATA7	MMC_DATA4
	nc	nc		MMC_BUSPOW	7		MMC_BUSPOW	MMC_DATA6
	nc	nc		MMC_nSDCD	8		MMC_nSDCD	MMC_CMD
	nc	nc		RSVD	9		RSVD	MMC_LED
	nc	nc		RSVD	10		RSVD	MMC_SDWC
	nc	nc		RSVD	11		RSVD	RSVD
	nc	nc		RSVD	12		RSVD	RSVD
	P4.2	P4.2		AudioRST	13		AudioRST	nc
	P3.4	U1C1_SELO2		I2S_WA	14		I2S_WA	P5.11
	nc	nc		I2S_MCLK	15		I2S_MCLK	I2S_MTSR
	nc	nc		I2S_SYNCCLK	16		I2S_SYNCCLK	I2S_MRST
	P3.10	U2C0_SELO0		SPI_CSH0	17		SPI_CSH0	I2S_SCLK
	P5.6	U2C0_SELO3		SPI_CSH1	18		SPI_CSH1	U2C0_DOUT0
	nc	nc		SPI_CSH2	19		SPI_CSH2	U2C0_DX0C
	P3.11/P3.12	U2C1_DOUT0/DX0D	HMI	I2C_SDA	20	HMI	I2C_SDA	SPI_MRST
	P15.5	P15.5 Input		HMI_GPIO1	21		HMI_GPIO1	SPI_SCLK
	P5.7	P5.7		HMI_GPIO0	22		HMI_GPIO0	I2C_SCL
				VDD5	23		VDD5	I2C_SCLKOUT
					24			P6.3
					25			RESET#
					26			POSRST
					27			
					28			
					29			
	VAGND	AGND	HMI	AGND	30	HMI	AGND	VAREF
	P14.9	DAC_OUT1		DAC0/ADC1	31		DAC0/ADC1	VAREF
	nc	nc		ADC3/ORC0	32		ADC3/ORC0	VADC_G1CH0
	P14.12	VADC_G1CH4		ADC15	33		ADC15	VADC_G0CH4
	P15.13	VADC_G3CH5		ADC17	34		ADC17	VADC_G0CH3
	P15.12	VADC_G3CH4		ADC19	35		ADC19	VADC_G2CH3
	nc	nc		RSVD	36		RSVD	nc
	nc	nc		RSVD	37		RSVD	nc
	nc	nc		RSVD	38		RSVD	nc
	nc	nc		TPx1	39		TPx1	nc
	nc	nc	HMI	TPx0	40	HMI	TPx0	nc
	nc	nc		COL3	41		COL3	nc
	nc	nc		COL2	42		COL2	nc
	nc	nc		COL1	43		COL1	nc
	nc	nc		COL0	44		COL0	nc
	nc	nc		COLA	45		COLA	nc
	VSS	GND		GND	46		GND	nc
					47			VSS
					48			
					49			

Figure 24 Satellite Connector Type HMI

2.12.3 ACT Satellite Connector

The ACT satellite connector on the CPU_45B-V1 board allows interface expansion through ACT satellite cards.

CPU_45B-V1 (SDRAM)		XMC Pin		XMC Function		CPU_45B-V1 (SDRAM)		XMC Pin		XMC Function	
VSS		GND		P14.7		VSS		GND		P14.7	
P14.9		P14.10		P14.11		P14.9		P14.10		P14.11	
P14.12		P14.13		P14.14		P14.12		P14.13		P14.14	
P14.15		P14.16		P14.17		P14.15		P14.16		P14.17	
P14.18		P14.19		P14.20		P14.18		P14.19		P14.20	
P14.21		P14.22		P14.23		P14.21		P14.22		P14.23	
P14.24		P14.25		P14.26		P14.24		P14.25		P14.26	
P14.27		P14.28		P14.29		P14.27		P14.28		P14.29	
P14.30		P14.31		P14.32		P14.30		P14.31		P14.32	
P14.33		P14.34		P14.35		P14.33		P14.34		P14.35	
P14.36		P14.37		P14.38		P14.36		P14.37		P14.38	
P14.39		P14.40		P14.41		P14.39		P14.40		P14.41	
P14.42		P14.43		P14.44		P14.42		P14.43		P14.44	
P14.45		P14.46		P14.47		P14.45		P14.46		P14.47	
P14.48		P14.49		P14.50		P14.48		P14.49		P14.50	
P14.51		P14.52		P14.53		P14.51		P14.52		P14.53	
P14.54		P14.55		P14.56		P14.54		P14.55		P14.56	
P14.57		P14.58		P14.59		P14.57		P14.58		P14.59	
P14.60		P14.61		P14.62		P14.60		P14.61		P14.62	
P14.63		P14.64		P14.65		P14.63		P14.64		P14.65	
P14.66		P14.67		P14.68		P14.66		P14.67		P14.68	
P14.69		P14.70		P14.71		P14.69		P14.70		P14.71	
P14.72		P14.73		P14.74		P14.72		P14.73		P14.74	
P14.75		P14.76		P14.77		P14.75		P14.76		P14.77	
P14.78		P14.79		P14.80		P14.78		P14.79		P14.80	
P14.81		P14.82		P14.83		P14.81		P14.82		P14.83	
P14.84		P14.85		P14.86		P14.84		P14.85		P14.86	
P14.87		P14.88		P14.89		P14.87		P14.88		P14.89	
P14.90		P14.91		P14.92		P14.90		P14.91		P14.92	
P14.93		P14.94		P14.95		P14.93		P14.94		P14.95	
P14.96		P14.97		P14.98		P14.96		P14.97		P14.98	
P14.99		P14.100		P14.101		P14.99		P14.100		P14.101	
P14.102		P14.103		P14.104		P14.102		P14.103		P14.104	
P14.105		P14.106		P14.107		P14.105		P14.106		P14.107	
P14.108		P14.109		P14.110		P14.108		P14.109		P14.110	
P14.111		P14.112		P14.113		P14.111		P14.112		P14.113	
P14.114		P14.115		P14.116		P14.114		P14.115		P14.116	
P14.117		P14.118		P14.119		P14.117		P14.118		P14.119	
P14.120		P14.121		P14.122		P14.120		P14.121		P14.122	
P14.123		P14.124		P14.125		P14.123		P14.124		P14.125	
P14.126		P14.127		P14.128		P14.126		P14.127		P14.128	
P14.129		P14.130		P14.131		P14.129		P14.130		P14.131	
P14.132		P14.133		P14.134		P14.132		P14.133		P14.134	
P14.135		P14.136		P14.137		P14.135		P14.136		P14.137	
P14.138		P14.139		P14.140		P14.138		P14.139		P14.140	
P14.141		P14.142		P14.143		P14.141		P14.142		P14.143	
P14.144		P14.145		P14.146		P14.144		P14.145		P14.146	
P14.147		P14.148		P14.149		P14.147		P14.148		P14.149	
P14.150		P14.151		P14.152		P14.150		P14.151		P14.152	
P14.153		P14.154		P14.155		P14.153		P14.154		P14.155	
P14.156		P14.157		P14.158		P14.156		P14.157		P14.158	
P14.159		P14.160		P14.161		P14.159		P14.160		P14.161	
P14.162		P14.163		P14.164		P14.162		P14.163		P14.164	
P14.165		P14.166		P14.167		P14.165		P14.166		P14.167	
P14.168		P14.169		P14.170		P14.168		P14.169		P14.170	
P14.171		P14.172		P14.173		P14.171		P14.172		P14.173	
P14.174		P14.175		P14.176		P14.174		P14.175		P14.176	
P14.177		P14.178		P14.179		P14.177		P14.178		P14.179	
P14.180		P14.181		P14.182		P14.180		P14.181		P14.182	
P14.183		P14.184		P14.185		P14.183		P14.184		P14.185	
P14.186		P14.187		P14.188		P14.186		P14.187		P14.188	
P14.189		P14.190		P14.191		P14.189		P14.190		P14.191	
P14.192		P14.193		P14.194		P14.192		P14.193		P14.194	
P14.195		P14.196		P14.197		P14.195		P14.196		P14.197	
P14.198		P14.199		P14.200		P14.198		P14.199		P14.200	
P14.201		P14.202		P14.203		P14.201		P14.202		P14.203	
P14.204		P14.205		P14.206		P14.204		P14.205		P14.206	
P14.207		P14.208		P14.209		P14.207		P14.208		P14.209	
P14.210		P14.211		P14.212		P14.210		P14.211		P14.212	
P14.213		P14.214		P14.215		P14.213		P14.214		P14.215	
P14.216		P14.217		P14.218		P14.216		P14.217		P14.218	
P14.219		P14.220		P14.221		P14.219		P14.220		P14.221	
P14.222		P14.223		P14.224		P14.222		P14.223		P14.224	
P14.225		P14.226		P14.227		P14.225		P14.226		P14.227	
P14.228		P14.229		P14.230		P14.228		P14.229		P14.230	
P14.231		P14.232		P14.233		P14.231		P14.232		P14.233	
P14.234		P14.235		P14.236		P14.234		P14.235		P14.236	
P14.237		P14.238		P14.239		P14.237		P14.238		P14.239	
P14.240		P14.241		P14.242		P14.240		P14.241		P14.242	
P14.243		P14.244		P14.245		P14.243		P14.244		P14.245	
P14.246		P14.247		P14.248		P14.246		P14.247		P14.248	
P14.249		P14.250		P14.251		P14.249		P14.250		P14.251	
P14.252		P14.253		P14.254		P14.252		P14.253		P14.254	
P14.255		P14.256		P14.257		P14.255		P14.256		P14.257	
P14.258		P14.259		P14.260		P14.258		P14.259		P14.260	
P14.261		P14.262		P14.263		P14.261		P14.262		P14.263	
P14.264		P14.265		P14.266		P14.264		P14.265		P14.266	
P14.267		P14.268		P14.269		P14.267		P14.268		P14.269	
P14.270		P14.271		P14.272		P14.270		P14.271		P14.272	
P14.273		P14.274		P14.275		P14.273		P14.274		P14.275	
P14.276		P14.277		P14.278		P14.276		P14.277		P14.278	
P14.279		P14.280		P14.281		P14.279		P14.280		P14.281	
P14.282		P14.283		P14.284		P14.282		P14.283		P14.284	
P14.285		P14.286		P14.287		P14.285		P14.286		P14.287	
P14.288		P14.289		P14.290		P14.288		P14.289		P14.290	
P14.289		P14.291		P14.292		P14.289		P14.291		P14.292	
P14.290		P14.293		P14.294		P14.290		P14.293		P14.294	
P14.291		P14.295		P14.296		P14.291		P14.295		P14.296	
P14.292		P14.299		P14.300		P14.292		P14.299		P14.300	
P14.293		P14.303		P14.304		P14.293		P14.303		P14.304	
P14.294		P14.307		P14.308		P14.294		P14.307		P14.308	
P14.295		P14.311		P14.312		P14.295		P14.311		P14.312	
P14.296		P14.315		P14.316		P14.296		P14.315		P14.316	
P14.297		P14.319		P14.320		P14.297		P14.319		P14.320	
P14.298		P14.323		P14.324		P14.298		P14.323		P14.324	
P14.299		P14.327		P14.328		P14.299		P14.327		P14.328	
P14.300		P14.331		P14.332		P14.300		P14.331		P14.332	
P14.301		P14.335		P14.336		P14.301		P14.335		P14.336	
P14.302		P14.339		P14.340		P14.302		P14.339		P14.340	
P14.303		P14.343		P14.344		P14.303		P14.343		P14.344	
P14.304		P14.347		P14.348		P14.304		P14.347		P14.348	
P14.305		P14.351		P14.352		P14.305		P14.351		P14.352	
P14.306		P14.355		P14.356		P14.306		P14.355		P14.356	
P14.307		P14.359		P14.360		P14.307		P14.359		P14.360	
P14.308		P14.363		P14.364		P14.308		P14.363		P14.364	
P14.309		P14.367		P14.368		P14.309		P14.367		P14.368	
P14.310		P14.371		P14.372		P14.310		P14.371		P14.372	
P14.311		P14.375		P14.376		P14.311		P14.375		P14.376	
P14.312		P14.379		P14.380		P14.312		P14.379		P14.380	
P14.313		P14.383		P14.384		P14.313		P14.383		P14.384	
P14.314		P14.387		P14.388		P14.314		P14.387		P14.388	
P14.315		P14.391		P14.392		P14.315		P14.391		P14.392	
P14.316		P14.395		P14.396		P14.316		P14.395		P14.396	
P14.317		P14.399		P14.400		P14.317		P14.399		P14.400	
P14.318		P14.403		P14.404		P14.318		P14.403		P14.404	
P14.319		P14.407		P14.408		P14.319		P14.407		P14.408	
P14.320		P14.411		P14.412		P14.320		P14.411		P14.412	
P14.321		P14.415		P14.416		P14.321		P14.415		P14.416	
P14.322		P14.419		P14.420		P14.322		P14.419		P14.420	
P14.323		P14.423		P14.424		P14.323		P14.423		P14.424	
P14.324		P14.427		P14.428		P14.324		P14.427		P14.428	
P14.325		P14.431		P14.432		P14.325		P14.431		P14.432	
P14.326		P14.435		P14.436		P14.326		P14.435		P14.436	

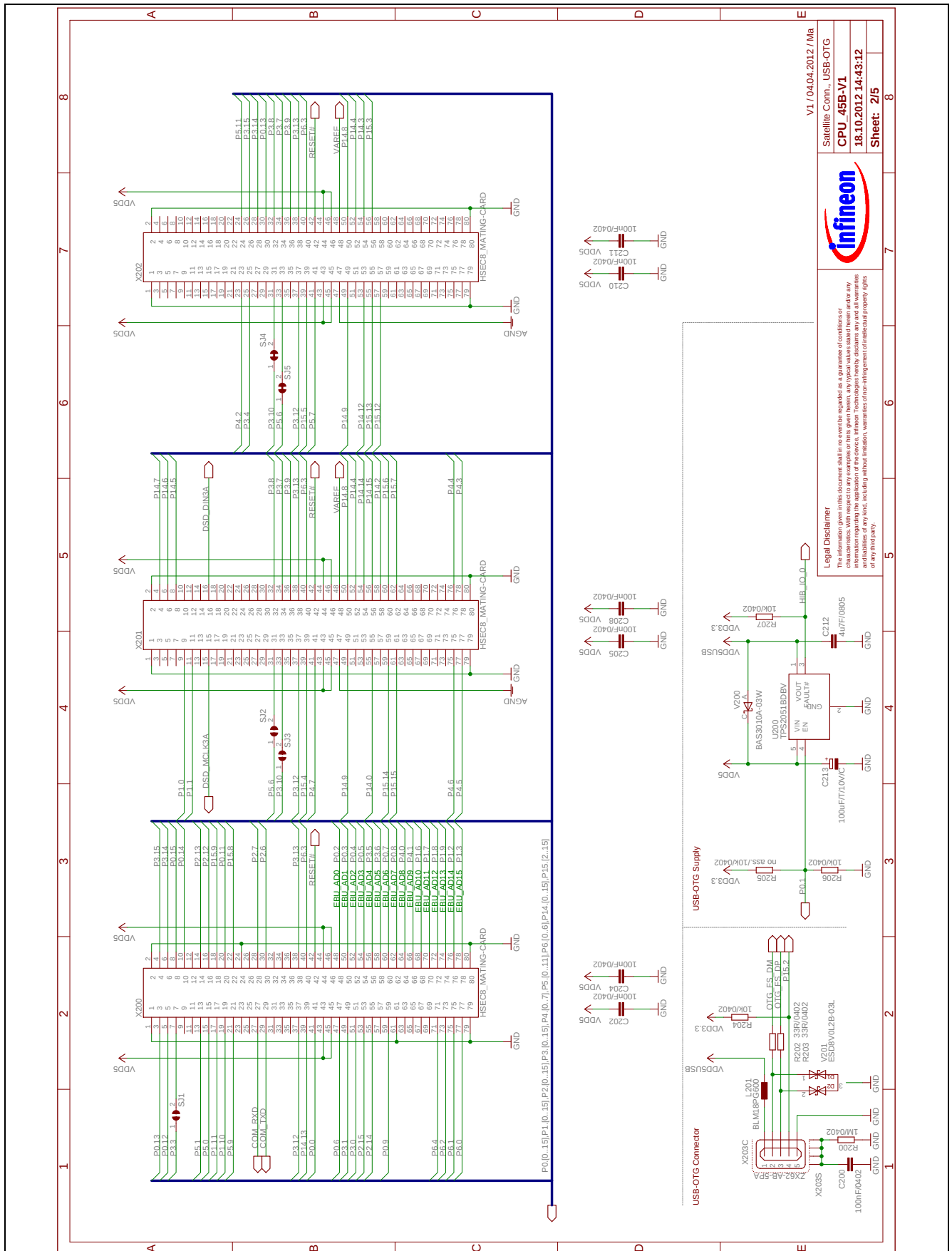


Figure 26 Satellite Connectors, USB-OTG

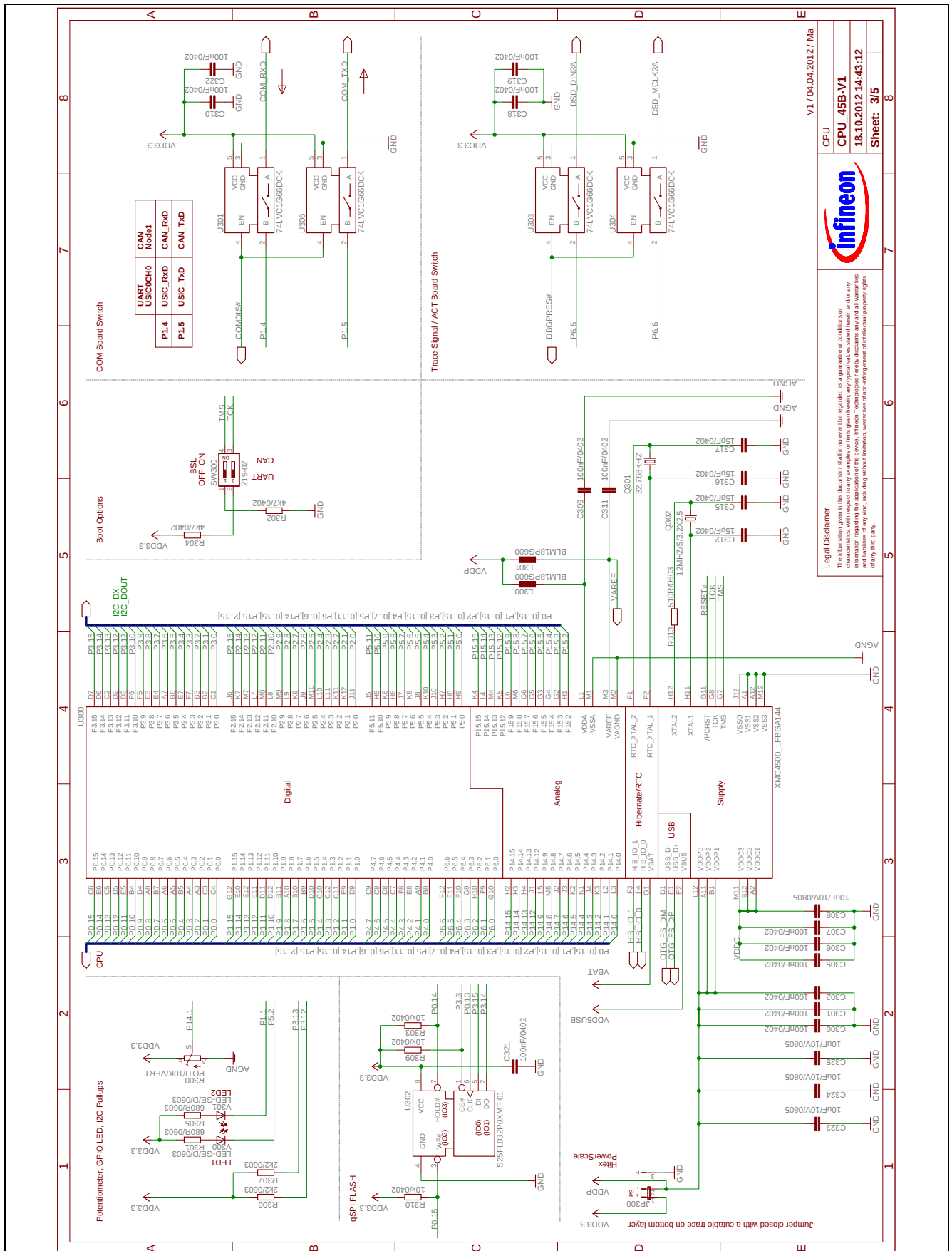


Figure 27 XMC4500

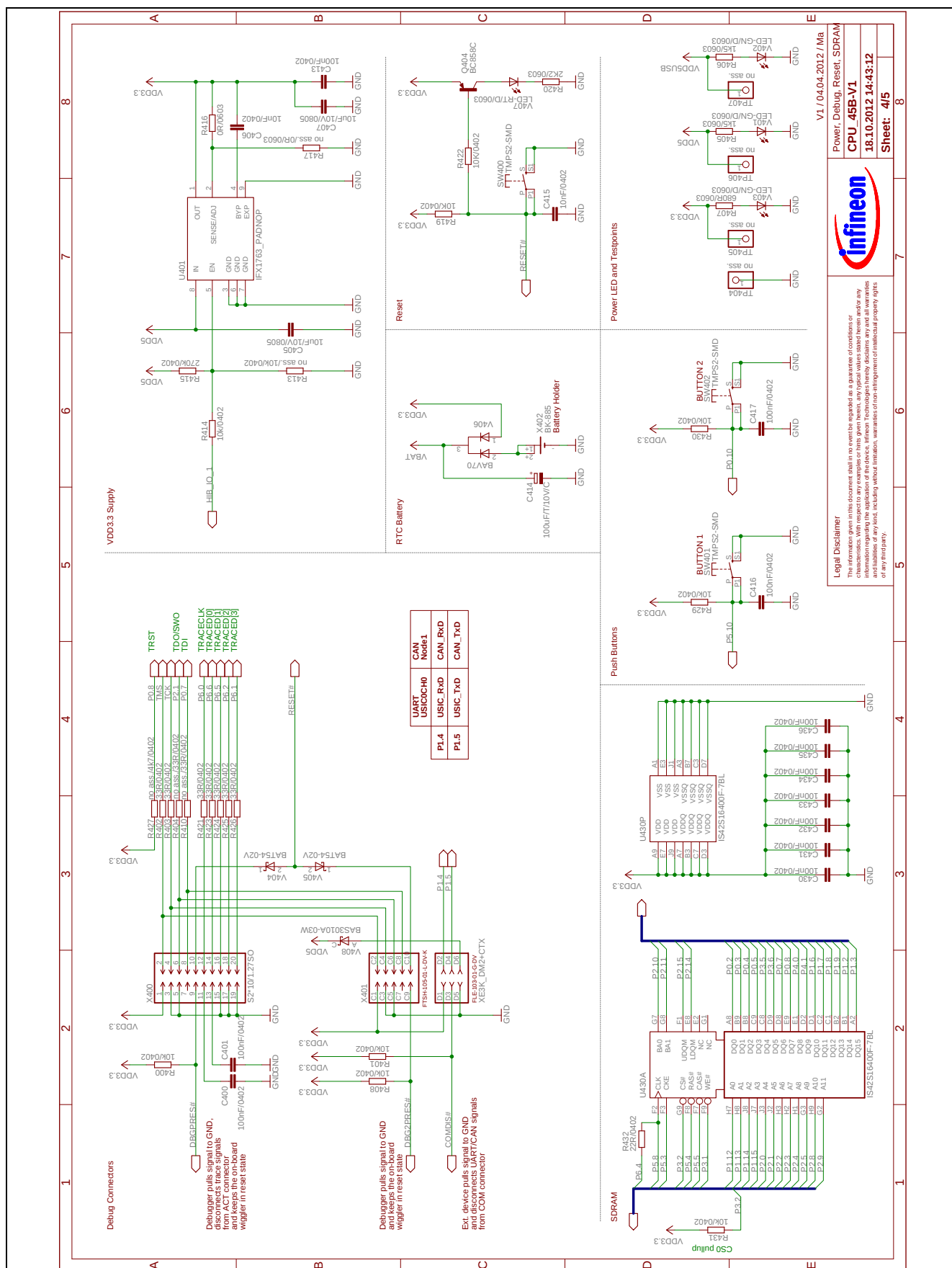


Figure 28 Power, Debug Connector, Reset, SDRAM

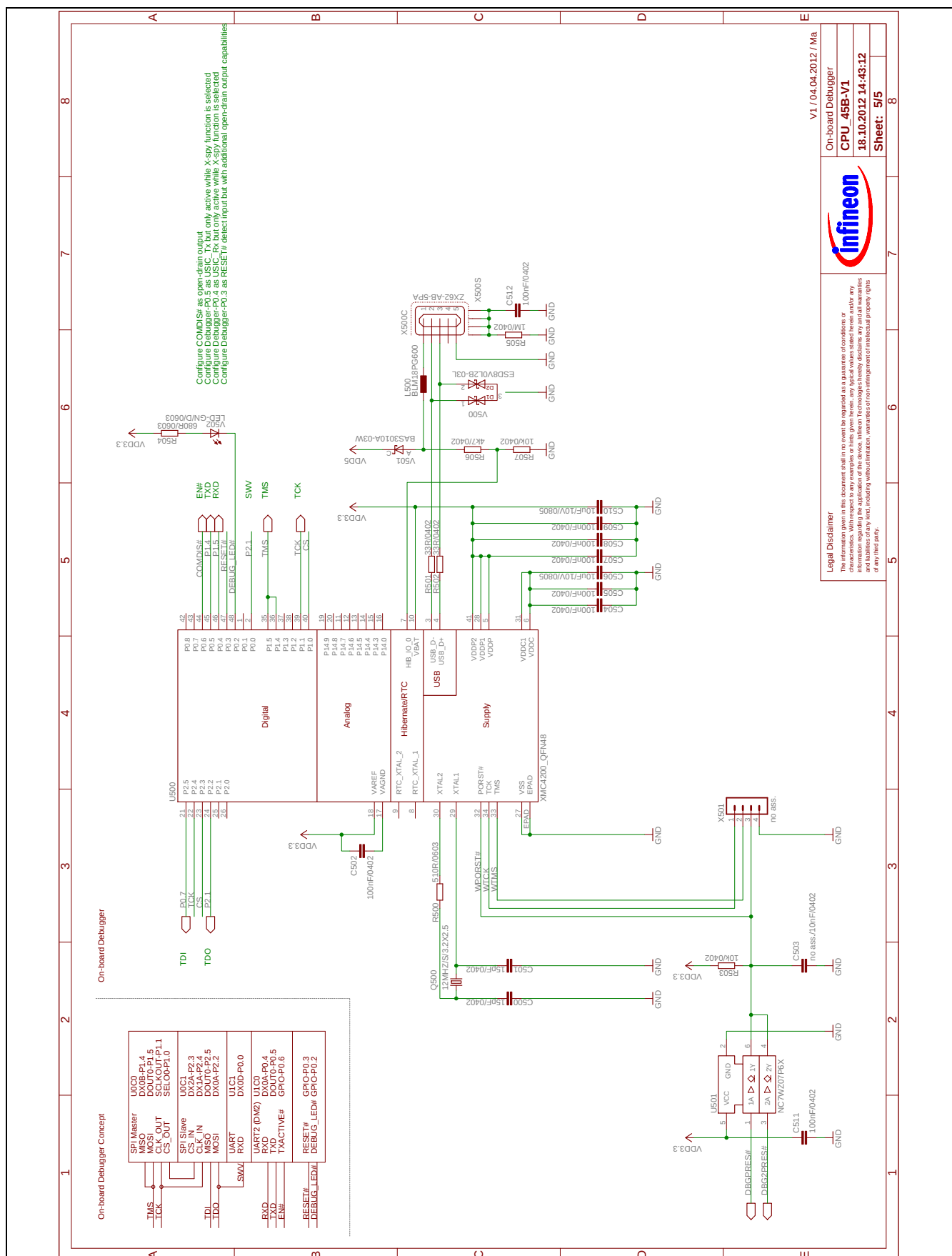


Figure 29 On-board Debugger

3.2 Component Placement and Geometry

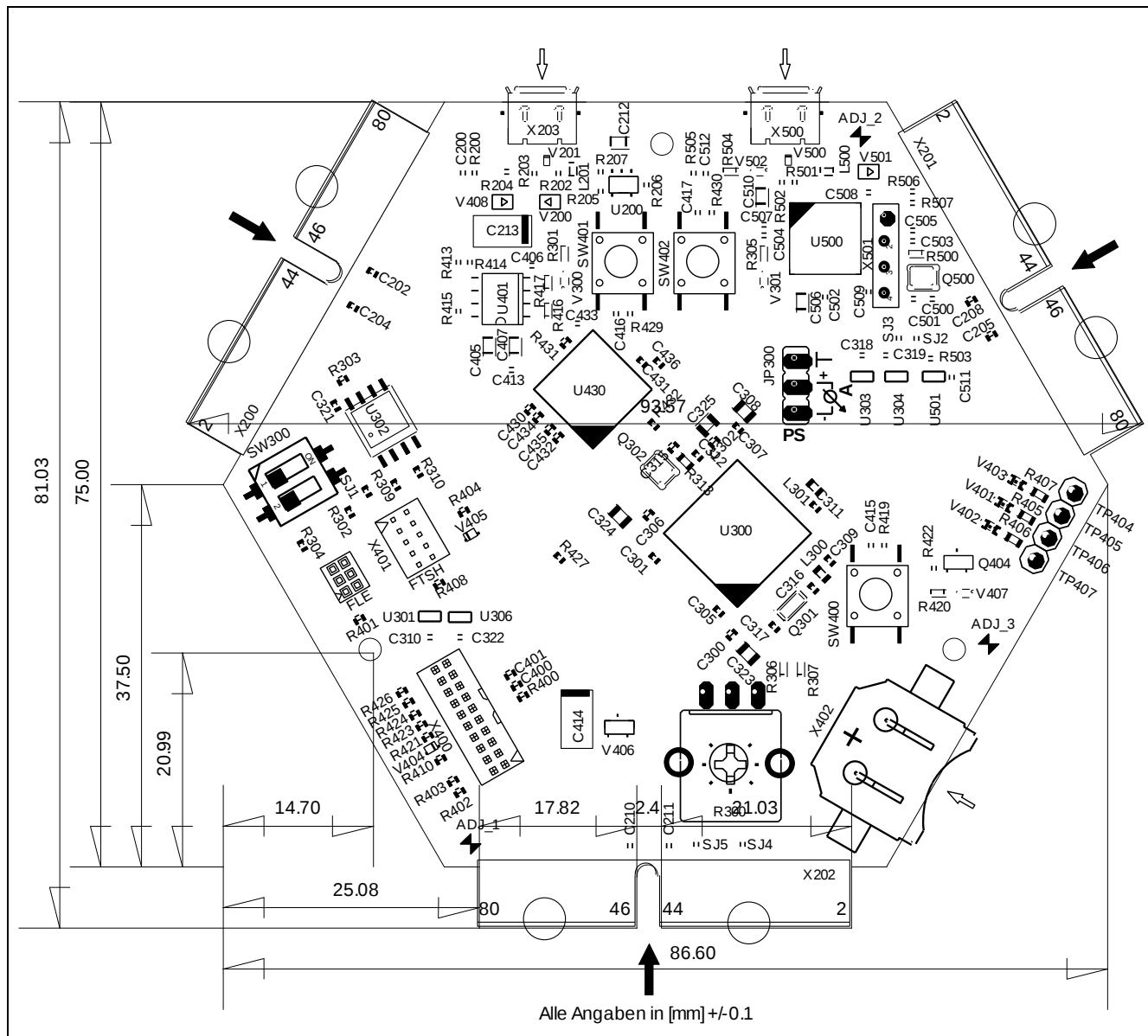


Figure 30 Component Placement and Geometry

3.3 Bill of Material (BOM)

Table 11 BOM of CPU_45B-V1 Board

Pos No.	Qty	Value	Device	Reference Des.
1	1	0R/0603	Resistor	R416
2	2	1M/0402	Resistor	R200, R505
3	2	1k5/0603	Resistor	R405, R406
4	3	2k2/0603	Resistor	R306, R307, R420
5	3	4k7/0402	Resistor	R302, R304, R506
6	1	4u7F/0805	Capacitor, ceramic	C212
7	17	10k/0402	Resistor	R204, R206, R207, R303, R309, R310, R400, R401, R408, R414, R419, R422, R429, R430, R431, R503, R507
8	2	10nF/0402	Capacitor	C406, C415
9	8	10uF/10V/0805	Capacitor, ceramic	C308, C323, C324, C325, C405, C407, C506, C510
10	2	12MHZ/S/3.2X2.5	Crystal, NX3225GD, NDK	Q302, Q500
11	6	15pF/0402	Capacitor	C312, C315, C316, C317, C500, C501
12	1	22R/0402	Resistor	R432
13	1	32.768KHZ	Crystal, NX3215SA, NDK	Q301
14	11	33R/0402	Resistor	R202, R203, R402, R403, R421, R423, R424, R425, R426, R501, R502
15	4	74LVC1G66DCK	IC, Single Analog Switch	U301, U303, U304, U306
16	40	100nF/0402	Capacitor	C200, C202, C204, C205, C208, C210, C211, C300, C301, C302, C305, C306, C307, C309, C310, C311, C318, C319, C321, C322, C413, C416, C417, C430, C431, C432, C433, C434, C435, C436, C400, C401, C502, C504, C505, C507, C508, C509, C511, C512
17	2	100uF/T/10V/C	Capacitor, bipolar	C213, C414
18	1	219-02	Dual DIP-Switch, 0.1" SMD	SW300
19	1	270k/0402	Resistor	R415
20	2	510R/0603	Resistor	R313, R500
21	4	680R/0603	Resistor	R301, R305, R407, R504
22	3	BAS3010A-03W	Diode, SOD323, Infineon	V200, V408, V501
23	2	BAT54-02V	Diode, SC79, Infineon	V404, V405
24	1	BAV70	Diode, SOT23-3, Infineon	V406
25	1	BC858C	Transistor, SOT23-3, Infineon	Q404

Production Data

26	1	BK-885	Battery Holder, 12mm Coin Cell	X402
27	4	BLM18PG600	Ferrite Bead, 0603, Murata	L201, L300, L301, L500
28	2	ESD8V0L2B-03L	Diode, TSLP-3-1, Infineon	V201, V500
29	3	HSEC8_MATING-CARD	Connector, Edgecard, Samtec	X200, X201, X202
30	1	IFX1763_PADNOP	Voltage Regulator, 3.3V LDO, Infineon	U401
31	2	LED-GE/D/0603	LED, yellow	V300, V301
32	4	LED-GN/D/0603	LED, green	V401, V402, V403, V502
33	1	LED-RT/D/0603	LED, red	V407
34	1	IS42S16400F-7BL	Synchronous Dynamic RAM, ISSI	U430
35	1	NC7WZ07P6X	IC, Dual Buffer OD, SC70-6	U501
36	1	POTI/10K/VERT	Potentiometer, K09K1130A8G, ALPS	R300
37	1	S2*10/1.27SO	Connector, FTSH-110-01-L-DV-K-P, Samtec	X400
38	1	S25FL032P0XMF101	IC, qSPI Flash Memory, SPANSION	U302
39	3	TMPS2-SMD	Switch, tactile	SW400, SW401, SW402
40	1	TPS2051BDBV	IC, Power Switch, SOT23-5	U200
41	1	XE3K_DM2+CTX	Connector, FTSH-105-01-LM-DV-K, w/o pin 7, Samtec Connector, FLE-103-01-G-DV, Samtec	X401
42	1	XMC4200_QFN48	IC, XMC4200, QFN48, Infineon	U500
43	1	XMC4500_LFBGA144	IC, XMC4500, LFBGA144, Infineon	U300
44	2	ZX62-AB-5PA	Connector, Micro-USB, Hirose	X203, X500
45	1	no ass.	Pinheader, 4-pin, 0.1" TH	X501
46	4	no ass.	Pinheader, 1-pin, 0.1" TH	TP404, TP405, TP406, TP407
47	1	no ass./0R/0603	Resistor	R417
48	1	no ass./4k7/0402	Resistor	R427
49	2	no ass./10k/0402	Resistor	R205, R413
50	1	no ass./10nF/0402	Capacitor	C503
51	2	no ass./33R/0402	Resistor	R404, R410
52	1	no ass.	Pinheader, 3-pin, 0.1" TH, Hitex PowerScale	JP300
53	3	no ass.	Solder Bridge (open)	SJ1, SJ2, SJ3
54	2	0R/0402	Solder Bridge (closed by resistor)	SJ4, SJ5

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