F^2MC-16LX

Flash Programming Manual

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1. Flash Memory

This chapter explains the flash memory.

1.1 Overview

Flash memory is rewritable built-in program memory.

1.1.1 Overview

Flash memory operates as built-in program memory. It allows data to be read by word and byte. As instruction codes can be fetched from the flash memory, the CPU can execute programs on the flash memory.

The flash memory is rewritable. Its data-write function enables data to be written by word. The data written through the data-write operation is saved to the flash memory and maintained even after the power is switched off. The flash memory is divided into sectors and this allows data to be erased by sector. It can also erase data from all of the sectors at once.

There are the following three methods to perform Data Write/Erase operation for flash memory.

- Execution of a program
- Serial programmer (flash memory writer)
- Parallel programmer (flash memory writer)

The flash security function can apply security to protect flash memory. When the security is applied, data cannot be read from, written to, or erased from the flash memory via external pins.

1.1.2 Features

Features of the flash memory are as follows:

- Data Write/Erase is possible according to the program execution of CPU.
- Commands can be performed automatically using automatic algorithms (equivalent to Embedded Algorithm).
- The hardware sequence flag detects the execution status of the automatic algorithm.
- Data can be written by word (16 bits).
- Data can be erased by sector or all sectors at once (chip erase).
- In flash memory mode, a parallel flash programmer can perform Data Write/Erase through external pins.
- Number of times Data Write/Erase operation (min.): 10,000 times
- Read cycle time (min.): 2 machine cycles

1.1.3 Size and Products of Flash Memory

Table 1-1 shows the product lineup of the flash memory.

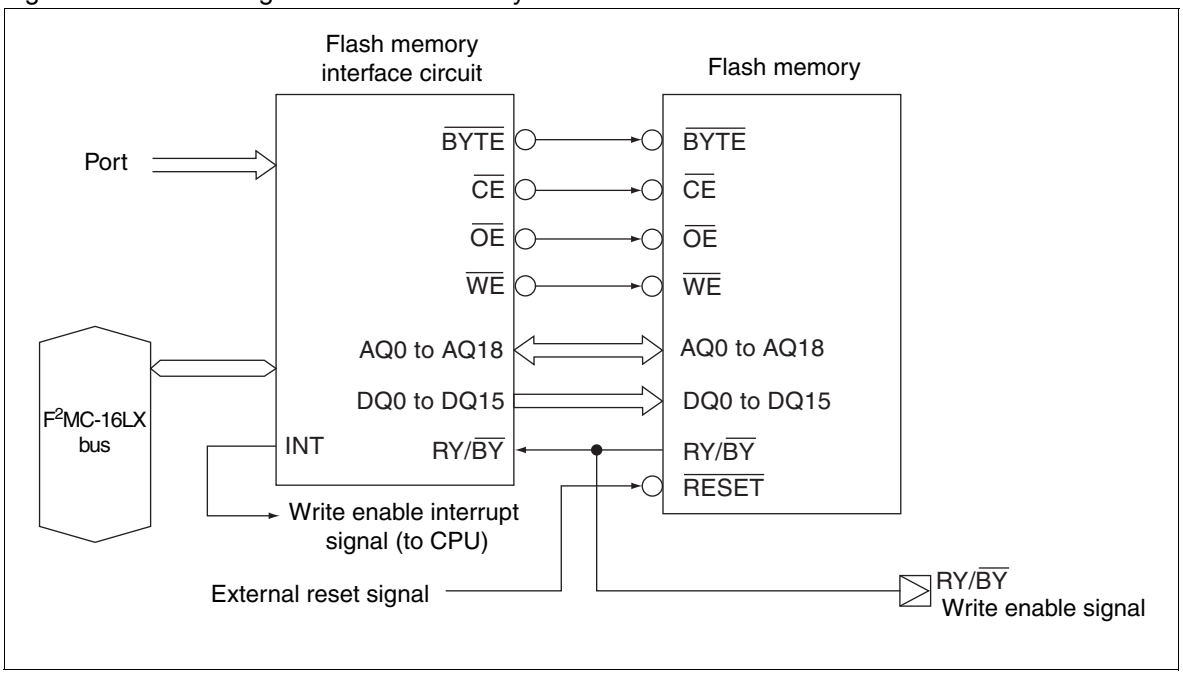
Table 1-1. Product Lineup of Flash Memory

Product	MB90F931, MB90F931S
Flash memory size	128 Kbytes
Flash memory area	$FE:0000_H$ to $FF:FFFF_H$
Sector configuration	8 Kbytes ´ 4 sectors 48 Kbytes ´ 2 sectors

1.1.4 Block Diagram

Figure 1-1 shows the block diagram of the flash memory.

Figure 1-1. Block Diagram of Flash Memory



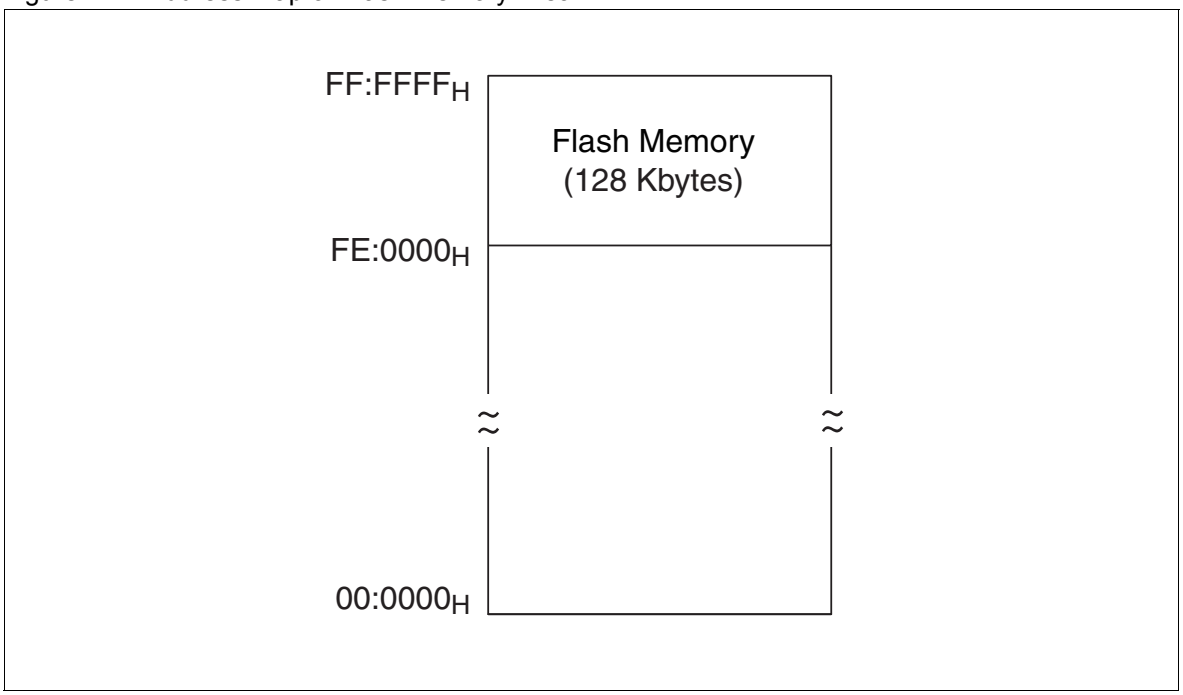
1.2 Address Map and Sector Configuration

The flash memory area is divided into sectors.

1.2.1 Flash Memory Area

Figure 1-2 shows the address map of the flash memory area.

Figure 1-2. Address Map of Flash Memory Area



1.2.2 Sector Configuration

Table 1-2 shows the sector configuration of the flash memory.

Table 1-2. Sector Configuration of Flash memory

Address Range	Bank	Sector
FF:FFFF$_H$ to FF:E000$_H$	FF$_H$	SA5 (8 Kytes)
FF:DFFF$_H$ to FF:C000$_H$		SA4 (8 Kytes)
FF:BFFF$_H$ to FF:0000$_H$		SA3 (48 Kytes)
FE:FFFF$_H$ to FE:4000$_H$	FE$_H$	SA2 (48 Kytes)
FE:3FFF$_H$ to FE:2000$_H$		SA1 (8 Kytes)
FE:1FFF$_H$ to FE:0000$_H$		SA0 (8 Kytes)

1.3 Registers

The flash memory has registers that control Data Write/Erase operations.

1.3.1 Flash Memory Registers

Table 1-3 shows the registers of the flash memory interface.

Table 1-3. Registers of Flash Memory Interface

Mnemonic	Register Name	Address	Size
FMCS	Flash Memory Control Status Register	$00:00AE_H$	Byte
FWR0	Flash Memory Write Control Register	$00:79A6_H$	Byte
FWR1		$00:79A7_H$	Byte

1.3.2 Flash Memory Control Status Register (FMCS)

This register indicates the status of and controls the flash memory.

1.3.2.1 Flash Memory Control Status Register (FMCS)

Table 1-4 shows the Bit configuration of Flash Memory Control Status Register (FMCS).

Table 1-4. Bit configuration of Flash Memory Control Status Register (FMCS)

bit	7	6	5	4	3	2	1	0
FMCS	INTE	RDYINT	WE	RDY	Reserved	Reserved	Reserved	Reserved
Bit attribute	R/W	R(1),W	R/W	R,WX	R/W0	R/W0	R/W0	R/W0
Initial value	0	0	0	X	0	0	0	0

R/W: Readable/writable
R(1),W: Readable and writable
R,WX: Read only
R/W0: Always write "0"
X: Undefined

Use a byte access to access the flash memory control status register (FMCS).

[bit7] INTE : Flash memory interrupt enable bit

This bit enables an interrupt request upon completion of the automatic algorithm of Data Write/Erase operation. An interrupt request occurs, if the RDYINT bit is set to "1" when the INTE bit is "1". The initial value of the INTE bit is "0". For this series, always write "0" to this bit.

INTE	Flash memory interrupt enable bit
0	Disables interrupt on completion of Data Write/Erase operation
1	Enables interrupt on completion of Data Write/Erase operation

[bit6] RDYINT : Flash memory interrupt request flag

This bit is an interrupt request flag set upon completion of the automatic algorithm of Data Write/Erase operation. When data write/erase operation is completed, the RDYINT bit becomes "1". An interrupt request occurs, if the RDYINT bit is set to "1" when the INTE bit is "1".

Writing "0" to the RDYINT bit clears the bit. Writing "1" to the RDYINT bit is ignored. Using a read modify write (RMW) instruction, the read value is "1". The initial value of the RDYINT bit is "0".

RDYINT	Flash memory interrupt request flag	
	Read operation	Write operation
0	Performing the data write/erase operation or not activated	Clears the RDYINT bit
1	Data Write/Erase operation has been completed	No effect

[bit5] WE : Flash memory write enable bit

This bit enables write access to the flash memory area. Setting the WE bit to "1" enables write access and allows the command for data write/erase operation of the flash memory to be issued. Setting the WE bit to "0" ignores a write access to the flash memory area. The initial value of the WE bit is "0".

WE	Flash memory write enable bit
0	Disables write access
1	Enables write access

[bit4] RDY : Data Write/Erase status bit

This bit indicates the status of the execution of the automatic algorithm of Data Write/Erase operation. The RDY bit detects the status of the flash memory by hardware. The RDY bit is a read-only bit. Writing does not affect the value of the RDY bit. The initial value of the RDY bit is undefined.

RDY	Data Write/Erase status bit
0	Performing the data write/erase operation (busy status)
1	The data write/erase operation has been completed or not activated (ready status)

[bit3 to bit0] Reserved

These bits are reserved bits. Always write "0" to these bits. The read value is "0", the value written to them. The initial value is "0".

1.3.3 Flash Memory Write Control Register (FWR1/FWR0)

This register enables/disables write access to each sector of the flash memory.

1.3.3.1 Flash Memory Write Control Register (FWR1/FWR0)

Figure 1-3 shows the bit configuration of the flash memory write control register (FWR1/FWR0).

Figure 1-3. Bit configuration of Flash Memory Write Control Register (FWR1/FWR0)

bit	15	14	13	12	11	10	9	8
FWR1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit attribute	RX,W0	RX,W0	RX,W0	RX,W0	RX,W0	RX,W0	RX,W0	RX,W0
Initial value	X	X	X	X	X	X	X	X
bit	7	6	5	4	3	2	1	0
FWR0	Reserved	Reserved	SA5E	SA4E	SA3E	SA2E	SA1E	SA0E
Bit attribute	RX,W0	RX,W0	R,W	R,W	R,W	R,W	R,W	R,W
Initial value	X	X	0	0	0	0	0	0

R,W: Readable and writable
RX,W0: Always write "0"
X: Undefined

[bit15 to bit6] Reserved

These bits are reserved bits. Always write "0" to these bits. The read value is undefined.

[bit5 to bit0] SA5E to SA0E : Accidental write prevention setting bits

These bits set the accidental write prevention for corresponding sectors of the flash memory. Writing "1" to the SAxE bit allows write access to the corresponding sector. Writing "0" to the SAxE bit enables write-protect function and disables write access to the corresponding sector. The initial value of the SAxE bit is "0".

SAxE	Accidental write prevention setting bit
0 (after reset)	Disables write access
1	Enables write access
0	Prevents accidental write

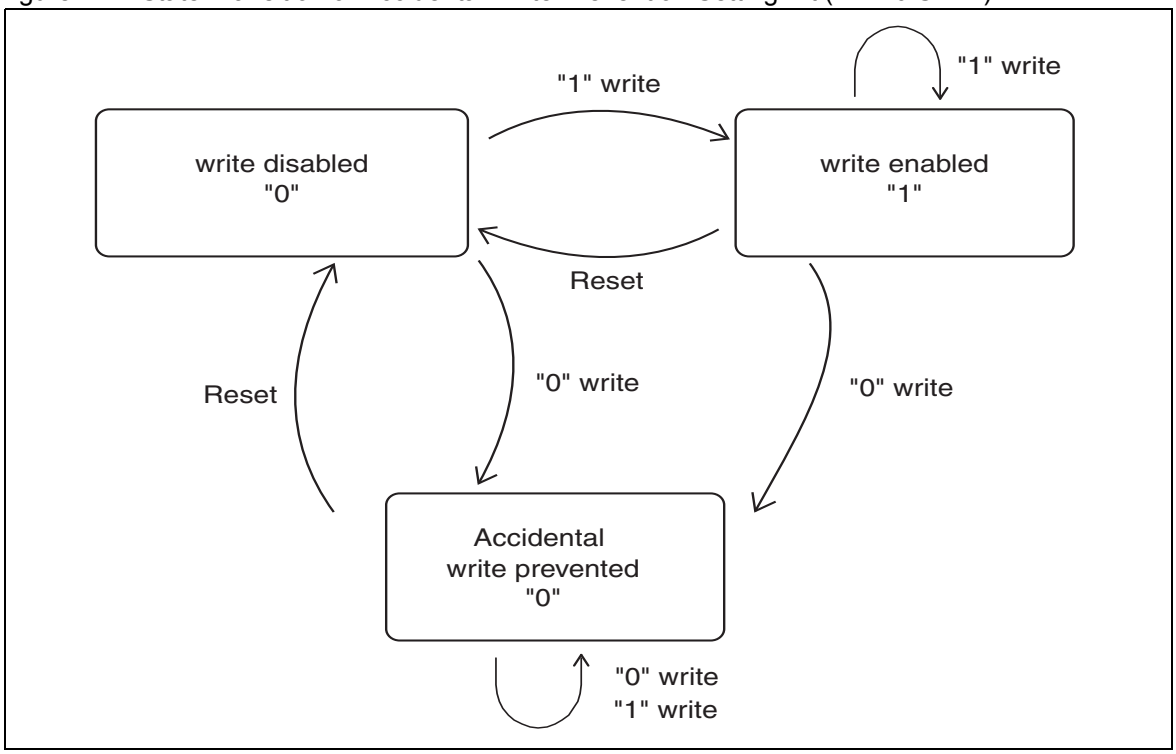
Table 1-5 shows the sectors corresponding to accidental write prevention setting bits (FWR0:SAxE).

Table 1-5. Sectors Corresponding to Accidental Write Prevention Setting Bits (FWR0:SAxE)

	Bit Name	Corresponding sector	Remarks
7	Reserved	¾	Set these bits to "0".
6	Reserved	¾	
5	SA5E	SA5	
4	SA4E	SA4	
3	SA3E	SA3	
2	SA2E	SA2	
1	SA1E	SA1	
0	SA0E	SA0	

A reset initializes the accidental write prevention setting bit (FWR0:SAxE) to "0". After reset, the write disabled status is maintained until the first write access to the flash memory write control register (FWR0:FWRx). When "1" is written at the first write access after the reset, the write-enabled status is set. Writing "0" to the bit in the write-enabled status changes it to the write-protected status. When "0" is written at the first write access after the reset, the write-protected status is set. Even if "1" is written to the bit in the write-protected status, the accidental write prevention setting bit is not set to "1" and remains in the write-protected status. Figure 1-4 shows the state transition of accidental write prevention setting bit (FWR0:SAxE).

Figure 1-4. State Transition of Accidental Write Prevention Setting Bit (FWR0:SAxE)



1.4 Setting for Data Write/Erase Operations

This section explains the setting methods for Data Write/Erase operation of the flash memory.

1.4.1 Enabling/Disabling Write Access to Sectors

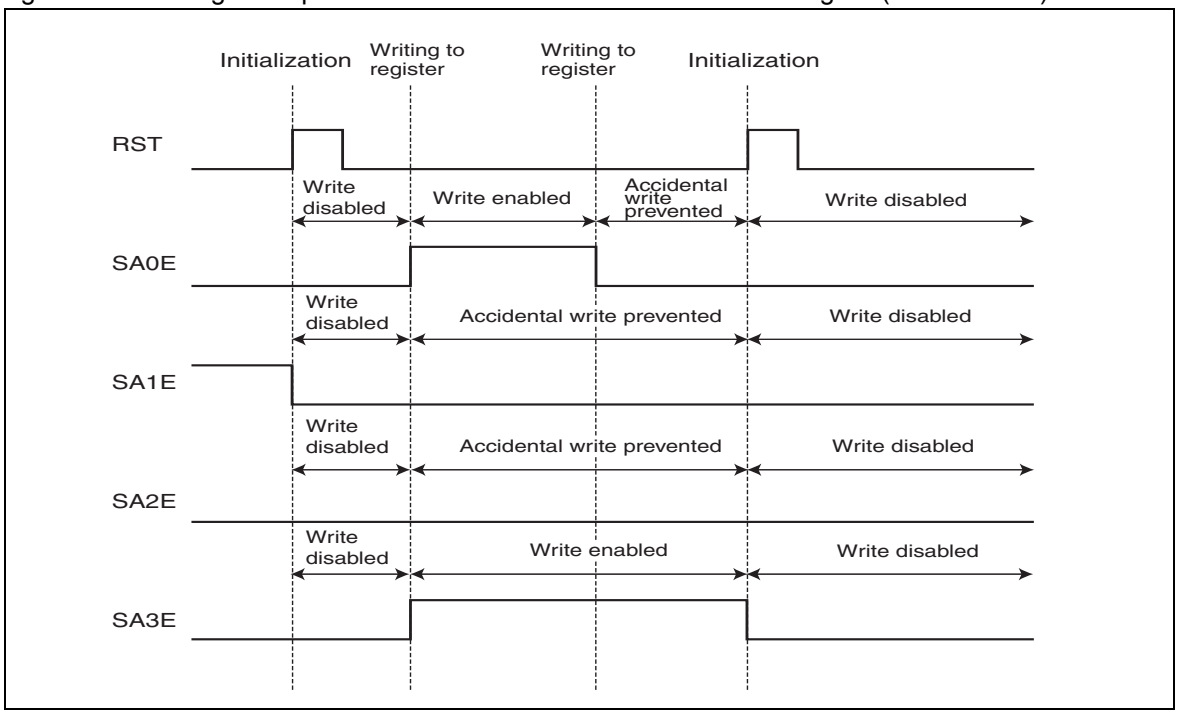
Before performing Data Write/Erase operation to the flash memory, set the accidental write prevention setting bit (FWR0:SAxE). Write access is allowed to the sectors to which both the flash memory write enable bit (FMCS:WE) and the corresponding accidental write prevention setting bit (FWR0:SAxE) have been set to enable write operation. Table 1-6 shows the relationship between the write enable bit (FMCS:WE) and the accidental write prevention setting bit (FWR0:SAxE).

Table 1-6. Relationship between Write Enable Bit (FMCS:WE) and Accidental Write Prevention Setting Bit (FWR0:SAxE)

Write enable bit (FMCS:WE)	Accidental write prevention setting bit (FWR0:SAxE)	Enabling/disabling of sector write operation
0	0	Disables write access
0	1	
1	0	
1	1	Enables write access

The accidental write prevention setting bit (FWR0:SAxE) can be set to the write-enabled status by only the first register writing after a reset. Set it to the write-enabled status only for the sectors which is to be performed Data Write/Erase operation. Figure 1-5 shows a setting example of the accidental write prevention setting bit (FWR0:SAxE).

Figure 1-5. Setting Example of the Accidental Write Prevention Setting Bit (FWR0:SAxE)



1.4.2 Enabling Write Access to Flash Memory

Set the flash memory write enable bit (FMCS:WE) to enable write access (FMCS:WE="1"), immediately before Data Write/Erase operations. After completing the data write/erase operation, set the bit to disable write access (FMCS:WE="0").

When the automatic algorithm of Data Write /erase operation is activated by issuing a command to the flash memory, no instruction or data can be read from the flash memory. When performing a Data Write/Erase operation, disable all interrupts. Because it becomes impossible to read the interrupt vector area while executing an automatic algorithm, the interrupt cannot be used.

1.4.3 Performing Data Write/Erase Operation for the Flash Memory

It is necessary to perform Data Write/Erase operation of the Flash Memory via a program on RAM. Copy to RAM a program that performs Data Write/Erase operation. Then, execute the program on RAM to perform Data Write/Erase operation.

Use the following procedure for performing Data Write/Erase operation for the Flash Memory.

1. Copy a program code to RAM.
2. Disable all interrupts
3. Branch to the copied program on RAM.
4. Set the flash memory to enable write access (FMCS:WE="1").
5. Perform Data Write/Erase operations to the flash memory.
6. Set the flash memory to disable write access (FMCS:WE="0").
7. Return to the program on the flash memory.
8. Enable interrupt.

1.5 Automatic Algorithm

On the flash memory, Data Write/Erase operation is performed using an automatic algorithm.

1.5.1 Automatic Algorithm

Issue a command by writing command sequence to the flash memory. Once the command is issued, the automatic algorithm is activated. The automatic algorithm completes automatically after performing Data Write/Erase operation, and then the flash memory returns to the read/reset state. The flash memory has the following commands:

1. Reset command
2. Data write command
3. Chip erase command
4. Sector erase command
5. Sector erase suspend command
6. Sector erase resume command

1.5.2 Command Sequence

Write the command sequence continuously in the flash memory area. If data other than the command sequence is written to the flash memory area in the middle of the command sequence, the command will not be issued correctly. The command sequence has meanings in both the address and data. Write the command sequence to write enabled sectors of the flash memory.

Set the flash memory to enable write access (FMCS:WE="1"), then write the command sequence by word access. The upper byte of data, except for writing data (PD) by the data write command, is ignored. For example, apply an upper byte to the same value as lower byte (AA_H) like $AAAA_H$.

Write the command sequence correctly. If data is written to an improper address or written in an incorrect order, the flash memory returns to the read/reset state.

Table 1-7 shows the command sequence of the flash memory.

Table 1-7. Command Sequence of Flash Memory

Command		First writing	Second writing	Third writing	Fourth writing	Fifth writing	Sixth writing
Reset	Address	$XXXXXe_H$	-	-	-	-	-
	Data	$F0F0_H$	-	-	-	-	-
Reset	Address	$XXXAAA_H$	$XXX554_H$	$XXXAAA_H$	-	-	-
	Data	$AAAA_H$	5555_H	$F0F0_H$	-	-	-
Data write	Address	$XXXAAA_H$	$XXX554_H$	$XXXAAA_H$	PA	-	-
	Data	$AAAA_H$	5555_H	$A0A0_H$	PD	-	-
Chip erase	Address	$XXXAAA_H$	$XXX554_H$	$XXXAAA_H$	$XXXAAA_H$	$XXX554_H$	$XXXAAA_H$
	Data	$AAAA_H$	5555_H	8080_H	$AAAA_H$	5555_H	1010_H
Sector erase	Address	$XXXAAA_H$	$XXX554_H$	$XXXAAA_H$	$XXXAAA_H$	$XXX554_H$	SA
	Data	$AAAA_H$	5555_H	8080_H	$AAAA_H$	5555_H	3030_H
Sector erase Suspend	Address	$XXXXXe_H$	-	-	-	-	-
	Data	$B0B0_H$	-	-	-	-	-
Sector erase Resume	Address	$XXXXXe_H$	-	-	-	-	-
	Data	3030_H	-	-	-	-	-

PA : Data writing address (word address)

PD : Write data (word data)

SA : Erase sector address

e : Even hexadecimal number (0, 2, 4, 6, 8, A, C, E)

1.5.3 Reset Command

The flash memory can be placed in read/reset state by issuing reset command.

1.5.3.1 Reset Command

Table 1-8 and Table 1-9 show the command sequence of the reset command. The reset command has two patterns of the command sequence, both have the same function.

Table 1-8. Command Sequence 1 of Reset Command

	Address		Data
	Formula	Value	
First writing	(adrs & $FFFFFE_H$)	$XXXXXe_H$	$F0F0_H$
adrs: Address in write enabled sectors of the flash memory area e : Even hexadecimal number (0, 2, 4, 6, 8, A, C, E)			

Table 1-9. Command Sequence 2 of Reset Command

	Address		Data
	Formula	Value	
First writing	(adrs & $FFF000_H$) + AAA_H	$XXXAAA_H$	$AAAA_H$
Second writing	(adrs & $FFF000_H$) + 554_H	$XXX554_H$	5555_H
Third writing	(adrs & $FFFF000_H$) + AAA_H	$XXXAAA_H$	$F0F0_H$

adrs: Address in write enabled sectors of the flash memory area

1.5.4 Data Write Command

The word data can be written in the flash memory by issuing the data write command.

1.5.4.1 Data Write Command

Table 1-10 shows the command sequence of the data write command.

Table 1-10. Command Sequence of Data Write Command

	Address		Data
	Formula	**Value**	
First writing	(adrs & $FFF000_H$) + AAA_H	$XXXAAA_H$	$AAAA_H$
Second writing	(adrs & $FFF000_H$) + 554_H	$XXX554_H$	5555_H
Third writing	(adrs & $FFF000_H$) + AAA_H	$XXXAAA_H$	$A0A0_H$
Fourth writing	(adrs & $FFFFFE_H$)	PA	PD
adrs: Address in write enabled sectors of the flash memory area			

The flash memory starts the automatic algorithm for data-write operation when the address and data of the fourth writing of the command sequence is written. During the execution of the automatic algorithm for data-write operation, only the reset command can be issued. And any write access to the flash memory (issuing the command) other than the reset command is ignored.

1.5.5 Chip Erase Command

The contents of all sectors of the flash memory can be erased by issuing the chip erase command.

1.5.5.1 Chip Erase Command

Table 1-11 shows the command sequence of the chip erase command.

Table 1-11. Command Sequence of Chip Erase Command

	Address		Data
	Formula	Value	
First writing	(adrs & $FFF000_H$) + AAA_H	$XXXAAA_H$	$AAAA_H$
Second writing	(adrs & $FFF000_H$) + 554_H	$XXX554_H$	5555_H
Third writing	(adrs & $FFF000_H$) + AAA_H	$XXXAAA_H$	8080_H
Fourth writing	(adrs & $FFF000_H$) + AAA_H	$XXXAAA_H$	$AAAA_H$
Fifth writing	(adrs & $FFF000_H$) + 554_H	$XXX554_H$	5555_H
Sixth writing	(adrs & $FFF000_H$) + AAA_H	$XXXAAA_H$	1010_H
adrs: Address in write enabled sectors of the flash memory area			

The flash memory starts the automatic algorithm for chip erase operations when the sixth writing of the command sequence are written. During the execution of the automatic algorithm for chip erase operations, only the reset command can be issued. And any write access to the flash memory (issuing the command) other than the reset command is ignored.

1.5.6 Sector Erase Command

The contents of each sector of the flash memory can be erased by issuing the sector erase command.

1.5.6.1 Sector Erase Command

Table 1-12 shows the command sequence of the sector erase command.

Table 1-12. Command Sequence of Sector Erase Command

	Address		Data
	Formula	Value	
First writing	(adrs & $FFF000_H$) + AAA_H	$XXXAAA_H$	$AAAA_H$
Second writing	(adrs & $FFF000_H$) + 554_H	$XXX554_H$	5555_H
Third writing	(adrs & $FFF000_H$) + AAA_H	$XXXAAA_H$	8080_H
Fourth writing	(adrs & $FFF000_H$) + AAA_H	$XXXAAA_H$	$AAAA_H$
Fifth writing	(adrs & $FFF000_H$) + 554_H	$XXX554_H$	5555_H
Sixth writing	(adrs & $FFFFFE_H$)	SA	3030_H
adrs: Address in write enabled sectors of the flash memory area			

When the command sequence is written, the flash memory starts the automatic algorithm for sector erase operation.

The sixth writing of the command sequence is a sector erase code. Writing the sector erase code of the command sequence starts a sector erase time-out period. The next sector erase code can be written during this sector erase time-out period. Multiple target sectors can be specified for sector erase operation by writing the sector erase code more than once. Table 1-13 shows the sector erase code.

Table 1-13. Sector Erase Code

	Address		Data
	Formula	Value	
After seventh writing	(adrs & $FFFFFE_H$)	SA	3030_H

adrs: Address in write enabled sectors of the flash memory area

SA : Erase sector address

During the execution of the automatic algorithm for sector erase operations, only the sector erase suspend command and the reset command can be issued.

1.5.7 Sector Erase Suspend Command

The sector erase operation can be suspended temporarily by issuing sector erase suspend command.

1.5.7.1 Sector Erase Suspend Command

Table 1-14 shows the command sequence of the sector erase suspend command.

Table 1-14. Command Sequence of Sector Erase Suspend Command

	Address		Data
	Formula	**Value**	
First writing	**(adrs & $FFFFFE_H$)**	**$XXXXXe_H$**	**$B0B0_H$**
adrs: Address in write enabled sectors of the flash memory area e : Even hexadecimal number (0, 2, 4, 6, 8, A, C, E)			

If the sector erase suspend command is issued during the execution of the automatic algorithm for sector erase operations, the flash memory temporarily suspends the sector erase operation. During the suspension of the sector erase operation, data can be read from sectors other than the sector that was specified for the erase target by preceding sector erase command. Even if the sector erase suspend command is reissued during the suspension of the sector erase operation, that command is ignored.

1.5.8 Sector Erase Resume Command

The suspended sector erase operation can be resumed by issuing sector erase resume command.

1.5.8.1 Sector Erase Resume Command

Table 1-15 shows the command sequence of the sector erase resume command.

Table 1-15. Command Sequence of Sector Erase Resume Command

	Address		Data
	Formula	**Value**	
First writing	(adrs & $FFFFFE_H$)	$XXXXXe_H$	3030_H
adrs: Address in write enabled sectors of the flash memory area e : Even hexadecimal number (0, 2, 4, 6, 8, A, C, E)			

When the sector erase resume command is issued during the suspension of a sector erase operation, the flash memory resumes the sector erase operation. Even if the sector erase resume command is issued at a time other than during the suspension of a sector erase operation, that command is ignored.

1.6 Hardware Sequence Flag

During the execution of the automatic algorithm for the Data Write/Erase operation, data reading from the flash memory area is the hardware sequence flag. The hardware sequence flag indicates the progress/completion of the automatic algorithm.

1.6.1 Hardware Sequence Flag

The hardware sequence flag can be read by reading from the flash memory area after the automatic algorithm is activated.

The hardware sequence flag consists of the following bits:

- Data polling flag (DQ7)
- Toggle bit flag (DQ6)
- Timing limit exceeded flag (DQ5)
- Sector erase timer flag (DQ3)

Read the hardware sequence flag by word assess or byte access. When it is read by word access, the lower byte represents the hardware sequence flag. In case of byte access, read it from the even-numbered address. Figure 1-6 shows the position of the hardware sequence flag.

Figure 1-6. Position of Hardware Sequence Flag

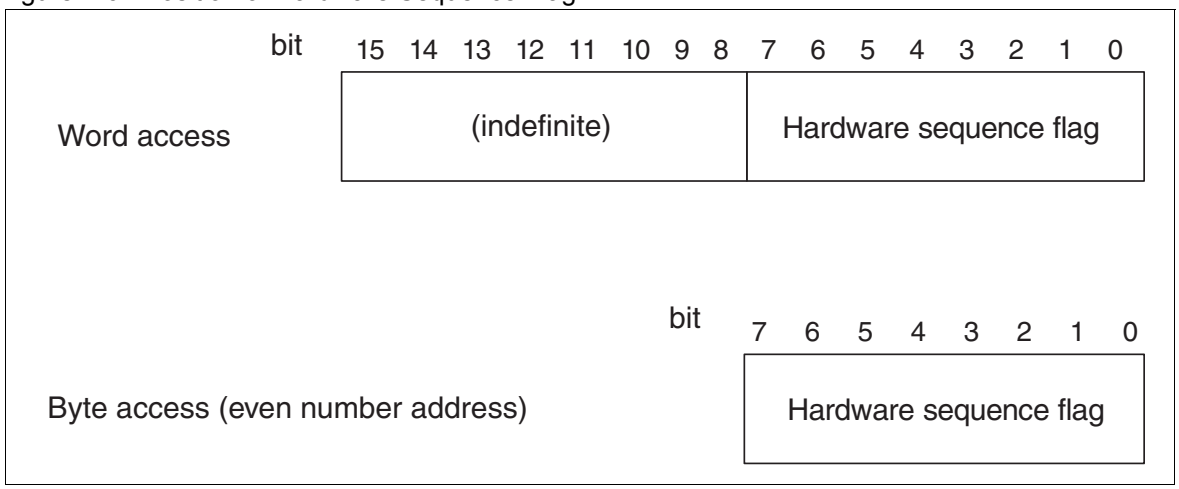


Figure 1-7 shows the bit configuration of hardware sequence flag. The read value of undefined bits of the hardware sequence flag is indeterminate.

Figure 1-7. Bit Configuration of Hardware Sequence Flag

bit	7	6	5	4	3	2	1	0
Hardware Sequence Flag	DQ7	DQ6	DQ5	Undefined	DQ3	Undefined	Undefined	Undefined
	R	R	R	R	R	R	R	R

Table 1-16 shows the list of states of hardware sequence flag. "End of execution (read/reset state)" in Table 1-16 is not a result of the hardware sequence flag but a result of a usual read. To make easily to compare, the item is shown in the table.

Table 1-16. List of States of Hardware Sequence Flag

Execution status of automatic algorithm			DQ7	DQ6	DQ5	DQ3
End of execution (read/reset state)			DATA[7]	DATA[6]	DATA[5]	DATA[3]
Execution in progress	Data write		$\overline{PD[7]}$	Toggle	0	0
	Chip erase		0	Toggle	0	1
	Sector erase	Timeout period	1	Toggle	0	0
		Erasing	0	Toggle	0	1
	Sector erase suspend	Read (sector to be erased)	1	1	0	0
		Read (sectors not to be erased)	DATA[7]	DATA[6]	DATA[5]	DATA[3]
Timing limit exceeded	Data write		$\overline{PD[7]}$	Toggle	1	0
	Chip erase		0	Toggle	1	1
	Sector erase		0	Toggle	1	1

$\overline{PD[7]}$: Value reversed from bit 7 of writing data specified by Data write command

DATA : Data written in the read address

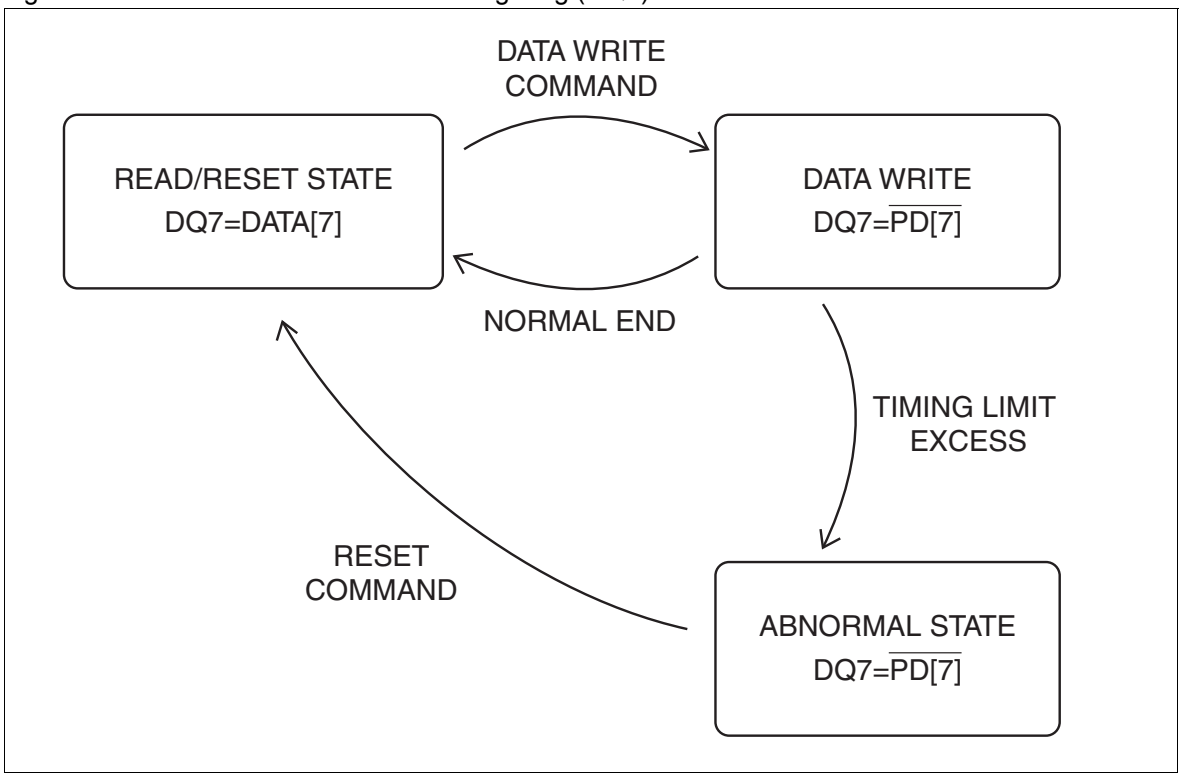
1.6.2 Data Polling Flag (DQ7)

The data polling flag (DQ7) indicates that the automatic algorithm is currently being executed.

1.6.2.1 Data Write Operation

The data polling flag (DQ7) can be read by making read access to the flash memory area during the execution of the automatic algorithm for writing data. Figure 1-8 shows the state transition of the data polling flag (DQ7) at the data write.

Figure 1-8. State Transition of Data Polling Flag (DQ7) at Data Write



When the data polling flag (DQ7) is read during the execution of the automatic algorithm, its read value is the value reversed from bit 7 of the write data (PD). The read address is any address in the flash memory area. The write data (PD) is the data specified by the data write command.

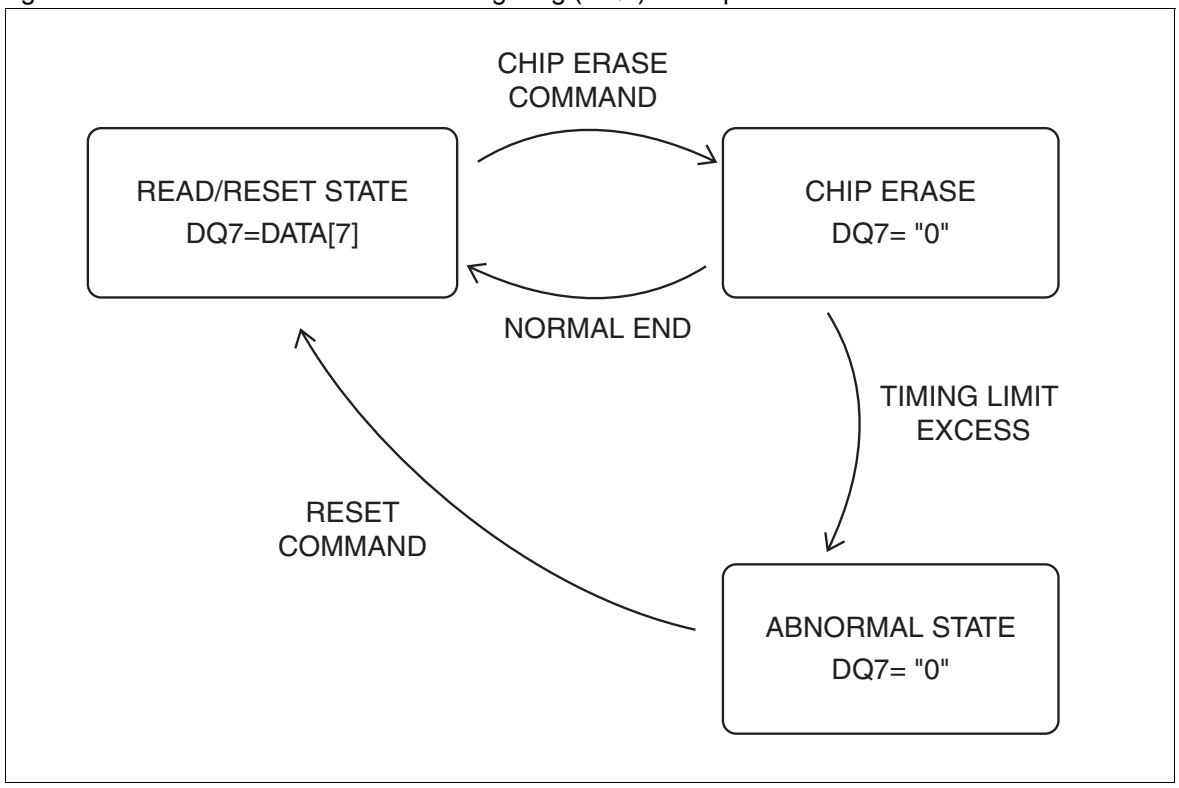
When the flag is read after the completion of the automatic algorithm, the read value is bit 7 of the data at that address. The flash memory returns to the read/reset state. The data written in the flash memory is read as normal read data.

Read the address (PA) specified by the data write command as the data polling flag (DQ7). During the execution of the automatic algorithm, it indicates the value reversed from bit 7 of the write data (PD). After the completion of the automatic algorithm, it indicates the value of bit 7 of the write data (PD). Although the written data (DATA) is read after the completion of the automatic algorithm, that value is actually the same as the write data (PD).

1.6.2.2 *Chip Erase Operation*

The data polling flag (DQ7) can be read by making read access to the flash memory area during the execution of the automatic algorithm for chip erase operations. Figure 1-9 shows the state transition of the data polling flag (DQ7) at the chip erase.

Figure 1-9. State Transition of Data Polling Flag (DQ7) at Chip Erase



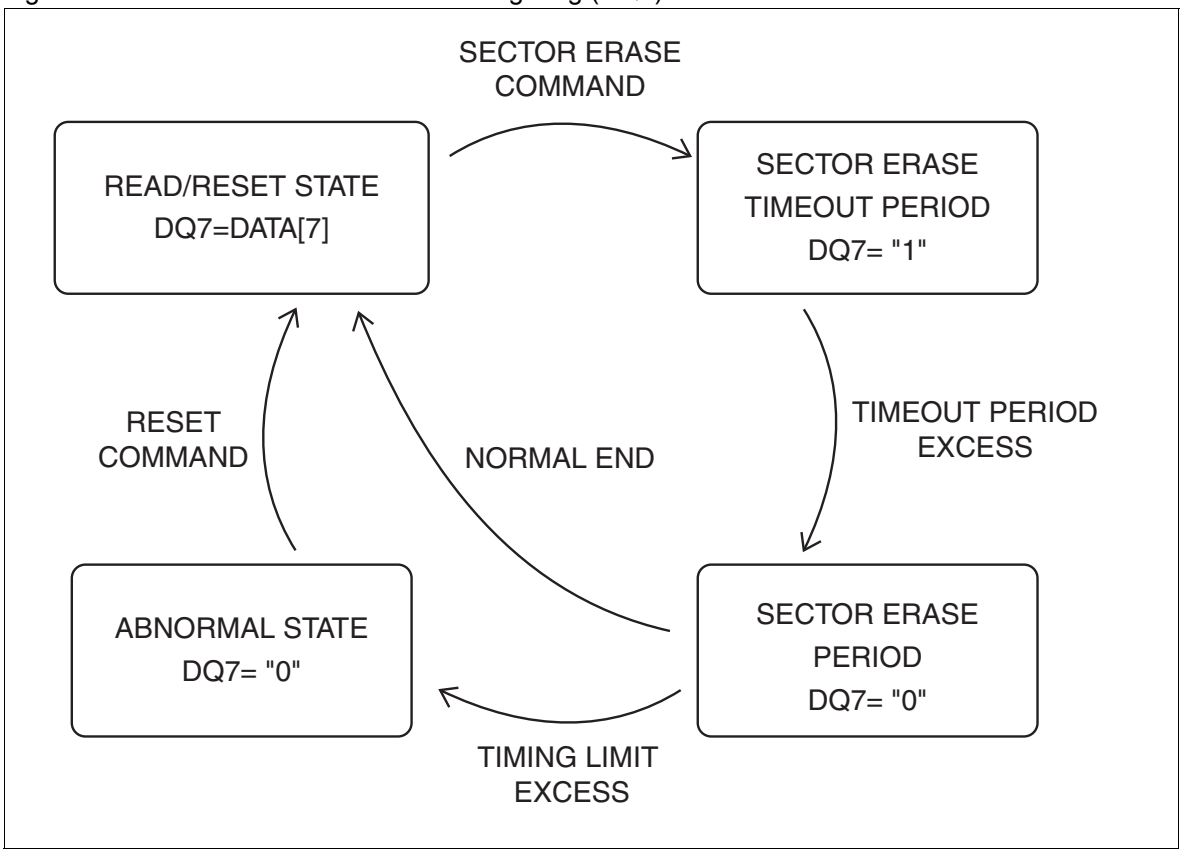
When the data polling flag (DQ7) is read during the execution of the automatic algorithm, its read value is "0". The read address is any address in the flash memory area.

When the flag is read after the completion of the automatic algorithm, the read value is "1". The flash memory returns to the read/reset state. After the completion of the automatic algorithm, "1" is actually read as the erased data from the flash memory.

1.6.2.3 *Sector Erase Operation*

The data polling flag (DQ7) can be read by making read access to the sector to be erased in the flash memory area during the execution of the automatic algorithm for sector erase operations. Figure 1-10 shows the state transition of the data polling flag (DQ7) at the sector erase.

Figure 1-10. State Transition of Data Polling Flag (DQ7) at Sector Erase



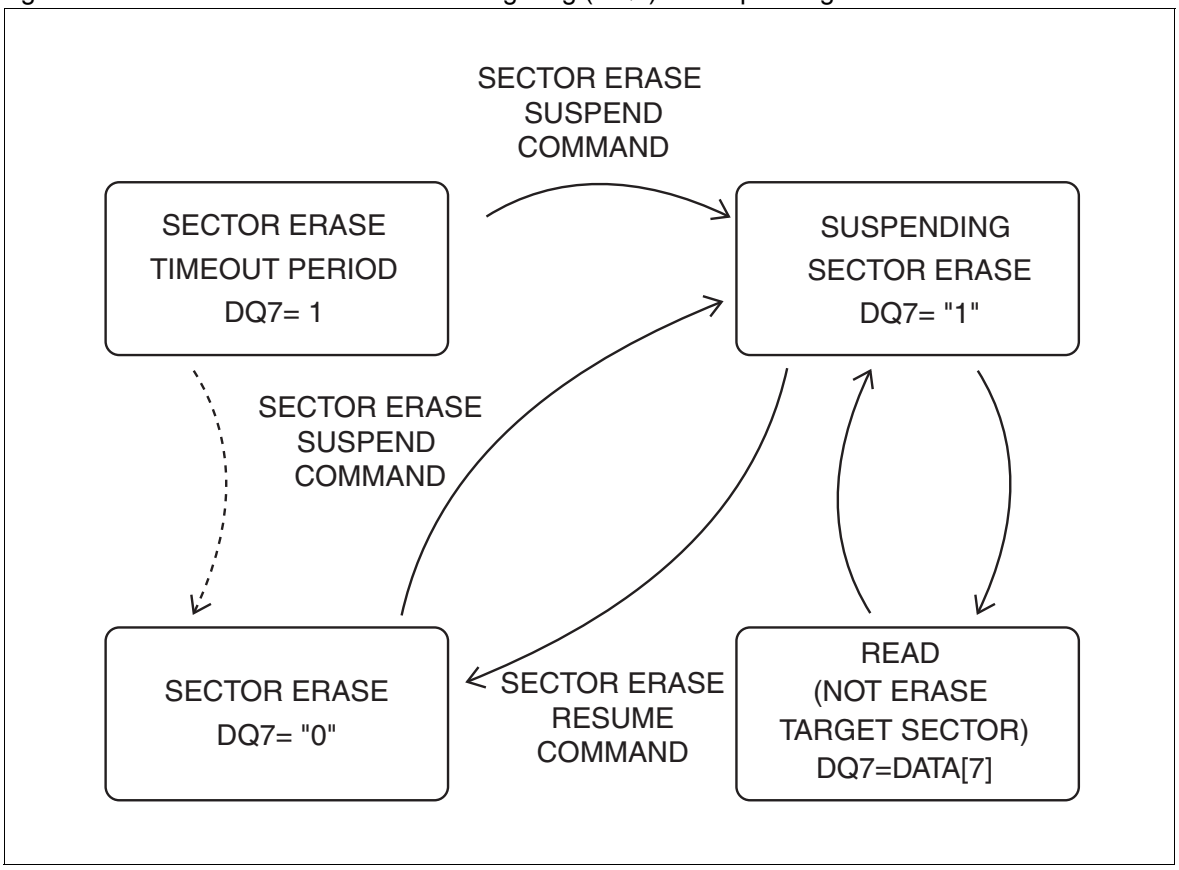
The data polling flag (DQ7) can be read by making read access to the sector to be erased during the execution of the automatic algorithm. In this series, the read value of the data polling flag (DQ7) is set to "1" when the sector erase command is issued. Then, after the sector erase timeout period is reached, the read value is changed to "0". Once the sector erase timeout period is reached, the read value is "0" during the execution of the automatic algorithm.

When the flag is read after the completion of the automatic algorithm, the read value is "1". The flash memory returns to the read/reset state. After the completion of the automatic algorithm, "1" is actually read as the erased data from the flash memory.

1.6.2.4 *Sector Erase Suspend Operation*

The data polling flag (DQ7) can be read by making read access to the sector to be erased in the flash memory area during the suspension of a sector erase operation. Figure 1-11 shows the state transition of the data polling flag (DQ7) at the suspending sector erase.

Figure 1-11. State Transition of Data Polling Flag (DQ7) at Suspending Sector Erase



When the data polling flag (DQ7) is read during the suspension of a sector erase operation, its read value is "1". The read address is the address of the sector to be erased in the flash memory area. When the sector erase operation is resumed, the read value of the data polling flag (DQ7) is changed to "0".

If a sector that is not to be erased is read during the suspension of a sector erase operation, the read value is bit 7 of the data at that address. The data written in the flash memory is read as normal read data.

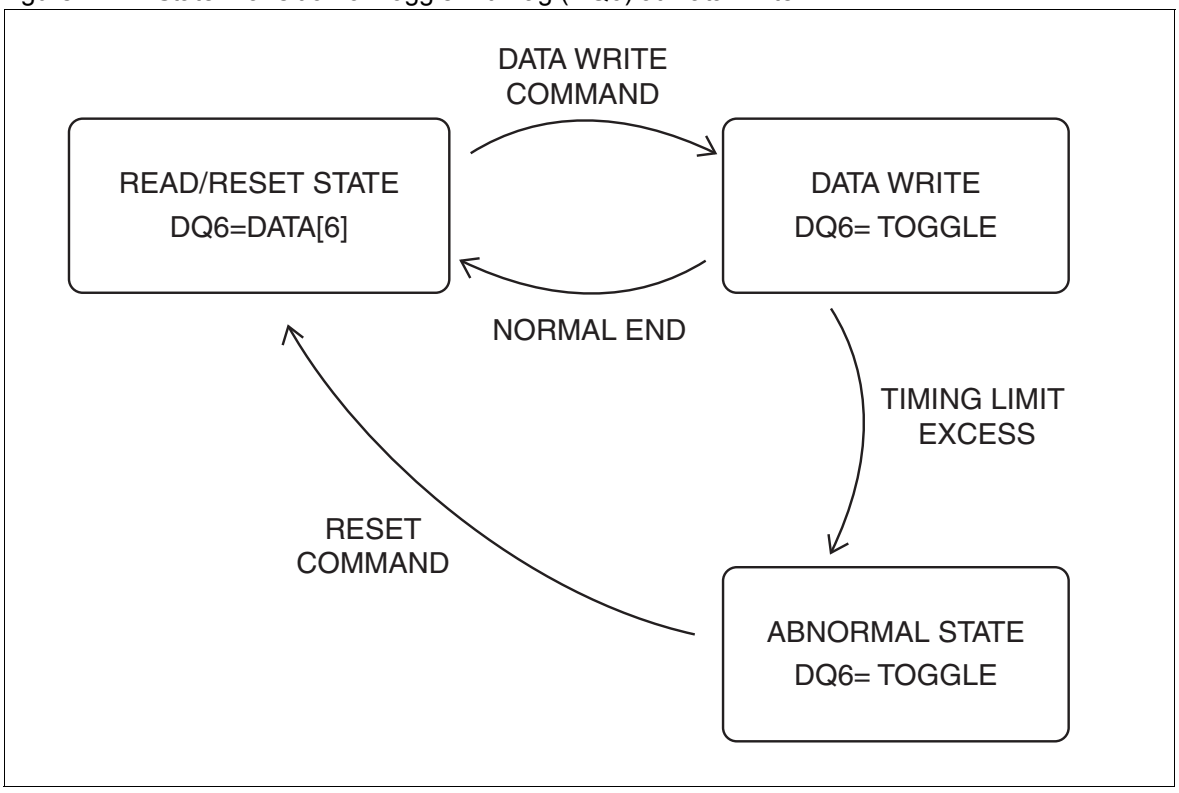
1.6.3 Toggle Bit Flag (DQ6)

The toggle bit flag (DQ6) indicates, through its toggle operation, that the automatic algorithm is currently being executed.

1.6.3.1 Data Write Operation

The toggle bit flag (DQ6) can be read by making read access to the flash memory area during the execution of the automatic algorithm for data-write operation. Figure 1-12 shows the state transition of the toggle bit flag (DQ6) at the data write.

Figure 1-12. State Transition of Toggle Bit Flag (DQ6) at Data Write



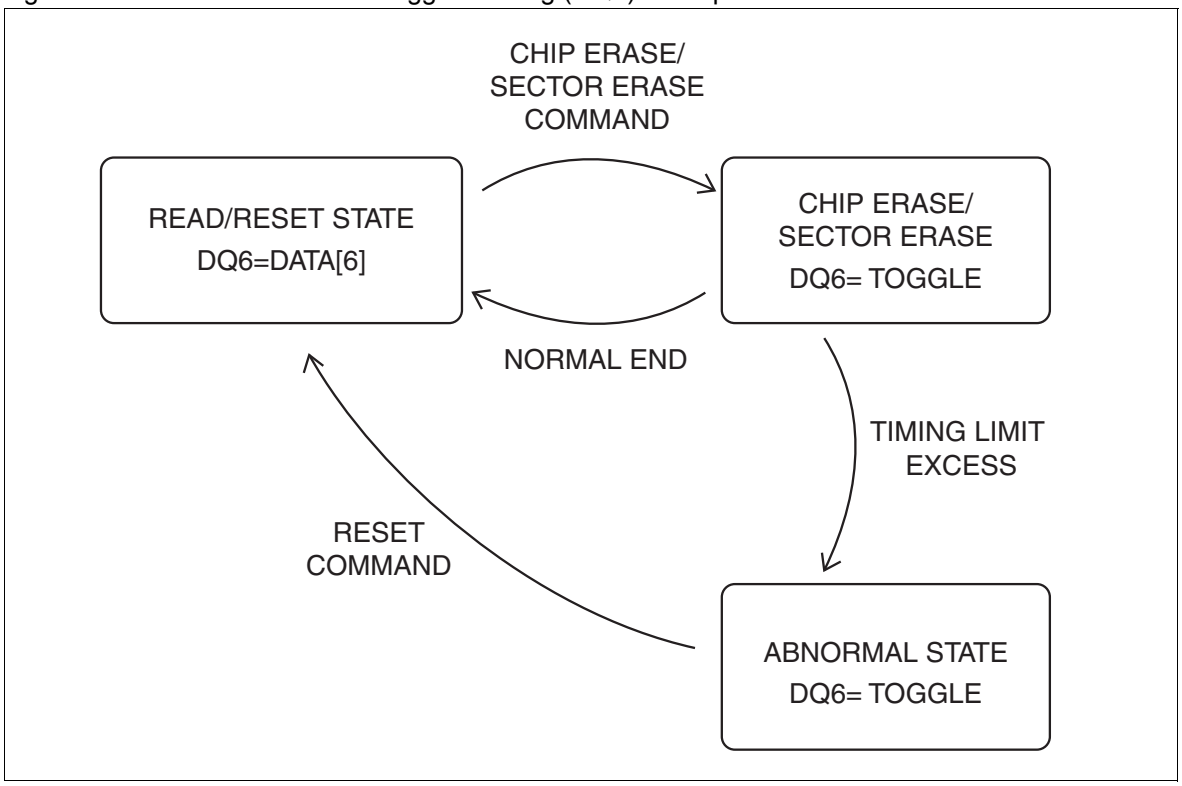
The toggle bit flag (DQ6) performs a toggle operation through which it indicates "1" and "0" alternatively every time it is read during the execution of the automatic algorithm. The read address is any address in the flash memory area.

When the flag is read after the completion of the automatic algorithm, its read value is bit 6 of the data at that address. The flash memory returns to the read/reset state. The data written in the flash memory is read as normal read data.

1.6.3.2 *Chipt Erase/Sector Erase Operations*

The toggle bit flag (DQ6) can be read by making read access to the sector that is to be erased in the flash memory area during the execution of the automatic algorithm for a chip erase or sector erase operation. Figure 1-13 shows the state transition of the toggle bit flag (DQ6) at the chip erase/sector erase.

Figure 1-13. State Transition of Toggle Bit Flag (DQ6) at Chip Erase/Sector Erase



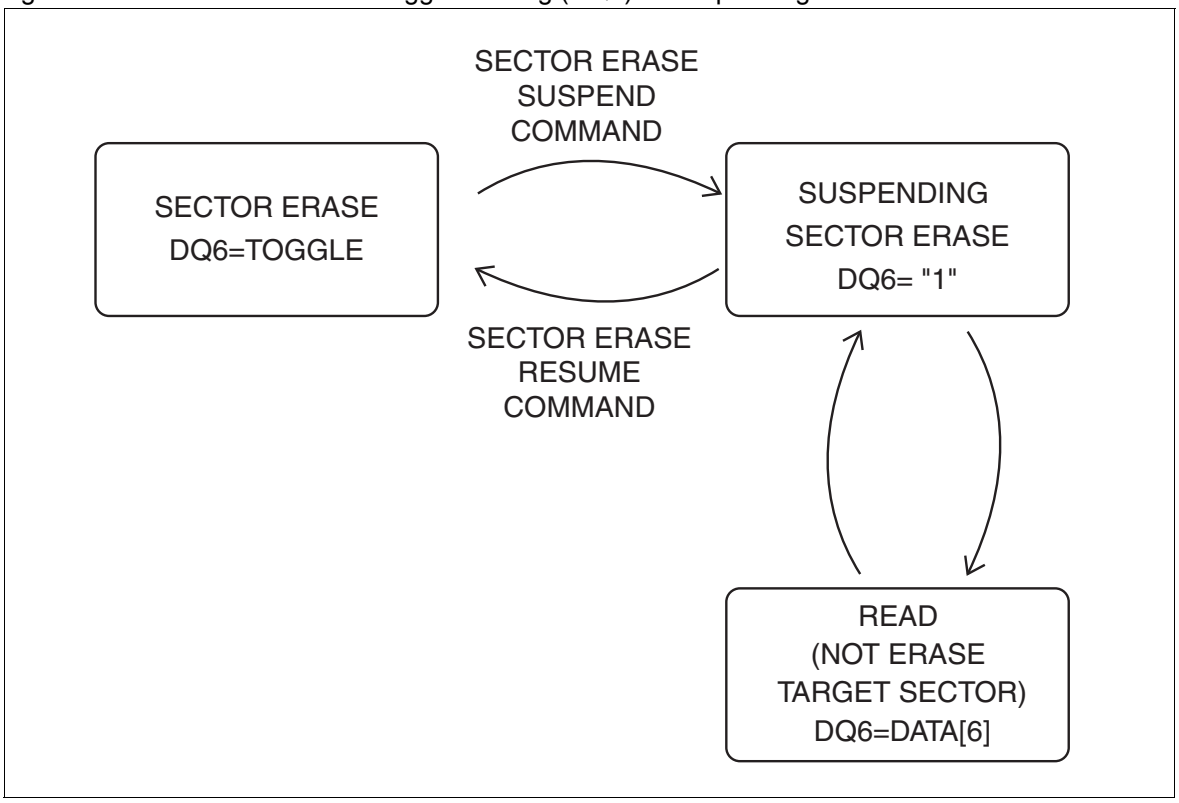
The toggle bit flag (DQ6) performs a toggle operation through which it indicates "1" and "0" alternatively every time it is read during the execution of the automatic algorithm. The read address for the chip erase operation is any address in the flash memory area. The read address for the sector erase operation is the address of the sector to be erased in the flash memory area.

When the flag is read after the completion of the automatic algorithm, the read value is "1". The flash memory returns to the read/reset state. After the completion of the automatic algorithm, "1" is actually read as the erased data from the flash memory.

1.6.3.3 *Sector Erase Suspend Operation*

The toggle bit flag (DQ6) can be read by making read access to the sector that is to be erased in the flash memory area during the suspension of a sector erase operation. Figure 1-14 shows the state transition of the toggle bit flag (DQ6) at the suspending sector erase.

Figure 1-14. State Transition of Toggle Bit Flag (DQ6) at Suspending Sector Erase



When the toggle bit flag (DQ6) is read during the suspension of a sector erase operation, its read value is "1". The read address is the address of the sector to be erased in the flash memory area. When the sector erase operation is resumed, the read value of the toggle bit flag (DQ6) performs a toggle operation.

When a sector that is not to be erased is read during the suspension of a sector erase operation, the read value is bit 6 of the data at that address. The data written in the flash memory is read as normal read data.

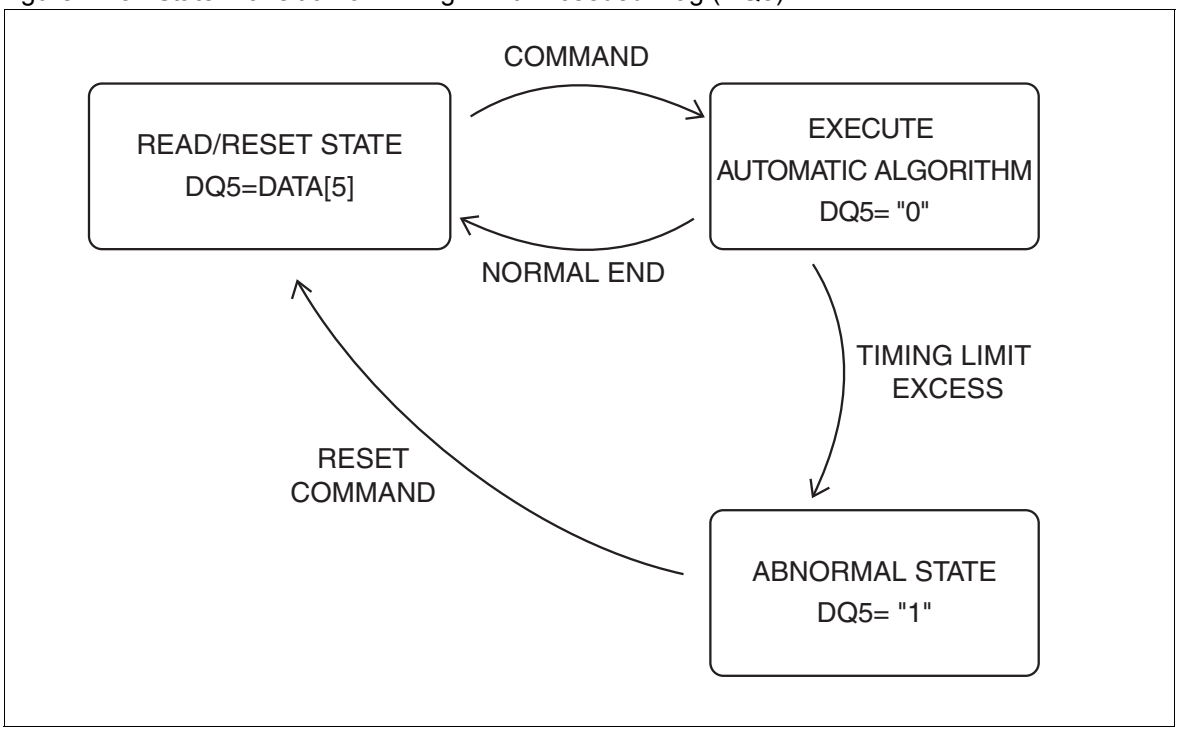
1.6.4 Timing Limit Exceeded Flag (DQ5)

The timing limit exceeded flag (DQ5) indicates that the execution of the automatic algorithm has exceeded the time specified within the flash memory.

1.6.4.1 Data Write/Chip Erase/Sector Erase Operations

The timing limit exceeded flag (DQ5) can be read by making read access to the flash memory area during the execution of the automatic algorithm. Figure 1-15. shows the state transition of the timing limit exceeded flag (DQ5).

Figure 1-15. State Transition of Timing Limit Exceeded Flag (DQ5)



If the specified time (required for the Data Write/Erase operation) has not yet been reached when the flag is read during the execution of the automatic algorithm, the read value is "0". If the specified time has already been exceeded, the read value is "1".

If the data polling flag (DQ7) or the toggle bit flag (DQ6) indicates that the automatic algorithm is currently being executed when the timing limit exceeded flag (DQ5) becomes "1", the Data Write/Erase operation can be determined as unsuccessful. In such cases, issue the reset command to the flash memory.

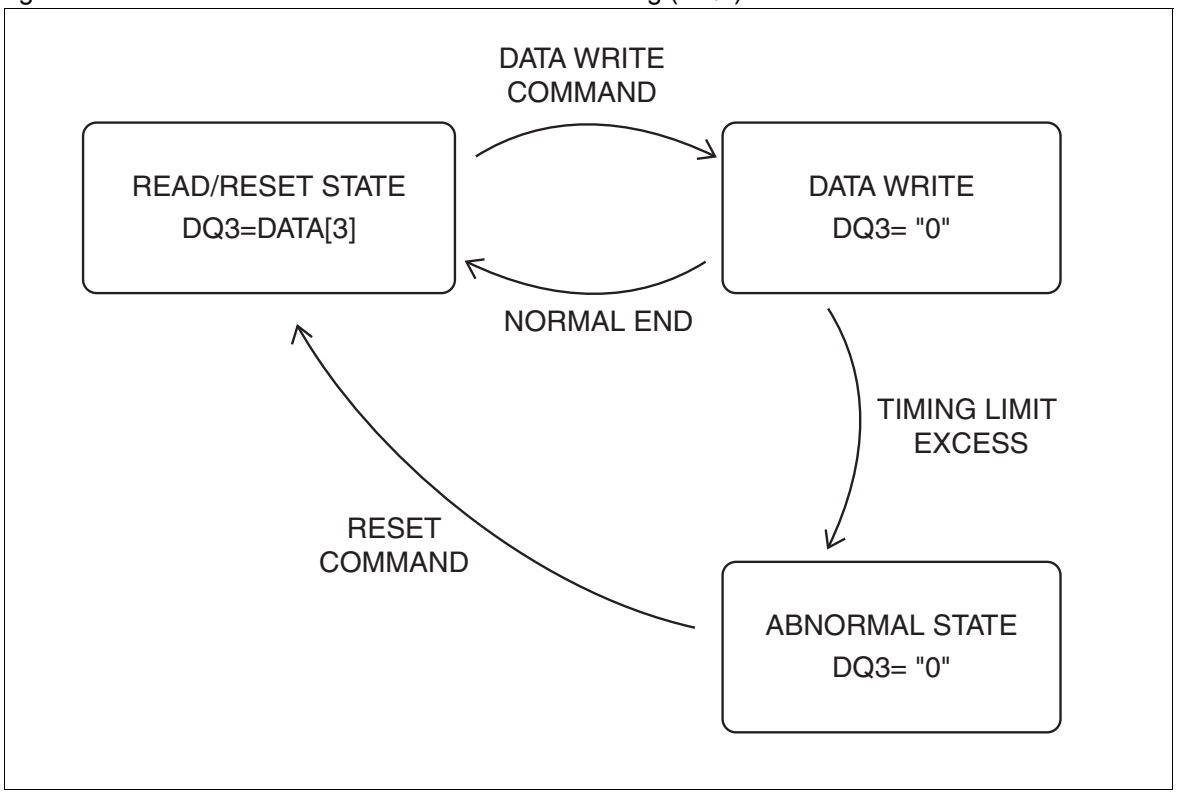
1.6.5 Sector Erase Timer Flag (DQ3)

The sector erase timer flag (DQ3) indicates the end of the sector erase time-out period.

1.6.5.1 Data Write Operation

The sector erase timer flag (DQ3) can be read by making read access to the flash memory area during the execution of the automatic algorithm for data-write operation. Figure 1-16 shows the state transition of the sector erase timer flag (DQ3) at the data write.

Figure 1-16. State Transition of Sector Erase Timer Flag (DQ3) at Data Write



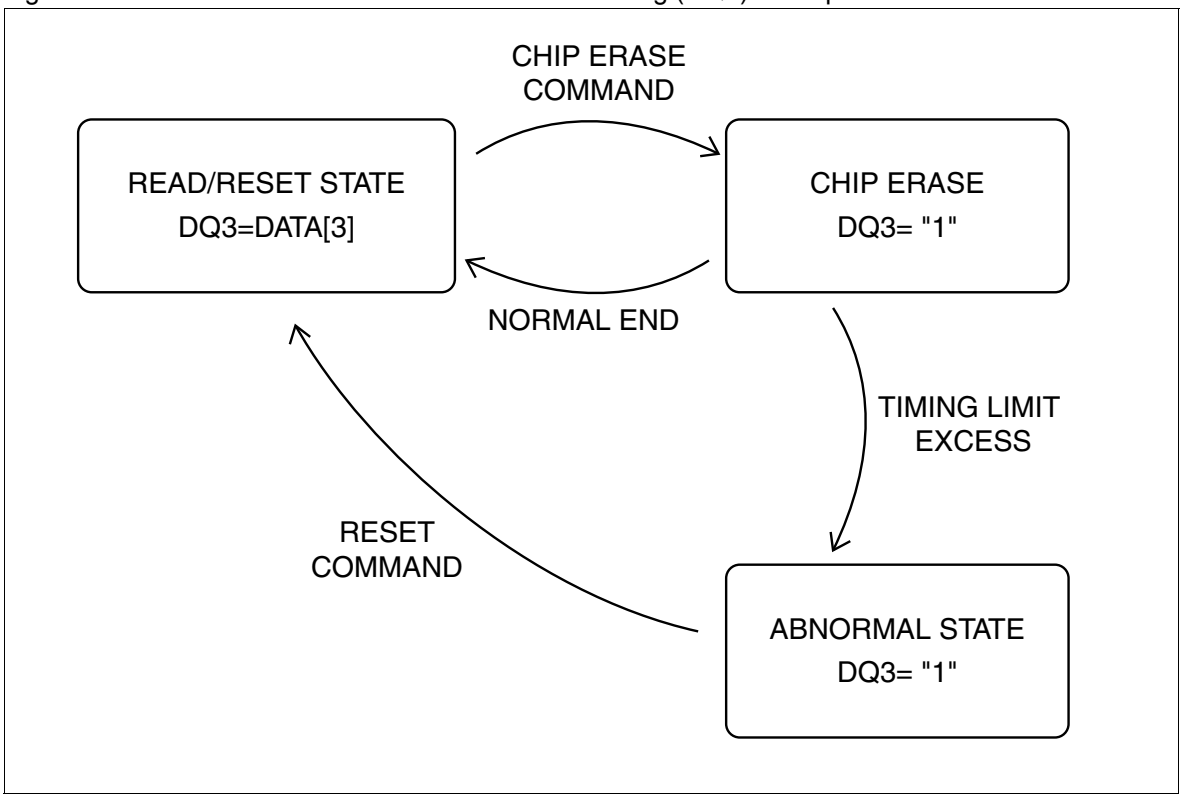
When the sector erase timer flag (DQ3) is read during the execution of the automatic algorithm, its read value is "0". The read address is any address in the flash memory area.

When the flag is read after the completion of the automatic algorithm, the read value is bit 3 of the data at that address. The flash memory returns to the read/reset state. The data written in the flash memory is read as normal read data.

1.6.5.2 *Chip Erase Operation*

The sector erase timer flag (DQ3) can be read by making read access to the flash memory area during the execution of the automatic algorithm for chip erase operations. Figure 1-17 shows the state transition of the sector erase timer flag (DQ3) at the chip erase.

Figure 1-17. State Transition of Sector Erase Timer Flag (DQ3) at Chip Erase



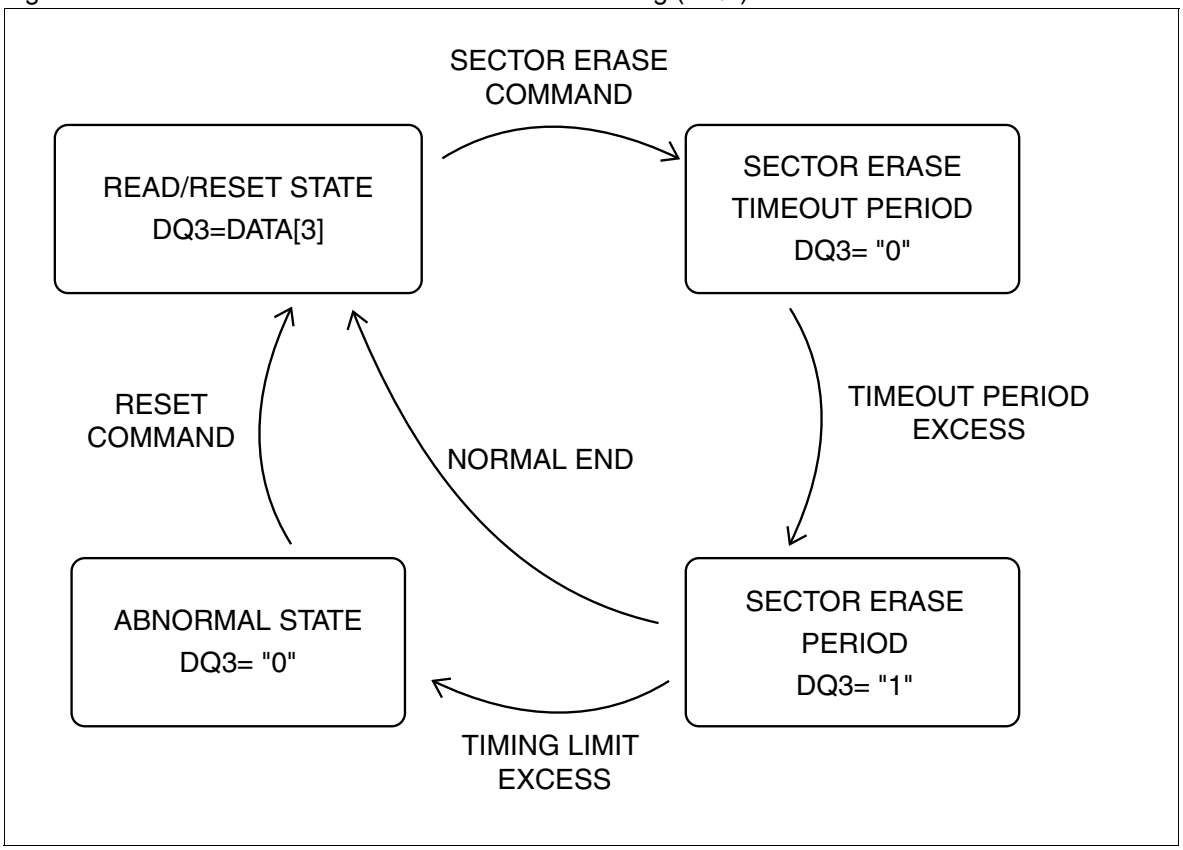
When the sector erase timer flag (DQ3) is read during the execution of the automatic algorithm, its read value is "1". The read address is any address in the flash memory area.

When the flag is read after the completion of the automatic algorithm, the read value is "1". The flash memory returns to the read/reset state. The data erased from the flash memory is read as normal read data.

1.6.5.3 *Sector Erase Operation*

The sector erase timer flag (DQ3) can be read by making read access to the flash memory area during the execution of the automatic algorithm for sector erase operation. Figure 1-18 shows the state transition of the sector erase timer flag (DQ3) at the sector erase.

Figure 1-18. State Transition of Sector Erase Timer Flag (DQ3) at Sector Erase



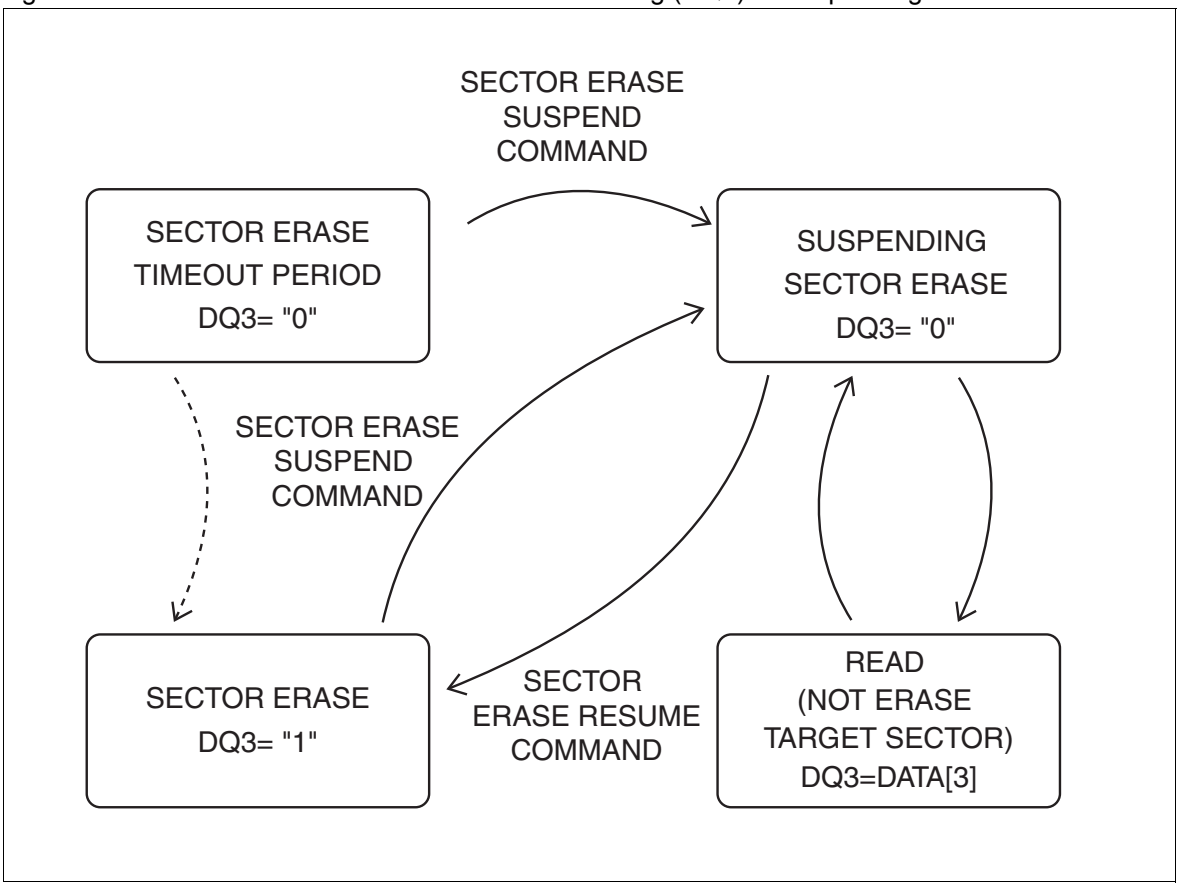
When the sector erase command is issued, the read value of the sector erase timer flag (DQ3) is set to "0". After that, when the sector erase timeout period is reached, the read value is changed to "1". After the sector erase timeout period is reached, the read value is "1" during the execution of the automatic algorithm.

When the flag is read after the completion of the automatic algorithm, the read value is "1". The flash memory returns to the read/reset state. The data erased from the flash memory is read as normal read data.

1.6.5.4 *Sector Erase Suspend Operation*

The sector erase timer flag (DQ3) can be read by making read access to the sector that is to be erased in the flash memory area during the suspension of a sector erase operation. Figure 1-19 shows the state transition of the sector erase timer flag (DQ3) at the suspending sector erase.

Figure 1-19. State Transition of Sector Erase Timer Flag (DQ3) at Suspending Sector Erase



When the sector erase timer flag (DQ3) is read during the suspension of a sector erase operation, its read value is "0". The read address is the address of the sector to be erased in the flash memory area. When the sector erase operation is resumed, the read value of the sector erase timer flag (DQ3) is changed to "1".

When the sector that is not to be erased is read during the suspension of a sector erase operation, the read value is bit 3 of the data at that address. The data written in the flash memory is read as normal read data.

1.7 Explanation of Operations

This section explains the operations of the flash memory and how to use them.

1.7.1 Read Operation

Data can be read from the flash memory, when it is in the read/reset state. No command needs to be issued for the read operation. Just do a read access to read out a data from flash memory.

The flash memory goes to the read/reset state when the power is turned on, the MCU is reset, the automatic algorithm is completed, or the reset command is issued.

1.7.2 Resetting Flash Memory

The flash memory goes to the read/reset state, when the reset command is issued to the flash memory.

If the timing limit exceeded flag (DQ5) indicates "1" because the Data Write/Erase operation has not been completed within a specified time, it can be determined that an error has occurred. In such cases, issue the reset command to the flash memory to put it back to the read/reset state.

1.7.3 Writing Data

A word data can be written by issuing the data write command to the flash memory.

1.7.3.1 Writing Data

The unit used for writing data is by word. Each time the data write command is issued, one word is written. There is no restriction on the order of address where data is written. Data can also be written to a different sector of the flash memory by changing the sector.

The flash memory can change a bit value from "1" to "0" or keep a bit value, through data write operations. However, bit value "0" cannot be changed to "1". Written data can be overwritten. Table 1-17 shows the example of writable bit patterns at data write.

Table 1-17. Examples of Writable Bit Pattern at Data Write

Old data	Write data
1111111111111111_B	0000000000000000_B
1111111111111111_B	1111111111111111_B
1111111111111010_B	1010111111111010_B
0000000000010000_B	0000000000000000_B

Old data	Write data
1111111111000000_B	1111111110000000_B
1111111110000000_B	1111101000000000_B
1100101010101100_B	0100101010101100_B
1111111111111111_B	1111111111101111_B

1.7.3.2 Write Protection

The data-write operation is only possible to a write enabled sector of the flash memory.

1.7.3.3 Procedure for Writing Data

Issue the data write command when the flash memory is in the read/reset state. Once the data write command is issued, the flash memory performs the automatic algorithm to write data automatically.

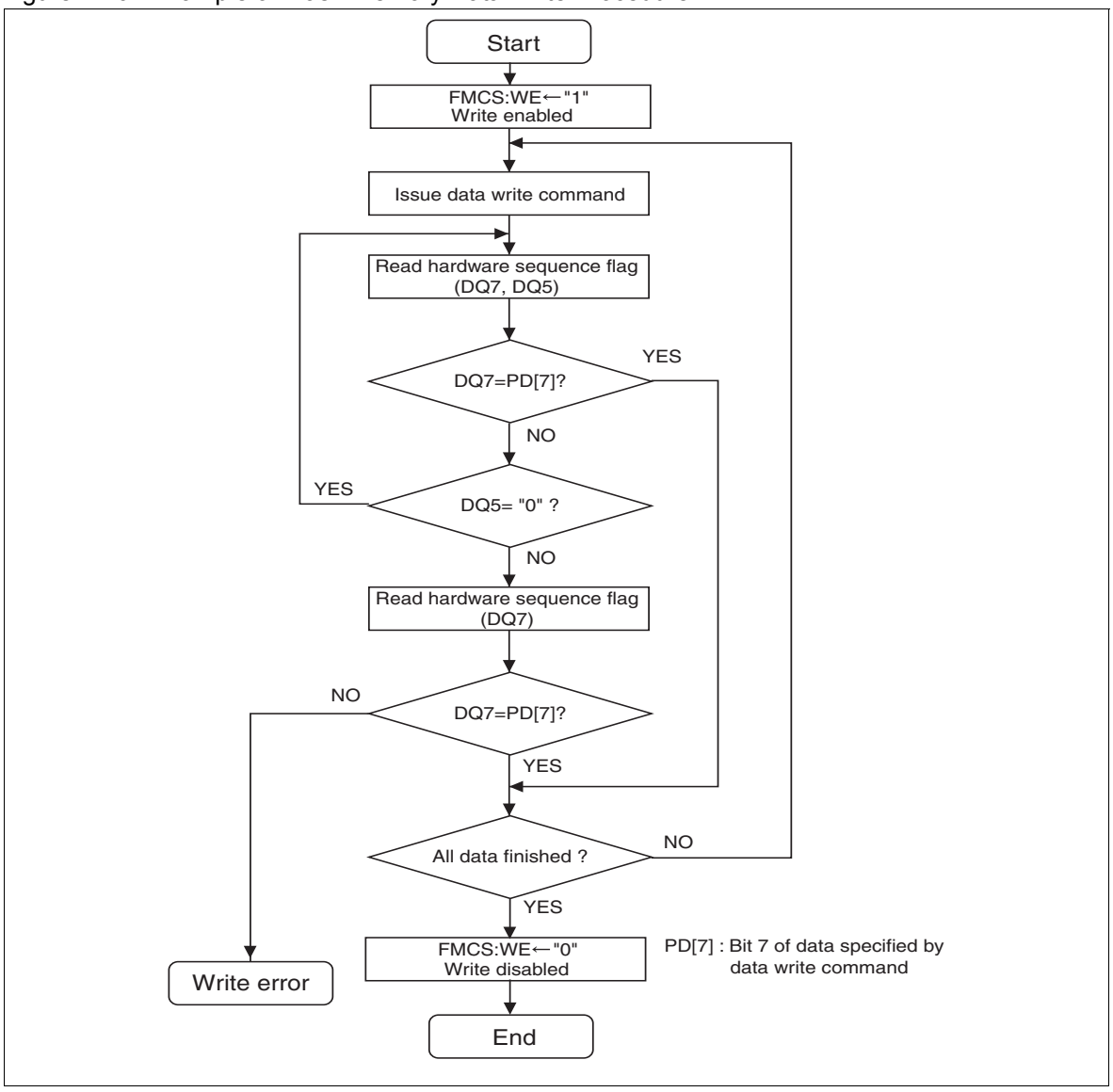
After issuing the data write command to the flash memory, read the hardware sequence flag to check if the automatic algorithm is completed. The data polling flag (DQ7) or the toggle bit flag (DQ6) can be used to confirm if the data write operation is completed.

The timing limit exceeded flag (DQ5) can be checked to detect an unsuccessful data write operation. The data polling flag (DQ7) may change almost at the same time as the timing limit exceeded flag (DQ5). Check the data polling flag (DQ7) again after the timing limit exceeded flag (DQ5) indicates "1".

Similarly, the toggle bit flag (DQ6) may also stop its toggle operation almost at the same time as the timing limit exceeded flag (DQ5). Check the toggle bit flag (DQ6) again after the timing limit exceeded flag (DQ5) indicates "1".

Figure 1-20 shows the example of the flash memory data write procedure using the data polling flag (DQ7).

Figure 1-20. Example of Flash Memory Data Write Procedure



1.7.4 Chip Erase Operation

The contents of all sectors can be erased by issuing the chip erase command to the flash memory.

1.7.5 Chip Erase Operation

The chip erase operation erases data from all of the sectors of the flash memory. When the contents of a sector are erased, all bits of the sector are set to "1".

1.7.5.1 Write Protection

The chip erase operation is enabled by writing the chip erase command sequence to a write enabled sector of the flash memory.

The chip erase operation cannot be performed from a sector that is not write enabled, even if the chip erase command sequence is written to the sector. Once the chip erase operation is performed from a write enabled sector, the contents of all of the sectors are erased including that is not write enabled.

1.7.5.2 Procedure for Chip Erase Operation

Issue the chip erase command when the flash memory is in the read/reset state. Once the chip erase command is issued, the flash memory performs the automatic algorithm to erase the contents of all sectors automatically.

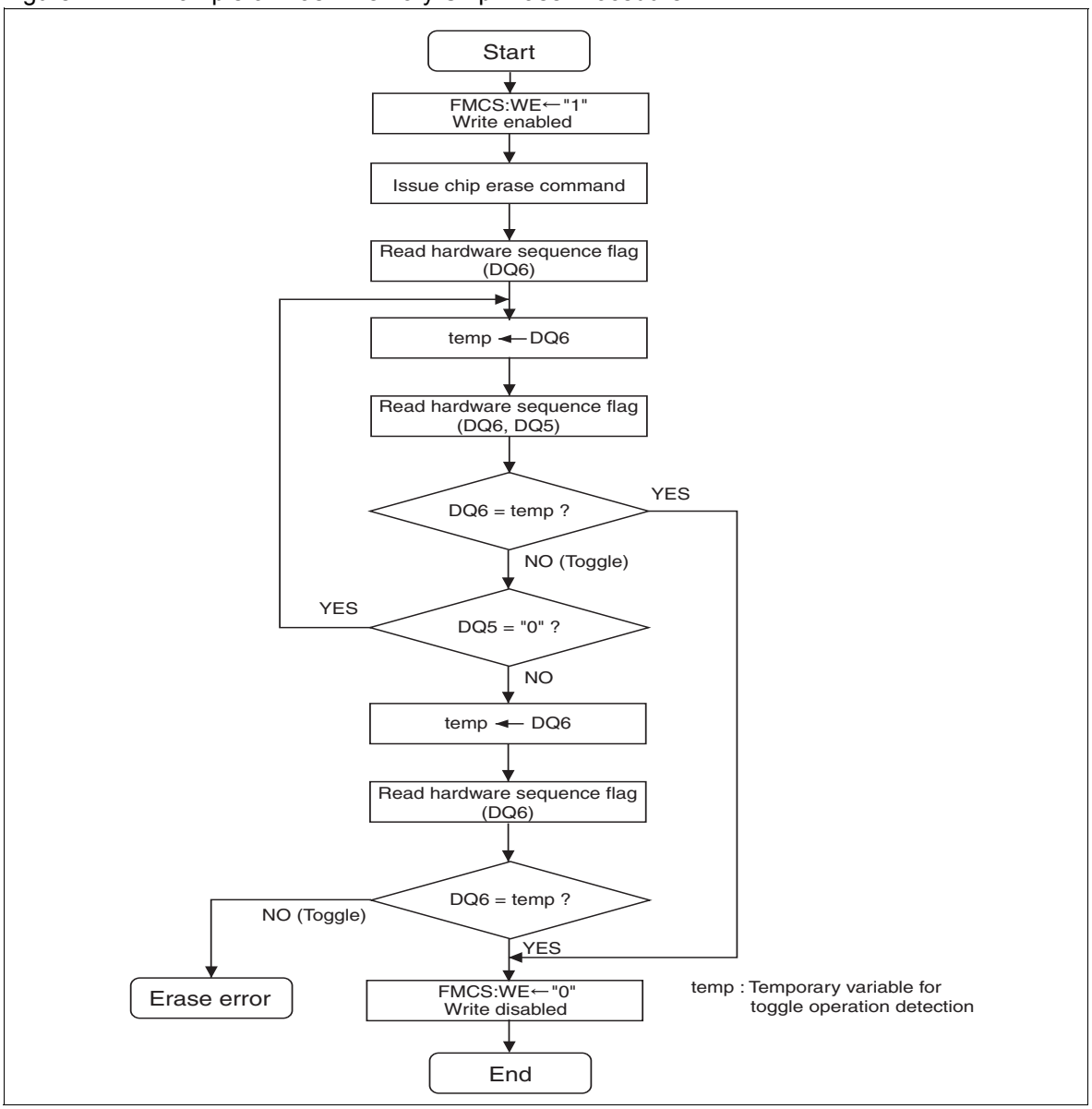
After issuing the chip erase command to the flash memory, read the hardware sequence flag to check if the automatic algorithm is completed. The data polling flag (DQ7) or the toggle bit flag (DQ6) can be used to confirm if the chip erase operation is completed.

The timing limit exceeded flag (DQ5) can be checked to detect an unsuccessful chip erase operation. The data polling flag (DQ7) may change almost at the same time as the timing limit exceeded flag (DQ5). Check the data polling flag (DQ7) again after the timing limit exceeded flag (DQ5) indicates "1".

Similarly, the toggle bit flag (DQ6) may also stop its toggle operation almost at the same time as the timing limit exceeded flag (DQ5). Check the toggle bit flag (DQ6) again after the timing limit exceeded flag (DQ5) indicates "1".

Figure 1-21 shows the example of the flash memory chip erase procedure using the toggle bit flag (DQ6).

Figure 1-21. Example of Flash Memory Chip Erase Procedure



1.7.6 Sector Erase Operation

The contents of a sector can be erased by issuing the sector erase command to the flash memory.

1.7.6.1 Sector Erase Operation

The sector erase operation erases the contents of specified sectors of the flash memory. One or more sectors can be specified. Once the contents of the specified sector(s) are erased, all bits of these sectors are set to "1".

1.7.6.2 Write Protection

The sector erase operation is enabled by writing the sector erase command sequence to a write enabled sector of the flash memory.

1.7.6.3 Procedure for Sector Erase Operation

Issue the sector erase command when the flash memory is in the read/reset state. Once the sector erase command is issued, the flash memory executes the automatic algorithm to erase the contents of the specified sector(s) automatically.

Once the sector erase command is issued, the flash memory starts the sector erase timeout period. The minimum sector erase timeout period is 50 μs. When erasing the contents of multiple sectors, specify such sectors by writing the sector erase code within the sector erase timeout period. Write the sector erase code to the sectors whose contents are to be erased.

The sector erase timeout period can be checked by the sector erase timer flag (DQ3) that is one of the hardware sequence flags. When specifying multiple sectors, make sure that the sector erase timer flag (DQ3) is "0" every time after writing an additional sector erase code. If the sector erase timer flag (DQ3) is "1", the last sector erase code may not have been written within the sector erase timeout period.

If the sector erase timer flag (DQ3) changes to "1" while specifying a sector whose contents are to be erased, stop the process of specifying sectors. Reissue the sector erase command later for sectors including the last specified sector, after the automatic algorithm is completed.

After issuing the sector erase command and the sector erase code to the flash memory, read the hardware sequence flag to check if the automatic algorithm is completed. The data polling flag (DQ7) or the toggle bit flag (DQ6) can be used to confirm if the sector erase operation is completed.

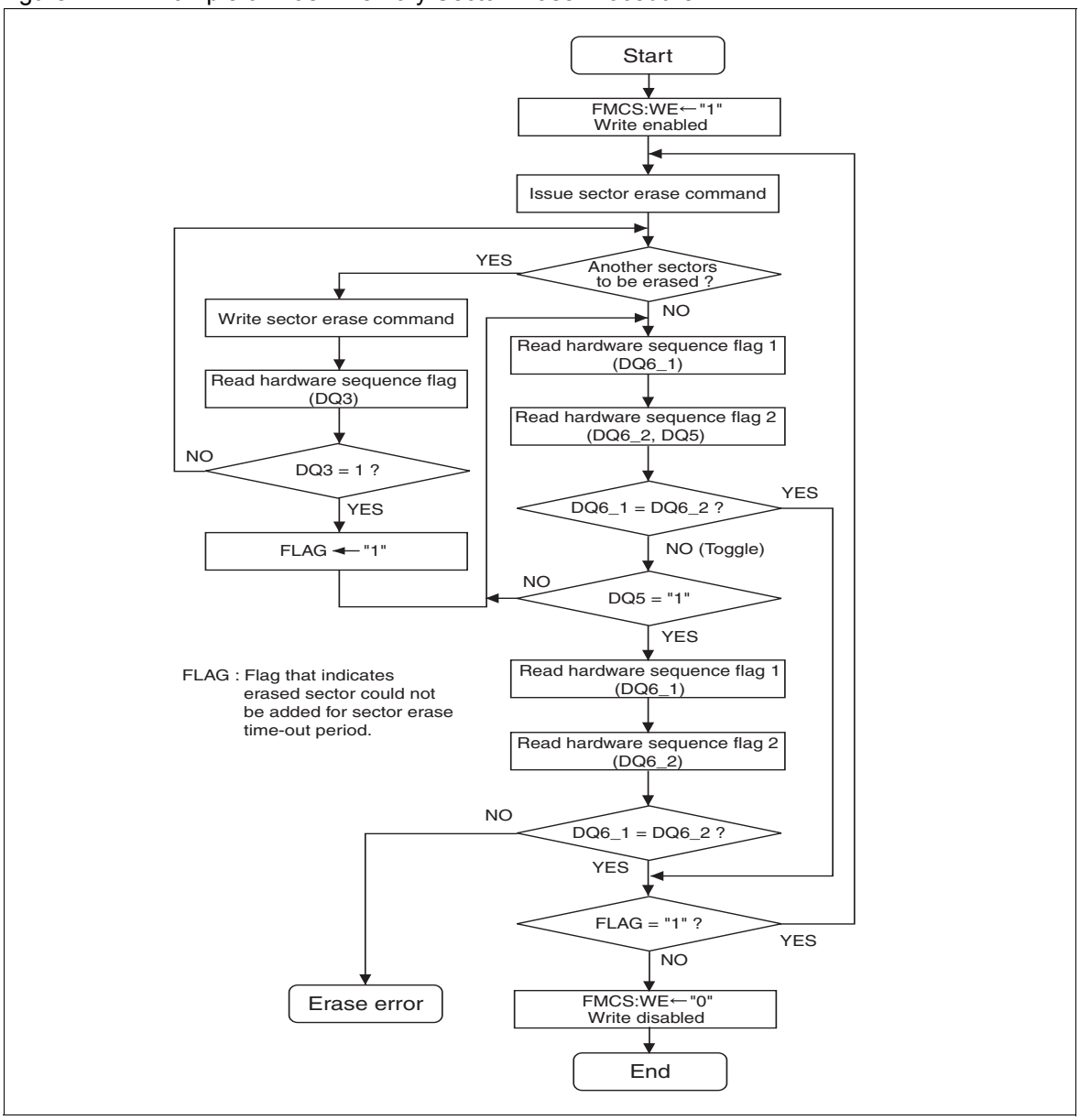
In this series, the data polling flag (DQ7) becomes "1", when the sector erase command is issued. After that, it changes to "0", when the sector erase timeout period is reached. And once the automatic algorithm is completed, it changes to "1". To confirm that the sector erase operation is completed, check that the data polling flag (DQ7) has changed to "1" → "0" → "1". Or, check that the data polling flag (DQ7) has changed from "0" to "1", after the sector erase timer flag (DQ3) became "1".

The timing limit exceeded flag (DQ5) can be checked to detect an unsuccessful sector erase operation. The data polling flag (DQ7) may change almost at the same time as the timing limit exceeded flag (DQ5). Check the data polling flag (DQ7) again after the timing limit exceeded flag (DQ5) indicates "1".

Similarly, the toggle bit flag (DQ6) may also stop its toggle operation almost at the same time as the timing limit exceeded flag (DQ5). Check the toggle bit flag (DQ6) again after the timing limit exceeded flag (DQ5) indicates "1".

Figure 1-22 shows the example of the flash memory sector erase procedure using the toggle bit flag (DQ6).

Figure 1-22. Example of Flash Memory Sector Erase Procedure



1.7.7 Sector Erase Suspend Operation

A sector erase operation can be suspended by issuing the sector erase suspend command to the flash memory during the sector erase operation.

1.7.7.1 Sector Erase Suspend Operation

During the suspension of a sector erase operation, data can be read from sectors other than erase target sectors.

1.7.7.2 Procedure for Sector Erase Suspend Operation

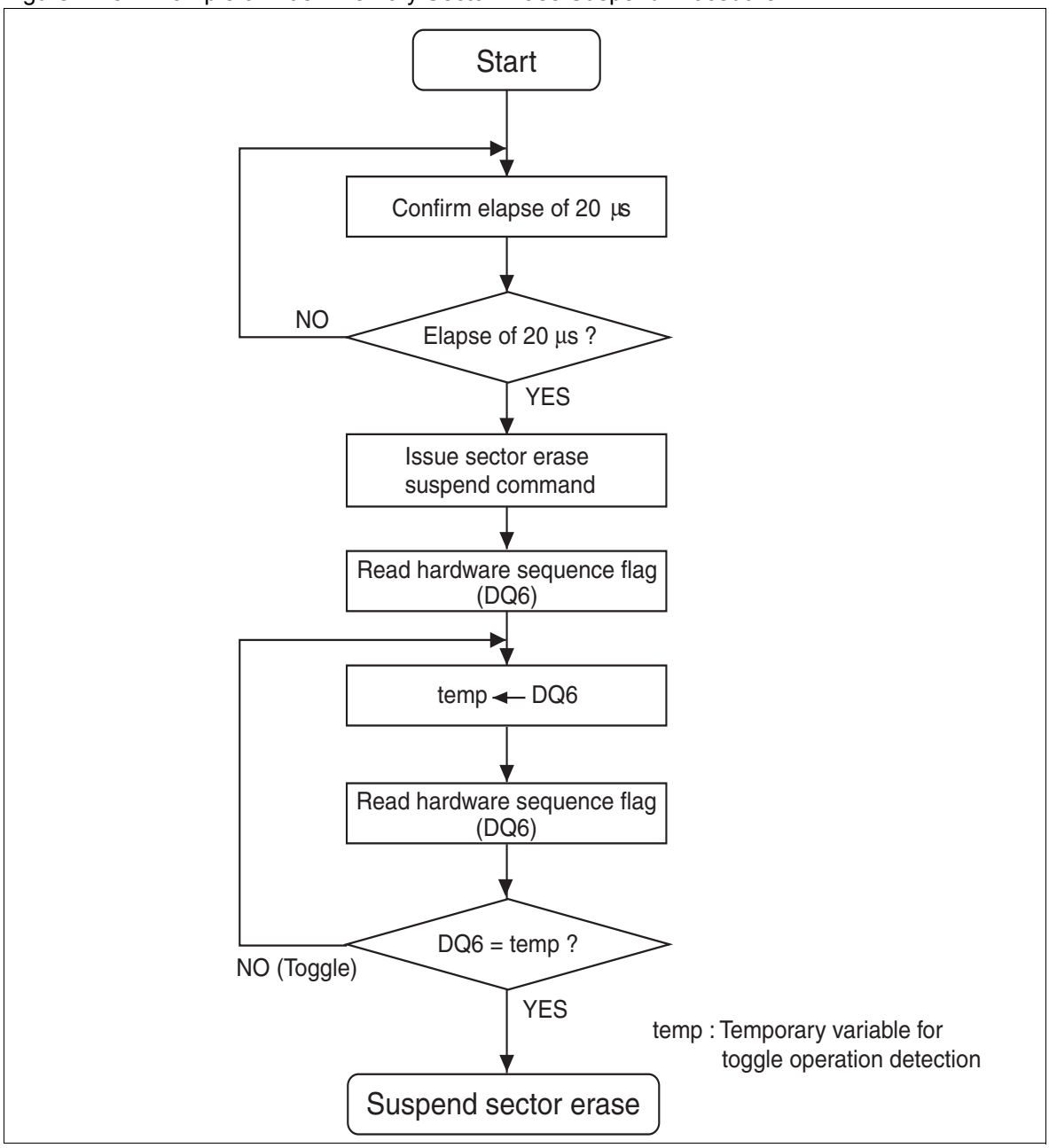
The sector erase suspend command is valid only during the execution of the automatic algorithm for sector erase operations, including the sector erase timeout period. If the sector erase suspend command is issued during the sector erase timeout period, the sector erase timeout period is terminated immediately in order to suspend the sector erase operation.

When the sector erase suspend command is issued during a sector erase operation after the sector erase timeout period is reached, it takes up to 20 μs for the sector erase operation to be suspended. Before issuing the sector erase suspend command, wait for 20μs or more to elapse after the sector erase command or the sector erase resume command is issued.

The hardware sequence flag can be read by read access from erase target sectors, during the suspension of a sector erase operation. During the suspension of the sector erase operation, the read value of the data polling flag (DQ7) is "1", and the read value of the toggle bit flag (DQ6) is also "1". After issuing the sector erase suspend command, make sure that the sector erase operation has been suspended.

Figure 1-23 shows the example of the flash memory suspending sector erase procedure using the toggle bit flag (DQ6).

Figure 1-23. Example of Flash Memory Sector Erase Suspend Procedure



1.7.8 Sector Erase Resume Operation

A sector erase operation can be resumed by issuing the sector erase resume command to the flash memory during the suspension of the sector erase operation.

1.7.8.1 Sector Erase Resume Operation

Once the sector erase operation is resumed, the automatic algorithm for sector erase operations restarts its execution.

1.7.8.2 Procedure for Resuming Sector Erase Operation

Issue the sector erase resume command when the sector erase operation is being suspended. The flash memory resumes the automatic algorithm for sector erase operations to erase the contents of the remaining sectors automatically.

After issuing the sector erase resume command to the flash memory, read the hardware sequence flag to check if the automatic algorithm for sector erase operations has been resumed and completed. The procedure to confirm the completion of the sector erase operation is the same as described in "1.7.6 Sector Erase Operation".

1.8 Flash Memory Mode

When flash memory mode is set, the built-in flash memory can be controlled via external pins. The flash memory mode is used to perform Data Write/Erase operations using a parallel flash programmer.

1.8.1 Setting Flash Memory Mode

The device is switched to the flash memory mode when the signal level of the mode setting pins (MD2 to MD0) is set and the MCU is rebooted. Table 1-18 shows the setting of the mode setting pins for the flash memory mode.

Table 1-18. Setting of Mode Setting Pins for Flash Memory Mode

Mode Setting Pins	Signal level	Mode
MD2	1 (high)	Flash Memory Mode
MD1	1 (high)	
MD0	1 (high)	

1.8.1.1 Correspondence between Flash Memory Mode Control Signal and External Pin

In flash memory mode, the MCU functions stop. The built-in flash memory is associated with external pins via which the built-in flash memory can be controlled. The automatic algorithm of the flash memory is activated via the external pins in order to Data Write/Erase operation. The flash memory interface circuit is connected to ports.

1.8.1.2 Sector Configuration for Flash Memory Mode

The sector configuration for the flash memory mode is different from the sector configuration seen from CPU. The address of the sector of the flash memory mode is called "writer address". Table 1-19 shows the sector configuration in flash memory mode.

Table 1-19. Sector Configuration in Flash Memory Mode

Address range (Writer address)	Sector	CPU address
$FFFFF_H$ to $FE000_H$	SA5 (8 Kbytes)	$FF:FFFF_H$ to $FF:E000_H$
$FDFFF_H$ to $FC000_H$	SA4 (8 Kbytes)	$FF:DFFF_H$ to $FF:C000_H$
$FBFFF_H$ to $F0000_H$	SA3 (48 Kbytes)	$FF:BFFF_H$ to $FF:0000_H$
$EFFFF_H$ to $E4000_H$	SA2 (48 Kbytes)	$FE:FFFF_H$ to $FE:4000_H$
$E3FFF_H$ to $E2000_H$	SA1 (8 Kbytes)	$FE:3FFF_H$ to $FE:2000_H$
$E1FFF_H$ to $E0000_H$	SA0 (8 Kbytes)	$FE:1FFF_H$ to $FE:0000_H$

1.9 Flash Security

The content of the flash memory can be protected by flash security.

1.9.1 Flash Security

When the protection code is written to the security bit of the flash memory, access to the flash memory is restricted to protect the content of the flash memory. Table 1-20 shows the address of the security bit and the protection code.

Table 1-20. Address of Security Bit and Protection Code

Product	Flash memory size	Address of security bit	Protection code
MB90F931 MB90F931S	1 M bits	FE: 0001_H	01_H

Setting Flash Security

Write the protection code to the security bit. Security will be applied at an external reset or at power-on. Once the security is applied, the flash memory is protected. As the security is applied to the entire area of the flash memory. The security of each sector cannot be specified.

When the flash memory is protected, the invalid data is read via external pins. Data Write/Erase operation except chip erase can not be performed.

Set the protection code at the end of flash programming (a series of data write/erase process). This prevents unnecessary protection during the flash programming.

1.9.2 Canceling Flash Security

Execute chip erase operation. The security will be canceled at an external reset or at power-on.

Once the flash memory is protected, its protection will not be canceled until the chip erase operation is performed. And unless the protection is canceled, data cannot be read from flash memory, data write/erase operation cannot be performed via an external pin.

1.10 Notes

This section explains the notes of the flash memory.

1.10.1 Notes

1.10.1.1 Writing data to bits whose value is "0"

Bits whose value is "0" cannot be changed to "1" by writing data to them. If an attempt is made to write "1" to a bit to which "0" is written as its value, the flash memory is locked and the automatic algorithm does not complete. In rare cases, however, it may complete normally as if "1" has been written successfully.

When the flash memory is locked, the time limit is exceeded and the timing limit exceeded flag (DQ5) indicates "1". This state represents incorrect use of the flash memory, rather than a failure in the flash memory. If the timing limit exceeded flag (DQ5) indicates "1", issue the reset command to the flash memory.

1.10.1.2 Issuing a command to a sector that is not write enabled

Write a command sequence to write enabled sectors of the flash memory. Write the command sequence correctly. The flash memory may malfunction, if a command is issued to a sector that is not write enabled, data is written to an improper address or written in an incorrect order.

1.10.1.3 Chip erase operation

When sectors that are write enabled and sectors that are not write enabled coexist, the contents of all of the sectors, including the sectors that are not write enabled, will be erased, if the chip erase command is issued to a sector that is write enabled.

1.10.1.4 If a reset occurs during data write/erase operation

If a hardware reset or low-voltage detection reset occurs, the data write/erase operation sequence is initialized. The flash memory returns to read/reset state after the reset is released. The data being written/erased become indeterminate. Therefore, issue the command of data write/erase operation again.

It takes up to 20 μs for the state machine of the flash memory that has received a hardware reset or low-voltage detection reset to complete the reset and enable read operation. This applies to the case in which the flash memory is currently executing an automatic algorithm due to a command other than the reset command.

If a hardware reset or low-voltage detection reset occurs while the automatic algorithm is inactive, it takes up to 500ns to complete the resetting of the flash memory. And once the reset is released, it takes 200ns for read operation to be enabled.

If a software reset, watchdog timer reset or CPU operation detection reset occurs, the data write/erase operation sequence is not initialized. After the data write/erase operation sequence is completed, the flash memory returns to read/reset state.

1.10.1.5 Mode transition during data write/erase operation

Do not change to the sub clock mode or a standby mode (time-base timer mode, watch mode, stop mode) when the flash memory is enabled for write operation (FMCS:WE="1").

1.10.1.6 *Extended intelligent I/O service (EI^{2}OS)*

EI^{2}OS cannot be used to accept data write/erase interrupts issued from the flash memory to the CPU.

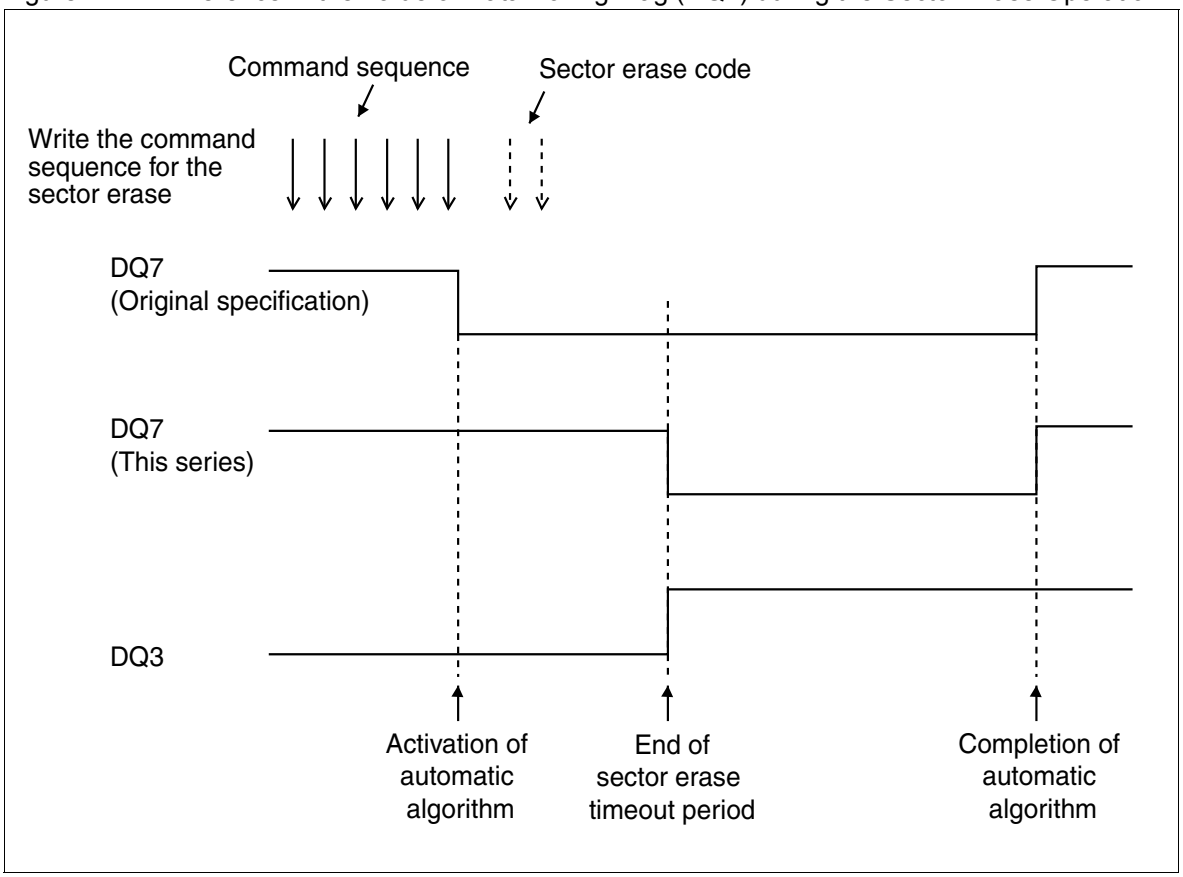
1.10.1.7 *Fault analysis of the flash memory when security is applied*

Be forewarned that fault analysis of the flash memory cannot be performed when security is applied.

1.10.1.8 *Restrictions on the data polling flag (DQ7) during the sector erase operation*

In this series, when the sector erase command is issued, the value of the data polling flag (DQ7) changes differently from the original value of the automatic algorithm. In the original specification, the flag indicates "0" when the sector erase command is issued, and it changes to "1" when the automatic algorithm is completed. In this series, however, the flag indicates "1" when the sector erase command is issued, it changes to "0" when the sector erase timeout period is reached, and then, it changes back to "1" when the automatic algorithm is completed. Figure 1-24 shows the difference in the value of the data polling flag (DQ7) during the sector erase operation.

Figure 1-24. Difference in the Value of Data Polling Flag (DQ7) during the Sector Erase Operation



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3. Major changes

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FOR MORE DETAILS PLEASE SEE THE DOCUMENT HISTORY TABLE

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