# Card Coil Design Guide

## Application Note

**Contactless memories compliant to ISO/IEC 14443-3 Type A**

**Document release reference: Z8F80907524-A**

## Devices

- my-d™ move
- my-d™ move NFC
- my-d™ move lean
- my-d™ move lean NFC
- NRG™ SLE 66R35I, NRG™ SLE 66R35R
- NRG™ SLE 66R35E7, NRG™ SLE 66R35E7H

## About this document

### Scope and purpose

This document serves as a guideline for the design of card coils for Infineon's contactless memory products compliant to ISO/IEC 14443-3 Type A. The recommendations given are for orientation only. The specific behavior of the coil design shall be verified by measurement as described within this document.

### Intended audience

The information within this document is intended for antenna designers and card manufacturers, who want to understand the theory behind card coil design and card coil characterization.

# Table of contents

**Devices** . . . 1
**About this document** . . . 1
**Table of contents** . . . 2
**List of tables** . . . 3
**List of figures** . . . 4
**1 General information** . . . 5
1.1 Inlay requirements . . . 5
**2 Electrical characteristics** . . . 6
2.1 Circuit model . . . 6
2.2 Calculations and formulas . . . 6
2.2.1 Card capacitance . . . 6
2.2.2 Coil inductance . . . 7
2.2.3 Resonance frequency . . . 8
2.2.4 Q factor . . . 8
**3 Electrical specifications** . . . 9
3.1 my-d™ move (NFC) and my-d™ move lean (NFC) . . . 9
3.2 NRG™ SLE 66R35I, NRG™ SLE 66R35R . . . 11
3.3 NRG™ SLE 66R35E7, NRG™ SLE 66R35E7H . . . 13
3.4 Physical parameters . . . 14
**References** . . . 15
**Glossary** . . . 16
**Revision history** . . . 17
**Disclaimer** . . . 18

# List of tables

Table 1 Chip variants . . . . . 5
Table 2 Coil manufacturing parameter . . . . . 7
Table 3 Electrical parameters my-d™ move (NFC) and my-d™ move lean (NFC) . . . . . 9
Table 4 Absolute maximum ratings my-d™ move (NFC) and my-d™ move lean (NFC) . . . . . 10
Table 5 Electrical parameters NRG™ SLE 66R35I, NRG™ SLE 66R35R . . . . . 11
Table 6 Absolute maximum ratings NRG™ SLE 66R35I, NRG™ SLE 66R35R . . . . . 12
Table 7 Electrical parameters NRG™ SLE 66R35E7, NRG™ SLE 66R35E7H . . . . . 13
Table 8 Electrical characteristics table template . . . . . 14

# List of figures

Figure 1 Contactless memory card . . . . . 5
Figure 2 Equivalent circuit of chip and the antenna coil . . . . . 6
Figure 3 Equivalent circuit of the coil . . . . . 7
Figure 4 Chip input capacitance of my-d™move (NFC) and my-d™ move lean (NFC) . . . . . 9
Figure 5 Chip input resistance of my-d™ move (NFC) and my-d™move lean (NFC) . . . . . 10
Figure 6 Chip input capacitance of NRG™ SLE 66R35I, NRG™ SLE 66R35R . . . . . 11
Figure 7 Chip input resistance of NRG™ SLE 66R35I, NRG™ SLE 66R35R . . . . . 12
Figure 8 Chip input capacitance of NRG™ SLE 66R35E7, NRG™ SLE 66R35E7H . . . . . 13
Figure 9 Chip input resistance of NRG™ SLE 66R35E7, NRG™ SLE 66R35E7H . . . . . 14

# 1 General information

This document gives details on ISO/IEC 14443-3 Type A [3] devices and shall assist designers of Tag antenna inlays. The recommendations given are for guidance only. The specific behavior of the antenna design shall be verified by measurement according to ISO/IEC 10373-6 [4] Test methods for proximity cards.

The following ISO/IEC 14443-3 Type A [3] compliant contactless memory chips are available:

**Table 1 Chip variants**

| Device name | Type |
|---|---|
| my-d™ move | SLE 66R01P |
| my-d™ move NFC | SLE 66R01PN |
| my-d™ move lean | SLE 66R01L |
| my-d™ move lean NFC | SLE 66R01LN |
| 1 KB memory chip with NRG™ | NRG™ SLE 66R35I, NRG™ SLE 66R35R |
| 1 KB memory chip with NRG™ | NRG™ SLE 66R35E7, NRG™ SLE 66R35E7H |

For more details please contact Connected Secure Systems CSSCustomerService@infineon.com.

## 1.1 Inlay requirements

The resonance frequency of a complete card should be in the range of 15 MHz operating at the lower limit of the field strength. If two or more cards are magnetically coupled (by being close or even on top of each other) the resonance frequency of all of them will be reduced.

The target is to minimize the impact on the operating range if at least two cards are stacked. For this reason, the lower limit of the resonance frequency of a single card should not be below 15 MHz.

On the other hand, the operating distance of a card will be reduced if the resonance frequency deviates too much from the operating frequency. To ensure full operability of a card at the minimum value for the magnetic field $H_{min}$ = 1.5 A/m (as defined by ISO/IEC 14443-2 [2]) the upper limit of the resonance frequency of a single card should not exceed 17 MHz.

In applications requiring only one card in the magnetic field (e.g. tokens or watches), the resonance frequency of a complete card can be close to the carrier frequency, to enhance the coupling distance.

Figure 1 shows a typical construction of a contactless memory card based on the ID1 form factor. The design of other form factors deviate and are not in the scope of this document.

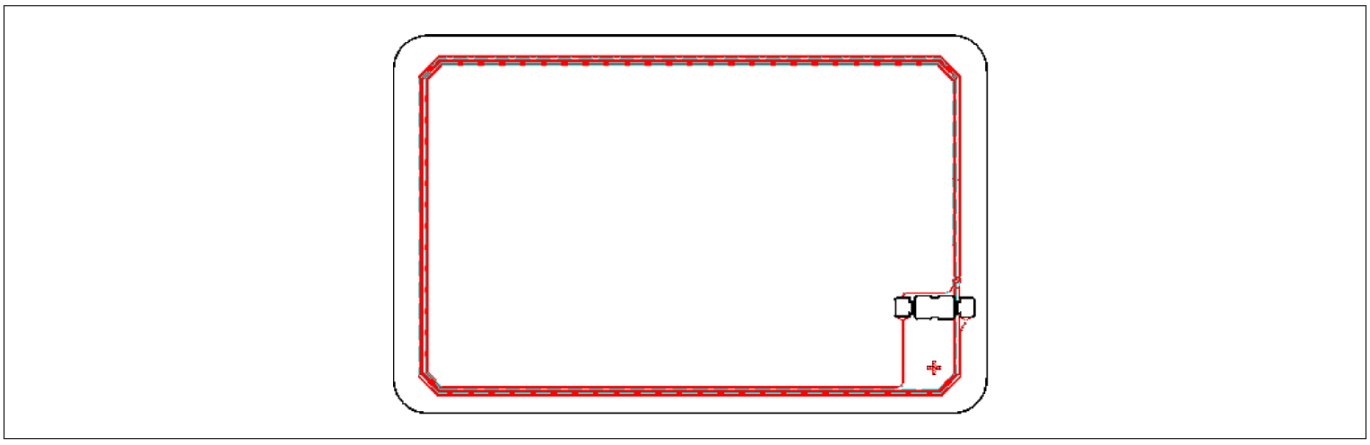


**Figure 1 Contactless memory card**

# 2 Electrical characteristics

The electrical characteristics are part of the datasheet, but they can also be measured at the $L_A$ and $L_B$ pads of the chip. Based on the circuit model the different parameters listed have an impact on the tuning.

## 2.1 Circuit model

An equivalent circuit of the chip and antenna coil is shown in Figure 2.

An antenna coil $L_{coil}$ is connected to the antenna pads $L_A$ and $L_B$. When the chip is powered it represents an AC load resistance $_{RIC}$ and an input capacitance $C_{chip}$ to the antenna coil. From the electrical point of view, the mounting of the chip adds the capacitance $C_{mount}$ to the resonance circuit, but the main portion of the capacitance is still given by the ICs input capacitance.

The coil will include some stray capacitance $C_{stray}$ and a series AC resistance $R_{coil}$. An external tuning capacitor $C_{ext}$ can also be added to the coil if required.

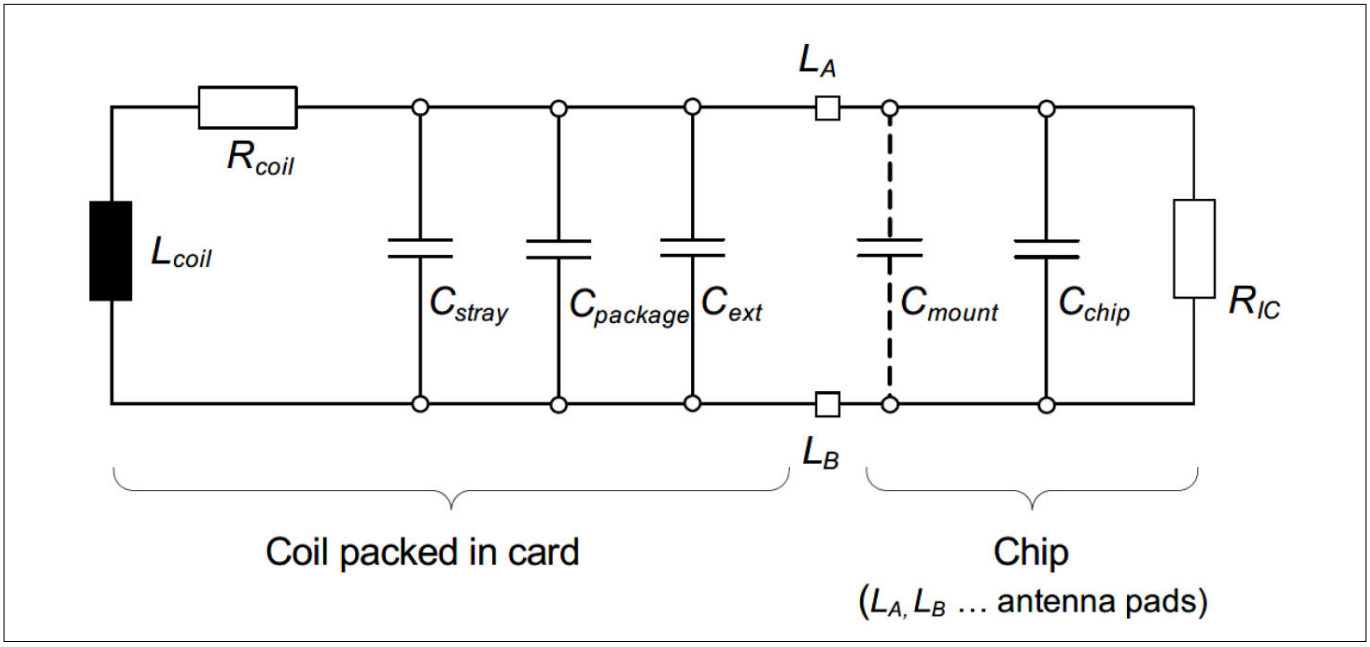



**Figure 2 Equivalent circuit of chip and the antenna coil**

## 2.2 Calculations and formulas

Based on the equivalent circuit (see Figure 2), the following correlations may be used to estimate the tuning of a card.

### 2.2.1 Card capacitance

The entire capacitance of the inlay/card comprises the following components:

- $C_{stray}$ → Stray capacitance
- $C_{package}$ → Package capacitance due to dielectric properties of the packaging material
- $C_{ext}$ → An optional external capacitance to achieve the desired tuning
- $C_{chip}$ → Chip capacitance
- $C_{mount}$ → Parasitic mounting capacitor

Due to the dielectric property of the card package material, $C_{package}$ has to be added to the resonant circuit. This value is influenced by the card manufacturing process and must be considered in the verification of a coil design.

It is recommended to keep this dependence in mind when changing from one packaging material to another and to verify the new card material with the given limits.

The resulting capacitance is the sum of those capacitors:

Resulting capacitance

$$c_{\text{res}} = c_{\text{stray}} + c_{\text{package}} + c_{\text{ext}} + c_{\text{chip}} + c_{\text{mount}} \quad (1)$$

### 2.2.2 Coil inductance

From the electrical point of view, the coil is not only an ideal inductivity ($L_{coil}$) but has also a resistive ($R_{coil}$) and a capacitive component ($C_{stray}$). The value of these components is of essential importance for the card's electrical and functional properties.

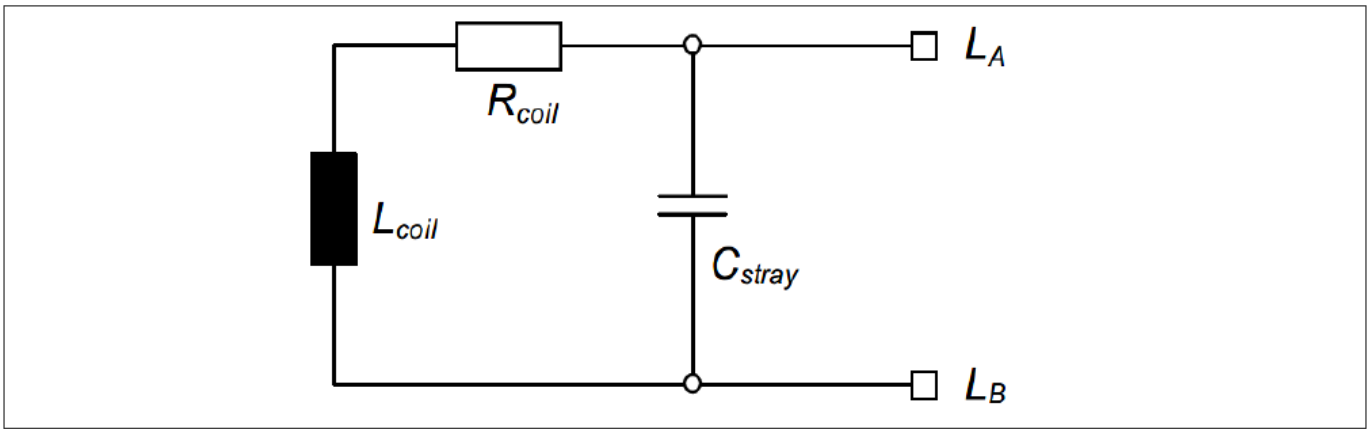



**Figure 3 Equivalent circuit of the coil**

The inductivity of the coil $L_{coil}$ may be estimated with the following equation:

Estimation of coil inductance

$$L_{\text{coil}} = 2 \times l \times \left(\ln\frac{l}{D} - 1,04\right) \times N^{P}[\text{nH}] \quad (2)$$

- l → Length of one turn of the coil (mm)
- N → Number of turns
- D → Diameter of wire or width of conductor (mm)
- P → Exponent of N depends on the coil manufacturing technology

P gives the exponent for the calculation of the inductivity and depends on the different coil manufacturing technologies. The table below gives the estimated values for turn exponent P.

**Table 2 Coil manufacturing parameter**

| P | Coil manufacturing technology |
|---|---|
| 1.8 | Wired coil |
| 1.7 | Etached coil |
| 1.5 - 1.7 | Printed coil |

***Note**: The equation is only considered for a first estimation. The real value of the inductivity has to be verified by measurement.*

Q factor estimation coil

$$Q_{\text{coil}} = \frac{2 \times \pi \times f_{\text{operating}} \times L_{\text{coil}}}{R_{\text{coil}}} \tag{3}$$

From the formula above it is obvious that the resistive part of the coil $R_{coil}$ must be as small as possible to achieve a high coil quality factor $Q_{coil}$. With a higher coil quality factor $Q_{coil}$, the operating distance will increase.

### 2.2.3 Resonance frequency

The entire capacitance together with the inductance of the coil influence the resonance frequency of the card and its performance:

Resonance frequency

$$f_{\text{res}} = \frac{1}{2\pi\sqrt{L_{\text{coil}} \times C_{\text{res}}}} \tag{4}$$

### 2.2.4 Q factor

$R_{IC}$ mainly determines the quality factor of the chip. The Q factor of the chip can be calculated using the following equation:

Q factor estimation chip

$$Q_{\text{chip}} = 2 \times \pi \times f_{\text{operating}} \times C_{\text{chip}} \times R_{\text{IC}} \tag{5}$$

The total Q factor can be estimated when using the following equation:

$$Q_{\text{total}} = \frac{1}{\frac{1}{Q_{\text{coil}}} + \frac{1}{Q_{\text{chip}}}} \tag{6}$$

For good energy transmission, a high Q factor is desirable.

# 3 Electrical specifications

The electrical specifications are of the different contactless memory chips supporting the ISO/IEC 14443 Type A [1]. The standards are listed below.

## 3.1 my-d™ move (NFC) and my-d™ move lean (NFC)

Values for the chip input capacitance $C_{chip}$ and AC load resistance $R_{IC}$ are given below.
All values are measured at sinusoidal waveform ($f_C$) = 13.56 MHz and ambient temperature ($T_A$) = 25°C.

**Table 3 Electrical parameters my-d™ move (NFC) and my-d™ move lean (NFC)**

| Parameter | Symbol | Values | | | Unit | Note or test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Chip input capacitance $L_A$-$L_B$ | $C_{chip}$ | 16.15 | 17 | 17.85 | pF | $V_{AB\ peak}$ = 3.0 V, $f_C$ = 13.56 MHz, $T_A$ = 25°C |
| Chip load resistance $L_A$-$L_B$ | $R_{IC}$ | 3 | 4.5 | 6 | kΩ | $V_{AB\ peak}$ = 3.0 V, $f_C$ = 13.56 MHz, $T_A$ = 25°C |

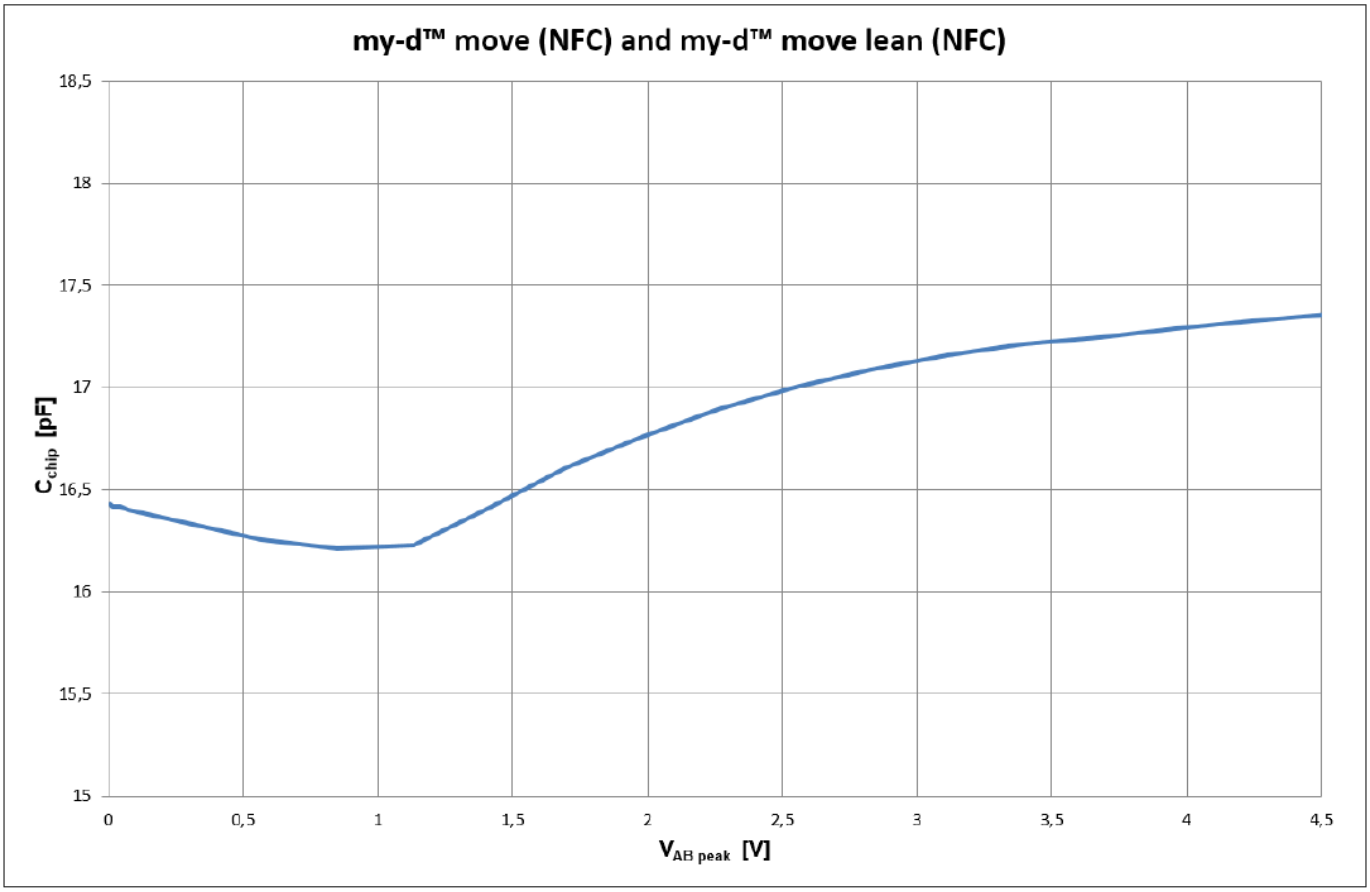



**Figure 4 Chip input capacitance of my-d™move (NFC) and my-d™ move lean (NFC)**

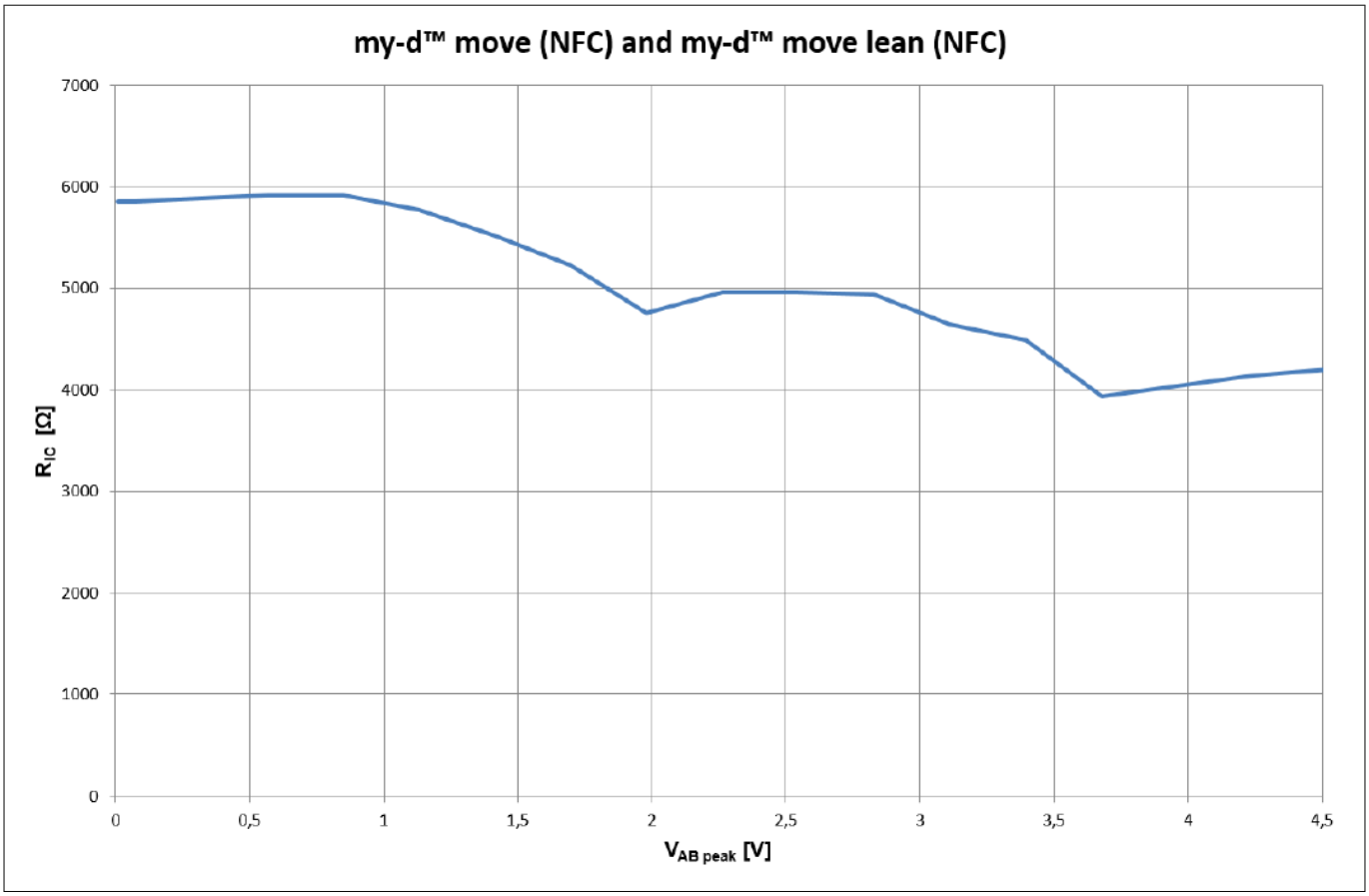



**Figure 5** **Chip input resistance of my-d™ move (NFC) and my-d™move lean (NFC)**

**Table 4** **Absolute maximum ratings my-d™ move (NFC) and my-d™ move lean (NFC)**

| Parameter | Symbol | Values | | | Unit | Note or test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input peak voltage between $L_A$-$L_B$ | $V_{AB\ peak}$ | - | - | 6 | V | - |
| Input current through $L_A$-$L_B$ | $I_{IN}$ | - | - | 30 | mA | - |
| Storage temperature | $T_S$ | -40 | - | +125 | °C | - |
| ESD protection voltage ($L_A$, $L_B$ pins) | $V_{ESD}$ | 2 | - | - | kV | JEDEC STD EIA/ JESD22 A114-B |

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this application note is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability, including EEPROM data retention and write/erase endurance.

## 3.2 NRG™ SLE 66R35I, NRG™ SLE 66R35R

Values for the chip input capacitance $C_{chip}$ and AC load resistance $R_{IC}$ are given below.
All values are measured at sinusoidal waveform ($f_C$) = 13.56 MHz and ambient temperature ($T_A$) = 25°C.

**Table 5 Electrical parameters NRG™ SLE 66R35I, NRG™ SLE 66R35R**

| Parameter | Symbol | Values | | | Unit | Note or test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Chip input capacitance $L_A$-$L_B$ | $C_{chip}$ | 16.5 | 18.3 | 20.1 | pF | $V_{AB\ peak}$ = 2.3 V, $f_C$ = 13.56 MHz, $T_A$ = 25°C |
| Chip load resistance $L_A$-$L_B$ | $R_{IC}$ | 13.6 | 17 | 20.4 | kΩ | $V_{AB\ peak}$ = 2.3 V, $f_C$ = 13.56 MHz, $T_A$ = 25°C |

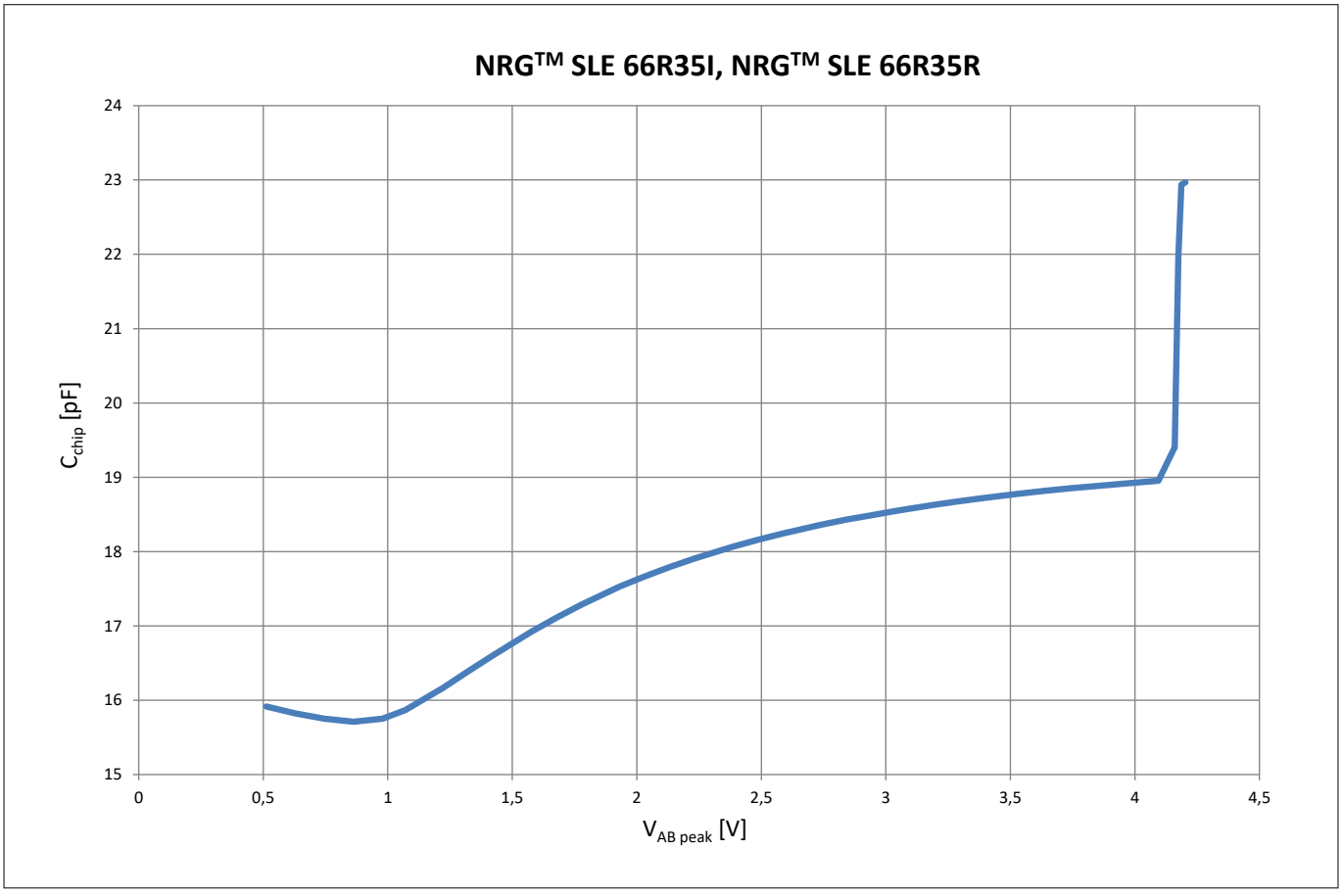



**Figure 6 Chip input capacitance of NRG™ SLE 66R35I, NRG™ SLE 66R35R**

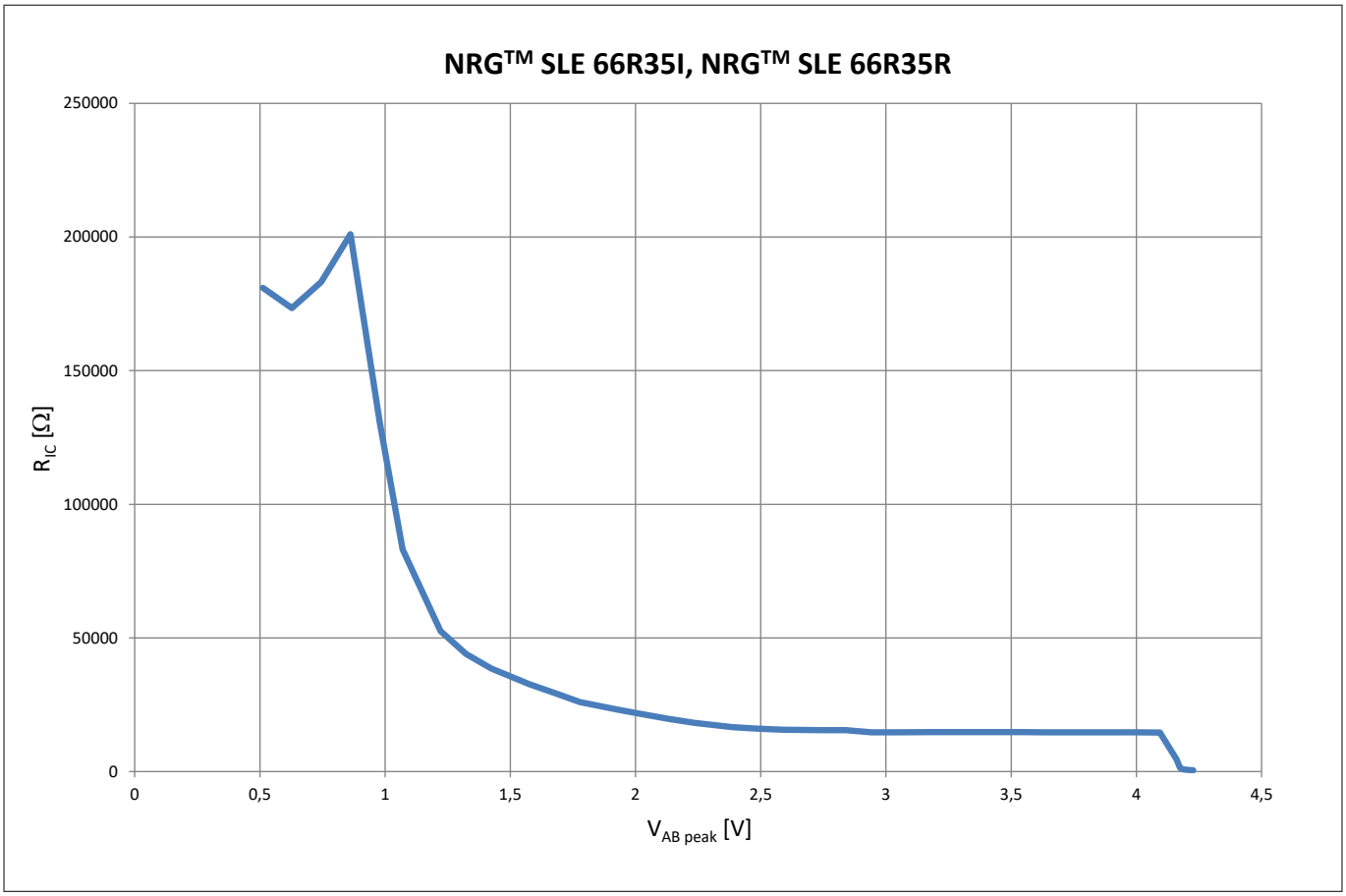



**Figure 7** **Chip input resistance of NRG™ SLE 66R35I, NRG™ SLE 66R35R**

**Table 6** **Absolute maximum ratings NRG™ SLE 66R35I, NRG™ SLE 66R35R**

| Parameter | Symbol | Values | | | Unit | Note or test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input peak voltage between $L_A$-$L_B$ | $V_{AB\ peak}$ | -7 | - | +7 | V | - |
| Input current through $L_A$-$L_B$ | $I_{IN}$ | - | - | 50 | mA | - |
| Storage temperature | $T_S$ | -40 | - | +125 | °C | - |
| ESD protection voltage ($L_A$, $L_B$ pins) | $V_{ESD}$ | 2 | - | - | kV | JEDEC STD EIA/ JESD22 A114-B |

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## 3.3 NRG™ SLE 66R35E7, NRG™ SLE 66R35E7H

Values for the chip input capacitance $C_{chip}$ and AC load resistance $R_{IC}$ are given below.
All values are measured at sinusoidal waveform ($f_C$) = 13.56 MHz and ambient temperature ($T_A$) = 25°C.

**Table 7 Electrical parameters NRG™ SLE 66R35E7, NRG™ SLE 66R35E7H**

| Parameter | Symbol | Values | | | Unit | Note or test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Chip input capacitance $L_A$-$L_B$ | $C_{chip}$ | 17.3 | 18.3 | 19.3 | pF | $V_{AB\ peak}$ = 2.0 V,<br>$f_C$ = 13.56 MHz,<br>$T_A$ = 25°C<br>Tolerance: +/-5% |
| Chip load capacitance $L_A$-$L_B$ | $R_{IC}$ | - | 4.5 | - | kΩ | $V_{AB\ peak}$ = 2.0 V,<br>$f_C$ = 13.56 MHz,<br>$T_A$ = 25°C |

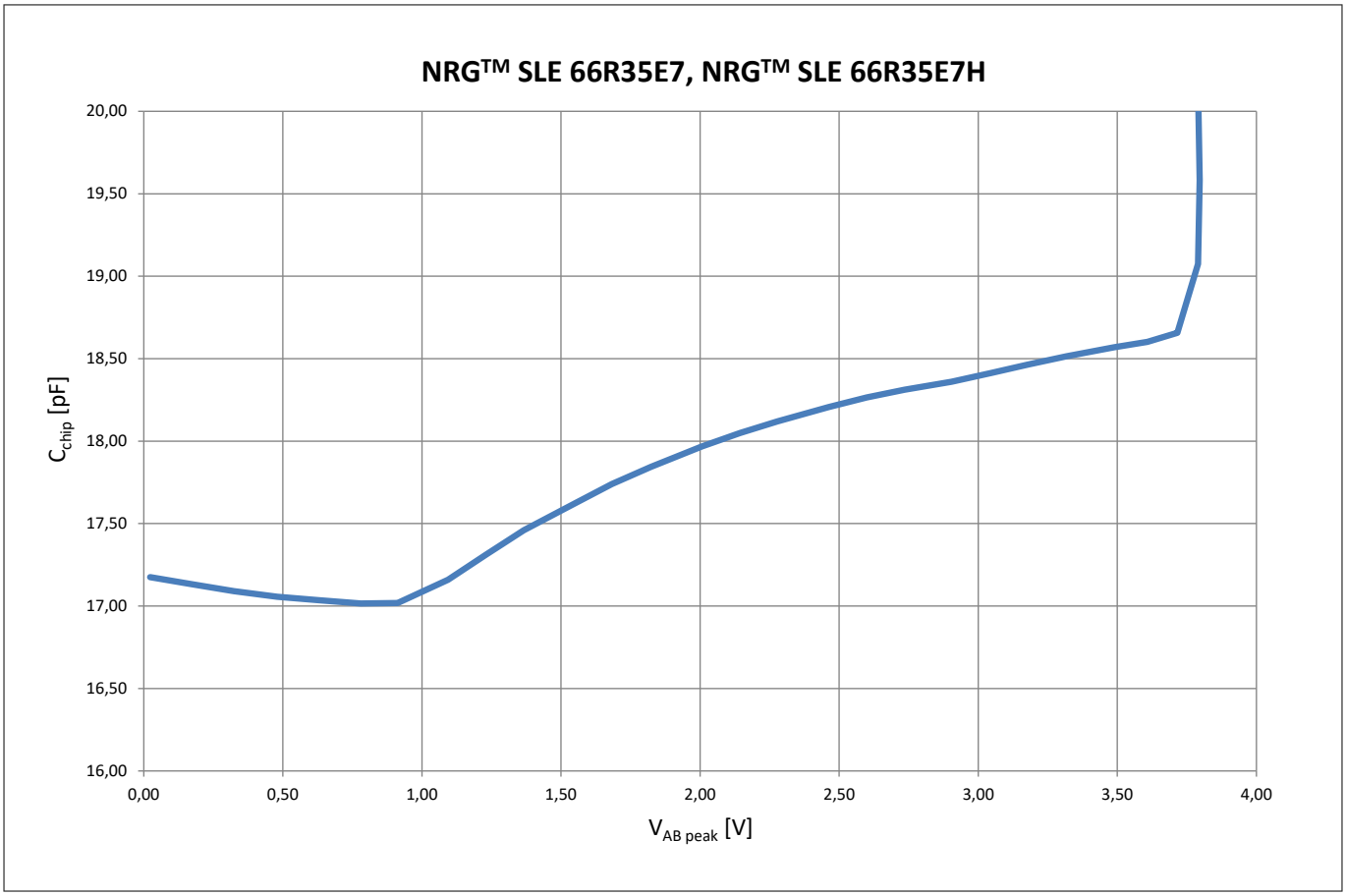



**Figure 8 Chip input capacitance of NRG™ SLE 66R35E7, NRG™ SLE 66R35E7H**

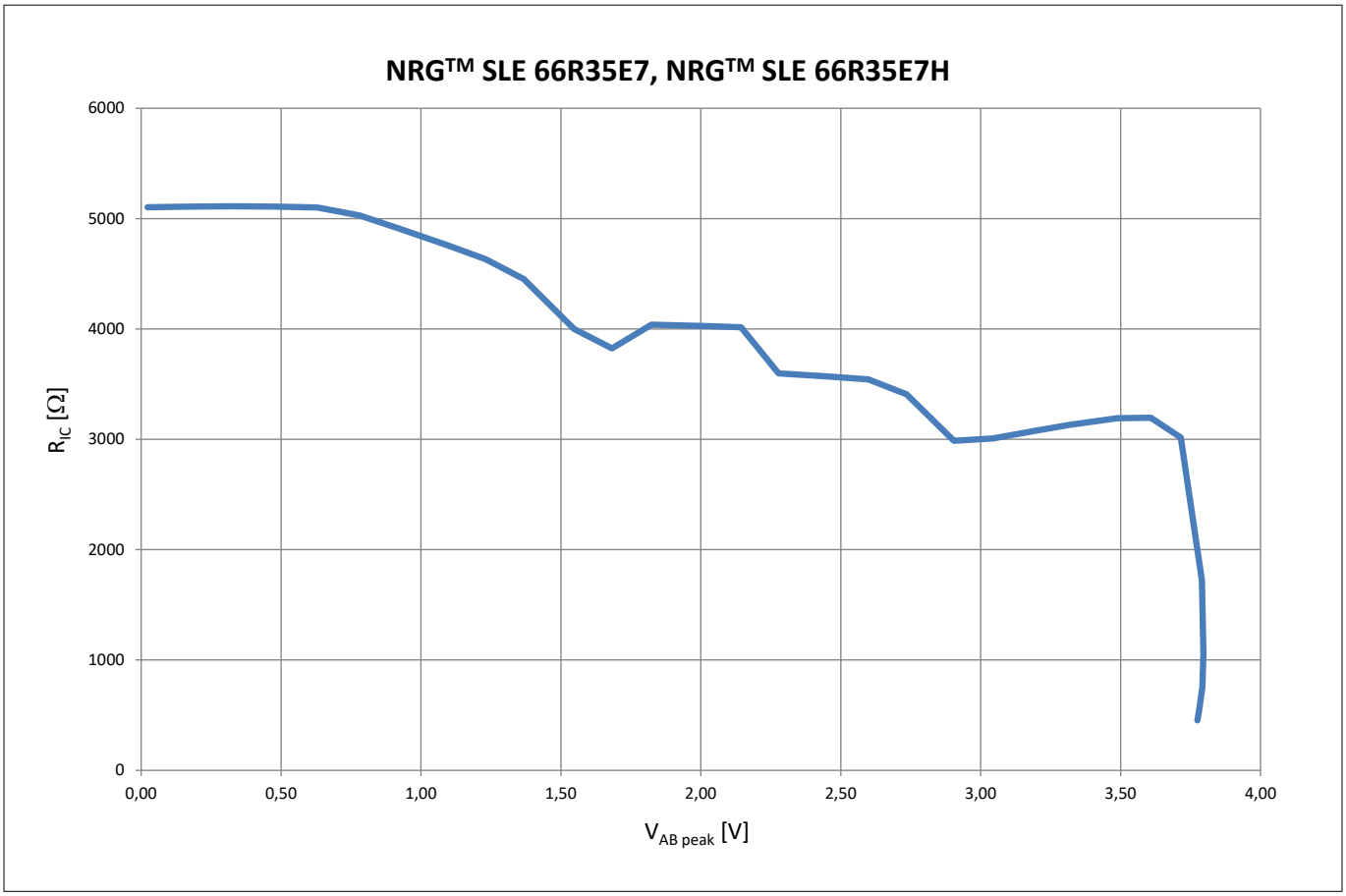



**Figure 9** **Chip input resistance of NRG™ SLE 66R35E7, NRG™ SLE 66R35E7H**

**Table 8** **Electrical characteristics table template**

| Parameter | Symbol | Values | | | Unit | Note or test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input peak voltage between $L_A$-$L_B$ | $V_{AB\ peak}$ | - | - | 6 | V | - |
| Input current through $L_A$-$L_B$ | $I_{IN}$ | - | - | 50 | mA | - |
| Storage temperature | $T_S$ | -40 | - | +125 | °C | - |
| ESD protection voltage ($L_A$, $L_B$ pins) | $V_{ESD}$ | 2 | - | - | kV | JEDEC STD EIA/ JESD22 A114-B |

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this application note is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability, including EEPROM data retention and write/erase endurance.

## 3.4 Physical parameters

Physical specifications are listed in the “appropriate wafer specification”.

# References

**[1]** ISO/IEC 14443-1:2016: *Identification cards - Contactless integrated circuit cards - Proximity cards - Part 1: Physical characteristics (Third edition)*; 2016-03

**[2]** ISO/IEC 14443-2:2020: *Cards and security devices for personal identification – Contactless proximity objects - Part 2: Radio frequency power and signal interface (Fourth edition)*; 2020-07

**[3]** ISO/IEC 14443-3:2018: *Cards and security devices for personal identification – Contactless proximity objects – Part 3: Initialization and anticollision (Fourth edition)*; 2018-07

**[4]** ISO/IEC 10373-6:2020: *Cards and security devices for personal identification – Test methods – Part 6: Contactless proximity objects*; 2020-07

# Glossary

**AC**

*alternating current (AC)*

A synonym for dynamic parameters of an electronic circuit.

**EEPROM**

*electrically erasable programmable read-only memory (EEPROM)*

**ESD**

*electrostatic discharge (ESD)*

A sudden and momentary flow of electric current between two electrically charged objects caused by contact, an electrical short or dielectric breakdown.

**IC**

*integrated circuit (IC)*

A miniature electronic circuit built on the surface of a thin substrate of a semiconductor material.

**IEC**

*International Electrotechnical Commission (IEC)*

The international committee responsible for drawing up electrotechnical standards.

**ISO**

*International Organization for Standardization (ISO)*

**JEDEC**

*Joint Electron Device Engineering Council (JEDEC)*

**NFC**

*near field communication (NFC)*

# Revision history

| Reference | Description |
|---|---|
| **Revision 4.0, 2026-03-05** | |
| All | Template updates |
| **Revision 3.1, 2022-11-04** | |
| All | • Updated editorial changes<br>• Removed my-d™ NFC and my-d™ proximity related information |
| **Revision 3.0, 2022-10-06** | |
| All | • Updated the product name from SLE 66R35x to NRG™ SLE 66R35x |
| **Revision 2.0, 2022-03-02** | |
| All | • Migrated to latest IFX template and updated editorial changes<br>• Updated References list and removed NRG™ SLE 66R35 |
| **Revision 1.3, 2021-04-14** | |
| All | Removed “confidential” marking |
| **Revision 1.2, 2019-07-23** | |
| All | • Added NRG™ SLE 66R35E7H and NRG™ SLE 66R01LN<br>• Editorial changes |
| **Revision 1.1, 2017-05-12** | |
| All | Major review |
| **Revision 1.0, 2017-03-28** | |
| All | Initial release |

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