Hardware design guidelines for EZ-PD™ PMG1-S3/EZ-PD™ CCG8 in TBT certifications for VCONN source

About this document

Scope and purpose

This application note recommends practices for hardware design and the critical items that a designer must consider while using VCONN source with EZ-PD™ PMG1-S3 MCU and EZ-PD™ CCG8 controller-based Intel reference platforms.

Intended audience

This document is intended for anyone who uses EZ-PD™ PMG1-S3 MCU and EZ-PD™ CCG8 controller-based Intel reference platforms and its certifications.

Key points

- Demonstrates VCONN source design considerations for EZ-PD™ PMG1-S3 MCU and EZ-PD™ CCG8 controllers
- Provides hardware implementation aspects for VCONN SCP

About this product family

Product family

Infineon's EZ-PD™ portfolio is the industry's most complete portfolio of USB Type-C Power Delivery (PD) controller solutions, enabling more robust end-to-end Power Delivery (PD) and charging solutions for laptop and mobile devices, including AEC-Q100-certified versions for automotive-grade performance.

Target applications

- Docks and host designs

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1 Introduction

EZ-PD™ PMG1 (Power Delivery microcontroller Gen 1) is a family of high-voltage USB-C Power Delivery (PD) microcontrollers (MCU). EZ-PD™ CCG8 is a dual/single-port USB Type-C controller that complies with the latest USB Type-C and Power Delivery (PD) specifications.

Intel dock or hosts reference designs use EZ-PD™ PMG1-S3 as a PD controller along with a dock management controller and EZ-PD™ CCG8 as a PD controller. As part of the development, there are various tests carried out in validating the fault protections on VBUS and VCONN lines.

As part of USB-IF PD Specification, it does not require the short-circuit protection (SCP) on VCONN fault protection, but the Thunderbolt (TBT) specification requires this feature to be supported.

Both the MCUs support the following protections:

- VBUS overvoltage protection (VBUS OVP)
- VBUS overcurrent protection (VBUS OCP)
- VBUS short-circuit protection (VBUS SCP)
- VCONN overcurrent protection (VCONN OCP)
- VBUS undervoltage protection (VBUS UVP)

This document will act as a design guideline for supporting the VCONN short-circuit protection (VCONN SCP) fault protections externally as EZ-PD™ PMG1-S3/EZ-PD™ CCG8 products does not support SCP fault protections on VCONN line.

This guideline is intended for designs using EZ-PD™ PMG1-S3/EZ-PD™ CCG8 products to support the VCONN short-circuit protection (VCONN SCP) fault protections externally and achieve the TBT certification.

2 Design considerations for VCONN source with EZ-PD™ PMG1-S3/EZ-PD™ CCG8 devices

The EZ-PD™ PMG1-S3/EZ-PD™ CCG8 devices does not have provision for VCONN short-circuit protection (SCP), any instance of SCP fault on VCONN would cause electrical overstress (EOS) damage as the power is enabled to a VCONN pin which gets directly connected to GND.

Figure 1 shows the power rails of silicon, which depicts the internal FET design of VCONN in EZ-PD™ PMG1-S3/ EZ-PD™ CCG8 devices.

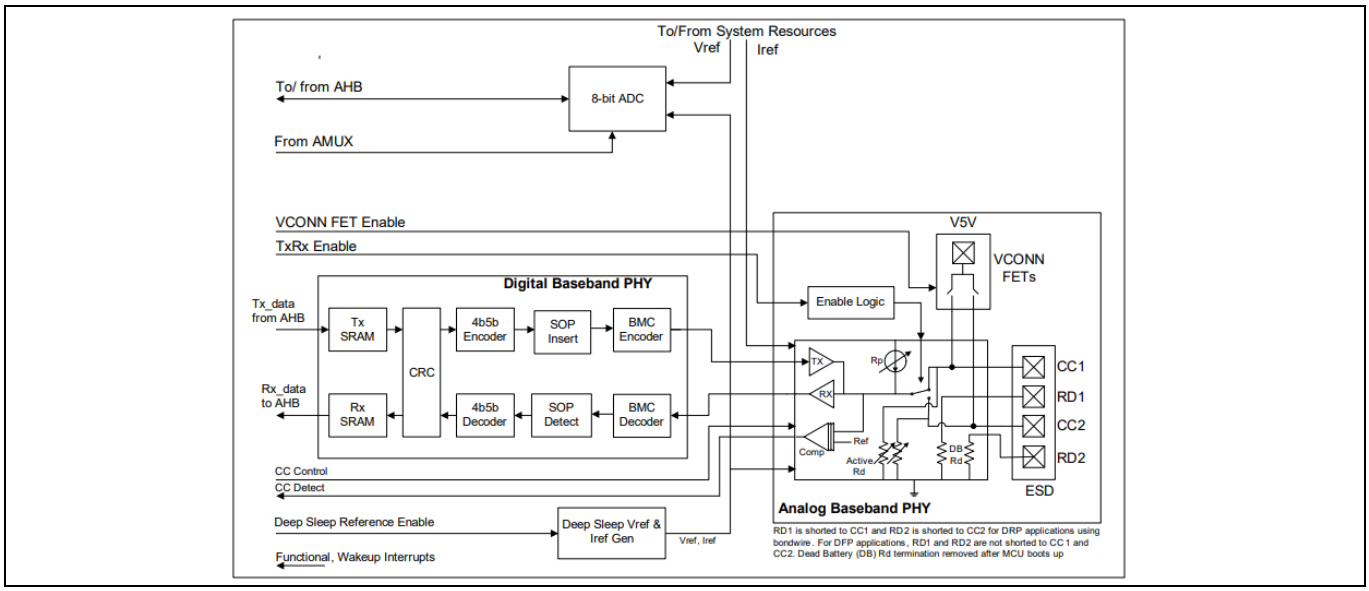


Figure 1 FET design in USB PD subsystem

The primary purpose of this document is to provide guideline for recommended protections on CC lines and limit the current to the CC1/2 VCONN power source (V5V of EZ-PD™ PMG1-S3/EZ-PD™ CCG8) pins and prevent the silicon damage during VCONN SCP fault.

Overcurrent protection (OCP) prevents excessive current from damaging the VCONN switch or downstream cable electronics due to normal overcurrent conditions and this usually happens in steps whereas in short-circuit protection (SCP), which protects the VCONN path from catastrophic faults like a hard short between the CC line and VCONN source, which can damage the IC or cable.

This issue will not be seen in case of OCP, which is different from SCP as in SCP test, device under test (DUT) will enable power (VCONN of this case) that connects to GND directly and that is different with OCP test that increments current by a few steps of mA.

To mitigate this, the docks or hosts designs with EZ-PD™ PMG1-S3/EZ-PD™ CCG8 silicon is suggested to include following changes to limit current from VCONN power source directly to VCONN path pin.

It is recommended to choose a buck-boost regulator to limit the current in between 1 A to 1.5 A passing through the CC1/2 VCONN power source (V5V of EZ-PD™ PMG1S3/EZ-PD™ CCG8) pins.

2 Design considerations for VCONN source with EZ-PD™ PMG1-S3/EZ-PD™ CCG8 devices

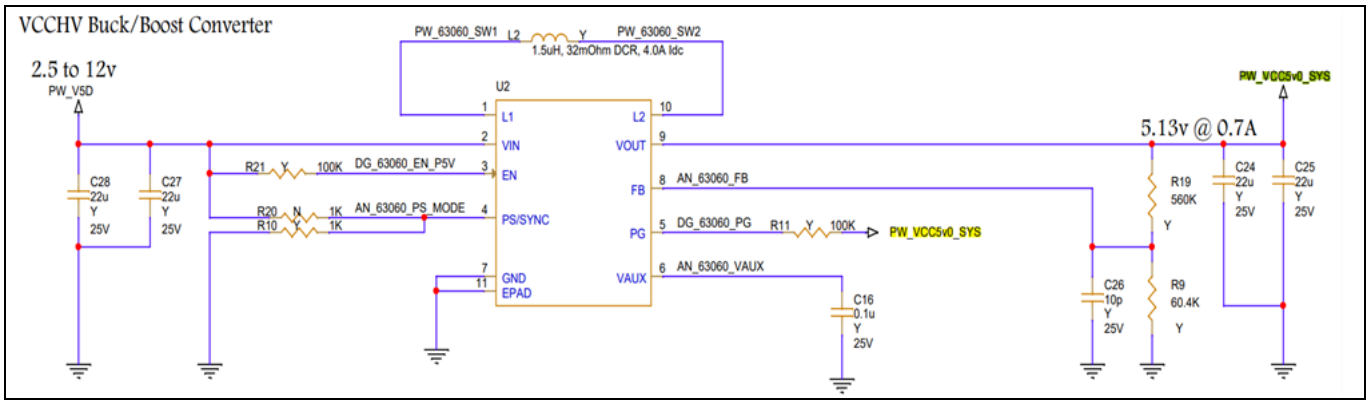


Figure 2 Buck-boost converter on VCONN source

As shown in Figure 2, consider the schematic to design the buck-boost circuitry on the CC1/2 VCONN power source (V5V of EZ-PD™ PMG1-S3/EZ-PD™ CCG8) pin path.

Adding a buck-boost stage on VCONN pins prevents SCP faults by smoothing voltage transients, limiting inrush currents, and buffering energy spikes, ensuring the VCONN pins never experience extreme currents that trigger short-circuit protection.

In designing a buck-boost converter on VCONN pins to provide short-circuit protection (SCP), the concept of power-good functionality can be effectively leveraged as a protective mechanism by continuously monitoring the inductor current and output voltage to detect early signs of overcurrent or voltage drop.

Alternatively, if the VCONN load is low power, and fast transient disconnection is not required and for low-cost bill of materials (BOM), it is suggested to choose a polyfuse or power-switch with current limitation of ~1.5 A ~ 2 A.

The MOSFET's on-resistance ($R_{DS(on)}$) of power-switch or polyfuse is a key parameter that directly affects voltage drop, conduction losses, and coordination during fault events. Proper selection balances normal operating efficiency with protection effectiveness. The best practice is to choose the value of $R_{DS(on)}$ close to 100 mΩ to 300 mΩ, as this provides a good compromise between low normal voltage drop and effective short-circuit current limiting with a power-switch or polyfuse rated for 1 A to 2 A.

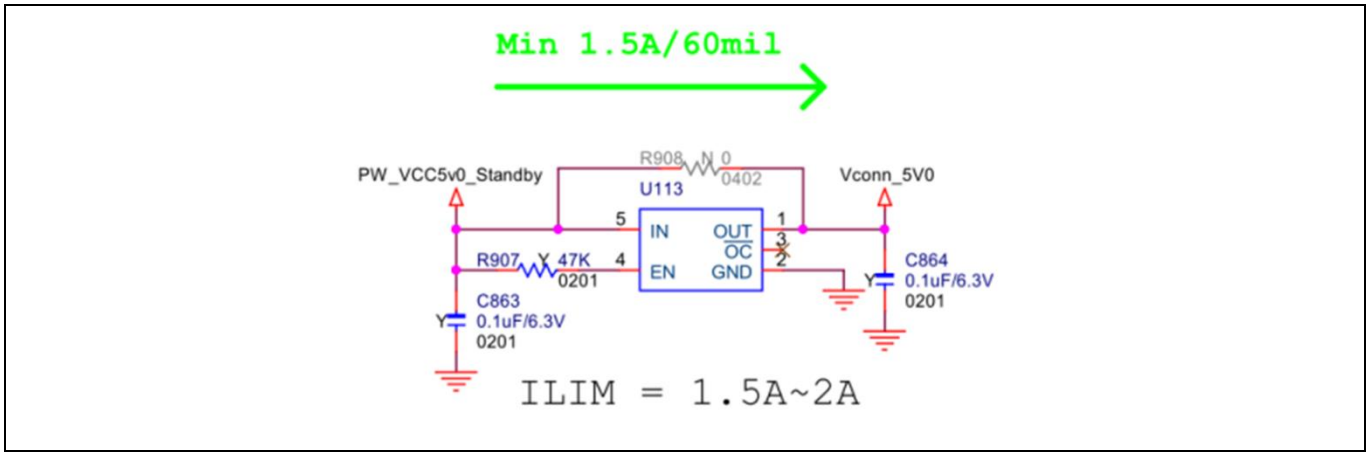


Figure 3 Low-cost power-switch or polyfuse on VCONN source

2 Design considerations for VCONN source with EZ-PD™ PMG1-S3/EZ-PD™ CCG8 devices

As shown in Figure 3, consider the circuitry in designing the power-switch or polyfuse to VCONN path. In current limit circuitry design, it prevents damage to the MOSFET switch and the hub port and can deliver load current up to the current limit threshold through the switch of power-switch or polyfuse.

When a heavy load or short-circuit is applied to an enabled switch, a large transient current may flow until the current limit circuitry responds. Once exceeding the current limit threshold, the power-switch or polyfuse will enter constant current (CC) mode until the thermal shutdown occurs or the fault is removed. With this the VCONN path can be protected.

3 Related resources

- EZ-PD™ PMG1-S3 MCU webpage
- EZ-PD™ CCG8 controller webpage
- CYPM13xx, EZ-PD™ PMG1-S3 Power Delivery MCU Gen1 datasheet
- EZ-PD™ CCG8 USB Type-C port controller datasheet
- EZ-PD™ USB Type-C forum from Infineon Developer Community
- AN232565 – EZ-PD™ PMG1 MCU hardware design guidelines and checklist

Revision history

Document revision	Date	Description of changes
**	2026-02-25	Initial release

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