EZ-USB™ FX5/FX5N/FX10/FX20 hardware design guidelines and schematic checklist

About this document

Scope and purpose

This application note discusses the recommended practices for EZ-USB™ FX5/FX5N/FX10/FX20 hardware design and the critical items that a designer must consider. EZ-USB™ FX20 is the next-generation USB 3.2 Gen 2x2 peripheral controller that supports higher bandwidth up to 20 Gbps. With its highly integrated and flexible features, developers can add USB 3.2 Gen 2x2 functionality to any system using EZ-USB™ FX20.

Intended audience

This document is intended for anyone who uses the EZ-USB™ FX5/FX5N/FX10/FX20 peripheral controller.

Table of contents

About this document **1**
Table of contents **2**
1 Introduction **3**
2 Related resources **4**
2.1 EZ-USB™ FX20 Software Development Kit 4
3 Power system **5**
3.1 Power supply design 5
3.2 Device supply decoupling 6
4 Power modes **8**
5 Crystal **9**
5.1 Crystal effective load capacitor calculation 10
5.2 Layout consideration 10
6 High-bandwidth data subsystem (HBWSS) interface **11**
6.1 LVDS mode 11
6.2 LVCMOS 12
7 USB **13**
7.1 USB 20 Gbps 13
7.2 USB Full-Speed 16
7.3 USB-C cable 16
7.4 USB host controller 16
8 Low-speed peripherals **17**
8.1 I^2C interface 17
8.2 SWD/JTAG 17
8.3 I^2S 18
8.4 PDM 18
8.5 Quad SPI 18
8.6 CAN FD 19
9 Booting **20**
10 EMI and ESD considerations **21**
11 Generic electrical design considerations **22**
12 Schematics and layout review checklist **27**
13 Summary **29**
14 Appendix A – PCB layout tips **30**
15 Appendix B – Troubleshooting **31**
15.1 EZ-USB™ FX20 device not enumerating 31
References **32**
Revision history **33**
Disclaimer **34**

1 Introduction

Infineon's EZ-USB™ FX20 is a USB 3.2 Gen 2x2 (20 Gbps) peripheral controller that has a fully-configurable, general programmable interface called GPIF III, which can connect to any processor, ASIC, or FPGA using LVDS or LVCMOS interface. EZ-USB™ FX20 consists of dual Arm® Cortex®-M4 and M0+ core CPUs, integrated flash, SRAM, Serial Communication Blocks (SCBs), a cryptography accelerator, and high-bandwidth data subsystem providing DMA data transfers between low-voltage differential signalling (LVDS)/low-voltage CMOS (LVCMOS) and USB ports at speeds up to 20 Gbps. An additional 1 MB SRAM is included in the high-bandwidth data subsystem to provide buffering for USB data. EZ-USB™ FX20 also supports USB Type-C plug orientation detection and flip-mux function without needing an external mux.

See the reference schematic of the EZ-USB™ FX20 Development Kit (DVK) [8].

All the design guidelines and checklist mentioned in this document are applicable for FX5/FX5N/FX10/FX20 silicon.

2 Related resources

Infineon provides a wealth of data on Infineon Developer Community to help you to select the right EZ-USB™ FX20 device for your design and to help you quickly and effectively integrate the device into your design.

- Application notes: Infineon offers a large number of USB application notes covering a broad range of topics, from basic to advanced levels. Recommended application notes for getting started with EZ-USB™ FX20 are:
  - AN237841 – Getting started with EZ-USB™ FX20 [1]
- Reference manual:
  - EZ-USB™ FX20 reference manual [6]
- Development kits:
  - KIT_FX20_FMC_001, EZ-USB™ FX20 Development Kit [8]
  - KIT_FX10_FMC_001, EZ-USB™ FX10 Development Kit [9]
  - KIT_FX5N_FMC_001, EZ-USB™ FX5N Development Kit [10]
  - KIT_FX5_FMC_001, EZ-USB™ FX5 Development Kit [11]
  - DEMO_FX20_MIPI_001, EZ-USB™ FX20 USB MIPI Camera Demo Kit [12]

  Visit the EZ-USB™ FX20 webpage to view the development kits available for EZ-USB™ FX20
- Models: IBIS

2.1 EZ-USB™ FX20 Software Development Kit

Infineon delivers the complete firmware stack for EZ-USB™ FX20 to easily integrate any embedded application to USB 3.2 Gen 2x2. The EZ-USB™ FX20 Software Development Kit (SDK) comes with tools and application examples, which help accelerate application development .

For a complete and updated list of EZ-USB™ FX20 code examples, visit our GitHub repository.

Note: EZ-USB™ FX20 can be programmed using the EZ-USB™ Control Center Utility [13].

3 Power system

EZ-USB™ FX20 has the following power domains.

- USB3V18: Power supply for the USB 3.2 Gen 2x2 physical layer (PHY)
- V33: 3.3 V power supply for the USB 2 HS PHY, USB 2 FS PHY, and LVDS PHY
- VDDD: Main digital supply input that provides the inputs for internal regulators
- VCCD: Internal core logic supply; this supply needs to be decoupled externally
- VDDIO_Px: Power supplies for LVDS/LVCMOS I/Os
- VDDIO_Px_CTRL: Power supplies for LVCMOS control I/Os
- VDDIOQSPI: Power supply for the QSPI port
- VDDIOXTAL: Power supply for the crystal
- VDDIO: GPIO power supply
- VSS: Main ground for the entire chip

3.1 Power supply design

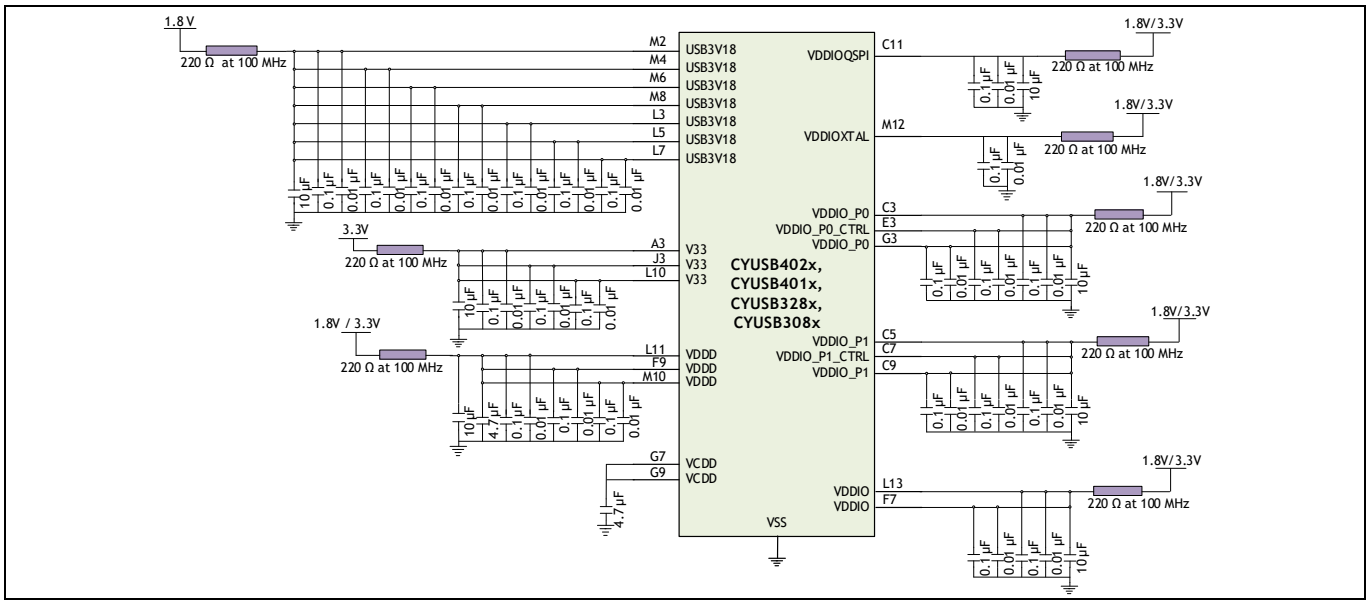


Figure 1 EZ-USB™ FX20 power domains

Note: For optimum noise performance of EZ-USB™ FX20, ensure a combination of 0.1 µF and 0.01 µF capacitors per pin. No power sequence is needed.

Note: For LVDS operation, VDDIO_P0 and VDDIO_P1 must be kept at 3.3 V. VDDIO_P0_CTRL and VDDIO_P1_CTRL can be at either 1.8 V or 3.3 V, depending on the desired CTRL signal logic level.

Table 1 EZ-USB™ FX20 power domains

Parameter	Description	Min.	Typ.	Max.	Unit
VDDD	Main analog supply voltage	1.62	1.8 or 3.3	3.63	V
USB3V18	Power supply voltage for USB 3 ports	1.62	1.8	1.98	V
V33	Power supply voltage for 3.3 V supply	2.97	3.3	3.63	V
VDDIO VDDIO_Px VDDIO_Px_CTRL VDDIOQSPI VDDIOXTAL	Power supply voltage for I/O in the 1.8 V range	1.62	1.8, 2.5, or 3.3	3.63	V
VCCD	Core logic supply output	–	1.1	–	V

3.2 Device supply decoupling

Power supply decoupling is critical in ensuring that system noise does not propagate into the device through the power supply. Improper decoupling can lead to jittery signaling, especially on the USB and LVDS bus, which results in a higher CRC error rate and more retries. Decoupling capacitors must be the ceramic type of a stable dielectric. It is important to have the decoupling caps close to the power pins, and short trace runs for the power and ground connections on the EZ-USB™ FX20 device to solid power and ground planes.

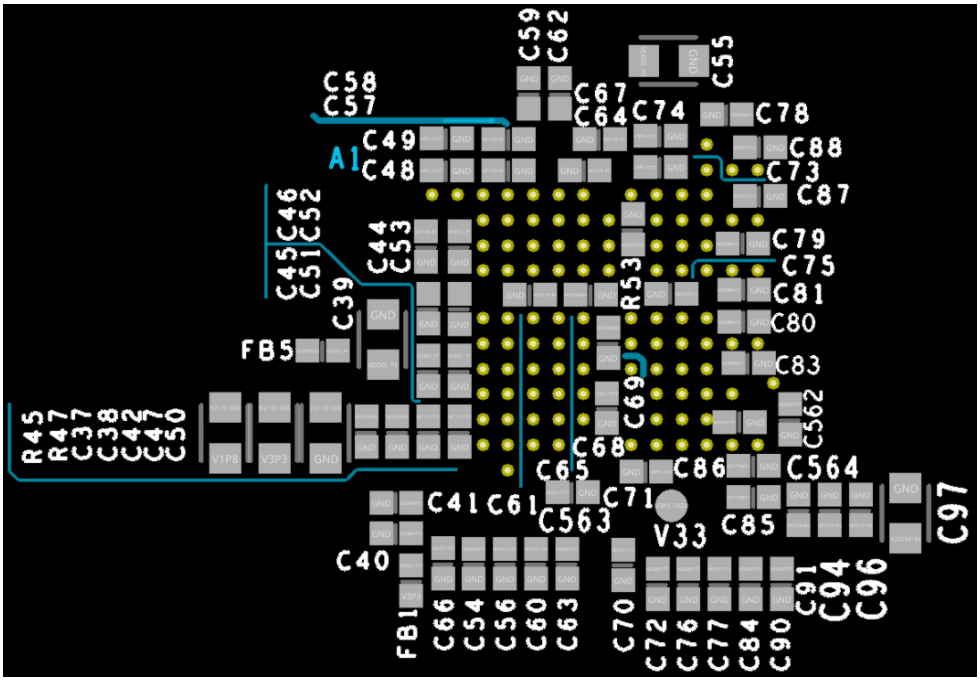


Figure 2 Placement of decoupling caps on the bottom layer of KIT_FX20_FMC_001 DVK

The specific recommendation for the ceramic capacitor nearest to each EZ-USB™ FX20 power pin is given in Table 2.

Table 2 Power domain decoupling requirements

Power domain (pin numbers)	Bulk capacitor	Capacitors per pin
USB3V18 (M2, M4, M6, M8, L3, L5, L7)	10 µF, 10 V	0.01 µF, 10 V and 0.1 µF, 10 V
V33 (A3, J3, L10)	10 µF, 10 V	0.01 µF, 10 V and 0.1 µF, 10 V
VDDD (L11, F9, M10)	22 µF, 10 V and 4.7 µF, 10 V	0.01 µF, 10 V and 0.1 µF, 10 V
VCCD (G7, G9)	4.7 µF, 10 V	–
VDDIOQSPI (C11)	10 µF, 10 V	0.01 µF, 10 V and 0.1 µF, 10 V
VDDIOXTAL (M12)	–	0.01 µF, 10 V and 0.1 µF, 10 V
VDDIO_P0 (C3, E3, G3)	10 µF, 10 V	0.01 µF, 10 V and 0.1 µF, 10 V
VDDIO_P1 (C5, C7, C9)	10 µF, 10 V	0.01 µF, 10 V and 0.1 µF, 10 V
VDDIO (F7, L13)	10 µF, 10 V	0.01 µF, 10 V and 0.1 µF, 10 V

Note: To get USB-IF certification for the product in bus power mode, plan to disable the power supply powering up the rest of the device apart from EZ-USB™ FX20.

4 Power modes

EZ-USB™ FX20 supports the following power modes:

- System Low Power (LP): All peripherals and CPU power mode are available at maximum speed
- CPU Active: CPU is executing code in system LP mode
- CPU Sleep: CPU code execution is halted in system LP mode
- CPU Deep Sleep: CPU code execution is halted and system Deep Sleep is requested in system LP mode
- System Deep Sleep: Only low-frequency peripherals are available after both CPUs enter CPU Deep Sleep mode
- Normal mode: Fully functional operating mode. The internal CPU clock and the internal PLLs are enabled in this mode
  - USB 3 operation at 5 Gbps, 10 Gbps, or 20 Gbps (U0 mode)
  - USB 3 low-power modes (U1, U2)
  - High-bandwidth data subsystem I/Os port in LVCMOS SDR or DDR mode
  - High-bandwidth data subsystem I/Os port in LVDS mode

The I/O power supplies (VDDIO_P0, VDDIO_P1, VDDIO_P0_CTRL, and VDDIO_P1_CTRL) can be turned off when the corresponding interface is not used. These supplies cannot be turned off at any time if the GPIF III interface is used in the application.

Other low-power modes include:

- Suspend mode with USB 3.0 mode
- Deep Sleep mode
- Core power-down mode

CPU Active, Sleep, and Deep Sleep are standard Arm®-defined power modes supported by the Arm® CPU instruction set architecture (ISA). System LP and Deep Sleep modes are additional low-power modes supported by EZ-USB™ FX20.

5 Crystal

The EZ-USB™ FX20 device has a built-in clock oscillator and uses a 24 MHz external crystal. The VDDIOXTAL supply is the supply associated with the clock input.

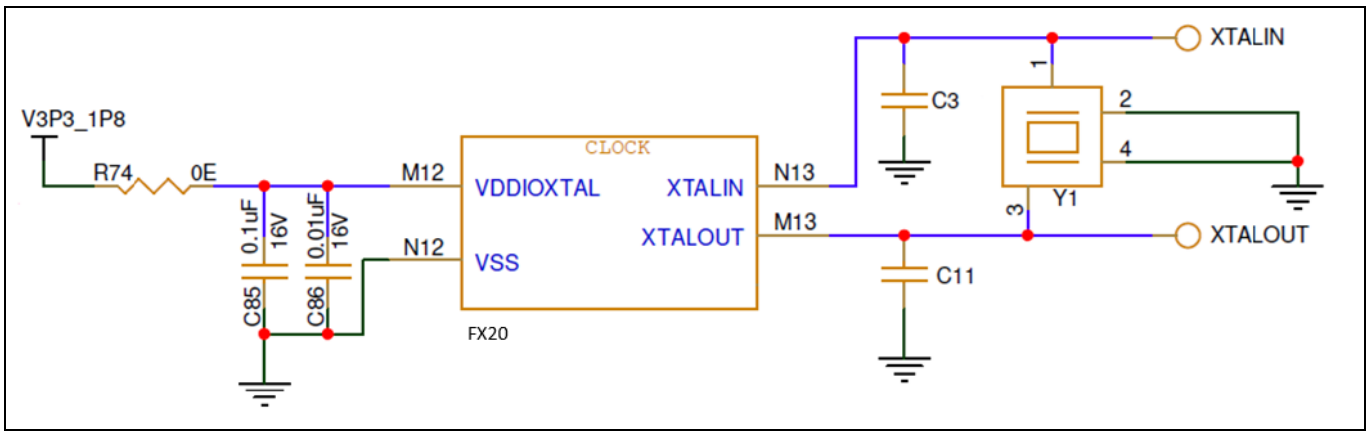


Figure 3 Crystal circuit

Table 3 Crystal requirements

Parameter	Specification	Unit
Frequency	24	MHz
Tolerance	< ±30	ppm
Temp range	–40 to +85	°C
Drive level	Use Equation 1	mW

Note: For more details on crystal specifications, see XTAL/clock specification in the datasheet [2].

The power dissipation of the crystal depends on the following:

- Drive level of the XTALOUT pin (for EZ-USB™ FX20, this depends on VDDIOXTAL)
- Desired frequency (24 MHz)
- Equivalent resistance of the crystal.

$$P = I^2R = \left(\frac{V_x}{|Z|}\right)^2 R = 2[\pi f\ (C_0 + C_L)\ V_x]^2 R$$

Equation 1 Power dissipation of the crystal

Where,

f is the crystal frequency

C_0 is the shunt capacitance of the crystal obtained from the crystal datasheet

C_L is the load capacitance; for CL calculation, see the next section

R is the crystal ESR obtained from the datasheet of the crystal

V_x is the peak voltage on the XTALOUT pin

Using a crystal with a drive level less than the crystal's power dissipation may result in accelerated aging or even burnout of the crystal.

Examples of compatible crystals are shown in Table 4. Only the ECS-240-8-36CKM-TR is characterized with EZ-USB™ FX20, and the remaining crystals are provided as examples using Equation 1.

Table 4 Crystal selection

Device	Max R (Ω) from the datasheet	CL Eqv (pF)	C0 (pF) estimate	Drive level using Equation 1 (µW)	Max drive level (spec) µW
ECS-240-8-36CKM-TR	60	8	5	93.38	100
ABM10W-24.0000MHZ-6-B1U-T3	50	6	2	29.47	100

Note: Do not connect any series resistor to the XTALOUT and XTALIN pins of the crystal. Placing a series resistor will add resistance to the crystal ESR, resulting in increased crystal power dissipation and startup time.

5.1 Crystal effective load capacitor calculation

Load capacitance (C_L) plays a critical role in providing an accurate clock source to EZ-USB™ FX20. Select the capacitors C3 and C11 (as shown in Figure 3) based on the load capacitance value of the crystal.

The load capacitance is calculated using the following equation:

$$C_L = \frac{C_3 * C_{11}}{C_3 + C_{11}} + C_S$$

Equation 2 Load capacitance of a crystal

C_S is the stray capacitance of XTALOUT and XTALIN traces on the PCB. Generally, the value of C_S is approximately 2–5 pF if you follow good layout practice and keep the trace from the crystal to the pins on EZ-USB™ FX20 as short as possible.

For the crystal used in EZ-USB™ FX20 Development Kit, C_L = 8 pF. EZ-USB™ FX20 PCB C_S = 3 pF.
From Equation 2, $C_3 = C_{11}$ = 10 pF.

5.2 Layout consideration

- Place the crystal as close as possible near EZ-USB™ FX20
- Ensure shortest crystal traces to EZ-USB™ FX20
- Guard the XTALIN and XTALOUT traces with GND on the same layer
- Provide solid GND for the entire crystal and the traces in the next layer
- XTALIN and XTALOUT traces should be of the same length.
- Do not to route XTALIN and XTALOUT traces without vias
- Do not place any high-speed signal and reset signal trace near the crystal. If needed because of space constraints, fill the space between high-speed trace and crystal with ground

See the EZ-USB™ FX20 DVK board layout [14] for reference.

6 High-bandwidth data subsystem (HBWSS) interface

EZ-USB™ FX20 offers a high-bandwidth data subsystem that allows data transfers between LVDS/LVCMOS I/O subsystem and USB 3.2 Gen 2x2 device. High-bandwidth data subsystem I/Os can be configured as LVDS or LVCMOS interfaces. It has two links and each link can be configured independently to support the LVDS interface or LVCMOS parallel interface. Both the links can be merged to operate as a single wide link in either LVDS or LVCMOS mode.

6.1 LVDS mode

The LVDS interface supports only Rx function. It has two links with eight data lanes, one control lane, and one clock lane. The data lanes can be configured as 1, 2, 4, or 8. Each LVDS link has seven LVCMOS control signals, of which three are input only, and the other four are input/output control signals. Gearing ratios of 1:1, 2:1, 4:1, and 8:1 are supported on each link configuration. The gearing ratio indicates the number of bits transferred per data lane and per clock on the interface. LVDS mode also supports wide link with 16 data lanes, one control lane, and two clock lanes. The same clock must be fed to both clock lanes when wide link configuration is used.

The following are general hardware design guidelines for EZ-USB™ FX20's high-bandwidth data subsystem LVDS interface.

- For LVDS operation, VDDIO_P0 and VDDIO_P1 must be kept at 3.3 V. VDDIO_P0_CTRL and VDDIO_P1_CTRL can be at either 1.8 V or 3.3 V depending on the desired CTRL signal logic level
- LVDS signals need 100 Ω termination at the receiver. EZ-USB™ FX20 has on-chip 100 Ω termination. So, no external termination is required
- Maintain the impedance of LVDS differential pairs in PCB within 100 Ω ± 10%
- Keep the impedance of LVCMOS control signals as 50 Ω ± 10%
- Length-match the intra-pair (p and n) differential lines within ± 5 mils
- The maximum clock frequency of the LVDS interface is 625 MHz, and the maximum data rate is 1.25 Gbps. So, at 625 MHz, only gear ratios of 1:1 and 1:2 can be used. All differential lanes on each link should be length-matched to the respective LVDS clock within ± 200 mils. This ensures that the skew between the signals lies within 1% of the total period considering the typical propagation delays for stripline and microstrip traces in PCBs (150 to 200 ps/inch or 0.15 to 0.2 ps/mil)
- In wide link mode, ensure that the same clock is fed as the LVDS clock for both links. Clock from both the links must be length matched with ± 10 mils, and all the differential lanes from both the links should match within ± 200 mils to the LVDS clock
- Ensure that the LVDS lanes do not cross split planes. Otherwise, it will lead to a change in impedance, resulting in signal integrity issues
- For the LVDS lanes, it is recommended to perform signal integrity simulation using the EZ-USB™ FX20 IBIS model and devise a termination
- Link training will help to correct the mismatch of the skew between the clock and data. For more details, see the link initialization section in the datasheet [2]
- To terminate LVDS signals on a connector, use a suitable high-speed connector that supports up to 625 MHz signal frequency

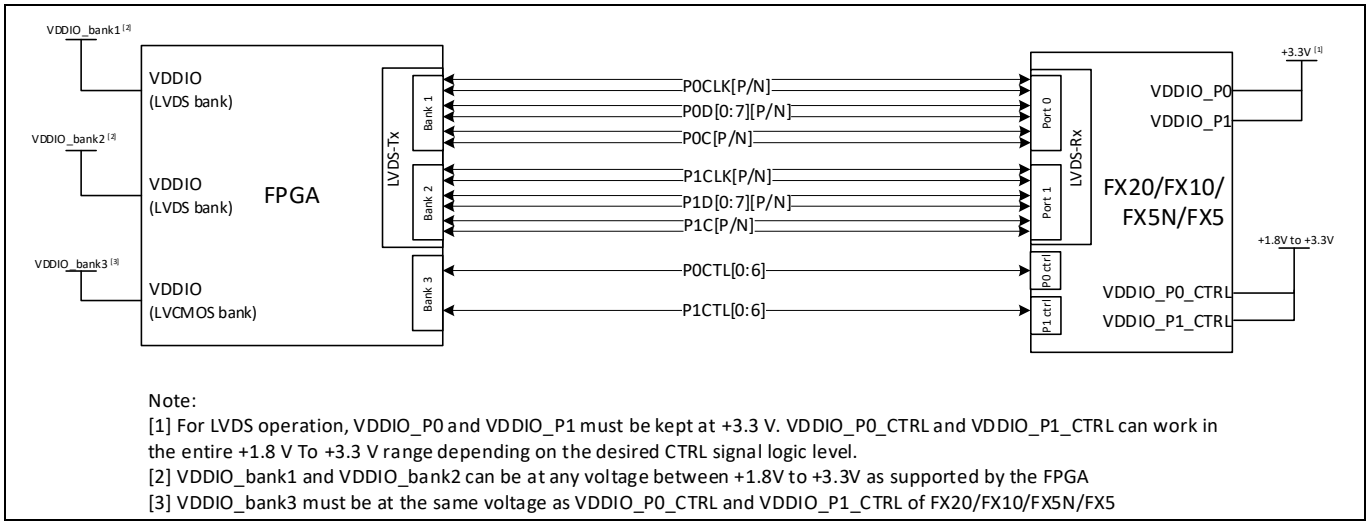


Figure 4 LVDS connection between EZ-USB™ FX20/FX10/FX5N/FX5 and FPGA

6.2 LVCMOS

The LVCMOS parallel interface supports two links each with Rx and Tx interface. Each link contains 16 LVCMOS I/Os and seven control signals. The maximum data rate on each LVCMOS I/O is:

- 160 MHz for SDR and DDR in Rx mode
- 100 MHz SDR and 80 MHz DDR in Tx mode

LVCMOS operation is supported at VDDIO in the range of 1.8 V to 3.3 V.

The following are some general design guidelines for EZ-USB™ FX20's high-bandwidth data subsystem LVCMOS interface.

- Maintain the impedance of all LVCMOS signals within 50 Ω ± 10%
- Length-match all LVCMOS signals to the clock within 500 mils
- In wide link mode, ensure that the same clock is fed to the clock input of both links. Clock from both the links must be length-matched with ± 10 mils and all the signals from both the links should be matched within 500 mils to the clock

Note: For using both LVDS and LVCMOS modes in the same design, follow the length-matching criteria of both modes. For more details, see the DVK layout.

Note: The I/O mappings are different between LVCMOS SDR and DDR modes. See the "Pin Definition" section in the datasheet [2].

7 USB

7.1 USB 20 Gbps

EZ-USB™ FX20 has an integrated USB 3.2 Gen 2x2 20 Gbps PHY that allows connection to a USB-C connector directly. Ensure that the following are taken care of in the design.

- Minimize the trace length of USB lines as much as possible (< 3 inches). Route these first to ensure certain recommendations on this list are achievable. Long traces affect the transmitter quality and introduce intersymbol interference (ISI) on the receive side
- USB signals must refer to the solid ground plane on the PCB
- Length-match the intra-pair (p and n) differential lines within +/- 5 mils
- The polarity can be swapped on the USB Tx and Rx differential pairs. Polarity detection is done automatically by the USB 3.2 PHY during link training and does not require any additional changes to the device firmware. Given the different USB connectors pinouts, the polarity inversion mechanism can be used to ensure that USB traces do not cross each other
- USB3 traces require additional series AC coupling capacitors (0.1 µF) on the Tx lines. See in Figure 5, capacitors C6 and C7 are the AC coupling capacitors placed in the DVK on the TX1 line. Similarly, AC coupling capacitors are present on the TX2 line in the bottom side of the PCB. No AC coupling capacitors are required on the Rx lines

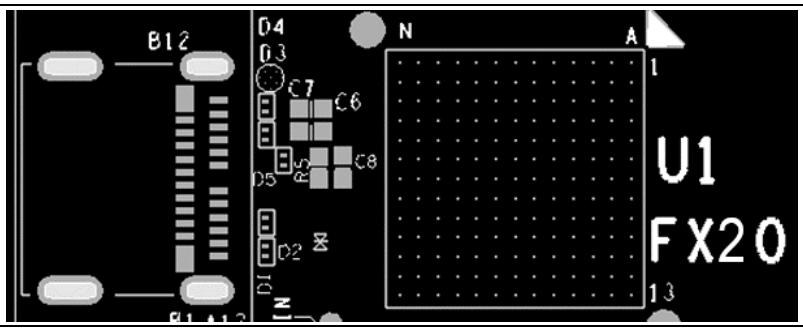


Figure 5 Tx capacitors C6 and C7 placed symmetrically in the EZ-USB™ FX20 DVK layout

- Anti-pads are required underneath the area in the top layer with wider copper pads than the USB signal trace width. See Figure 6: Red is layer 1 and Green is layer 2. Anti-pads are provided under USB-C connector pins, AC coupling capacitors, and ESD diodes. This reduces reflection on the SuperSpeed signals by maintaining the impedance. It is mandatory to provide the ground reference on the layer, which is immediate to the solid GND layer. Place AC capacitors near to USB connector only if the host and device are connected through the cable. This helps to avoid the cable noise reaching to EZ-USB™ FX20 device. Place AC capacitors near EZ-USB™ FX20 if the latter is connected to the hub or another embedded controller on the same PCB
- If the silicon used in the design has a B0 suffix after the part number such as CYUSB4024B0, the RESREF pin K5 should have the 6.04 kΩ ± 1% resistor pull-down to GND as DNP. If there is no B0 suffix on the part number, the RESREF pin K5 should have a 6.04 kΩ ± 1% resistor pull-down to GND. This resistor is a termination for the USB 2.0 PHY

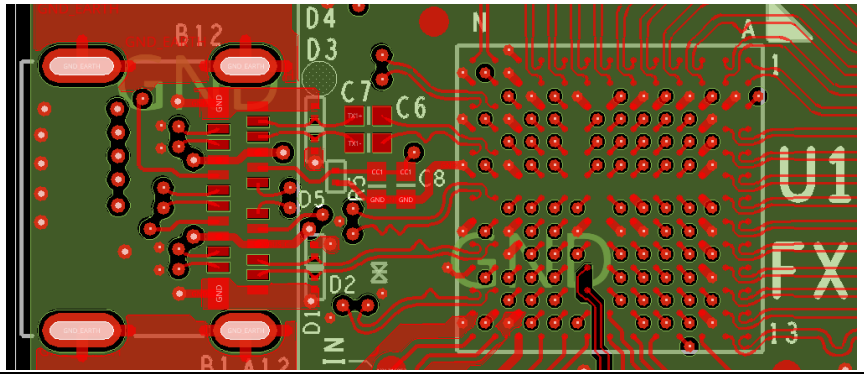


Figure 6 Anti-pad in USB layout

- Keep the USB signal line impedance at 90 Ω differential (±5%)
- Fill the space between the two differential pairs with the ground. Maintain a minimum of 2 W space between the ground and the differential pairs, where W = trace width
- Connect at least one bulk capacitor of 10 µF at the USB-C VBUS pin along with the ceramic capacitors between 22 nF and 100 nF. All capacitors should be rated 10 V or higher to ensure at least 50% derating. The bulk capacitor will maintain the voltage levels in case of a transient current requirement
- FX20 can detect the USB-C connector orientation. It needs an external 5.1k ± 1% pull-down resistor on each CC line. After detection, FX20 will swap the USB SuperSpeed lanes thus eliminating the need for an external MUX. Connect 5.1 kΩ ± 1% pull-down resistor on the CC1 and CC2 lines
- VBUSDETECTn pin of EZ-USB™ FX20 allows for self-power mode operation. This pin, however, is a negative logic pin. When a host is connected, the VBUSDETECTn will go low, indicating a connection
- Use appropriate ESD diodes near the USB-C connector, as shown in Figure 7
- Shield pins on the USB-C receptacle should be terminated to the ground with a parallel LC (or) RC circuit to avoid EMI/EMC issues. It is recommended to use an RC circuit, as shown in Figure 7
- Use USB-IF certified USB-C connectors in the design for optimum performance
- Ensure that the USB-C connector PCB mounting pins are longer than the PCB thickness to ensure robust connection with the cable

See the EZ-USB™ FX20 DVK board [14] file for more details.

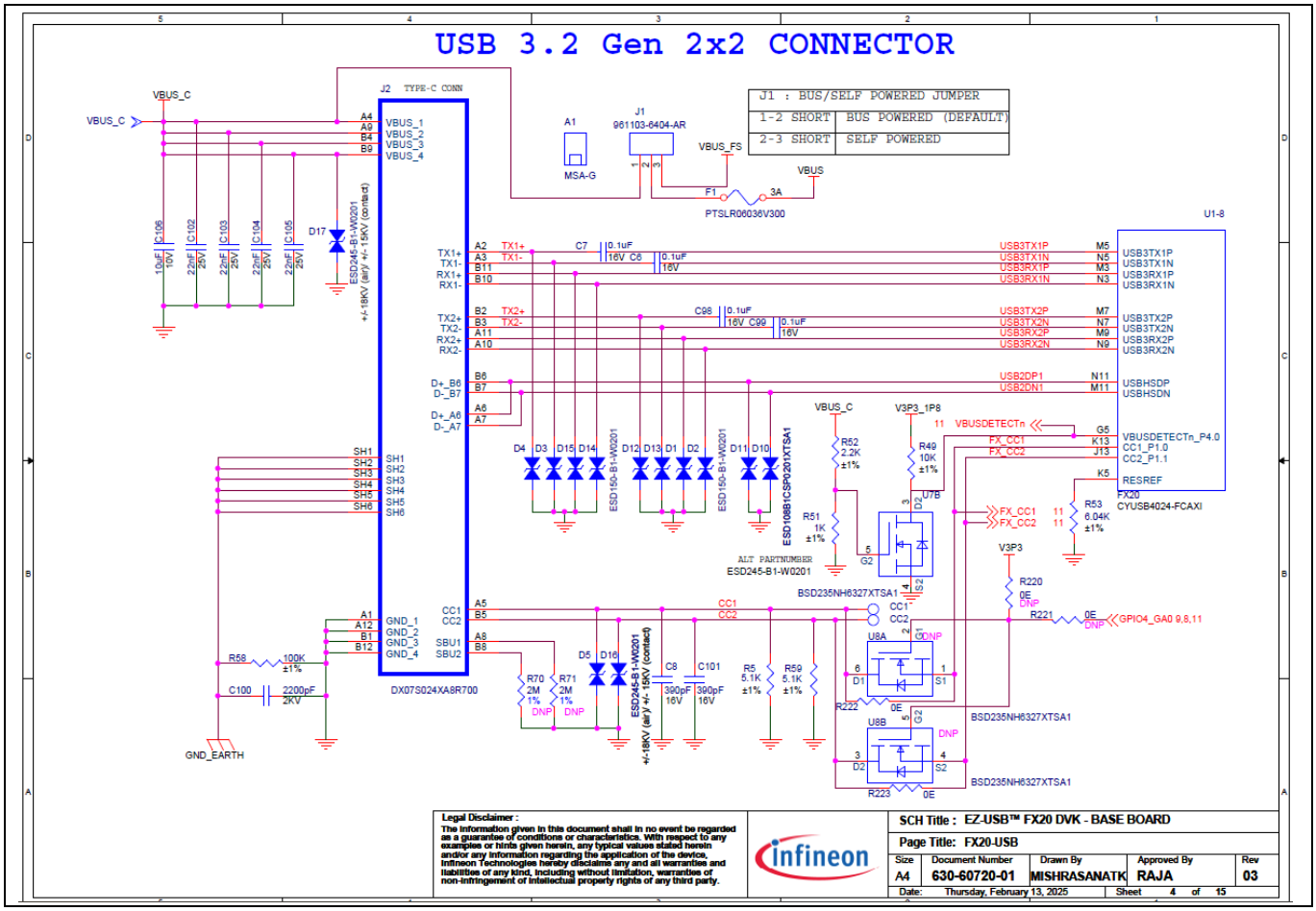


Figure 7 EZ-USB™ FX20 interface with USB-C connector

7.2 USB Full-Speed

EZ-USB™ FX20 has a separate USB Full-Speed interface that can be used to log messages for debugging purposes. Use a Micro-B or USB-C Full-Speed connector for this purpose. Ensure to maintain 90 Ω ± 5% impedance for the data lines. If a USB-C Full-Speed connector is used in the design, use 5.1 kΩ ± 5% on the CC lines. Shield pins on the USB-C receptacle should be terminated to the ground with a parallel LC (or) RC circuit to avoid EMI/EMC issues. It is recommended to use an RC circuit, as shown in Figure 8.

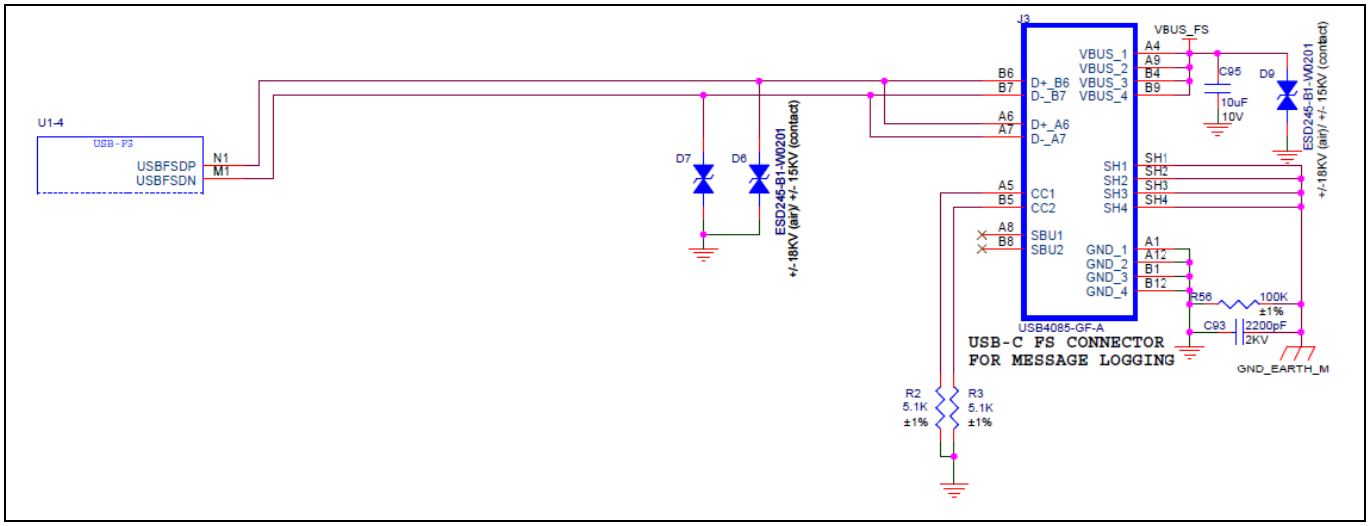


Figure 8 EZ-USB™ FX20 Full-Speed interface with USB-C connector

7.3 USB-C cable

Use a certified USB 10 Gbps 2 lane cable for achieving 20 Gbps throughput while using EZ-USB™ FX20 silicon. See the cable part number mentioned in the DVK schematic for more details.

7.4 USB host controller

EZ-USB™ FX20 DVK is tested with various Intel USB 3.2 Gen 2x2 host controllers and ASMedia ASM3242 host controller.

8 Low-speed peripherals

EZ-USB™ FX20 has 7 SCBs, each can be configured as SPI, UART, or I2C. Apart from this, other peripherals are PDM, QSPI, CAN, and UART are also supported. See the “Pin definition” section in the datasheet [2].

8.1 I²C interface

EZ-USB™ FX20 has an I²C interface compatible with the I²C bus specification. The power supply for the I²C interface is VDDIO, which is the power domain for all the other low-speed peripherals. EZ-USB™ FX20 has one main I²C interface and two-port I²C interfaces.

- P10.0 and P10.1 are the main I²C of the chip. They are overvoltage-tolerant up to 5 V
- P0.0 and P0.1 are Port0 I²C interface
- P8.6 and P8.7 are Port1 I²C interface

The bus frequencies supported by the I²C controller are 100 kHz, 400 kHz, and 1 MHz.

All the I2C interfaces can operate at 1.8 V or 3.3 V. A 2 kΩ ± 1% pull-up to VCCIO voltage is recommended on all the I²C lines.

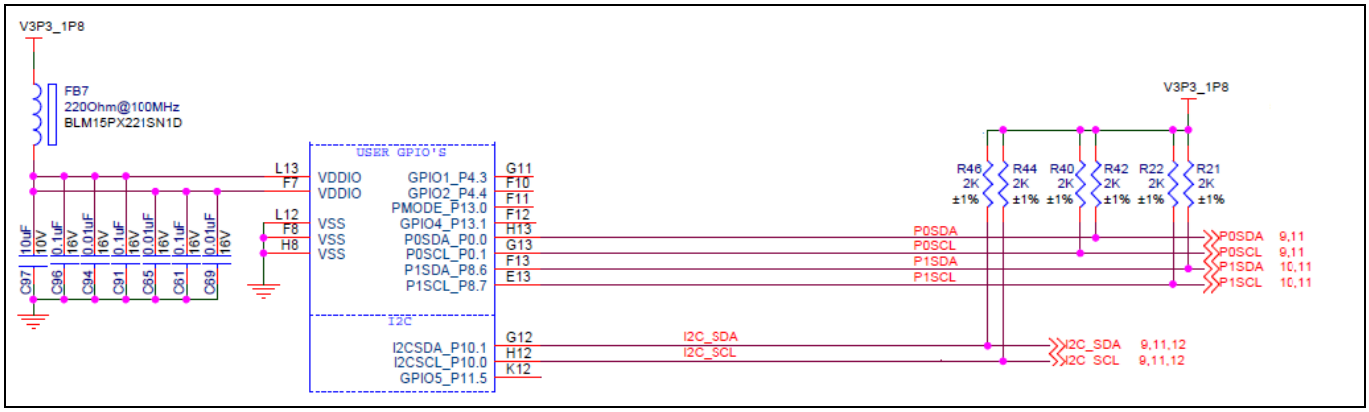


Figure 9 I²C configuration

8.2 SWD/JTAG

EZ-USB™ FX20 has a debug access port (DAP) as the interface for device programming and debugging. An external programmer or debugger can communicate with the DAP through the device Serial Wire Debug (SWD) or JTAG interface pins. Through the DAP (and subject to restrictions), the host can access the device memory and peripherals and the registers in both CPUs.

EZ-USB™ FX20 has a JTAG interface to provide a standard five-pin interface for connecting to a JTAG debugger. A 10 kΩ external pull-up resistor is recommended on the JTAG signals TDI, TDO, TMS, and TRST# pins. EZ-USB™ FX20 also supports boundary scan. See the datasheet [2] for more details.

EZ-USB™ FX20 also supports SWD to program the bootloader and perform debugging.

8.3 I²S

EZ-USB™ FX20 has two I²S interfaces that have independent transmitters or receivers which can operate in master or slave mode. This enables to connect audio transmitters and receivers with an I²S interface directly to EZ-USB™ FX20. I²S Tx signals consist of SCKOUT, TXWS, TXMCLK, and SDO. I²S Rx signals consist of SCKIN, RXWS, RXMCLK, and SDI. It is recommended to length-match the I²S signals within 1000 mils.

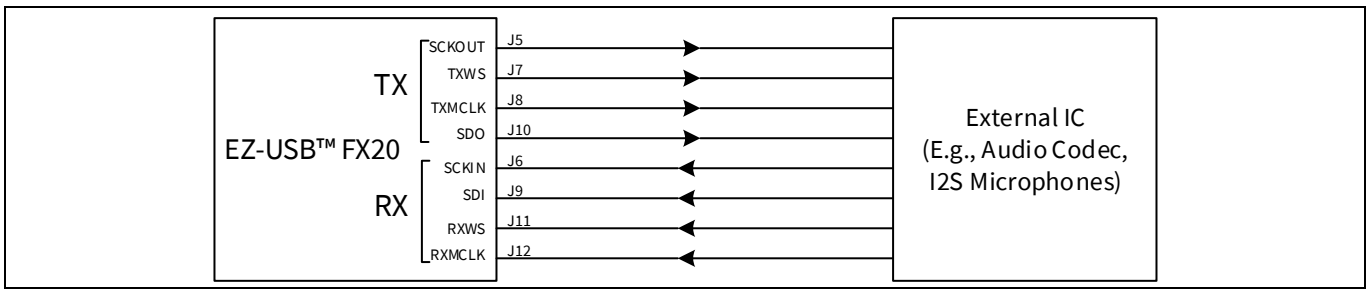


Figure 10 Interfacing I²S audio device with EZ-USB™ FX20

8.4 PDM

EZ-USB™ FX20 has one PDM to PCM decoder. Up to two microphones can be connected to the same PDM data line. Ensure to follow these points in the layout.

- If a single microphone is used, length-match the data to clock within ± 25 mils
- If two microphones are used in the design, length-match the data to the clock for each microphone separately. Figure 11 shows how to connect two microphones to EZ-USB™ FX20. Length-match Cx and Dx, Ca and Da, Cb, and Db individually, all within ± 30 mils

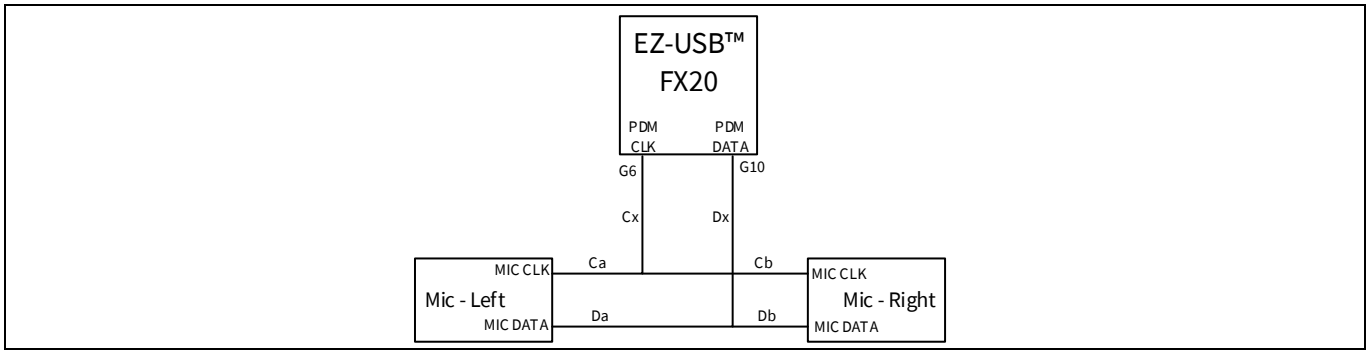


Figure 11 Connecting two microphones to EZ-USB™ FX20

8.5 Quad SPI

EZ-USB™ FX20 supports single, dual, quad, dual-quad, and octal SPI configurations. External SPI flash can be used to store FPGA configuration file. It supports up to four external memory devices. SPI clock operates at up to 80 MHz. All the data signals should be length-matched to the clock within 1000 mils.

See the EZ-USB™ FX20 DVK schematic for more details on connecting dual/quad SPI flashes.

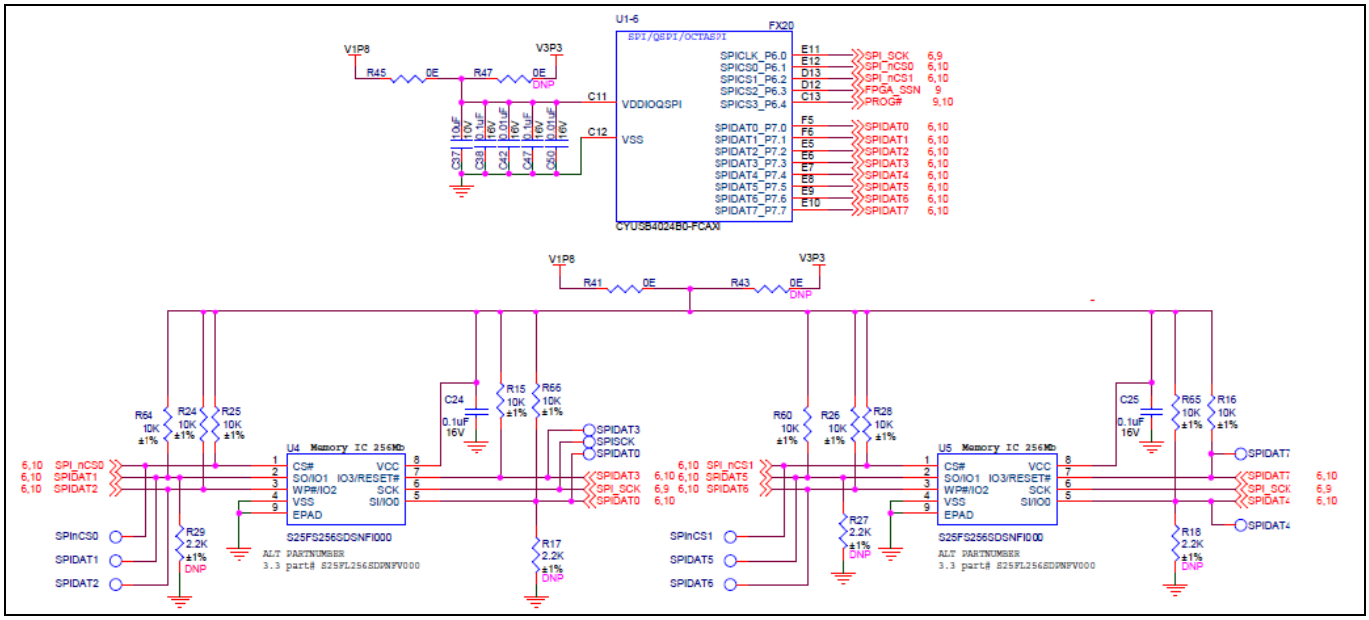


Figure 12 Interfacing two QSPI flash with EZ-USB™ FX20

8.6 CAN FD

External CAN device can be interfaced to EZ-USB™ FX20 using a CAN transceiver as shown below. Maintain trace impedance of CANH and CANL at 120 Ω. The FX20 CAN FD interface supports 1.8 V to 3.3 V. Ensure the VIO voltage of the CAN transceiver matches the VDDIO voltage of FX20. See the datasheet [2] for more details.

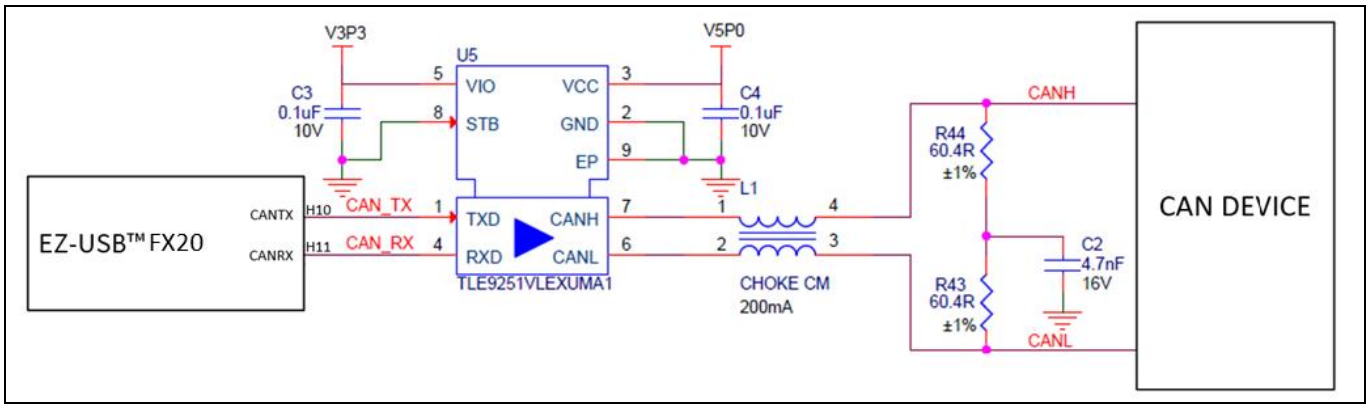


Figure 13 Interfacing CAN device with EZ-USB™ FX20

9 Booting

EZ-USB™ FX20 operates only on two boot modes; USB boot and internal flash boot based on the voltage level on the PMODE pin.

Table 5 PMODE signal setting

PMODE	Boot from
GND	Internal flash
VCCIO	USB boot

Note: Whenever PMODE selection changes, press the RESET button or power cycle the EZ-USB™ FX20 device.

10 EMI and ESD considerations

All pins of EZ-USB™ FX20 support ±2.0 kV human body model (HBM)-based on JESD22-A114 Specification.

Provide the IEC protection at the system level. Provide additional protection to all pins with user interface by using high-performance and low-capacitance external ESD devices. See Figure 7 for Infineon ESD diodes used on the USB lines of the USB 20 Gbps connector.

Regarding EMI, all signal and clock traces emit electromagnetic (EM) radiation when they switch from one level to another. To meet the various standards in different countries, minimize these emissions. Several techniques can be implemented during the design to lower EM emissions in all high-speed signals (USB and LVDS):

- Consider placing the power and ground planes as the outside layers with signal layers underneath
- Always have solid copper fills beneath integrated circuits and clocks
- Ensure an adequate ground return path for all the signals
- Minimize the trace length of high-speed and high-current traces

11 Generic electrical design considerations

See Appendix A – PCB layout tips for general information on PCB layout techniques.

- Place the capacitor used in the RC reset circuitry as close as possible to the reset pin of EZ-USB™ FX20
- Use split planes on the power layer for different power domains
- Keep the power traces away from high-speed data and clock lines
- Power trace widths should be ≥25 mils to reduce the inductance
- Keep power traces as short as possible. Use larger vias (at least 30-mil pad, 15-mil hole) on power traces
- Avoid any split in the immediate plane under the USB/LVDS lines. The presence of a split under the USB/LVDS trace will result in a variation of characteristic impedance at that point
- Keep trace spacing between differential pairs consistent to avoid impedance mismatches as shown in Figure 14

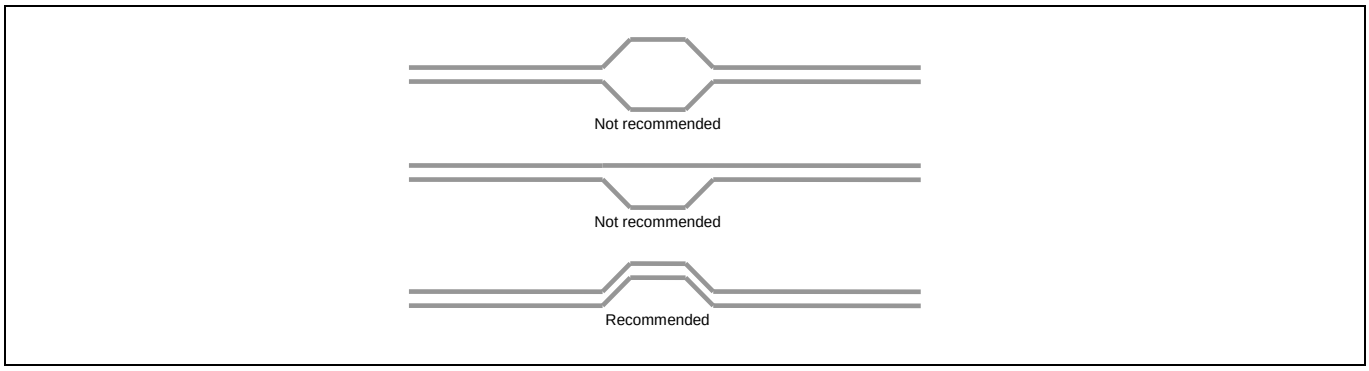


Figure 14 Differential pairs impedance matching techniques

- Route all USB/LVDS signal lines entirely over a solid ground plane on an adjacent layer. Splitting the ground plane underneath the USB/LVDS signals increases the loop inductance, which introduces impedance mismatches and increases electrical emissions. See Figure 15

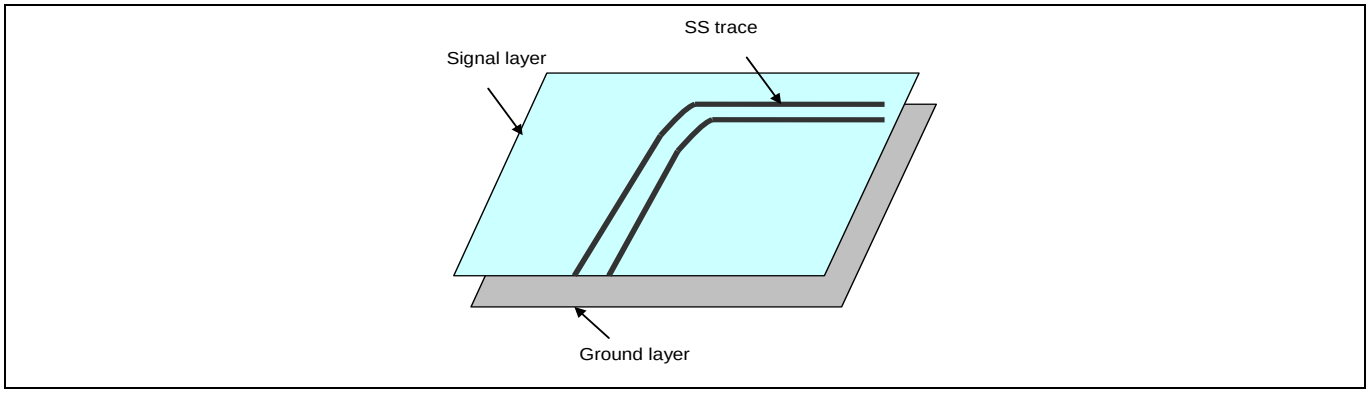


Figure 15 Solid ground plane under the SuperSpeed signal

- Whenever two pairs of USB/LVDS traces cross each other in different layers, run a ground layer between the two USB signal layers. See Figure 16

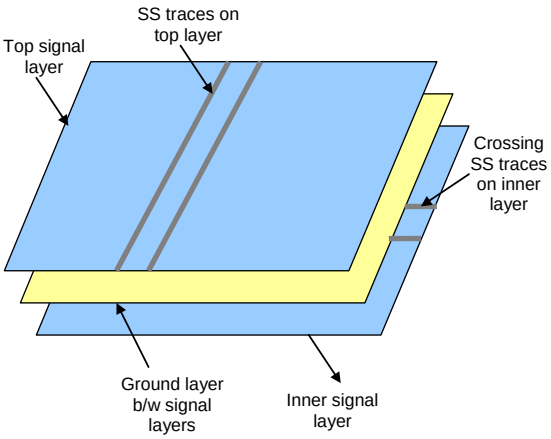


Figure 16 Ground insertion

- On the USB/LVDS signal lines, use as few bends as possible. Do not use a 90-degree bend. Use 45-degree or rounded (curved) bends if necessary. See Figure 17

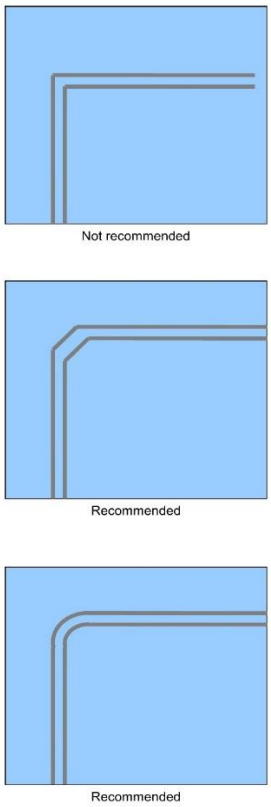


Figure 17 USB signal bends

- Match intra-pair differential trace lengths within 0.12 mm (5 mils). Always adjust for USB signal trace lengths near the USB receptacle and not near the device. Always adjust the length at the mismatched ends. An example of length-matching for SuperSpeed signals is shown in Figure 18

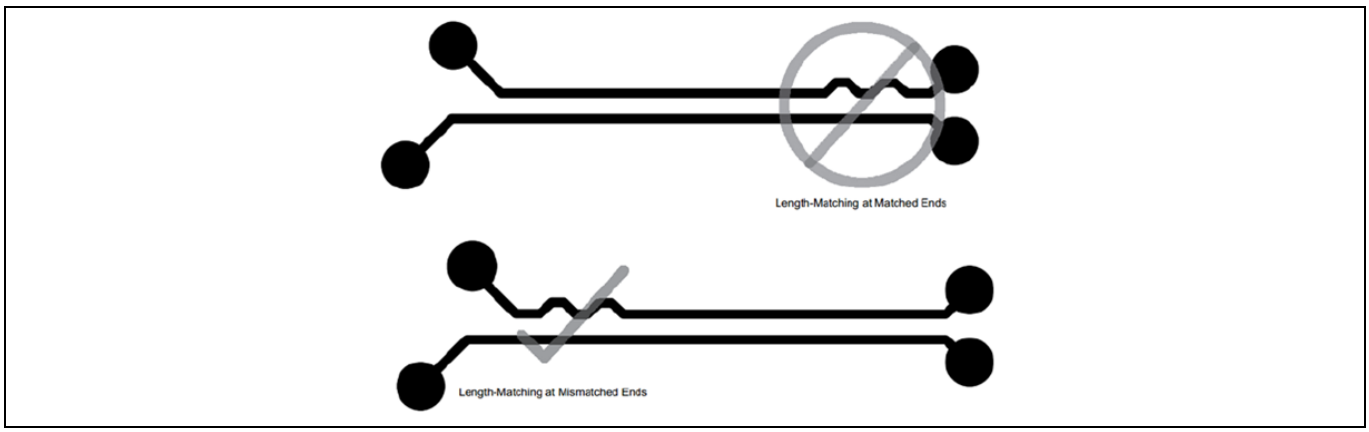


Figure 18 Intra-pair differential signal length matching

- There are different routing methods for length matching: single arc routing and serpentine routing methods. See Figure 19 and Figure 20 for single arc routing and serpentine routing respectively

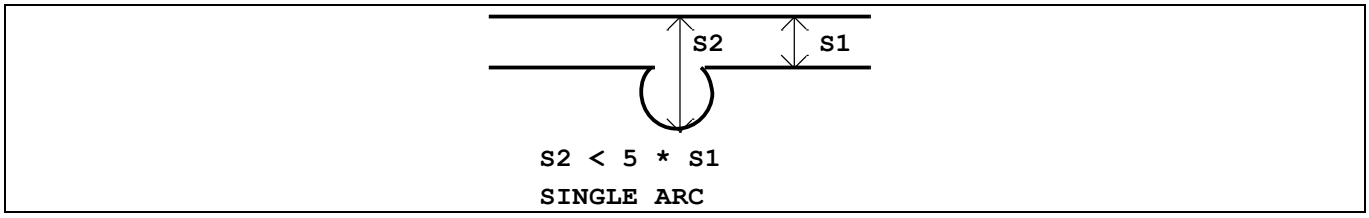


Figure 19 Single arc routing

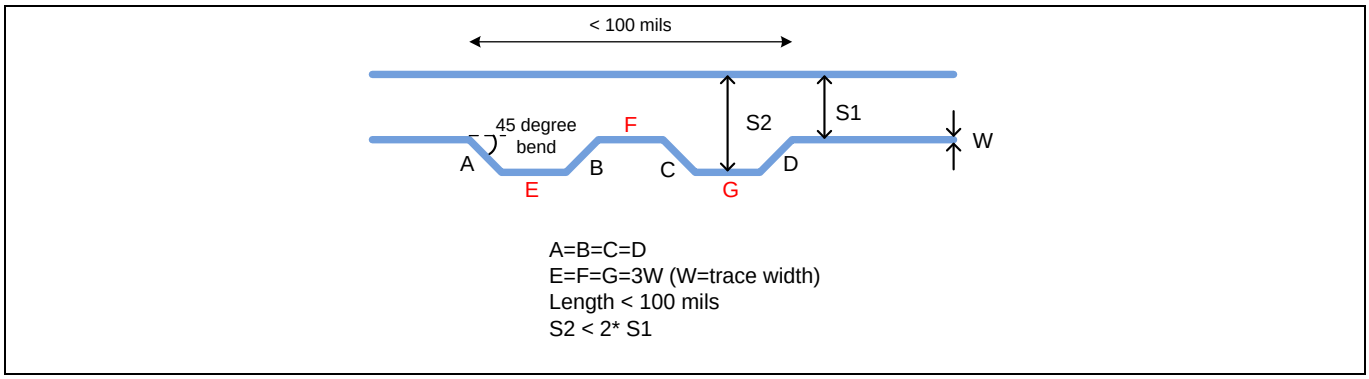


Figure 20 Serpentine routing

- The number of layers on the PCB should at least be four
- If signal routing has to be changed to another layer, maintain continuous grounding to ensure uniform impedance throughout. To achieve this, place ground vias next to signal vias. Keep at least 40 mils as the distance between signal and ground vias. See Figure 21

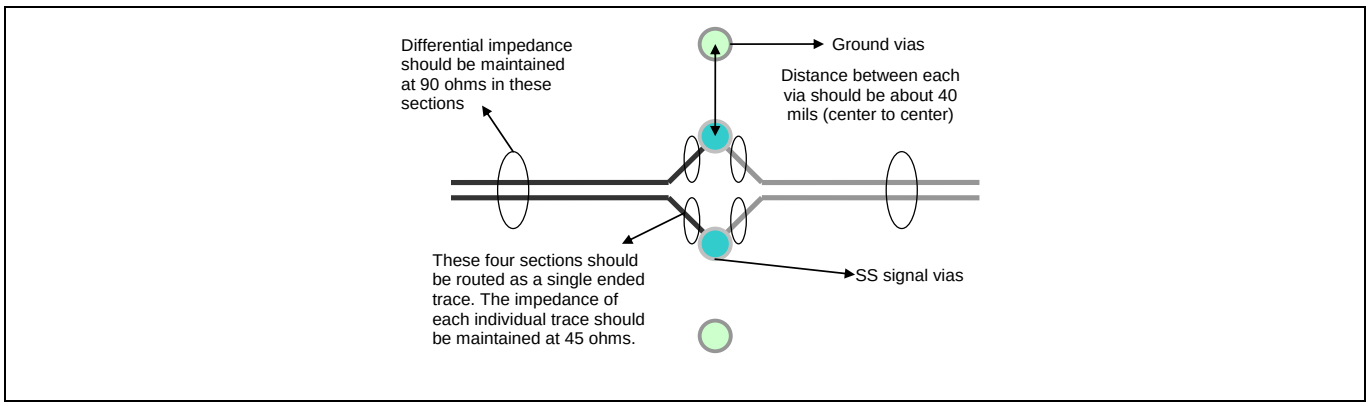


Figure 21 Ground vias

- Maintain constant trace width in differential pairs to avoid impedance mismatches as shown below:

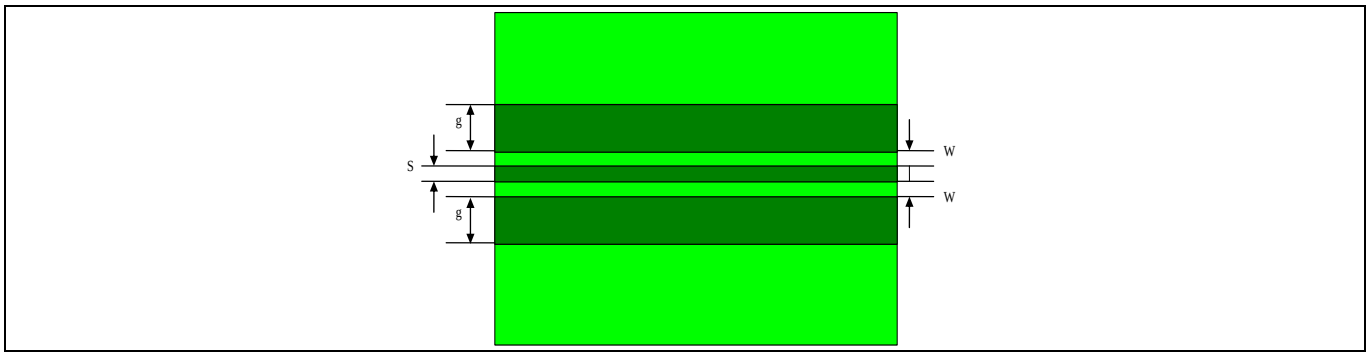


Figure 22 Differential pairs placements

- Avoid stubs on all high-speed lines. If pads are needed on the lines for probing purposes, they should not extend out of the trace in the form of a stub. See Figure 23

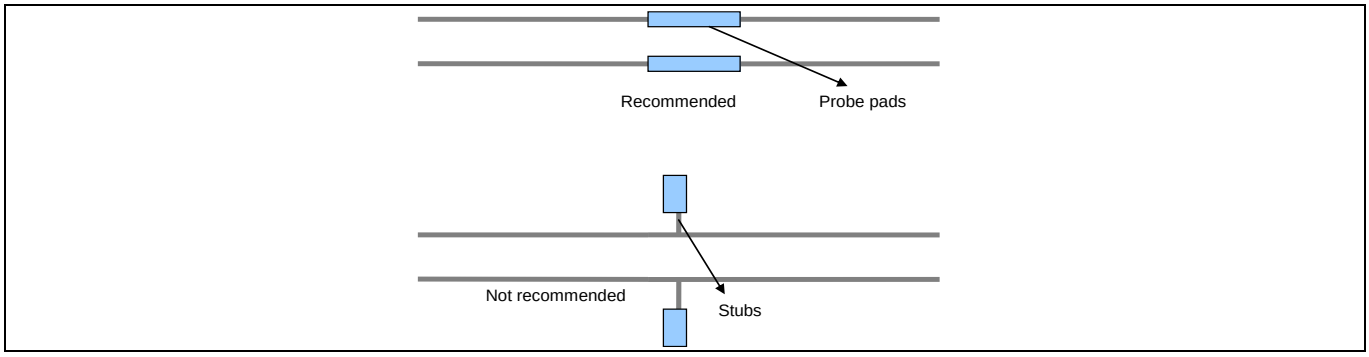


Figure 23 Probing pads placement

- Ensure that voids for vias on the high-speed signal lines are common for the differential pair. A common void, as shown in Figure 24, maintains better impedance matching in comparison to separate vias

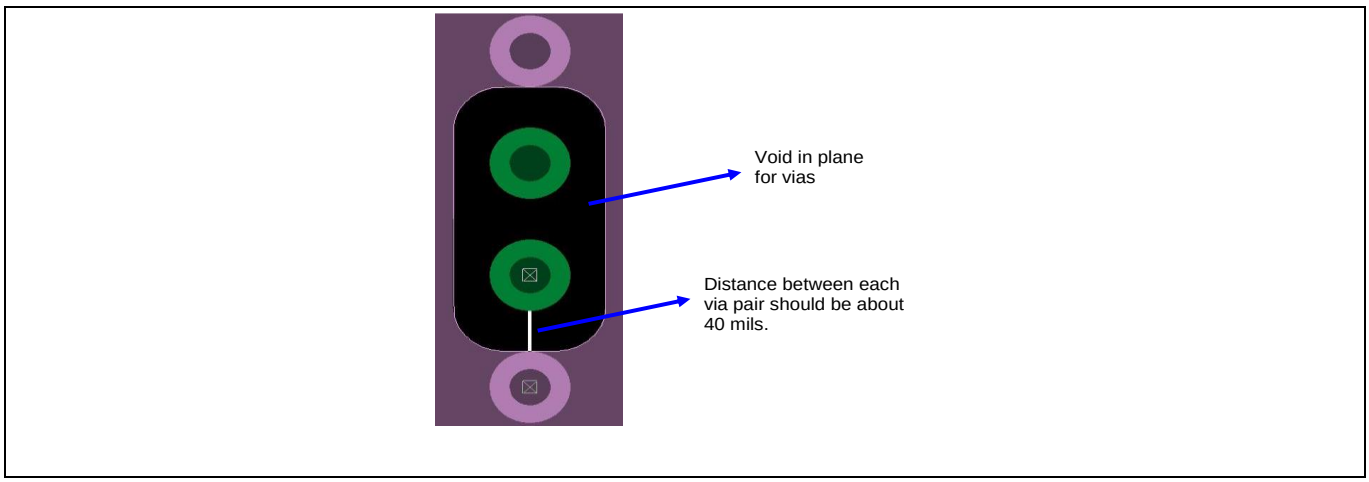
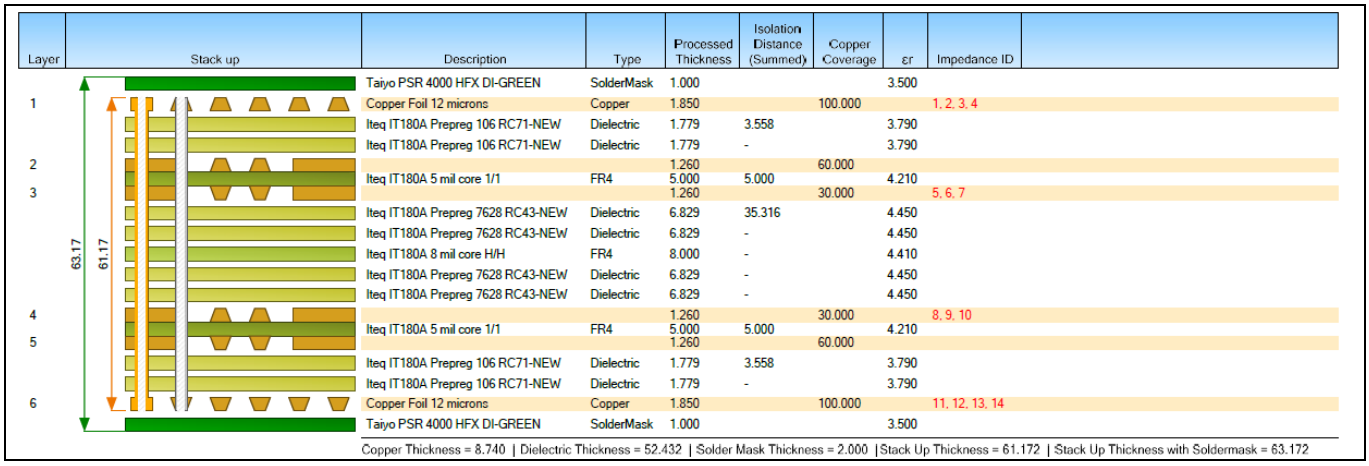


Figure 24 Void vias placement for high-speed differential traces

- To avoid cross-talk, do not place the differential pairs close to other differential pairs, clock signals, or high-speed signals. It is recommended to maintain a 3x distance with other differential pair and other signals where ‘x’ is the width of the signal trace

Figure 25 shows an example of a six-layer stack up from the EZ-USB™ FX20 development kit. This is captured using the Polaris tool.



Layer	Stack up	Description	Type	Processed Thickness	Isolation Distance (Summed)	Copper Coverage	εr	Impedance ID
		Taiyo PSR 4000 HFX DI-GREEN	SolderMask	1.000			3.500	
1		Copper Foil 12 microns	Copper	1.850		100.000		1, 2, 3, 4
		Iteq IT180A Prepreg 106 RC71-NEW	Dielectric	1.779	3.558		3.790	
		Iteq IT180A Prepreg 106 RC71-NEW	Dielectric	1.779	-		3.790	
2				1.260		60.000		
		Iteq IT180A 5 mil core 1/1	FR4	5.000	5.000		4.210	
3				1.260		30.000		5, 6, 7
		Iteq IT180A Prepreg 7628 RC43-NEW	Dielectric	6.829	35.316		4.450	
		Iteq IT180A Prepreg 7628 RC43-NEW	Dielectric	6.829	-		4.450	
		Iteq IT180A 8 mil core H/H	FR4	8.000	-		4.410	
		Iteq IT180A Prepreg 7628 RC43-NEW	Dielectric	6.829	-		4.450	
		Iteq IT180A Prepreg 7628 RC43-NEW	Dielectric	6.829	-		4.450	
4				1.260		30.000		8, 9, 10
		Iteq IT180A 5 mil core 1/1	FR4	5.000	5.000		4.210	
5				1.260		60.000		
		Iteq IT180A Prepreg 106 RC71-NEW	Dielectric	1.779	3.558		3.790	
		Iteq IT180A Prepreg 106 RC71-NEW	Dielectric	1.779	-		3.790	
6		Copper Foil 12 microns	Copper	1.850		100.000		11, 12, 13, 14
		Taiyo PSR 4000 HFX DI-GREEN	SolderMask	1.000			3.500	

Copper Thickness = 8.740 | Dielectric Thickness = 52.432 | Solder Mask Thickness = 2.000 | Stack Up Thickness = 61.172 | Stack Up Thickness with Soldermask = 63.172

Figure 25 Stackup details for EZ-USB™ FX20 Development Kit

12 Schematics and layout review checklist

Table 6 and Table 7 list the checklist for all the important guidelines. Respond to each checklist item to determine the extent to which your hardware design meets these guidelines. A design that satisfies all the schematic and layout checklists will definitely work without any system-level hardware issues.

Table 6 Schematics checklist

Sl. no	Schematic checklist	Answer (Yes/No/NA)
1	Are the decoupling capacitors and bulk capacitors connected according to Table 2?	
2	Does the crystal meet the specification in this application note according to Table 3?	
3	Are the ferrite beads connected to the supply pins according to Figure 1?	
4	Do the power-on-reset RC components meet the minimum reset time requirement of >1 µs?	
5	Is a 5.1 kΩ resistor pull-down connected to CC1 and CC2 lines?	
6	Are the I2C lines provided with pull-up resistors to the VDDIO domain?	
7	Does the USB port shield terminate with the RC circuit?	
8	Do the USB traces have an ESD device connected?	
9	Is the VBUSDETECTn pin connected to VBUS through negative logic as shown in Figure 7?	
10	Are the PMODE lines connected to achieve the functionality listed in Table 5?	
11	Does the SPI flash device meet the specification in this application note according to **Section 8.5**?	
12	Do the JTAG lines have pull-up resistors to VDDIO?	
13	Does the VBUS pin of EZ-USB™ FX20 device has overvoltage protection?	
14	Does the VBUS pin of EZ-USB™ FX20 has a 10 µF bulk capacitor?	
15	Does the Tx pins of EZ-USB™ FX20 has an AC (0.1 µF) capacitor?	
16	LVDS mode also supports wide link with 16 data lanes, 1 control lane, and 2 clock lanes. Check if both clock lanes are connected between LVDS TX and EZ-USB™ FX20	

Table 7 Layout checklist

Sl. no	Layout checklist	Answer (Yes/No/NA)
1	Is the crystal placed close to the chip (less than 2 cm)?	
2	Are the decoupling capacitors and bulk capacitors placed close to FX20 power pins?	
3	Are the clock traces routed away from high-speed data lines and power lines?	
4	Are the power traces routed away from high-speed data lines and clock lines?	

Schematics and layout review checklist

Sl. no	Layout checklist	Answer (Yes/No/NA)
5	Is the capacitor in the RC reset circuitry placed close to the reset pin of EZ-USB™ FX20?	
6	Do the USB SS, HS, and FS signal lines have a 90 Ω differential impedance?	
7	Are the USB SS, HS, and FS signal lines intra-pair match done?	
8	Are the USB data lines provided with a solid ground plane underneath?	
9	Are the SS traces provided with guard traces along the USB data trace with stitching vias?	
10	Is an anti-pad provided on the pins and components with high-speed routing?	
11	Do the USB traces have few bends and no 90-degree bend?	
12	Is it ensured that SS and HS USB traces are routed with consistent trace spacing?	
13	Are the USB traces kept less than 3 inches?	
14	Is it ensured that there are no stubs on all the USB traces?	
15	Do the LVDS signal lines have 100 Ω differential impedance?	
16	Do the LVCMOS signal lines have 50 Ω single-ended impedance?	
17	Are the LVDS signals referring to the solid GND plane?	

13 Summary

The developer must consider the recommended practices for EZ-USB™ FX20 hardware design and the critical items discussed in this document.

14 Appendix A – PCB layout tips

There are many classic techniques for designing PCBs for low noise and EMC. A few of these techniques include:

- **Multiple layers:** Although they are more expensive, it is best to use a multi-layer PCB with separate layers dedicated to the ground and power supplies. This gives good decoupling and shielding effects
- **Component position:** Separate the different circuits on the PCB according to their electromagnetic interference (EMI) contribution. This will help reduce cross-coupling on the PCB. For example, separate noisy high-current circuits, low-voltage circuits, and digital components
- **Ground and power supply:** There should be a single point for gathering all ground returns. Avoid ground loops, or minimize their surface area. All component-free surfaces of the PCB should be filled with additional grounding to create a shield, especially when using a two-layer PCB
- The power supply should be close to the ground line to minimize the area of the supply loop. The supply loop can act as an antenna and can be a major emitter or receiver of EMI
- **Decoupling:** The standard decoupler for external power is a 100 µF capacitor. Supplementary 0.1 µF capacitors should be placed as close as possible to the GND and supply pins of the device to reduce high-frequency power supply ripple

Generally, decouple all sensitive or noisy signals to improve electromagnetic compatibility (EMC) performance. Decoupling can be both capacitive and inductive.

- **Signal routing:** When designing an application, the following areas should be closely studied to improve EMC performance:
  - Noisy signals, for example, signals with fast edge times
  - Sensitive and high-impedance signals
  - Signals that capture events, such as interrupts and strobe signals

To increase the EMC performance, keep trace lengths as short as possible and isolate traces with V_{SS} traces. To avoid cross-talk, do not route them near to or parallel to other noisy and sensitive traces.

15 Appendix B – Troubleshooting

15.1 EZ-USB™ FX20 device not enumerating

Many factors contribute to the EZ-USB™ FX20 enumeration issue. A few of these points include:

- **PMODE pins:** Check if the PMODE pin is properly configured according to the application
- **USB-C receptacle to EZ-USB™ FX20 device connections:** Connect the Tx pins of the EZ-USB™ FX20 device to the Tx pins of the USB-C receptacle. Connect the Rx pins of the EZ-USB™ FX20 device to the Rx pin of the USB receptacle. Check if CC lines are terminated with a 5.1 KΩ resistor
- **Hub/embedded controller to EZ-USB™ FX20 device connections:** Some applications require the EZ-USB™ FX20 device to be connected to downstream ports of the hub (or) embedded controller in the same PCB. In these cases, EZ-USB™ FX20 device Tx pins should be connected to Rx pins of the downstream ports (or) Rx pins of the embedded controller. EZ-USB™ FX20 device RX pins should be connected to the TX pins of the downstream ports (or) Tx pins of the embedded controller

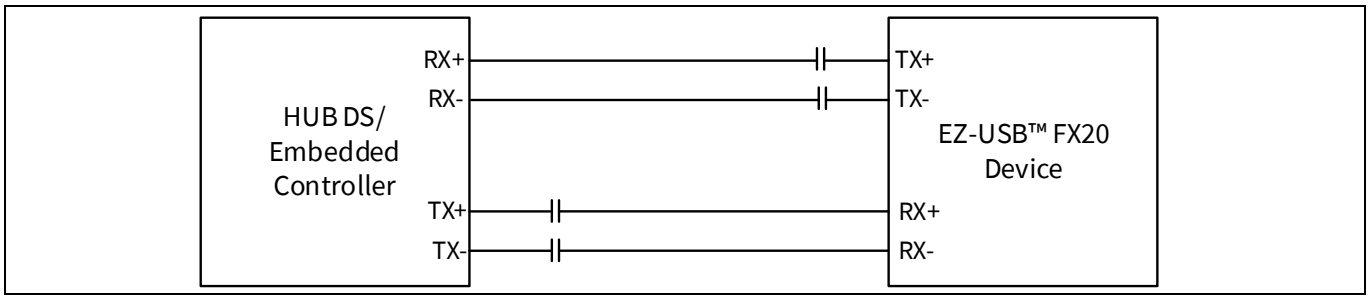


Figure 26 Hub/embedded controller to EZ-USB™ FX20 device connections

- **Power domain isolation:** Ensure that EZ-USB™ FX20 power supplies are isolated and connected with ferrite beads. Also, the source of these supplies should have noise/ripple less of than 100 mV
- **TX AC capacitor:** Connect the AC capacitor on the Tx lines of the EZ-USB™ FX20 device. This will prevent the common-mode noise from the cable/host from entering EZ-USB™ FX20 device Tx lines. The AC capacitor should be near the Type-C receptacle for the application that uses the Type-C receptacle; the AC capacitor should be near the EZ-USB™ FX20 Tx pins for the application which uses the hub/embedded controller

References

For a complete and updated list of EZ-USB™ FX20 code examples, visit our GitHub repository. For more EZ-USB™ FX20 related documents, visit the EZ-USB™ FX20 webpage.

Application note

[1] Infineon Technologies AG: *AN237841 – Getting started with EZ-USB™ FX20/FX10/FX5N/FX5*

Datasheet

[2] Infineon Technologies AG: *002-33684: CYUSB402x EZ-USB™ FX20 USB 20 Gbps peripheral controller*

[3] Infineon Technologies AG: *002-40837: CYUSB401x EZ-USB™ FX10 USB 10 Gbps peripheral controller*

[4] Infineon Technologies AG: *002-41019: CYUSB328x EZ-USB™ FX5N USB 10 Gbps peripheral controller*

[5] Infineon Technologies AG: *002-40850: CYUSB308x EZ-USB™ FX5 USB 5 Gbps peripheral controller*

Reference manual

[6] Infineon Technologies AG: *002-36077: EZ-USB™ FX20 USB 3.2 Gen 2x2 device controller architecture reference manual*

Programming specifications

[7] Infineon Technologies AG: *002-37666: CYUSB401x, CYUSB308x EZ-USB™ FX20 programming specifications*

Development kits

[8] Infineon Technologies AG: *KIT_FX20_FMC_001: EZ-USB™ FX20 Development Kit*

[9] Infineon Technologies AG: *KIT_FX10_FMC_001: EZ-USB™ FX10 Development Kit*

[10] Infineon Technologies AG: *KIT_FX5N_FMC_001: EZ-USB™ FX5N Development Kit*

[11] Infineon Technologies AG: *KIT_FX5_FMC_001: EZ-USB™ FX5 Development Kit*

[12] Infineon Technologies AG: *DEMO_FX20_MIPI_001: EZ-USB™ FX20 MIPI Camera Demo Kit*

Tools

[13] Infineon Technologies AG: *EZ-USB™ FX Control Center*; Available online

Product webpages

[14] Infineon Technologies AG: *EZ-USB™ FX20 webpage*; Available online

[15] Infineon Technologies AG: *EZ-USB™ FX10/FX5N webpage*; Available online

[16] Infineon Technologies AG: *EZ-USB™ FX5 webpage*; Available online

Revision history

Document revision	Date	Description of changes
**	2025-03-13	Initial release

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2025-03-13

Published by

Infineon Technologies AG

81726 Munich, Germany

© 2025 Infineon Technologies AG. All Rights Reserved.

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

002-38422 Rev. **

Important notice

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Warnings

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.