EZ-USB™ FX2G3 hardware design guidelines and schematic checklist

About this document

Scope and purpose

This application note discusses the recommended practices for EZ-USB™ FX2G3 hardware design and the critical items that a designer must consider. EZ-USB™ FX2G3 is the USB Hi-Speed (HS) peripheral controller that is going to replace FX2LP and supports 480 Mbps bandwidth. With its highly integrated and flexible features, developers can add USB HS functionality to any system using EZ-USB™ FX2G3.

Intended audience

This document is intended for anyone who uses the EZ-USB™ FX2G3 peripheral controller.

Keypoints

- Explains recommended hardware design practices and critical schematic checks for reliable EZ-USB™ FX2G3 implementations
- Describes power architecture, decoupling, clocking, and reset considerations affecting signal integrity and system stability
- Details USB HS, LVCMOS, and peripheral interface layout guidelines to support robust high-bandwidth data transfer
- Provides EMI, ESD, and PCB layout techniques to improve compliance and reduce system-level issues
- Summarizes schematic and layout review checklists to help identify and mitigate common design risks

About this product family

Product family

Infineon's EZ-USB™ FX2G3 is a family of highly integrated USB 2.0 peripheral controllers with higher clock frequency and improved processing capabilities such as extended memory options and increased peripherals that support the demanding data processing tasks.

Target applications

- Industrial HMI monitors and panels
- Healthcare and lifestyle

Table of contents

About this document **1**
About this product family **1**
Table of contents **2**
1 Introduction **3**
2 Related resources **4**
2.1 EZ-USB™ FX2G3 Software Development Kit 4
3 Power system **5**
3.1 Power supply design 5
3.2 Device supply decoupling 6
4 Power modes **8**
5 Crystal **9**
5.1 Crystal effective load capacitor calculation 10
5.2 Layout consideration 10
6 High-bandwidth data subsystem (HBWSS) interface **11**
7 USB **12**
7.1 USB HS 12
7.2 USB Full-Speed 14
8 Low-Speed peripherals **15**
8.1 I^2C interface 15
8.2 SWD/JTAG 15
8.3 PDM 15
8.4 Quad SPI 16
8.5 CAN 16
9 Booting **17**
10 EMI and ESD considerations **18**
11 Generic electrical design considerations **19**
12 Schematic and layout review checklist **24**
13 Summary **26**
14 Appendix A – PCB layout tips **27**
15 Appendix B – Troubleshooting **28**
15.1 EZ-USB™ FX2G3 device not enumerating 28
References **29**
Revision history **30**
Disclaimer **31**

1 Introduction

Infineon's EZ-USB™ FX2G3 is a USB Hi-Speed (HS) peripheral controller that has a fully-configurable, general programmable interface called GPIF III, which can connect to any processor, ASIC, or FPGA. EZ-USB™ FX2G3 consists of dual Arm® Cortex®-M4 and M0+ core CPUs, integrated flash, SRAM, Serial Communication Blocks (SCBs), cryptography accelerator, and high bandwidth data subsystem providing DMA data transfers between low-voltage CMOS (LVCMOS) and USB ports at speeds up to 480 Mbps. An additional 1 MB SRAM is included in the high bandwidth data subsystem to provide buffering for USB data.

EZ-USB™ FX2G3 replace EZ-USB™ FX2LP. For differences between FX2G3 and FX2LP, see the "Points to be taken care while migrating from FX2LP to FX2G3" section of EZ-USB™ FX2G3 datasheet [2].

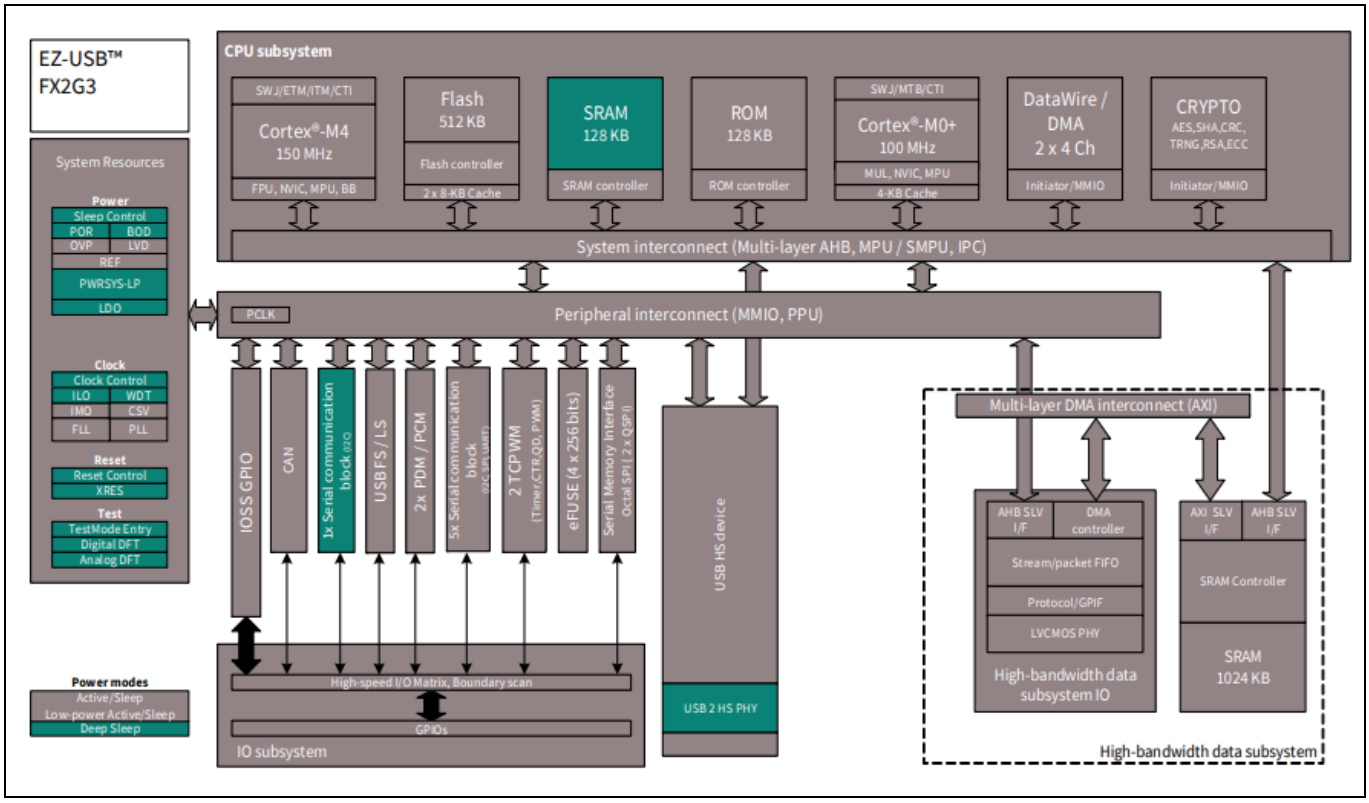


Figure 1 EZ-USB™ FX2G3 architecture block diagram

See the reference schematic of the EZ-USB™ FX2G3 Development Kit (DVK) [4].

2 Related resources

Infineon Technologies provides a wealth of data on Infineon Developer Community to help you to select the right EZ-USB™ FX2G3 device for your design, and to help you quickly and effectively integrate the device into your design.

- Application notes: Infineon offers a large number of USB application notes covering a broad range of topics, from basic to advanced levels. Recommended application notes for getting started with EZ-USB™ FX2G3 are:
  - AN240743 – Getting started with EZ-USB™ FX2G3 [1]
- Datasheet:
  - EZ-USB™ FX2G3 USB 2.0 High-Speed peripheral controller datasheet [2]
- Knowledge Base Article:
  - EZ-USB™ FX2LP to EZ-USB™FX2G3 migration guide [3]
- Development kits:
  - KIT_FX2G3_104LGA, EZ-USB™ FX2G3 Development Kit [4]
  - Visit the EZ-USB™ FX2G3 webpage to view the development kits available for EZ-USB™ FX2G3.
- Models: IBIS, BSDL

2.1 EZ-USB™ FX2G3 Software Development Kit

Infineon Technologies delivers the complete firmware stack for EZ-USB™ FX2G3, to easily integrate any embedded application to USB HS. The EZ-USB™ FX2G3 Software Development Kit (SDK) comes with tools and application examples, which help accelerate application development [5].

Note: EZ-USB™ FX2G3 can be programmed using the EZ-USB™ Control Center.

3 Power system

EZ-USB™ FX2G3 has the following power domains.

- V33 is the 3.3 V power supply for the USB 2 HS PHY and USB 2 FS PHY
- VDDD is the main digital supply input. It provides the inputs for the internal regulators
- VCCD is the internal core logic supply and needs an external decoupling capacitor
- VDDIOP0 is the power supply for LVCMOS I/Os
- VDDIOP0_CTRL is the power supply for the LVCMOS control I/Os
- VDDIOQSPI is the power supply for the QSPI port
- VDDIOXTAL is the power supply for crystal
- VDDIO is the GPIO power supply
- VSS is the main ground for the entire chip

3.1 Power supply design

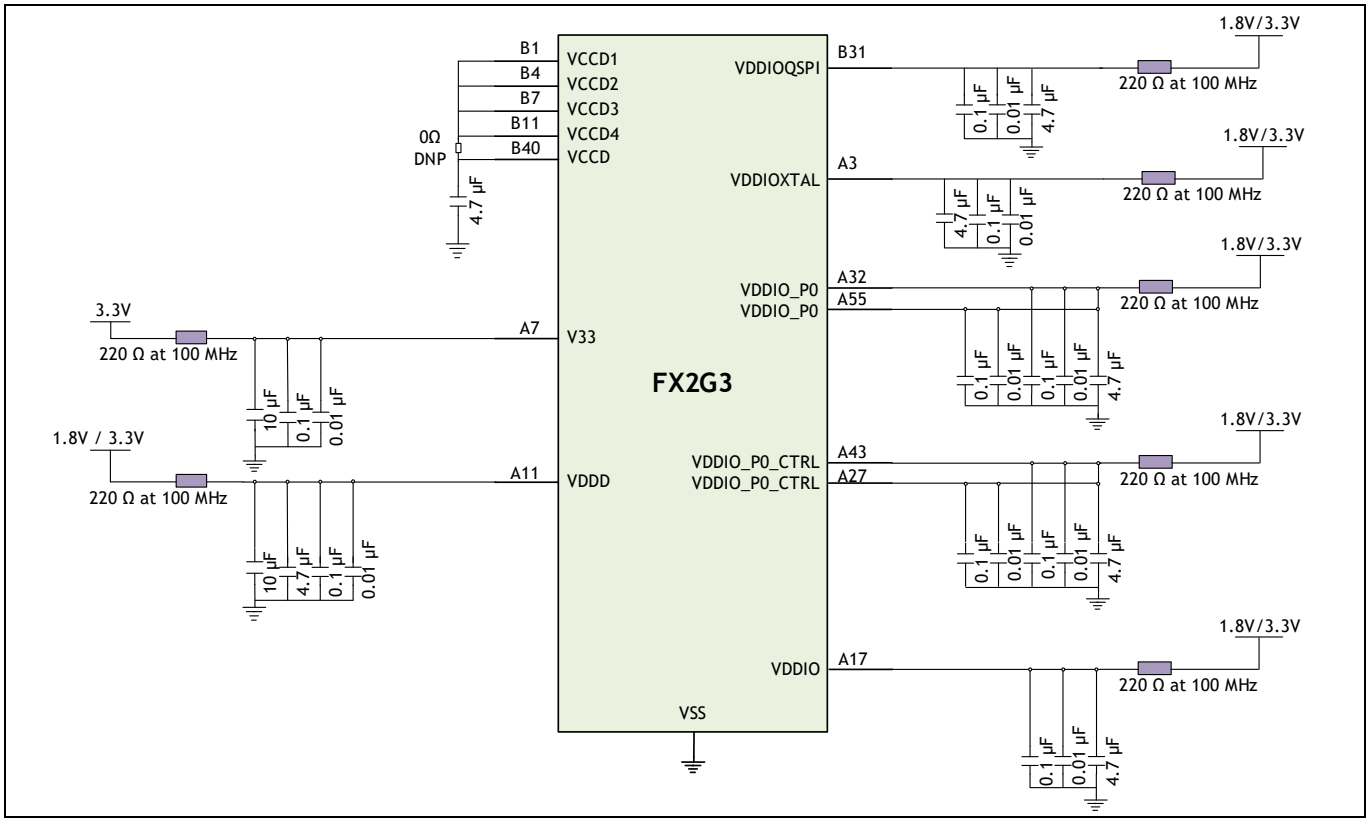


Figure 2 EZ-USB™ FX2G3 power domains

Note: For optimum noise performance of EZ-USB™ FX2G3, a combination of 0.1 µF and 0.01 µF capacitors per pin is required. A power sequence is not needed.

Note: For A0 silicon, VCCDx should be connected to VCCD.

Table 1 EZ-USB™ FX2G3 power domains

Parameter	Description	Min.	Typ.	Max.	Unit
VDDD	Main analog supply voltage	1.62	1.8 or 3.3	3.63	V
V33	Power supply voltage for 3.3 V supply	2.97	3.3	3.63	V
VDDIO VDDIOP0 VDDIOP0_CTRL VDDIOQSPI VDDIOXTAL	Power supply voltage for IO	1.62	1.8 or 3.3	3.63	V
VCCD	Core logic supply output *Note: Do not connect external supply to this pin.*	–	1.1	–	V

3.2 Device supply decoupling

Power supply decoupling is critical in ensuring that system noise does not propagate into the device through the power supply. Improper decoupling can lead to jittery signaling, especially on the USB and LVDS bus, which results in a higher CRC error rate and more retries. Decoupling capacitors must be the ceramic type of a stable dielectric. It is important to have the decoupling caps close to the power pins, and short trace runs for the power and ground connections on the EZ-USB™ FX2G3 device to solid power and ground planes.

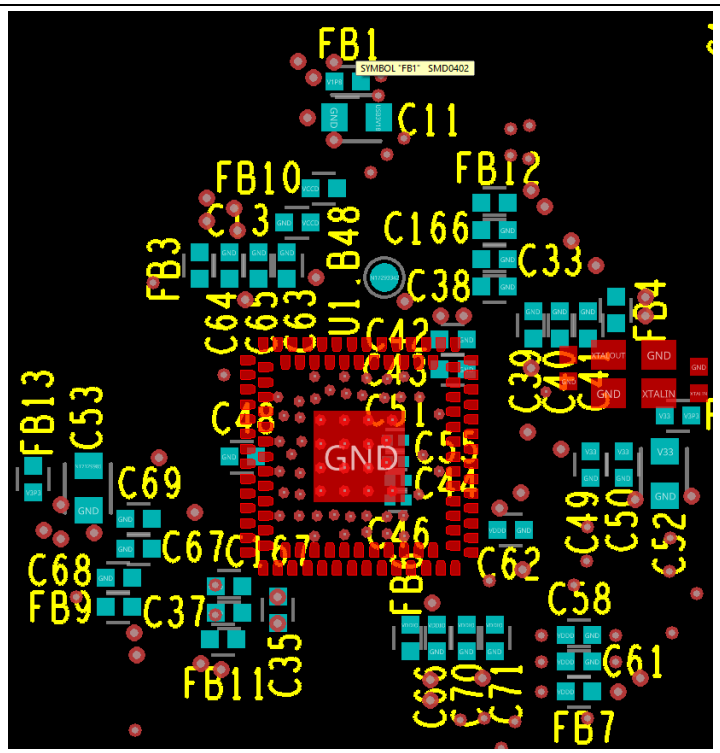


Figure 3 Placement of decoupling caps on the bottom layer of KIT_FX2G3_104LGA DVK

In Figure 3, the top layer is shown in red color and bottom layer is shown in blue color. All the decoupling capacitors are placed in bottom layer.

The specific recommendation for the ceramic capacitor nearest to each EZ-USB™ FX2G3 power pin is given in Table 2.

Table 2 Power domain decoupling requirements

Power domain (pin numbers)	Capacitors for group	Capacitors per pin
V33 (A7)	10 µF, 10 V	0.01 µF, 10 V, and 0.1 µF, 10 V
VDDD (A11)	10 µF, 10 V, and 4.7 µF, 10 V	0.01 µF, 10 V, and 0.1 µF, 10 V
VCCD (B40)	4.7 µF, 10 V	–
VDDIOQSPI (B31)	4.7 µF, 10 V	0.01 µF, 10 V, and 0.1 µF, 10 V
VDDIOXTAL (A3)	4.7 µF, 10 V	0.01 µF, 10 V, and 0.1 µF, 10 V
VDDIO_P0 (A32, A55)	4.7 µF, 10 V	0.01 µF, 10 V, and 0.1 µF, 10 V
VDDIO_P0_CTRL (A43, A27)	4.7 µF, 10 V	0.01 µF, 10 V, and 0.1 µF, 10 V
VDDIO (A17)	4.7 µF, 10 V	0.01 µF, 10 V, and 0.1 µF, 10 V

Note: To get USB-IF certification for the product in bus power mode, plan to disable the power supply powering up the rest of the device apart from EZ-USB™ FX2G3.

4 Power modes

EZ-USB™ FX2G3 supports the following power modes:

- System Low Power (LP): All peripherals and CPU power mode are available at maximum speed
- CPU Active: CPU is executing code in system LP
- CPU Sleep: CPU code execution is halted in system LP
- CPU Deep Sleep: CPU code execution is halted and system Deep Sleep is requested in system LP mode
- System Deep Sleep: Only low-frequency peripherals are available after both CPUs enter CPU Deep Sleep mode
- Normal mode: Full-functional operating mode. The internal CPU clock and the internal PLLs are enabled in this mode
  - USB 2.0 operation at 480 Mbps
  - High-bandwidth data subsystem IOs port in LVCMOS SDR mode

Other low-power modes include:

- Suspend mode
- Deep Sleep mode
- Core power-down mode

CPU Active, Sleep, and Deep Sleep are standard Arm®-defined power modes supported by the Arm® CPU instruction set architecture (ISA). System LP and Deep Sleep modes are additional low-power modes supported by the EZ-USB™ FX2G3.

5 Crystal

The EZ-USB™ FX2G3 device has a built-in clock oscillator and uses a 24 MHz external crystal. VDDIOXTAL supply is the supply associated with the clock input.

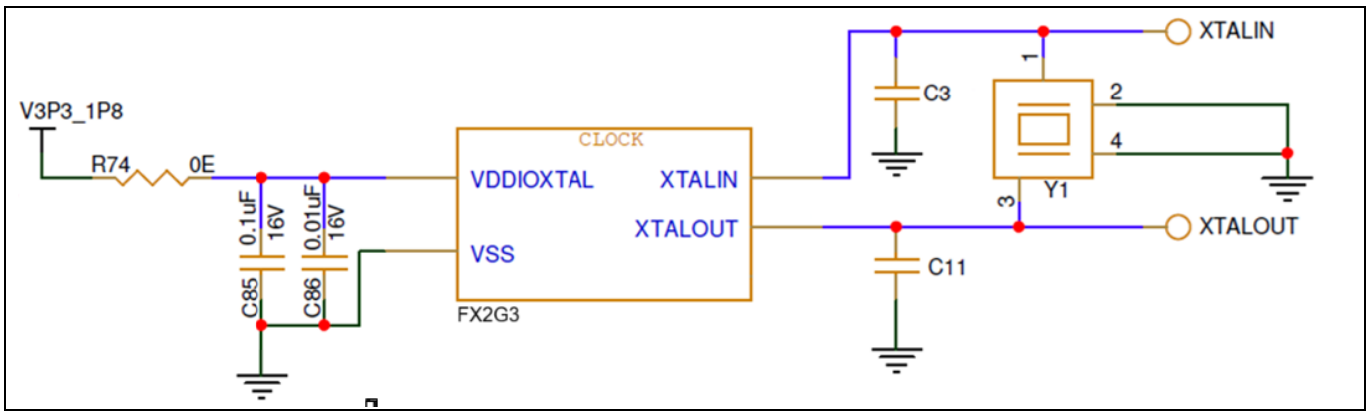


Figure 4 Crystal circuit

Table 3 24 MHz crystal requirements

Parameter	Specification	Unit
Tolerance	< ±30	ppm
Temperature range	–40 to 85	°C
Drive level	Use Equation 1	mW

Note: For more details on crystal specifications, see XTAL/clock specification in the datasheet [2].

The power dissipation of the crystal depends on the following:

- Drive level of the XTALOUT pin (for EZ-USB™ FX2G3, this depends on VDDIOXTAL)
- Desired frequency (24 MHz)
- Equivalent resistance of the crystal

$$P = I^2R = \left(\frac{V_x}{|Z|}\right)^2 R = 2[\pi f\ (C_0 + C_L)\ V_x]^2 R$$

Equation 1 Power dissipation of the crystal

Where,

f is the crystal frequency

C_0 is the shunt capacitance of the crystal obtained from the crystal datasheet

C_L is the load capacitance; for CL calculation, see the Crystal effective load capacitor calculation section

R is the crystal ESR obtained from the datasheet of the crystal

V_x is the peak voltage on the XTALOUT pin

Using a crystal with a drive level less than the crystal's power dissipation may result in accelerated aging or even burnout of the crystal.

Examples of compatible crystals are shown in Table 4. Only the ECS-240-8-36CKM-TR is characterized with the EZ-USB™ FX2G3, and the remaining crystals are provided as examples using Equation 1.

Table 4 Crystal selection

Device	Max R (Ω) from the datasheet	CL Eqv (pF)	C0 (pF) estimate	Drive level using Equation 1 (µW)	Max drive level (spec) µW
ECS-240-8-36CKM-TR	60	8	5	93.38	100
ABM10W-24.0000MHZ-6-B1U-T3	50	6	2	29.47	100

Note: Do not connect any series resistor to the XTALOUT and XTALIN pins of the crystal. Placing a series resistor will add resistance to the crystal ESR, resulting in increased crystal power dissipation and startup time.

5.1 Crystal effective load capacitor calculation

Load capacitance C_L plays a critical role in providing an accurate clock source to EZ-USB™ FX2G3. Select the capacitors C_3 and C_{11} (as shown in Figure 4) based on the load capacitance value of the crystal.

The load capacitance is calculated using the following equation:

$$C_L = \frac{C_3 * C_{11}}{C_3 + C_{11}} + C_S$$

Equation 2 Load capacitance of a crystal

C_S is the stray capacitance of XTALOUT and XTALIN traces on the PCB. Generally, the value of C_S is around 2-5 pF if you follow good layout practice and keep the trace from the crystal to the pins on the EZ-USB™ FX2G3 as short as possible.

For the crystal used in EZ-USB™ FX2G3 Development Kit, C_L = 8 pF. EZ-USB™ FX2G3 PCB C_S = 3 pF.
From Equation 2, $C_3 = C_{11}$ = 10 pF.

5.2 Layout consideration

- Place crystal as close as possible near EZ-USB™ FX2G3
- Ensure the crystal traces to EZ-USB™ FX2G3 are shortest
- Guard the XTALIN and XTALOUT traces with GND on the same layer
- Provide solid GND for the entire crystal and the traces in the next layer
- XTALIN and XTALOUT traces should be of the same length
- It is recommended to route XTALIN and XTALOUT traces without vias
- Do not place any Hi-Speed signal and reset signal trace near the crystal. If needed because of space constraints, fill the space with ground

See the EZ-USB™ FX2G3 DVK board layout for reference.

6 High-bandwidth data subsystem (HBWSS) interface

EZ-USB™ FX2G3 offers a high-bandwidth data subsystem that allows data transfers between LVCMOS I/O subsystem and USB HS device. The LVCMOS parallel interface supports both Rx and Tx interface. Each link contains 16 LVCMOS I/Os and 10 control signals. The maximum data rate on each LVCMOS I/O is 100 MHz for SDR in both Tx and Rx mode.

The following are some general design guidelines for the EZ-USB™ FX2G3's high-bandwidth data subsystem LVCMOS interface.

- Maintain the impedance of all LVCMOS signals at 50 Ω ± 10%
- All LVCMOS signals should be length matched to the clock within 500 mils

Note: For more details, see the EZ-USB™ FX2G3 DVK layout.

7 USB

7.1 USB HS

EZ-USB™ FX2G3 has an integrated USB HS 480 Mbps PHY that allows connection to a USB-C connector directly. Ensure the following recommendations are considered in the design.

- Minimize the trace length of USB lines as much as possible (< 3 inches). Route these first to ensure certain recommendations on this list are achievable. Long traces affect the transmission quality and introduce intersymbol interference (ISI) on the receiver side
- USB signals must refer to the solid ground plane on the PCB
- It is recommended that the intra-pair (p and n) differential lines should be length matched within +/- 5 mils.
- Keep the USB signal line impedance at 90 Ω differential (±5%)
- Fill the space around USB signals with the ground. Maintain a minimum of 2W space between the ground and the differential pairs, where W = trace width
- Connect at least one bulk capacitor of 10 µF at the USB-C VBUS pin along with the ceramic capacitors between 22 nF and 100 nF. All capacitors should be rated 10 V or higher to ensure at least 50% derating. The bulk capacitor will maintain the voltage levels in case of a transient current requirement
- Connect 5.1 KΩ ± 1% pull-down resistor on the CC1 and CC2 lines of the USB-C connector
- VBUSDETECTn pin of EZ-USB™ FX2G3 allows for self-power mode operation. This pin, however, is used as a negative logic pin and is connected in the DVK to VBUS through a NMOS FET as shown in Figure 5. When a host is connected, VBUSDETECTn will go low, indicating a connection. This pin can be used as positive logic with a firmware update
- Use appropriate ESD diodes near the USB-C connector, as shown in Figure 6
- Shield pins on the USB-C receptacle should be terminated to the ground with a parallel LC (or) RC circuit to avoid EMI/EMC issues. It is recommended to use an RC circuit, as shown in Figure 6
- Use USB-IF certified USB-C connectors in the design for optimum performance
- See the EZ-USB™ FX2G3 DVK board file for more details

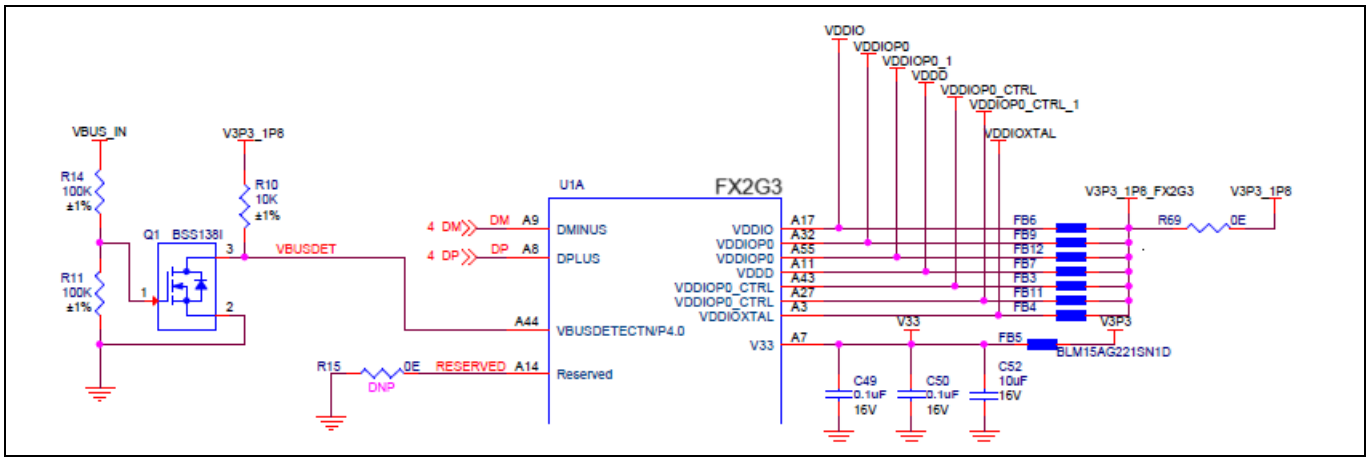


Figure 5 VBUSDETECTn pin

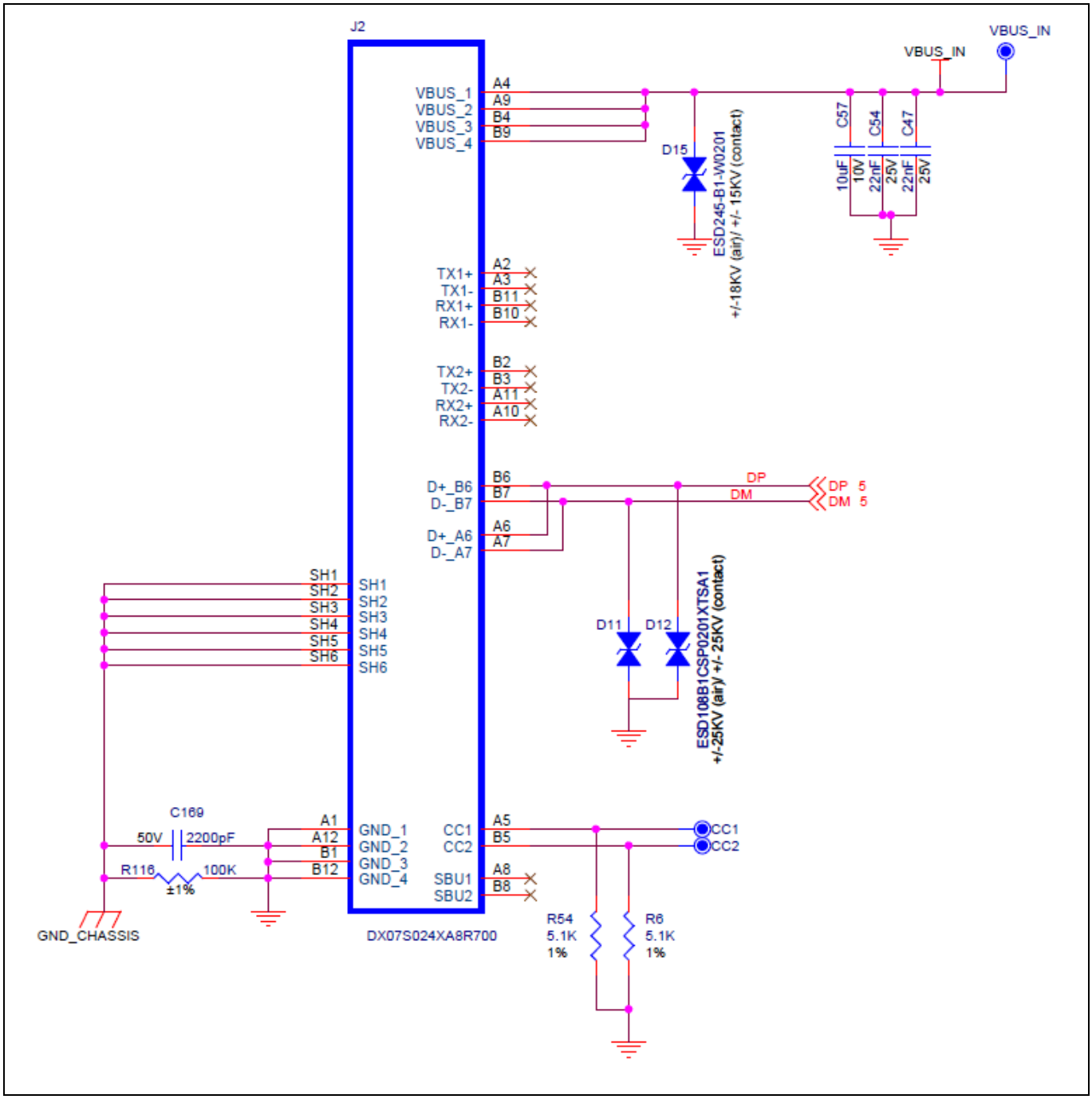


Figure 6 EZ-USB™ FX2G3 interface with USB-C connector

7.2 USB Full-Speed

EZ-USB™ FX2G3 has a separate USB Full-Speed interface that can be used to log messages for debugging purposes. Use a USB-C Full-Speed connector for debugging. Ensure that there is 90 Ω ± 5% impedance for the data lines. If a USB-C Full-Speed connector is used in the design, use 5.1 KΩ ± 5% on the CC lines. Shield pins on the USB-C receptacle should be terminated to the ground with a parallel LC (or) RC circuit to avoid EMI/EMC issues. It is recommended to use an RC circuit, as shown in Figure 7.

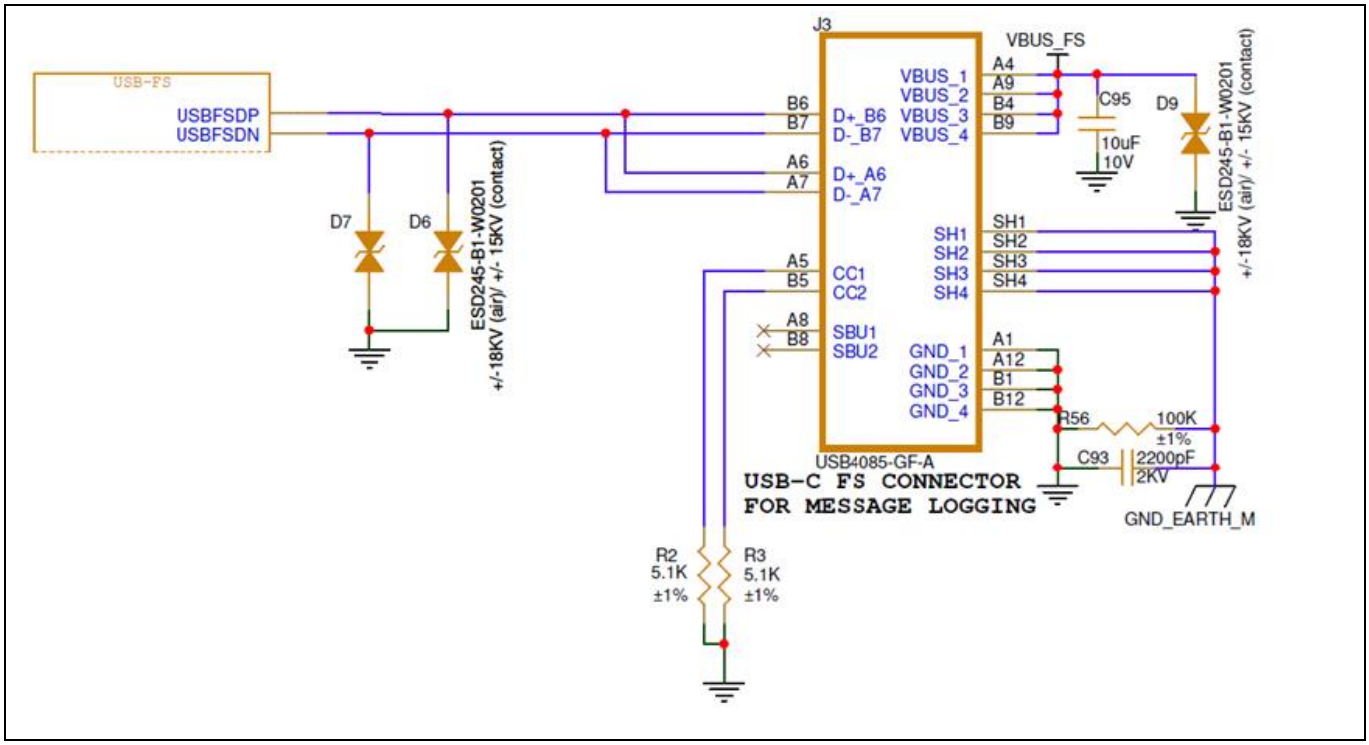


Figure 7 EZ-USB™ FX2G3 interface with USB-C FS connector

8 Low-Speed peripherals

EZ-USB™ FX2G3 has six SCBs, that can be configured as SPI, UART, or I²C. Apart from this, other peripherals such as PDM, QSPI, CAN, and UART are also supported. See the “Pin definition” section in the datasheet [2].

8.1 I²C interface

EZ-USB™ FX2G3 has an I²C interface compatible with the I²C bus specification. The power supply for the I²C interface is VDDIO, which is the power domain for all the other low-speed peripherals. P10.0 and P10.1 are the I²C of the chip. They are overvoltage tolerant up to 5 V.

The bus frequencies supported by the I²C controller are 100 kHz, 400 kHz, and 1 MHz.

The I²C interface can operate at 1.8 V or 3.3 V. A 2 KΩ ± 1% pull-up to VCCIO voltage is recommended on the I²C lines.

8.2 SWD/JTAG

EZ-USB™ FX2G3 has a debug access port (DAP) as the interface for device programming and debugging. An external programmer or debugger can communicate with the DAP through the device Serial Wire Debug (SWD) or Joint Test Action Group (JTAG) interface pins. Through the DAP (and subject to restrictions), the host can access the device memory and peripherals and the registers in both CPUs.

EZ-USB™ FX2G3 has a JTAG interface to provide a standard five-pin interface for connecting to a JTAG debugger. A 10 kΩ external pull-up resistor is recommended on the JTAG signals TDI, TDO, TMS, and TRST# pins.
EZ-USB™ FX2G3 also supports boundary scan. See the datasheet [2] for more details.

EZ-USB™ FX2G3 also supports SWD to program the bootloader and perform debugging.

8.3 PDM

EZ-USB™ FX2G3 has one PDM to PCM decoder. Up to two microphones can be connected to the same PDM data line. Ensure that you follow these points in the layout.

- If a single microphone is used, length match the data to clock within ± 25 mils.
- If two microphones are used in the design, length match the data to the clock for each microphone separately. Figure 8 shows connecting two microphones to EZ-USB™ FX2G3. Length match Cx and Dx, Ca and Da, Cb, and Db individually, all within ± 30 mils.

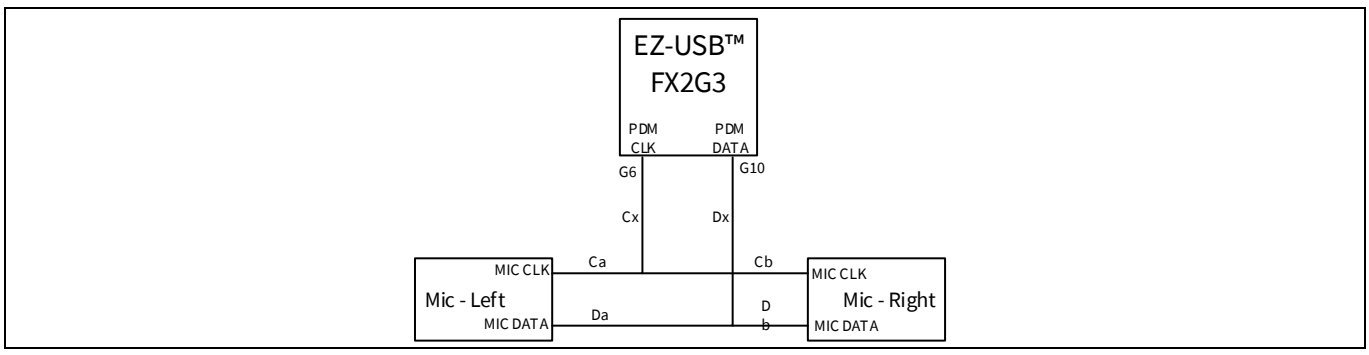


Figure 8 Connecting two microphones to EZ-USB™ FX2G3

8.4 Quad SPI

EZ-USB™ FX2G3 supports single, dual, quad, dual-quad, and octal SPI configurations. External SPI flash can be used to store FPGA configuration file. It supports up to two external memory devices. SPI clock operates at up to 80 MHz. All the data signals should length match to the clock within 1000 mils.

Note: See the datasheet [2] for appropriate FX2G3 MPN that supports Quad SPI.

8.5 CAN

External CAN device must be connected to EZ-USB™ FX2G3. Maintain trace impedance of CANH and CANL at 120 Ω.

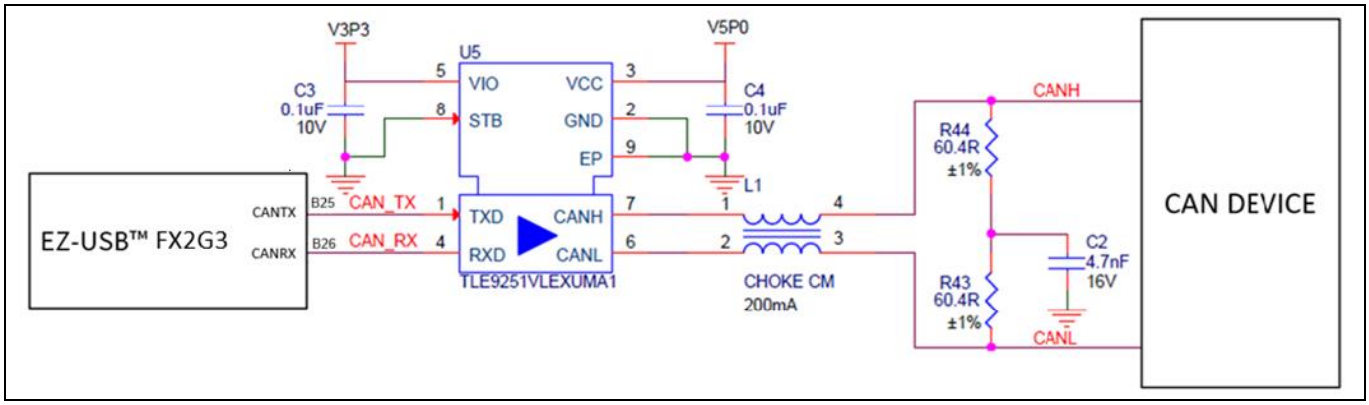


Figure 9 Interfacing CAN device with EZ-USB™ FX2G3

Note: See the datasheet for appropriate EZ-USB™ FX2G3 MPN that supports CAN.

9 Booting

EZ-USB™ FX2G3 operates only on two boot modes; USB boot and internal flash boot based on the voltage level on the PMODE pin.

Table 5 PMODE signal setting

PMODE	Boot from
GND	Internal flash
VCCIO	USB boot

Note: Whenever PMODE selection changes, press the RESET button or power cycle the EZ-USB™ FX2G3 device.

10 EMI and ESD considerations

All pins of EZ-USB™ FX2G3 support ±2.2 kV human body model (HBM)-based on JESD22-A114 specification.

Provide the IEC protection at the system level. Provide additional protection to all pins with user interface by using high-performance and low-capacitance external ESD devices. See Figure 6 for the Infineon Technologies ESD diodes used on the USB lines of the USB 10 Gbps connector.

Regarding EMI, all signal and clock traces emit electromagnetic (EM) radiation when they switch from one level to another. To meet the various standards in different countries, minimize these emissions. Several techniques can be implemented during the design to lower EM emissions in all high-speed signals (USB):

- Consider placing the power and ground planes as the outside layers with signal layers underneath
- Always have solid copper fills beneath integrated circuits and clocks
- Ensure an adequate ground return path for all the signals
- Minimize the trace length of high-speed and high-current traces

11 Generic electrical design considerations

See Appendix A – PCB layout tips for general information on PCB layout techniques.

- Place the capacitor used in the RC reset circuitry as close as possible to the reset pin of EZ-USB™ FX2G3
- Use split planes on the power layer for different power domains
- Keep the power traces away from high-speed data and clock lines
- Power trace widths should be ≥25 mils to reduce the inductance
- Keep power traces as short as possible. Use larger vias (at least 30-mil pad, 15-mil hole) on power traces
- Avoid any split in the immediate plane under the USB/LVCMOS lines. The presence of a split under the USB/LVCMOS trace will result in a variation of characteristic impedance at that point
- Keep trace spacing between differential pairs consistent to avoid impedance mismatches as shown in Figure 10

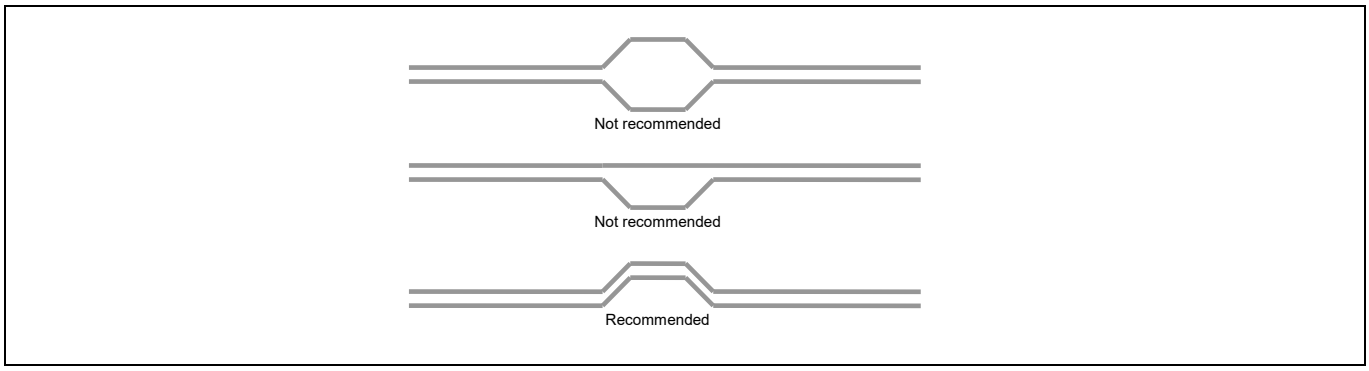


Figure 10 Differential pairs impedance matching techniques

- All USB/LVCMOS signal lines should be routed entirely over a solid ground plane on an adjacent layer. Splitting the ground plane underneath the USB/LVCMOS signals increases loop inductance introduces impedance mismatches and increases electrical emissions. See Figure 11

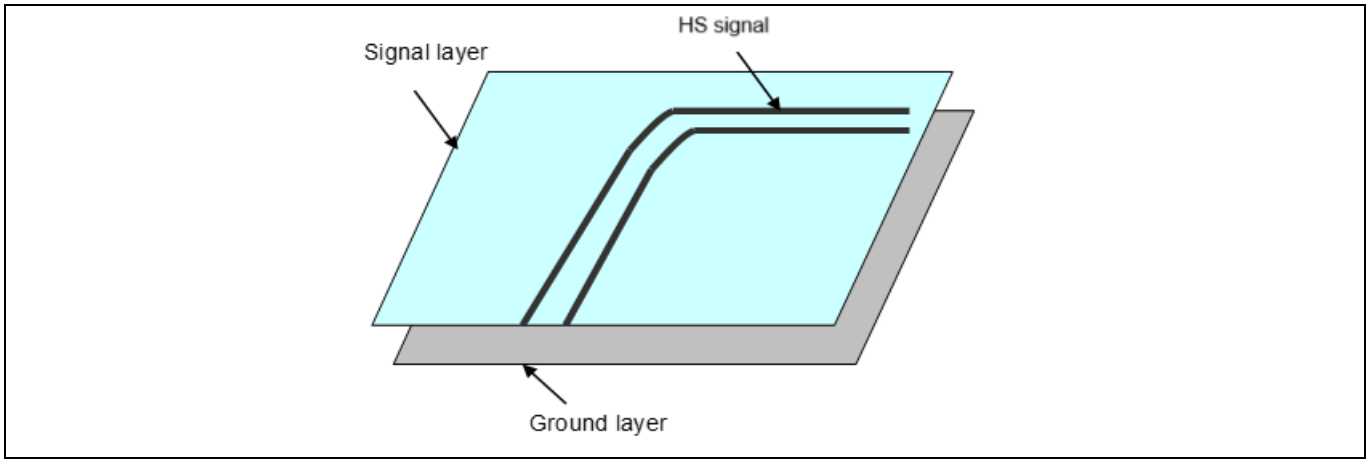


Figure 11 Solid ground plane under the Hi-Speed signal

- Whenever two pairs of USB/LVCMOS traces cross each other in different layers, a ground layer should run between the two signal layers. See Figure 12

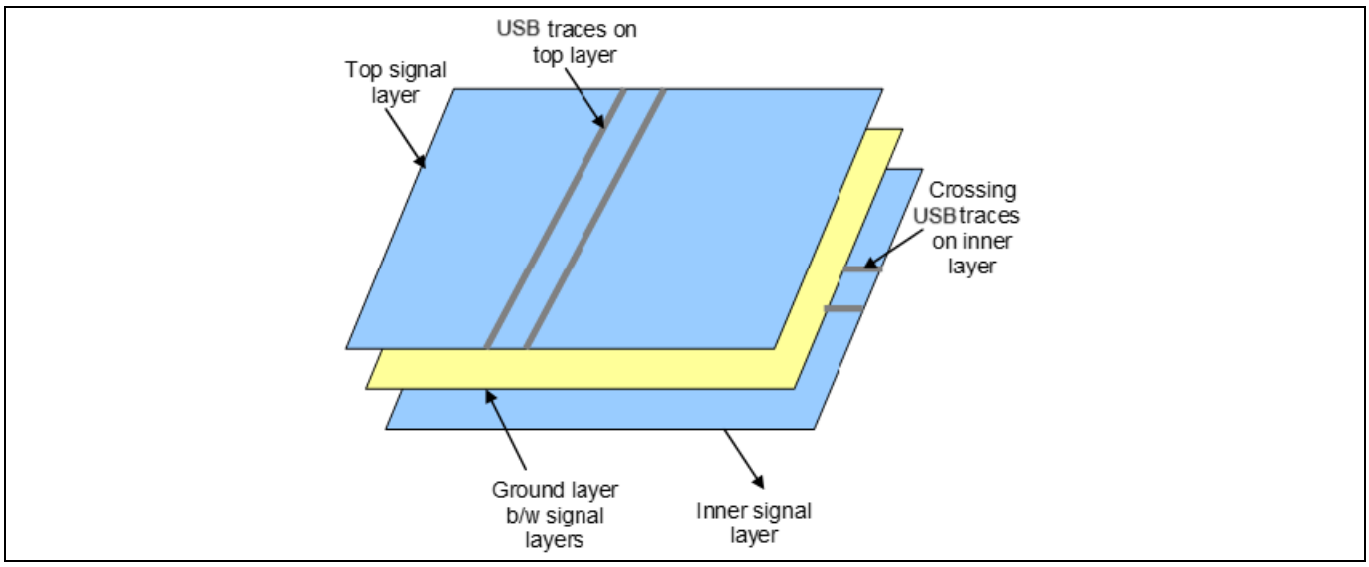


Figure 12 Ground insertion

- On the USB/LVCMOS signal lines, use as few bends as possible. Do not use a 90-degree bend. Use 45-degree or rounded (curved) bends if necessary. See Figure 13

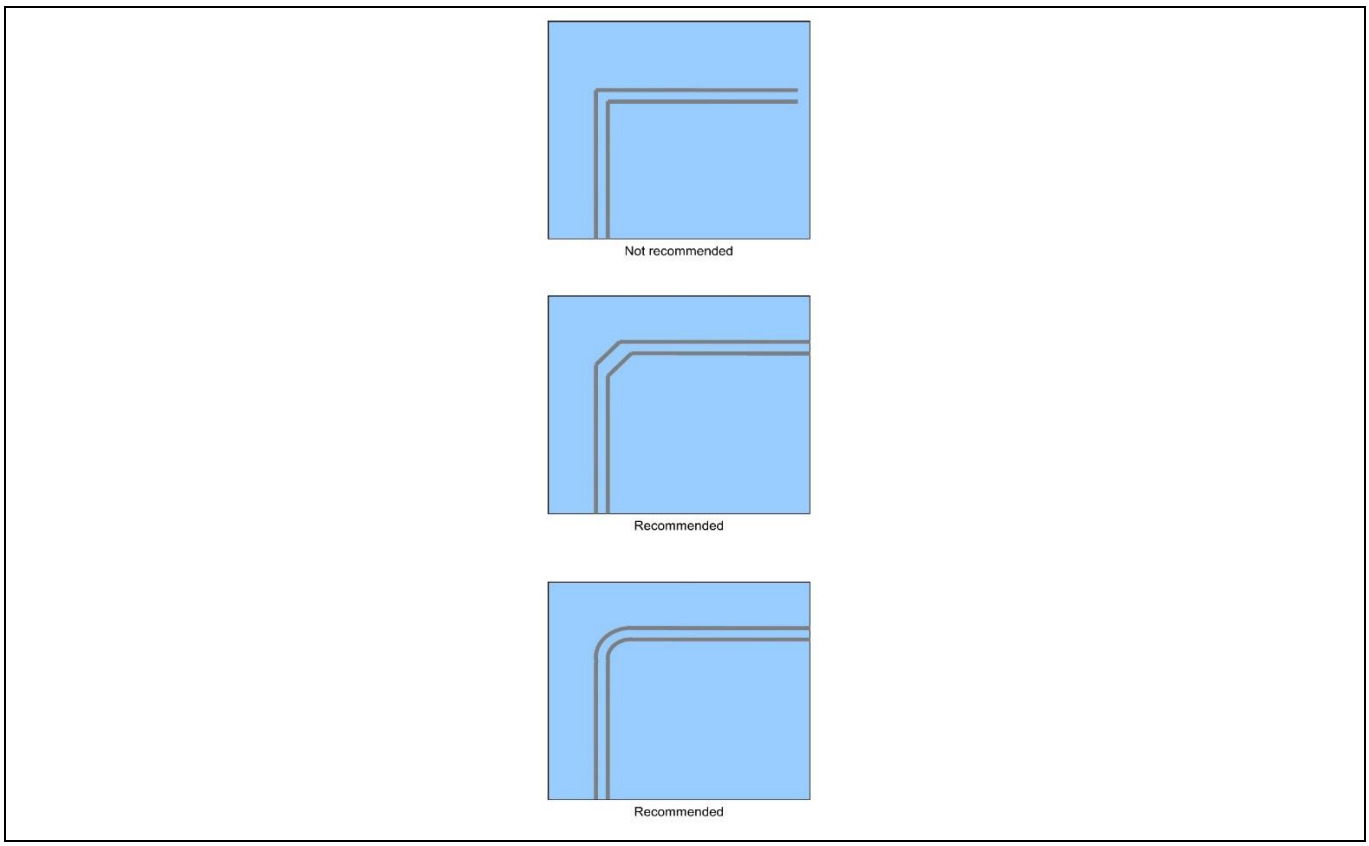


Figure 13 USB signal bends

- Intra-pair differential trace lengths should be matched within 0.12 mm (5-mils). Always adjust for USB signal trace lengths near the USB receptacle and not near the device. Always adjust the length at the mismatched ends. An example of length matching for the USB signal is shown in Figure 14

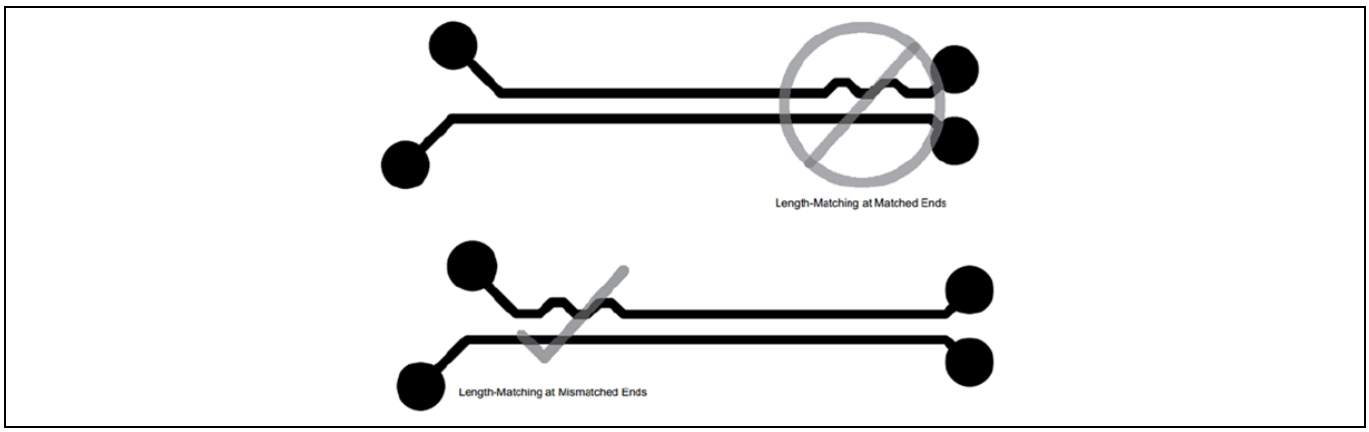


Figure 14 Intra-pair differential signal length matching

- There are different routing methods for length matching: single arc routing and serpentine routing methods. See Figure 15 and Figure 16 for single arc routing and serpentine routing respectively

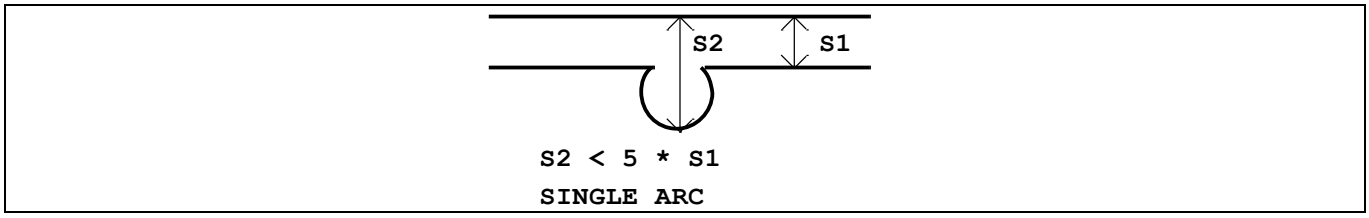


Figure 15 Single arc routing

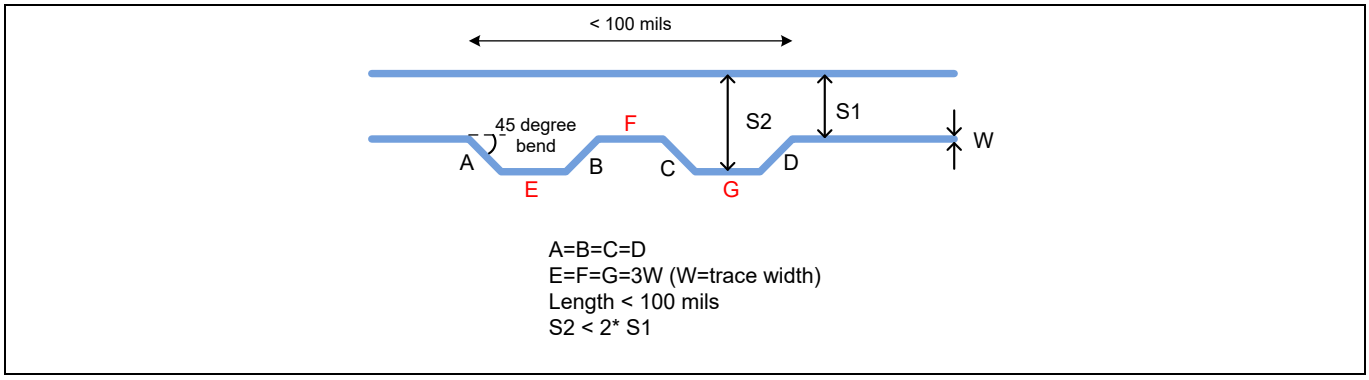


Figure 16 Serpentine routing

- The number of layers on the PCB should at least be four
- If signal routing has to be changed to another layer, continuous grounding has to be maintained to ensure uniform impedance throughout. To achieve this, it is good to have ground vias next to signal vias. The distance between the signal and ground vias should be at least 40 mils. See Figure 17

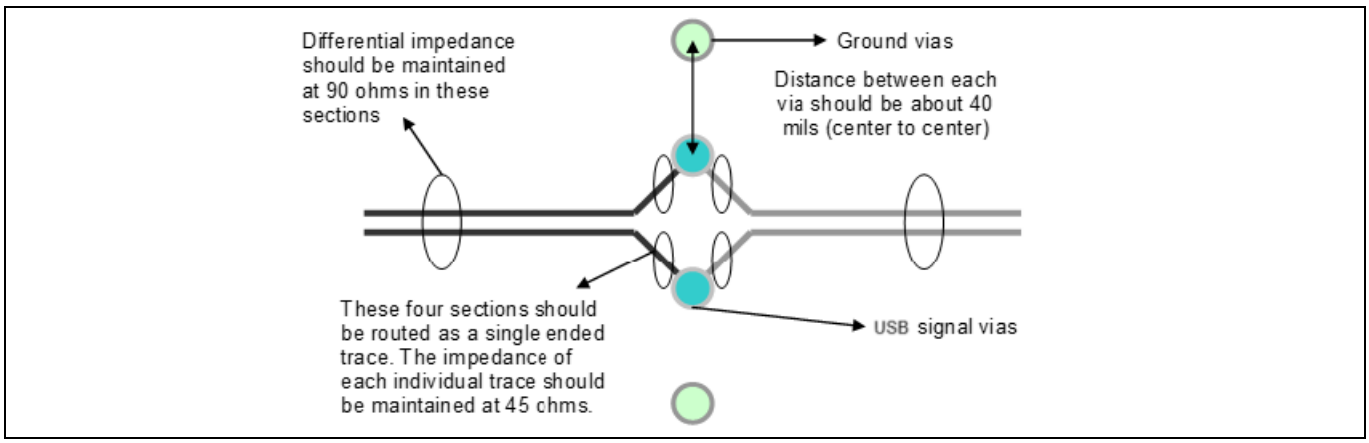


Figure 17 Ground vias

- Maintain constant trace width in differential pairs to avoid impedance mismatches:

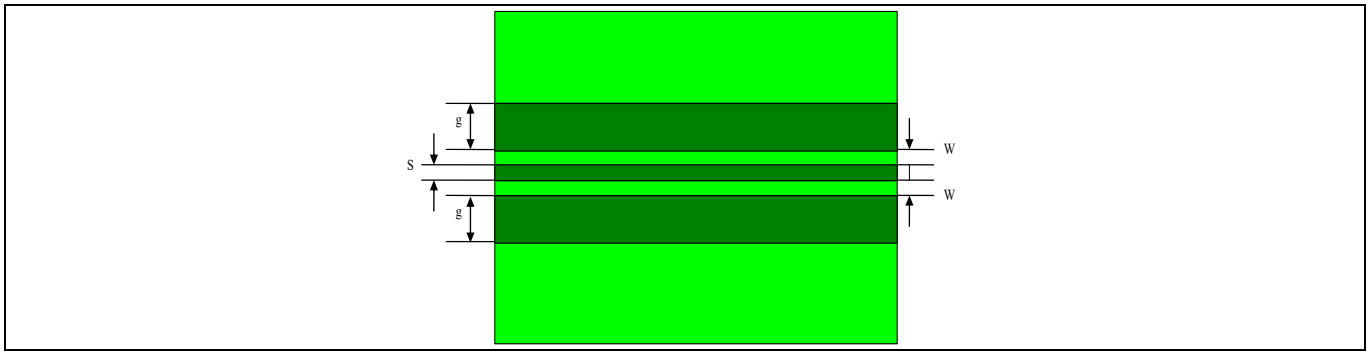


Figure 18 Differential pairs placements

- Avoid stubs on all Hi-Speed lines. If pads are needed on the lines for probing purposes, they should not extend out of the trace in the form of a stub. See Figure 19

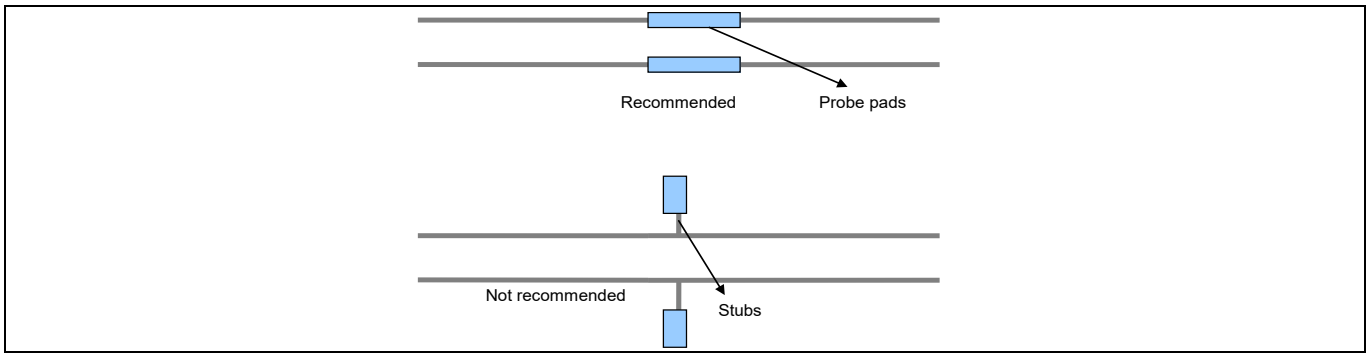


Figure 19 Probing pads placement

- Void for vias on the high-speed signal lines should be common for the differential pair. A common void, as shown in Figure 20, maintains better impedance matching in comparison to separate vias

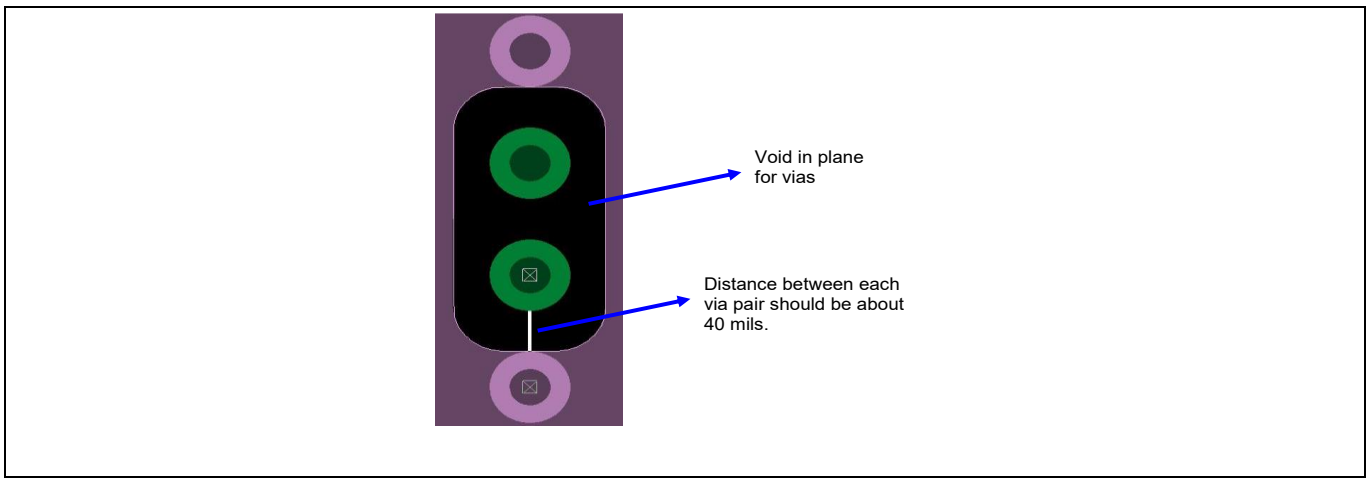
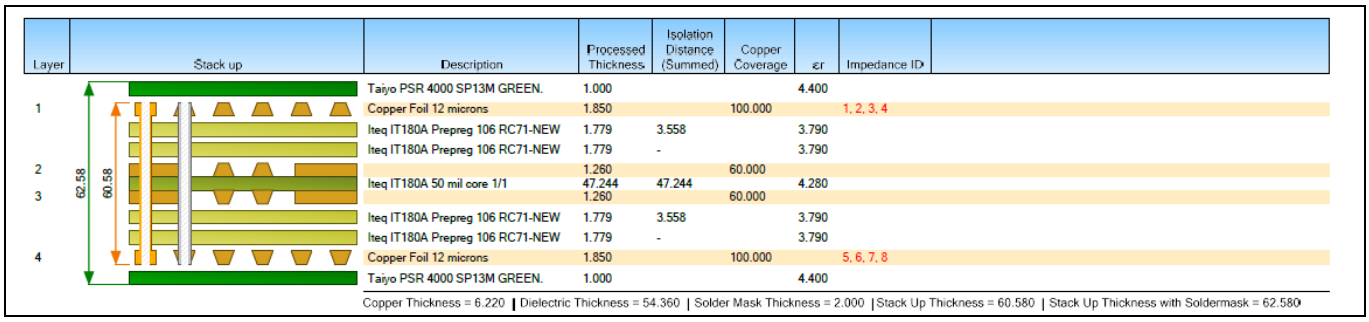


Figure 20 Void vias placement for high-speed differential traces

- To avoid cross-talk, do not place the differential pairs close to other differential pairs, clock signals, or high-speed signals. It is recommended to maintain a 3x distance with other differential pair and other signals where 'x' is the width of the signal trace
- Figure 21 shows an example of a four-layer stack up from the EZ-USB™ FX2G3 development kit. This is captured using the Polaris tool



Layer	Stack up	Description	Processed Thickness	Isolation Distance (Summed)	Copper Coverage	εr	Impedance ID
		Taiyo PSR 4000 SP13M GREEN.	1.000			4.400	
1		Copper Foil 12 microns	1.850		100.000		1, 2, 3, 4
		Iteq IT180A Prepreg 106 RC71-NEW	1.779	3.558		3.790	
		Iteq IT180A Prepreg 106 RC71-NEW	1.779	-		3.790	
2			1.260		60.000		
3		Iteq IT180A 50 mil core 1/1	47.244	47.244		4.280	
			1.260		60.000		
		Iteq IT180A Prepreg 106 RC71-NEW	1.779	3.558		3.790	
		Iteq IT180A Prepreg 106 RC71-NEW	1.779	-		3.790	
4		Copper Foil 12 microns	1.850		100.000		5, 6, 7, 8
		Taiyo PSR 4000 SP13M GREEN.	1.000			4.400	

Copper Thickness = 6.220 | Dielectric Thickness = 54.360 | Solder Mask Thickness = 2.000 | Stack Up Thickness = 60.580 | Stack Up Thickness with Soldermask = 62.580

Figure 21 Stackup details for EZ-USB™ FX2G3 Development Kit

12 Schematic and layout review checklist

Table 6 and Table 7 list the checklist for all the important guidelines. Respond to each checklist item to determine the extent to which your hardware design meets these guidelines. A design that satisfies all the schematic and layout checklists will definitely work without any system-level hardware issues.

Table 6 Schematics checklist

Sl. no	Schematic checklist	Answer (Yes/No/NA)
1	Are the decoupling capacitors and bulk capacitors connected according to Table 2?	
2	Does the crystal meet the specification in this application note according to Table 3?	
3	Are the ferrite beads connected to the supply pins according to Figure 2?	
4	Do the power-on-reset RC components meet the minimum reset time requirement of >1 µs?	
5	Is 5.1 KΩ resistor pull-down connected to CC1 and CC2 lines?	
6	Are the I^2C lines provided with pull-up resistors to the VDDIO domain?	
7	Does the USB port shield terminate with the RC circuit?	
8	Do the USB traces have an ESD device connected?	
9	Is the VBUSDETECTn pin connected to VBUS through negative logic as shown in Figure 5? If not, is it connected as a positive logic? If it is connected as a positive logic, a firmware change is necessary.	
10	Are the PMODE lines connected to achieve Table 5 functionality?	
11	Does the SPI flash meet the specification in this application note according to Section 8.4?	
12	Do the JTAG lines have pull-up resistors to VDDIO?	
13	Does the VBUS pin of EZ-USB™ FX2G3 device has overvoltage protection?	
14	Does the VBUS pin of EZ-USB™ FX2G3 has a 10 µF bulk capacitor?	

Table 7 Layout checklist

Sl. no	Layout checklist	Answer (Yes/No/NA)
1	Is the crystal placed close to the chip (less than 2 cm)?	
2	Are the decoupling capacitors and bulk capacitors placed close to the EZ-USB™ FX2G3 power pins?	
3	Are the clock traces routed away from the high-speed data lines and the power lines?	
4	Are the power traces routed away from the high-speed data lines and the clock lines?	
5	Is the capacitor in the RC reset circuitry placed close to the reset pin of EZ-USB™ FX2G3?	
6	Do the USB HS and FS signal lines have a 90 Ω differential impedance?	

Schematic and layout review checklist

Sl. no	Layout checklist	Answer (Yes/No/NA)
7	Are the USB HS and FS signal lines intra-pair match done with in 5 mils?	
8	Are the USB data lines provided with a solid ground plane underneath?	
9	Are the crystal signals provided with the guard traces?	
11	Do the USB traces have few bends and no 90-degree bend?	
13	Are the USB traces kept less than 3 inches?	
14	Is it ensured that there are no stubs on all the USB traces?	
16	Do the LVCMOS signal lines have 50 Ω single ended impedance?	
17	Are the LVCMOS signals referring to the solid GND plane?	

13 Summary

The developer must consider the recommended practices for EZ-USB™ FX2G3 hardware design and the critical items discussed in this document.

14 Appendix A – PCB layout tips

There are many classic techniques for designing PCBs for low noise and EMC. A few of these techniques include:

- **Multiple layers:** Although they are more expensive, it is best to use a multi-layer PCB with separate layers dedicated to the ground and power supplies. This gives good decoupling and shielding effects
- **Component position:** Separate the different circuits on the PCB according to their electromagnetic interference (EMI) contribution. This will help reduce cross-coupling on the PCB. For example, separate noisy high-current circuits, low-voltage circuits, and digital components
- **Ground and power supply:** There should be a single point for gathering all ground returns. Avoid ground loops or minimize their surface area. All component-free surfaces of the PCB should be filled with additional grounding to create a shield, especially when using a two-layer PCB
- The power supply should be close to the ground line to minimize the area of the supply loop. The supply loop can act as an antenna and can be a major emitter or receiver of EMI
- **Decoupling:** The standard decoupler for external power is a 100-µF capacitor. Supplementary 0.1-µF capacitors should be placed as close as possible to the GND and supply pins of the device to reduce high-frequency power supply ripple

Generally, decouple all sensitive or noisy signals to improve electromagnetic compatibility (EMC) performance. Decoupling can be both capacitive and inductive.

- **Signal routing:** When designing an application, the following areas should be closely studied to improve EMC performance:
  - Noisy signals, for example, signals with fast edge times
  - Sensitive and high-impedance signals
  - Signals that capture events, such as interrupts and strobe signals

To increase EMC performance, keep the trace lengths as short as possible and isolate the traces with V_{SS} traces. To avoid cross-talk, do not route them near to or parallel to other noisy and sensitive traces.

15 Appendix B – Troubleshooting

15.1 EZ-USB™ FX2G3 device not enumerating

Many factors contribute to the EZ-USB™ FX2G3 enumeration issue. A few of these points include:

- **PMODE pins:** Check if the PMODE pin is properly configured according to the application
- **USB-C receptacle to EZ-USB™ FX2G3 device connections:** Check if CC lines are terminated with a 5.1 KΩ resistor
- **Power domain isolation:** Ensure that EZ-USB™ FX2G3 power supplies are isolated and connected with ferrite beads. Also, the source of these supplies should have noise/ripple less of than 100 mV

References

For a complete and updated list of EZ-USB™ FX2G3 code examples, visit Infineon's GitHub repository. For more EZ-USB™ FX2G3 related documents, visit the EZ-USB™ FX2G3 webpage.

Application note

[1] Infineon Technologies AG: *AN240743 - Getting started with EZ-USB™ FX2G3;* Available online

Datasheet

[2] Infineon Technologies AG: *002-39966: CYUSB231x EZ-USB™ FX2G3 USB 2.0 high-speed peripheral controller* Available online

Reference manual

[3] Infineon Technologies AG: *EZ-USB™ FX2LP to EZ-USB™FX2G3 migration guide;* Available online

Development kits

[4] Infineon Technologies AG: *KIT_FX2G3_104LGA: EZ-USB™ FX2G3 Development Kit;* Available online

Tools

[5] Infineon Technologies AG: *EZ-USB™ FX2G3 Software Development Kit;* Available online

Revision history

Document revision	Date	Description of changes
**	2024-12-02	Initial release
*A	2025-02-11	Removed the restricted tag from the header VCCDx connection to VCCD added for A0 silicon
*B	2025-08-17	Updated Figure 6
*C	2026-04-09	Web release

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2026-04-09
Published by

Infineon Technologies AG
Am Campeon 1-15
85579 Neubiberg
Germany

© 2026 Infineon Technologies AG. All Rights Reserved.

Do you have a question about this document?
Email: erratum@infineon.com

Document reference
002-40541 Rev. *C

Important Notice
Products which may also include samples and may be comprised of hardware or software or both ("Product(s)") are sold or provided and delivered by Infineon Technologies AG and its affiliates ("Infineon") subject to the terms and conditions of the frame supply contract or other written agreement(s) executed by a customer and Infineon or, in the absence of the foregoing, the applicable Sales Conditions of Infineon. General terms and conditions of a customer or deviations from applicable Sales Conditions of Infineon shall only be binding for Infineon if and to the extent Infineon has given its express written consent.
For the avoidance of doubt, Infineon disclaims all warranties of non-infringement of third-party rights and implied warranties such as warranties of fitness for a specific use/purpose or merchantability.
Infineon shall not be responsible for any information with respect to samples, the application or customer's specific use of any Product or for any examples or typical values given in this document.
The data contained in this document is exclusively intended for technically qualified and skilled customer representatives. It is the responsibility of the customer to evaluate the suitability of the Product for the intended application and the customer's specific use and to verify all relevant technical data contained in this document in the intended application and the customer's specific use. The customer is responsible for properly designing, programming, and testing the functionality and safety of the intended application, as well as complying with any legal requirements related to its use.
Unless otherwise explicitly approved by Infineon, Products may not be used in any application where a failure of the Products or any consequences of the use thereof can reasonably be expected to result in personal injury. However, the foregoing shall not prevent the customer from using any Product in such fields of use that Infineon has explicitly designed and sold it for, provided that the overall responsibility for the application lies with the customer.
Infineon expressly reserves the right to use its content for commercial text and data mining (TDM) according to applicable laws, e.g. Section 44b of the German Copyright Act (UrhG).
If the Product includes security features:
Because no computing device can be absolutely secure, and despite security measures implemented in the Product, Infineon does not guarantee that the Product will be free from intrusion, data theft or loss, or other breaches ("Security Breaches"), and Infineon shall have no liability arising out of any Security Breaches.
If this document includes or references software:
The software is owned by Infineon under the intellectual property laws and treaties of the United States, Germany, and other countries worldwide. All rights reserved. Therefore, you may use the software only as provided in the software license agreement accompanying the software.
If no software license agreement applies, Infineon hereby grants you a personal, non-exclusive, non-transferable license (without the right to sublicense) under its intellectual property rights in the software (a) for software provided in source code form, to modify and reproduce the software solely for use with Infineon hardware products, only internally within your organization, and (b) to distribute the software in binary code form externally to end users, solely for use on Infineon hardware products. Any other use, reproduction, modification, translation, or compilation of the software is prohibited. For further information on the Product, technology, delivery terms and conditions, and prices, please contact your nearest Infineon office or visit https://www.infineon.com