EZ-USB™ HX2G3 hardware design guidelines and schematic checklist

About this document

Scope and purpose

This application note discusses the recommended practices for EZ-USB™ HX2G3 hardware design and the critical items that a designer must consider. With its highly integrated and flexible features, developers can add USB HS hub functionality to any system using EZ-USB™ HX2G3.

Intended audience

This document is intended for anyone who intend to build high speed USB Hub using EZ-USB™ HX2G3 USB2.0 hub controller.

Table of contents

About this document **1**
Table of contents **2**
1 Introduction **3**
1.1 Consumer application 4
2 Related resources **6**
2.1 EZ-USB™ HX2G3 Configuration Utility 6
3 Power system **7**
3.1 Power supply design 7
3.2 Device supply decoupling 8
4 Boot Mode Flow **11**
4.1 I2C Master Mode 11
4.1.1 Selection of I2C EEPROM 11
4.2 I2C Slave Mode 11
4.3 SPI Master Mode 12
4.3.1 Selection of SPI Flash 12
5 Design Considerations **13**
5.1 Crystal 13
5.1.1 Crystal effective load capacitor calculation 14
5.1.2 Layout consideration 14
5.2 Reset Circuit 15
5.3 VBUSDET_IO 15
5.4 Downstream VBUS and Shield Termination 15
5.5 USB Precision Resistors 16
5.6 USB 16
5.6.1 USB HS 16
5.7 Low-Speed peripherals (LPP) 18
5.7.1 I2C interface 18
5.7.2 SPI 18
5.8 Downstream power switch and overcurrent requirement 18
5.9 Ganged and Individual power mode 18
5.10 Power and external regulator requirement 20
6 EMI and ESD considerations **21**
7 Generic electrical design considerations **22**
8 Schematic and layout review checklist **27**
9 Summary **29**
10 Appendix A – PCB layout tips **30**
11 Appendix B – Troubleshooting **31**
11.1 EZ-USB™ HX2G3 device not enumerating 31
References **32**
Revision history **33**
Disclaimer **34**

Table of contents

1 Introduction

EZ-USB™ HX2G3 is a USB2.0 hub controller with a Cortex®-M0+ MCU, 32 KB of SRAM and 32 KB of ROM. It includes six programmable USB2.0 PHYs and one serial communication block (SCB) that supports I2C or SPI. It can run from

- firmware (FW) on ROM or
- firmware can be downloaded from external device like I2C EEPROM, SPI Flash, or
- Firmware can be downloaded from an external I2C master.

EZ-USB™ HX2G3 is available in two packages:
• 40-QFN for commercial/industrial
• 36-LGA for commercial/industrial applications

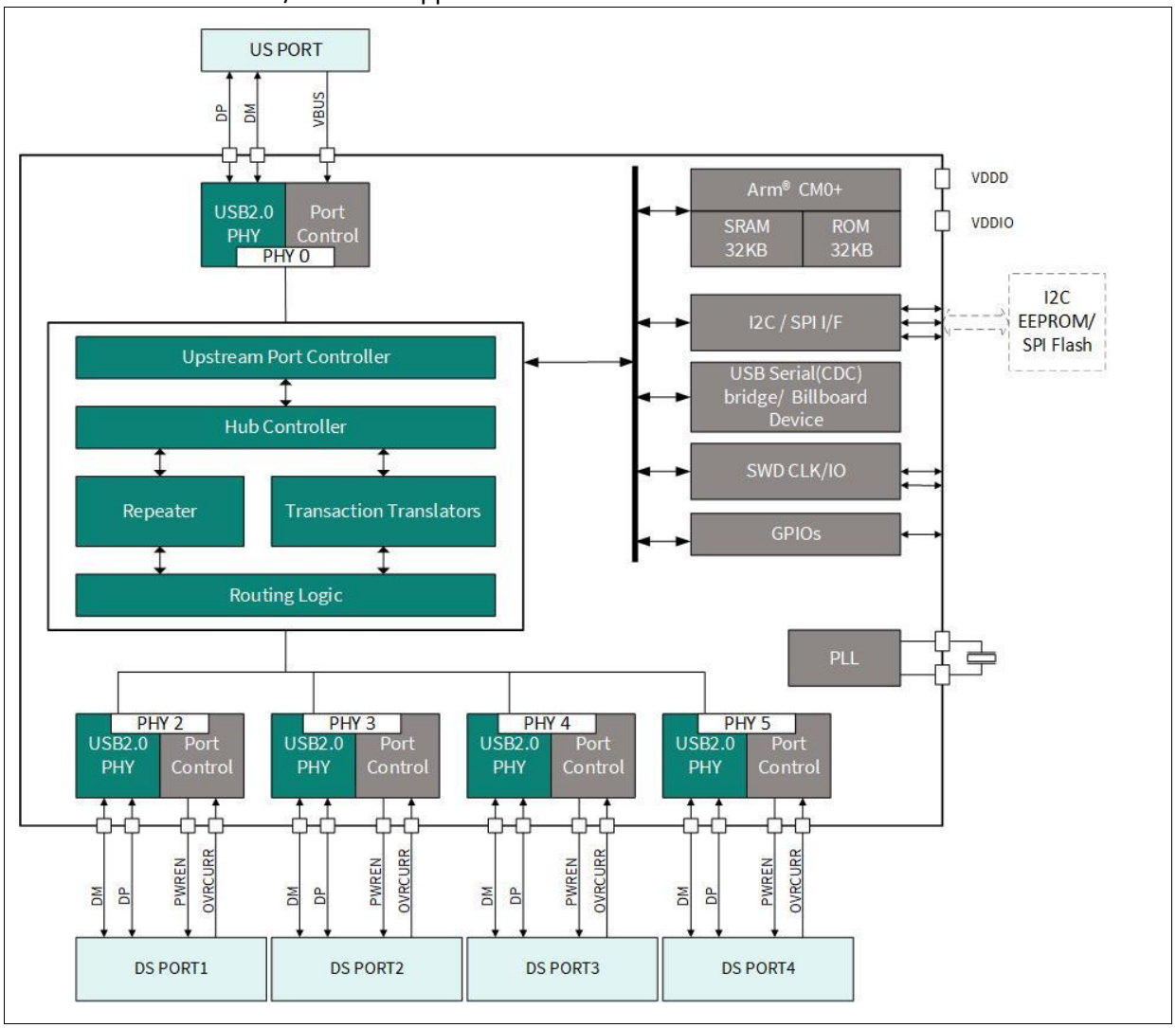


Figure 1 EZ-USB™ HX2G3 architecture block diagram

See the reference schematic of the EZ-USB™ HX2G3 Development Kit (DVK) [3].

This application note provides hardware guidelines for a hub system based on EZ-USB™ HX2G3.

Features	CYUSB2354-40LTXI	CYUSB2352-40LTXI	CYUSB2364-36BFXI
Description	USB 2.0 hub with one upstream and four downstream ports	USB 2.0 hub with one upstream and two downstream ports	USB 2.0 hub for with one upstream and four downstream ports
Number of DS ports	4	2	4
Number of US ports	1	1	1
LDO	No	No	No
Application	Commercial / Industrial	Commercial / Industrial	Commercial / Industrial
Temperature Range	-40 to 85 ° C	-40 to 85 ° C	-40 to 85 ° C
Package	40 QFN, 5 × 5 mm, 0.4 mm pitch	40 QFN, 5 × 5 mm, 0.4 mm pitch	36 LGA, 6 × 6 mm, 0.5 mm pitch
I2C EEPROM Support	Yes	Yes	No
Vendor Commands	Yes	Yes	No

Table 1 EZ-USB™ HX2G3 Product Options

1.1 Consumer application

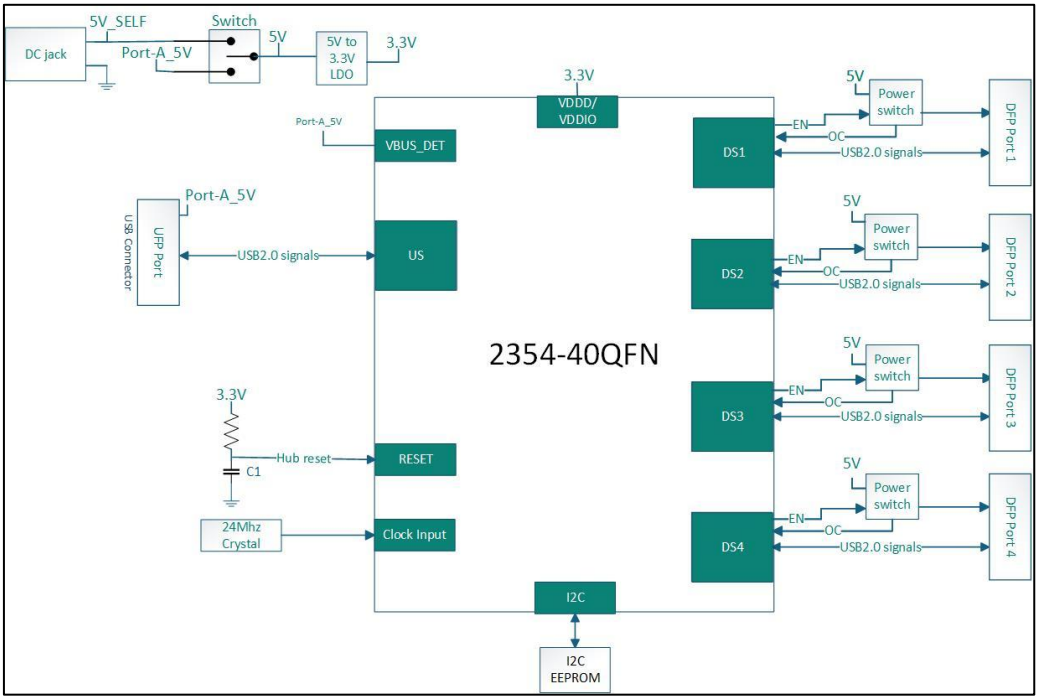


Figure 2 EZ-USB™ HX2G3 (2354-40QFN) as 1:4 Consumer hub

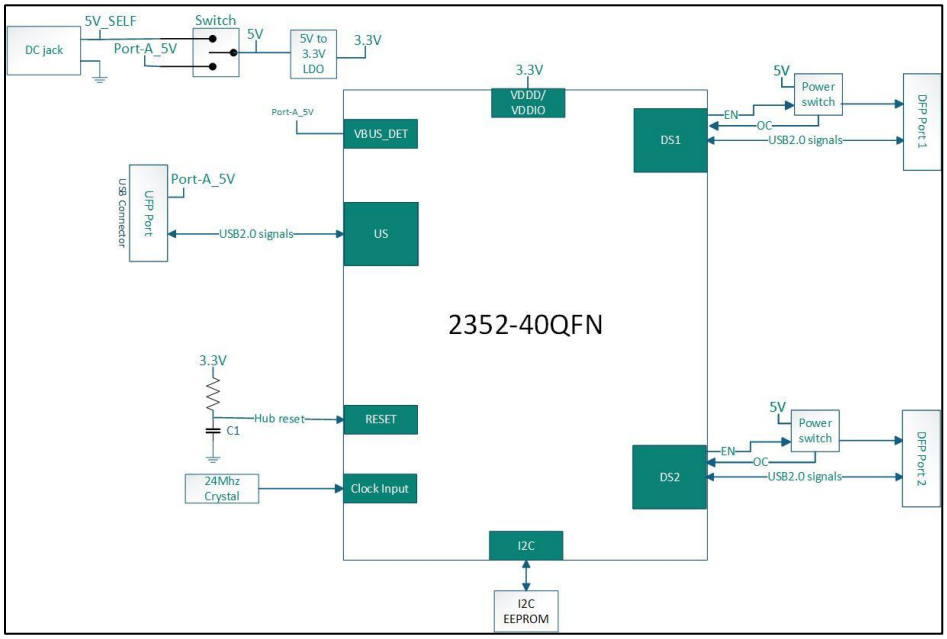


Figure 3 EZ-USB™ HX2G3 (2352-40QFN) as 1:2 Consumer hub

Figure 2 and Figure 3 show a typical consumer application in which EZ-USB™ HX2G3 is a self-powered HUB with 1 Upstream & 4 Downstream (1:4) and 1 Upstream & 2 Downstream (1:2) configuration respectively.

Here EZ-USB™ HX2G3 acts as a generic hub for port extension.

Below is the typical application of 2364-36LGA part where EZ-USB™ HX2G3 is used as a vanilla HUB without power switch. 2364-36LGA part can work with power switch enabled by changing the configuration.

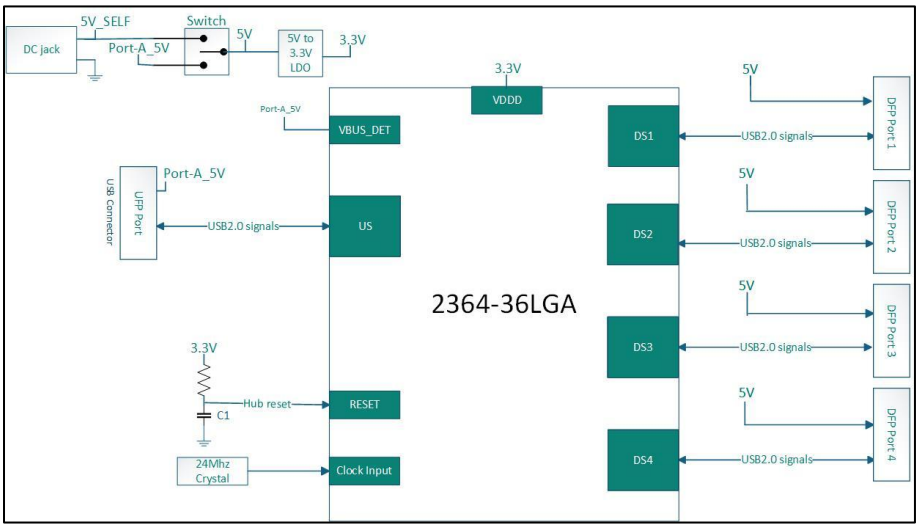


Figure 4 EZ-USB™ HX2G3 (2364-36LGA) as 1:4 Consumer hub

2 Related resources

Infineon Technologies provides a wealth of data on Infineon Developer Community to help you to select the right EZ-USB™ HX2G3 device for your design, and to help you quickly and effectively integrate the device into your design.

- Application notes: Infineon offers a large number of USB application notes covering a broad range of topics, from basic to advanced levels. Recommended application notes for getting started with EZ-USB™ HX2G3 are:
  - EZ-USB™ HX2G3 hardware design guidelines and schematic checklist[1]
- Datasheet:
  - EZ-USB™ HX2G3 Consumer USB 2.0 High-Speed Hub [2]
- Development kits:
  - KIT_HX2G3_235x_40QFN, EZ-USB™ HX2G3 Development Kit [3]
  - Visit the EZ-USB™ HX2G3 webpage to view the development kits available for EZ-USB™ HX2G3.

2.1 EZ-USB™ HX2G3 Configuration Utility

Infineon Technologies delivers the EZ-USB™ HX2G3 configuration utility to configure and program the I2C EEPROM/SPI Flash. Please refer the Kit guide on how to use the Tool to program: EZ-USB™ HX2G3 hardware design guidelines and schematic checklist[1]

3 Power system

EZ-USB™ HX2G3 has the following power domains.

- VDDD is the main digital supply input. It provides the inputs for the internal regulators
- VCCD is the internal core logic supply and needs an external decoupling capacitor
- VDDIO is the GPIO power supply
- VSS is the main ground for the entire chip

3.1 Power supply design

Refer Table 3 for power domain decoupling requirements.

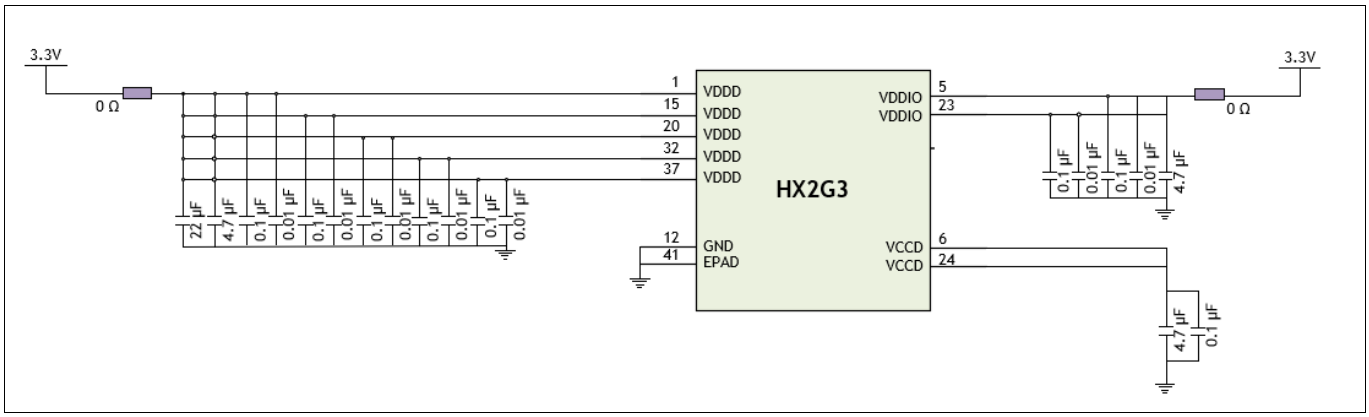


Figure 5 EZ-USB™ HX2G3 power domains for 40QFN

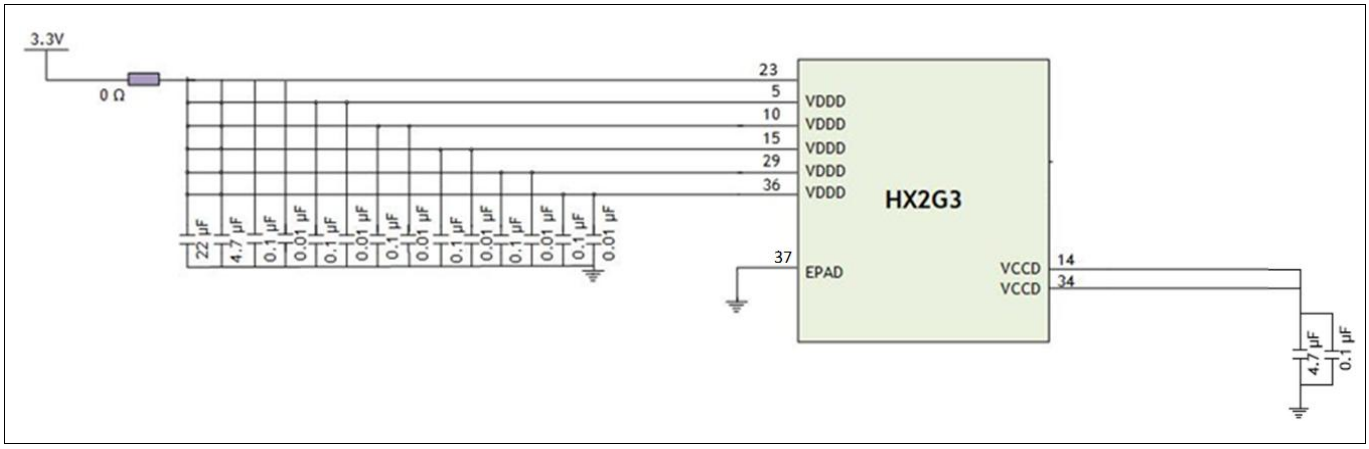


Figure 6 EZ-USB™ HX2G3 power domains for 36LGA

Note: For optimum noise performance of EZ-USB™ HX2G3, a combination of 0.1 µF and 0.01 µF capacitors per pin is required. A power sequence is not needed

Note: For 36LGA, VDDIO & VDDD lines are shorted internally

Table 2 EZ-USB™ HX2G3 power domains for 40QFN

Parameter	Description	Min.	Typ.	Max.	Unit
VDDD	Main analog supply voltage	2.97	3.3	3.63	V
VCCD	Core logic supply output *Note: Do not connect external supply to this pin.*	–	1.1	–	V
VDDIO	Power supply voltage for IO	2.97	3.3	3.63	V

Note: For 36LGA, VDDIO & VDDD lines are shorted internally

3.2 Device supply decoupling

Power supply decoupling is critical in ensuring that system noise does not propagate into the device through the power supply. Improper decoupling can lead to jittery signaling, especially on the USB bus, which results in a higher CRC error rate and more retries. Decoupling capacitors must be the ceramic type of stable dielectric. It is important to have the decoupling caps close to the power pins, and short trace runs for the power and ground connections on the EZ-USB™ HX2G3 device to solid power and ground planes.

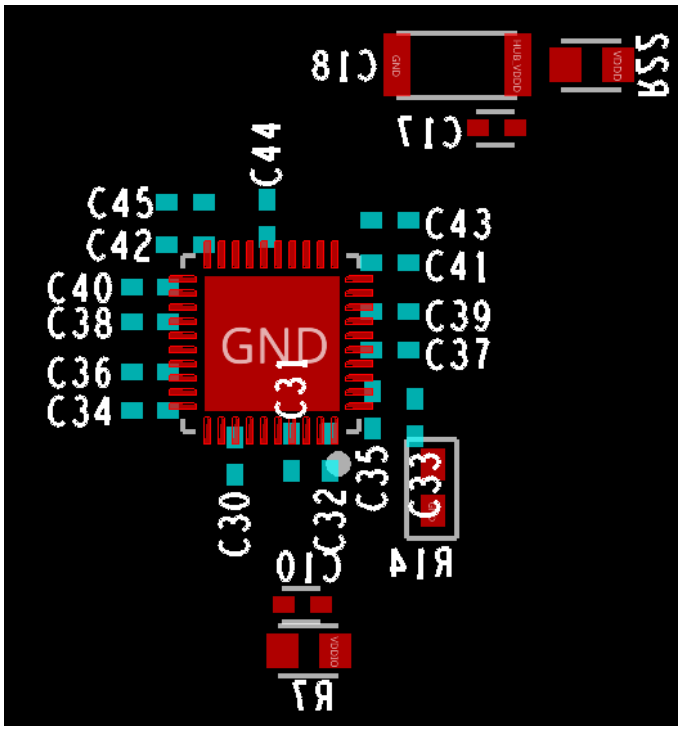


Figure 7 Placement of decoupling caps on the bottom layer of KIT_HX2G3_235x_40QFN DVK

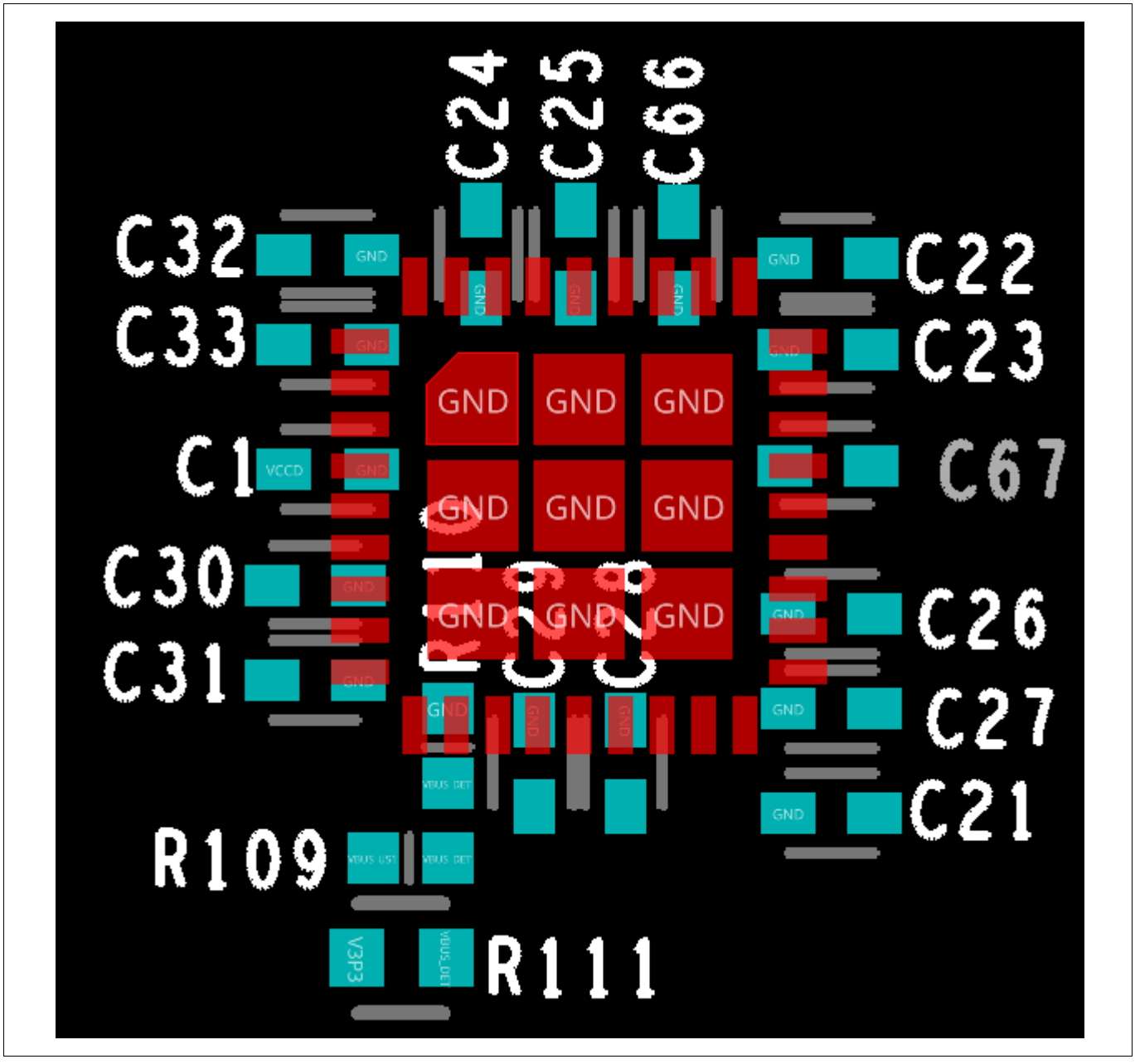


Figure 8 Placement of decoupling caps on the bottom layer of HX2G3 2364 36LGA validation board

In Figure 7 & Figure 8, the top layer is shown in red color, and bottom layer is shown in blue color. All the decoupling capacitors are placed in bottom layer.

The specific recommendation for the ceramic capacitor nearest to each EZ-USB™ HX2G3 power pin is given in Table 3.

Table 3 Power domain decoupling requirements

Power domain (pin numbers)	Capacitors for group	Capacitors per pin
VDDD	22 µF, 10 V, and 4.7 µF, 10 V	0.01 µF, 10 V, and 0.1 µF, 10 V
VCCD	4.7 µF, 10 V and 0.1uF, 10 V	–
VDDIO	4.7 µF, 10 V	0.01 µF, 10 V, and 0.1 µF, 10 V

Note: For 36LGA, VDDIO & VDDD lines are shorted internally

4 Boot Mode Flow

EZ-USB™ HX2G3 has complete ROM code with full USB2.0 stack which is compliant with USB 2.0 specification, and it can work as a fixed FW part. In case any custom FW is needed for any specific application, EZ-USB™ HX2G3 can download firmware from external devices and boot with the new firmware.

Below is the Boot flow of HX2G3.

EZ-USB HX2G3 will try to boot in I2C master mode first, if fails, will try booting in I2C slave mode. If it fails to boot in I2C slave mode as well, it will try booting in SPI master mode. If it doesn't find a SPI master, it will boot from internal ROM.

Depending upon the eFuse setting, the bootloader will allow external booting of EZ-USB™ HX2G3. Please refer the EZ-USB™ HX2G3 Consumer USB 2.0 High-Speed Hub datasheet [2] for details on the sequence with a flow diagram.

4.1 I2C Master Mode

EZ-USB™ HX2G3 Bootloader will configure the internal serial communication block in I2C Master mode and tries to read the external EEPROM over I2C.

If there is an ACK, then that signifies the presence of external EEPROM and start downloading the configuration from EEPROM.

In case of NAK, Bootloader will consider no external EEPROM present and moves to the I2C slave mode.

4.1.1 Selection of I2C EEPROM

- The slave address of the EEPROM is fixed as 0x50 (default EEPROM address).
- The minimum size of EEPROM is 1KB, if only configuration needs to be downloaded.
- Frequency of operation supported are 100KHz, 400KHz, and 1MHz.
- Recommended Pull up on the I2C lines are 2.2 kΩ for all operating frequencies.

4.2 I2C Slave Mode

EZ-USB™ HX2G3 can act as an I2C Slave and external I2C master can download the custom configuration to SRAM of EZ-USB™ HX2G3 and the latter can boot from SRAM.

EZ-USB™ HX2G3 Bootloader will configure the SCB in I2C Slave mode and waits for 100ms to receive any I2C command from the external I2C Master. EZ-USB™ HX2G3 Bootloader will enter in this mode only if the I2C master mode fails.

If any I2C command is received within the stipulated time, then EZ-USB™ HX2G3 continues to be in I2C Slave mode and configuration can be downloaded to SRAM of EZ-USB™ HX2G3 to boot. Maximum allowed time to complete configuration is 5 seconds.

By default, Slave will be configured in 1MHz.

Default I2C slave address for EZ-USB™ HX2G3 is 0x38, but this can be configured to any value using configuration table.

Recommended Pull up on the I2C lines are 2.2 kΩ for all operating frequencies.

4.3 SPI Master Mode

Bootloader will configure EZ-USB™ HX2G3 in SPI Master mode and download the configuration from the SPI flash. EZ-USB™ HX2G3 Bootloader will enter in this mode only if both I2C master mode & I2C Salve mode fails.

4.3.1 Selection of SPI Flash

- The minimum size of SPI Flash is 1KB, if only configuration needs to be changed.
- SPI allows Frequencies 1MHz,5MHz,7.5MHz, and 10MHz.
- Command set: SPI flash should support the following commands to support SPI boot.
    - Read data: 03h with 3-byte addressing
    - Read status register: 05h
    - Write enable: 06h
    - Write data (Page Program): 02h
    - Sector erase: D8h

5 Design Considerations

5.1 Crystal

The EZ-USB™ HX2G3 device has a built-in clock oscillator and uses a 24 MHz external crystal. VDDIO supply is the supply associated with the clock input.

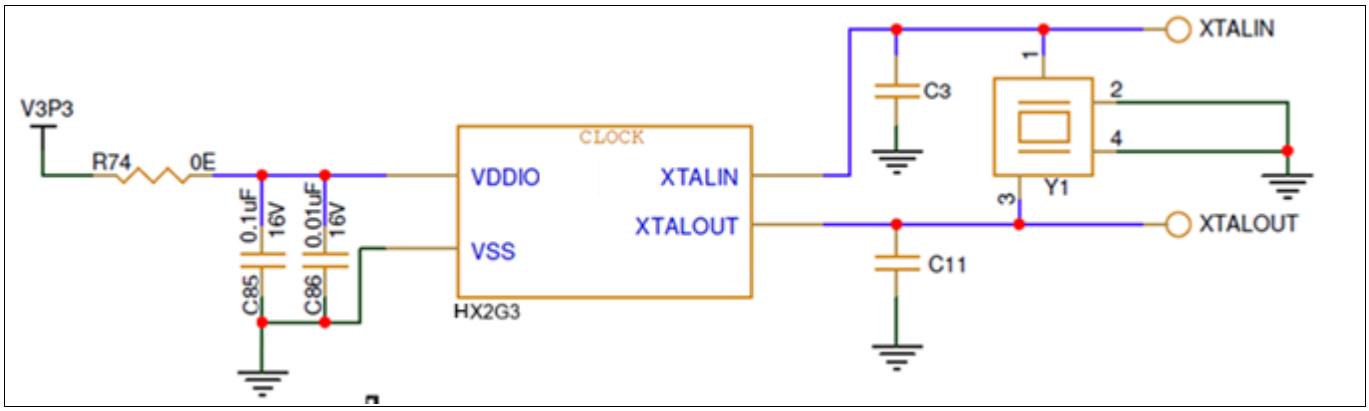


Figure 9 Crystal circuit

Table 4 24 MHz crystal requirements

Parameter	Specification	Unit
Tolerance	< ±30	ppm
Temperature range	–40 to 85	°C
Drive level	Use Equation 1	mW

Note: For more details on crystal specifications, see XTAL/clock specification in the datasheet [2].

The power dissipation of the crystal depends on the following:

- Drive level of the XTALOUT pin (for EZ-USB™ HX2G3, this depends on VDDIO)
- Desired frequency (24 MHz)
- Equivalent resistance of the crystal

$$P = I^2R = \left(\frac{V_x}{|Z|}\right)^2 R = 2[\pi f\ (C_0 + C_L)\ V_x]^2 R$$

Equation 1 Power dissipation of the crystal

Where,

f is the crystal frequency

C_0 is the shunt capacitance of the crystal obtained from the crystal datasheet

C_L is the load capacitance; for CL calculation, see the Crystal effective load capacitor calculation section

R is the crystal ESR obtained from the datasheet of the crystal

V_x is the peak voltage on the XTALOUT pin

Using a crystal with a drive level less than the crystal's power dissipation may result in accelerated aging or even burnout of the crystal.

Examples of compatible crystals are shown in Table 5. Only the ECS-240-8-36CKM-TR is characterized with the EZ-USB™ HX2G3, and the remaining crystals are provided as examples using Equation 1.

Table 5 Crystal selection

Device	Max R (Ω) from the datasheet	CL Eqv (pF)	C0 (pF) estimate	Drive level using Equation 1 (µW)	Max drive level (spec) µW	Manufacturer
ECS-240-8-36CKM-TR	60	8	5	93.38	100	ECS
ABM10W-24.0000MHZ-6-B1U-T3	50	6	2	29.47	100	Abracon

Note: Do not connect any series resistor to the XTALOUT and XTALIN pins of the crystal. Placing a series resistor will add resistance to the crystal ESR, resulting in increased crystal power dissipation and startup time.

5.1.1 Crystal effective load capacitor calculation

Load capacitance C_L plays a critical role in providing an accurate clock source to EZ-USB™ HX2G3. Select the capacitors C_3 and C_{11} (as shown in Figure 9) based on the load capacitance value of the crystal.

The load capacitance is calculated using the following equation:

$$C_L = \frac{C_3 * C_{11}}{C_3 + C_{11}} + C_S$$

Equation 2 Load capacitance of a crystal

C_S is the stray capacitance of XTALOUT and XTALIN traces on the PCB. Generally, the value of C_S is around 2-5 pF if you follow good layout practice and keep the trace from the crystal to the pins on the EZ-USB™ HX2G3 as short as possible.

For the crystal used in EZ-USB™ HX2G3 Development Kit, C_L = 8 pF. EZ-USB™ HX2G3 PCB C_S = 2 pF.
From Equation 2, $C_3 = C_{11}$ = 12 pF.

5.1.2 Layout consideration

- Place crystal as close as possible near EZ-USB™ HX2G3
- Ensure the crystal traces to EZ-USB™ HX2G3 are shortest
- Guard the XTALIN and XTALOUT traces with GND on the same layer
- Provide solid GND for the entire crystal and the traces in the next layer
- XTALIN and XTALOUT traces should be of the same length
- It is recommended to route XTALIN and XTALOUT traces without vias
- Do not place any Hi-Speed signal and reset signal trace near the crystal. If needed because of space constraints, fill the space with ground

Note: See the EZ-USB™ HX2G3 DVK board layout for reference

5.2 Reset Circuit

EZ-USB™ HX2G3 operates with 3.3V (or 1.8V for Dock part) external power supply.

The RESETN pin can be tied to VDDD through an external resistor and to ground (GND) through an external capacitor (minimum 1 us time constant), as shown in Figure 10. This creates a clean reset signal for power-on reset (POR). There is an internal Pull Up resistor of 100kΩ to VDDD inside the HX2G3. Hence external pull up resistor can be omitted. HX2G3 can be put to reset by pulling the XRES pin LOW.

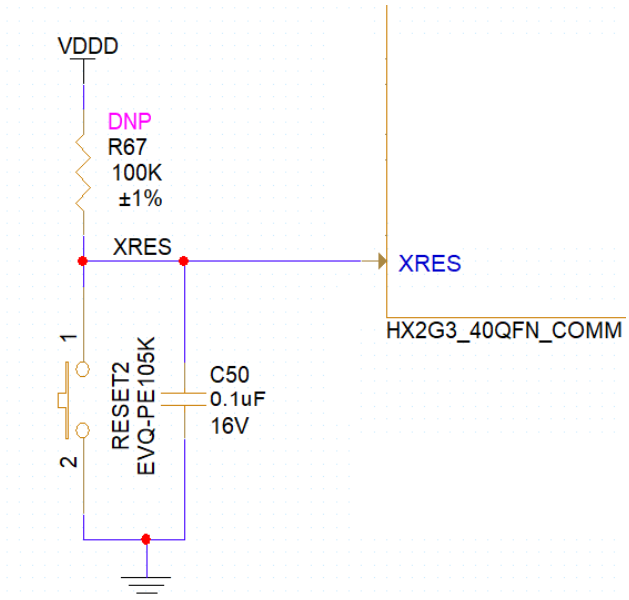


Figure 10 Reset circuit

5.3 VBUSDET_IO

VBUSDET_IO is an active high pin used to initiate the upstream enumeration process. To utilize this pin, connect it to the upstream VBUS through a voltage divider. The voltage divider should be configured to provide an output voltage equal to VDDIO.

5.4 Downstream VBUS and Shield Termination

According to the USB specification, each DS port must have a minimum capacitance of 120 µF on the VBUS pin, to maintain stable voltage under maximum load condition.

The USB connector shield (SHD1 and SHD2) should be terminated to GND with a parallel RC circuit to reduce the EMI as shown in Figure 11.

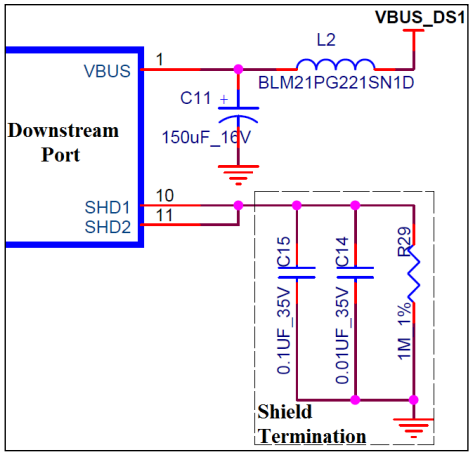


Figure 11 DS VBUS Connection and Shield Termination

5.5 USB Precision Resistors

RREF_USB2: This pin should be connected to a precision resistor (6.04 kΩ ±1%) to generate a current reference for USB 2.0 PHY (as shown in Figure 12).

These resistors should be placed close to HX2G3 and the resistors should be connected to GND using the shortest path.



Figure 12 USB Precision Resistors

5.6 USB

5.6.1 USB HS

EZ-USB™ HX2G3 has an integrated USB HS 480 Mbps PHY that allows connection to a USB-C connector directly. Ensure the following recommendations are considered in the design.

- Minimize the trace length of USB lines as much as possible (< 3 inches). Route these first to ensure certain recommendations on this list are achievable. Long traces affect the transmission quality and introduce inter symbol interference (ISI) on the receiver side
- USB signals must refer to the solid ground plane on the PCB
- It is recommended that the intra-pair (p and n) differential lines should be matched with length within +/- 5 mils.
- Keep the USB signal line impedance at 90 Ω differential (±5%)
- Fill the space around USB signals with the ground. Maintain a minimum of 2W space between the ground and the differential pairs, where W = trace width
- Connect at least one bulk capacitor of >4.7 µF at the USB upstream VBUS pin along with the ceramic capacitors between 22 nF and 100 nF. All capacitors should be rated 10 V or higher to ensure at least 50% derating. The bulk capacitor will maintain the voltage levels in case of a transient current requirement
- Connect 5.1 KΩ ± 1% pull-down resistor on the CC1 and CC2 lines of the USB-C upstream connector
- Connect a 56 KΩ ± 1% Pull-up resistor on the CC1 and CC2 lines of the USB-C downstream connector

- VBUSDET_IO pin of EZ-USB™ HX2G3 is connected to VBUS of the US port via a voltage divider. When a host is connected, VBUS_DET_IO will go high, indicating a connection. Ensure to maintain voltage level equal to VDDIO.
- Shield pins on the USB-C receptacle should be terminated to the ground with a parallel LC (or) RC circuit to avoid EMI/EMC issues. It is recommended to use an RC circuit, as shown in Figure 14
- Use appropriate ESD diodes near the USB-C connector, as shown in Figure 14
- Use USB-IF certified USB-C connectors in the design for optimum performance
- See the EZ-USB™ HX2G3 DVK board file for more details

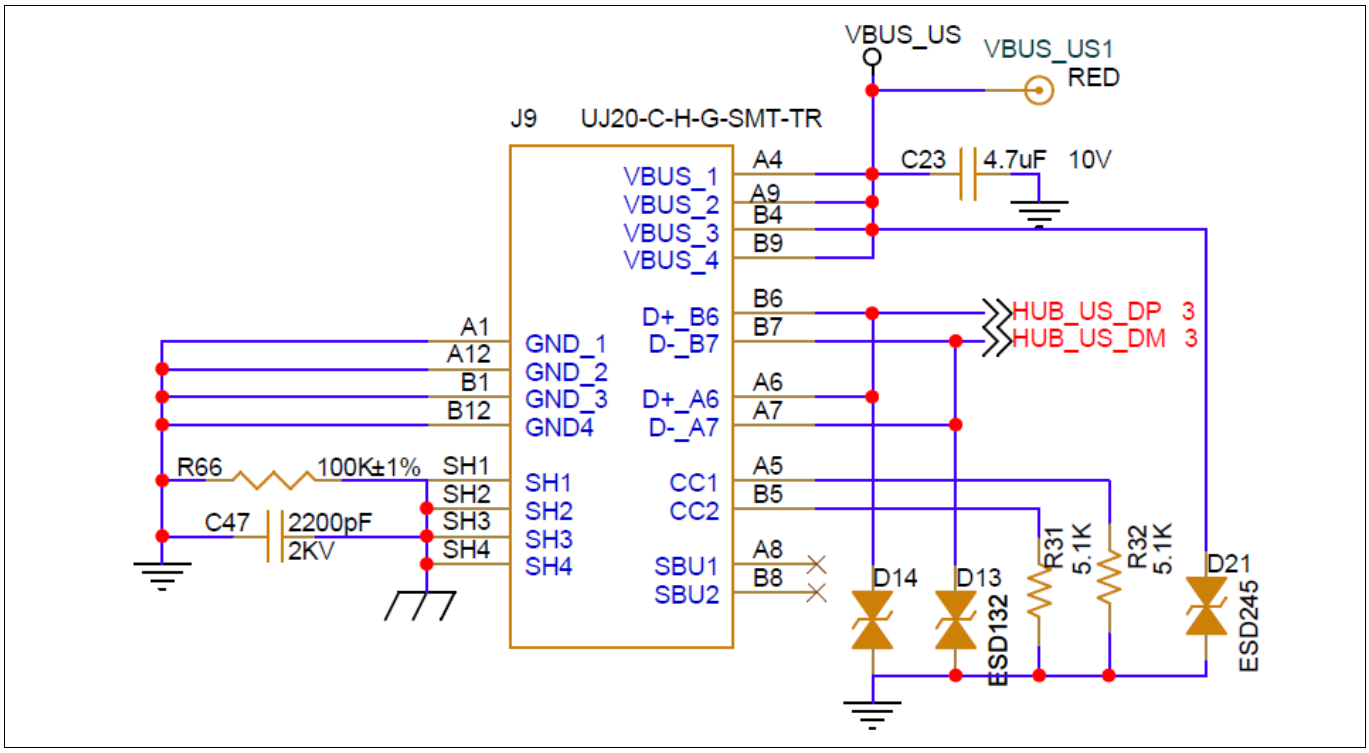


Figure 13 EZ-USB™ HX2G3 interface with USB-C connector

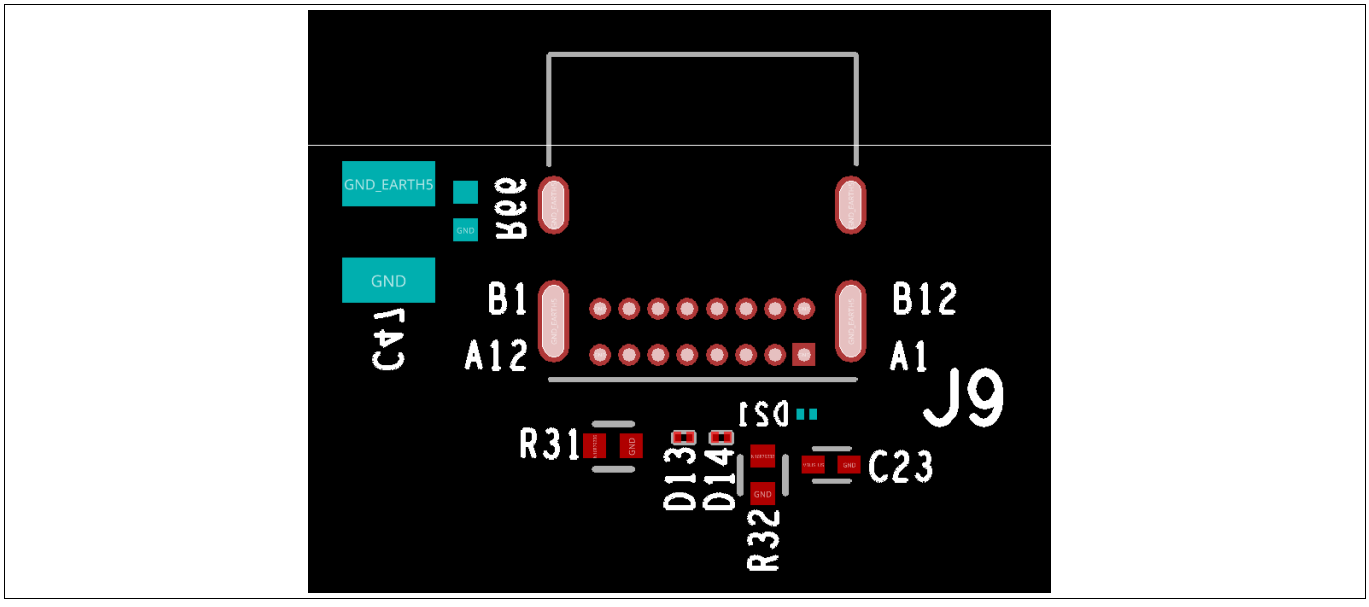


Figure 14 ESD placement in EZ-USB™ HX2G3 interface with USB-C connector

5.7 Low-Speed peripherals (LPP)

EZ-USB™ HX2G3 has one SCB, that can be configured as SPI or I2C. See the “Pin Configurations” section in the datasheet for more details [2].

5.7.1 I2C interface

EZ-USB™ HX2G3 has an I2C interface compatible with the I2C bus specification. The power supply for the I2C interface is VDDIO, which is the power domain for all the other low-speed peripherals. P10.0 and P10.1 are the I2C of the chip. They are overvoltage tolerant up to 5 V.

The bus frequencies supported by the I2C controller are 100 kHz, 400 kHz, and 1 MHz.

The I2C interface can operate at 3.3 V. A 2.2 KΩ ± 1% pull-up to VCCIO voltage is recommended on the I2C lines.

EZ-USB™ HX2G3 2364-36LGA part does not support I2C Interface.

5.7.2 SPI

EZ-USB™ HX2G3 supports single SPI configuration. External SPI flash can be used to store HX2G3 config table and firmware. SPI clock operates at up to 80 MHz. All the data signals should match the length to the clock within 1000 mils.

EZ-USB™ HX2G3 2364-36LGA part does not support SPI Interface.

Note: See the datasheet [2] for appropriate HX2G3 MPN that supports Quad SPI.

5.8 Downstream power switch and overcurrent requirement

Each of the downstream (DS) ports need to provide VBUS to the downstream devices, this DS port’s VBUS must have a power switch to enable or disable the VBUS power in case of any Overcurrent events as shown in Figure 15 & Figure 16

EZ-USB™ HX2G3 has dedicated enable and overcurrent pins for each port. The enable pin nDSx_PWREN can be used to enable or disable the power switch. Fault/overcurrent output from the power switch can be connected to DSx_OVRCURR pins of EZ-USB™ HX2G3 to indicate a fault . EZ-USB™ HX2G3 will disable the power switch by disabling the enable pin for that port.

Both the nDSx_PWREN and DSx_OVRCURR are active low by default and can be configured as active high by updating the config table, flashing the updated config table in external EEPROM and boot EZ-USB™ HX2G3 with EEPROM.

5.9 Ganged and Individual power mode

EZ-USB™ HX2G3 supports ganged and individual power modes for the downstream VBUS. Individual power mode is selected by default in the EZ-USB™ HX2G3’s ROM firmware. To change it to ganged power mode , EZ-USB™ HX2G3’s config table needs to be updated, flashed in an external EEPROM and boot EZ-USB™ HX2G3 from the EEPROM.

In Ganged power mode, all the downstream ports can be controlled using a single enable pin - nGANG_PWREN this is an active low signal by default (can be changed to active high using external config table and external EEPROM) so the power switch must be active low. Similarly, if one of the ports experience an overcurrent event, VBUS of all the ports will be disconnected. Overcurrent/fault pin from the power switch must be connected to

GANG_OVC of EZ-USB™ HX2G3. GANG_OVC is also an active low signal by default, this can be changed using external config table.

In Individual power mode, each downstream port is controlled using a separate enable pin - nDSx_PWREN. This is an active low signal by default (can be changed to active high using external config table and external EEPROM) so the power switch must be active low by default. Since each port is separately controlled, if one of port experiences an overcurrent event, VBUS of that port alone switches off, all the other ports will remain connected. Overcurrent/fault pin from the power switch must be connected to DSx_OVRCURR of EZ-USB™ HX2G3. DSx_OVRCURR is also active low signal by default, this can be changed using external config table.

Note: EZ-USB™ HX2G3 2364-36LGA part does not support ganged & Individual power mode.

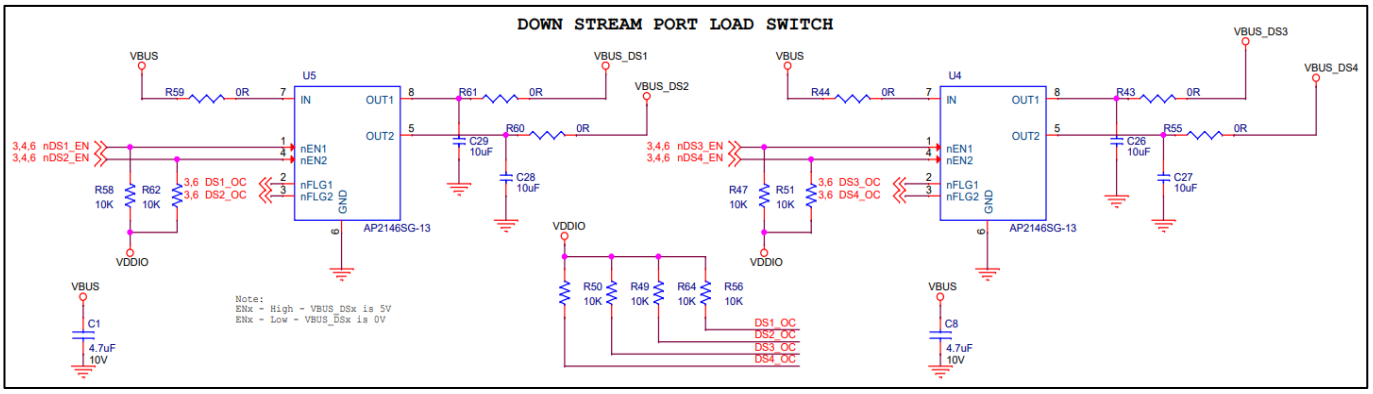


Figure 15 EZ-USB™ HX2G3 power switch in individual power mode

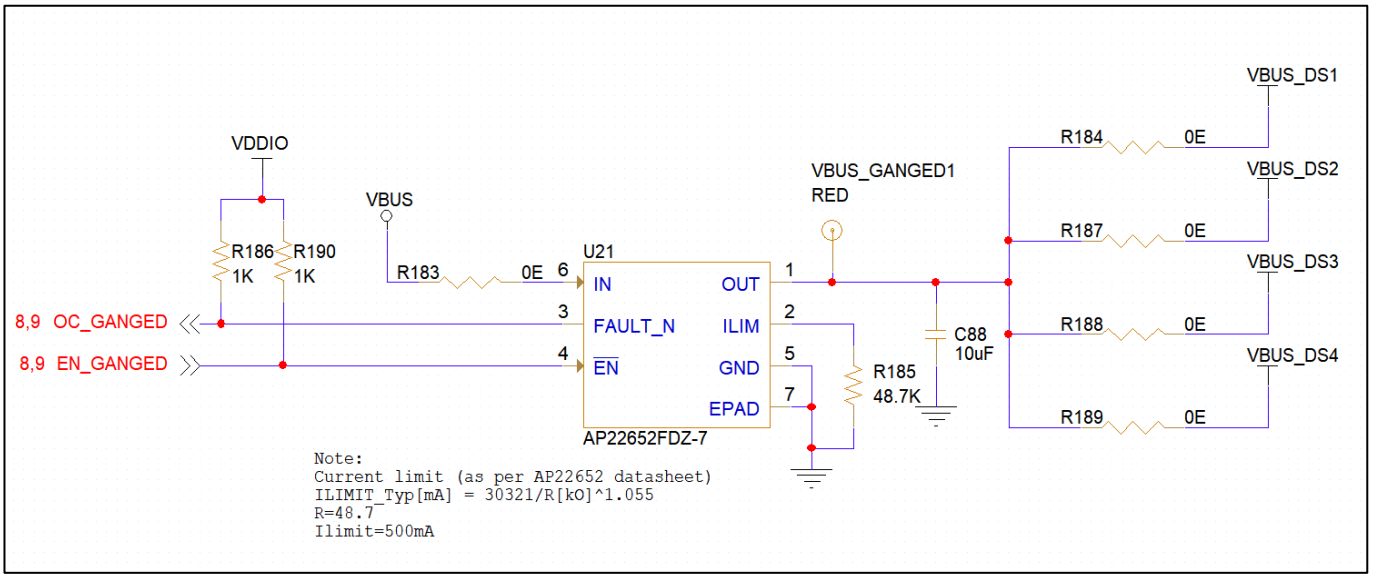


Figure 16 EZ-USB™ HX2G3 power switch in ganged power mode

5.10 Power and external regulator requirement

Below table shows the power consumption details of HX2G3 under various conditions.

Parameter	Description	Power (mW)		
		Min	Typ	Max
HX2G3_SUSPEND	Suspend – upstream port connected and hub in suspend, all DS ports have devices connected	-	-	2.5
HX2G3_L0_SUSPEND	Suspend - upstream port in deep-sleep and hub is in suspend, no devices connected to DS ports	-	-	2.5
HX2G3_NODEVICE	Upstream port in HSIDLE. All downstream ports are disconnected	-	-	140
HX2G3_L0_1HS_RW	One upstream and one downstream port active	-	-	250
HX2G3_L0_2HS_RW	One upstream and two downstream ports active	-	-	350
HX2G3_L0_3HS_RW	One upstream and three downstream ports active	-	-	450
HX2G3_L0_4HS_RW	One upstream and four downstream ports active	-	-	500

6 EMI and ESD considerations

All pins of EZ-USB™ HX2G3 support ±2.2 kV human body model (HBM)-based on JESD22-A114 specification.

Provide the IEC protection at the system level. Provide additional protection to all pins with user interface by using high-performance and low-capacitance external ESD devices. See Figure 14 for the Infineon Technologies ESD diodes used on the USB lines of the USB connector. ESD132 diodes provides ±30kv contact and ±30kv air discharge protection for data lines with low line capacitance and ESD245 diodes provide ±15kv contact and ±18kv air discharge protection.

Regarding EMI, all signal and clock traces emit electromagnetic (EM) radiation when they switch from one level to another. To meet the various standards in different countries, minimize these emissions. Several techniques can be implemented during the design to lower EM emissions in all high-speed signals (USB):

- Consider placing the power and ground planes as the outside layers with signal layers underneath
- Always have solid copper fills beneath integrated circuits and clocks
- Ensure an adequate ground return path for all the signals
- Minimize the trace length of high-speed and high-current traces

7 Generic electrical design considerations

See Appendix A – PCB layout tips for general information on PCB layout techniques.

- Place the capacitor used in the RC reset circuitry as close as possible to the reset pin of EZ-USB™ HX2G3
- Use split planes on the power layer for different power domains
- Keep the power traces away from high-speed data and clock lines
- Power trace widths should be ≥25 mils to reduce the inductance
- Keep power traces as short as possible. Use larger vias (at least 30-mil pad, 15-mil hole) on power traces
- Avoid any split in the immediate plane under the USB lines. The presence of a split under the USB trace will result in a variation of characteristic impedance at that point
- Keep trace spacing between differential pairs consistent to avoid impedance mismatches as shown in Figure 17

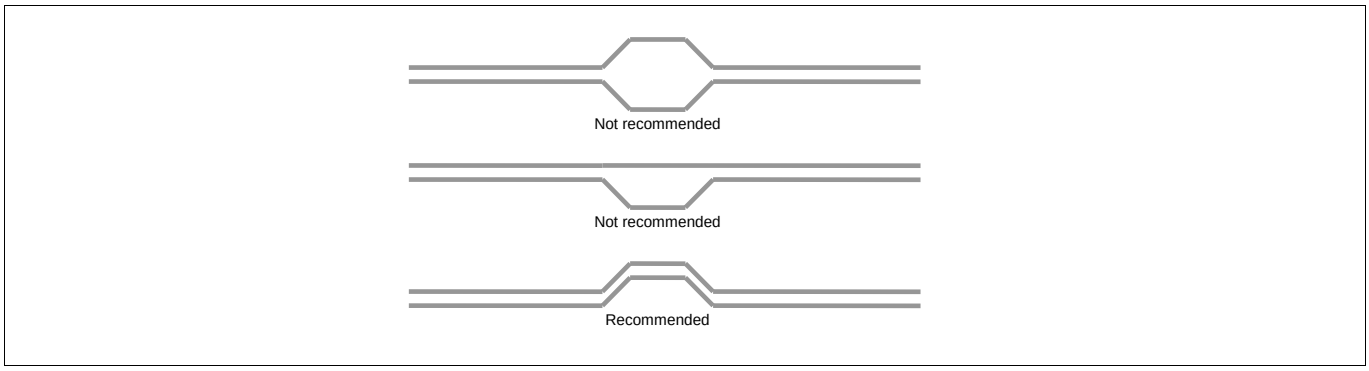


Figure 17 Differential pairs impedance matching techniques

- All USB signal lines should be routed entirely over a solid ground plane on an adjacent layer. Splitting the ground plane underneath the USB signals increases loop inductance introduces impedance mismatches and increases electrical emissions. See Figure 18

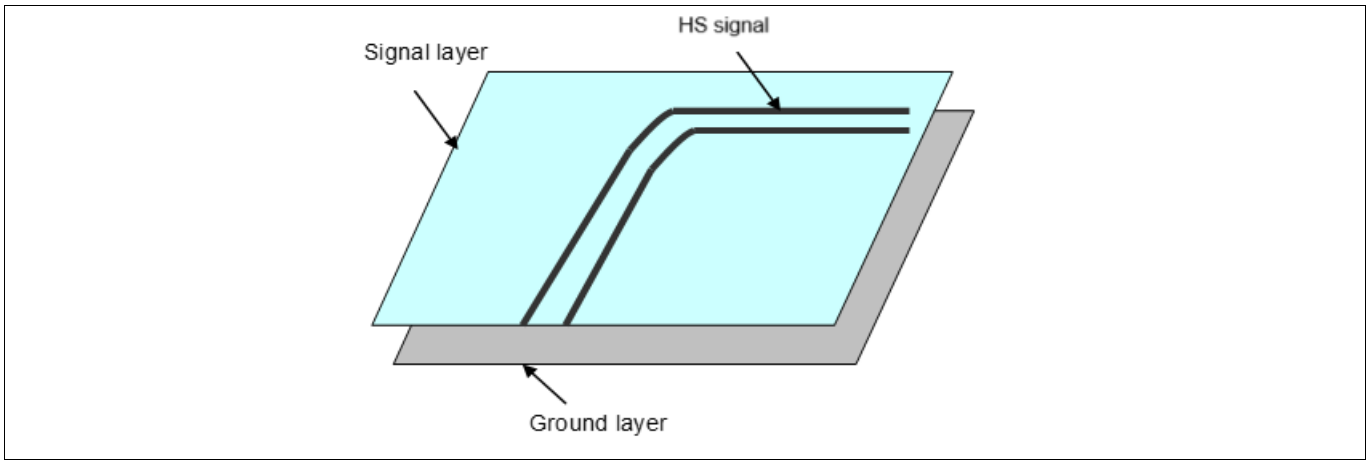


Figure 18 Solid ground plane under the Hi-Speed signal

- Whenever two pairs of USB traces cross each other in different layers, a ground layer should run between the two signal layers. See Figure 19

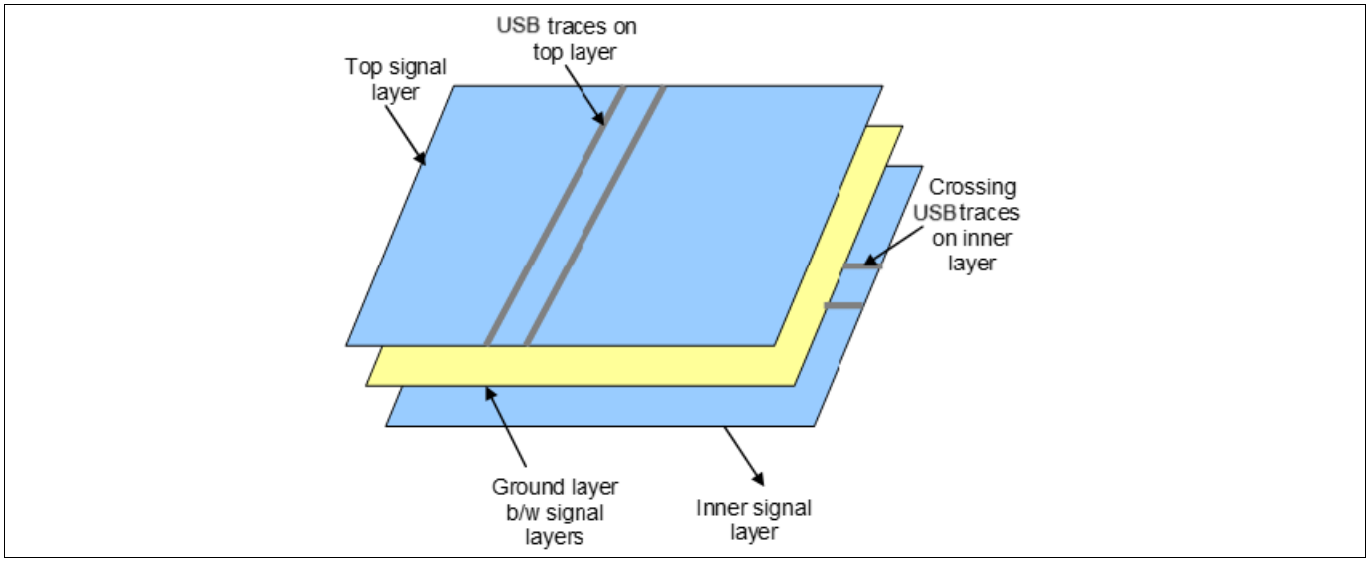


Figure 19 Ground insertion

- On the USB signal lines, use as few bends as possible. Do not use a 90-degree bend. Use 45-degree or rounded (curved) bends if necessary. See Figure 20

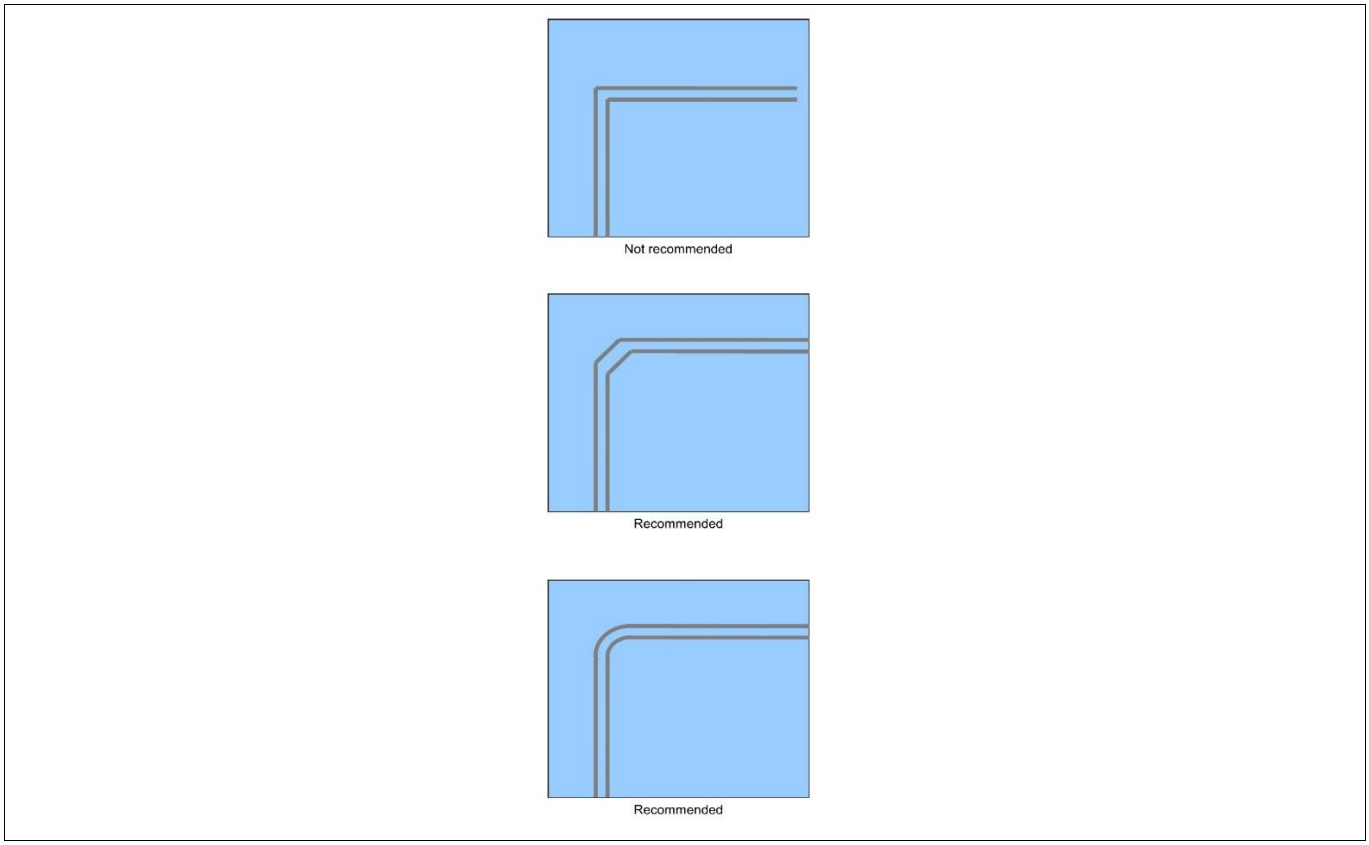


Figure 20 USB signal bends

- Intra-pair differential trace lengths should be matched within 0.12 mm (5-mils). Always adjust for USB signal trace lengths near the USB receptacle and not near the device. Always adjust the length at the mismatched ends. An example of length matching for the USB signal is shown in Figure 21

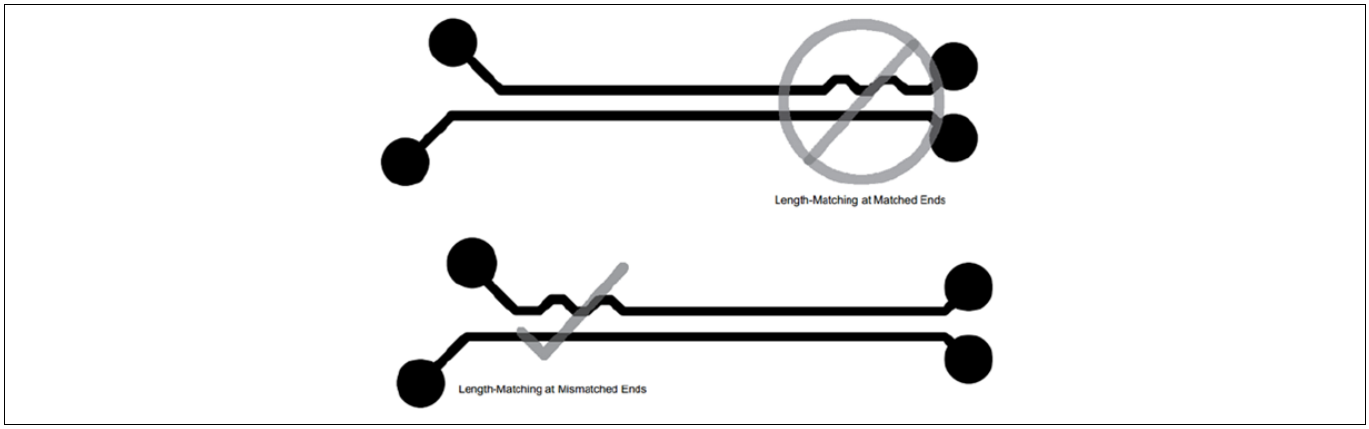


Figure 21 Intra-pair differential signal length matching

- There are different routing methods for length matching: single arc routing and serpentine routing methods. See Figure 22 and Figure 23 for single arc routing and serpentine routing respectively

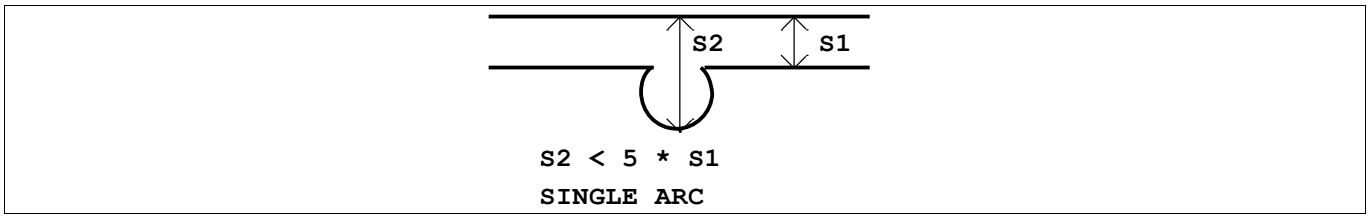


Figure 22 Single arc routing

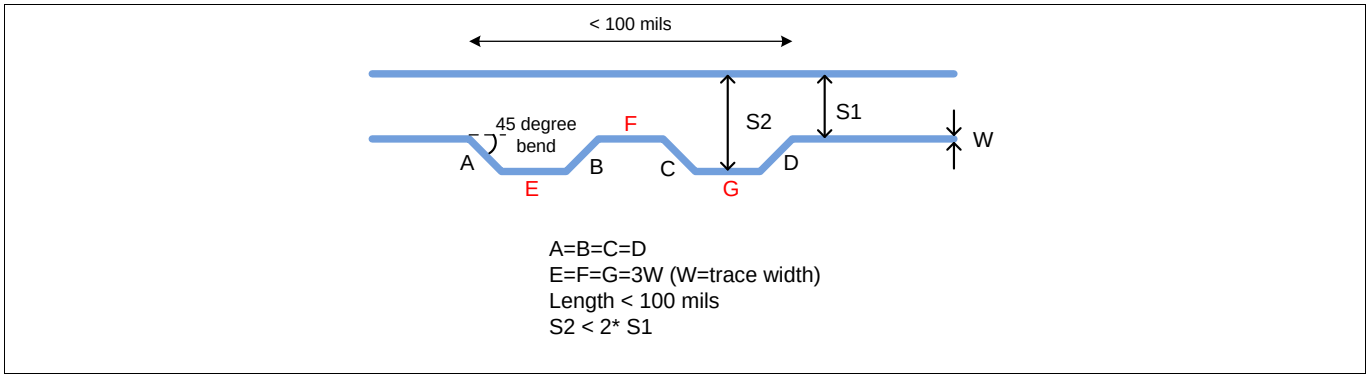


Figure 23 Serpentine routing

- The number of layers on the PCB should be at least four
- If signal routing must be changed to another layer, continuous grounding has to be maintained to ensure uniform impedance throughout. To achieve this, it is good to have ground vias next to signal vias. The distance between the signal and ground vias should be at least 40 mils. See Figure 24

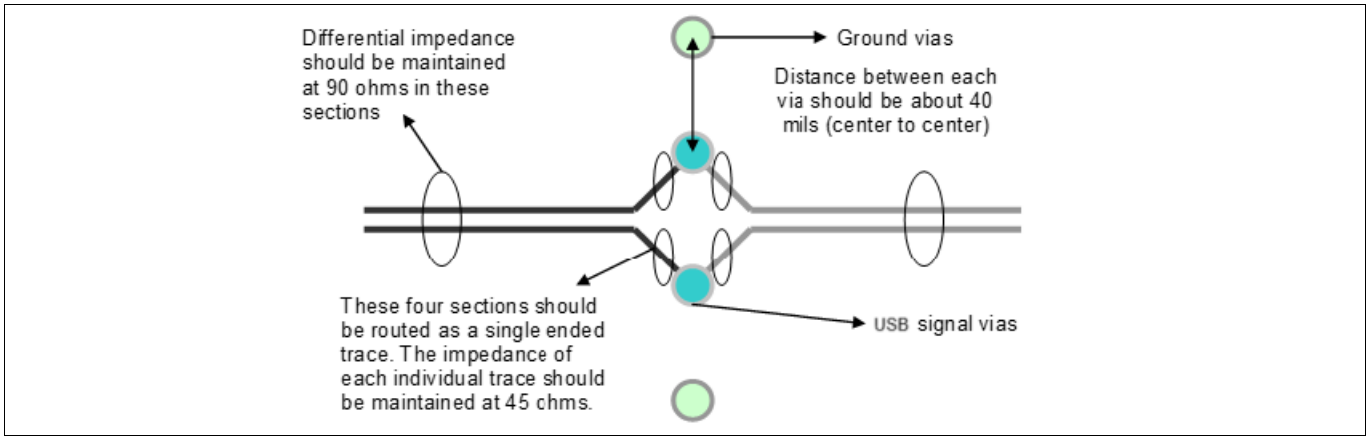


Figure 24 Ground vias

- Maintain constant trace width in differential pairs to avoid impedance mismatches:

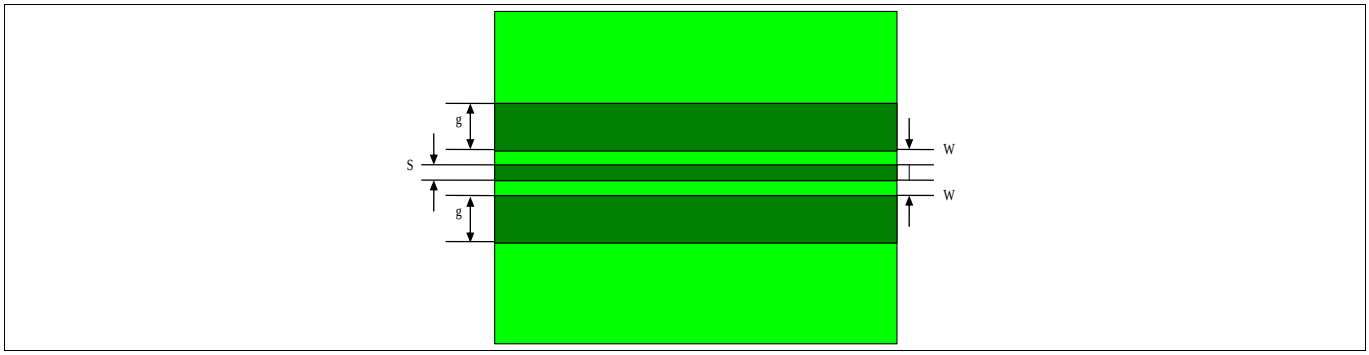


Figure 25 Differential pairs placements

- Avoid stubs on all Hi-Speed lines. If pads are needed on the lines for probing purposes, they should not extend out of the trace in the form of a stub. See Figure 26

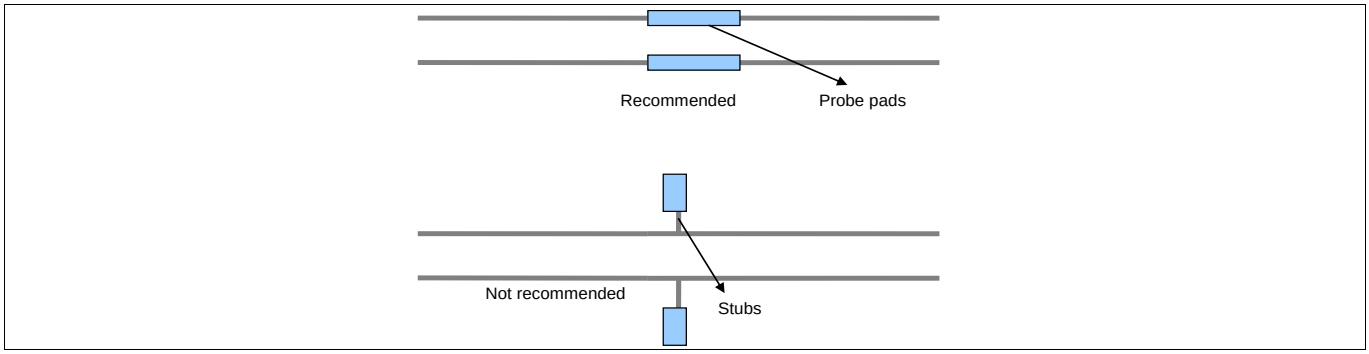


Figure 26 Probing pads placement

- Void for vias on the high-speed signal lines should be common for the differential pair. A common void, as shown in Figure 27, maintains better impedance matching in comparison to separate vias

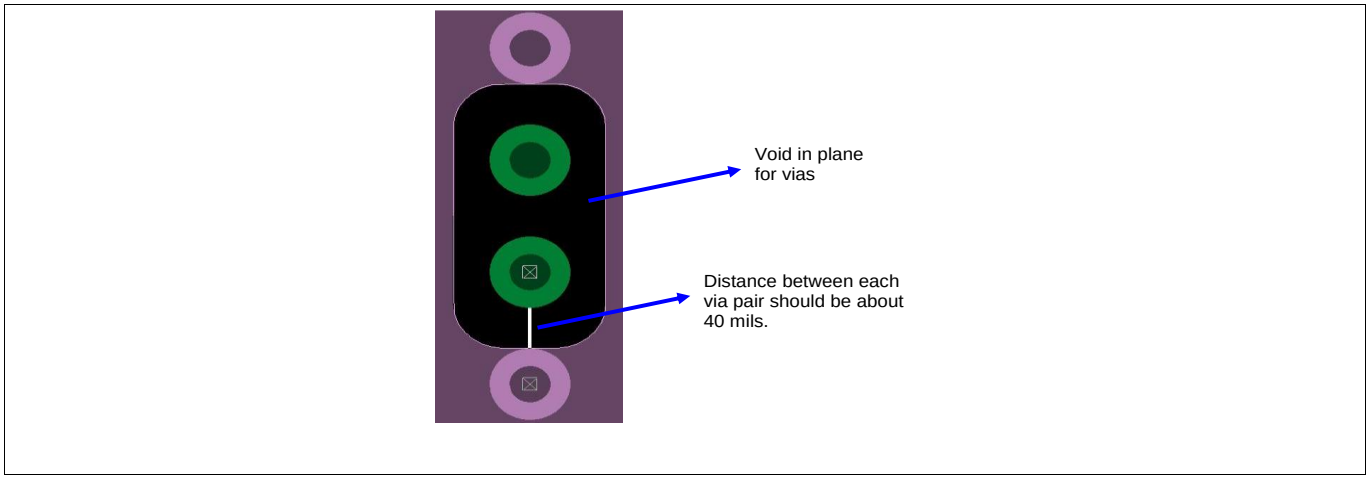
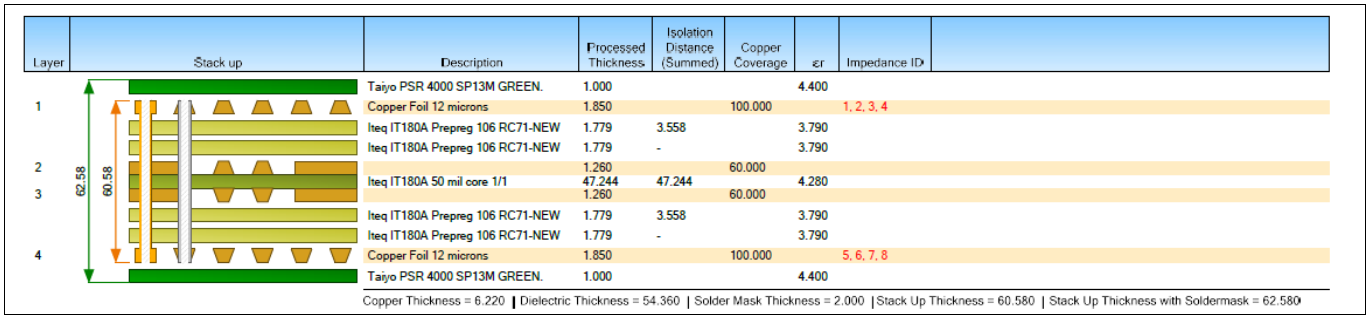


Figure 27 Void vias placement for high-speed differential traces

- To avoid cross-talk, do not place the differential pairs close to other differential pairs, clock signals, or high-speed signals. It is recommended to maintain a 3x distance with other differential pair and other signals where ‘x’ is the width of the signal trace
- Figure 28 shows an example of a four-layer stack up from the EZ-USB™ HX2G3 development kit. This is captured using the Polaris tool



Layer	Stack up	Description	Processed Thickness	Isolation Distance (Summed)	Copper Coverage	εr	Impedance ID
		Taiyo PSR 4000 SP13M GREEN.	1.000			4.400	
1		Copper Foil 12 microns	1.850		100.000		1, 2, 3, 4
		Iteq IT180A Prepreg 106 RC71-NEW	1.779	3.558		3.790	
		Iteq IT180A Prepreg 106 RC71-NEW	1.779	-		3.790	
2			1.260		60.000		
3		Iteq IT180A 50 mil core 1/1	47.244	47.244		4.280	
			1.260		60.000		
		Iteq IT180A Prepreg 106 RC71-NEW	1.779	3.558		3.790	
		Iteq IT180A Prepreg 106 RC71-NEW	1.779	-		3.790	
4		Copper Foil 12 microns	1.850		100.000		5, 6, 7, 8
		Taiyo PSR 4000 SP13M GREEN.	1.000			4.400	

Copper Thickness = 6.220 | Dielectric Thickness = 54.360 | Solder Mask Thickness = 2.000 | Stack Up Thickness = 60.580 | Stack Up Thickness with Soldermask = 62.580

Figure 28 Stackup details for EZ-USB™ HX2G3 Development Kit

8 Schematic and layout review checklist

Table 6 and Table 7 list the checklist for all the important guidelines. Respond to each checklist item to determine the extent to which your hardware design meets these guidelines. A design that satisfies all the schematic and layout checklists will work without any system-level hardware issues.

Table 6 Schematics checklist

Sl. no	Schematic checklist	Answer (Yes/No/NA)
1	Are the decoupling capacitors and bulk capacitors connected according to Table 3?	
2	Does the crystal meet the specification in this application note according to Table 4?	
3	Do the power-on-reset RC components meet the minimum reset time requirement of >1 µs?	
4	Is 5.1 KΩ resistor pull-down connected to CC1 and CC2 lines of upstream port if Type-C connector is used?	
5	Is 56K resistor pull-up to VBUS connected on the CC1 and CC2 lines of downstream port if Type-C connector is used??	
6	Does the USB port shield terminate with the RC circuit?	
7	Do the USB traces have an ESD device connected?	
8	Is the VBUSDET_IO pin connected to VBUS through a voltage divider such that the output of the divider is VDDIO.	
9	Does the RREF is 6.04kΩ?	
10	Does the SPI flash meet the specification in this application note according to Section 5.7.2?	
11	Does the VBUS pin of USB downstream connector has a 120 µF bulk capacitor?	
12	Does the VBUS pin of USB upstream connector has a 10 µF bulk capacitor?	
13	Does the VBUS pin of EZ-USB™ HX2G3 device has overvoltage protection?	
14	Does the power switch used for DS ports have Active low Enable?	
15	Does the OC pin have a pull up of 10kΩ to VDDIO?	
16	Are the Power switch rated for required current?	
17	Are the I2C lines provided with pull-up resistors to the VDDIO domain?	
18	Are all port shields terminated properly?	
19	Is it ensured that power switch has fast discharge?	

Table 7 Layout checklist

Sl. no	Layout checklist	Answer (Yes/No/NA)
1	Is the crystal placed close to the chip (less than 2 cm)?	
2	Are the decoupling capacitors and bulk capacitors placed close to the EZ-USB™ HX2G3 power pins?	

Schematic and layout review checklist

Sl. no	Layout checklist	Answer (Yes/No/NA)
3	Are the clock traces routed away from the high-speed data lines and the power lines?	
4	Are the power traces routed away from the high-speed data lines and the clock lines?	
5	Is the capacitor in the RC reset circuitry placed close to the reset pin of EZ-USB™ HX2G3?	
6	Do the USB HS signal lines have a 90 Ω differential impedance?	
7	Are the USB HS signal lines intra-pair match done with in 5 mils?	
8	Are the USB data lines provided with a solid ground plane underneath?	
9	Are the crystal signals provided with the guard traces?	
10	Do the USB traces have few bends and no 90-degree bend?	
11	Are the USB traces kept less than 3 inches?	
12	Is it ensured that there are no stubs on all the USB traces?	
13	Is the 120-µF capacitor placed close to the DS port connector?	

9 Summary

The developer must consider the recommended practices for EZ-USB™ HX2G3 hardware design and the critical items discussed in this document.

10 Appendix A – PCB layout tips

There are many classic techniques for designing PCBs for low noise and EMC. A few of these techniques include:

- **Multiple layers:** Although they are more expensive, it is best to use a multi-layer PCB with separate layers dedicated to the ground and power supplies. This gives good decoupling and shielding effects
- **Component position:** Separate the different circuits on the PCB according to their electromagnetic interference (EMI) contribution. This will help reduce cross-coupling on the PCB. For example, separate noisy high-current circuits, low-voltage circuits, and digital components
- **Ground and power supply:** There should be a single point for gathering all ground returns. Avoid ground loops or minimize their surface area. All component-free surfaces of the PCB should be filled with additional grounding to create a shield, especially when using a two-layer PCB
- The power supply should be close to the ground line to minimize the area of the supply loop. The supply loop can act as an antenna and can be a major emitter or receiver of EMI
- **Decoupling:** The standard decoupler for external power is a 100-µF capacitor. Supplementary 0.1-µF capacitors should be placed as close as possible to the GND and supply pins of the device to reduce high-frequency power supply ripple

Generally, decouple all sensitive or noisy signals to improve electromagnetic compatibility (EMC) performance. Decoupling can be both capacitive and inductive.

- **Signal routing:** When designing an application, the following areas should be closely studied to improve EMC performance:
  - Noisy signals, for example, signals with fast edge times
  - Sensitive and high-impedance signals
  - Signals that capture events, such as interrupts and strobe signals

To increase EMC performance, keep the trace lengths as short as possible and isolate the traces with V_{SS} traces. To avoid cross-talk, do not route them near to or parallel to other noisy and sensitive traces.

11 Appendix B – Troubleshooting

11.1 EZ-USB™ HX2G3 device not enumerating

Many factors contribute to the EZ-USB™ HX2G3 enumeration issue. A few of these points include:

- **USB-C receptacle to EZ-USB™ HX2G3 device connections:** Check if CC lines are terminated with a 5.1 kΩ resistor
- **Power domain isolation:** Ensure that EZ-USB™ HX2G3 power supplies are isolated and connected with ferrite beads. Also, the source of these supplies should have noise/ripple less than 100 mV

References

For all EZ-USB™ HX2G3 related documents, visit the EZ-USB™ HX2G3 webpage.

Application note

[1] Infineon Technologies AG: *EZ-USB™ HX2G3 hardware design guidelines and schematic checklist;* Available online

Datasheet

[2] Infineon Technologies AG: *002-41112: CYUSB231x EZ-USB™ HX2G3 USB 2.0 high-speed peripheral controller* Available online

Development kits

[3] Infineon Technologies AG: *KIT_HX2G3_235x_40QFN: EZ-USB™ HX2G3 Development Kit;* Available online

Tools

[4] Infineon Technologies AG: EZ-USB™ HX2G3 configuration utility*;* Available online

Revision history

Document revision	Date	Description of changes
**	2026-06-19	Initial release

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2026-06-19

Published by

Infineon Technologies AG

81726 Munich, Germany

© 2026 Infineon Technologies AG. All Rights Reserved.

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

002-42358 Rev. **

Important notice

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Warnings

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.