EZ-PD™ PAG2x: Design guidelines for reducing conducted emissions in flyback converters

About this document

Scope and purpose

This document provides design guidelines to reduce conducted emissions (CE) for power adapters based on EZ-PD™ PAG2x devices. The PAG2x device is a ZVS flyback converter chipset with USB Power Delivery (PD), synchronous rectifier (SR), and pulse width modulator (PWM).

Additionally, the document shows how the low-side SR provides similar CE performance compared to the high-side SR based on the simulation. It also describes the common-mode current in flyback converters with SR in both the high-side and low-side configurations and provides the experimental CE test results based on the proposed design guidelines in low-side SR.

Intended audience

This document is intended for power electronics hardware designers.

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1 Introduction

The application note introduces design techniques to reduce conducted emissions (CE) for Infineon's EZ-PD™ PAG2P and PAG2S secondary-side controllers. The controllers feature AC-DC topologies like active clamp flyback (ACF) and quasi-resonant (QR) zero-voltage switching (ZVS). PAG2P and PAG2S ICs are targeted for USB PD chargers; they are best suitable for high-efficiency AC-DC flyback designs with USB PD, Qualcomm Quick Charge, and other standard charging protocols. PAG2S also supports USB PD Extended Power Range (EPR) mode.

PAG2P interfaces with the rectified output from the AC mains on the primary side and receives the necessary PWM signal from the secondary side to provide a regulated output voltage. PAG2P is designed to complement a secondary-controlled AC/DC flyback converter topology. In this approach, voltage and current regulation is performed by the secondary controller (PAG2S). PAG2P is responsible for providing the startup function, driving the primary-side FET, and responding to fault conditions.

EZ-PD™ PAG2S is an integrated secondary-side PWM controller and USB PD controller. PAG2S integrates secondary-side synchronous rectifier (SR), PWM, and ACF control. In addition to being the secondary controller, PAG2S also controls ACF/QR ZVS operation to achieve higher efficiency and ZVS operation. PWM and ACF signals are transferred to the primary side through the same pulse-edge transformer. PAG2S uses time multiplexing to transfer PWM and ACF signals. In addition to driving the primary side switch, PAG2S also performs the SR controller function. PAG2S features the low-side SR FET for easy driving. For more details, see the PAG2P [1] and PAG2S [2] datasheets.

In flyback converters, generally, the secondary side SR can be placed either at the high side or low side. PAG2S supports low-side SR gate driving. Low-side SR provides advantages of ease of operation and lower BOM cost.

This application note presents the aspects of common-mode current in flyback converters when the SR is at high side and low side. The comparative study of low-side SR vs. high-side SR is augmented with simulation. Subsequently, common-mode emission reduction techniques are explained for low-side SR. The reduction techniques are validated through experimental results.

2 Conducted emission (CE)

2.1 Common-mode and differential mode currents

USB PD chargers have high voltage and current switching nodes on both primary and secondary sides of the coupled inductor/transformer. This results in sources of both conducted and radiated emissions (CE and RE). Limiting these emissions is imperative for seamless and safe operation of the charger. There are many regulatory standards which govern the maximum allowed emissions. For USB PD chargers, the most prevailing standard is CISPR 32 Class B. This application note mainly describes the common-mode current sources, their path, comparative study of SR in high-side vs. low-side, and design techniques to minimize the CE for low-side SR.

The CE is affected by common-mode (CM) and differential-mode (DM) emissions. Differential mode currents flow from AC mains/line to the power supply and back to the AC neutral. The harmonics in input switching current and switching noise are the main sources of DM CE currents.

Common-mode CE are caused by common-mode currents that start from the AC mains line/neutral or both and take a return path from earth via the parasitic capacitances. Figure 1 provides common-mode and differential current paths in a flyback converter. The primary sources of CM CE are the primary-side switching node and the secondary-side SR FET switching nodes.

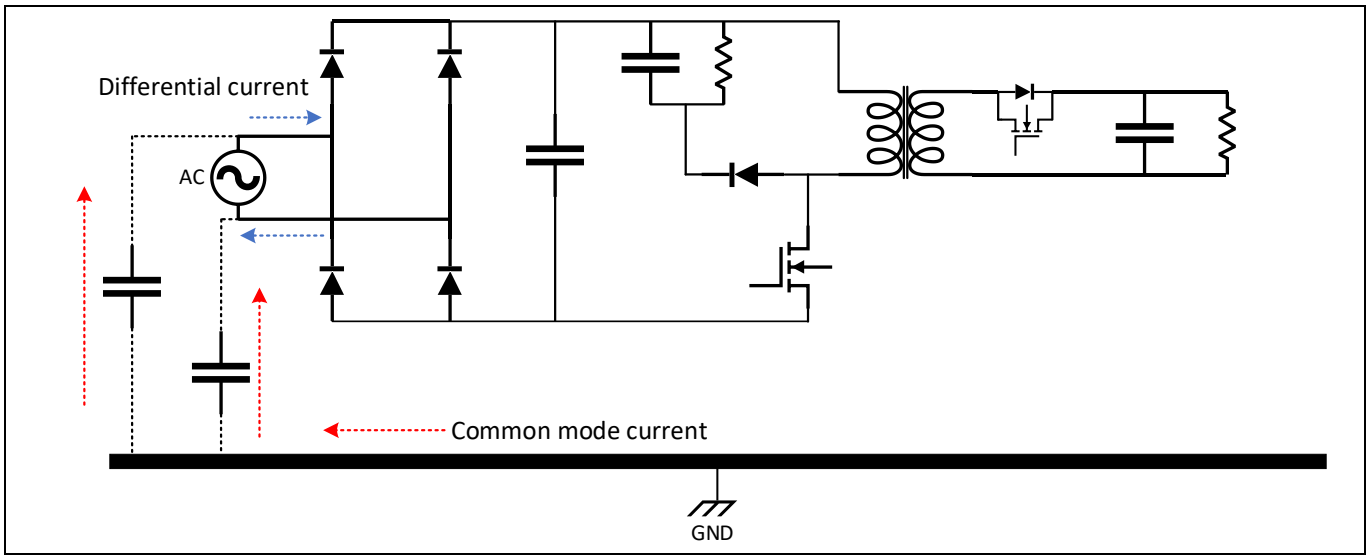


Figure 1 Common-mode and differential-mode current in a flyback converter

2.2 Position of secondary SR in flyback converters

Synchronous rectifiers are used mainly to achieve higher efficiency. In flyback converters, they can be placed either on the low side or on the high side as shown in Figure 2. From the efficiency point of view, placing a synchronous rectifier on the low side or high side is identical. However, implementing the gate driver power supply can be little more complex when the SR is placed on the high side compared to the low side.

Typically, using an additional winding followed by a regulator can power the gate driver in the high-side SR. In low-side SR applications, the voltage for the gate driver can be generated from the main output. In cost-sensitive applications, the SR on the low side is preferred, such as in PAG2S-based flyback converters. This application note describes how to evaluate the common-mode current for low-side and high-side SR. Suitable remedy is also proposed to reduce common-mode currents in the low-side SR.

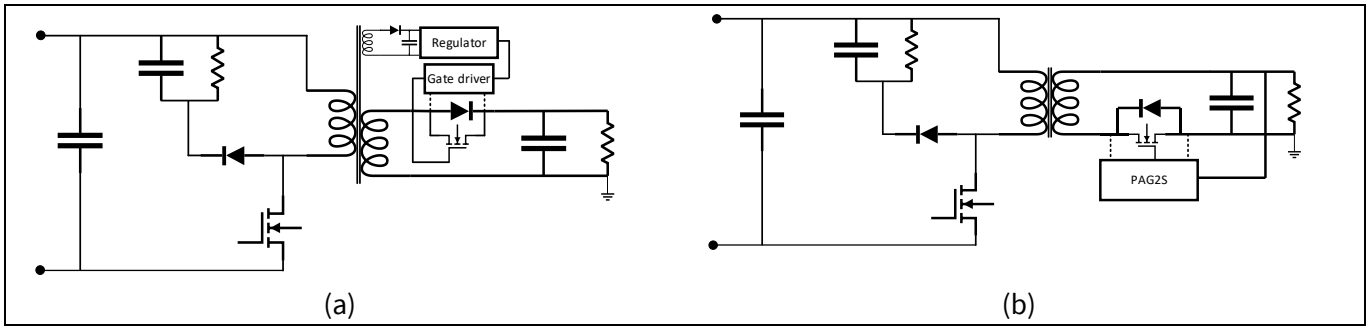


Figure 2 Synchronous rectifier in high side vs. low side

2.3 Common-mode current sources vs. SR position in flyback converters

Figure 3 shows the flyback converter with SR on the high side. To analyse the flyback converter's common-mode current sources and current path when the SR is in the low side and high side, necessary capacitances are introduced in the circuit as a lumped parameter. Being a high-density power supply, many other capacitances could be there in the system.

Table 1 capacitances list

Capacitance	Description
C_{PH}	Capacitance between the DC bus and ground plane in the primary circuit
C_{PG}	Capacitance between the primary section return path and the ground plane
C_{PT}	Capacitance between the drain of the flyback MOSFET and the primary section return
C_{ST}	Capacitance between the secondary return path near the transformer and the ground plane
C_{SH}	Capacitance between the anode of secondary diode and ground plane
C_{SG}	Capacitance between the secondary section return path near load side and ground plane
C_{IP}	Intra-winding capacitance in the primary of the transformer
C_{PS}	Inter-winding capacitance between the primary and secondary winding of the transformer
C_{IS}	Intra-winding capacitance in the primary of the transformer

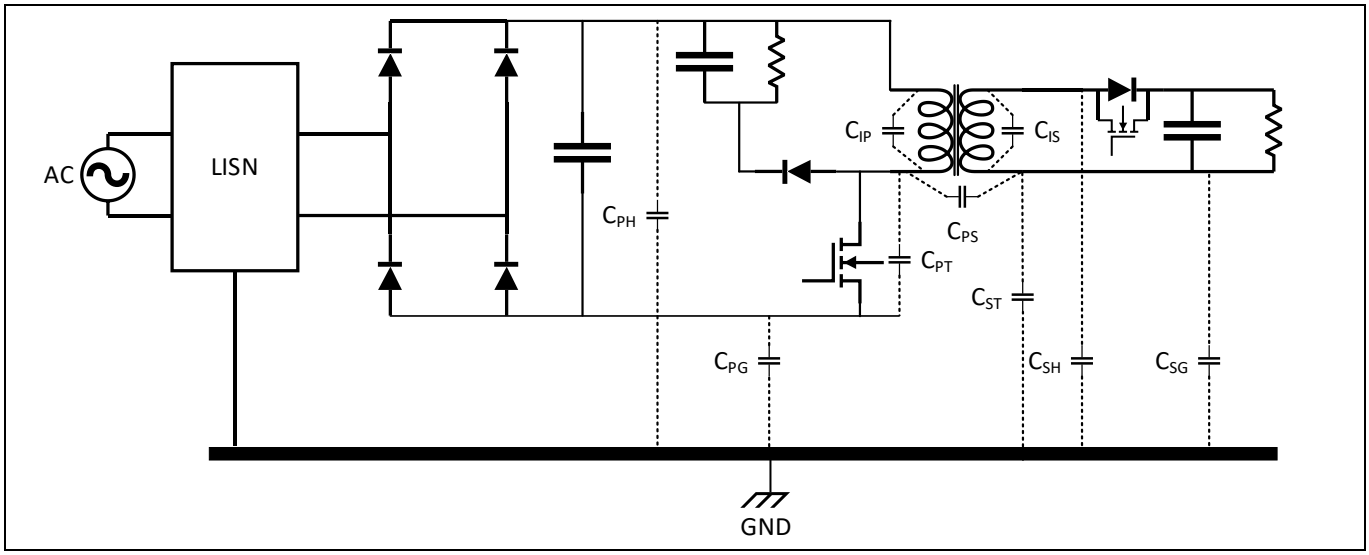


Figure 3 Flyback converter with high side SR with different capacitances

Flyback converters based on PAG2P and PAG2S can operate in QR-ZVS mode or ACF mode. In either mode, the flyback switch achieves ZVS during the turn-on transition. However, turn-off transition is noisy due to high dV/dt. The secondary-side SR FET starts conducting at the same instant, which also results in high dV/dt in the secondary circuit. These two nodes are the key sources of common-mode currents in the system.

Figure 4 shows the direction of the common-mode currents from the high dV/dt sources for high-side SR – flyback switch drain (**RED**) and SR diode anode (**Blue**).

The flyback switch common-mode current direction is through **C_{PS} – C_{SG} (or C_{ST}) – GND – C_{PG} – C_{PT}**. The secondary-side common-mode current direction is through **C_{SH} – GND – C_{PG} - C_{PT} - C_{PS} – C_{IS}**. However, in real time, these capacitances are distributed in nature; considering the high-density power supplies, the common-mode current can choose an alternate path also.

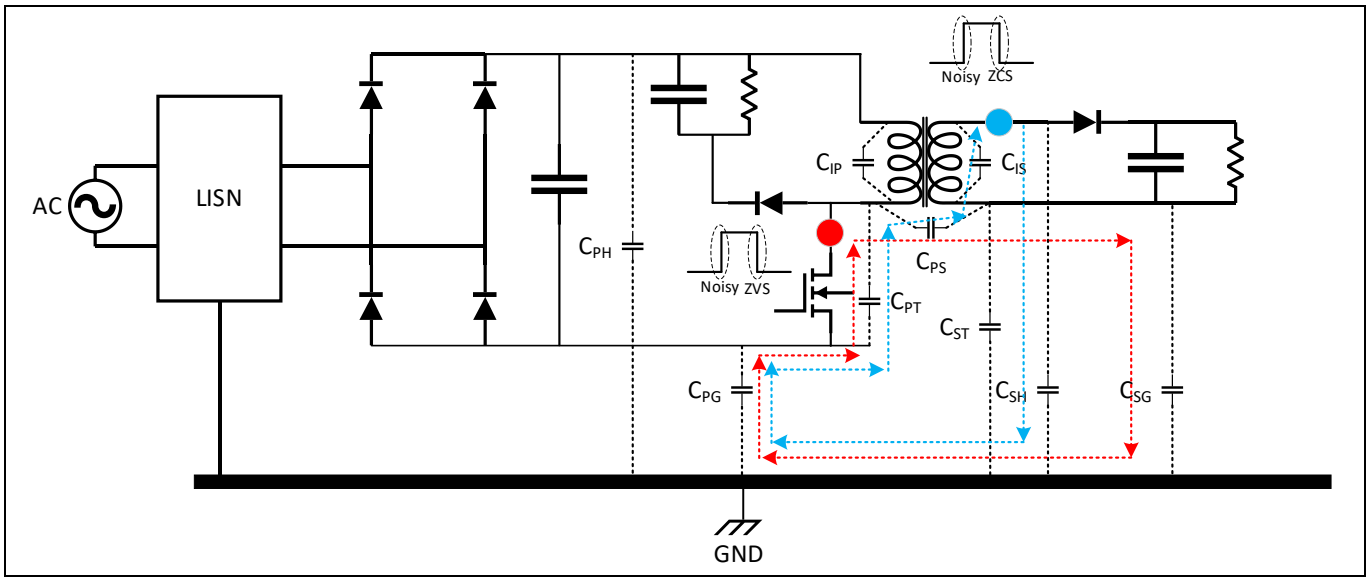


Figure 4 Flyback converter with high-side SR with common-mode current direction

Figure 5 shows the common-mode current in the flyback converter with SR on the low side. The flyback switch common-mode current direction is through **C_{PS} – C_{ST} – GND – C_{PG} - C_{PT}**. The secondary-side common-mode current direction is through **C_{PS} – C_{PT} – C_{PG} - GND - C_{ST}**. Compared to the SR in the high side, the direction of the common-mode current from the SR is the opposite. This is due to the voltage transition across the SR, as shown in Figure 5.

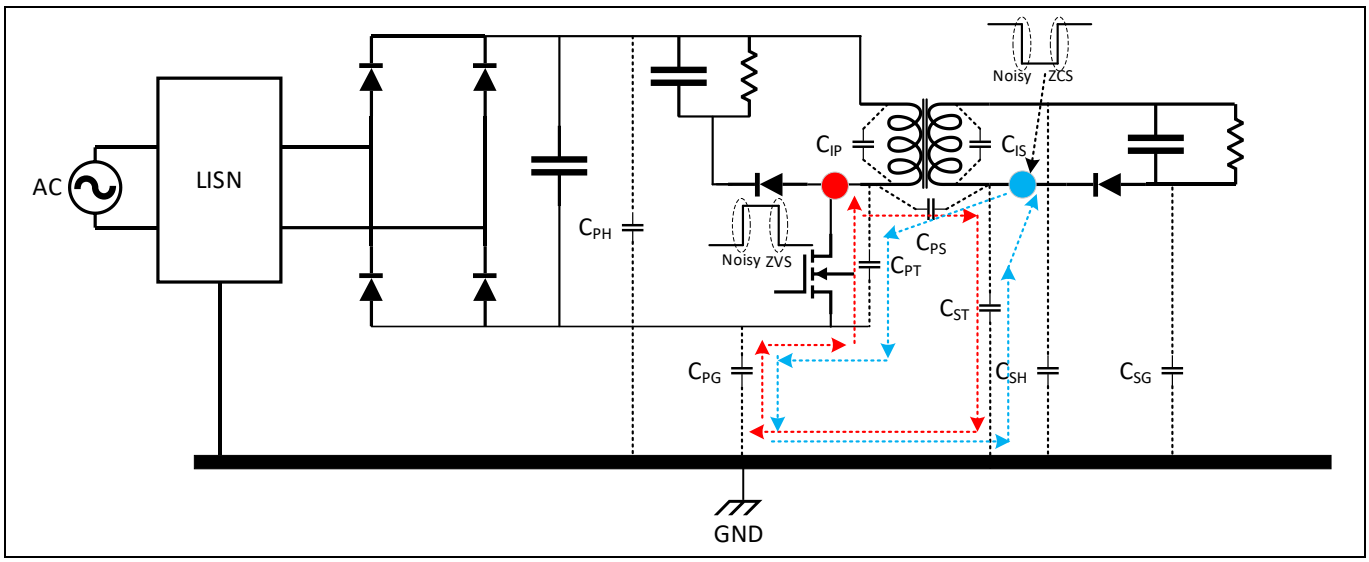


Figure 5 Flyback converter with high-side SR with common-mode current direction

2.4 Inference from the hypothesis of common-mode current paths

- There are two potential sources of common-mode currents: primary-side and secondary-side common-mode currents in both the low-side and high-side SR.
- Common-mode current from the primary side **(RED)** in the high-side SR is intuitively lower due to the lower dV/dt across C_{PS} compared to the low-side SR.
- However, if the direction of the currents **(Blue)** due to SR dV/dt is noticed in the high side vs. low side, **RED** and **Blue** currents oppose each other for the low-side SR and become additive in nature for the high-side SR. Therefore, overall the common-mode currents can be comparable in either SR position.

This hypothesis is validated through a SIMPLIS simulation in the subsequent section.

3 Simulation results

Based on the model proposed, SIMPLIS-based simulation was performed with a secondary diode on the high side and low side. The typical operating condition of a flyback converter with PAG2P and PAG2S was chosen. The common-mode current is measured as shown in Figure 6.

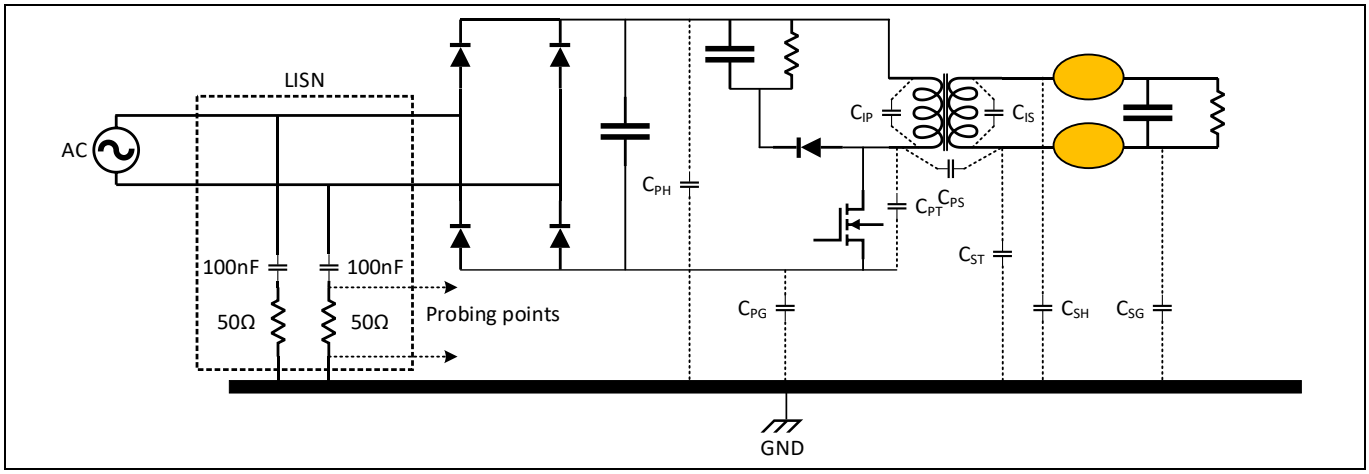


Figure 6 Flyback converter with high-side SR with common-mode current direction

3.1 Simulating conditions

The simulating conditions listed are derived from the typical operating conditions of PAG2S/PAG2P-based flyback converter, with the following list of parameters:

- Input voltage = 380 V
- Duty cycle = 10%
- Switching frequency = 100 kHz
- Output Voltage = 20 V
- Flyback transformer = 110 µH
- Transformer turns ratio (Np/Ns) = 6
- C_{PH} = Ignored in the simulation
- C_{PG} = 1 pF (Assumption)
- C_{PT} = 20 pF
- C_{SH} = Ignored in the simulation
- C_{SG} = 1 pF (Assumption)
- C_{ST} = 1 pF (Assumption)
- C_{IP} = 16 pF
- C_{PS} = 25 pF
- C_{IS} = 700 pF

A few capacitances listed here are assumed to be lumped; however, in reality, these could be distributed.

3.2 Simulation results

Based on the simulation results, when the secondary diode is placed on the high side, the common-mode voltage is 32 mV. When the secondary diode is placed on the low side, the common-mode voltage is 34 mV. Figure 7 shows the CM current waveform.

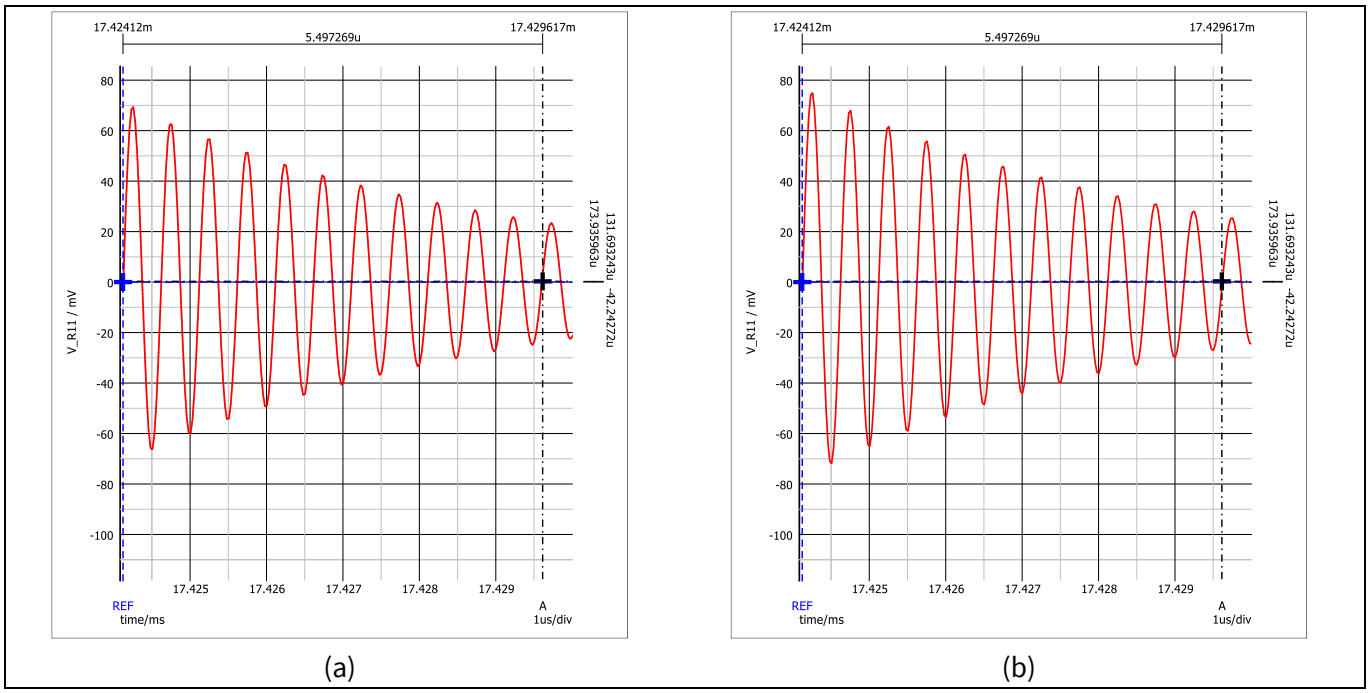


Figure 7 CM current when diode is on the high side (a) and low side (b)

4 Potential solution for reducing common-mode emissions in low-side SR

To reduce the common-mode current shielding between the primary and secondary windings was introduced. This shielding was terminated to DC bus as shown in Figure 8. The model was modified to accommodate the shielding. C_{PS_1} and C_{PS_2} are the capacitances between the primary and secondary windings and are terminated to the shield. C_{PS_3} is the leakage capacitance between the primary windings.

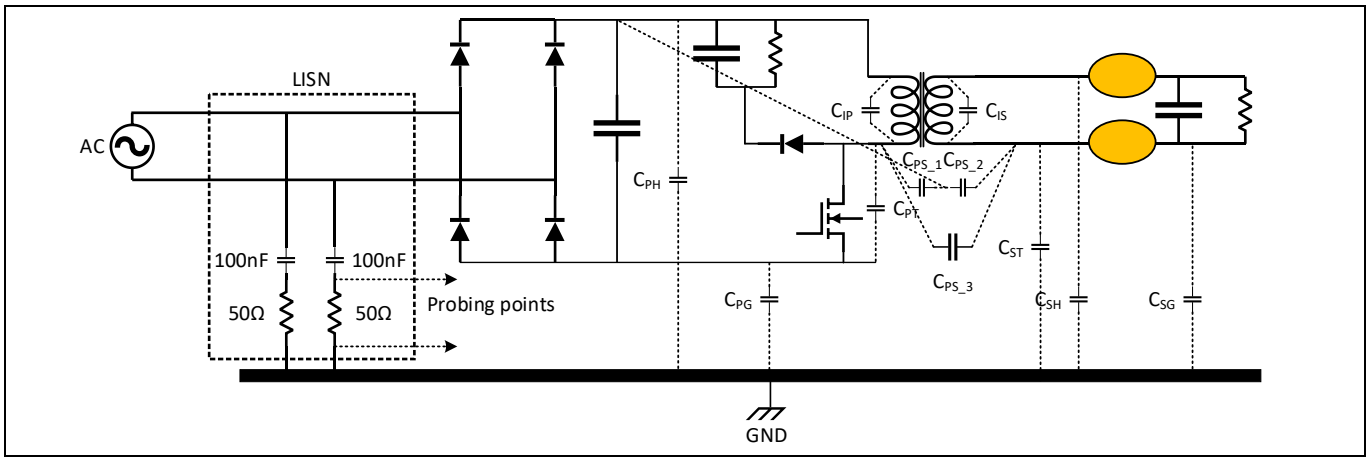


Figure 8 Flyback transformer with shielding

4.1 Simulation results with shielding

Simulation was performed using SIMPLIS with two different cases: tight shielding and loose shielding. In either shielding, common-mode currents are bypassed and therefore, common-mode currents reduce considerably.

Case 1: Loose shielding

The PAG2S device drives the SR at the low side; therefore, subsequent simulation results focus only on the low-side SR. In this case, it was assumed that $C_{PS_1} = C_{PS_2} = 40$ pF, and C_{PS_3} is 5 pF. Shielding considerably reduces the common-mode voltage and it is 6.3 mV; see Figure 9.

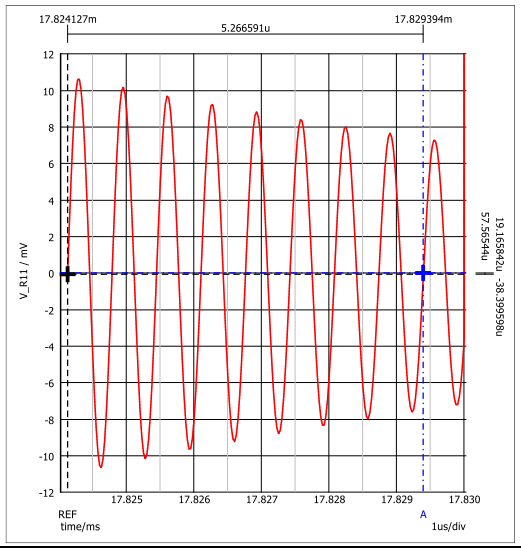


Figure 9 CM current when diode is on the low side with a decent shielding ($C_{PS_1} = C_{PS_2} = 40$ pF and $C_{PS_3} = 5$ pF)

Case 2: Tight shielding

In this case, it was assumed that C_{PS_1} = C_{PS_2} = 48 pF. C_{PS_3} is 1 pF. Notice that compared to Case 1, an effective shielding is beneficial from the common-mode current point of view. The common-mode voltage decreases to 3.4 mV; see the simulation results in Figure 10.

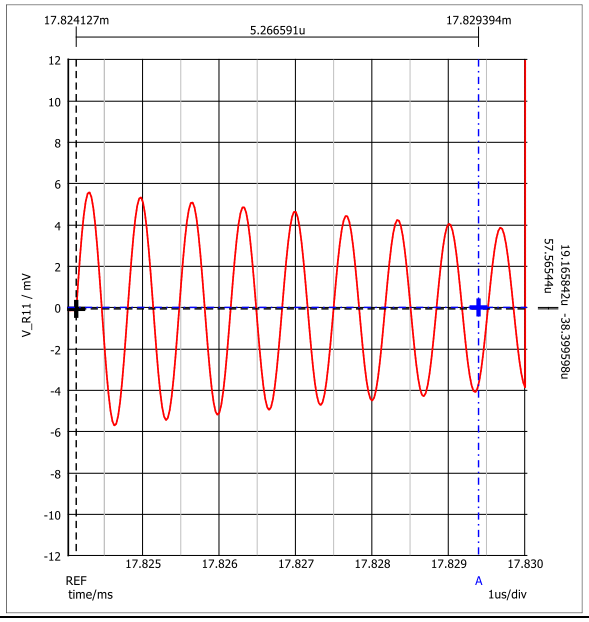


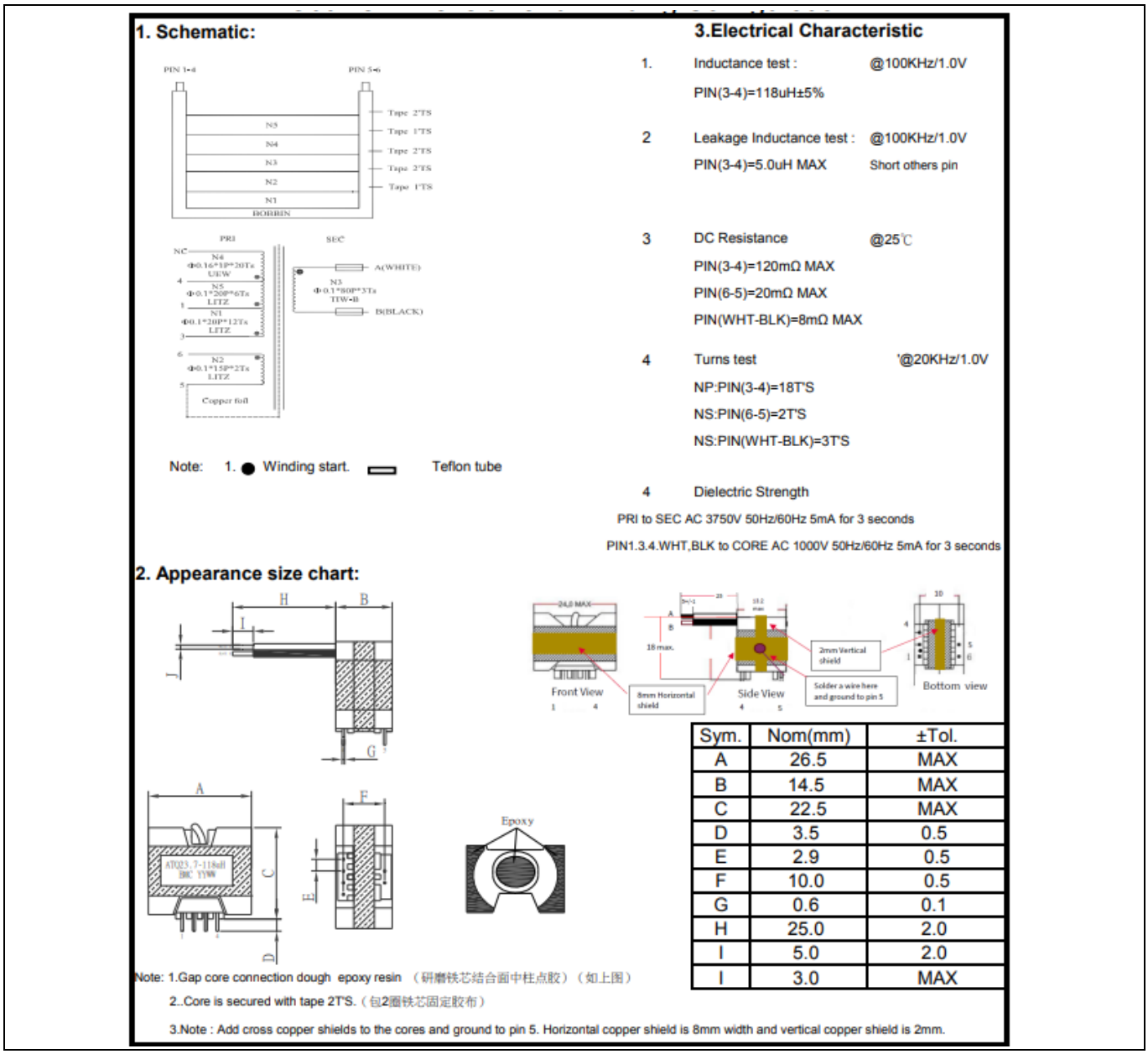
Figure 10 CM current when diode is on the low side and with a tight shielding (C_{PS_1} = C_{PS_2} = 48 pF and C_{PS_3} = 1 pF)

5 Experimental results

Based on the common-mode current reduction technique suggested, the transformer was appropriately built and the shielding was terminated in the DC bus. This section provides the details of transformer construction, schematics, and experimental CE test results.

5.1 Transformer details

Shielding winding is between NC and 4 of transformer. In flyback converter schematics based on PAG2S and PAG2P, terminal 4 is terminated to the DC bus.



1. Schematic:

PIN 1-4 PIN 5-6

N5 Tape 2TS
N4 Tape 1TS
N3 Tape 2TS
N2 Tape 2TS
N1 Tape 1TS
BOBBIN

PRI SEC

NC N4 Φ0.16*1P*20Ts UEW
4 N5 Φ0.1*20P*6Ts LETZ
1 N1 Φ0.1*20P*12Ts LETZ
3
6 N2 Φ0.1*15P*2Ts LITZ
5 Copper foil

N3 Φ0.1*80P*3Ts TIW-B
A(WHITE)
B(BLACK)

Note: 1. ● Winding start. ▭ Teflon tube

3.Electrical Characteristic

1. Inductance test : @100KHz/1.0V
PIN(3-4)=118uH±5%

2 Leakage Inductance test : @100KHz/1.0V
PIN(3-4)=5.0uH MAX Short others pin

3 DC Resistance @25℃
PIN(3-4)=120mΩ MAX
PIN(6-5)=20mΩ MAX
PIN(WHT-BLK)=8mΩ MAX

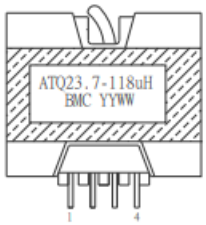
4 Turns test '@20KHz/1.0V
NP:PIN(3-4)=18T'S
NS:PIN(6-5)=2T'S
NS:PIN(WHT-BLK)=3T'S

4 Dielectric Strength
PRI to SEC AC 3750V 50Hz/60Hz 5mA for 3 seconds
PIN1.3.4.WHT,BLK to CORE AC 1000V 50Hz/60Hz 5mA for 3 seconds

2. Appearance size chart:

Sym.	Nom(mm)	±Tol.
A	26.5	MAX
B	14.5	MAX
C	22.5	MAX
D	3.5	0.5
E	2.9	0.5
F	10.0	0.5
G	0.6	0.1
H	25.0	2.0
I	5.0	2.0
I	3.0	MAX

Note: 1.Gap core connection dough epoxy resin （研磨铁芯结合面中柱点胶）（如上图）
2..Core is secured with tape 2T'S.（包2圈铁芯固定胶布）
3.Note : Add cross copper shields to the cores and ground to pin 5. Horizontal copper shield is 8mm width and vertical copper shield is 2mm.



All materials listed are in compliance with RoHS requirements

No.	Name	Description	Rating	Approval	Maker
1	Core	Ferrite core ATQ23.7/12.8/17.8 NH97 or equivalent			LIANFENG
2	Bobbin	Phenolic PM-9630 UL 94V-0	150℃	E41429	SUMITOMO
3	Wire	Polyurethane enamelled copper Wire UEW MW75-C Ø0.1*20P,Ø0.1*15P Ø0.16	130℃ 130℃	E339217 E201757	WEIHAN PACIFIC
		Triple insulated wire TIW-B Ø0.1X80P or equivalent	130℃	E357240	KAIZHONGHEDONG
4	Tape	Polyester tape #1350F-1 or #CT280	130℃ 130℃	E17385 E165111	3M YA HUA
5	Tube	CB-HFT ND-LL	125℃ 200℃	E180908 E350651	CHANGYUAN NANDIAN
6	Copper foil	0.05(T)*8mm 0.05(T)*3mm			HAIYU DETAI
7	Epoxy	2050 2041			CHENGGE CHENGGE
8	Varnish	BC-359 WP-2952F-2G(Y)	180℃ 130℃	E317427 E72979	DOLPH HITACHI

Figure 11 Transformer details

5.2 Schematics of HF ACF

As the schematics shows, a simple, single-stage filter is sufficient for a 65 W power supply to pass CE requirements.

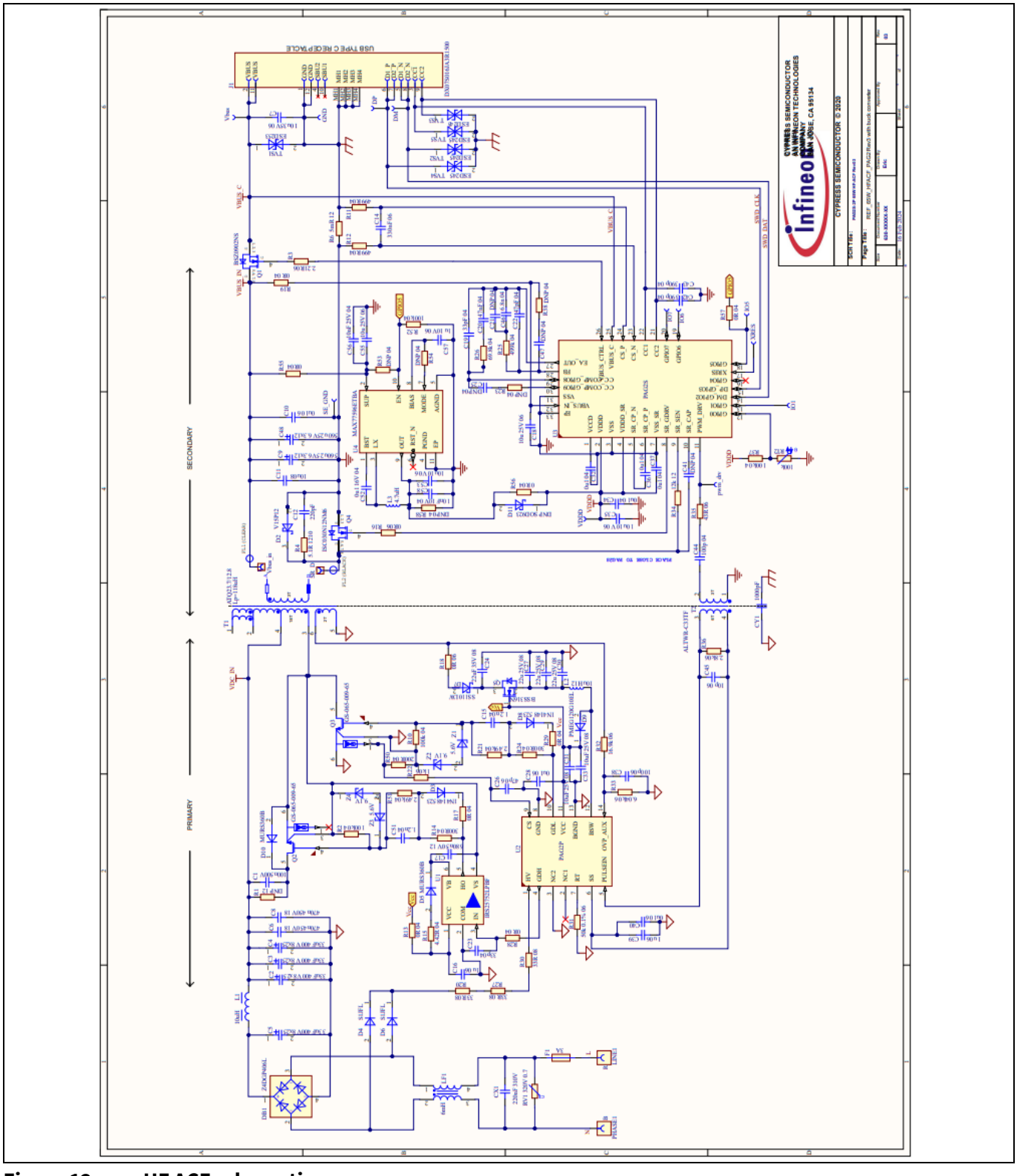


Figure 12 HF ACF schematics

5.3 Conducted emission signature

A 65 W flyback HF ACF unit based on PAG2P and PAG2S was tested for CE at 115 V and 230 V. The transformer was shielded and terminated as discussed. Figure 13, Figure 14, Figure 15, and Figure 16 provide the CE signature at different conditions.



Figure 13 CE testing (Line – QP and Avg) at 230 VAC input



Figure 14 CE testing (Neutral – QP and Avg) at 230 VAC input

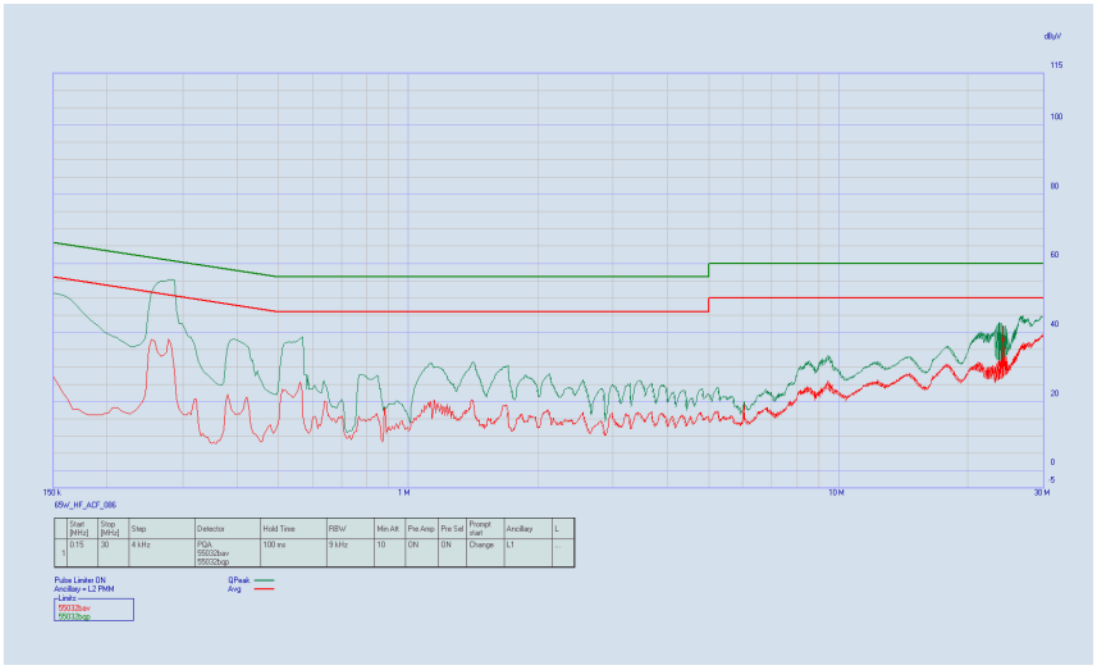


Figure 15 CE testing (Line – QP and Avg) at 115 VAC input

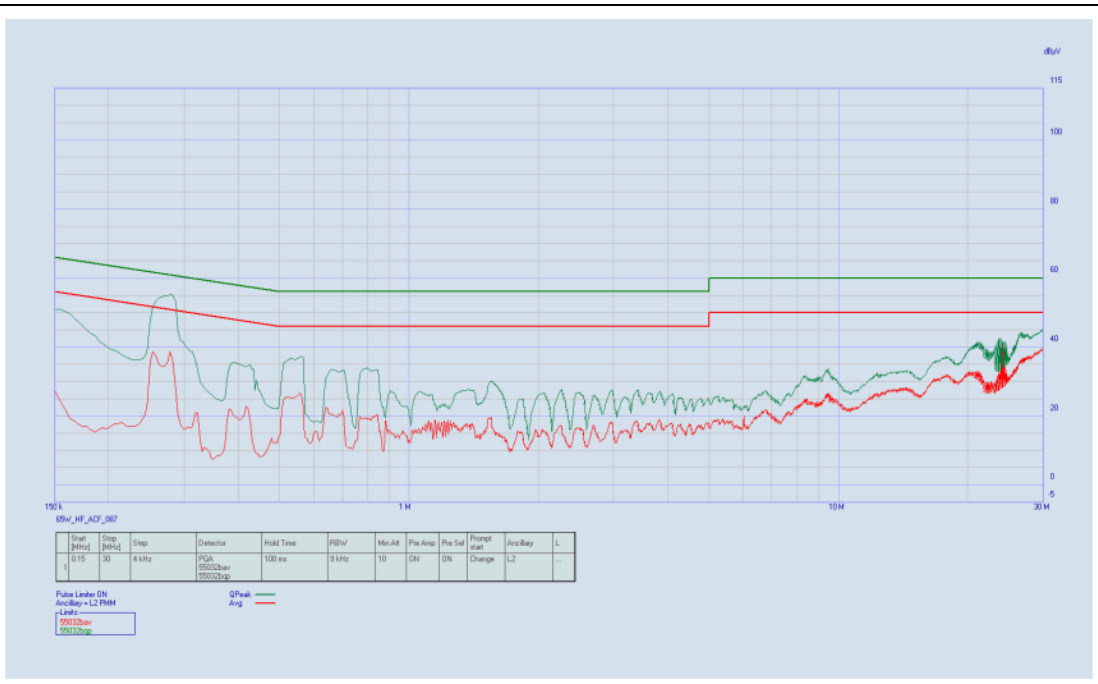


Figure 16 CE testing (Neutral – QP and Avg) at 115 VAC input

6 Guideline for reducing CE in low-side SR

Based on the analysis and experiments, it is understood that appropriate construction of transformer can significantly reduce the CE emissions. While constructing the transformer, two types of shielding is proposed: Internal shielding and external shielding.

6.1 Internal shielding

Figure 17 provides the typical structure of the transformer. To reduce CE emissions, interleaved winding is proposed with a shield. A PAG2S/PAG2P-based system will have an auxiliary winding to bias PAG2P. Electrically, the auxiliary winding is part of primary ground; therefore, it can be wound closer to the primary winding with the required insulation. The primary winding is split into two halves, while the secondary winding is sandwiched between the primary windings with the shield on either side. The shield windings are shorted together and terminated to the DC bus as explained in Section 4.

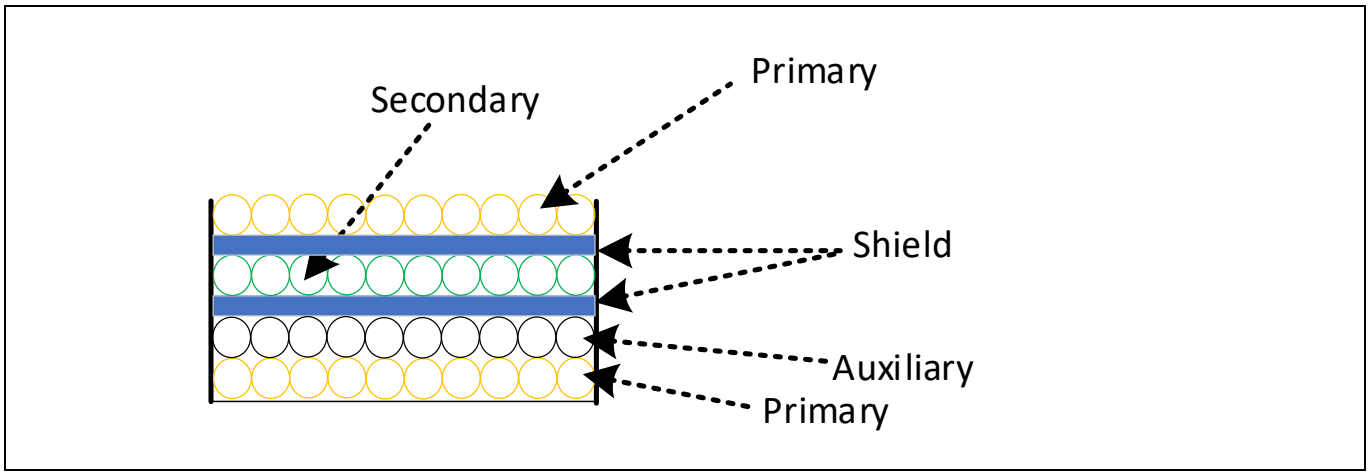


Figure 17 Transformer stackup

You should ensure that the shield winding covers the entire primary and secondary winding area. This would result in a tightly coupled shield winding and mitigate the CE more effectively. Based on the proposal, an actual transformer was built as listed in Section 5.1.

6.2 External component shielding

In high power density designs, all components are bound to come in the proximity. This would result in cross-coupling between the emitting components and EMI filters. Figure 18 shows a 65 W ACF design in which the transformer and EMI filters are shielded externally. This is a typical example of high power density design in which the EMI filter is in proximity of the flyback transformer. This would make the EMI filter less effective.

To eliminate or reduce the cross-coupling effect, put an external shield layer over the transformer; i.e., wrap the transformer with conductive material like copper. This would contain all the emission from the transformer and prevent cross-coupling from nearby components.

Based on the specific design, such cross-coupling scenarios must be identified and appropriate shielding must be done. In some cases, shielding the entire EMI filter also might help.

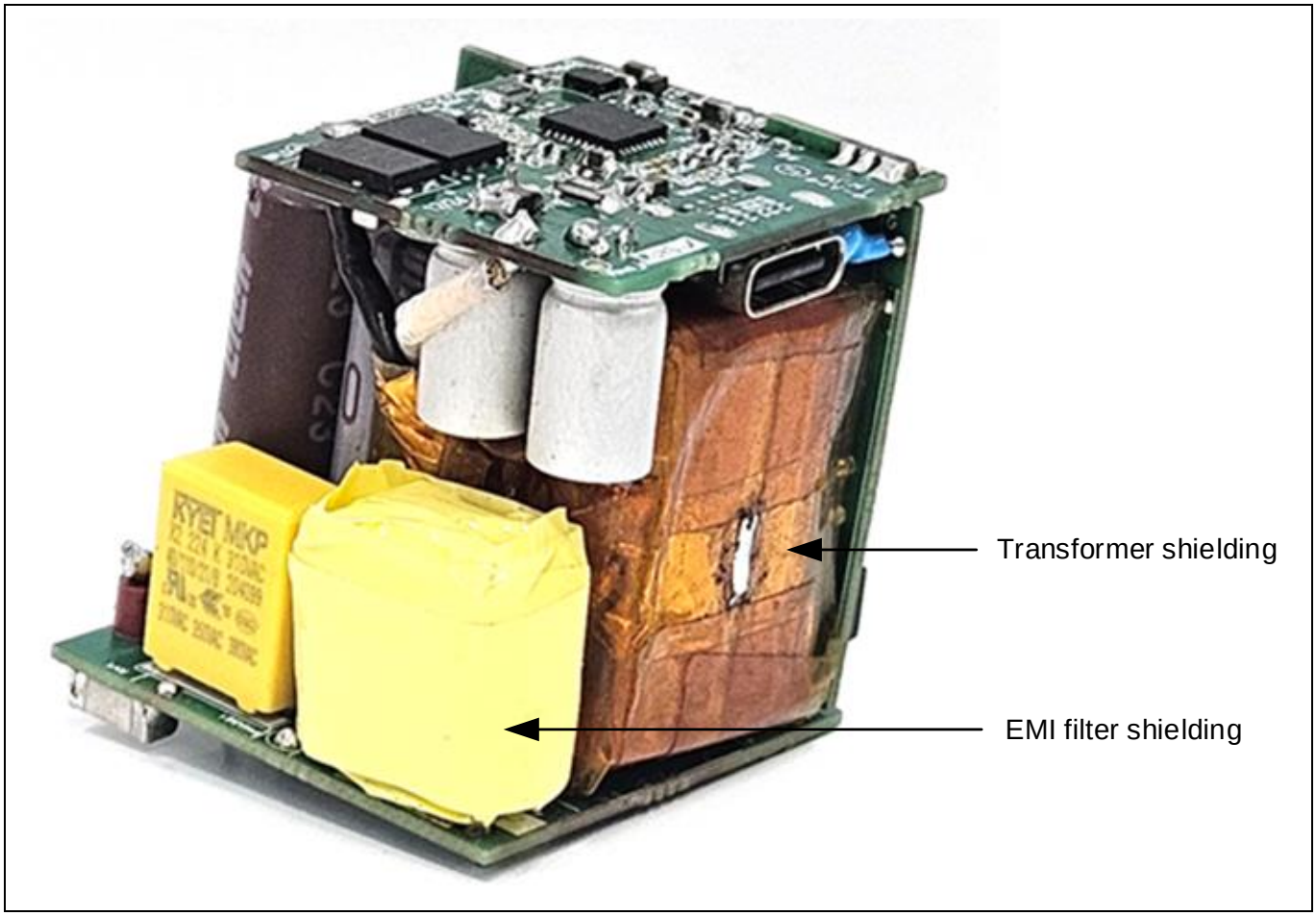


Figure 18 PAG2P/PAG2S-based 65 W ACF design

7 Summary

The comparative study shows that the difference in common-mode currents with the high-side and low-side SR is marginally different. In either approach, the common-mode current mitigation or improvements in conducted emissions can be achieved by simple techniques like shield winding and proper termination. Shield windings are part of the transformer construction and thus does not increase the system size and cost. With this guideline, the external EMI filter need not be increased in size to reduce common-mode currents due low-side SR.

Therefore, the common-mode current due to the low-side SR and its effect on conducted emission can be mitigated without increasing the EMI filter size. This ensures that there is no impact on the size and efficiency with low-side SR designs with PAG2S and PAG2P. In addition, general guidelines for improved EMI performance for high power density design has been provided in terms of shielding the components and EMI filter.

References

[1] Infineon Technologies AG: *EZ-PD™ PAG2P Primary Side Controller*, Available online

[2] Infineon Technologies AG: *EZ-PD™ PAG2S Secondary Side Controller*, Available online

Revision history

Document revision	Date	Description of changes
**	2024-07-09	Initial release
*A	2024-07-26	Fixed typo and updated scope and purpose of the document

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