3 kW dual-phase LLC evaluation board

Using 600 V CoolMOS™ C7 and digital control by XMC4400

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About this document

Feedback

Scope and purpose

This document describes the design and performance of a 3 kW dual-phase LLC evaluation board intended for use in the isolated HV DC-DC stage of a Switch Mode Power Supply (SMPS) for telecom and industrial applications.

This is a high performance example with a complete Infineon solution, including HV and LV power MOSFETs, controllers, and drivers, demonstrating a very effective way to design the HV DC-DC stage of a telecom rectifier or Industrial SMPS fulfilling the highest standard of efficiency and reliability. The additional benefit of a very flat efficiency plot is also achieved through a mix of proper control techniques and best-in class power device selection.

Key Infineon products used to achieve this performance level include:

- 600 V CoolMOS™ C7 superjunction MOSFET
- Isolated gate driver 1EDI60N12AF
- SyncRec MOSFETs OptiMOS™ BSC093N15NS5
- Advanced dual channel gate driver 2EDN7524
- XMC4400 microcontroller
- Bias QR flyback controller ICE2QR2280Z

As well as design information and documentation of the LLC converter, the reader will receive additional information on how the 600 V CoolMOS™ C7 behaves in LLC applications and the associated benefits, how the high performance magnetics design can be approached, and insights on how to develop dual-phase LLC converters in similar power ranges adapted to specific requirements.

Intended audience

This document is intended for design engineers who wish to evaluate high performance topologies for high power SMPS converters, and develop an understanding of the design process and how to apply the multi-phase LLC design methods to their own system applications.

Note: *General knowledge about the resonant HB LLC converter principle of operation is required for proper comprehension of the concepts reported in this paper.*

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1 Introduction

The combined trends of continuous reduction of volume and size of the power converters and increase of required output power represent a serious challenge in modern Switch Mode Power Supply (SMPS) designs.

When addressing the high power density requirement, even in a SMPS with high peak efficiency, a typical problem consists in getting rid of the heat generated, especially at the full load, in the limited volume available.

A very powerful fan can help, but there may be a lot of side effects, like the acoustic noise or the generated vibration, which may be not tolerated by other system components, like e.g. hard disk drives in computing applications. And in any case the effectiveness of the forced ventilation is linked to the air impedance inside the SMPS. Unfortunately, a typical consequence of the power density increase is the increase of the air impedance inside the Power Supply Unit (PSU).

Especially in industrial and telecom applications, there are cases where the fan is even not allowed.

The best solution is to try to limit the heat generated especially in the most critical condition from thermal perspective, the full load operation. This means that having a very high peak efficiency (typically achieved at 50% load) may not be enough on the purpose, but the same high efficiency has to be extended up to full load operation.

In order words, this requirement involves the need of a very flat efficiency plot, at least from 40-50% up to 100% load.

On the other hand, in N+1 redundant application the percentage of SMPS operation near full load is relatively lower compared to the one below half load, making for this reason also important the efficiency down to around 30% load.

The combination of these typical performance requirements of industrial and telecom high power SMPS can be fulfilled through a very flat efficiency plot from 30% to 100% load.

Similar curve is not compatible with the natural behavior of a power converter, whose efficiency plot has typically the shape of a parabola with the peak at around mid load. In other words, the desired “flatness” can be achieved only through a dedicated power converter design, which involves a proper selection of the topologies, power devices, magnetic components and control techniques.

One of the most popular solutions adopted in power conversion in order to achieve this goal is the Multiphase approach. Scaling and balancing are two typical aspects of this design technique [15].

In this document the fundamental aspects of a multiphase LLC converter are analyzed, giving an overview about the most important design choices, especially in power semiconductors and control techniques.

A practical example is provided thorugh the description of a 3 kW dual-phase LLC demo board totally designed with Infineon power semiconductors and IC components.

In this document it is demonstrated that the usage of state-of-art high and medium voltage silicon MOSFETs, in combination with optimized driving and sophisticated digital control allows fulfilling all the most important requirements of a modern high power SMPS, both in term of perfomance and reliability.

2 Dual-phase HB LLC design concept

Our goal is to give you a general overview about the Infineon 3 kW dual-phase LLC demo board and the concept behind it. Three important aspects of the present design are explained in this chapter. The specific control techniques used to address these three key aspects will be explained in more detail in the chapter 4.

2.1 Current sharing and phase shedding

2.1.1 The design challenges

The principle of operation of a single half bridge LLC converter is described in details in [1].

Unlike a conventional 'PWM' topology, based on a fixed frequency and variable duty cycle control, a resonant converter uses the switching frequency as main control parameter. The typical high gain of the resonant tank makes the resonant current very sensitive to the operating frequency.

When two resonant converters operate in parallel at the same frequency, any mismatch between the components of the two resonant tanks may generate a current imbalance in the two converters, which in the worst case can force all the current in one of the two phases, thus generating overstress and most likely shutdown due to overcurrent protection mechanism.

A simulation performed with Simetrix on a dual-phase LLC circuit (Figure 1) clearly demonstrates the design challenges related to the current sharing implementation.

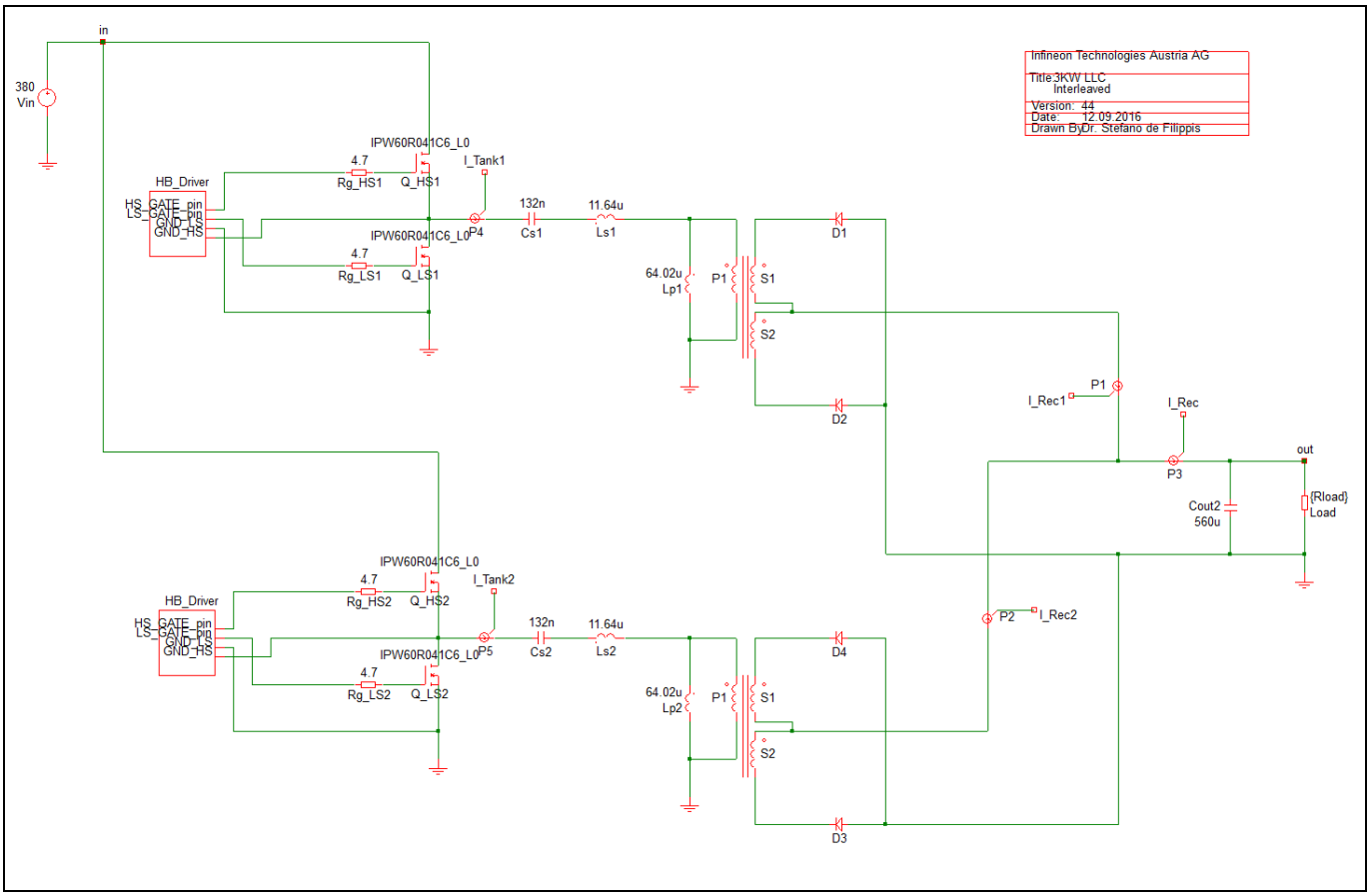


Figure 1 Simetrix simulation model of the 3 kW dual-phase LLC

Dual-phase HB LLC design concept

Figure 2 and Figure 3 below show the perfect balance of the current in the two LLC converters, respectively called Conv1 and Conv2, both on the primary and secondary side, in case of identical resonant tank components. The switching frequency used for the simulations is the resonant frequency, which the same for both converters. For the reader's convenience, all the waveforms (both primary and secondary) related to Conv1 are plotted in red; the ones related to Conv2 are plotted in green.

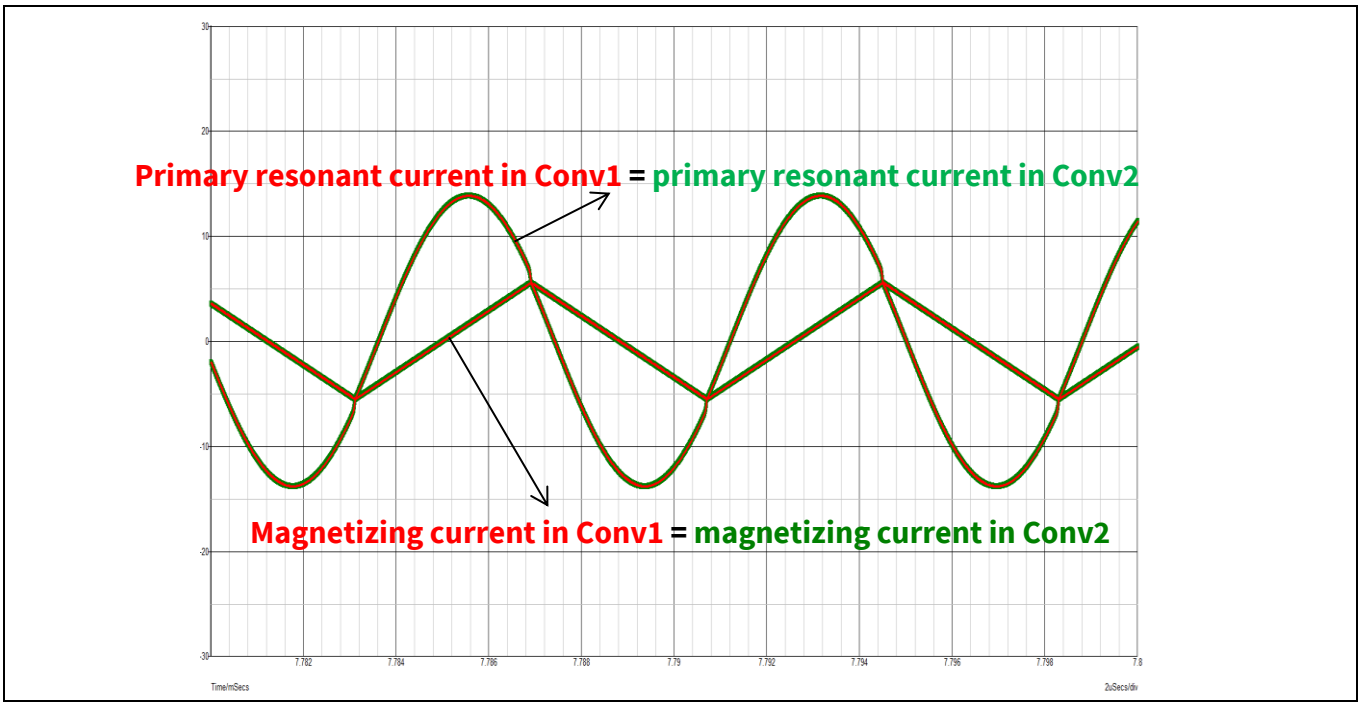


Figure 2 Resonant and magnetizing currents in case of identical resonant tank components

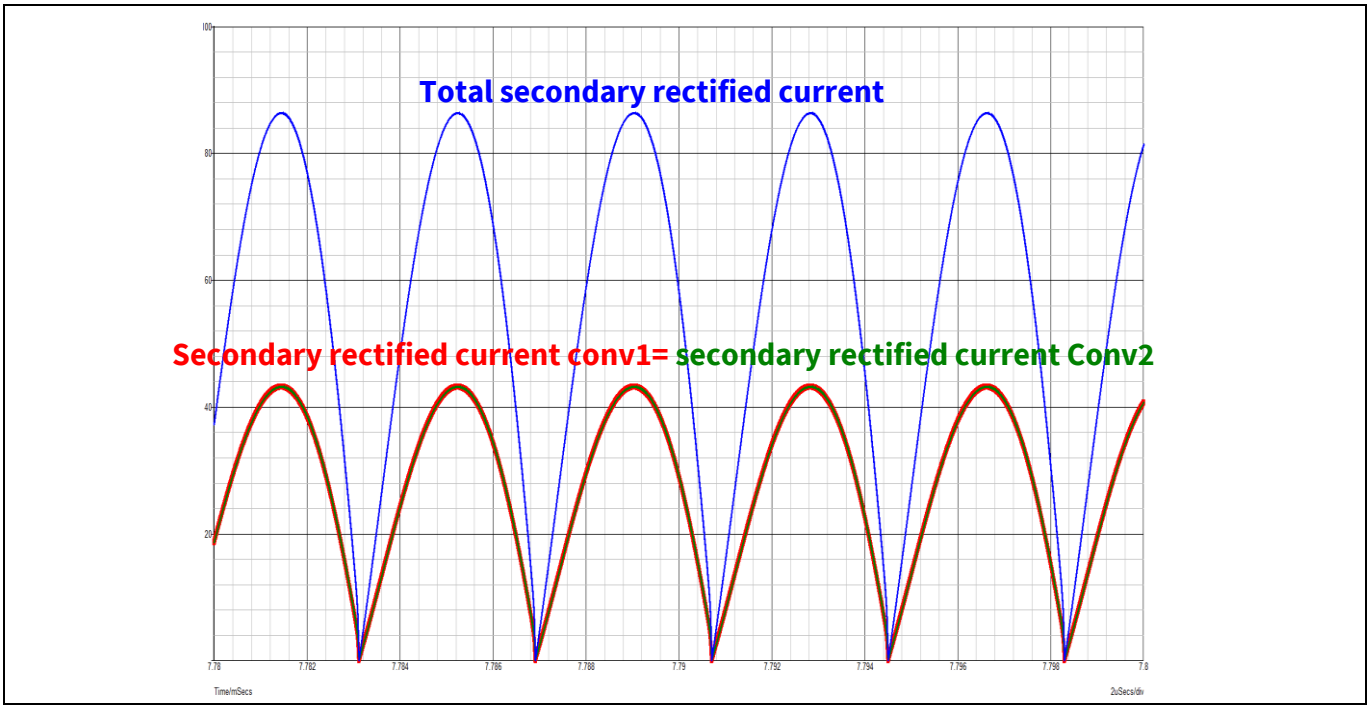


Figure 3 Secondary rectified currents in case of identical resonant tank components

From Figure 2 one can appreciate that the primary resonant currents and, of course, the magnetizing currents are completely overlapped, as obvious consequence of the perfect balance of the two phases, ideally supposed

to operate at the same resonant frequency. In Figure 3 we see that also the secondary rectified currents are overlapped and each of them contributes by 50% to the full secondary rectified current, represented by the blue plot.

The Figures 4, 5 and 6 refer to the case where there is a difference of only 5% between the values of the inductances in the two resonant tanks, specifically the resonant inductance in the Conv2 (Lr2) is 5% smaller than the one in the other tank (Lr1). This is a very common situation which might be faced in the reality, due to the typical tolerances in the range of ±10% of the nominal values shown by this kind of magnetic components.

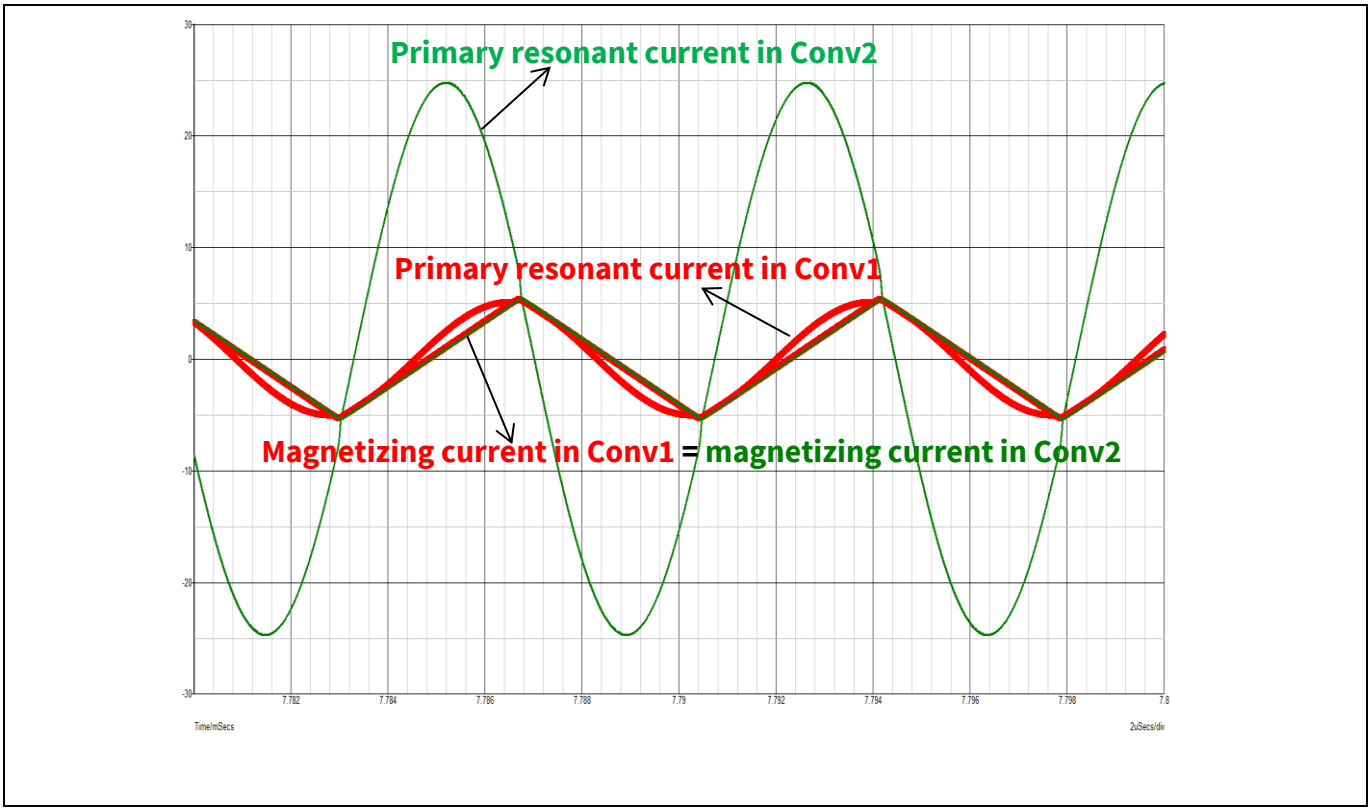
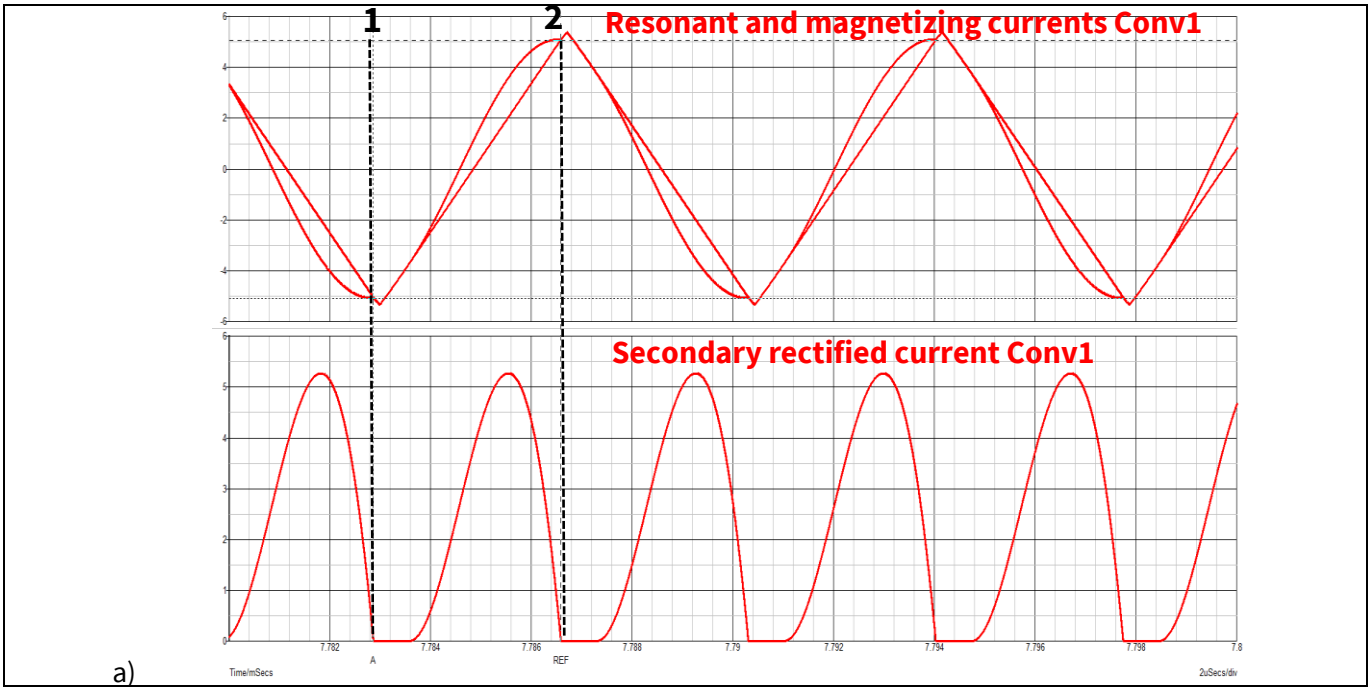


Figure 4 Resonant and magnetizing currents in case Lr2 is 5% smaller than Lr1

This small difference already generates a pretty high imbalance in the primary resonant current of the two phases, as appreciated in the Figure 4, while of course the two magnetizing currents are still perfectly concident, since there is not change in the main transformers.

Basically, the reduction of Lr2 generates a reduction in the equivalent impedance of the Conv2 resonant tank. Since the switching frequency has been kept the same as in the balanced case, Conv2 shows a larger gain than Conv1 at this switching frequency.

The Figure 5 explains the reason of the Conv1 secondary rectified current shape in the case of Lr imbalance: the current is diverted almost totally into the Conv2 resonant tank, so the resonant current in Conv1 becomes very low, almost overlapping the magnetizing current. In particular, during the time intervals when they are equal (e.g. starting from the points highlighted as 1 and 2 in the Figure 5), the secondary rectified current becomes zero. This operation resembles the no load operating condition and generates in Conv1 a secondary current similar to what it is expected in Discontinous Current Mode (DCM) operation, typically seen when the LLC converters operate below resonance. Actually, the Conv1 still operates at the resonant frequency, since Lr1 and Cr1 haven't been changed, but almost at no load, which is the reason why the secondary rectified current shows a discontinous behavior.



a)

Figure 5 Resonant, magnetizing and seconday rectified currents in case Lr2 is 5% smaller than Lr1

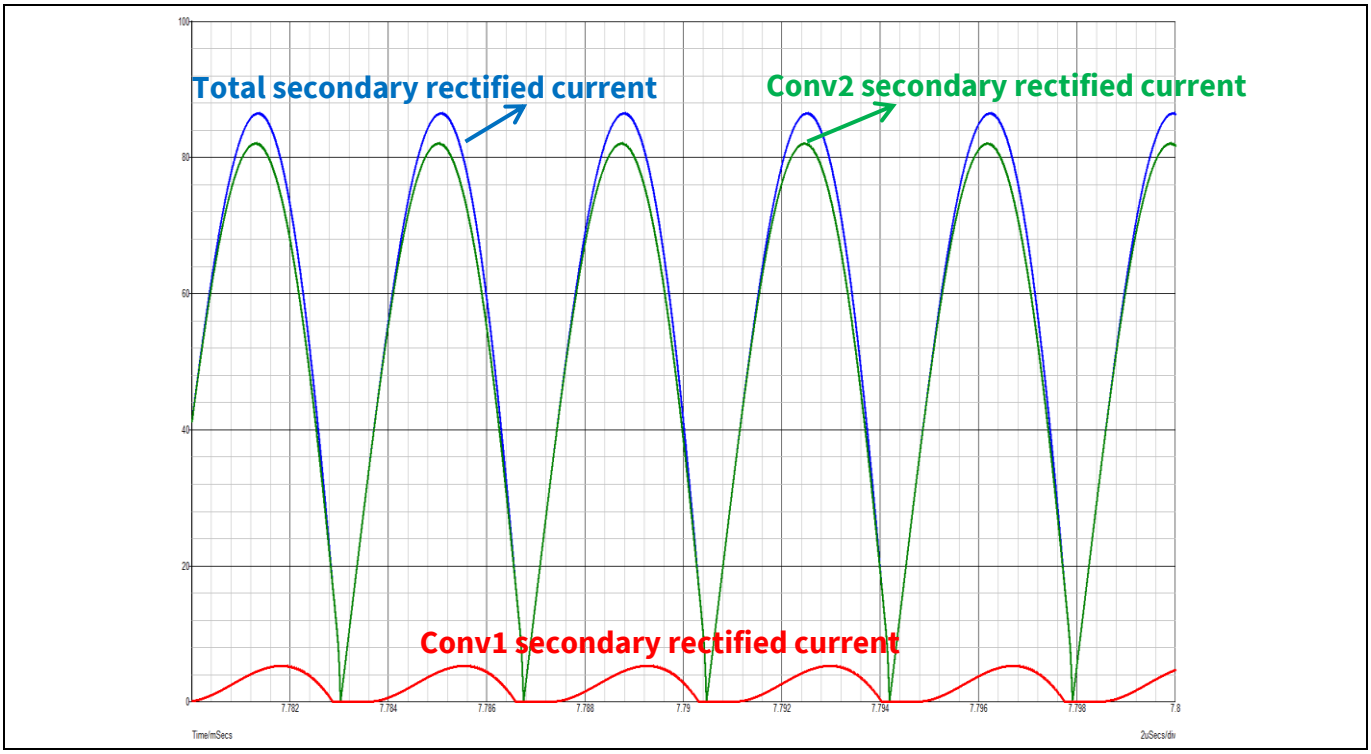


Figure 6 Secondary rectified currents in case Lr2 is 5% smaller than Lr1

Looking at Figure 6, the reader can easily understand what happens in practice. The total secondary rectified current is almost corresponding to the one in Conv2, which, in other words, will get almost the entire load current. Of course, the Conv2 is typically not designed to sustain the full load of the whole dual-phase converter, since it is supposed to work only up to half load. Therefore, it will go immediately into output overcurrent/overpower, thus generating the shutdown of the complete converter.

Further simulations show that a similar behavior can be noticed in case of mismatch of only 5% in the values of the resonant capacitors in the two HB LLCs.

These simple examples clearly demonstrate that the current sharing of two paralleled resonant converters is not a trivial topic and really represents a design challenge.

In the technical literature several techniques are proposed in order to get rid of this possible issue.

The simplest one is to perform a pre-selection of the resonant tank components (inductor and capacitor) in order to use identical values in the two phases. But this selection normally results expensive and time consuming in the SMPS mass production, especially for big volumes. For that reason this solution is typically not preferred by big SMPS manufacturers.

A possible alternative solution is proposed in [2], where an additional intermediate conversion stage is added to regulate the LLC converter input voltage in order to allow each of the two converters to always operate at the optimal frequency for current balancing. The key of this technique is to get the output regulated through the variation of the input voltage and not of the resonant stage gain. This solution will avoid the current imbalance, but, on the other hand, will unavoidably impact the overall converter efficiency, due to the introduction of an additional conversion stage.

Another valuable solution is proposed in [3] and [4]: it consists of compensating the resonant components mismatch by means of an additional inductor with adjustable inductance value. In that approach the use of a magnetic core with saturation windings can provide an effective way of varying the value of the inductor wound on the same core. In order to be really effective, this technique requires a very precise output current measurement combined with a very accurate control of the resonant inductor value as function of the current imbalance in the two or more converter phases.

2.1.2 The proposed implementation

As usual, each of the methods described in the previous paragraph has some pros and cons.

In our 3 kW dual-phase design we opted for a more traditional direct control of the converter's switching frequency in function of the current in each of the two phases.

This technique has also several different implementations and, of course, several tricky aspects.

One of them is faced when trying to keep the two switching frequencies as much close as possible. In case they are very close but not perfectly the same, this may result in beat frequency effects that can be very critical for EMI and acoustic noise, moreover heavily affecting the output ripple and thus requiring filtering. Some other techniques have the disadvantage of reducing the reliability and reproducibility of the resulting LLC converter arrangement.

In case the N paralleled converters run at synchronized frequencies, having independent input voltages helps. That means the need of a separated PFC for each of the paralleled LLCs, which might increase the complexity of the PFC control. This solution does not give effective ratio efficiency vs. cost and power density. Cost and power density are strongly in the focus of modern High Power SMPS design.

In some cases, one converter is voltage controlled and the other (N-1) are current controlled, where the values used by the current controller is the output current of the voltage controlled converter: a main drawback is that this may easily generate problems of instability of the N LLC loops.

Our 3 kW dual-phase LLC design concept is able to overcome load imbalance between the two HB LLC converters while maintaining a good reliability, practicability/reproducibility and efficiency.

The converter consists of two half bridge LLCs, each with its transformer, resonant choke and SR stage. A microcontroller located in the secondary side takes care about the control of both converters.

Dual-phase HB LLC design concept

Figure 7 shows a general principle of operation of the current sharing, by acting on the switching frequency of one of the two converters. The so called “phase shedding” function is also included: it consists in switching-off one of the two converters below certain load.

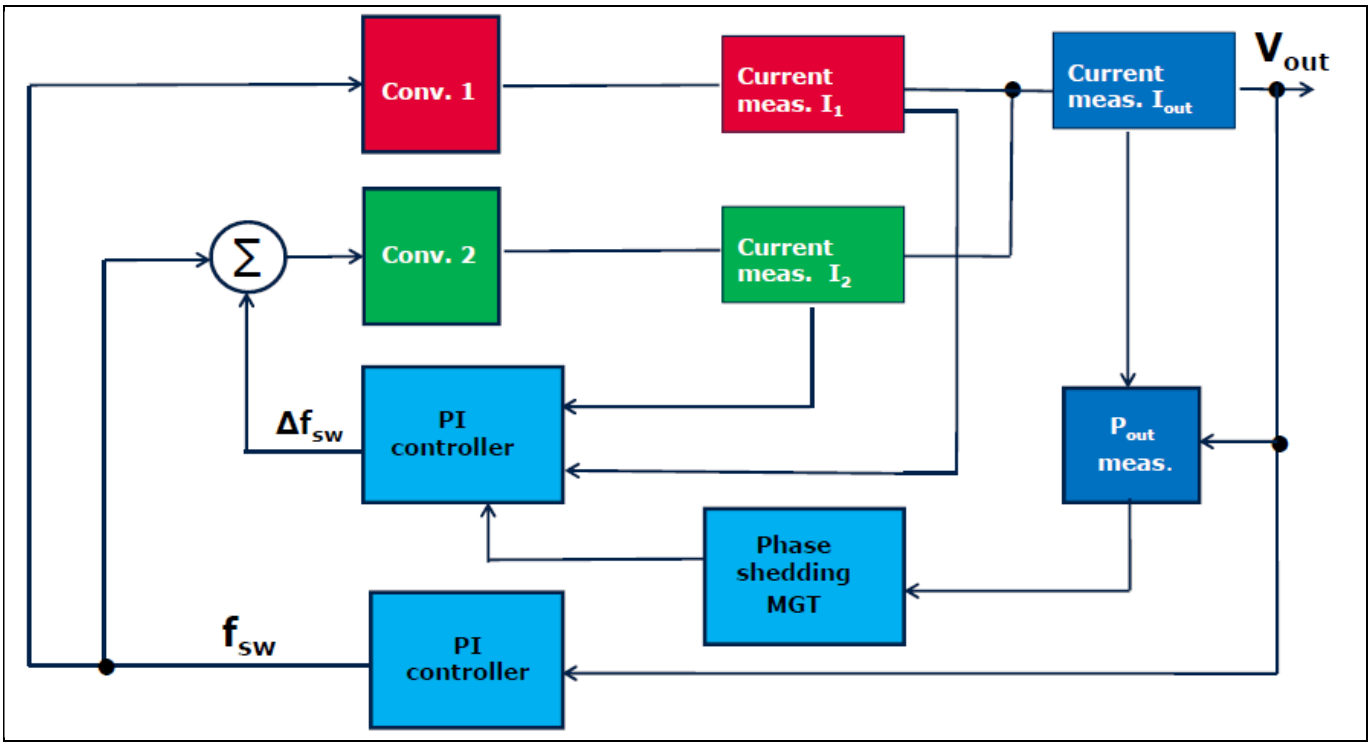


Figure 7 General current sharing principle of operation

In our approach, the two phases are treated separately, so the controller peripherals must accommodate the two phase’s requirements in terms of PWMs and ADCs. The two converters may have parts tolerance/mismatch, leading to different resonant frequencies; therefore, a separate PWM module is needed for each of both stages in order to modulate them separately to achieve current sharing.

The switching frequencies of the two LLCs are not the same and the secondary current ripple cancelation is not guaranteed. The output ripple will increase until reaching a maximum value when the two stages are in phase, then decreased until reaching a minimum value when the two stages are 90° out of phase. The ripple cancelation is in fact not in the main focus of our design, due to the relatively low output current (max 55 A). Of course, the output current ripple reduction becomes more critical in case of power converters with low output voltage and high output current: in those cases the interleaving by phase shift of the respective PWM paths is recommended.

The key concept of our control method is to split the output of the voltage controller into two or more control signals for the converters by special balancing function. The balancing function is responsible for keeping the highest efficiency in steady state operation and prevents overloading of one of the two phases during quick power changes for dynamic regulation.

In Figure 8 you can find a schematic description of our implemented current sharing method, which will be described more into details in Chapter 4.

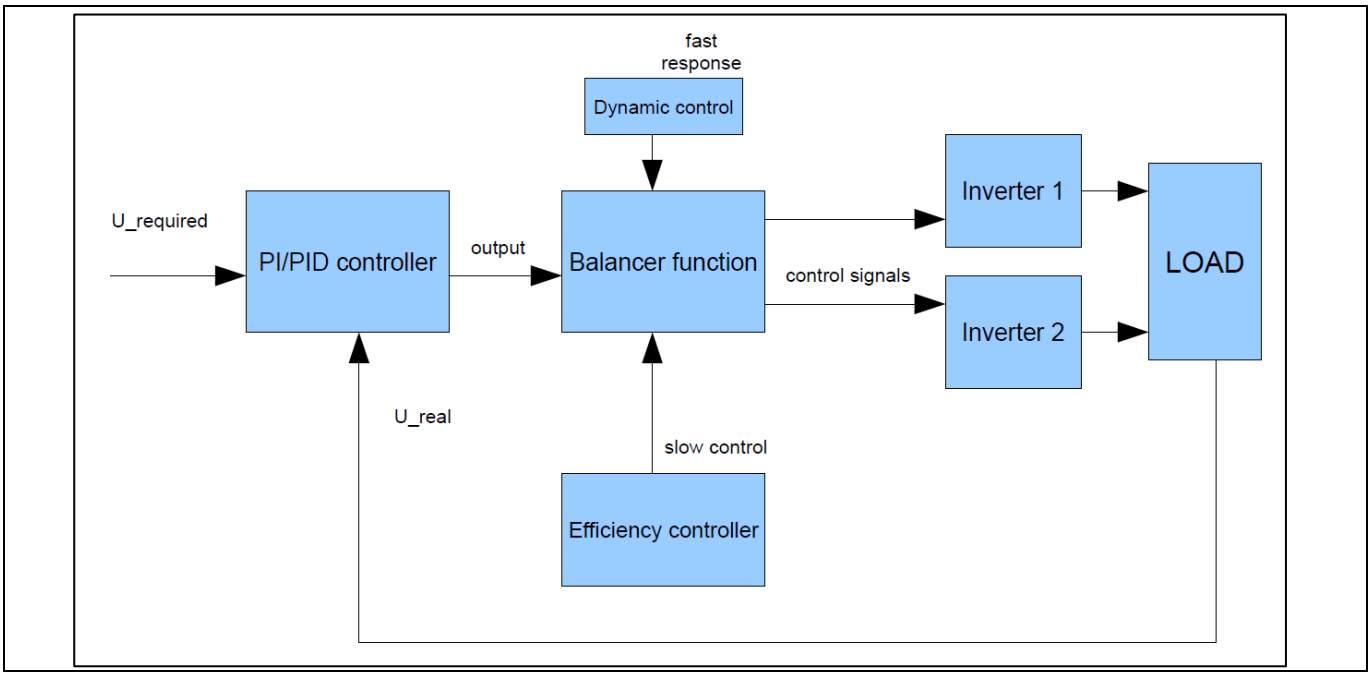


Figure 8 Implemented current sharing control

The implemented algorithm is also able to switch-off one of the two phases below certain output load, in order to guarantee a very flat efficiency plot in the entire load range. This technique is typically combined with the current sharing among two or more converters working in parallel and normally called “phase shedding”.

The importance of this feature appears clear if we look at the Figure 9, showing the typical operating time distribution of a HP SMPS used in telecom or industrial applications.

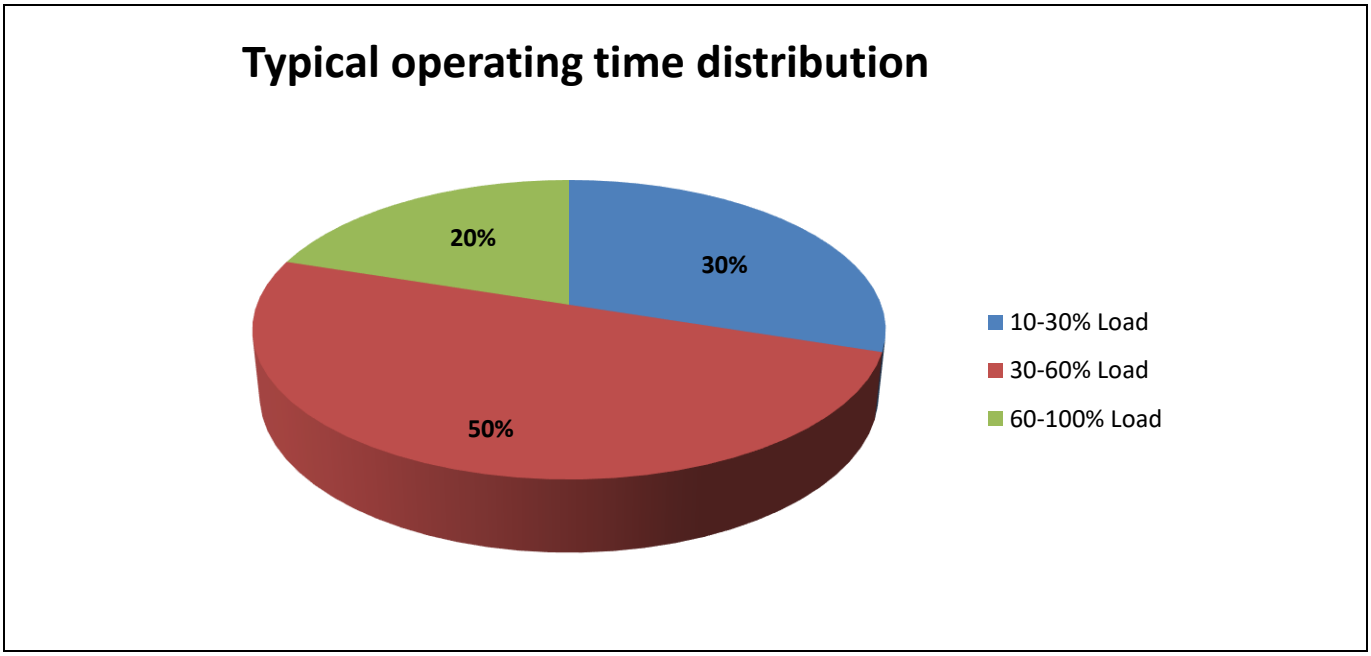


Figure 9 Example of operating time distribution of a typical 3 kW power converter for telecom or industrial application

You see that as average the most significant part of the operating time is spent in the 30-60% load range. The power supply also works for a considerable time in the range 10-30%, especially in N + 1 redundant system.

A minor portion is about the operation close to full load: hovewer, we know that this is the most critical from thermal perpective, so special care must be dedicated to it.

The Multiphase with phase shedding approach allows addressing the requirements of high efficiency not only at mid load (which is the “natural” behavior of a single phase converter), but also at light and heavy load, making possible the already mentioned flatness of the efficiency plot.

The performance achieved in the present demo board is described in details in the Chapter 5 of this document. In that section you’ll see the crucial contribution of the power devices, especially the new 600 V CoolMOS™ C7 family, along with the control technique by XMC™ controller.

In order to complete the introduction to our concept and corroborate its effectiveness, the Figure 10 just reports the final efficiency plot which has been achieved. One can appreciate the very high peak efficieny, but also the very flat plot over the entire load range.

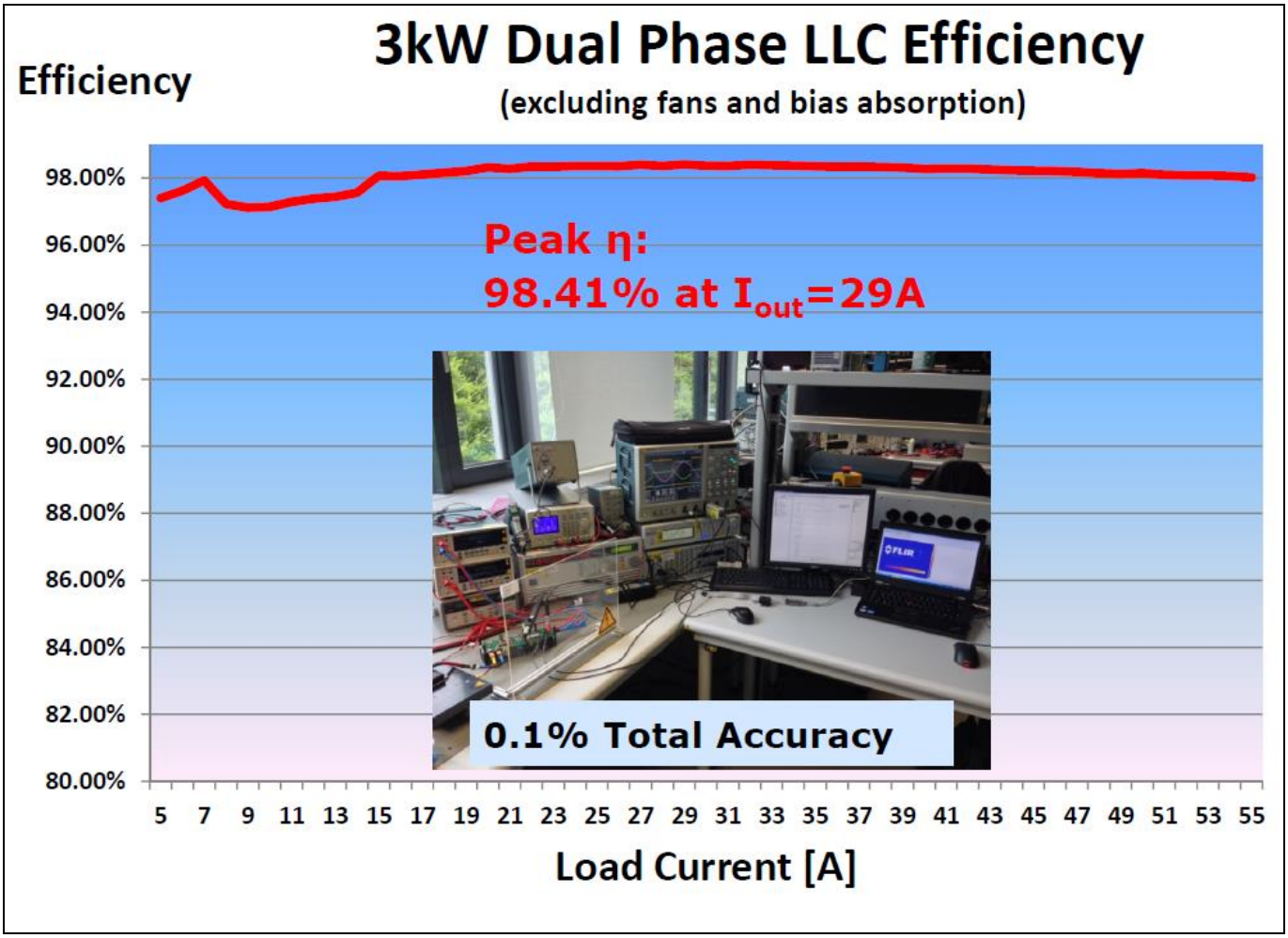


Figure 10 600 V CoolMOS™ C7 based 3 kW dual-phase LLC efficiency plot

2.2 Reliability features

The critical operating conditions of a HB LLC converter are well known in the SMPS designer’s community.

In fact, despite the knowledge about the HB LLC topology has significantly improved in the last 10 years, these crictical operations often still discourage SMPS designers to use that solution for high efficiency power converters where the reliability matters. In fact, those conditions are considered as a very challenging and tricky issue, since these might occur in the SMPS mass production, even in the field, despite the fact that this

has never been reproduced in the lab tests during the design and qualification phase. This is perceived by customers extremely risky. And to further confirm it, there are several studies showing that there is a huge difference in the cost to fix a SMPS problem at different phases of his life: e.g. the cost to fix it the field/final customer site is 1000 times higher than during the design phase.

These tricky operating conditions of the HB LLC converter have been already analysed in [1].

You can easily understand that in a dual-phase approach these troubles might be even amplified due to the synchronization of the two phases which may be critical especially during dynamic operation. So a special care must be dedicated to those aspects when designing LLC in multiphase approach.

It is worth to quickly re-call now the main problems which may occur in those critical operating conditions, before introducing the ways we use in order to prevent and solve it in our 3 kW dual-phase LLC.

The most known and dangerous mechanism unfortunately affecting the LLC operation is the so called hard commutation on the conduction MOSFET body diode. This may typically occur during the start-up sequence (illustrated in Figure 11), but also during burst mode or output short circuit and can lead into failure of the HV power devices in the primary side of the converter.

This problem occurs when in half bridge LLC configuration one of the two MOSFETs (let's call Q2, as in the Figure 11) is turned-off while its body diode is still not completely reverse recovered. If this happens, when the other device (Q1) turns-on, the MOSFET Q2 is submitted to heavy stress, since the $V_{O,PFC}$ voltage is applied between its drain and source while a huge reverse current is flowing through the body diode, creating a sort of shoot-through effect. This stress may lead firstly into device Q2 failure, and then also Q1 may be easily damaged. A very similar mechanism can be triggered during burst mode operation. The root cause of this behavior is the initial imbalanced voltage across the resonant capacitors, which leads to flux imbalance on the transformer primary side.

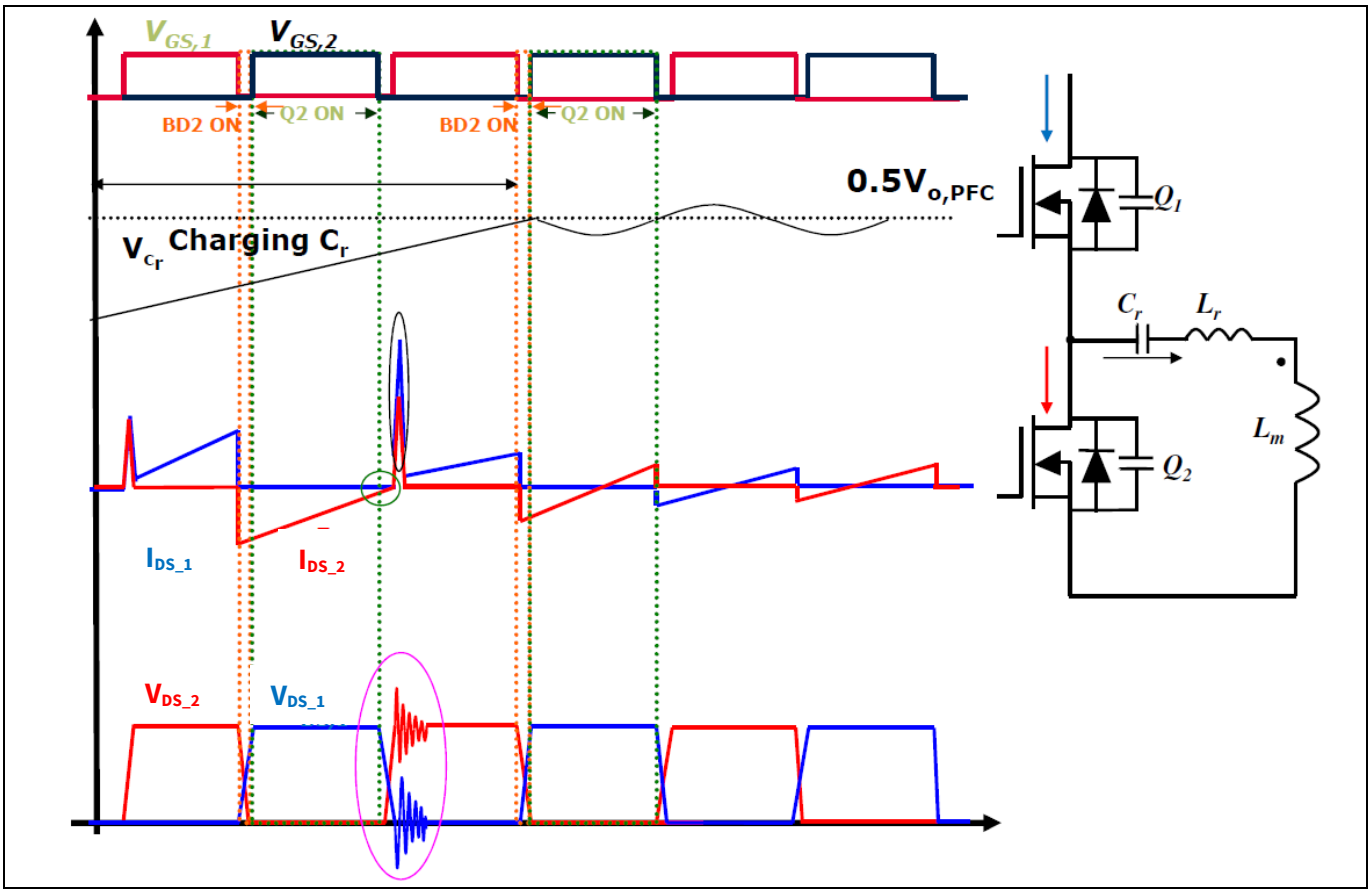


Figure 11 Hard commutation during HB LLC start-up sequence

The hard commutation may be also experienced during load dump in conjunction with secondary side synchronous rectification: a feedback of energy from secondary side to primary side may occur, which leads to reversal of tank current and thus to hard commutation on primary MOSFETs.

In general, hard commutation happens everytime the resonant current “leads” the resonant voltage, so that the voltage in the mid-point of the HB: this specific condition is well known as “capacitive load mode operation” of the LLC converter.

There are several ways to prevent hard commutation in HB LLC topology. Some of them are “by design” (like the use of the so called “split capacitor technique”). Actually it is impossible to precisely predict and avoid this condition by the converter design (e.g. LLC gain curves shape), without using a dedicated control strategy.

This latter is the way we decided to use with the goal to prevent hard commutation occurrence in all the possible triggering events, so not only at the startup or output overload, but in all those conditions, unpredictable by design, where the resonant current may potentially tend to “lead” the resonant voltage.

The proposed control is fully digital and located on the secondary side, which has a couple of benefits in transient response and output current measurement. The resonant current is guaranteed to be always lagging the resonant voltage: in fact the control is placed in the secondary side, but the primary side tank current is continuously monitored by using a current transformer providing the needed reinforced isolation.

The start-up and the burst mode sequences are based on the zero-crossing detection of the tank current, which is implemented totally inside the microcontroller without additional external hardware components (e.g. comparators). By detecting the tank current zero-crossing the control ensures change of sign of the tank current and thus current reversal in the main transformer. The 4 steps included in the start-up sequence will be explained with details in the Chapter 4.

The implemented algorithm also includes an additional procedure able to detect load dump and to prevent energy flow from secondary to primary side. The control measures the output current and detects a negative slope in the measured current (-di/dt), which indicates a fast decrease of load current. If a negative slope is detected a special Synchronous Rectification control is applied.

A special care is used in the capacitive load mode condition management, because this is recognized to be the most critical and often unpredictable HV MOSFETs failure mechanism in the LLC topology.

Our algorithm is able to implement both a prediction and an effective protection against it. The control measures the phase shift between resonant voltage and resonant current. Measurement for phase shift can be implemented by counting the time from the MOSFET turn off of the previous period until the tank current reverses (see Figure 12).

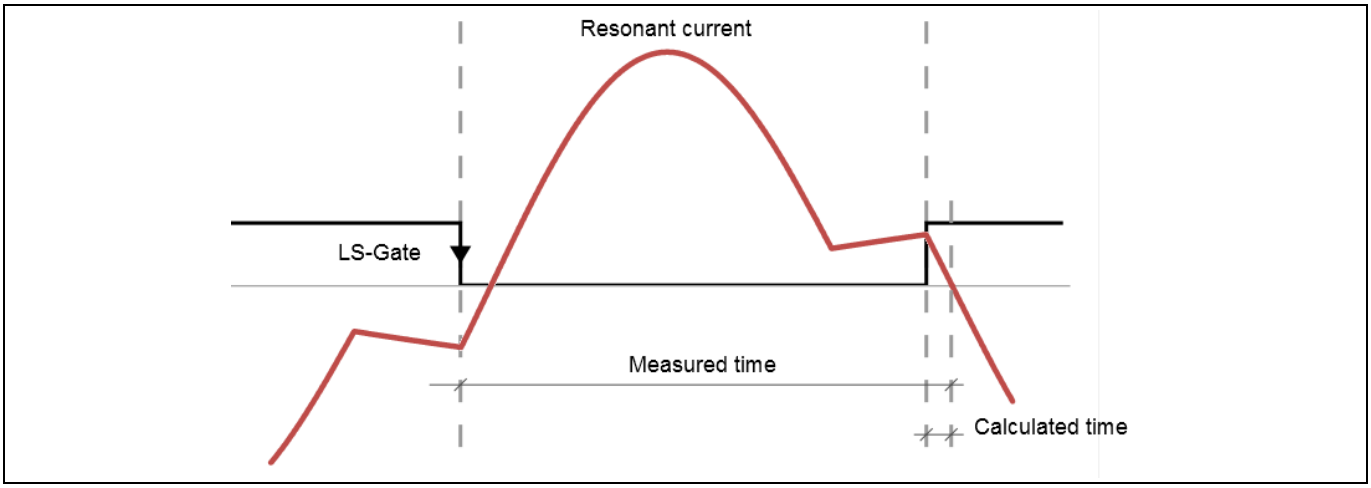


Figure 12 Capacitive load mode prediction & protection concept

The phase shift is calculated from the measured time, dead time and switching frequency. If the phase shift becomes zero the operation point is close to the capacitive mode. The control increases switching frequency to keep the operation point in the inductive region. This is the predictive or preventive feature implemented in our control. If a negative phase shift is sensed, it means that capacitive mode has already occurred, the failure can be then prevented by simply turning off the MOSFET and not turning on the other MOSFET in the next half-cycle. The half-bridge is also temporarily stopped as a precautionary measure to let the tank current decay to zero, and allow time for the switch node to bounce and the body diode of the MOSFET to be fully recovered: this is the failure protection feature of our algorithm.

2.3 Graphical User Interface (GUI)

A Graphical User Interface (GUI) has been designed as complementary tool of the 3 kW dual-phase LLC design with the purpose to allow an easy and intuitive interaction with the power converter.

In the GUI there is primarily the possibility to set some converter's electrical parameters, such as the value of the output voltage, max output current and related overcurrent protection threshold.

Moreover the GUI provides a continuous monitoring of the converter's operation, including in/out voltage and current or temperature on the transformer of both phases. Several status and fault registers are visible, allowing an immediate understanding of the reason of a fault condition.

The user may need to customize the operation of the board to his specific needs. For this reason the GUI gives also the possibility to re-configure the topology, by e.g. switching-off completely one of the two phases, then limiting the max power to 1.5 kW. Also the disable of the synchronious rectification stage is possible, in case a fine tuning is needed only using MOSFETs body diode rectification.

The GUI offers the feature to calculate the dead times in function of the output capacitance (C_{oss}) of the different MOSFETs which are used in the HB LLC: this allows to always optimize the design according to the different MOSFETs which may be used in the primary side, with the goal to always guarantee the ZVS behavior in the entire load range.

The user has also the possibility to adjust the converter's transfer function in order to optimize the dynamic performance and loop stability. The hidden and abstracted control concepts can be easily comprehended in a very precise and effective manner by means of a GUI. In fact, before the implementation of the control loop design, a simulation of it is a must. By doing so, the designer prevents problems that he will most likely face during the hardware implementation, normally with limited room for manoeuvre. On the other hand, getting optimal response through simulation requires certain skills in control system theory. So, the positioning of poles and zeros of the compensator is not easy to be minutely investigated especially by not very experienced designers. Moreover, the loop compensation is also heavily influenced by the total amount of output capacitance, including the one applied outside the Power Supply Unit (PSU). And this adddtional capacitance often changes from case to case even for the same PSU. In order to help the designers in this tedious part of their job, the GUI provides a menu where the total amount of additional external output capacitance can be set, and then the algoritm will automatically re-calculate poles and zeros of the transfer function in order to get in any case the loop stability, by fulfilling the technical spec. requirements:

Phase margin	min 45 degree @ 0 bode plot gain crossover frequency
Gain margin	min 10db @ 0 bode plot phase crossover frequency.

A more detailed description of the functions implemented in the GUI is included in a dedicated section of the Chapter 4 (see §4.8).

3 Board description

In the following sections the reader can find an overview on the 3 kW dual-phase demo board, with details about the technical specifications, the electrical schematics, the main active and passive components, including Infineon power devices and ICs and magnetic parts.

3.1 Main requirements in the technical specification

- Input voltage range 350-410 V_{dc}
- Nominal input voltage 380 V_{dc}
- Output voltage 44 V – 58 V ±1%
- Nominal output voltage 54 V_{dc}
- Max output current / power 55 A/3000 W
- dual-phase approach
- Power density >30 W/inch^3
- Efficiency target: 10/50/100% P_{max}=95%/98%/97.5%

3.2 General overview of the final design

The Figure 13 shows the basic structure of the 3 kW dual-phase LLC design.

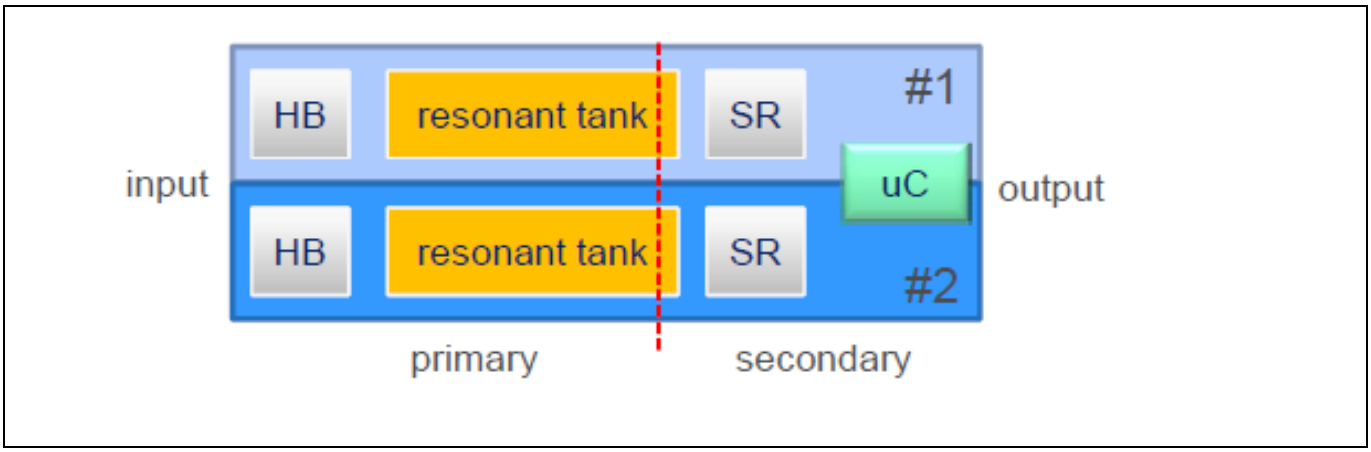


Figure 13 3 kW dual-phase LLC: basic concept

The board consists of two HB LLC converters working in parallel: each of them has its own resonant tank and synchronous rectification stage. For the sake of simplicity, we'll call these converters respectively Conv1 and Conv2, as in the simulation described in the previous chapter. A single microcontroller located in the secondary side controls both converters. It generates the PWM signals for both primary and secondary MOSFETs and manages the current sharing and all the advanced fetaures which will be analysed in depth in the following Chapter 4.

The Figure 13 shows a real picture of the 3 kW dual-phase LLC demo board and highlights the position of the most significant components, including of course the Infineon products which have been used inside.

A main power board and two daugher cards are visible in Figure 14. In the main board all the power components are assembled, including MOSFETs and magnetic parts. The first daughter card hosts the microcontroller and the related logic circuitry, so this is identified as "control card". The second daughter board (namely "bias card") hosts the auxiliary converter, which is done with a quasi resonant flyback converter:

as typical in HP SMPS, this small converter provides the voltages needed to supply the logic circuitry and the two ventilators, also visible in the Figure 14.

Section 3.3 gives an overview of the Infineon components which have been used in the present design, by highlighting the main feautures of them. Section 3.4 will go into the details of the electrical schematics and the magnetic components specification.

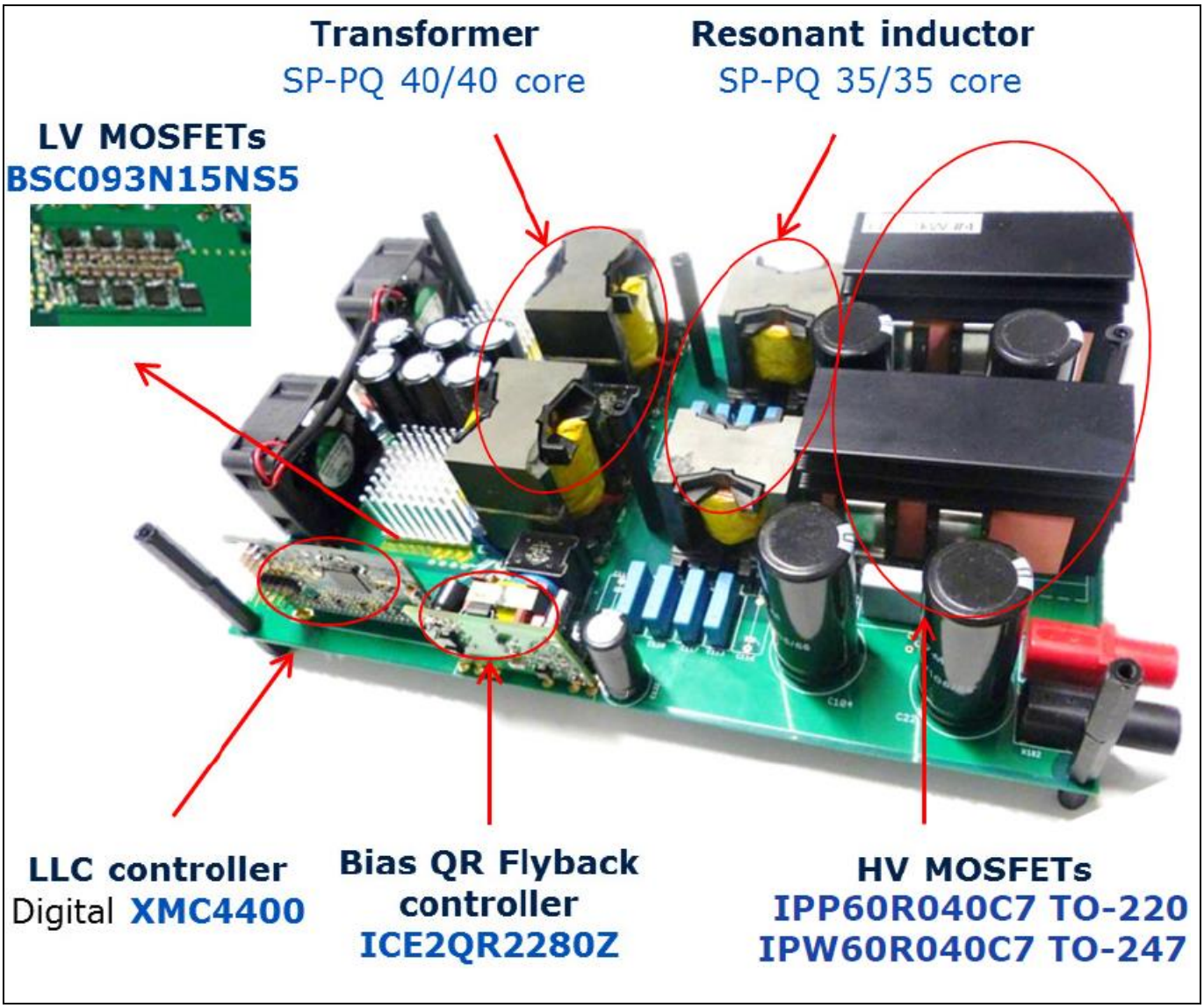


Figure 14 The 3 kW dual-phase LLC demo board

3.3 Infineon components

3.3.1 Primary HV MOSFETs 600 V CoolMOS™ C7

The 600 V CoolMOS™ C7 is the next step of silicon improvement based on the 650 V CoolMOS™ C7. It stays with the strategy to increase switching performance in order to enable the highest efficiency in any kind of target applications, such as for boost topologies including PFC's (power factor correction) and soft switching high voltage DC-DC stages such as LLC's (DC-DC stage with resonant tank in order to maintain zero voltage switching). Although the 600 V CoolMOS™ offers very fast switching it also retains the ease of use (ease of controlling the switch) of the 650 V C7 "mother technology". Therefore the 600 V CoolMOS™ C7 is an optimized device for highest efficiency SMPS.

In an LLC application, the converter is in resonant operation with guaranteed ZVS even in a very light load condition. Switching loss caused by E_{oss} during turn-on can be considered negligible in this topology. With this consideration, the CoolMOS™ C7 family offers a superior price/performance ratio with a low FoM ($R_{DS(ON)}$*Q_G and $R_{DS(ON)}$*Q_{OSS}), which means that the MOSFET switching transitions are fast, allowing very short deadtime. This will result in lower turn-off losses further improving the efficiency.

In the 3 kW LLC demo board the 600 V C7 can be used both in the TO-220 and TO-247 packages.

The following are additional features and benefits of the CoolMOS™ C7:

- Suitable for hard and soft switching (PFC and high performance LLC)
- High dv/dt ruggedness up to 120 V/ns
- Best in class FoM $R_{DS(ON)}$*E_{oss} and $R_{DS(on)}$ *Q_G
- Best in class $R_{DS(ON)}$/package
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)

3.3.2 Isolated gate drive 1EDI60N12AF

The Infineon EiceDRIVER™ 1EDI compact family consists of a single channel high voltage gate driver ICs with integrated Coreless Transformer (CLT) technology and a maximum offset voltage of 1200 V. The 1EDI compact driver ICs are available in a compact PG-DSO-8 (150 mil) package and provide either separated source/sink outputs or a single output with an additional clamping function.

Summary of the 1EDI60N12AF features:

- Separate source/sink output
- I_{out}: 6 A @ 15 V
- 1200 V Coreless Transformer IC with galvanic isolation
- Prop. delay <105 ns with 40 ns input filter time
- High CMTI robustness >100 V/ns

Benefits:

- Tailored for all 600 V CoolMOS™ C7 and P6 families and in general for super junction MOS transistors
- High switching frequency applications as SMPS, up to 4 MHz
- Turn-off vs. turn-on fine tuning
- High reliability @ small footprint

In the present demo board, the 1EDI60N12AF is used to drive the high side and low side MOSFETs of each of the two HB LLCs. Its reduced propagation delay is an important feature in our application due to the microcontroller position at secondary side; morever the high CMTI and the possibility of split source and sink outputs help to get full benefits out of the 600 V C7 fast switching behavior.

3.3.3 SyncRec MOSFETs OptiMOS™ BSC093N15NS5

The OptiMOS™ 5 150 V dramatically improved the $R_{DS(ON)}$ per package for this voltage range: 9.3 mΩ is available even in the compact Super SO8 package, which has been used in the present demo board. This allows the customer to switch from the full-bridge synchronous rectification topology on the secondary-side to the center-tap transformer approach yielding simplicity in the design and cost reduction (simple low-side drivers needed instaed of 2 half-bridge drivers).

This is in fact the main reason why we opted for a center tapped transformer in the present 3 kW LLC design despite the relatively high output voltage.

The OptiMOS™ 5 150 V has a more linear output capacitance, and yet reduced total output charge in comparison with the previous generation: this contributes to reduce any voltage overshoot.

The body diode has increased ruggedness due to the reduced Q_{rr} offered by the new technology: this brings reduced overshoot when the converter operates above resonance and during abnormal conditions.

Finally, the typical OptiMOS™ 5 technology very tight matching of some key parameters like $V_{GS,th}$ is a fundamental feature in order to guarantee a reliable synchronous rectification operation especially in a dual-phase design, where moreover each of the phases use several paralleled devices in each brach.

3.3.4 Advanced dual channel gate drive 2EDN7524

The fast dual channel 5 A non-isolated gate-driver is an advanced dual-channel driver optimized for both standard and superjunction MOSFETs, as well as GaN power devices, in all applications in which they are commonly used. The input signals are TTL compatible with a high-voltage capability up to 20 V and down to -5 V. The unique ability to handle -5 V_{DC} at the input pins protects the IC inputs against ground bounce transients.

Each of the two outputs is able to sink and source current up to 5 A utilizing a true rail-to-rail stage, that ensures very low impedances of 0.7 Ω up to the positive and 0.55 Ω down to the negative rail. Very low channel-to-channel delay matching (typically 1 nS) is implemented which enables the double source and sink capability of 10 A by paralleling both channels.

Different logic input/output configurations guarantee high flexibility for all applications; e.g. with two paralleled switches in a boost configuration. The gate driver is available in 3 package options: PG-DSO-8, PG-VDSON-8 and PG-TSDSO-8-X (size minimized DSO-8).

In the present demo board, the 2EDN7524 is used to drive the Synchronous Rectification (SR) MOSFETs. In this application the 5 A peak current capability and the very precise channel to channel delay matching, along with the high reverse current capability and negative input capability are beneficial features in order to guarantee a SR efficient but also reliable operation. In fact the aspect of reliability and perfect delay time matching is very important in the complex SR management inside a dual-phase LLC design.

3.3.5 XMC4400 microcontroller

The XMC4400 combines Infineon's leading-edge peripheral set with an industry-standard ARM® Cortex®-M4F Core.

The control of SMPS is a strong focus for XMC™ microcontrollers where users can benefit from features such as smart analog comparators, high-resolution PWM timers and the ARM® Cortex®–M4F DSP instruction set including floating point or high precision analog to digital converters.

As a key feature it offers a high-resolution PWM unit with a resolution of 150 pS. This unique peripheral makes it especially suitable for digital power conversion in applications such as solar inverters as well as SMPS and uninterruptible power supplies (UPS). The XMC4400 is supported by Infineon’s integrated development platform DAVE™, which includes an IDE, debugger and other tools to enable a fast, free of charge and application-orientated software development.

Summary of XMC4400 features:

- ARM® Cortex®-M4F, 120 MHz, incl. single cycle DSP MAC and floating point unit (FPU)
- 8-channel DMA + dedicated DMA for USB
- CPU frequency: 120 MHz
- High ambient temperature range: -40°C to 125°C
- Wide memory size options: up to 512 kB of flash and 80 kB of RAM

- HRPWM (High Resolution PWM) allowing PWM adjustment in steps of 150 ps
- 12 bits ADC, 2 MSample/sec. Flexible sequencing of conversions including synchronous conversion of different channels
- Fast and smart analog comparators offer protections such as overcurrent protection, including filtering, blanking and clamping of the comparator output. A 10 bit DAC with a conversion rate of 30 MSamples/sec provides an internal reference for the comparators that can be configured to be a negative ramp for slope compensation purposes
- A flexible timing scheme due to CCU timers and HRPWM (High Resolution PWM). These timers allow the creation of almost any PWM pattern and synchronize PWM signals with ADC measurements accurately.
- Interconnection matrix to route different internal signals from one peripheral to another. For example, the comparator output can connect to a PWM timer to indicate an overcurrent protection event and immediately switch off the PWM output
- Communication protocols supported including USB, UART, I2C, SPI
- USB 2.0 full-speed device
- Package: PG-LQFP-64

3.3.6 Bias QR flyback controller ICE2QR2280Z

ICE2QRxxxx is the second generation quasi-resonant PWM CoolSET™ with power MOSFET and startup cell included in a single package optimized for off-line power supply applications such as LCD TV, notebook adapter and auxiliary/housekeeping converter in SMPS. The digital frequency reduction with decreasing load enables a quasi-resonant operation down to a very low load. As a result, the average system efficiency is significantly improved compared to conventional solutions. The active burst mode operation enables ultra-low power consumption during standby mode operation and low output voltage ripple. The numerous protection functions give full protection of the power supply system in potential failure situations.

In the 3 kW demo board the ICE2QR2280Z is used in the auxiliary converter, which has the task to generate all the voltages supplying logic circuitry and ventilators.

The key features of the ICE2QR2280Z for use as an auxiliary converter of this LLC evaluation board are:

- High voltage (800 V) avalanche rugged CoolMOS™ with startup cell
- Quasi-resonant operation
- Load dependent digital frequency reduction
- Active burst mode for light load operation
- Built-in high voltage startup cell
- Built-in digital soft-start
- Cycle-by-cycle peak current limitation with built-in leading edge blanking time
- Foldback point correction with digital sensing and control circuits
- V_{CC} undervoltage and overvoltage protection with autorestart mode
- Over load /open loop protection with autorestart mode
- Built-in over temperature protection with autorestart mode
- Adjustable output overvoltage protection with latch mode
- Short-winding protection with latch mode
- Maximum on time limitation
- Maximum switching period limitation

3.4 Board schematics

3.4.1 LLC switching power stage

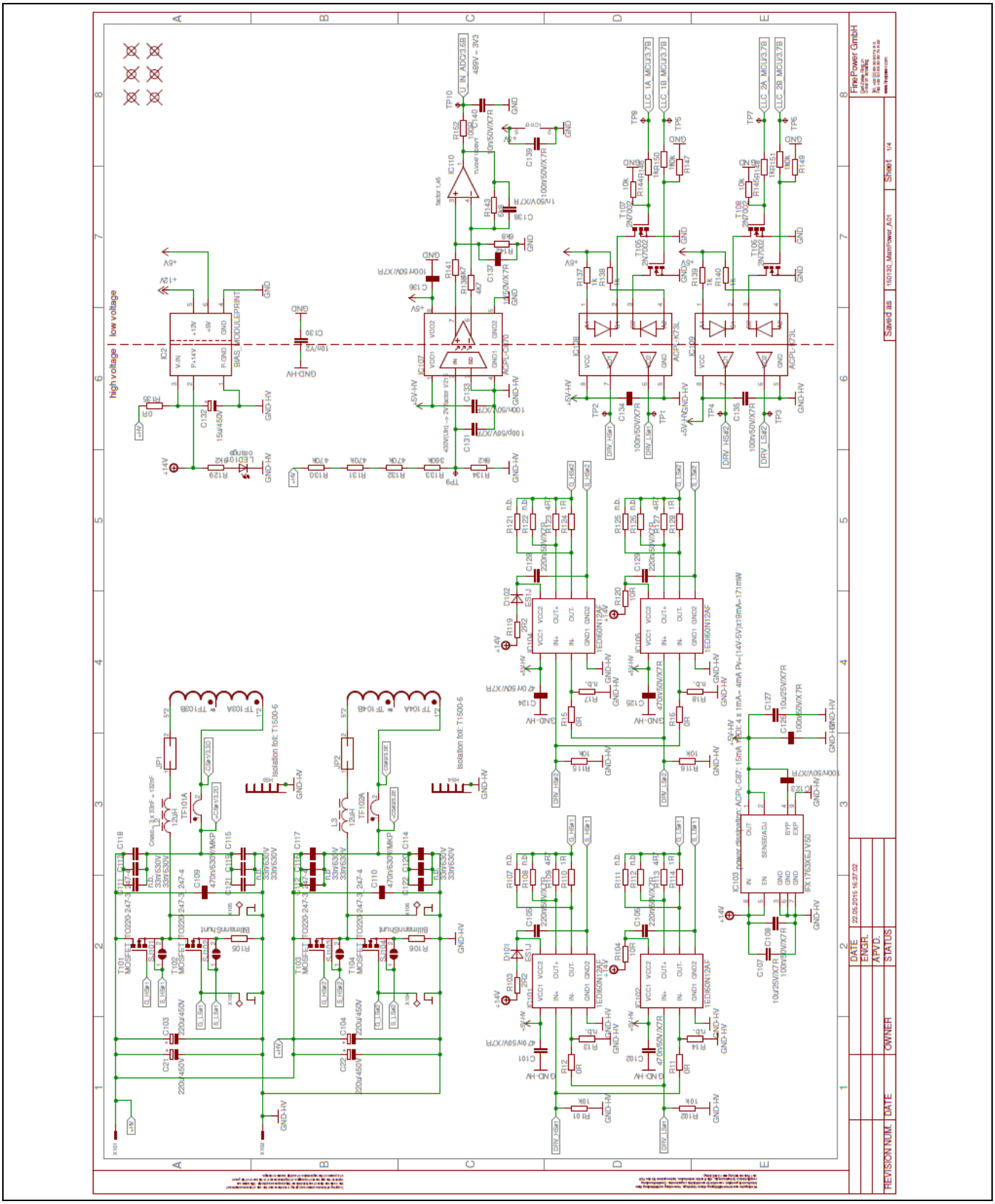


Figure 15 Primary HV power stage

3.4.2 Synchronous rectification and secondary stage

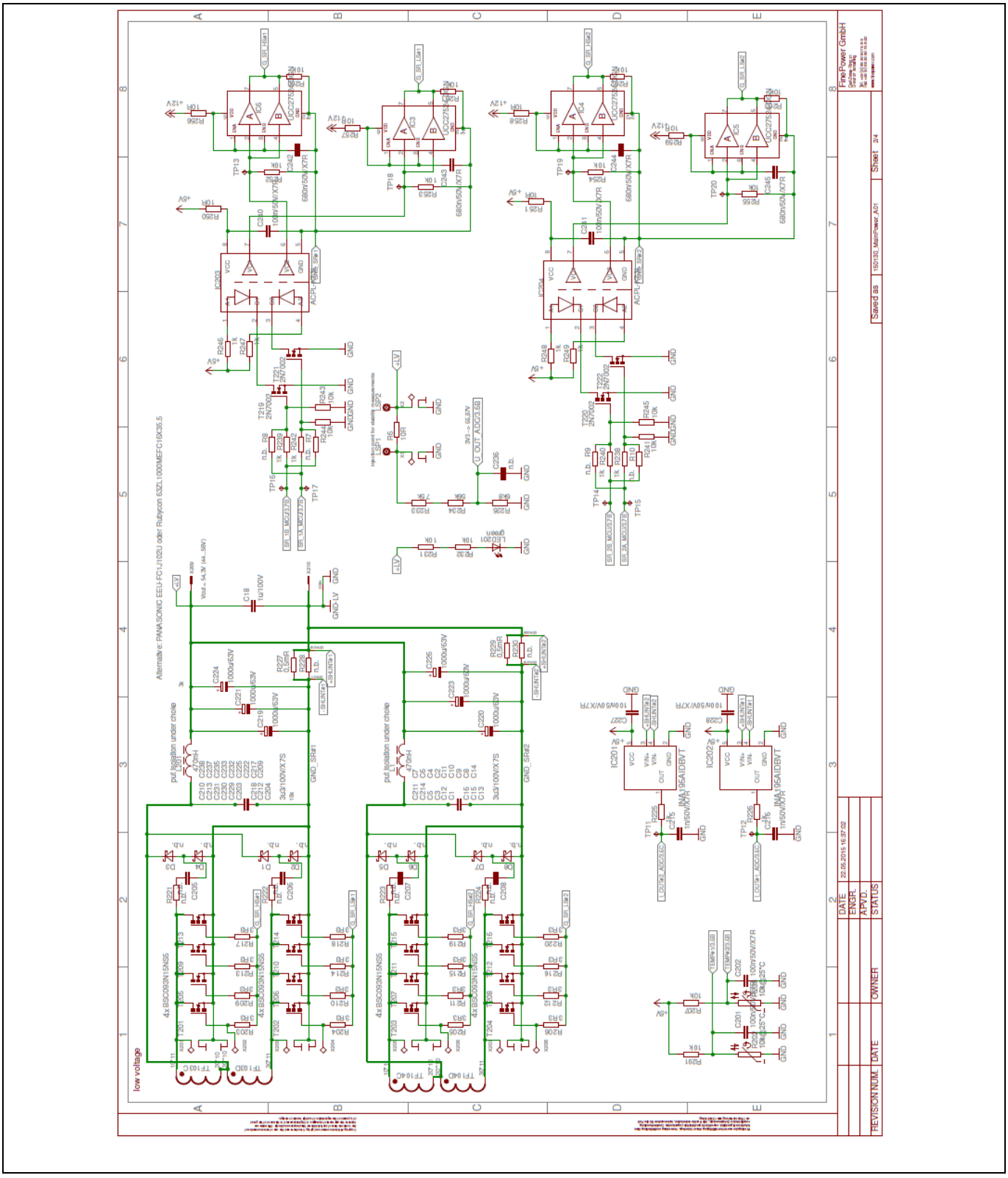


Figure 16 Secondary side power stage

3.4.3 Control board

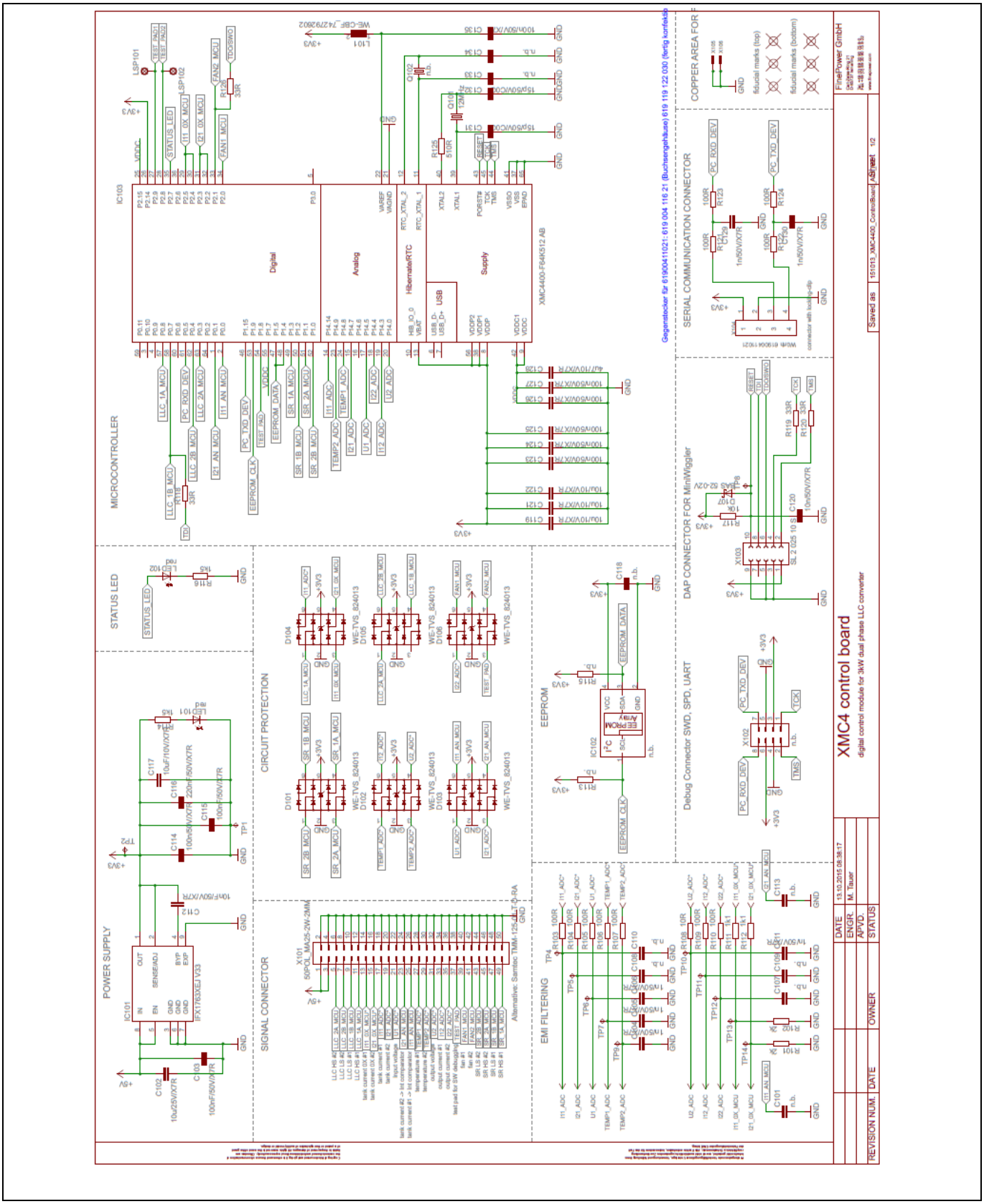


Figure 17 Control board schematics

3.4.4 Bias board (auxiliary converter)

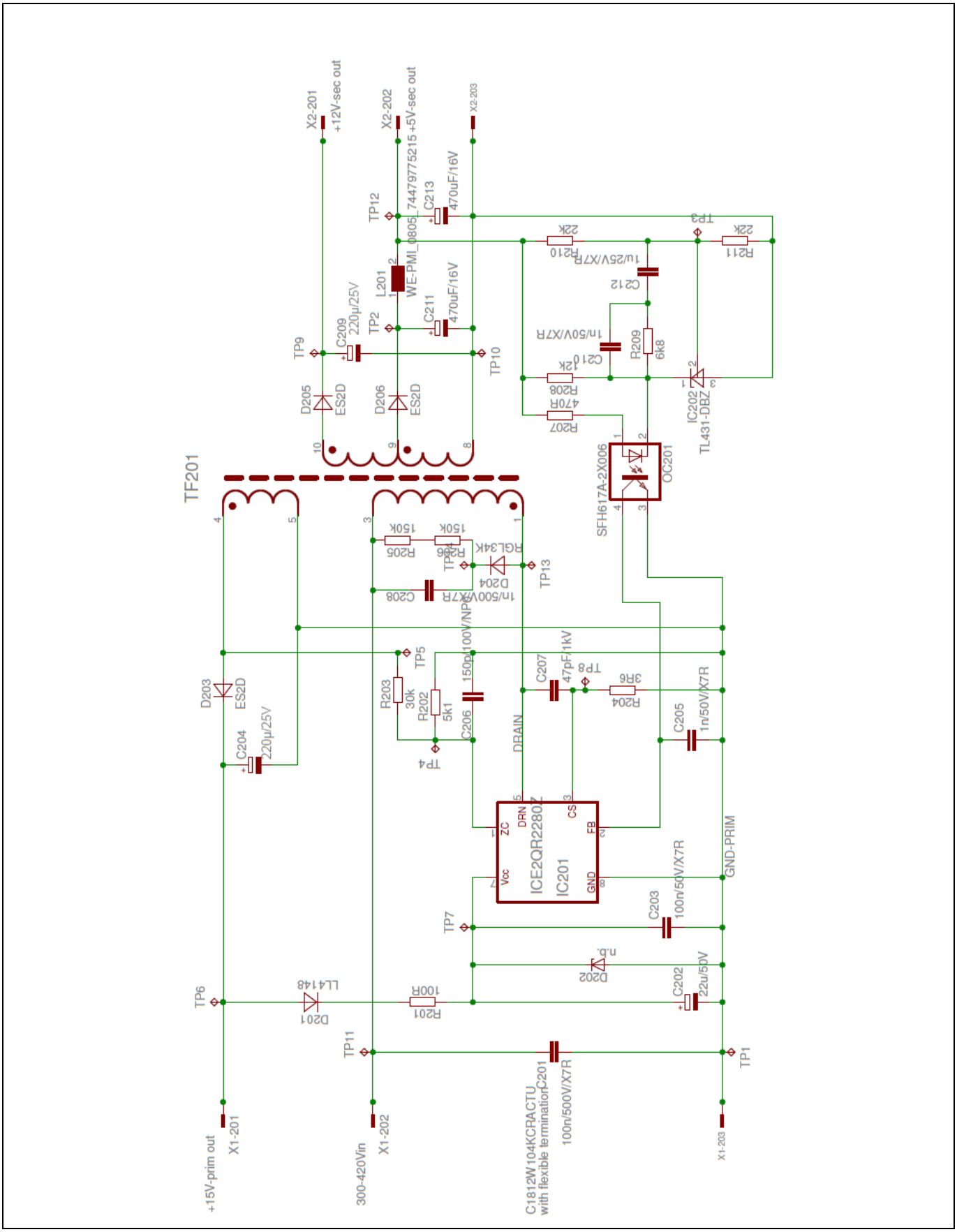
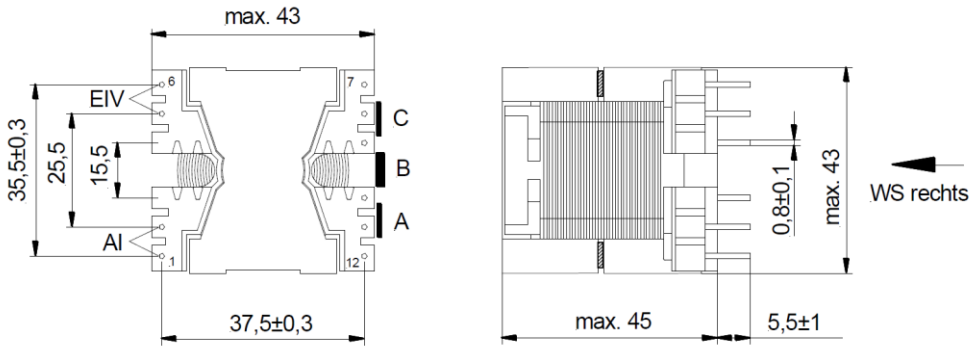


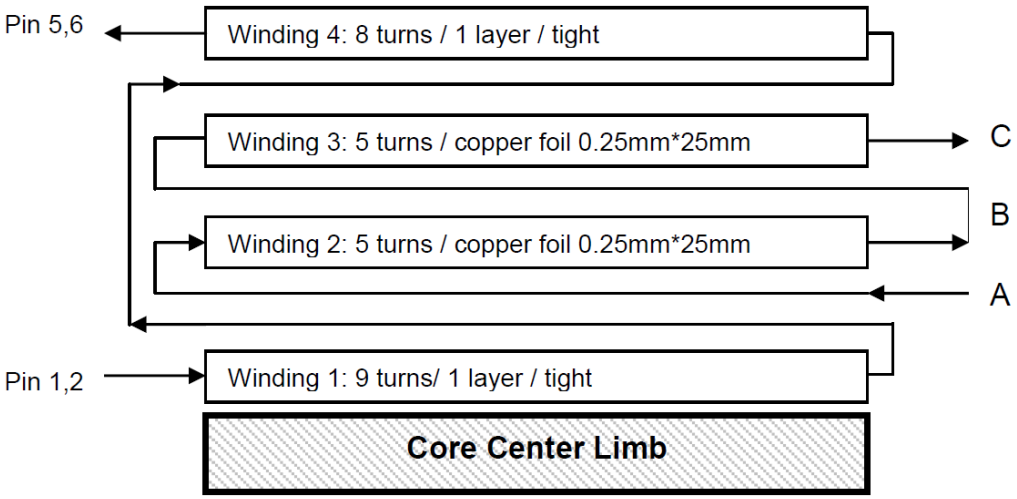
Figure 18 QR flyback auxiliary converter

3.5 Magnetic components

3.5.1 HB LLC main transformer



Core form and material	PQ40/40, N95
Bobbin	Epcos, B65884E0012D001
Primary inductance L_p	78uH, measured between 1,2 and 5,6, other pins open
Airgap	Distributed air gap on all three limbs
Leakage inductance L_{lk}	0.5uH, measured between 1,2 and 5,6, other pins shorted
Isolation voltage V_{iso}	2500V_{rms} / 50Hz, 1min (between 1,2,3,4,5,6 and A,B,C)

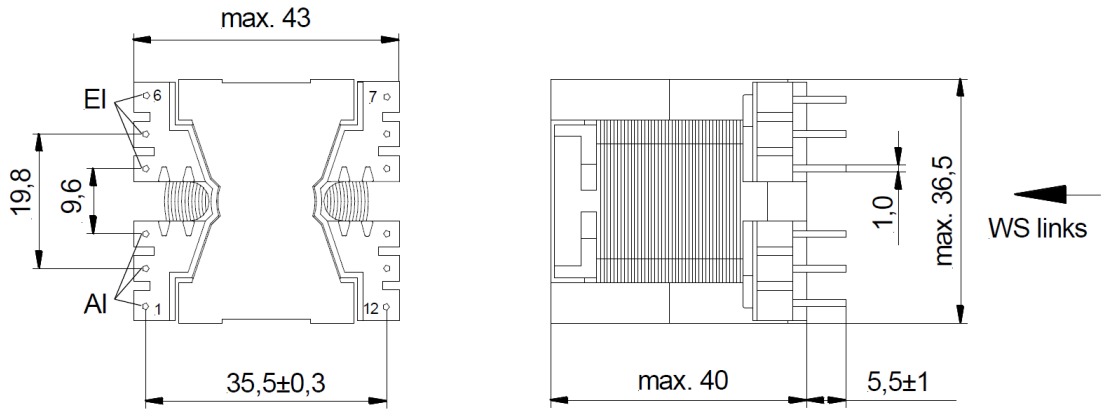


Windings	Start	End	Wire	Turns	Layers	Method
1	1,2	3 **or** float	60x0.2mm Litz **or** 2 times 30x0.2mm Litz	9	1	Tight
2	A	B	0.25mm*24mm copper foil	5	1	Tight
3	B	C	0.25mm*24mm copper foil	5	1	Tight
4	4 **or** float	4,5,6	60x0.2mm Litz **or** 2 times 30x0.2mm Litz	8	1	Tight

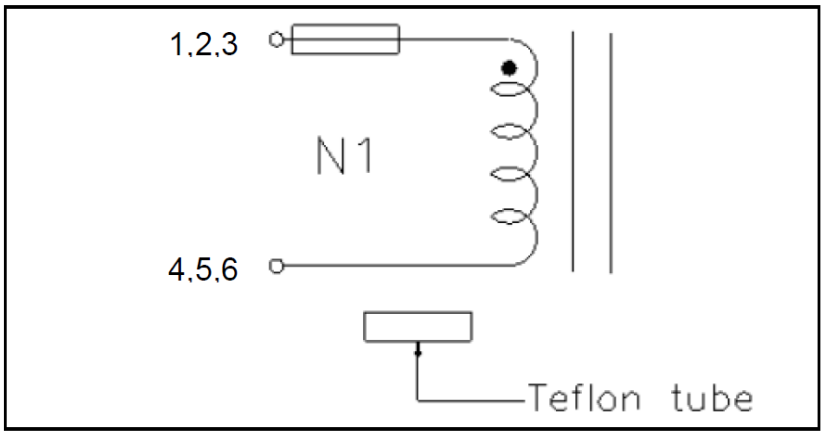
The transformer is produced by Infineon trusted partners in development and manufactuting of magnetic components:

- **Kaschke Components GmbH** – Göttingen, GERMANY - **https://www.kaschke.de/kaschke-en/**
- **ICE Transformers s.r.l.** – Loreto Aprutino (Pescara), ITALY - **https://www.icetransformers.com/en/**

3.5.2 LLC resonant choke



Core form and material	PQ35/35, N95 (Epcos)
Bobbin	12Pin-Standard-Bobbin e.g. NORWE 90369-087 (PQ 35-35/1k/-8/mo/rtg)
Inductance L	6.5 uH

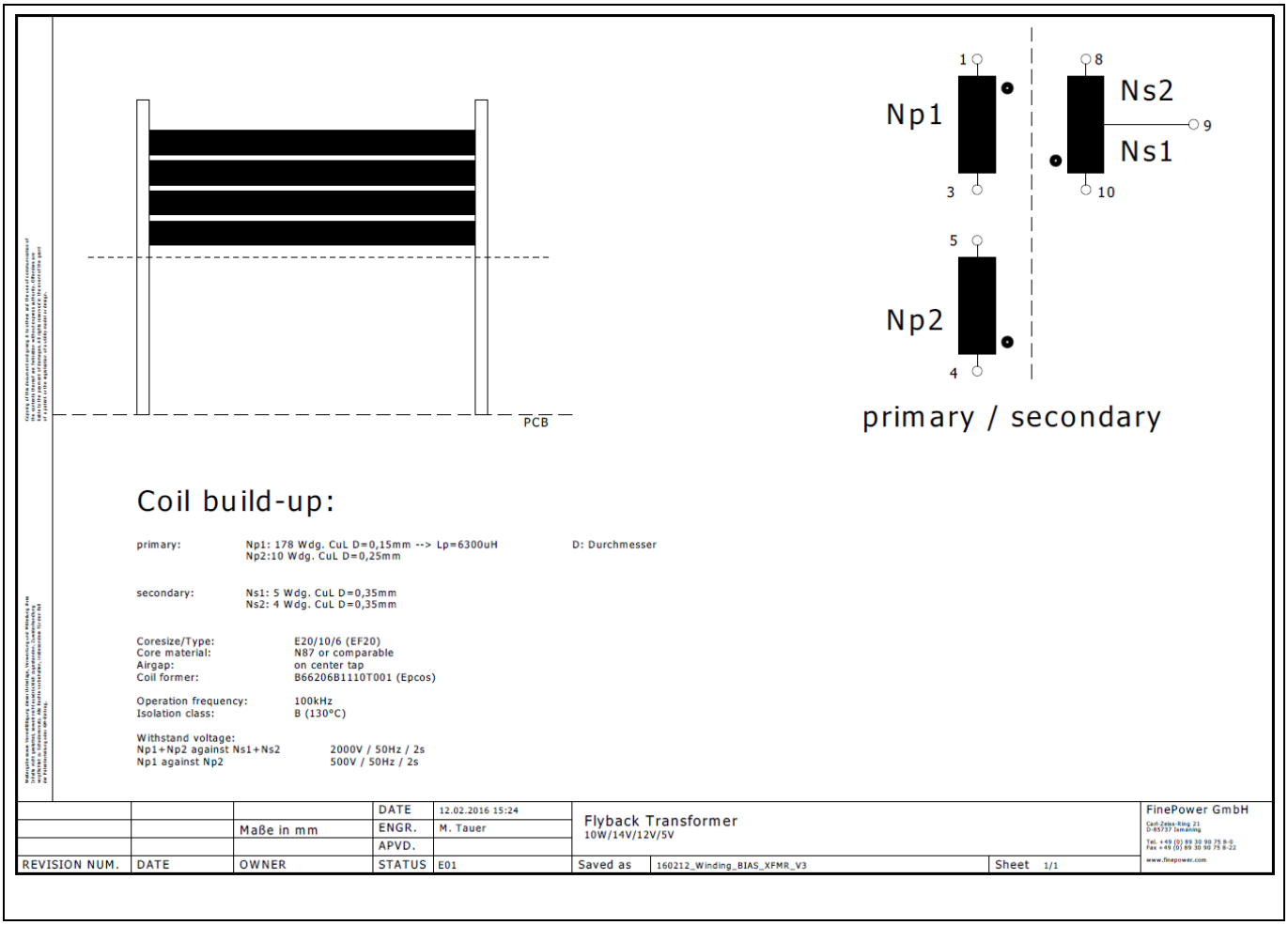


Windings	Start	End	Wire	Turns	Layers	Method
N1	1,2,3	4,5,6	60x0.2mm Litz	9	1	Tight

The inductor is produced by Infineon trusted partners in development and manufactuting of magnetic components:

- **Kaschke Components GmbH** – Göttingen, GERMANY - **https://www.kaschke.de/kaschke-en/**
- **ICE Transformers s.r.l.** – Loreto Aprutino (Pescara), ITALY - **https://www.icetransformers.com/en/**

3.5.3 Auxiliary transformer



The transformer is produced by Infineon trusted partners in development and manufactuting of magnetic components:

- **Kaschke Components GmbH** – Göttingen, GERMANY - **https://www.kaschke.de/kaschke-en/**
- **ICE Transformers s.r.l.** – Loreto Aprutino (Pescara), ITALY - **https://www.icetransformers.com/en/**

4 Digital control features

The control of the 3 kW dual LLC Converter has been implemented using XMC4400, which is part of the XMC™ microcontroller family from Infineon Technologies. This family is based on an ARM Cortex-M4 core, and the main features were summarized in section 3.3.5. The following chapter will introduce the main features of the implemented digital control as well as the resources necessary for a proper implementation.

4.1 Resources used and implementation concept

4.1.1 Resources (peripherals) used

XMC4400 has been selected due to the complexity of the design, which requires a high number of peripherals as well as a high calculation power. By using as an example the required peripherals for one of the LLC phases, this section presents the necessary resources for the multiphase LLC design.

Figure 17 depictes the available resources in the selected XMC4400 microcontroller. For a single LLC phase the following resources are used:

- Four timers for PWM generation of both half-bridge and synchronous rectification switches. XMC4400 includes two different timers (CCU4 and CCU8) which provide not only PWM outputs but a flexible and programmable signal conditioning scheme thanks to the available interconnections with other peripherals. In the dual LLC two CCU4 and two CCU8 timers are used for each phase.
- Two event request unit (ERU) slices for proper interconnection of the timers. The ERU is a versatile event detection and processing unit which allows increasing the peripheral connectivity.
- One high resolution PWM (HRPWM) which includes a high resolution timer (HRC) and an analog comparator with slope generation (CSG).
- Five ADC channels. These include the input and output voltage sensing, which are common for both phases, as well as output current, resonant current and temperature, which are measured for each phase.
- Apart from compare mode to generate PWM signals, CCU4 timers can be used in capture mode in order to adquire time between different events. Two CCU4 timers used in capture mode for frequency and time adquisition.

Apart from these specific resources, other shared peripherals are required for proper operation of the application:

- One serial communication channel (USIC) is used for communication with the graphical user interface (GUI). The USIC configured in UART mode can be connected to a PC through a serial COM port. This channel is associated with two interrupts for receiving and transmmiting the data.
- XMC4400 processor has a 24-bit system timer (SysTick) which count down to zero from a defined value. This special timer is used in the dual LLC for scheduling purposes to trigger a fixed frequency interrupt. The application SW is executed in this interrupt.
- Part of the flash memory is utilized to store the converter parameters sent via GUI. XMC4400 provides up to 512 kB of flash memory and therefore, no external EEPROM is necessary.

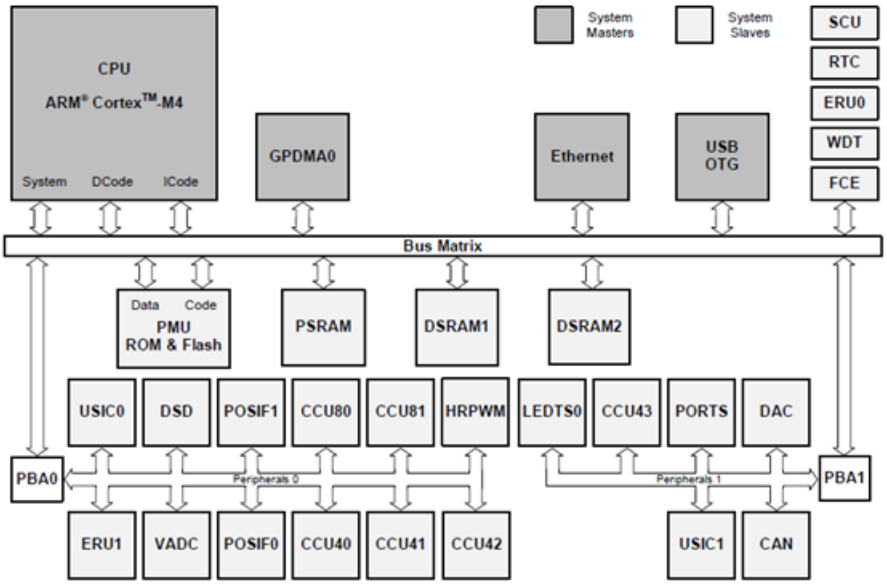


Figure 19 XMC4400 system resources

Considering the previously introduced resources, the total amount of resources is summarized in Table 1.

Table 1 Peripherals used in the dual LLC control implementation in XMC4400.

XMC Peripheral	Resource	used / available
CCU8	timer	6 / 8
CCU4	timer	8 / 16
VADC	channel/pin	8 / 9
USIC	channel	1 / 4
PORTS	pin	33 / 44

4.1.2 Implementation concept

Besides the presented peripherals, the implemented control algorithms are executed in a regular time base. The system timer (SysTick) sets this regular time base, thus fixing the sample rate as well as the loop execution. The main functionality of the multiphase converter is implemented in the control interrupt routine, triggered by the system timer (Figure 20). This functionality includes the following processes:

- Output current limitation protection
- Capacitive mode protection
- Burst mode management
- PI controller
- Start sequence
- Phase shedding
- SR management
- Dead time calculation
- Software ADC trigger of the control variables.

Digital control features

As shown in Figure 18, the PWM signal with 50% duty cycle is generated using a CCU8 timer. The flexibility of this peripheral in the XMC4000 series enables a synchronized trigger of the resonant current ADC measurement with the generated PWM signal.

In addition, the versatile ADC enables the scheduling of different measurements by using different measurement groups with different triggers and priorities. In the selected implementation the resonant current is measured using the queue function triggered by the PWM. However, the rest of channels are configured as background measurements with lower priority and triggered by SW in the control interrupt.

Furthermore, the CCU8 timer can be easily connected to the high-resolution channel of the HRPWM peripheral. This connection not only allows the utilization of the 150 ps PWM resolution of this peripheral but enables the update of the PWM dead time in a safe manner as it will be explain later.

More information about the highly configurable ADC and timer peripherals can be found in [14].

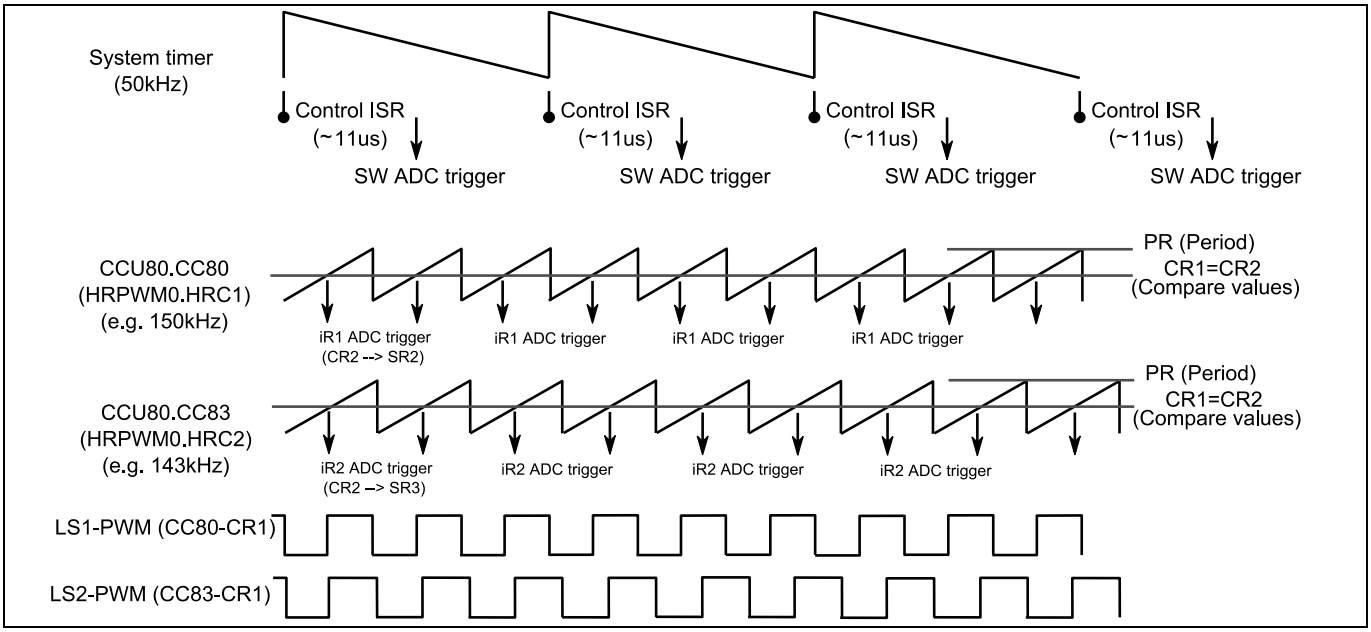


Figure 20 Time diagram of the 3 kW dual-phase LLC converter digital control implementation.

As presented above, the selected implementation is based on a single interrupt whih the highest priority. However, there are other tasks which are implemented in different background processes. Since the interrupt cannot be preempted by the lower priority tasks, such as the background ones, these last ones are assessed in the remaining processing time between interrupts:

- State machine
- Fault management
- SR time calculation
- Compensator coefficients according to output capacitance selection.
- Power balance between phases
- Memory observer
- Communication with GUI
- Time counting

In the next sections the main functionality implemented in the 3 kW dual half-bridge LLC converter will be presented in more detail.

4.2 Current-sharing and phase shedding

In section 2.1.2 the concept of the implemented current sharing is presented. As already explained both converter phases are controlled using related, but different, switching frequencies in order to balance the current between the phases. This difference in switching frequency can be observed in Figure 21 by the difference in phase of both resonant currents at different moments in time, for the same output power. In addition, the number of active phases is modified according to the load level with the goal of achieving a flat efficiency in a wide load range.

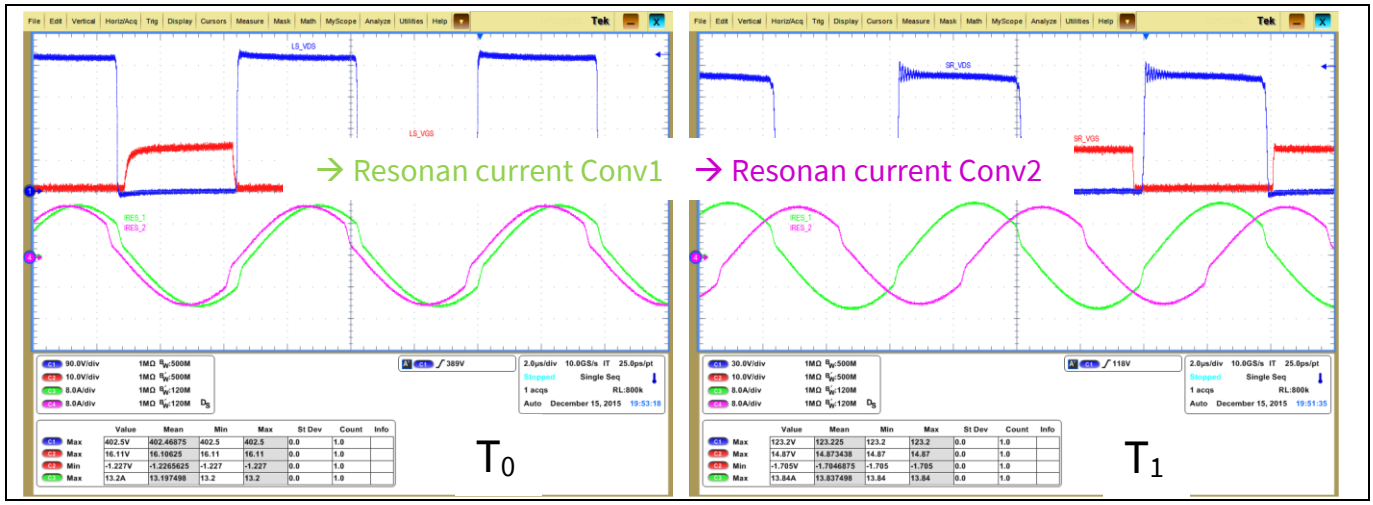


Figure 21 Phase difference of phase 1 (green) and phase 2 (purple) resonant currents at the same power at two different moments in time.

The implemented current sharing and phase shedding which was introduced in Figure 8, is redrawed in Figure 22 to show the different blocks involved in the process: both LLC phases (Conv1 and Conv2), a PI controller to ensure output voltage regulation and a current balancer which decides the switching frequency to be applied to each phase.

The PI controller is evaluated every control interrupt (50 kHz) according to the sensed output voltage and the required voltage target. This voltage target varies during soft-start and it can have different steady-state values, according to the specifications presented in section 3.1. The steady-state output voltage can be modified via GUI.

The output of the PI controller, which is the necessary switching frequency to match the input-output voltage gain, is fed to a current balancer block, together with the output current measurements of each LLC converter.

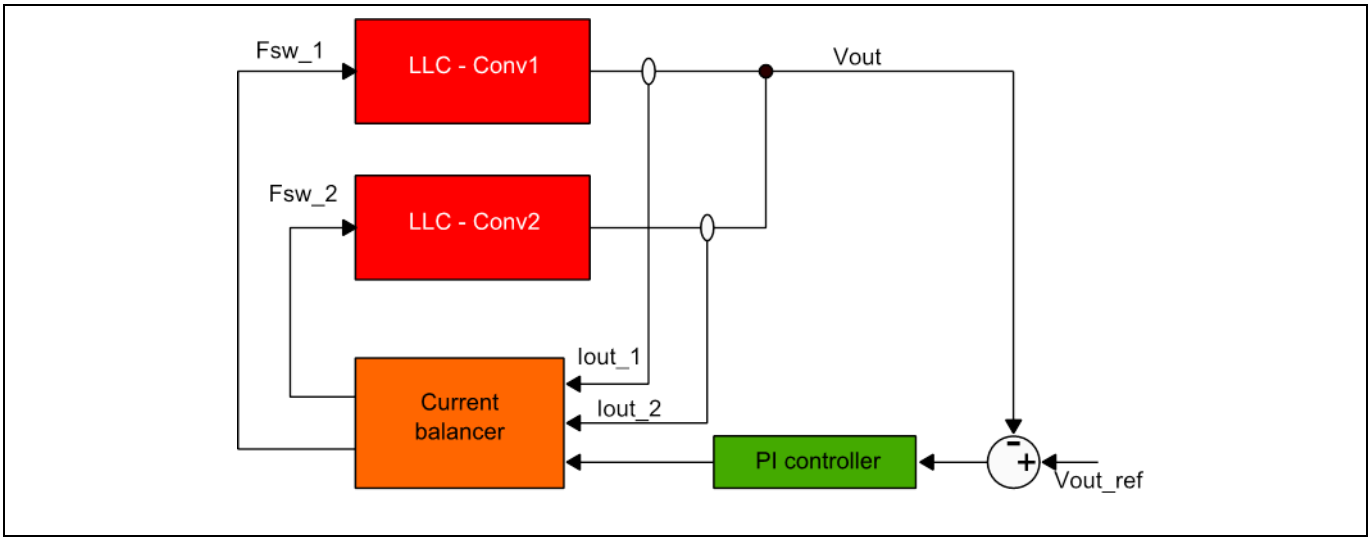


Figure 22 Block diagram of the current sharing and phase shedding functionalities.

The current balancer uses this information to calculate the switching frequency of both LLC converters considering not only the output voltage regulation but also a maximum current difference of 5 A between the phases. The balance mechanism is based on an intermediate variable which is modified in an iterative manner tracking the frequency calculated by the PI controller. The step of the iteration depends on the number of active phases as well as how far the balancer variable is from the output of the PI controller. This mechanism runs as a background process and corresponds to the slow control named as efficiency controller in Figure 8.

The previously presented variable to achieve the current balance is slowly modified to guarantee steady-state current sharing and stability. However, different mechanism is required to handle external perturbations with a fast response. The current balancer variable is therefore immediately modified (in the control service routine running at 50 kHz) when one of the following events is detected: current limitation (section 4.4.1), load jump and dump and capacitive mode detection (section 4.3.2). These three mechanisms are included in the block named as dynamic control in Figure 7.

The efficiency controller, inside the current balancer, is also responsible for the phase shedding functionality. In this case, the number of active phases is modified to achieve an efficiency curve as flat as possible. Two different thresholds separated by a certain hysteresis are defined to decide whether the second phase is enabled or disabled. The current thresholds are defined for the total output current and change accordingly to the output voltage target, as shown in Figure 23.

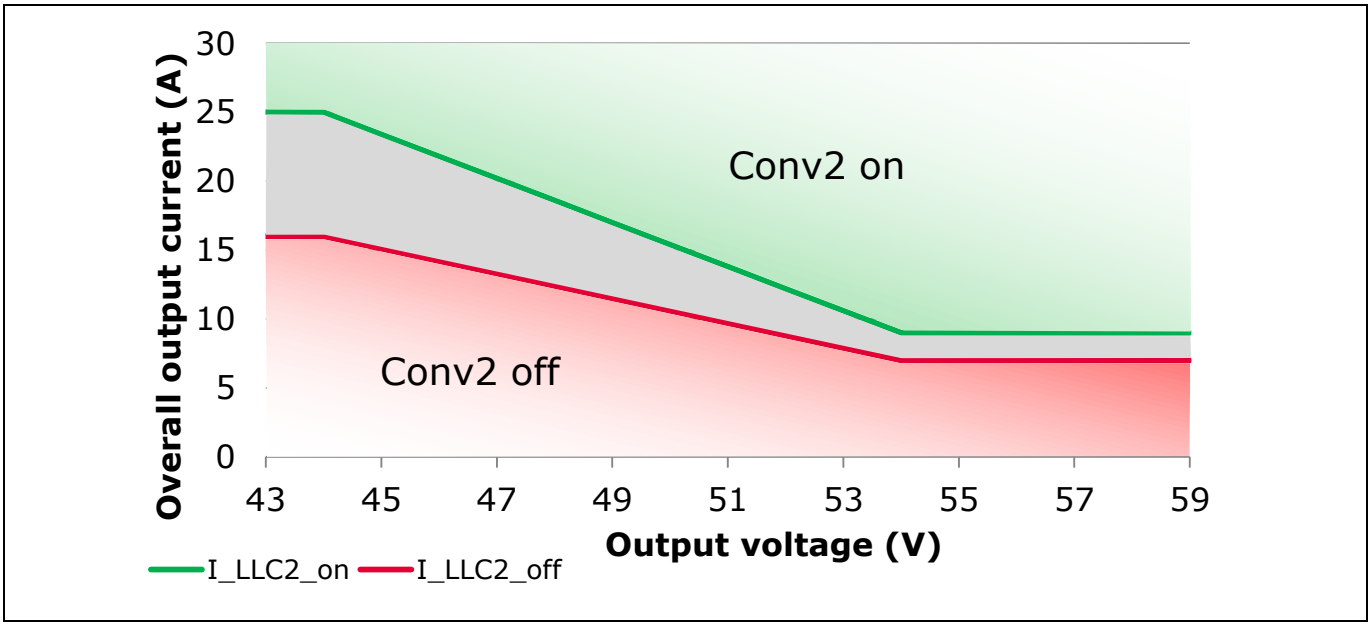
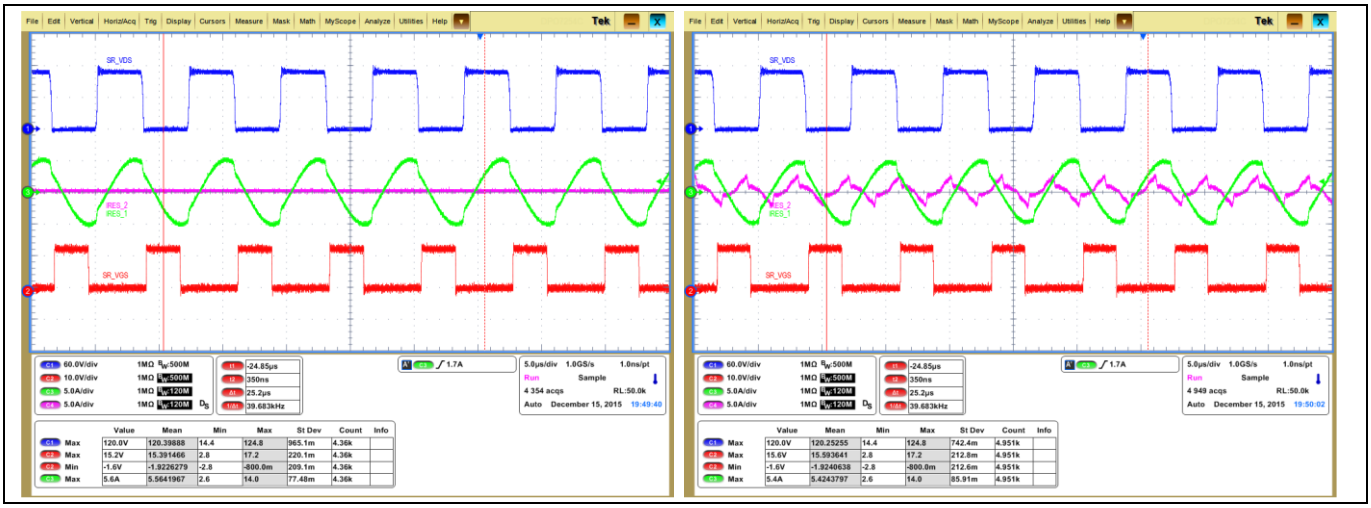


Figure 23 LLC Conv2 shedding depends on overall output current thresholds for a given target voltage.

The presented current levels are applied in steady-state operation of the converter. A third threshold is implemented in order to enable Conv2 as soon as a positive load jump is detected, thus providing an adequate transient response. The enabling of Conv2 for an output voltage of 54 V, when a smooth load transition across the defined on-threshold is applied is shown in Figure 24. As it can be seen the applied load change is small to change the phase 1 switching frequency but enough to start the operation of phase 2, which is appreciated in the change of its resonant current.

It must be noted that the second stage operates only in the case that the first phase is active. In case that Conv1 is turned off, e. g. in burst mode operation, Conv2 is automatically disabled and later enabled according to the presented current levels.



a) b)

Figure 24 Resonant current of phase 2 (purple) for single phase operation (a) and when phase 2 is enabled (b) after the current threshold is reached.

4.3 Hard-commutation prevention and capacitive mode detection

As presented in section 2.2, reliability is a main concern in SMPS. In LLC converters, hard conmutation is a tipicall failure mechanism under certain operating conditions. The dual LLC presented in this document implements two mechanisms to avoid hard-conmutation and capacitive mode operation respectively, as it was briefly introduced above. This section introduces the concept as well as the microcontroller implementation for both mechanisms.

4.3.1 Hard-commutation prevention

In order to avoid hard-conmutation during start-up, or during resuming operation in burst mode operation, an especial sequence is implemented for both phases of the 3 kW dual LLC converter. The applied sequence is divided in four phases as depicted in Figure 25, which will be explained in more detail in this section:

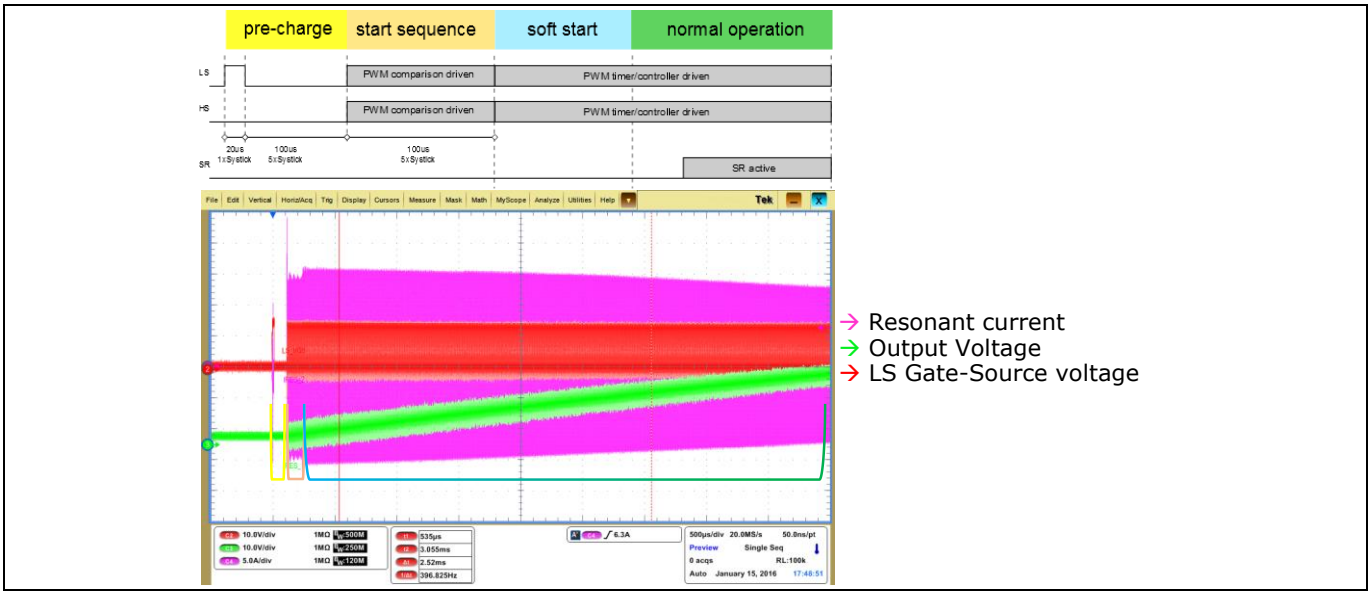


Figure 25 Converter start-up with the applied four-phase sequence.

1. Pre-charge: the aim of this phase is to charge the driver bootstrap capacitor to apply the proper PWM sequence afterwards. Therefore, before starting the converter a long pulse of 20 µs is applied to the LS switch while the HS is keept off (A). Afterwards both switches are off for 100 µs (B). In this phase the SR are kept off. Figure 26 shows a scope capture of this phase during Conv1 start-up, together with the first pulses of the next phase in the applied sequence.

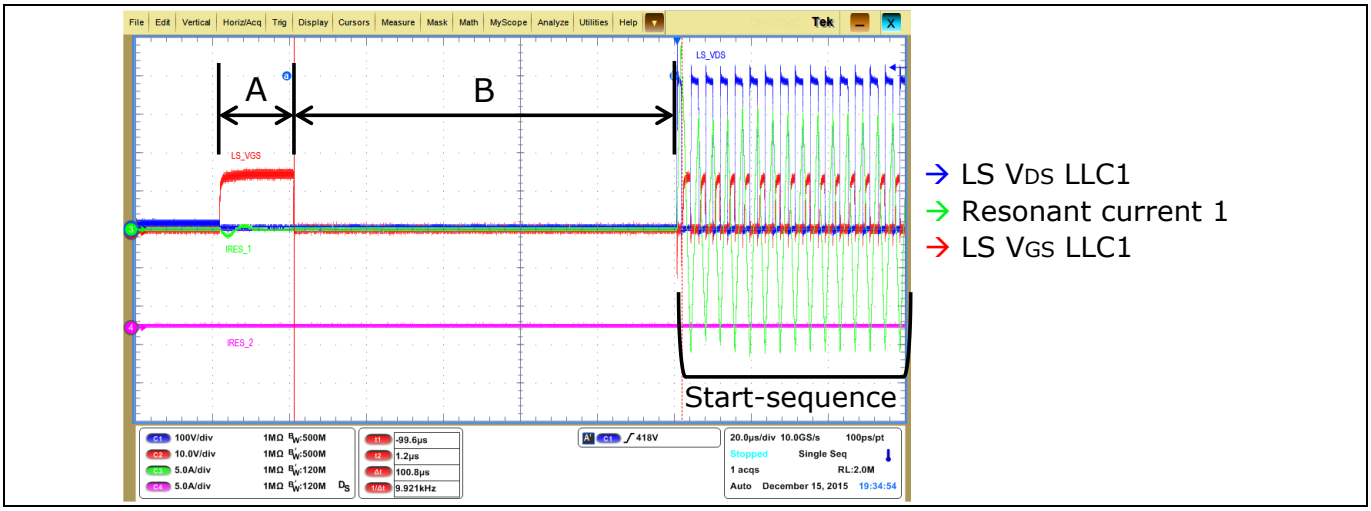


Figure 26 Pre-charge phase scope capture [Ch1=LS_Vds$_1$; Ch2=LS_Vgs$_1$; Ch3=Ires$_1$; Ch4=Ires2].

2. Start-sequence: with the driver bootstrap capacitor properly charged, the converter operation can be started as shown in Figure 24. In order to avoid hard-conmutation during the first cycles of the converter start-up, the PWM is driven by the comparison of the resonant current with zero. This allows delaying the change between LS and HS (and viceversa) after the current zero crossing. As a consequence the change in the current polarity is guaranteed and hard-conmutation avoided as presented in Figure 25. This phase is applied for 100 µs and the SR switches are kept off.
3.
4.

5.
6.

Figure 27 LS-HS driving signal change is applied with a delay after the resonant current crosses zero to guarrante current polarity change and avoid hard-conmutation.

1) and 4) Soft start and normal operation. During the previous phase the time between two consecutive crosses of zero is captured cycle by cycle using a CCU4 unit in capture mode. The adquired time is used as the period of another timer, thus generating a timer replica. After the 100 µs comparison driven phase the timer replica is used to drive the PWM, thus a smooth transition is guaranteed (Figure 28). At this same moment the output voltage is sensed and ramped to achieve the target voltage (soft start).

When the target voltage is achieved (normal operation) the SR are managed according to certain conditions, which will be presented in a different section.

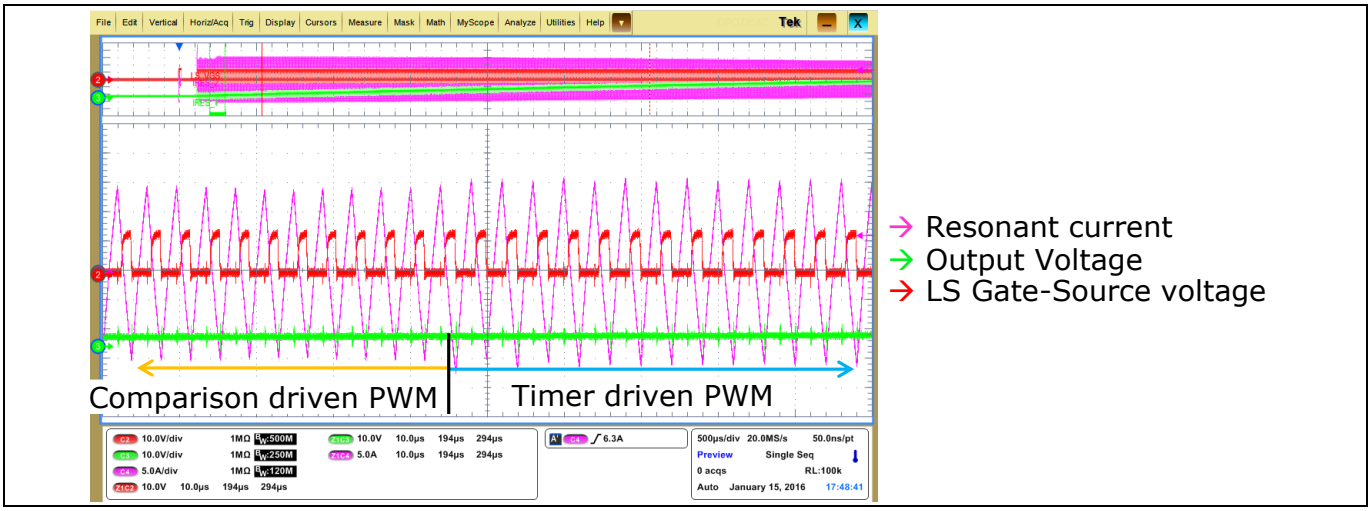


Figure 28 Smooth transition between comparison driven and timer driven PWM operation due to the implemented timer replica.

4.3.2 Capacitive mode detection and prevention

In capacitive load mode operation the resonant current leads the voltage in the mid-point of the half-bridge. Therefore, the operation in this mode, or the tendency to move from inductive to capacitive mode, can be monitored by knowing the phase difference between the mentioned current and voltage.

In the presented design, for each converter, this phase information is obtained by capturing the time between the PWM output edge and the corresponding zero crossing detection of the resonant current (Figure 29). In order to increase the robustness of the implementation, the previous PWM edge to the selected zero crossing is used for the time captured as shown in Figure 27. This modifaction allows to measure negative phase for fast capacitive mode detection. With the captured time information, the actual phase difference can be calculated by SW since the switching period is known.

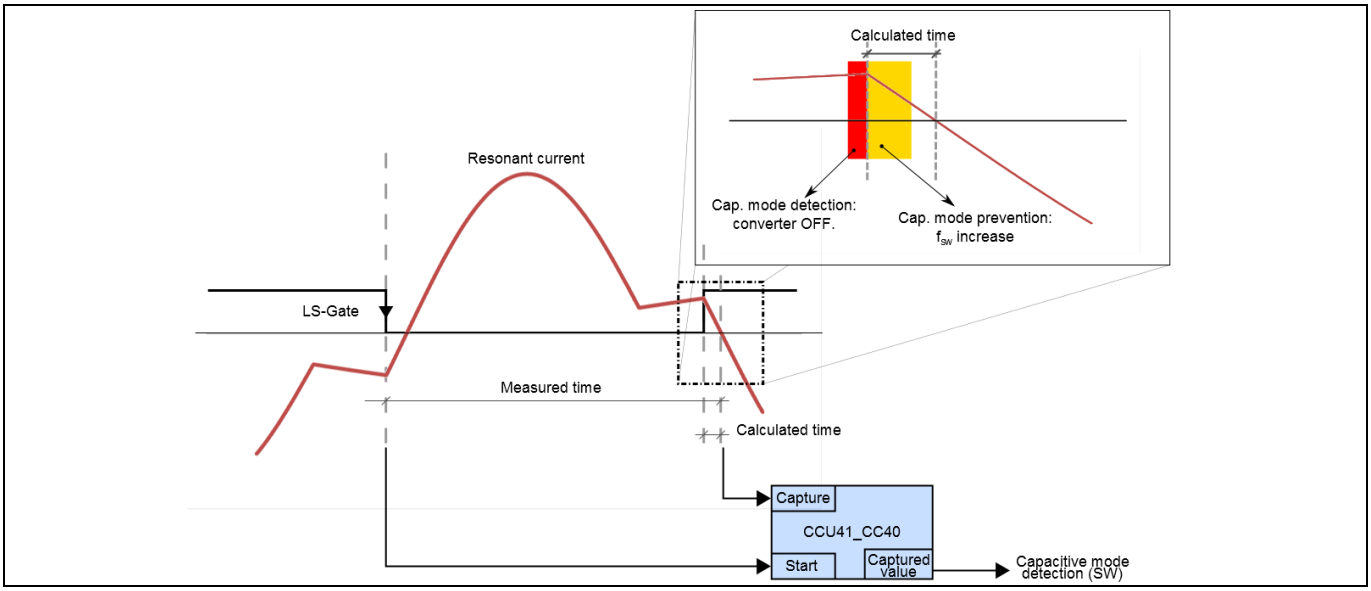


Figure 29 CCU4 timer in capture mode to adquire the phase difference between voltage and current and capacitive mode prevention and detection phase thresholds.

With this phase difference information two different protection mechanisms can be triggered: capacitive mode prevention and capacitive mode detection.

- When the captured phase difference decreases towards zero under a certain defined threshold, the prevention algorithm is activated. This prevention consists of increasing the switching frequency by decreasing the output voltage target. The implemented algorithm can shutdown the converter if, after several successive tries of increasing the switching frequency, the phase difference remains under the defined threshold.
- The second mechanism is named capacitive mode detection. Capacitve mode is detected if the captured threshold is zero or negative for two consecutive sampling periods. As a result of detecting capacitive mode the converter is inmediately turned off. The latching behaviour of the protections can be selected via GUI, as explained later in this document.

4.4 Protections

Two different levels of protections have been implemented in the microcontroller, depending on the variable to be monitored. Those which require fast reaction (linked to the input and output current) are evaluated in the interrupt service routine associated to the control loop. The rest of variables are monitored in the background process with different filter times as explained below.

The latching behavior of the implemented protections can be controlled using the GUI, with the exception of the overtemperature protection that is always latching type. By default the protections are configured to be non-latching and the converter will try to restart 2 s after the fault has been detected.

4.4.1 Over-current-protection

Different limits and algorithms have been implemented for each phase of the dual LLC converter regarding output current (Figure 30). A first limit is set to distinguish between normal operation and overcurrent condition. If the sensed output current is over this threshold, either current limitation or overcurrent protection mechanisms are applied.

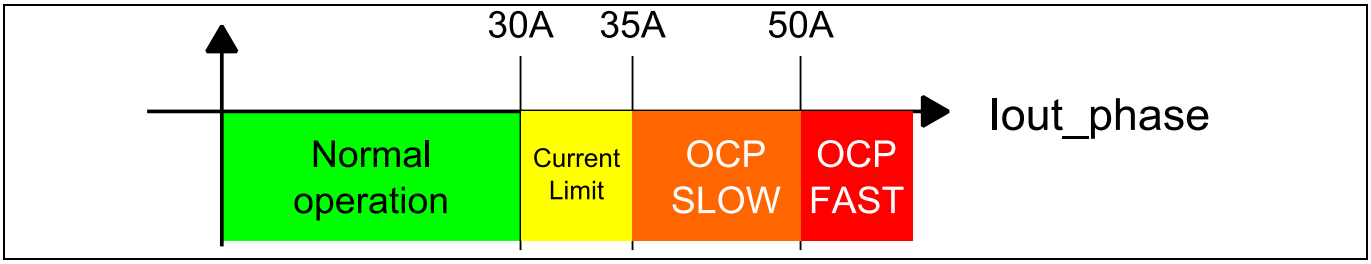


Figure 30 Output current monitoring limits.

For the fastest current protection, OCP FAST in Figure 30, the sensed current is compared with the highest of the defined thresholds (50 A). The comparison is assessed every interrupt cycle (20 µs) and it is active after the soft-start phase of the starting sequence is completed.

A second level of overcurrent protection is defined with an intermediate threshold (35 A). In this case the protection is triggered if the sensed current remains over this value (OCP SLOW in Figure 30) during 40 ms

If the sensed current is not reaching the OCP levels but is over the normal operation range, the current limit mechanism is triggered (Figure 31). Current limitation is applied via the output voltage target reduction, thus limititing the switching frequency. Different scenarios are possible in this situation depending on the number of active phases:

- If only phase 1 is enabled, the current limitation is obviously applied based on the output current of that phase.

- In case both phases are enabled, the output voltage target reduction is applied considering only the output current of phase 2.
- Furthermore, if both phases are active and current over the 30 A threshold is detected in phase 1, the current balance is modified to increase the current provided by phase 2.

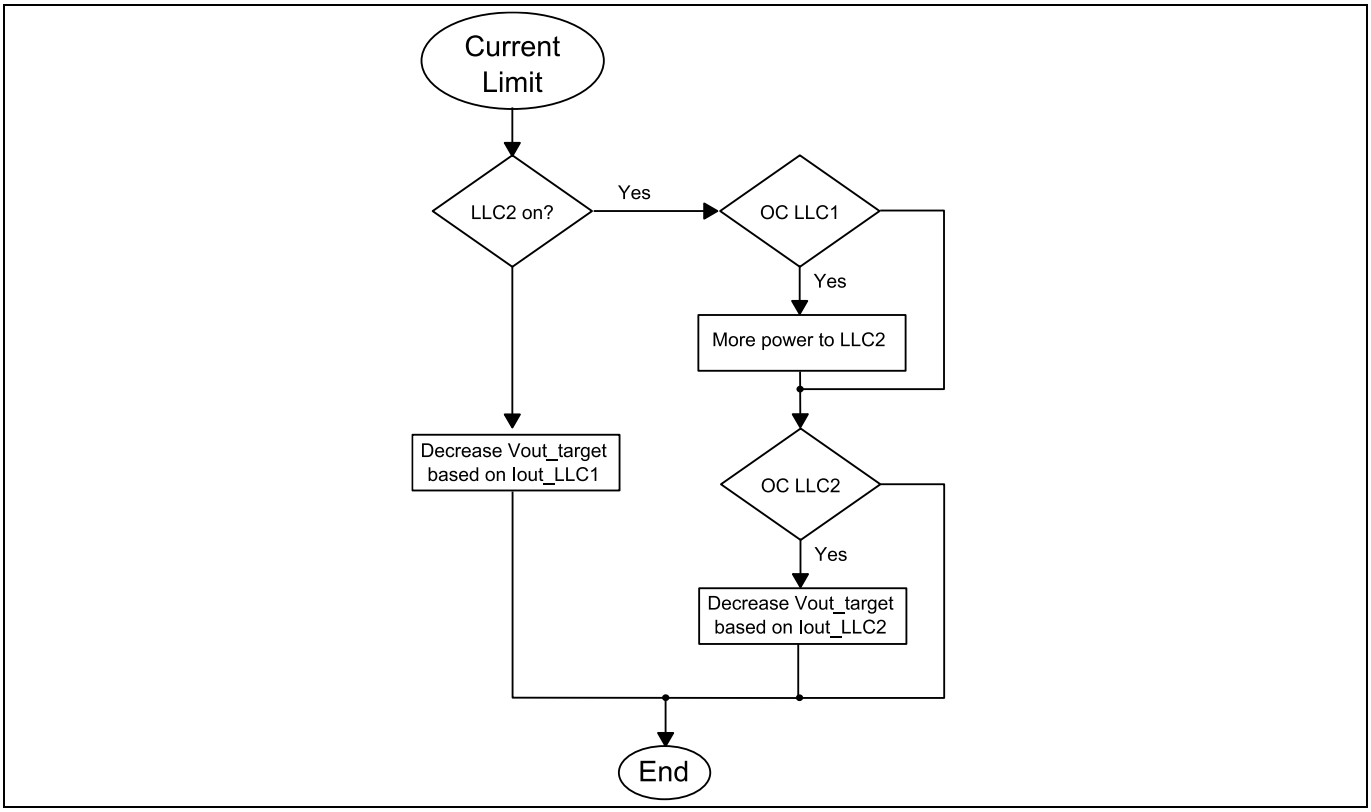


Figure 31 Flow diagram of the current limit algorithm

For any of the previously presented current limitation scenarios, a fault is triggered if the current remains over the lowest threshold (30 A) during 2 s.

Besides the mentioned output current protections, there is an input overcurrent protection based on the resonant current measurement. Unlike the other sensed variables in the system, the resonant current ADC measurement is synchronized with the PWM of each phase (Figure 20). Therefore, accurate information of the resonant current value of each phase is obtained. This information is used to detect either overcurrent or capacitive mode operation, by means of a comparison with a fixed current threshold.

4.4.2 Input and output voltage monitoring

Both input and output voltages are constantly monitored during operation of the dual LLC. In the case of the output voltage, a fault is set when the sensed and filtered value is above a defined level. This limit can be configured using the GUI and is set to 62 V by default. Setting the fault implies that the converter turns off. The resume of operation depends of the selected latching behavior in the user interface, as explained previously.

Regarding the input voltage, both upper and lower limits are defined. If the filtered sensed input voltage is outside the defined range the converter remains off. However, the converter is not latched and the operation is resumed when the input voltage is inside the range. The minimum and maximum limits for this protection are fixed to 345 V and 415 V respectively, and cannot be modified via the user interface.

4.4.3 Other protections

A part from the current and voltage protections for both input and output variables, other protections have been implemented in the presented converter.

Using the output voltage and output current measurements, the output power of each converter can be calculated. If the total output power is higher than a defined threshold, a fault is triggered and the converter is turned off. The limit cannot be modified and it is by default set to 3.2 kW. The same fault is reported in the user interface if the current limitation algorithm is not able to reduce the output current after 2 s.

An open loop operation protection has been as well implemented in the dual LLC converter. In open loop operation, the output voltage feedback is lost and the controller will try to increase the output voltage by reducing the switching frequency. Therefore, this condition is detected if both phases are operating at minimum frequency for 1 ms, triggering the corresponfing fault.

The last of the protections implemented is temperature protection for each phase of the converter. The temperature of each phase is sensed using NTCs coupled to the main transformer and this information is fed to the microcontroller. According to the sensed temperature the fan is turned on (over 45°) and off (under 35°). Furthermore, a protection is triggered if the sensed temperature is over 80°. This protection is always latching type and it cannot be modified using the GUI, thus a power reset of the converter is required.

4.5 Burst mode and SR management

In very light load or no load condition, burst mode is a common choice to keep ZVS operation and solve regulation problems [8]. In the presented implementation, burst mode operation is triggered according to the output voltage level and the frequency of operation. An overvoltage of 750 mV will start burst mode operation if the converter is operating at maximum frequency. Furthermore, if a 2.5 V overvoltage is detected, regardless the switching frequency, the converter is turned off and burst mode operation is started. The following table summarizes the conditions that trigger burst mode operation.

Table 2 Burst mode trigger conditions in the 3 kW dual LLC converter.

Overvoltage	Swtiching frequency	Burst mode
> 750mV	max. freq.	YES
	< max. freq.	NO
> 2.5V	Not considered	YES

Figure 30.a shows the primary side waveforms of Conv1 during burst mode operation. It must be noted that burst mode operation is triggered in light load operation and only Conv1 is enabled. The converter operation is resumed during burst mode when the output voltage target is reached again. In this condition, the starting sequence presented in section 4.3.1 is implemented to avoid hard conmutation, as shown in Figure 32.b.

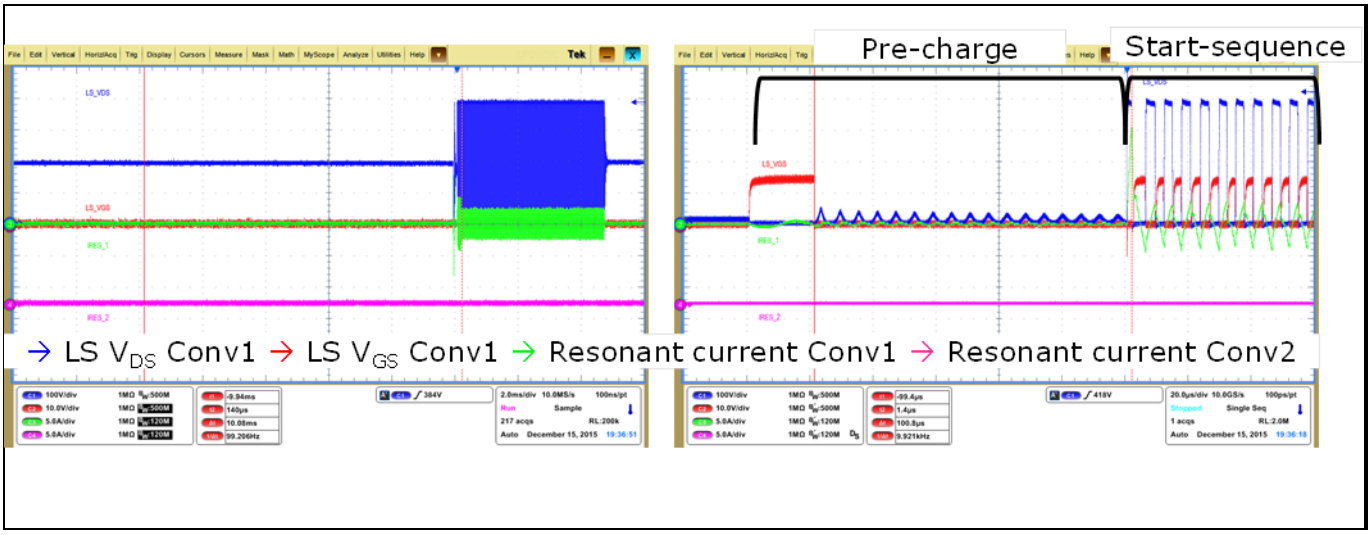


Figure 32 Burst mode operation of the dual-phase LLC converter (a) and detail of the starting sequence during burst mode (b)

The SR management is applied to both phases independently. If burst mode operation is triggered the synchronuous rectifiers (SR) are turned off to avoid reverse power flow and possible capacitive mode operation. Furthermore, SR switches are turned off for the same reason if a load jump is detected, as it was mentioned in section 2.2. These conditions together with steady-state operating conditions to disable the SR switches are summarized in the following tables.

Table 3 Synchronous rectifiers off conditions

OFF conditions	
OR	Iout_phase < 4A
	I resonant > 9.25A
	Vout < 42V
	Load change > 8A
Burst mode	

Previously the off conditions were presented. On the other hand, SR switches for each phase are allowed to be turned according to the conditions presented in. When the SR is enabled a soft-start of their on-time is applied in order to allow a smooth gain transition in the converter operation.

Table 4 Synchronous rectifiers on conditions

SR ON conditions	
AND	Iout_phase > 4.5A
	I resonant < 9A
	Vout > 43V
	Load change < 8A

4.6 Adaptive dead time

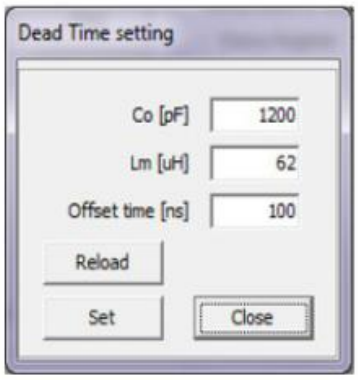
In order to keep proper ZVS operation for different load and line conditions, a variable dead time between the driving signals of the half- bridge is necessary. For a given design (Lm) and a given switch (time related C_{oss}) the necessary dead time for a specific operation frequency can be calculated based on the following equation.

$$t_{DT}[ns] = DT_offset + 2 \cdot \sqrt{2} \cdot \pi^2 \cdot C_{oss} \cdot L_m \cdot f_{sw}$$

This equation is implemented in the dual HB LLC software. Therefore, the proper dead time for the operating switching frequency of each phase is calculated. This calculation is done every control interrupt cycle (20 µs), according to the new calculated switching frequency.

The required parameters can be provided trough the graphical user interface. Figure 33 shows the window of the GUI where the necessary parameters for the dead time calculation can be provided. As an example of the required capacitance value, the time related output capacitance of two CoolMOS™ transitors extracted from the datasheet available online are presented. If different CoolMOS™ transistors from different generations are used, it might be necessary a fine adjustment of the deadtime. Therefore, a variable offset can be modified using the GUI for better adjustment.

The high-resolution PWM peripheral included in XMC™ (HRPWM) allows a safe modification of the dead time during operation. This safe update is possible due to the shadow transfer mechanism for the dead time included in the high-resolution channel of the HRPWM [14].



IPW60R041P6:	Effective output capacitance, time related [2]	$C_{o(tr)}$	-	1200	-	pF
IPW60R040C7:	Effective output capacitance, time related[2]	$C_{o(tr)}$	-	1640	-	pF

Figure 33 GUI window to provide the necessary parameters for adaptive dead time calculation and C_o for IPW60R041P6 and IPW60R040C7 CoolMOS™ transistors extracted from the datasheet

4.7 Loop compensation parameters

As introduced in section 2.3, the total amount of output capacitor in the PSU is affected by the total capacitance present outside the unit. The total amount of capacitance seen by the PSU influences the loop stability and therefore, the response of the unit to load and line jumps as well as any other external perturbance. Through the user interface developed for this dual-phase LLC converter, three different capacitors can be selected according to the output capacitor mounted by the user.

The three selectable capacitor values (4 mF, 6 mF and 8 mF) correspond to three set of integral and proportional gains for the implemented PI controller in the voltage loop. The adequate set of integral and

proportional gains is selected before the converter starts in accordance with the selected output capacitor in the user interface.

4.8 Graphical User Interface (GUI)

The GUI is a key part of our design concept, with the goal to allow some interactions of the engineers with the 3 kW dual-phase LLC during their evaluation on the bench. The main features of it have been already introduced and motivated in the section 2.3.

The physical aspect of the GUI is shown in the next page: 4 main blocks can be recognized inside:

- Setting and control: set the desired values for electrical parameters, converter operation and protections
- Measured values: measurement most relevant voltages, currents and temperatures
- Status register: short description of the converters operating condition
- Faul register: flags showing the type of detected malfunction in case of forced shut down

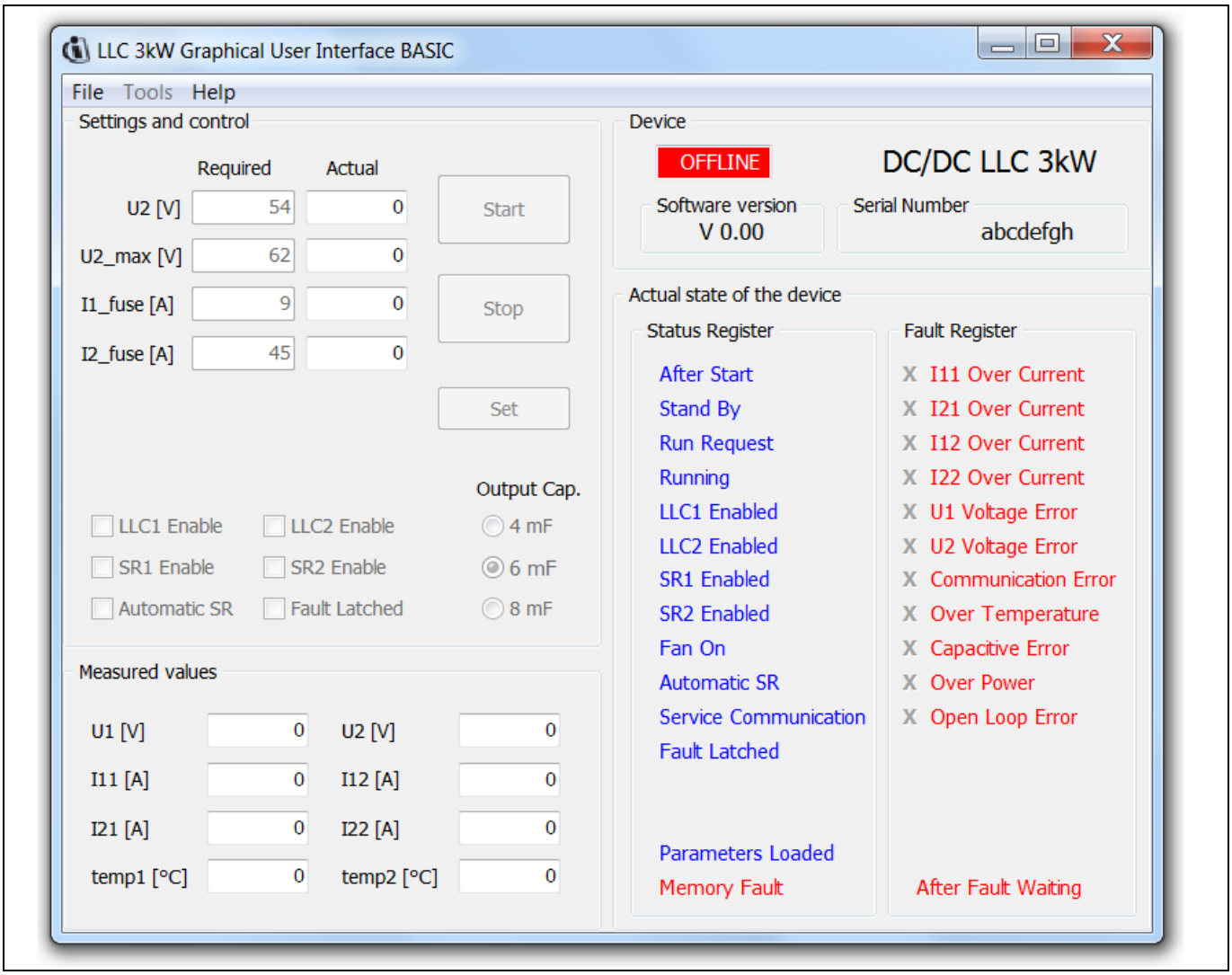


Figure 34 Graphical User Interface

The benefits are evident: the GUI is an intuitive and user-friendly tool, allowing even changing the mode of operation of the converter without need of modifying any line of the code. On the top of it, it provides in real time info about the status of the board, assuring a very constant monitoring of it, including the case of shut down due to the triggering of some protections.

Digital control features

For an introduction to the graphical user interface click on the following slide and find the “getting started sequence” presentation online.

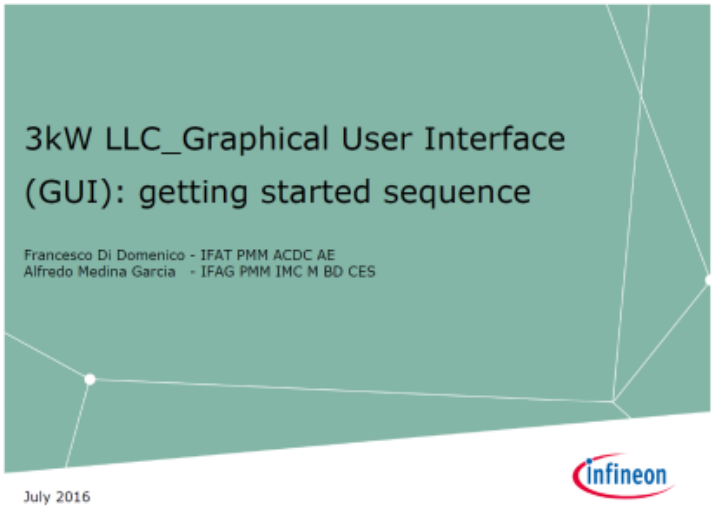


Figure 35 3 kW LLC Graphical User Interface – getting started sequence (link)

5 Performance evaluation

The present chapter provides an overview on the general operation and perfomance of the 3 kW dual-phase LLC.

The described results have been achieved using on the primary side of both phases the 600 V CoolMOS™ C7 in TO-247 package (IPW60R180C7). All these results remain valid also in case the TO-220 package is used.

5.1 Waveforms captured in significant operation modes

The following Figures show some of the most significant operation modes of the 3 kW dual-phase LLC.

Figures 36-38 illustrate the shape of the primary resonant tank and the gate and drain voltages measured on the low side (LS) MOSFET of Conv1. The not synchronized switching frequencies of the two converters can be easily noticed from the resonant current waveforms. The reduced peaks on the V_{DS} and V_{GS} are demonstration of the accurate Infineon driving scheme and layout, which are able to get the best performance of the very fast switching 600 V CoolMOS™ C7 technology. Special care must be used in the selection of the gate resistances located in the turn-on and turn-off path of the HB MOSFETs: the choice comes normally from a trade-off between the efficiency target (especially in matter of switching losses) and reliability topics (mostly related to drain-source voltage de-rating guidelines). In our case, the selection of $R_{G,on}$=47 Ω and $R_{G,off}$=1 Ω allows to combine excellent ZVS behavior and reduced switching losses with very limited stress on the device. Bear in mind that the value of these resistances actually has to be selected case by case, according to e.g. the PCB layout or the control applied during start-up sequence or output short circuit protection.

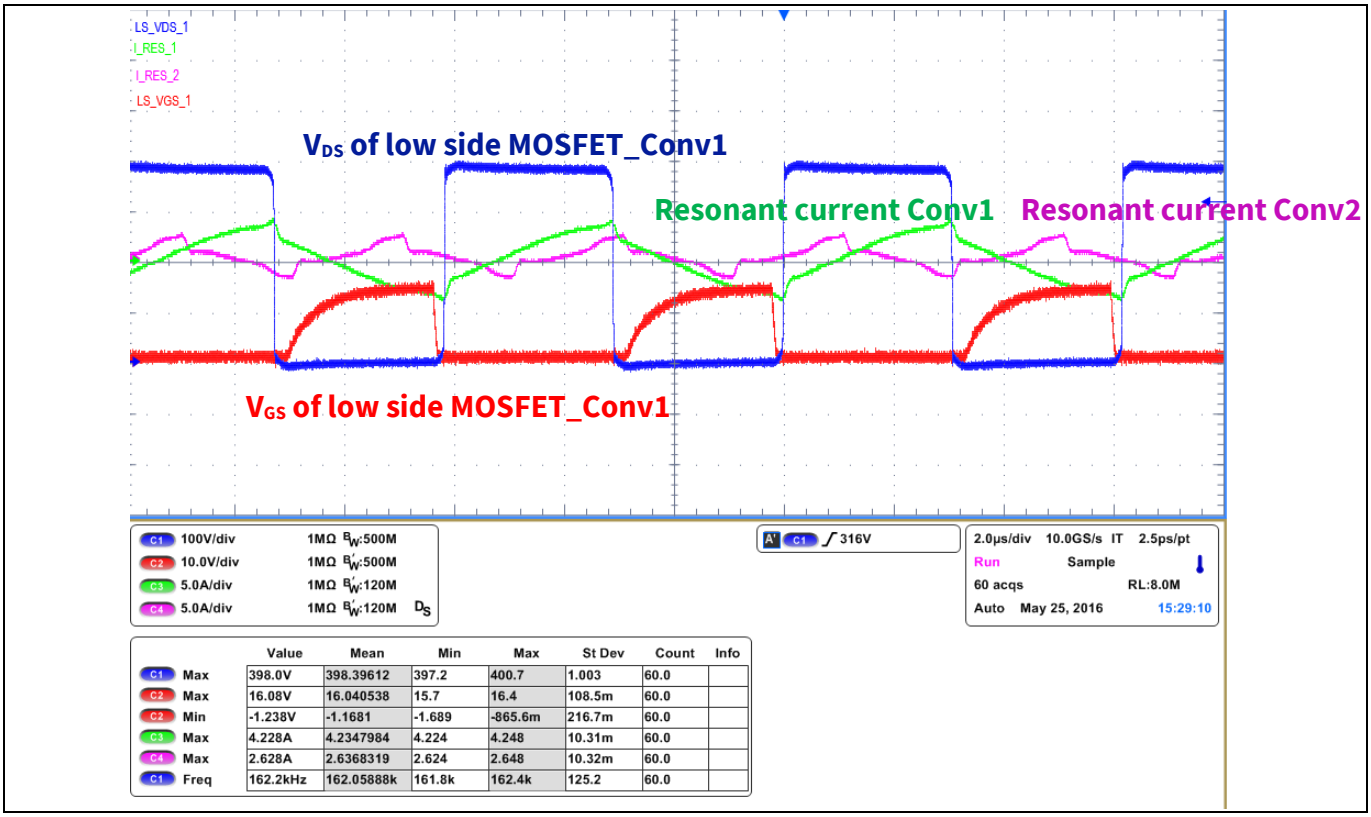
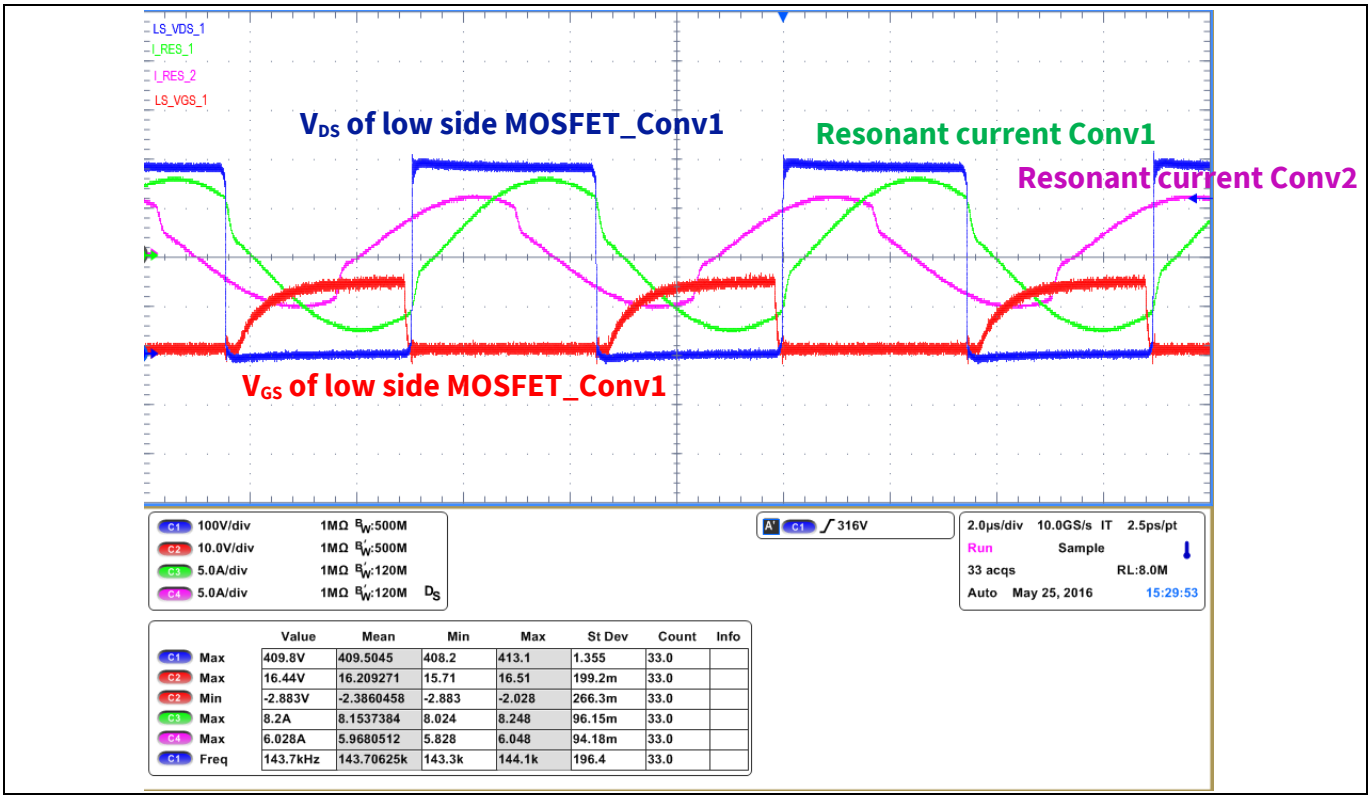
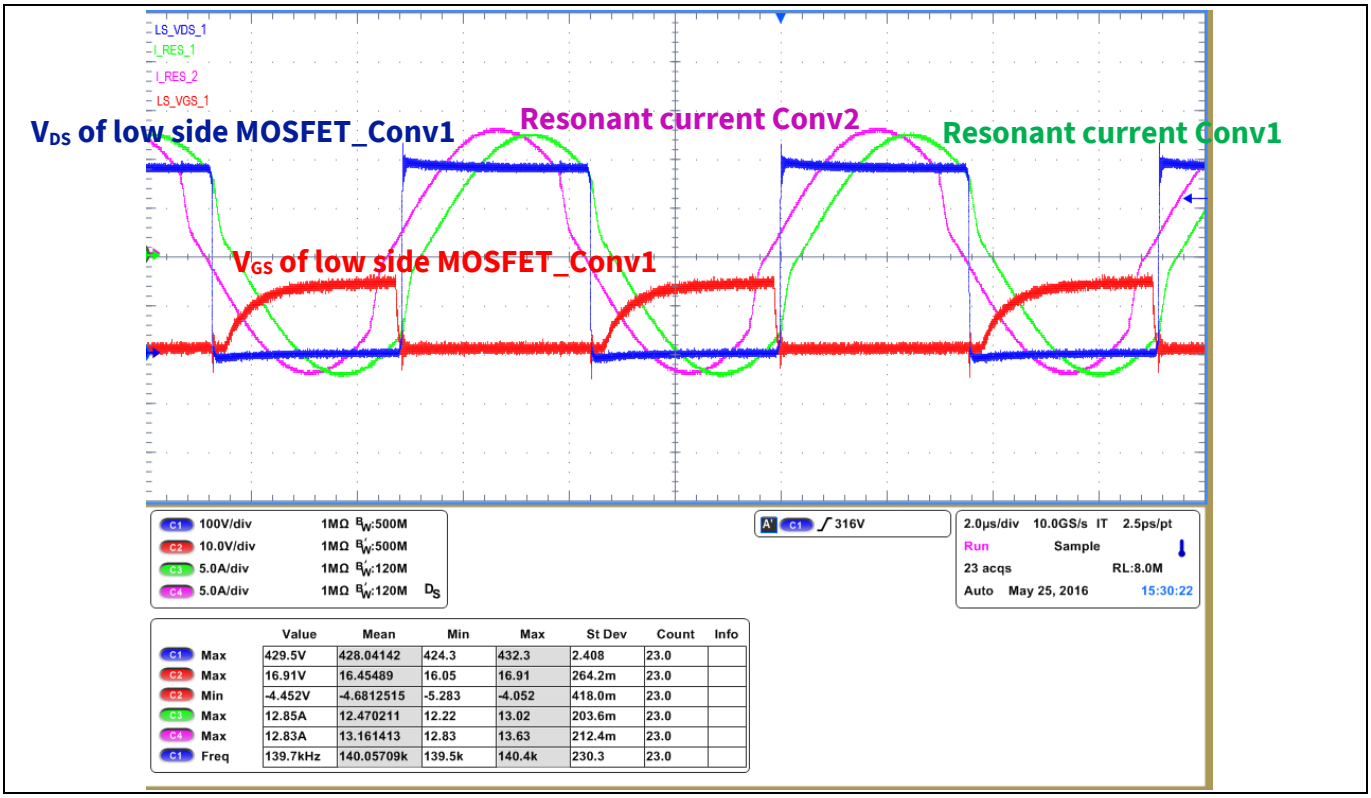


Figure 36 Resonant currents; V_{gs} and V_{ds} on the low side MOSFET (Conv1) at 10% load



	Value	Mean	Min	Max	St Dev	Count	Info
C1 Max	409.8V	409.5045	408.2	413.1	1.355	33.0	
C2 Max	16.44V	16.209271	15.71	16.51	199.2m	33.0	
C2 Min	-2.883V	-2.3860458	-2.883	-2.028	266.3m	33.0	
C3 Max	8.2A	8.1537384	8.024	8.248	96.15m	33.0	
C4 Max	6.028A	5.9680512	5.828	6.048	94.18m	33.0	
C1 Freq	143.7kHz	143.70625k	143.3k	144.1k	196.4	33.0	

Figure 37 Resonant currents; V_{gs} and V_{ds} on the low side MOSFET (Conv1) at 50% load



	Value	Mean	Min	Max	St Dev	Count	Info
C1 Max	429.5V	428.04142	424.3	432.3	2.408	23.0	
C2 Max	16.91V	16.45489	16.05	16.91	264.2m	23.0	
C2 Min	-4.452V	-4.6812515	-5.283	-4.052	418.0m	23.0	
C3 Max	12.85A	12.470211	12.22	13.02	203.6m	23.0	
C4 Max	12.83A	13.161413	12.83	13.63	212.4m	23.0	
C1 Freq	139.7kHz	140.05709k	139.5k	140.4k	230.3	23.0	

Figure 38 Resonant currents; V_{gs} and V_{ds} on the low side MOSFET (Conv1) at 100% load

The following Figures 39-40 are focused on the ZVS behavior, which is achieved already at very light load.

Performance evaluation

You can easily recognize the ZVS achievement from the absence of Miller Plateau in the V_{gs} waveforms, sign that the V_{ds} goes to zero before the device is turned-on. This will obviously minimize the device switching losses, which will be only affecting the turn-off transition, thus contributing to maximize the converters efficiency especially at light load, where the switching losses are predominant.

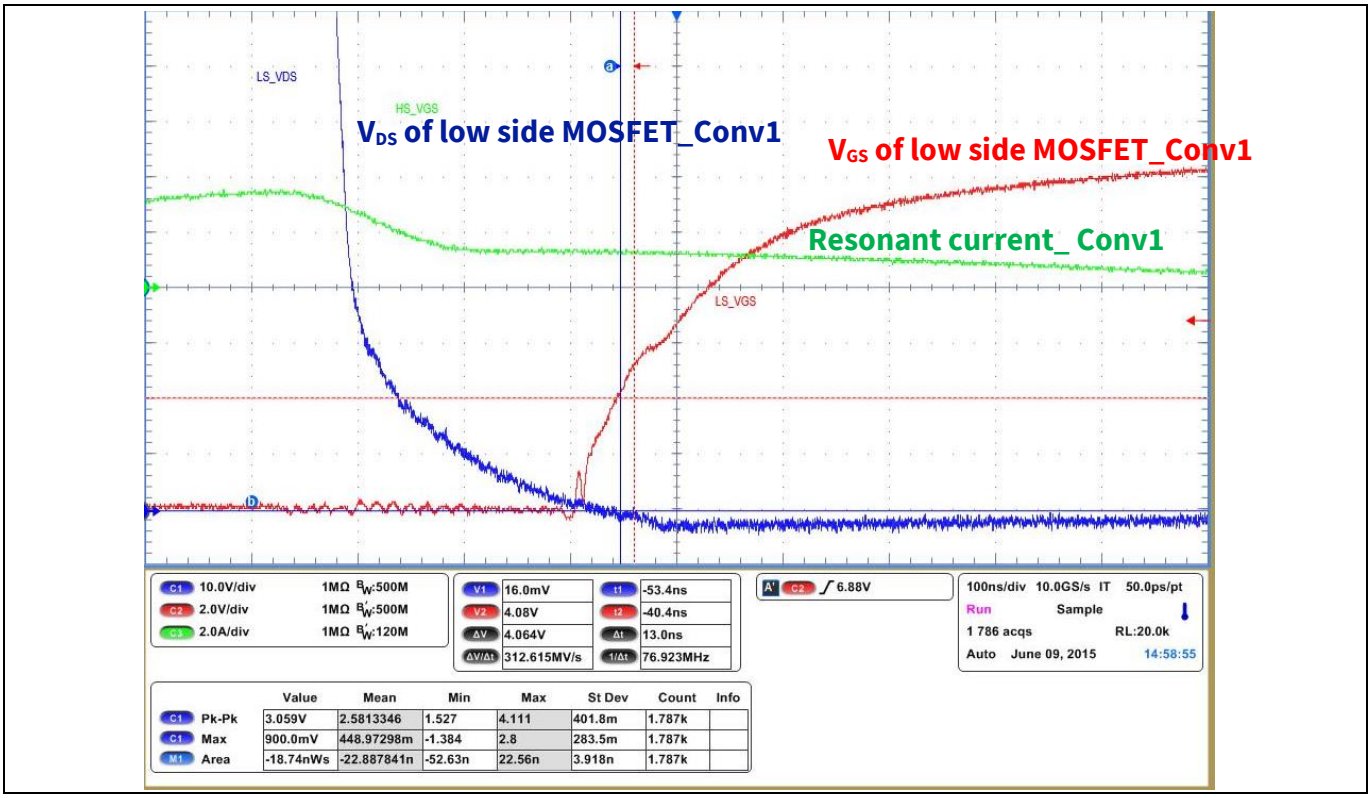


Figure 39 Full ZVS turn-on at only 3% load (90 W) and V_{in}= 380 V_{DC} (Conv1)

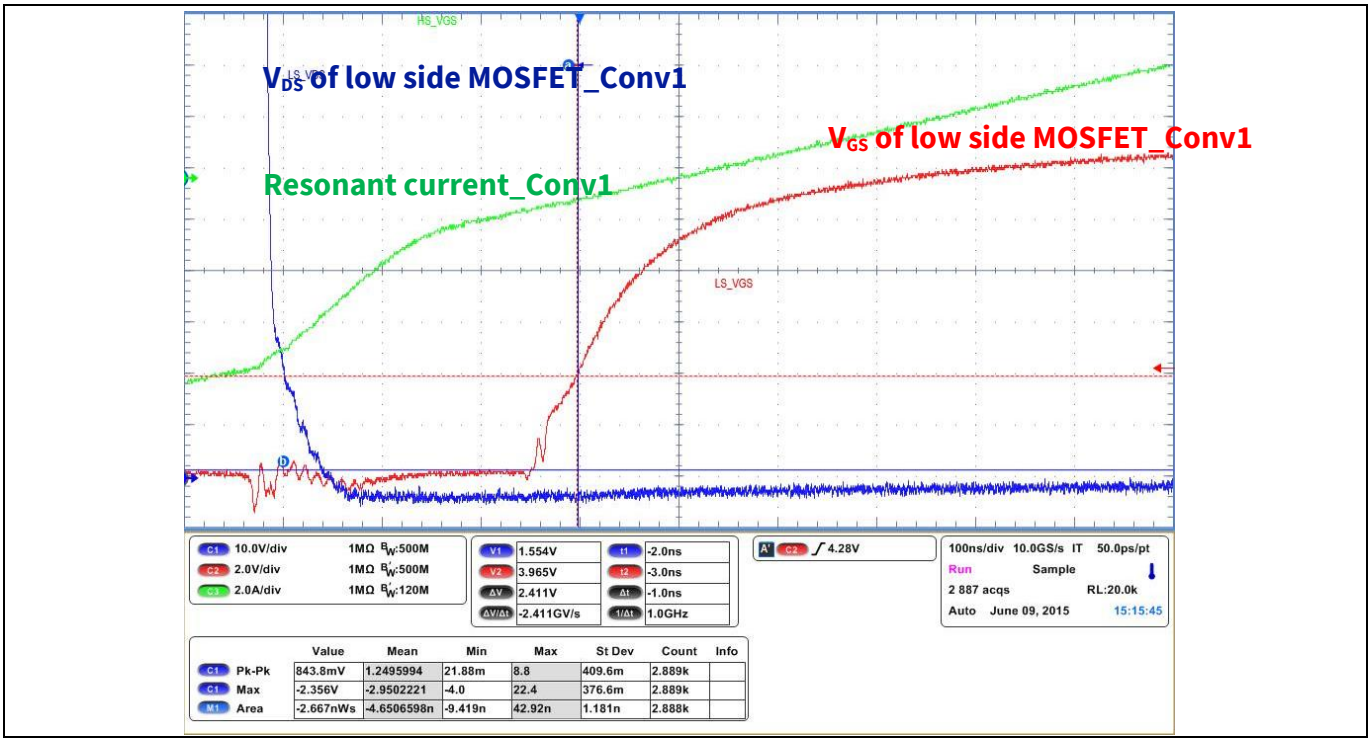


Figure 40 Full ZVS turn-on at Full Load (3000 W) and V_{in}=380 V_{DC} (Conv1)

Performance evaluation

Figures 41-42 show the synchronous rectification operation at 10% and 100% load: the V_{ds} reduced peak measured on the SR MOSFET is the result of an accurate layout and transformer construction, but also linked to the very low Q_{rr} offered by the OptiMOS™ 5 technology.

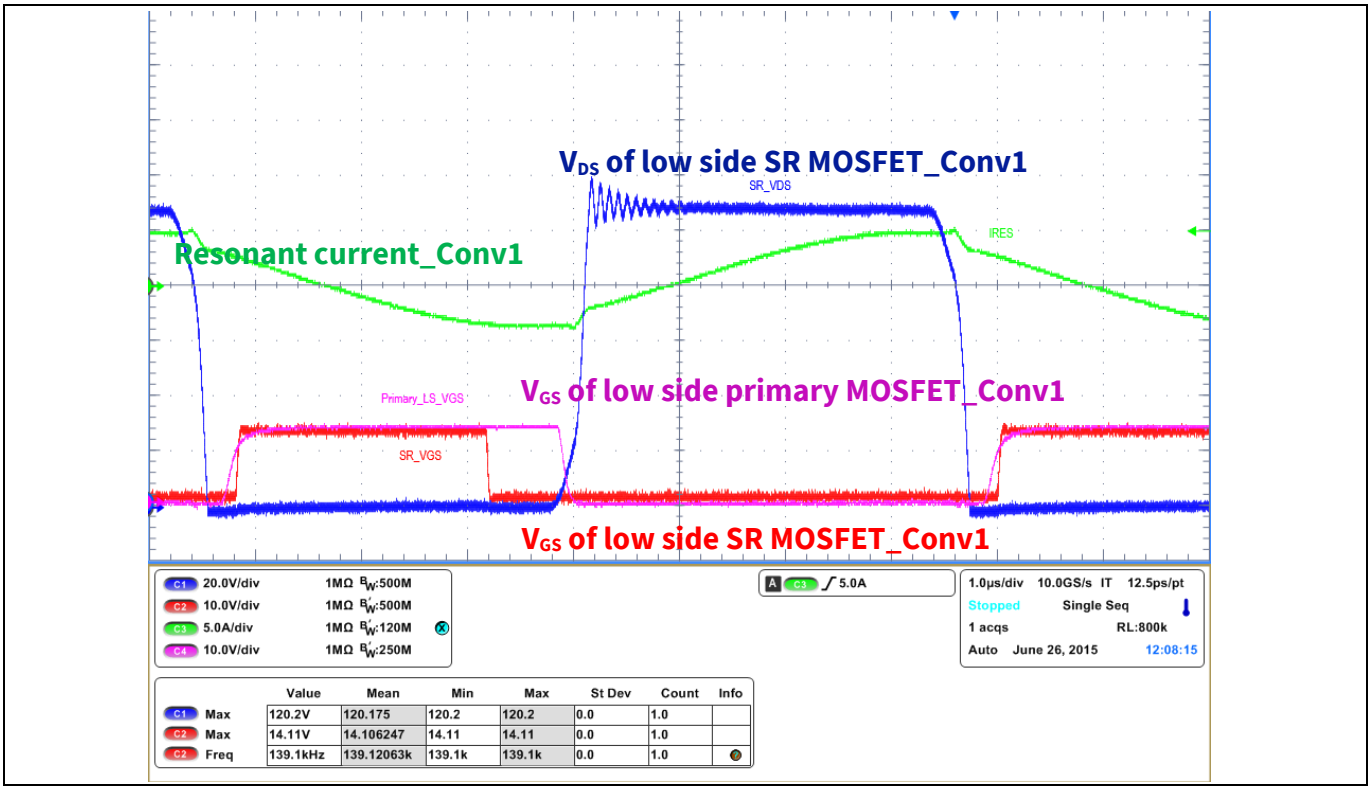


Figure 41 SR MOSFET operation at 10% load and V_{in}= 380 V_{DC} (Conv1)

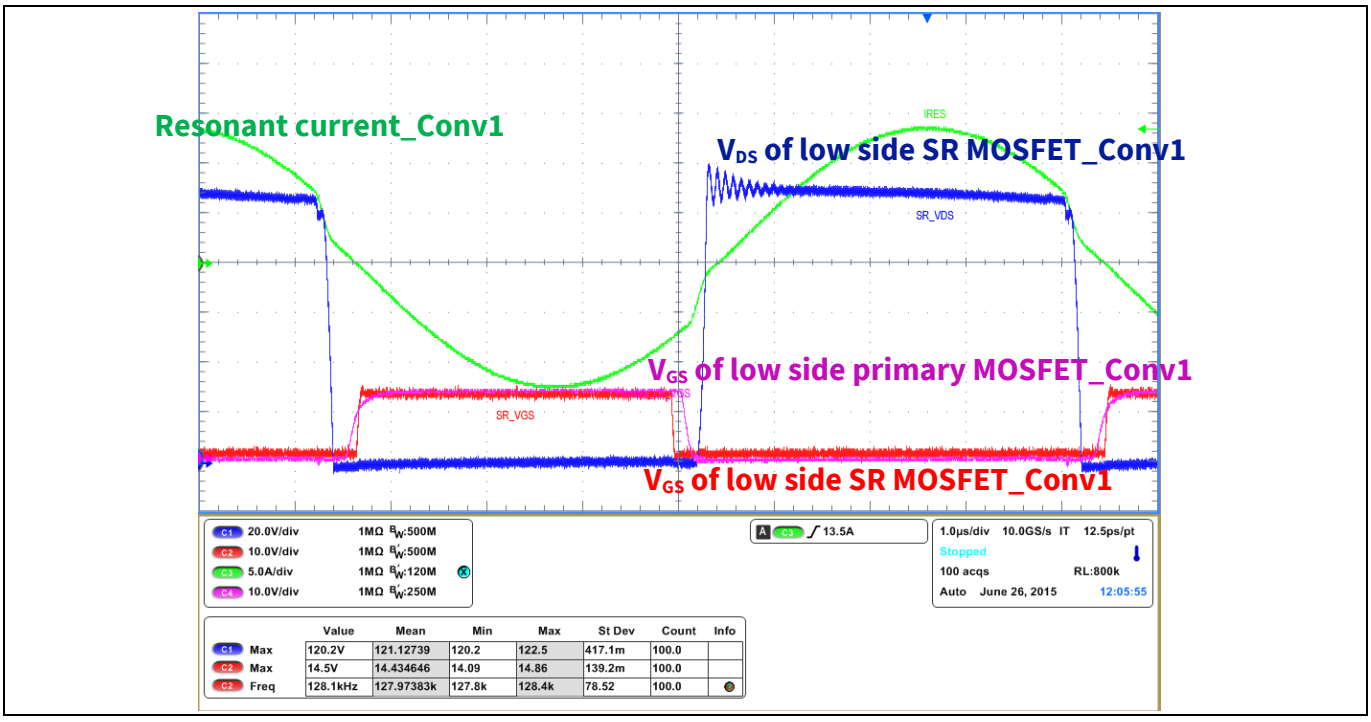


Figure 42 SR MOSFET operation at Full Load and V_{in}= 380 V_{DC} (Conv1)

5.2 Efficiency plot

Figure 43 reports the efficiency plot measured on the 3 kW dual-phase LLC assembled with IPW60R040C7. The fans and BIAS consumption are not included in the presented measurement.

A picture is attached showing the efficiency test bench where all measurements have been performed according to the methods described in [13].

A very flat plot can be observed: in fact the efficiency never goes below 97%, down to 10% load: this is the effect of the phase shedding. Moreover, the efficiency at 100% is not much lower compared to the 50% load, which gives significant benefits from thermal perspective.

For the sake of completeness, it should be stated that including BIAS and fans consumption would generate around 3 W additional losses, which would reduce the efficiency by 1% at 10% load, but only 0.1% at full load.

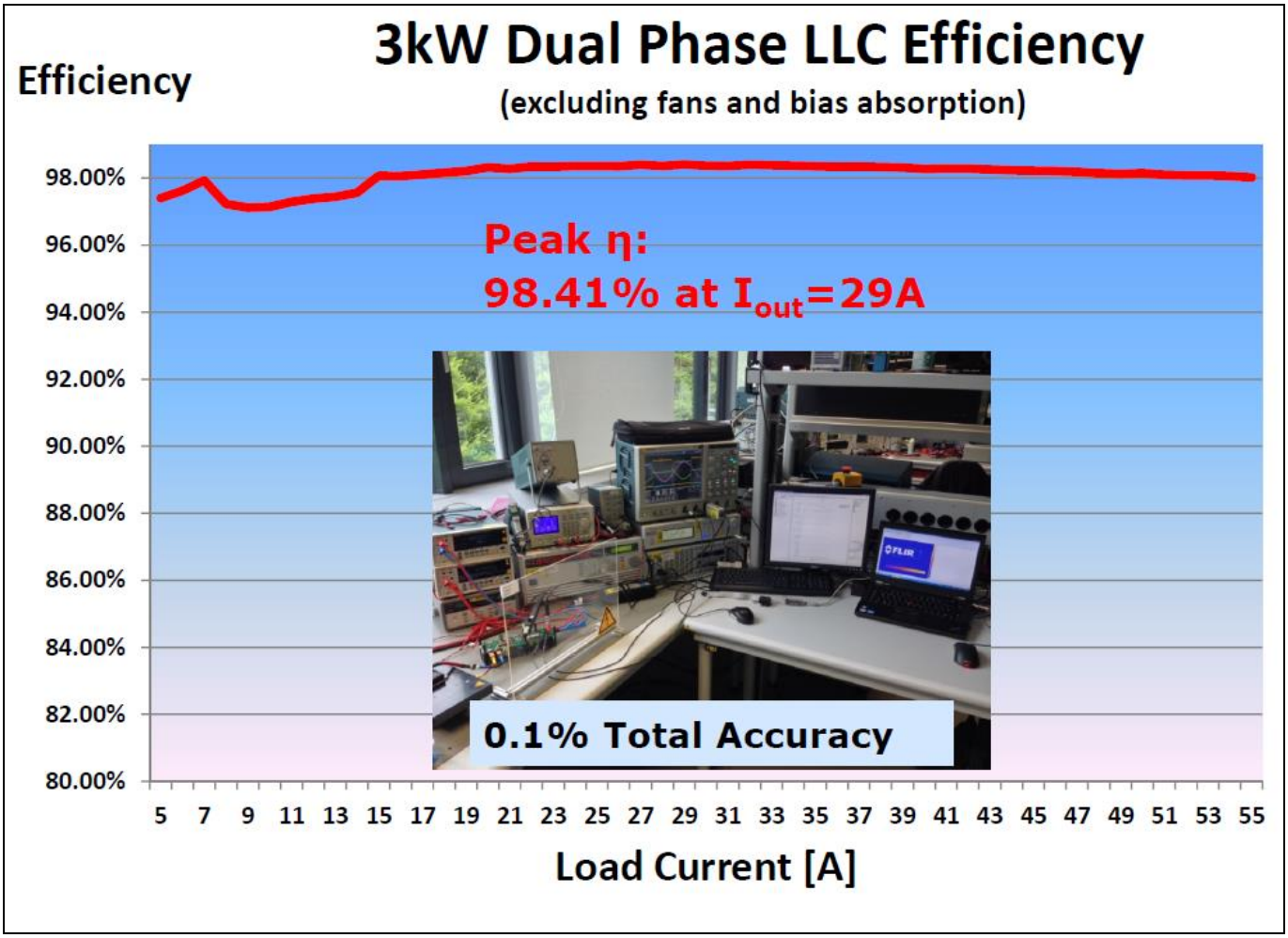


Figure 43 Efficiency versus Load measured with IPW60R040C7 at V_{in}=380V_{DC}

The plot above shows that the performance targets set at the beginning in the technical specification have been completely fulfilled.

In order to highlight the crucial contribution of the 600 V CoolMOS™ C7 MOSFET usage in the two HB LLCs, it is worth to show in Figure 44 another graph including the Δη measured in the same board in comparison with the previous 600 V CoolMOS™ P6 technology and two competitor devices in the same $R_{ds(on)}$ range.

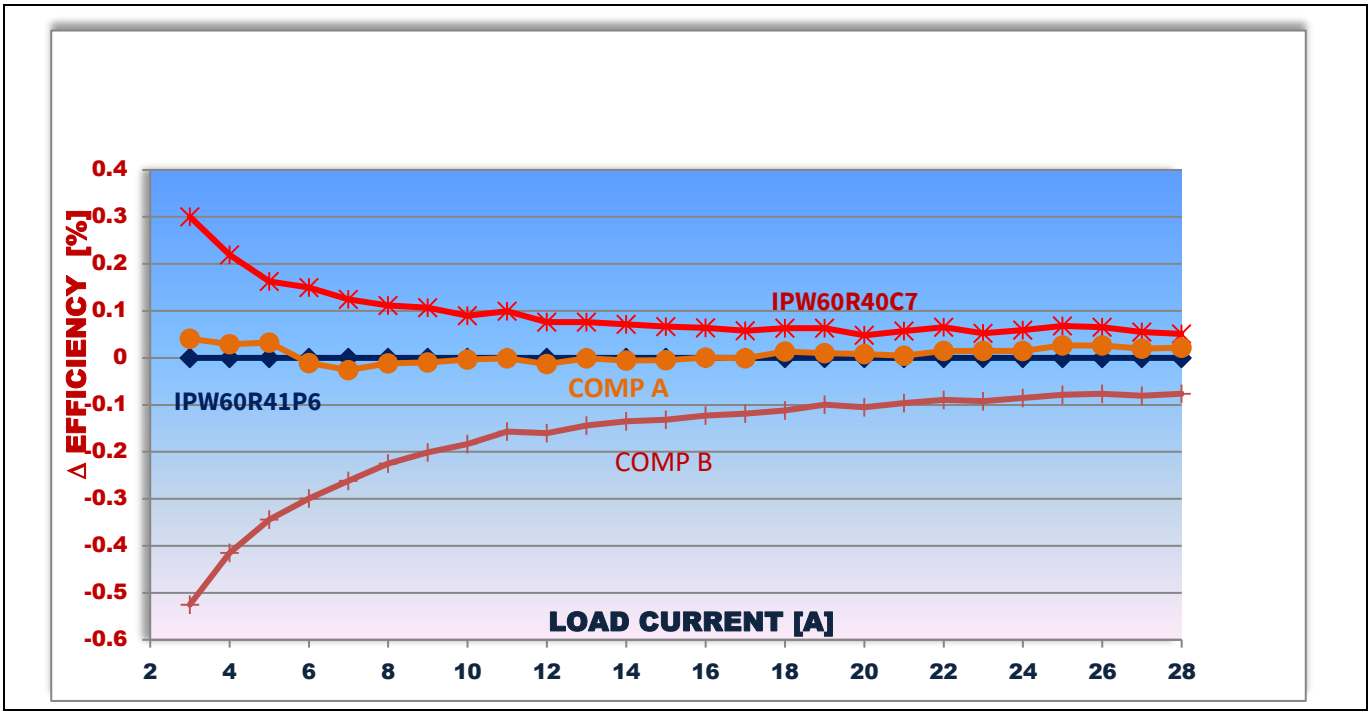


Figure 44 IPW60R040C7 versus IPW60R041P6 versus two competitors in 3 kW dual-phase LLC

The plots have been acquired during operation with only one phase activated (1500 W), in order to increase the measurement accuracy especially at very light load operation. IPW60R040C7 is able to achieve higher efficiency compared to the IPW60R040P6 and the two competitors in the entire load range. A significant improvement is visible in the range 10-20% load, up to 0.3%. This is mainly due to the reduced driving and switching losses, which are predominant in that load range. An improvement is also visible in the range 60-100% load, mostly related to lower typical $R_{ds(on)}$ and switching losses.

The analysis of the operation with only one phase activated triggers some interesting considerations about a possible further improvement in the flatness of the efficiency curve.

The Figure 45 shows in the same graph both the single phase (Conv1, up to 1500 W, red curve) and the dual-phase efficiency plot (up to 3000 W, blue curve).

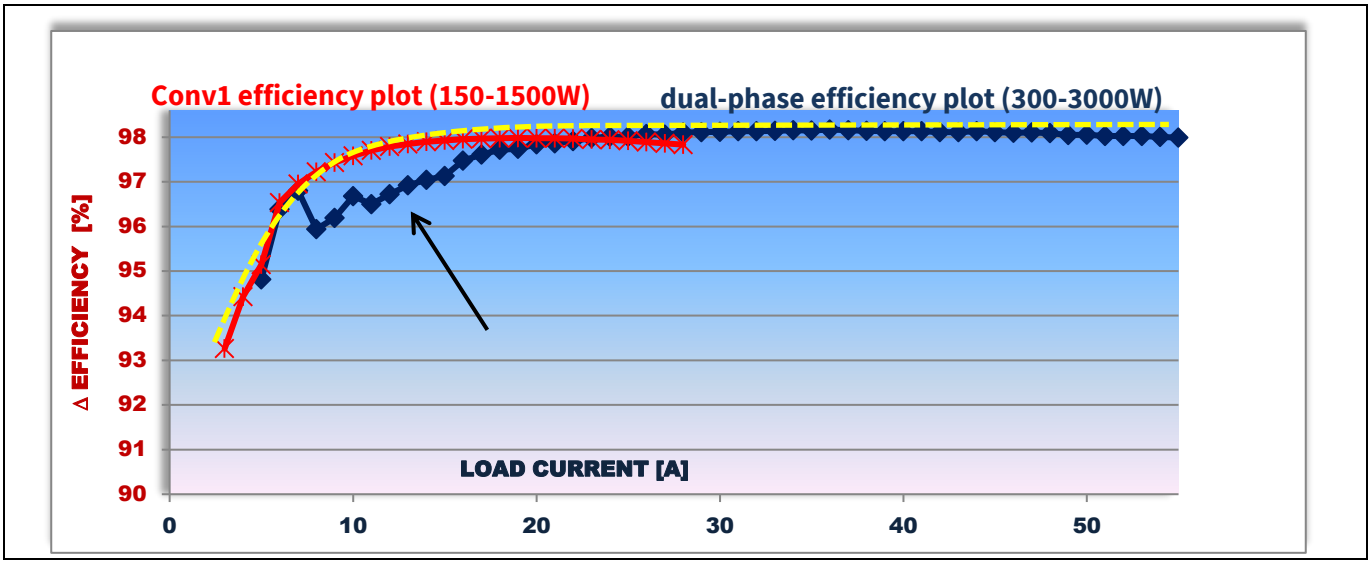


Figure 45 Single versus dual-phase efficency plot comparison

Performance evaluation

The operation of each of the two converters influence the phase shedding, specifically the output current level at which the Conv2 is activated/de-activated. Please refer to the definition of Conv1 and Conv2 as described in the section 4.2 of this document.

In fact the “valley” in the curve highlighted by the arrow in the Figure 45 can be explained as follows: by reducing the output load from 100% to 10% load, at the total output current around 15 A the synchronous rectification MOSFET of Conv2 switch-off, thus inducing the sudden reduction of efficiency in the well visible “valley”. This is due to conduction on the SR MOSFET body diodes.

If the output current is furthermore reduced, below the phase shedding threshold, the Conv2 switches off, then the only Conv1 takes over, thus generating the natural sudden increase of efficiency visible in the plot.

From these considerations, we derive that a possible way of getting even flatter efficiency plot is to switch-off the Conv2 while its synchronous rectification stage is still active. In that way we can minimize the “valley” above mentioned and get a final curve like the dotted yellow one in Figure 45.

The phase shedding is confirmed to be a very important feature allowing to really shaping the efficiency plot, according to the specific converter’s technical specification requirements.

6 Conclusion

The 3 kW dual-phase LLC demo board is the demonstration of how a mix of best-in-class CoolMOS™ and OptiMOS™ power device technologies with proper driver and control ICs allows getting a power converter design with superior features in performance and reliability.

The demo board promotes a full Infineon solution suitable for one the multi-phase/interleaving design technique with phase shedding, by achieving very high and flat efficiency plot and homogeneous heat spreading, needed conditions to achieve high power density.

The concept allows a reliable use of the HB LLC topology, which is the most cost effective for high efficiency designs. It fully proves the good operation in that topology of the 600 V CoolMOS™C7, a technology which is confirmed to be suitable for both hard and soft switching appications. The 150 V OptiMOS™ 5 series is demonstrated having all the needed features in order to guarantee an efficient and reliable operation in the synchronous rectification stage of a complex dual-phase design.

In order to make the board test even more “user friendly”, a graphical user interface has been designed, by giving the opportunity to the engineers to easily interact with the converter during the anaylsis on the bench.

The present document gives an overview about the most relevant design aspects and the considerations behind the decision to build up such a demonstrator.

A bill of material and a detailed description of the most important active and passive used components, including the specification of the magnetic parts is available inside this application note.

Details are also provided about the XMC4000 based digital control features, with an accurate description of the implemented algorithms.

Finally the performances are documented by captured waveforms and efficiency plot: all the shown results have been achieved with 600 V C7 40 mΩ in TO-247 package, but they are the same in case the device is used in the TO-220 package.

7 Technical data package (TDP)

By clicking on the **Figure** below, the reader can find a file providing a useful summary of all the technical and assembling features of the Infineon 3 kW dual-phase LLC demo board.

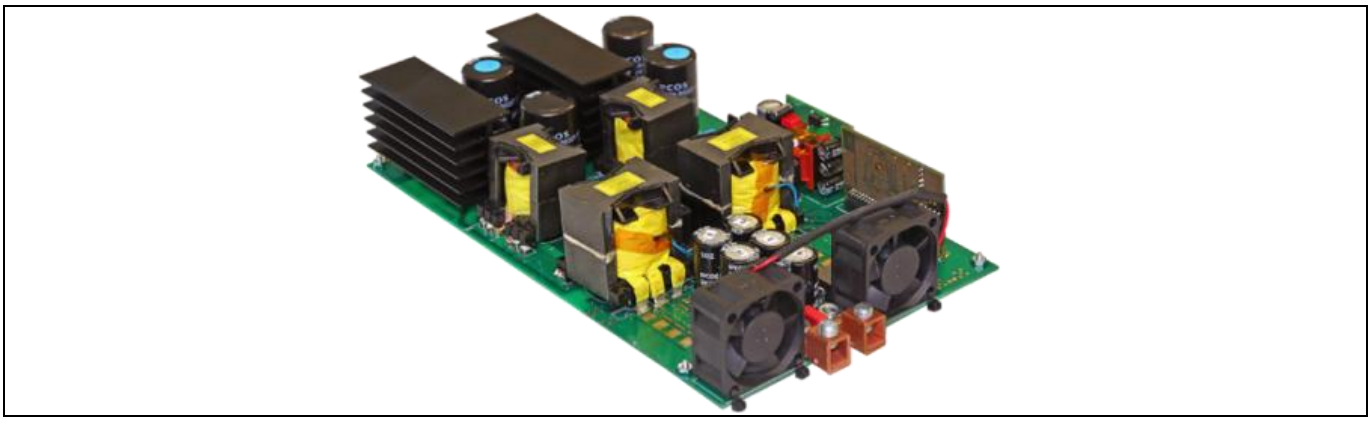


Figure 46 3 kW dual-phase LLC demo board (summary link)

The BOMs of the motherboard and the two daughter cards are available in this document. The CAD and Gerber files are available upon request.

Also a procedure for functional test is included: this is exactly the one applied to each prototype during the mass production.

8 Useful material and links

In the following links, you can find more detailed information about the devices used from Infineon and the magnetic components.

Primary HV MOSFETs CoolMOS™ IPW60R040C7

https://www.infineon.com/dgdl/Infineon-IPW60R040C7-DS-v02_00-EN.pdf?fileId=5546d4624cb7f111014d4c6ece273fe9

Primary HV MOSFETs CoolMOS™ IPP60R040C7

https://www.infineon.com/dgdl/Infineon-IPP60R040C7-DS-v02_00-EN.pdf?fileId=5546d4624cb7f111014d479ac7c56893

Microcontroller XMC4400

https://www.infineon.com/cms/en/product/microcontroller/32-bit-industrial-microcontroller-based-on-arm-cortex-m/32-bit-xmc4000-industrial-microcontroller-arm-cortex-m4/xmc4400/

Advanced dual channel gate drive 2EDN7524F

https://www.infineon.com/cms/en/product/power/gate-driver-ics/2edn7524f/

Isolated gate drive 1EDI60N12AF

https://www.infineon.com/dgdl/Infineon-1EDI60N12AF-DS-v02_00-EN.pdf?fileId=db3a3043427ac3e201428e5da08f372a

Bias QR flyback controller ICE2QR2280Z

https://www.infineon.com/dgdl/Datasheet_ICE2QR2280Z_v21_20110830.pdf?folderId=db3a304412b407950112b408e8c90004&fileId=db3a30432a7fedfc012a8d8038e00473

SR MOSFETs OptiMOS™ BSC093N15NS5

https://www.infineon.com/dgdl/Infineon-BSC093N15NS5-DS-v02_02-EN.pdf?fileId=5546d462503812bb01507033a3fa1175

Main transformer and resonant choke ferrite cores

https://en.tdk.eu/blob/519704/download/2/ferrites-and-accessories-data-book-130501.pdf

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10 List of abbreviations

Table 5

Abbreviation	Definition
ADC	Analog to Digital Converter
BD	Body Diode
BOM	Bill Of Materials
CAD	Computer-Aided Design
CCU	Capture and Compare Unit
CLT	Coreless transformer
CMTI	Common mode transient inmunity
Coss	Output capacitance Coss=CDS+CGD
Co(tr)	Effective output capacitance, time related
COM	Communication port
Cr	Resonant capacitance
CSG	Comparator and slope generator
DAC	Digital to analog converter
DC	Direct current
DMA	Direct memory access
DSP	Digital signal proccesor
di/dt	Steepness of current slope at turn off / turn on
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	Electromagnetic interference
EOSS	Stored energy in output capacitance (Coss) at typ. VDS=400V
ERU	Event request unit
FET	Field effect transistor
FPU	Floating point unit
Fsw	Switching frequency
GaN	Gallium nitride
GND	Electric ground
GUI	Graphical user interface
HB	Half-bridge
HS	High side
HRC	High resolution channel
HRPWM	High resolution PWM
HV	High voltage
IC	Integrated circuit
ID	Drain to source current
IDE	Integrated development environment
Iout_phase	Output current of one converter

List of abbreviations

Abbreviation	Definition
Ires	Resonant current
I2C	Inter-integrated circuit communication protocol
LCD TV	Liquid-crystal-display televisions
Lr	Resonant inductance
Lm	Magnetizing inductance
LS	Low side
LV	Low votage
MAC	Multiplication and accumulation unit
MOSFET	Metal oxide semiconductor field effect transistor
NTC	Negative Temperature Coefficient thermistor
OCP	Overcurrent protection
PFC	Power factor correction
PI	Proportional integral controller
PSU	Power supply unit
PWM	Pulse width modulation
QG	Gate charge
QOSS	Charge stored in the COSS
QR	Quasi resonant
RAM	Random access memory
RDS(on)	Drain-source on-state resistance
Rg,on/off	Gate resistor applied at on and aff transitions
SMPS	Switched mode power supply
SPI	Serial peripheral interface
SR	Synchronous rectification
SW	Software
TDP	Technical data package
TTL	Transistor-transistor logic
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal serial bus
USIC	Universal serial interface channel
VBulk	Bulk capacitor voltage
Vcc	Supply voltage
VCr	Resonant capacitor voltage
VDS	Drain to source voltage
VGS	Gate to source voltage
VO;PFC	PFC Output voltage
Vout	Output voltage
ZVS	Zero voltage switching

Revision History

Major changes since the last revision

Page or Reference	Description of change

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