Application note BGSA403ML10

Measurement and Application Guide

About this document

Scope and purpose

This application note provides an overview of the features, parameters and application guidelines for the antenna tuning switch BGSA403ML10. The measurement procedures are described for determining different key parameters.

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1 Antenna tuning

Nowadays, connected devices need more and more antennas to support growing RF requirements and cover an even wider frequency range. At the same time, antenna dimensions must be minimized due to Industrial Design (ID) constraints. As a result, antenna performance can be affected with regard to radiated power and receiver sensitivity.

Antenna tuning is a solution to this challenge, helping RF engineers to optimize antenna efficiency, which translates into enhanced user experience in terms of higher data rates, longer battery life and improved signal quality. Infineon offers a comprehensive portfolio of antenna tuning switches for impedance and aperture tuning cases to address antenna design challenges and enable maximum power transfer for best antenna efficiency.

1.1 Antenna impedance tuning

Antenna impedance matching is carried out at the antenna feed point, as shown in Figure 1. Using this type of antenna tuning, forward power to the antenna can be optimized by matching the antenna input impedance to 50 Ω. In this way, impedance tuning helps to maximize signal transmission between RF Front-End (RFFE) and the antenna by compensating for frequency and environmental effects.

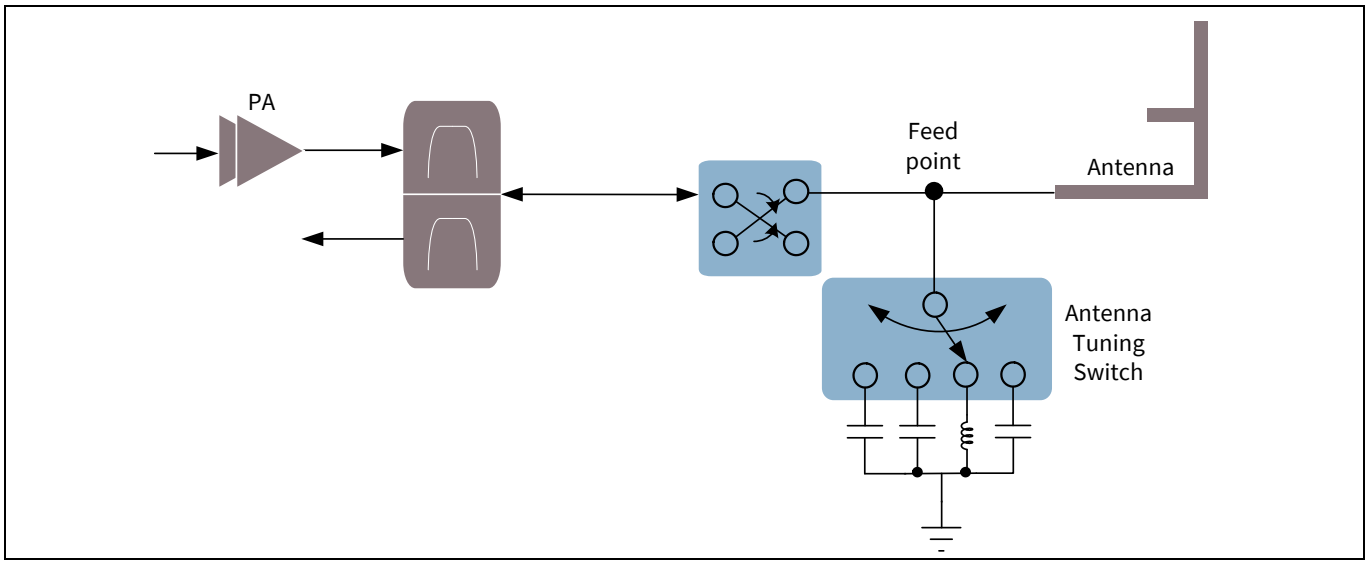


Figure 1 Antenna impedance matching

1.2 Antenna aperture tuning

A more widely used antenna tuning technique is aperture tuning, which improves antenna efficiency by shifting the natural resonance of an antenna to the required frequency band of operation. This reduces stress on the antenna-driving hardware on the transmitter side (Tx) and increases sensitivity on the receiver side (Rx). Aperture tuning also allows antennas to communicate on multiple bands simultaneously to support carrier aggregation.

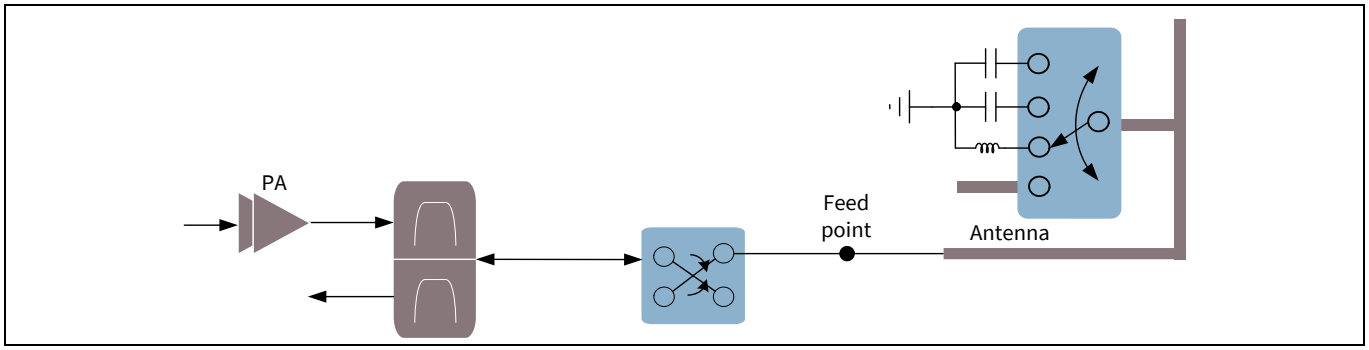


Figure 2 Antenna aperture tuning

1.3 Antenna tuner key parameters

Certain characteristics are important for antenna tuning. These are explained in the following section.

1.3.1 Voltage distribution on antenna tuning switches

Aperture tuners are implemented at the antennas with certain electromagnetic field distributions in the near field. For example, an IFA antenna is a quarter-wavelength resonating structure consisting of one open circuit at one end and one short-circuit at the other end. Its electromagnetic field distribution can be analyzed through the voltage and current distribution on the conducting parts. As shown in the figure below, the highest RF voltage (V_{RF}) is observed at the open-circuit side, while the highest RF current is located at the short-circuit side. Voltages across the tuner that exceed its limit can damage the device and can lead to antenna efficiency degradation. Therefore, the antenna tuner should be placed in the appropriate position at the antenna.

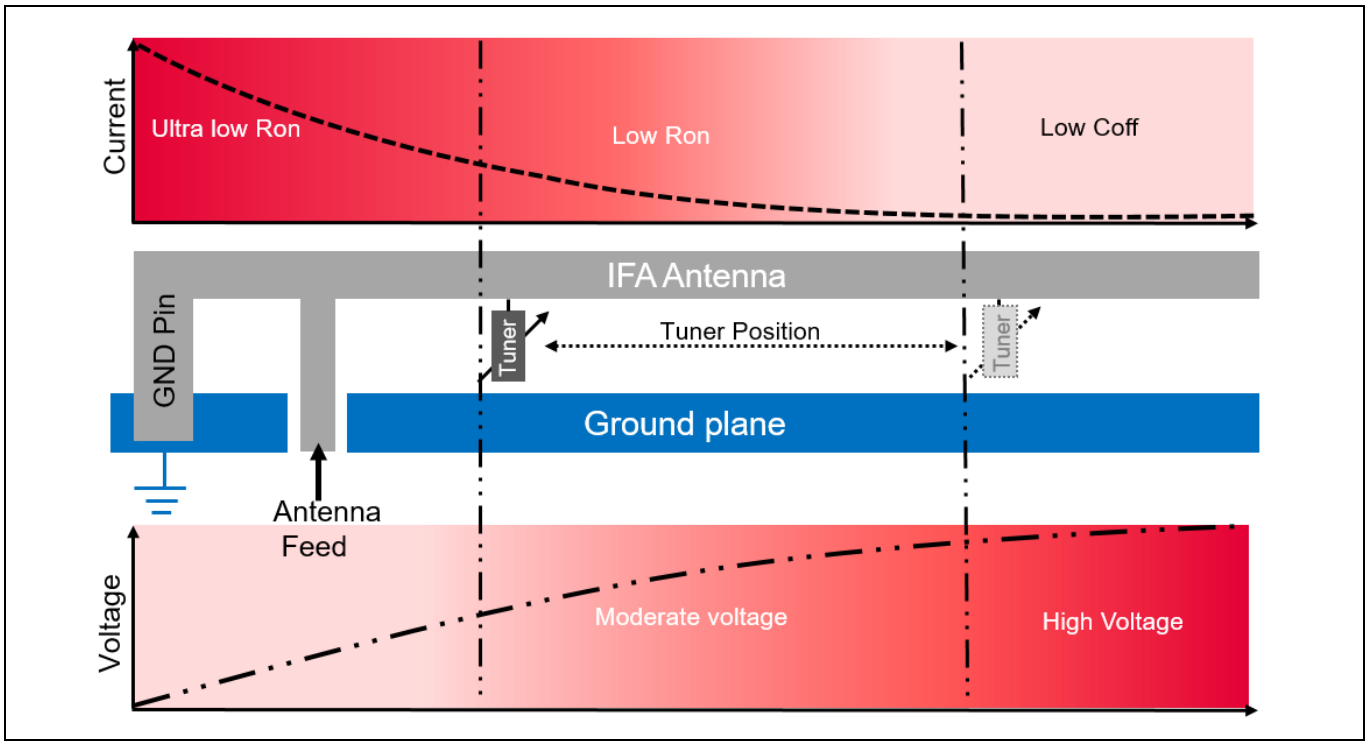


Figure 3 Impact of antenna tuner placement at the antenna on V_{RF}, R_{ON} and C_{OFF}

1.3.2 ON resistance (R_{ON})

The R_{ON} of antenna tuning switches is a key differentiating feature. The lower the R_{ON}, the lower the ON path loss. Because an antenna tuning switch is directly connected to the antenna, higher R_{ON} means higher ON path loss and consequently lower quality factor (Q-factor). The effect of R_{ON} varies depending on different types of antenna tuning. For antenna tuning at a higher RF voltage point of the antenna, where lower RF current is flowing through the ON path of the switch, R_{ON} has a negligible effect. However, for low-voltage tuning cases, R_{ON} has a significant effect. This phenomenon is explained in the figure below. The RF voltage level depends on the power fed to the antenna as well as the placement of the tuner at the antenna.

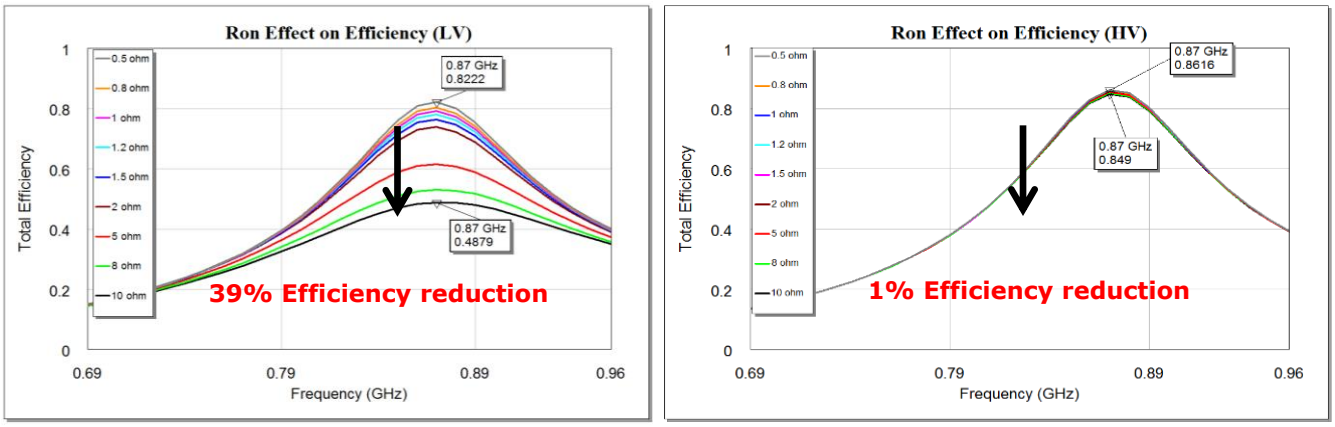


Figure 4 Low-voltage versus high-voltage tuning case

1.3.3 OFF capacitance (C_{OFF})

C_{OFF} is also one of the key features of antenna tuning switches. A higher C_{OFF} results in a large high-frequency band loss and causes self-resonances. Thus, for better performance, a lower C_{OFF} is important for an antenna tuning switch. The impact of C_{OFF} varies depending on different types of antenna tuning. For high-voltage aperture tuning, C_{OFF} has a significant de-tuning effect on the antenna. For low-voltage aperture tuning, this effect is quite small. This behavior is shown in Figure 5.

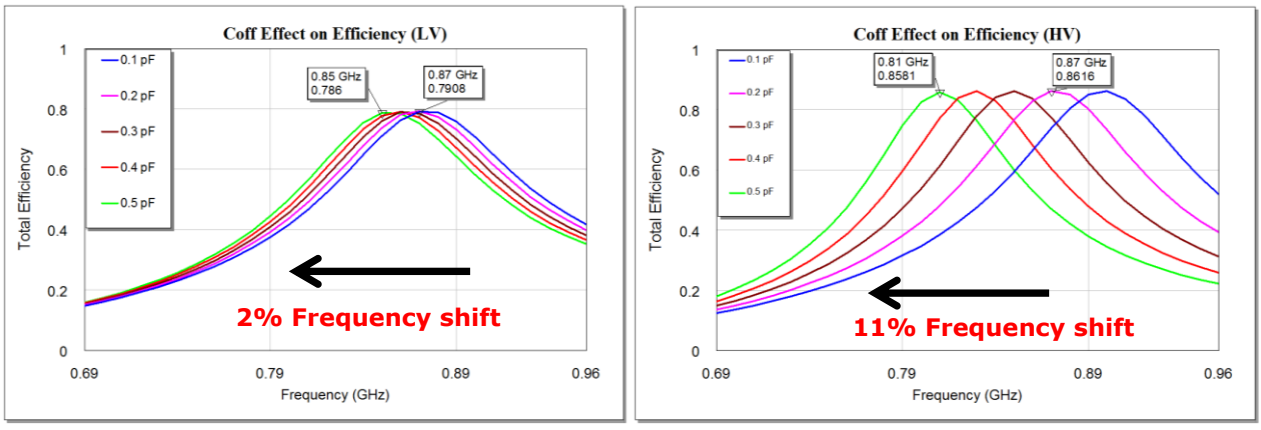


Figure 5 Low-voltage versus high-voltage tuning case

1.3.4 Maximum RF voltage (V_{RF})

Antenna tuning switches only work under certain RF voltage regulations, e.g. below breakdown voltage. When the antenna is analyzed by using a transmission line model, the characteristic impedance of the antenna model varies with antenna structure. High impedance of the antenna results in high V_{RF} across the antenna tuning switch (see VRF measurement). Generally, the voltage generated is much higher than the specified V_{RF} for a standard switch.

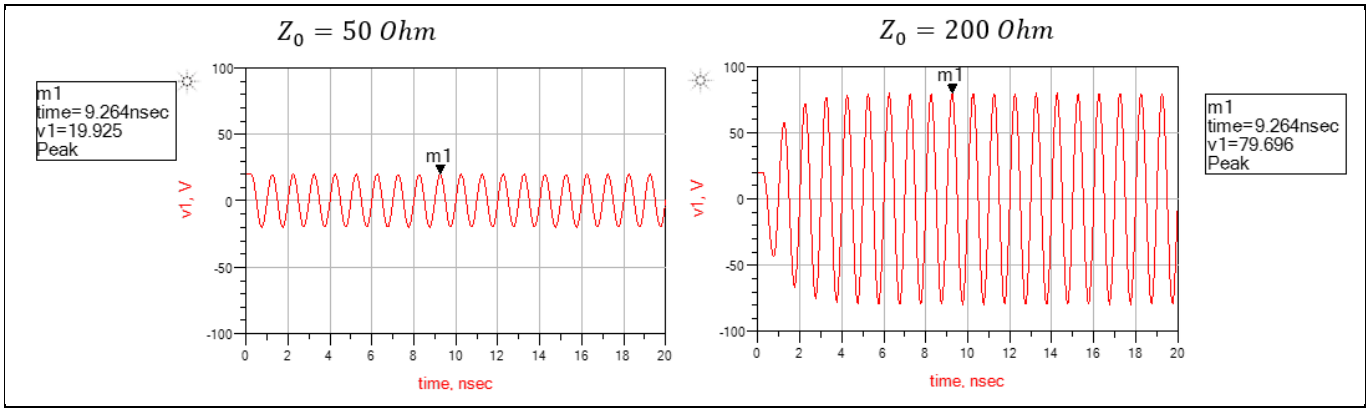


Figure 6 Maximum RF voltage with different impedances

The figure above shows how the characteristic impedance Z0 directly impacts the RF voltage across a transmission line. When Z0 is ideal (50 Ω), the RF voltage is moderate, but when the characteristic impedance increases, the RF voltage reacts accordingly. To calculate the RF voltage across a transmission line, the formula below can be used.

$$|V|_{RF} = \sqrt{2PZ_0}$$

In the formula, V_{RF} is the RF voltage, $\boldsymbol{Z_0}$ is the characteristic impedance and P is power at a lossless transmission line.

2 BGSA403ML10

The BGSA403ML10 is a versatile shunt to ground 4x single-pole single-throw (4xSPST) RF antenna tuning switch. It is optimized for low C_{OFF} as well as low R_{ON} enabling applications up to 7.125 GHz. The BGSA403ML10 is ideal for antenna tuning applications. This chip integrates on-chip CMOS logic and power supply regulation. Its digital control interface is compliant with MIPI2.1 RFFE specification and each switch throw can be programmed individually or all together in the same RFFE command frame. Up to 4 instantiations of the same device can be controlled using the same RFFE bus thanks to its 4 states USID_SEL pin unique feature.

Block diagram and key features

- Low R_{ON} resistance of 0.98 Ω at each port in ON state
- Low C_{OFF} capacitance of 205 fF at each port in OFF state
- High RF operating peak voltage handling of typical 50 V in OFF state
- MIPI RFFE 2.1 compliant control interface
- Extremely low current consumption of 22 µA
- 4 USID addresses enabled by external condition at USID_SEL pin
- Small form factor 1.1 mm x 1.5 mm (MSL1, 260 ◦C per JEDEC J-STD-020)

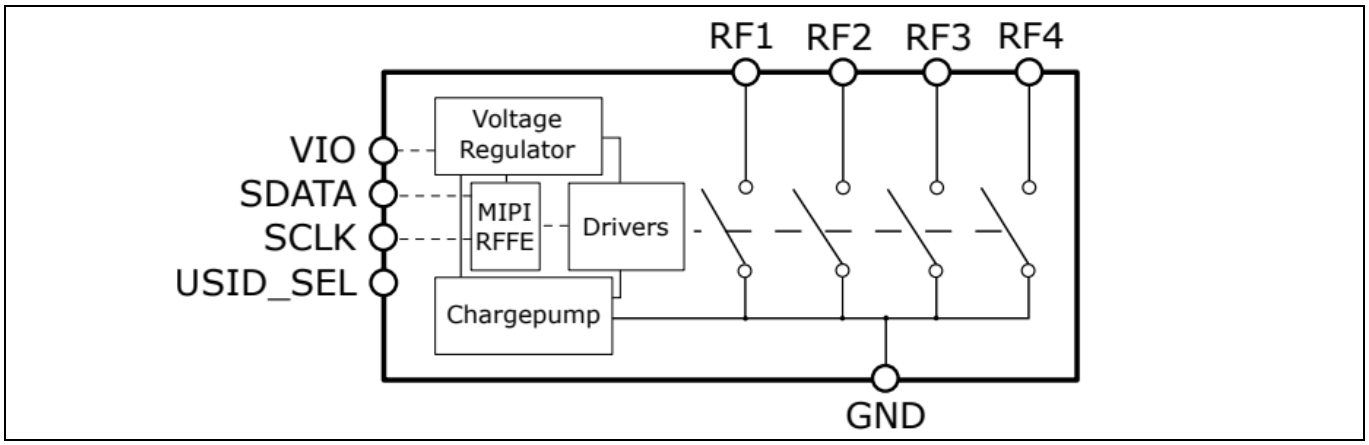


Figure 7 Block diagram BGSA403ML10

3 Measurement setups

3.1 Application boards

The evaluation boards (EVBs) for S-parameters, harmonics and V_{RF} measurements are shown below. The measurement setups and measurement procedures are explained in the following chapters. Each EVB has a 10-pin connector to control the device via the MIPI RFFE interface (see MIPI RFFE control interface). The pin configuration is printed on the EVB.

3.1.1 S-parameter evaluation board

The S-parameter EVB is used for S-parameter measurements (see S-parameter measurement). A separate de-embedding board is used to compensate for the effects of the PCB on the test results.

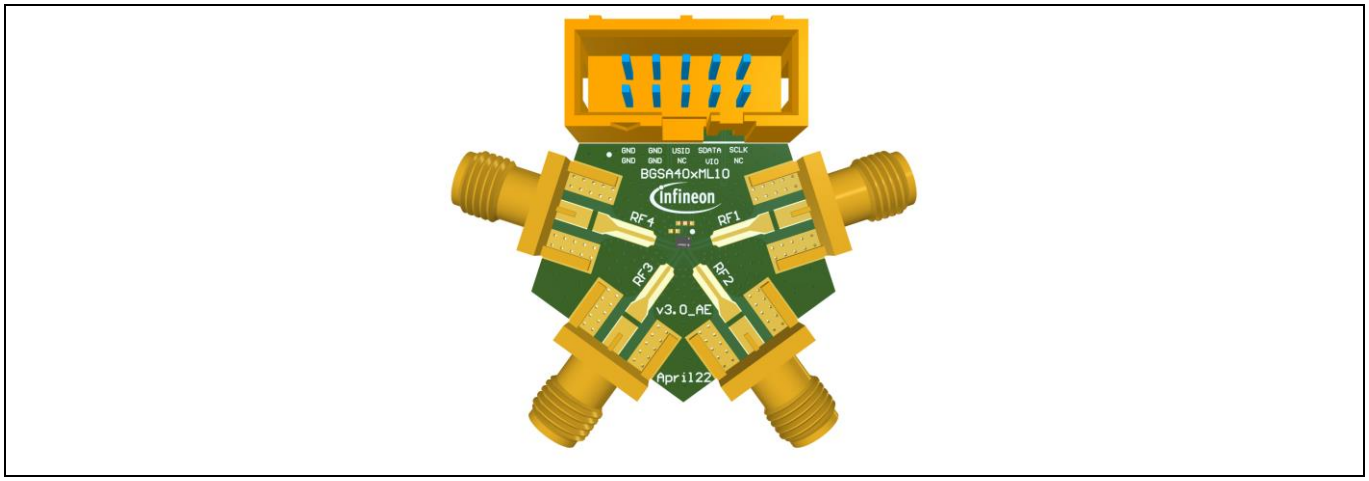


Figure 8 S-parameter evaluation board of BGSA403ML10

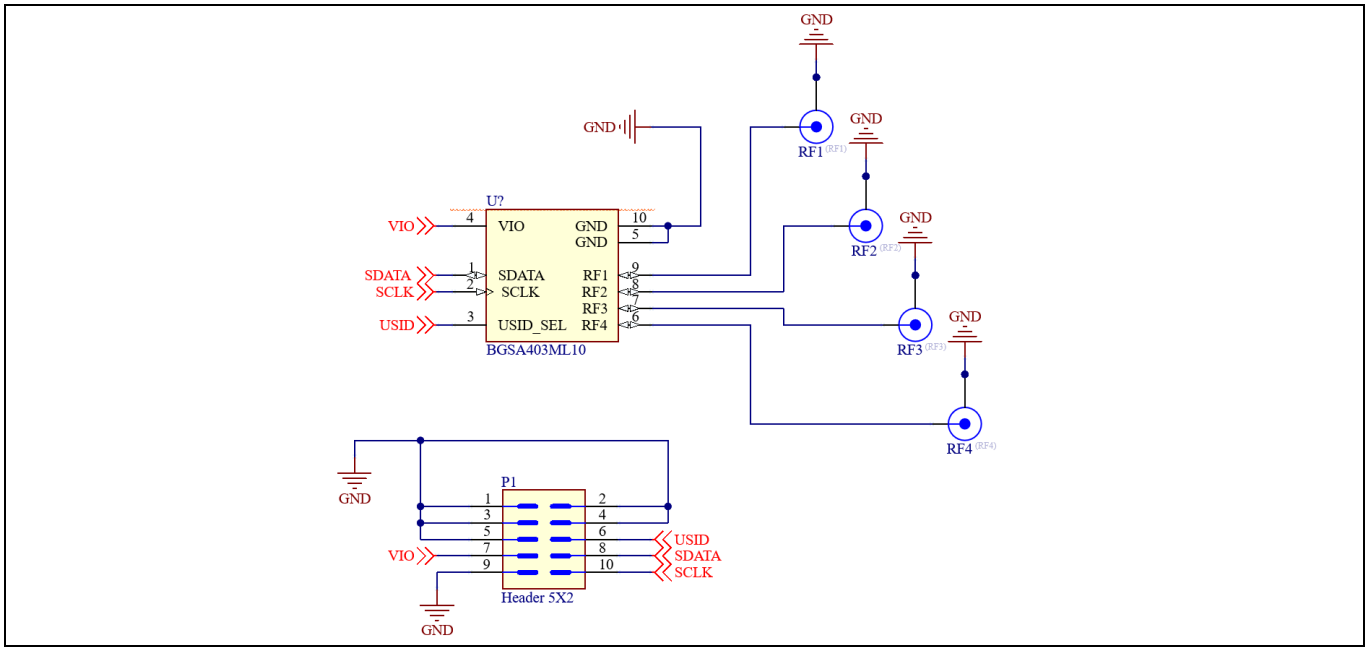


Figure 9 Schematic of the BGSA403ML10 S-parameter evaluation board

The layers of the S-parameter EVB are shown below.

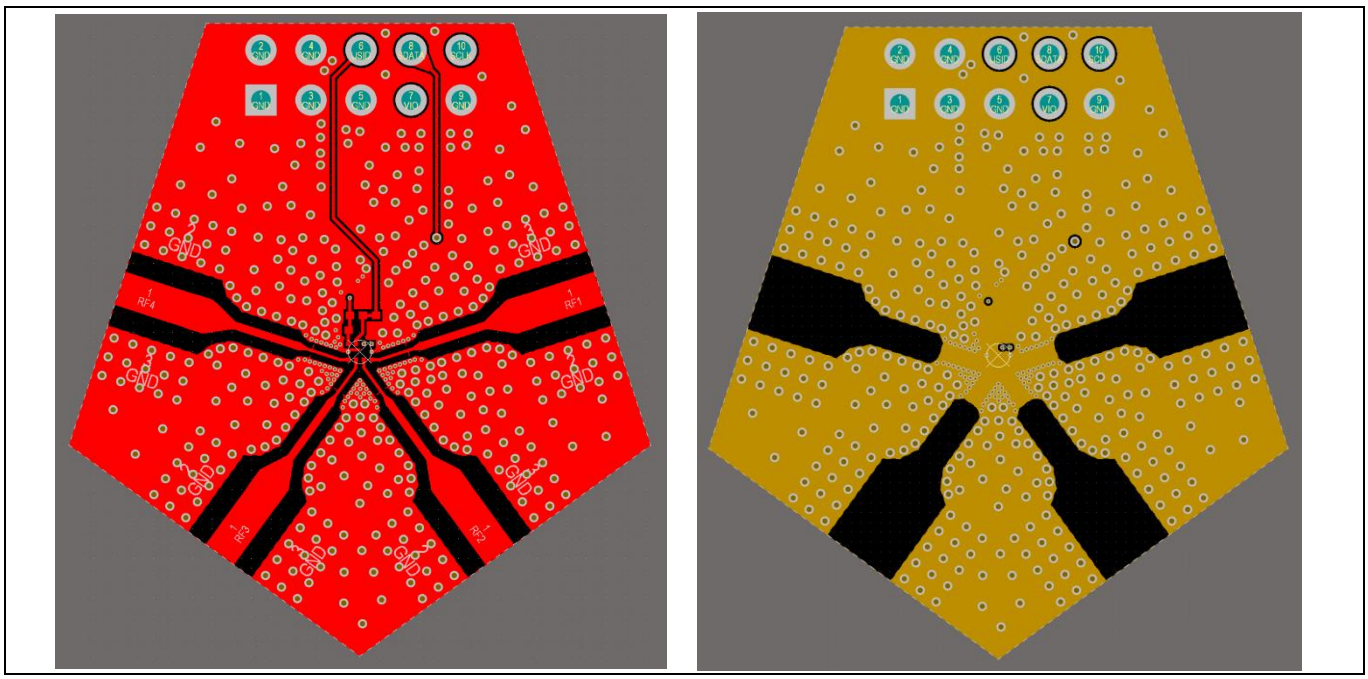


Figure 10 S-parameter EVB first and second layer

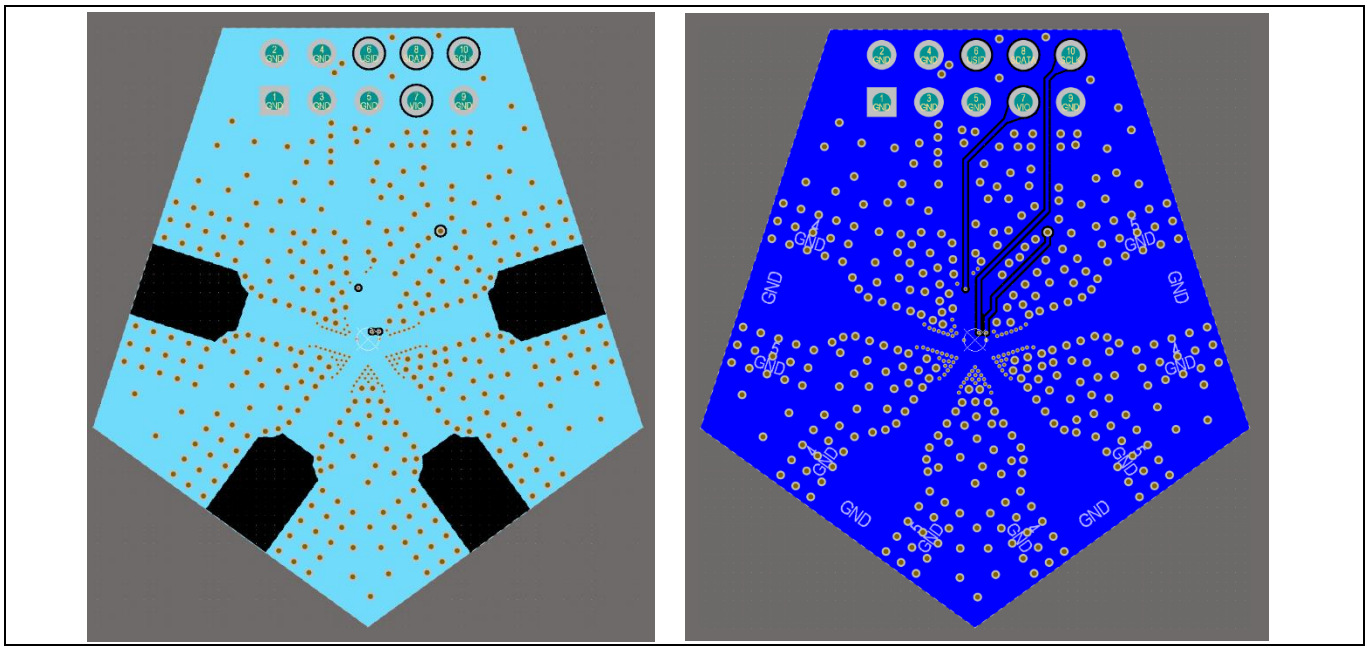


Figure 11 S-parameter EVB third and fourth layer

3.1.2 V_{RF} evaluation board

The V_{RF} EVB is used for V_{RF} measurements (see V_{RF} and harmonic measurement setup) as well as for harmonics measurements for this device (OFF mode). Each individual port can be stressed using this EVB.

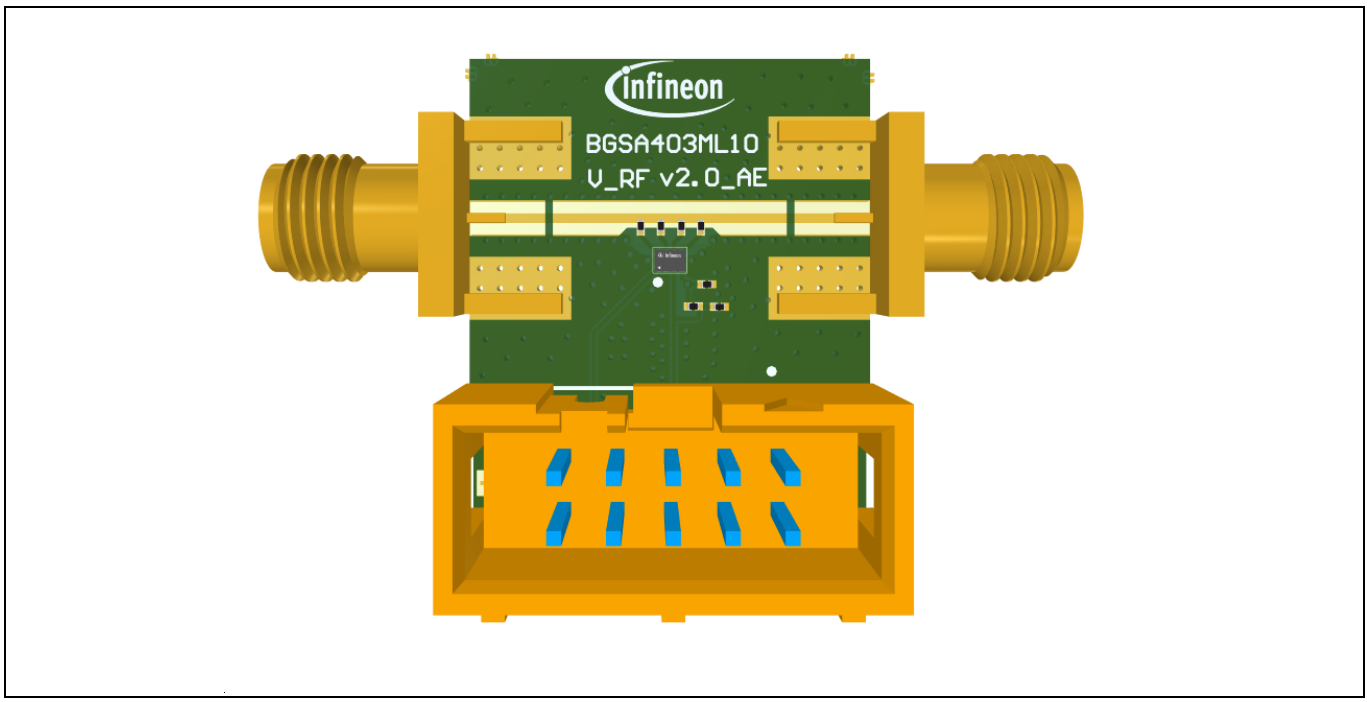


Figure 12 V_{RF} EVB for BGSA403ML10

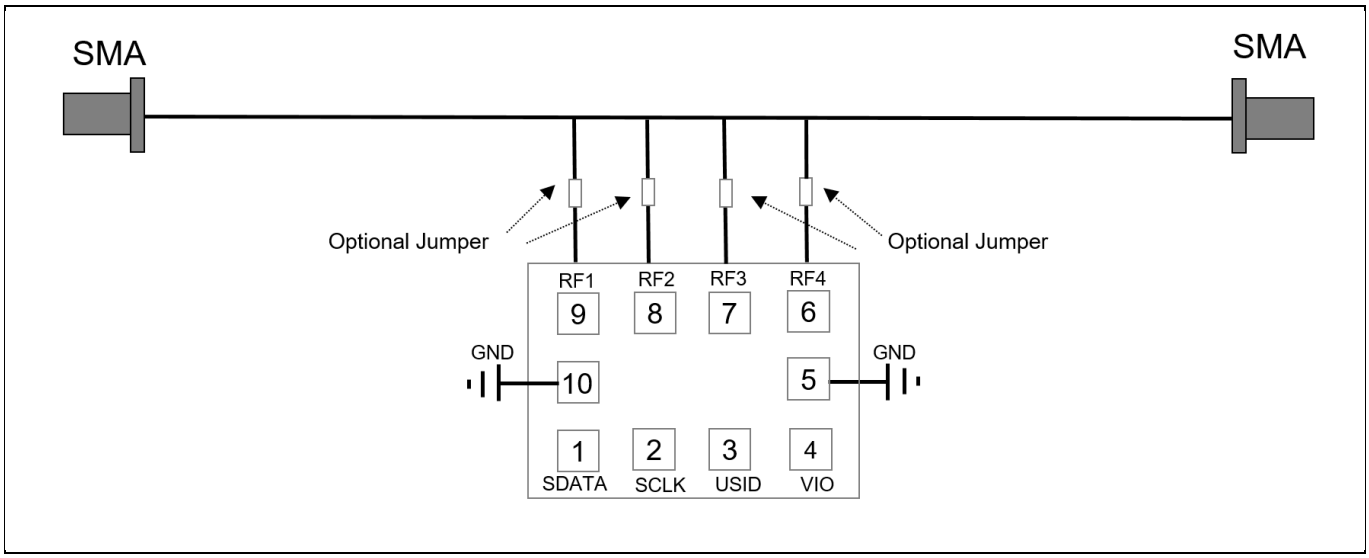


Figure 13 Schematic of the V_{RF} EVB for BGSA403ML10

The layers of the V_{RF} EVB are shown below.

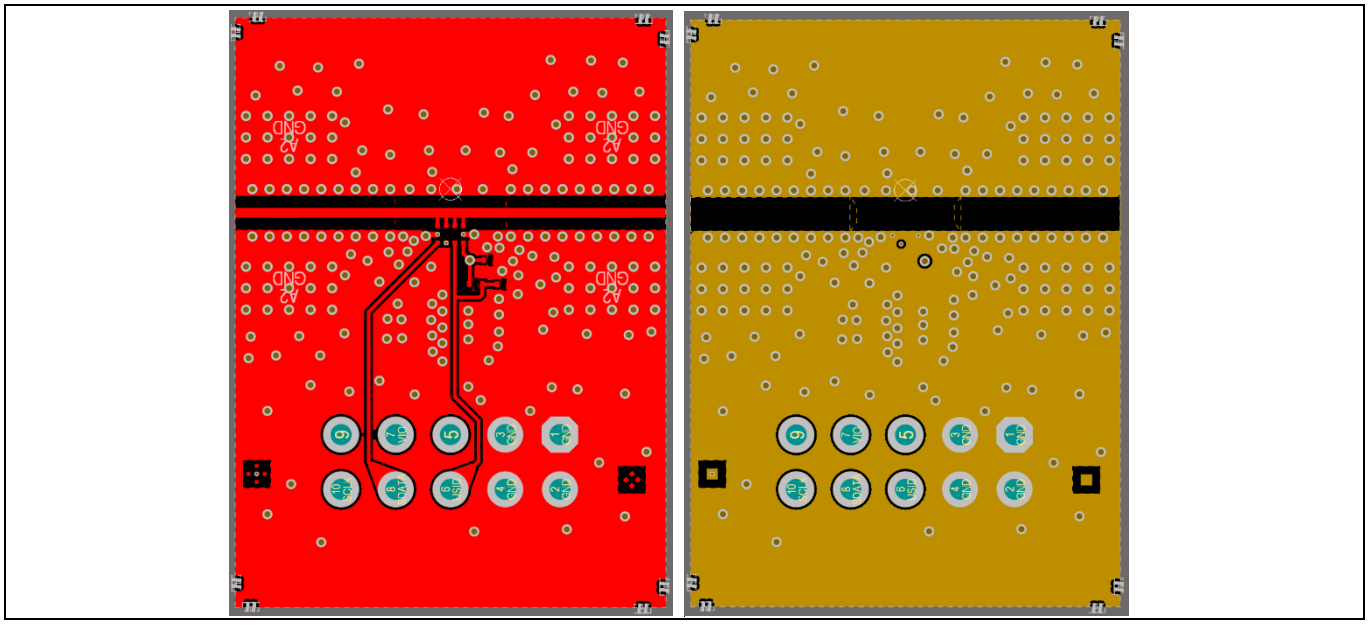


Figure 14 V_{RF} EVB first and second layer

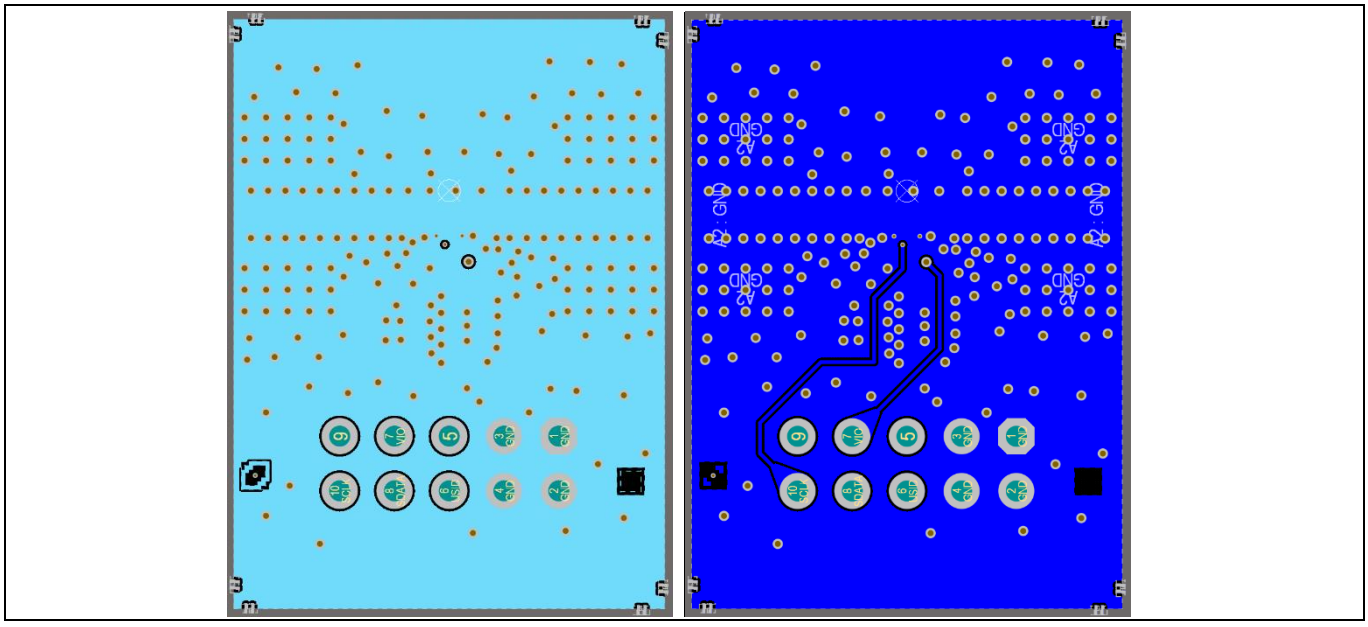


Figure 15 V_{RF} EVB third and fourth layer

3.2 Measurement setup preparation

3.2.1 De-embedding

The RF device under test (DUT) is soldered on a PCB for evaluation. A de-embedding procedure is necessary to compensate for the effects of the PCB (in terms of mismatch, losses, phase delay and parasitics).

For BGSA403ML10, the “2x through de-embedding” method is used. This method requires a S-parameter measurement of a through line board (see Figure 16), which is equal to two times the length of the EVB’s RF line. The de-embedding file is generated using an internal Infineon software with the information of the measured S-parameters.

This method is described in the paper “IEEE Standard for Electrical Characterization of Printed Circuit Board and Related Interconnects at Frequencies up to 50 GHz” (IEEE 370-2020).

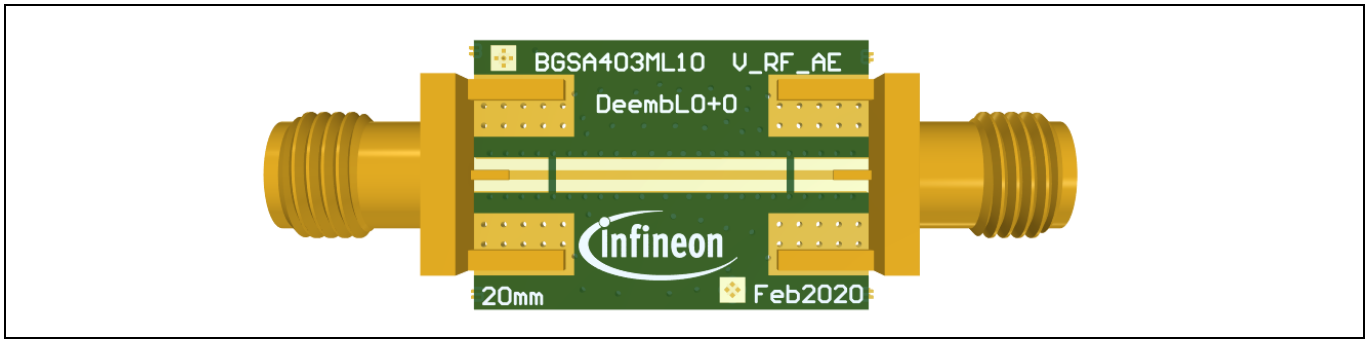


Figure 16 Deembedding board

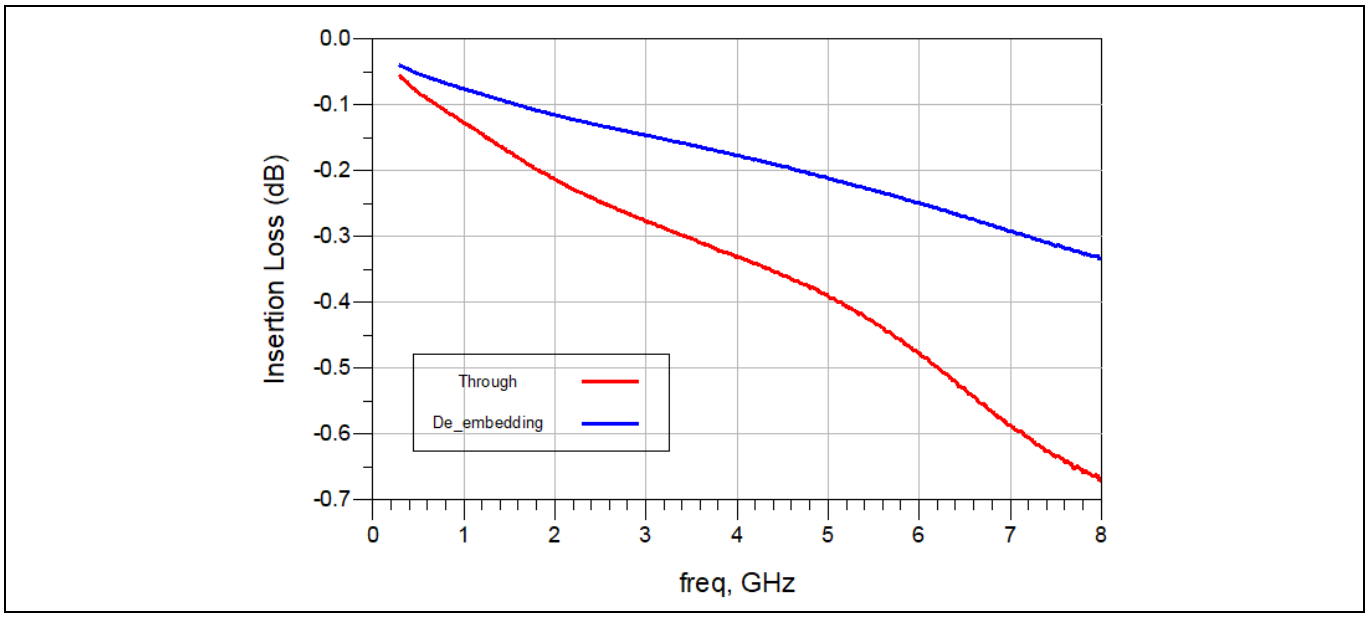


Figure 17 Example measurement of the through-line and the generated de-embedding file

3.3 MIPI RFFE control interface

A MIPI stick is needed to control the device via a computer. In the picture below, all the connections of the MIPI stick are shown that can be used to activate and control the device.

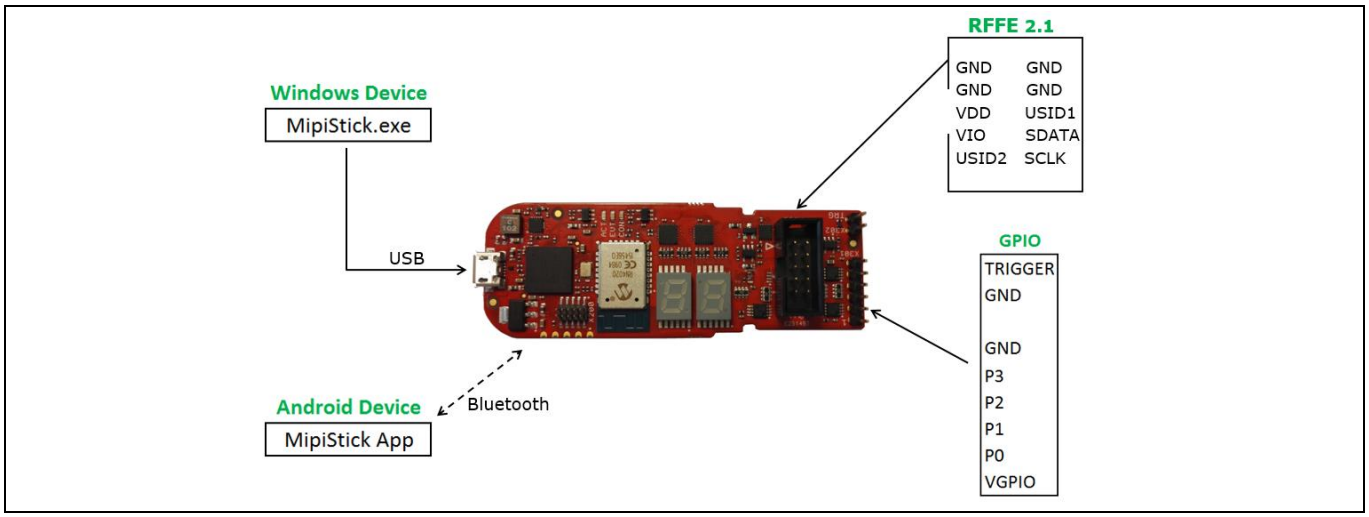


Figure 18 MIPI stick

Once the connection (VIO, SCLK, SDATA, GND) between the MIPI stick and the EVB is set up, it can be connected to a PC via USB. After starting the GUI and activating the device, the following control interface appears.

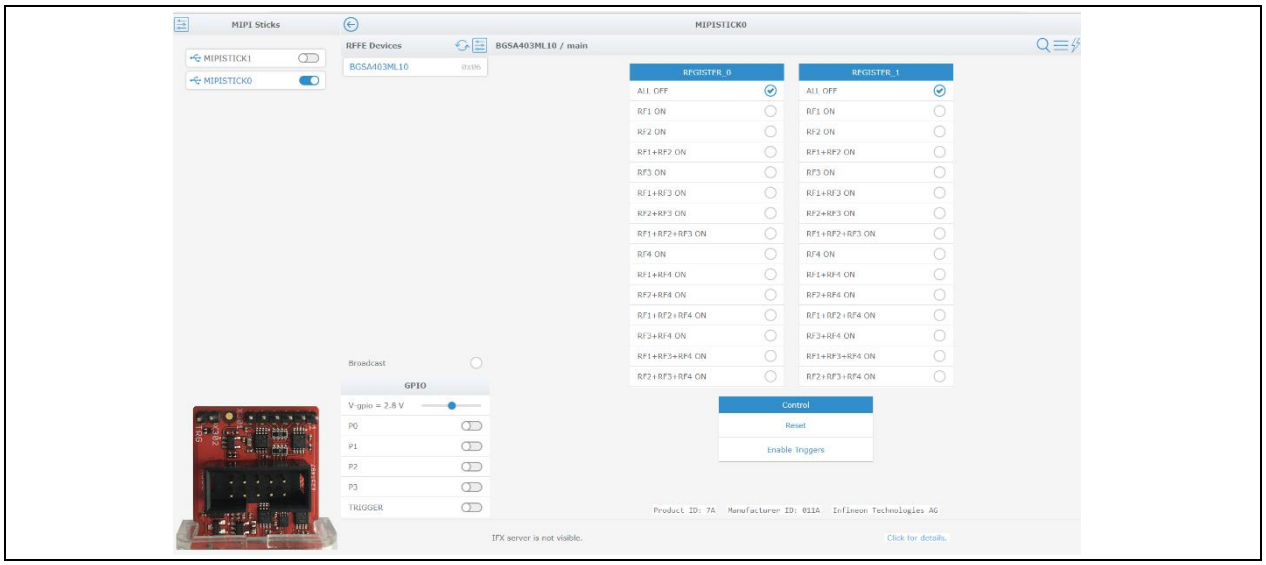


Figure 19 The MIPI GUI (control interface to control MIPI devices via a computer)

Here also the desired device states can be set. Register_0 and Register_1 RF switch control bits are identical. Writing both Registers (Register_0 and Register_1) simultaneously will lead to undefined behavior. The unused Register (Register_0 or Register_1) must remain 0x00 (all series OFF and all shunt OFF).

3.3.1 Truth table

With the help of the truth table, the desired state can be chosen. The BGSA403ML10 truth table enables connection of any combination of the bits below in one single write to register_0 (respectively register_1) command. Register_0 and Register_1 RF switch control bits are identical. Writing both registers (Register_0 and Register_1) simultaneously will lead to undefined behavior. The unused register (Register_0 or Register_1) must remain 0x00.

State	Mode	D7	D6	D5	D4	D3	D2	D1	D0
0	ALL OFF (Isolation)	x	x	x	x	0	0	0	0
1	RF1 ON	x	x	x	x	0	0	0	1
2	RF2 ON	x	x	x	x	0	0	1	0
3	RF1+RF2 ON	x	x	x	x	0	0	1	1
4	RF3 ON	x	x	x	x	0	1	0	0
5	RF1+RF3 ON	x	x	x	x	0	1	0	1
6	RF2+RF3 ON	x	x	x	x	0	1	1	0
7	RF1+RF2+RF3 ON	x	x	x	x	0	1	1	1
8	RF4 ON	x	x	x	x	1	0	0	0
9	RF1+RF4 ON	x	x	x	x	1	0	0	1
10	RF2+RF4 ON	x	x	x	x	1	0	1	0
11	RF1+RF2+RF4 ON	x	x	x	x	1	0	1	1
12	RF3+RF4 ON	x	x	x	x	1	1	0	0
13	RF1+RF3+RF4 ON	x	x	x	x	1	1	0	1
14	RF2+RF3+RF4 ON	x	x	x	x	1	1	1	0
15	RF1+RF2+RF3+RF4 ON	x	x	x	x	1	1	1	1

[1] Do not care, x = 0 or 1

Figure 20 Truth table BGSA403ML10

3.3.2 USID setting

The external USID_sel pin enables four default USID addresses: Ground, to VIO, Floating and 220 kΩ to VIO.

Address	Symbol	External conditon at USID_SEL Pin
USID=0110	Addr6	Ground
USID=0111	Addr7	to VIO
USID=1000	Addr8	Floating[1]
USID=1001	Addr9	220 kΩ to VIO[1]

[1] Total capacitance on the USID_SEL pin must be <5 pF.

Figure 21 Default MIPI USID states

By using different USID addresses, up to four devices in one MIPI bus can be individually controlled. The pin configuration below shows how the USID selection pin needs to be connected to configure various addresses.

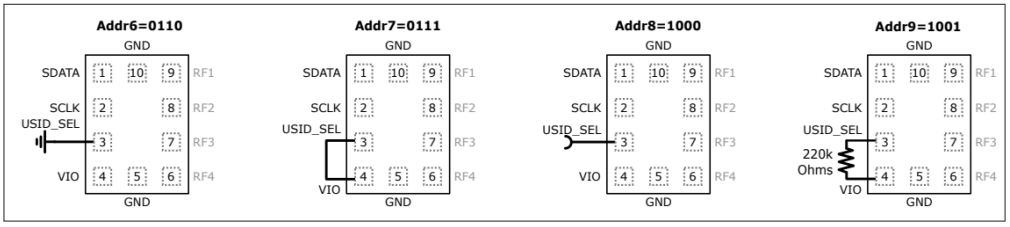


Figure 22 BGSA403ML10 USID_Sel pin configuration

3.4 Measurements

3.4.1 S-parameter measurement

With the help of a Vector Network Analyzer, the S-parameters (Isolation) of the device are measured. In the figure below, the connection of the RF ports as well as the DC pins with the DUT are shown. After activating the DUT in the desired state, all S-parameters for the specific RF ports with de-embedding are measured.

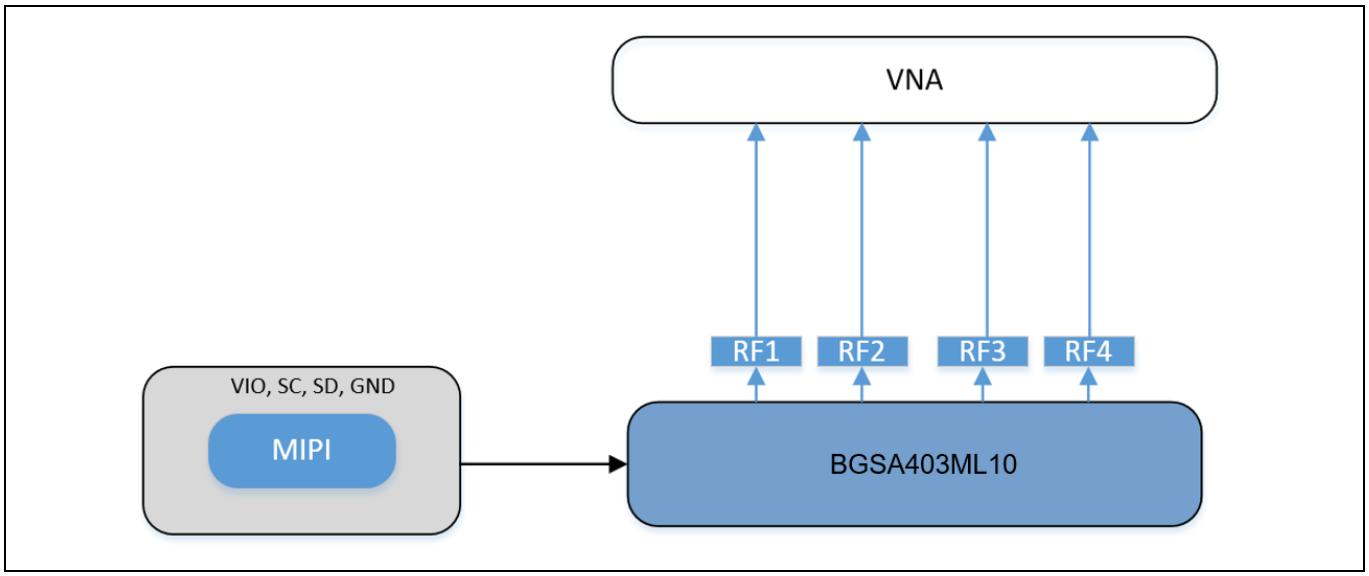


Figure 23 S-parameter measurement setup

3.4.2 C_{OFF} measurement process

One of the main parameters of antenna tuning switches is the OFF state capacitance. C_{OFF} significantly affects the antenna resonant frequency.

The capacitance value is checked using the Y-parameters, while the device is set to the isolation state. The C_{OFF} extraction of shunt devices is very sensitive to the phase. For this reason, the accuracy during the measurement process is very important.

For shunt antenna tuner switches like BGSA403ML10, C_{OFF} is extracted in three steps. At first, the S-parameters of the de-embedded unpopulated S-parameter EVB is measured and the pad-to-pad capacitance is extracted. Afterwards, the device is soldered on the EVB and the de-embedded S-parameter in isolation state is measured. To get rid of the impact of the pad-to-pad capacitance, in the last step the capacitance of the empty board is subtracted from the C_{OFF} of the DUT.

The C_{OFF} extraction is usually done in post processing (e.g. in ADS or microwave office). The OFF capacitance is specified in femto Farad (fF).

The used formulas are displayed below.

$$Coff_{RFx_Emptyboard} = \frac{(imag(Y(x,x)) * 10^{15}}{(2\pi * freq)}$$

$$Coff_{RFx_DUT} = \frac{(imag(Y(x,x)) * 10^{15}}{(2\pi * freq)}$$

$$Coff_{RFx_final} = Coff_{RFxDUT} - Coff_{RFx_Emptyboard}$$

Figure 24 Formula to calculate the OFF capacitance (C_{OFF})

3.4.3 R_{ON} measurement process

To measure the ON resistance of the switch (R_{ON}), a power source is used. The force and the sense lines of the power source are connected with the two banana cables to the desired port of the EVB using an adapter. The figure below shows the flow of measuring R_{ON} using the S-parameter board. To negate the cable resistance, the four-wire method is used.

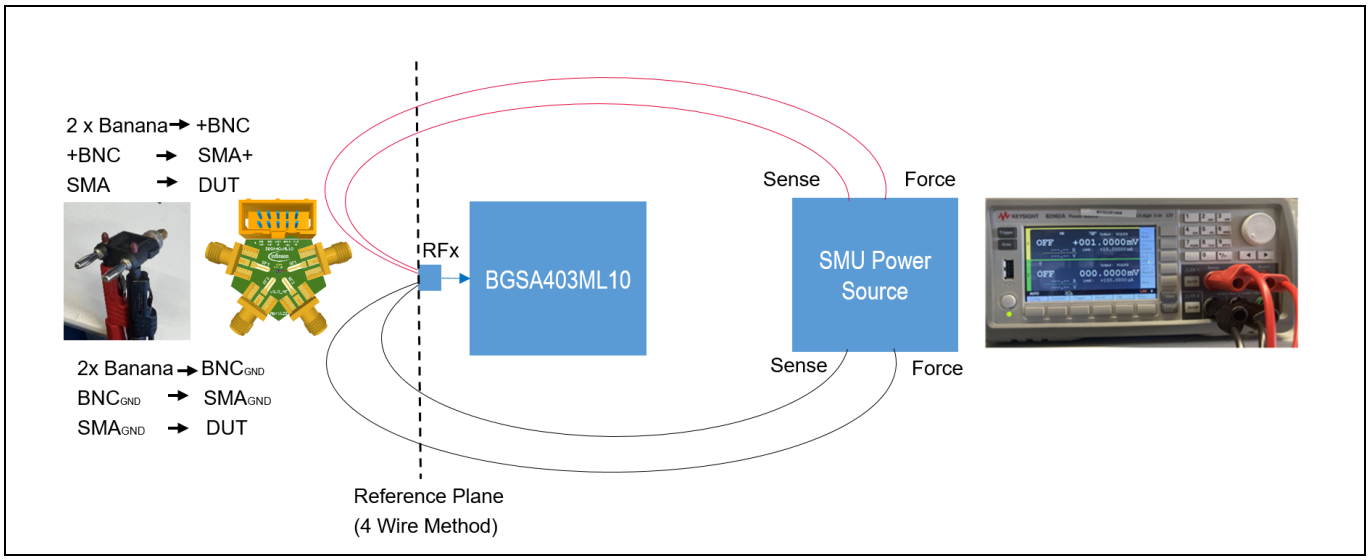


Figure 25 R_{ON} measurement setup

To compensate the impact of the PCB resistance, the resistance of the de-embedding board (through line) is taken into account. The resistance of the through-line is measured by connecting the force and the sense line at one port of the board and the other port is connected with a short to ground (Figure 26). The resistance of the de-embedding board is devided by two and is subtracted from the ON resistance of the PCB.



Figure 26 Resistance measurement of the de-embedding board

3.4.4 V_{RF} and harmonics measurement setup

To measure the harmonic behavior and the maximum V_{RF} capability, the same basic setup is used.

In both cases, an input signal at the DUT with a known power level and frequency is needed. The harmonic behavior of the DUT at the specified input power is monitored. The setup used to perform these measurements is illustrated and explained below.

The input signal (f = 900 MHz for the low band (LB) or f = 1800 MHz for the high band (HB)) with a duty cycle of 25 percent is generated by the signal generator. The Power Amplifier (PA) amplifies the signal by roughly 50 dB to reach an input power level that is close to the required system power level. A circulator protects the output of the PA by terminating the reflected signal. Diplexers are used as a band pass filter (LB signals below 1 GHz can pass while harmonics generated by the PA will be terminated to ground). A directional coupler is connected before the DUT to measure the available input power with the help of a power meter. This calibrated input signal is then fed to the DUT. The output signal of the DUT is fed to a Diplexer, to filter out the low band part of the post-DUT signal including the fundamental frequency, and then to the spectrum analyzer. If the low band signal is not filtered out properly, the spectrum analyzer could generate H2/H3 from the LB signal and distort the H2/H3 signals coming from the DUT.

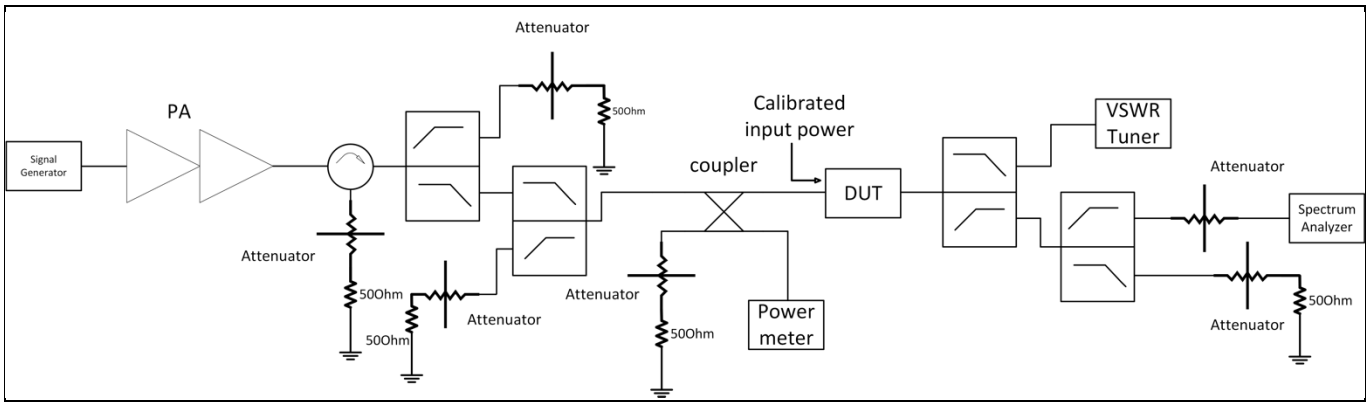


Figure 27 V_{RF} and harmonics measurement setup

3.4.4.1 V_{RF} measurement

For the V_{RF} measurements, the V_{RF} EVB is used, which allows the user to stress each channel individually. The maximum V_{RF} point is defined as the point where the harmonic level starts to increase exponentially. To perform this measurement, the device is set to isolation mode and placed in the setup shown below.

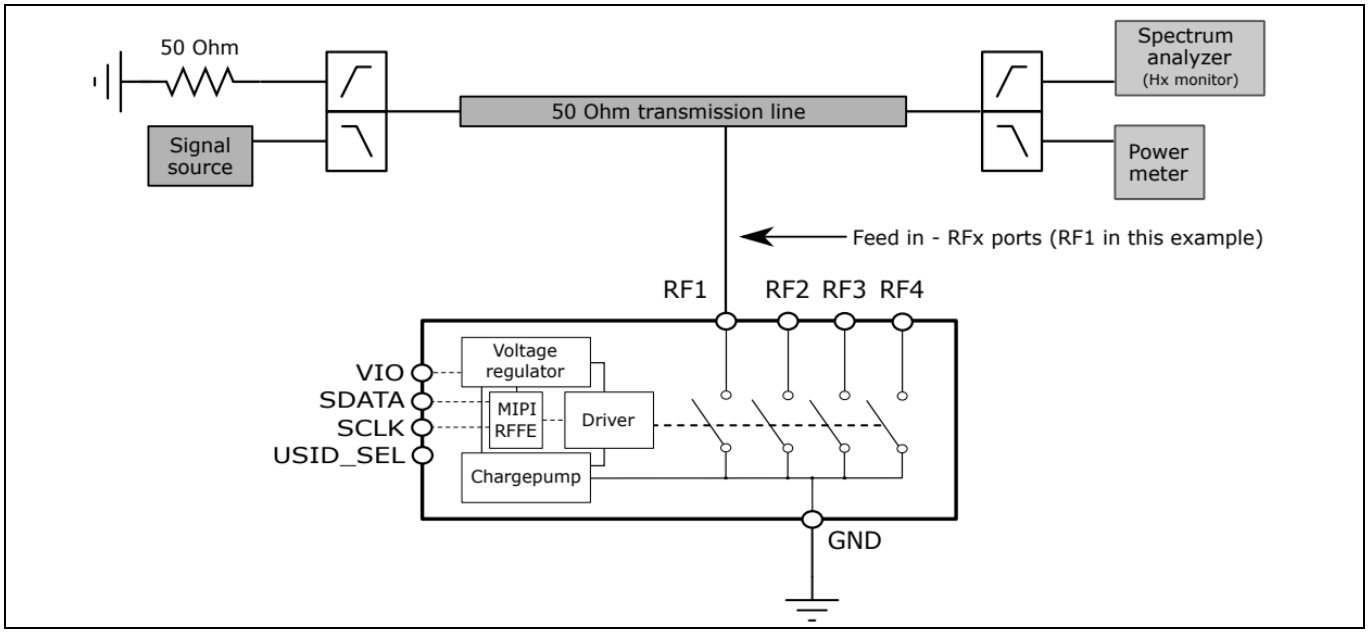


Figure 28 RF operating voltage measurement configuration in OFF mode

The input power must be increased steadily, while monitoring the harmonic behavior. At the maximum V_{RF} point of the DUT, the harmonics will start to increase drastically. This behavior is shown below.

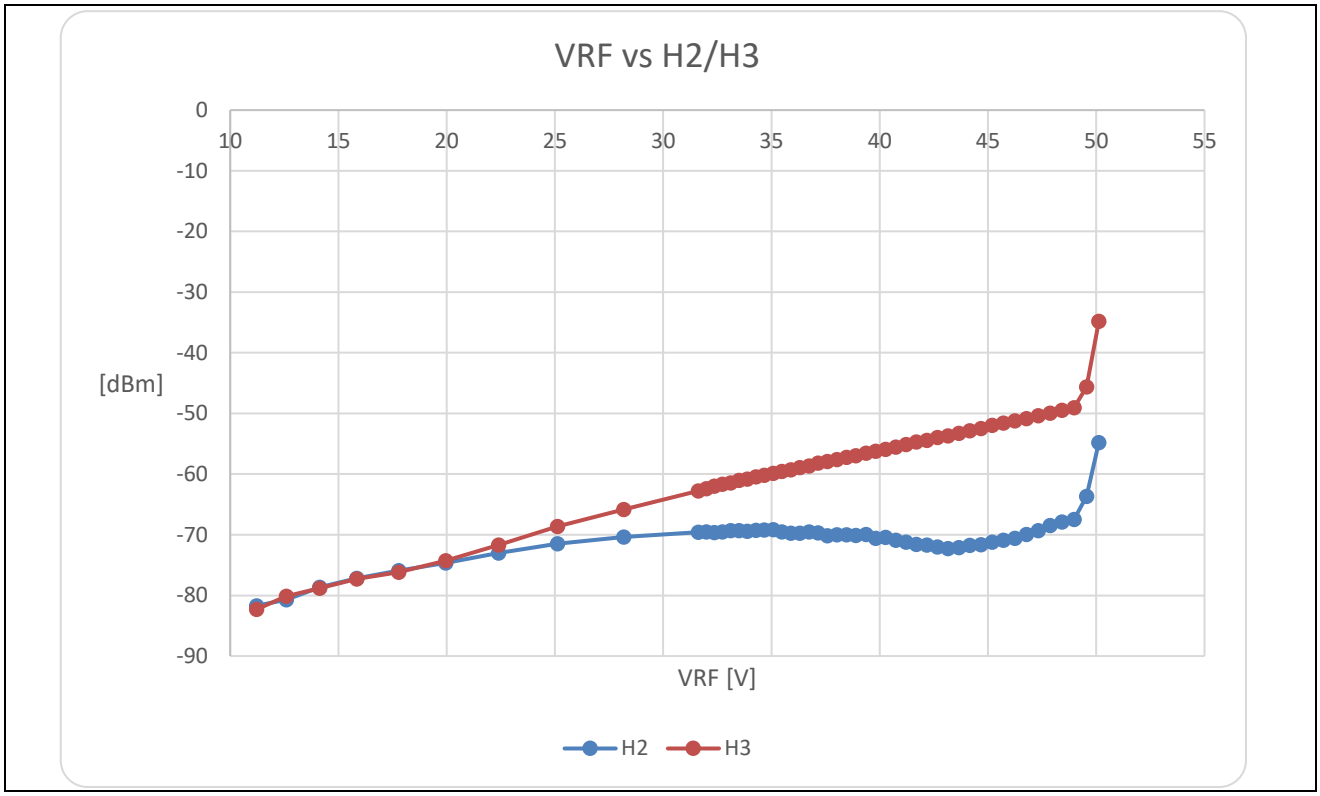


Figure 29 V_{RF} behavior of BGSA403ML10 in relation to the harmonics at 900MHz

3.4.4.2 Harmonics measurement

To measure the harmonic behavior, the V_{RF} board is required to monitor the signal of the device while in OFF mode as shown below.

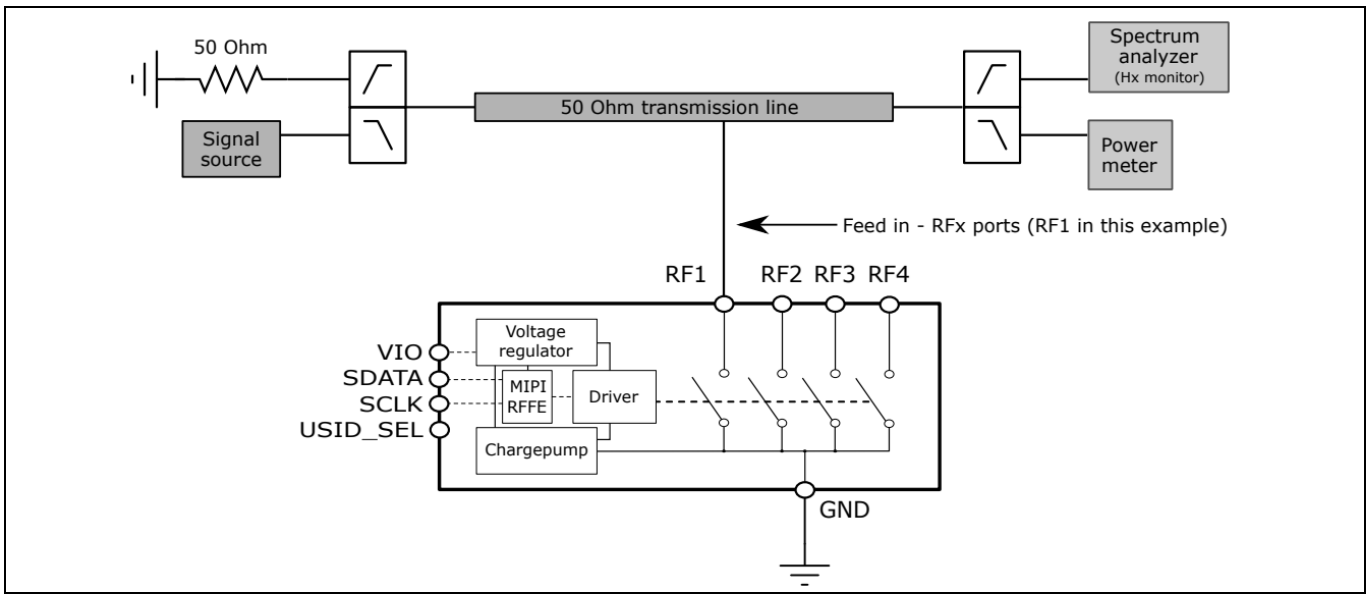


Figure 30 Harmonics measurement configuration – RFx in OFF mode

The calibrated input signal with a specific frequency and power level is fed to the port and the harmonic behavior is recorded for the desired power range. Below an example measurement of the harmonic behavior of BGSA403ML10 is shown.

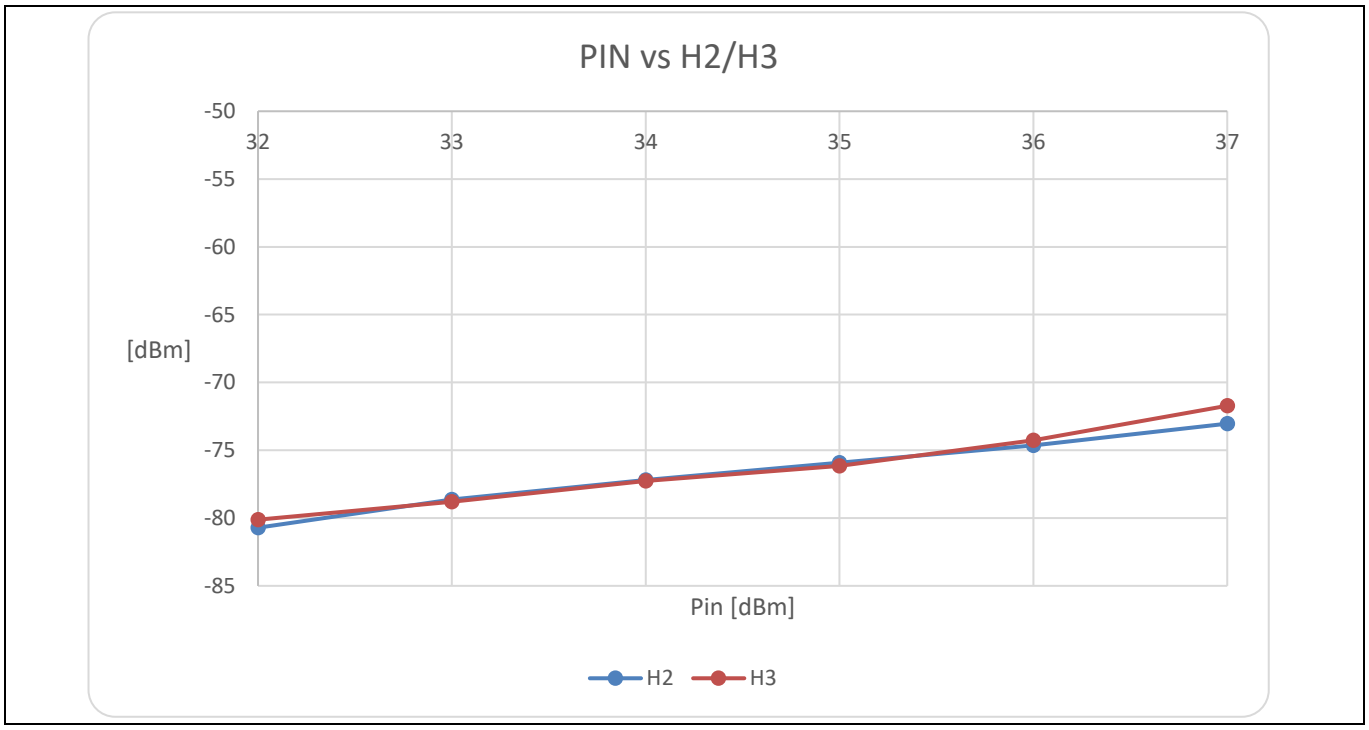


Figure 31 LB (900 MHz) harmonic behavior of BGSA403ML10 at 25°C

3.4.5 Switching time measurement

The switching time for an antenna tuner is the time it takes to fully complete a switching process. This process is initiated by a standard MIPI register write command.

Shunt device switching time behavior

The switching time behavior of shunt switches is different compared to the series switches. By turning the shunt switch on, the switch shorts the RF port to ground and therefore no RF signal is transmitted to the output. In this case, the RF amplitude at the output changes from high to low.

On the other hand, by turning the switch off, the switch behaves like an open circuit and the RF signal amplitude at the output changes from low to high.

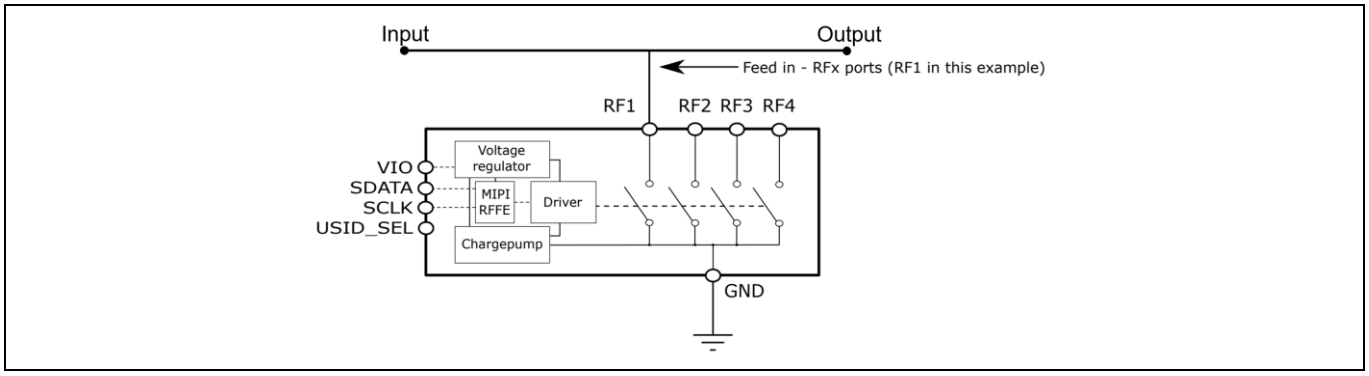


Figure 32 Switching time EVB configuration for shunt devices

Switching ON time: The ON time is the time it takes the RF signal at the output of the EVB to drop to 10 percent of maximum RF amplitude after 50 percent of the last rising edge of the clock signal (SCLK). This is the time it takes the switch to move from the OFF state to the ON state.

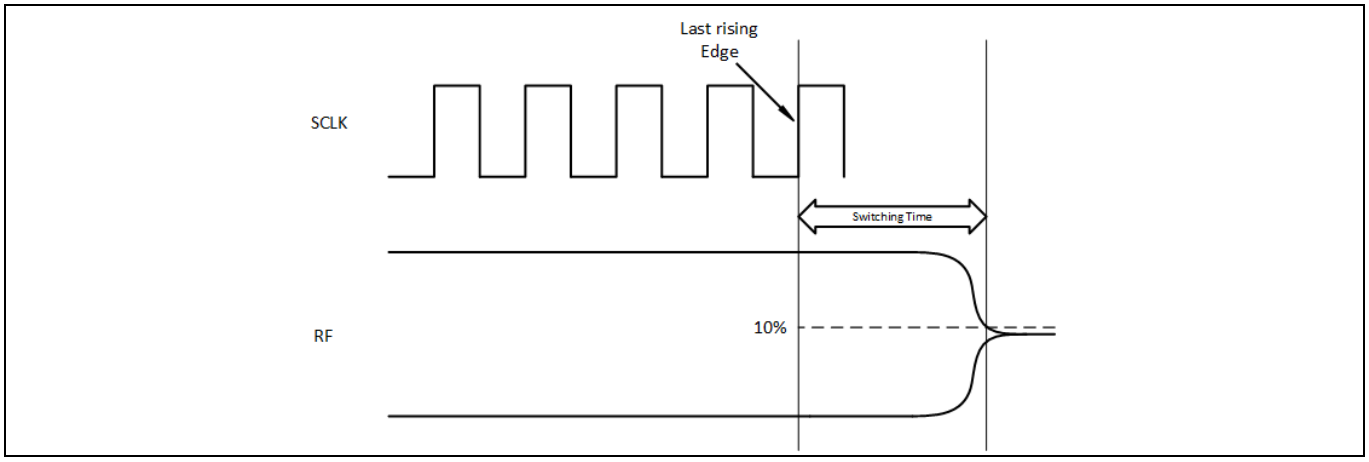


Figure 33 Switching ON Time

Switching OFF time: The OFF time is the time it takes the RF signal at the output of the EVB to rise to 90 percent of maximum RF amplitude after 50 percent of the last rising edge of the clock signal (SCLK). This is the time it takes the switch to move from the ON state to the OFF state.

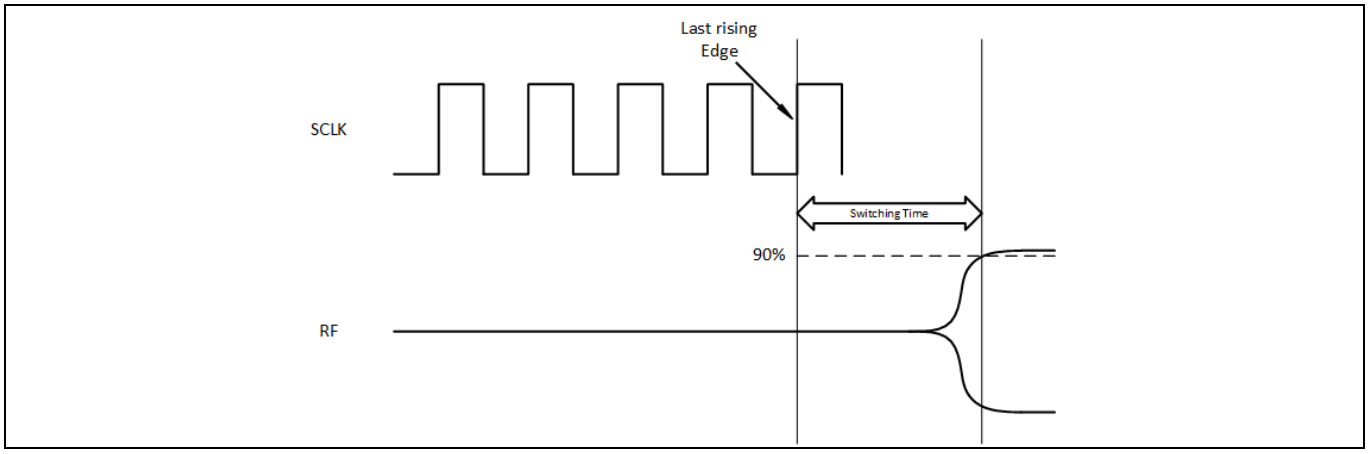


Figure 34 Switching OFF Time

Measurement setup

The figure below is showing the switching time measurement setup for BGSA403ML10. A RF input signal (RFIn) with 900MHz and a power level of 0dBm is used. In this switching time measurement, the VRF EVB has been used to measure the individual port performance.

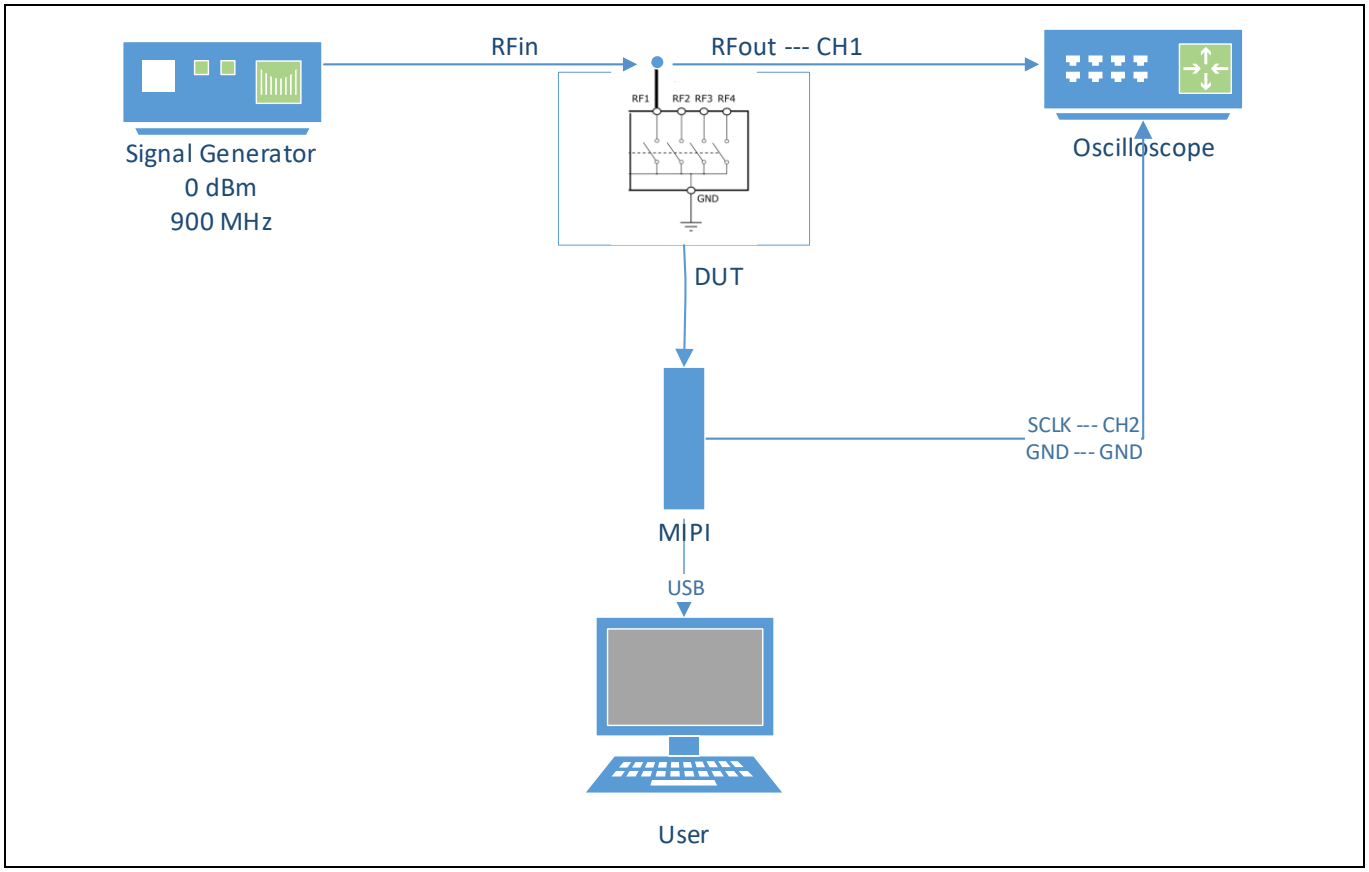


Figure 35 Switching time measurement setup

Measurement examples

The measurement examples of ON and OFF switching time for the BGSA403ML10 are shown below.

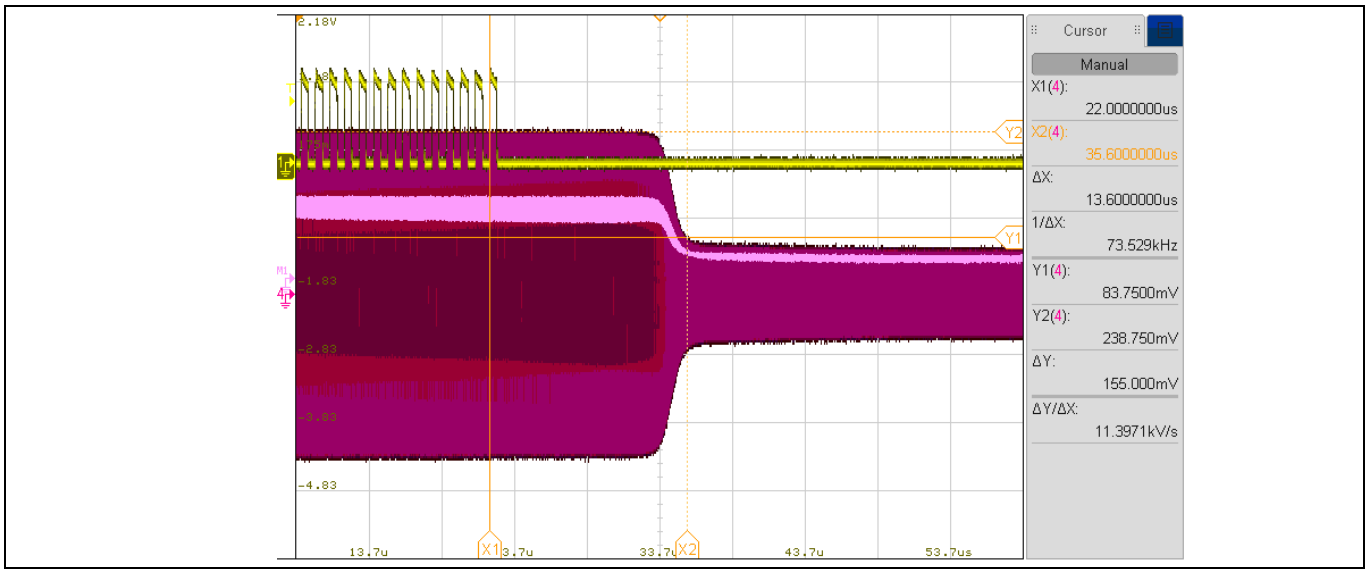


Figure 36 ON switching time (Isolation to RF1) of BGSA403ML10

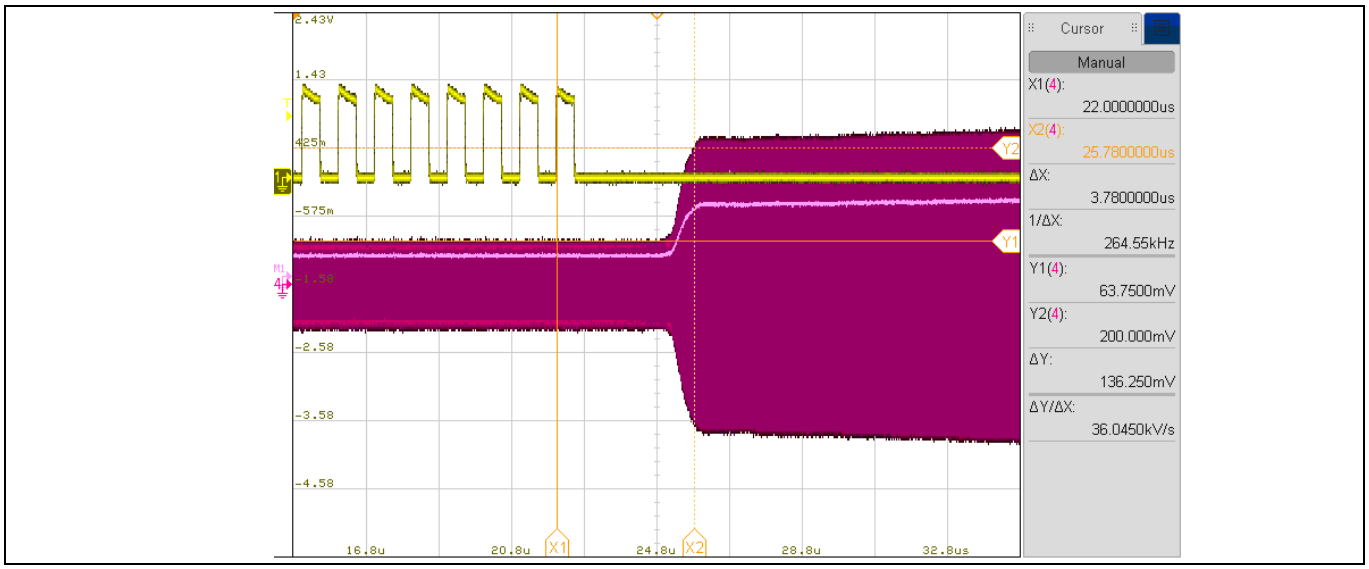


Figure 37 OFF switching time (RF1 to Isolation) of BGSA403ML10

4 Layout guidelines

In this chapter, some design guidelines for BGSA403ML10 are discussed.

There are a few recommendations of how the RF parasitics caused by the device during the PCB layout can be minimized, so that good antenna performance can be maintained. It is recommended that no ground plane is implemented under the RF transistor area. Also, the ground under the RF traces between BGSA403ML10 and the SMD tuning elements should be removed (see figure below). This layout design guide can also be applied to other similar Infineon antenna tuning devices.

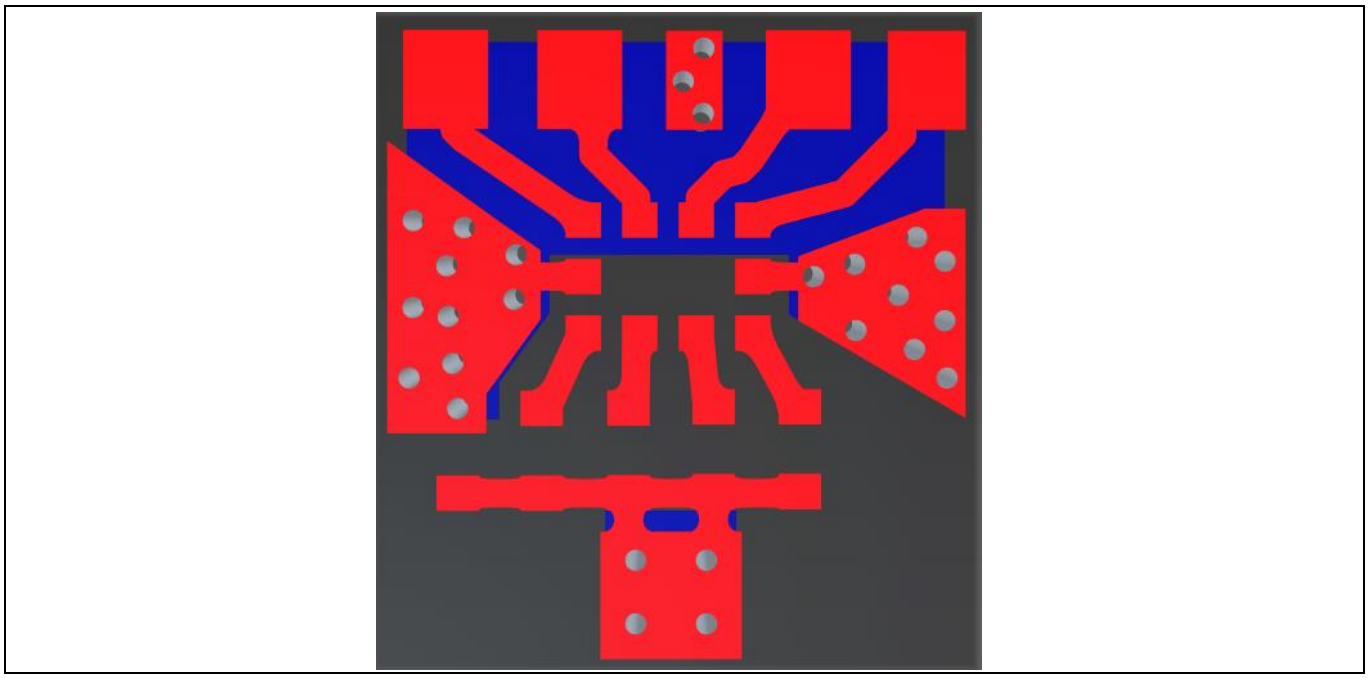


Figure 38 Top view of recommended draft PCB layout in device area

4.1 Trace impact on equivalent C_{OFF}

The trace length should be as short as possible. The longer trace will shift the C_{OFF} to a higher equivalent C value at the tuning elements as shown in the figure below. An example of how the traces could look in the application is shown in the 3D view of the recommended PCB layout shown above.

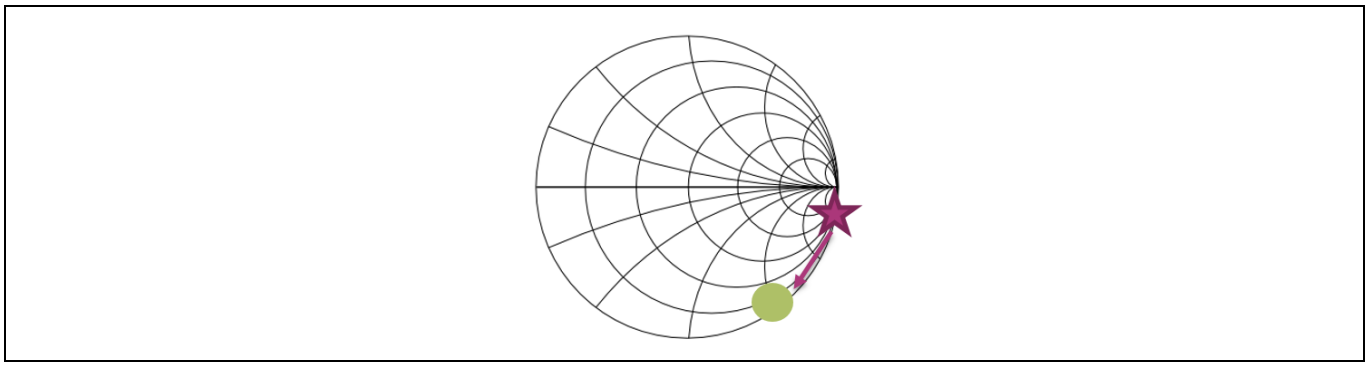


Figure 39 Impact of traces on the PCB on the C_{OFF}

The picture below shows the layout of an Infineon mini EVB that can be used to test the BGSA403ML10 in an application. By using flying cables, the mini EVB can be used to replace other components in the customer's system.

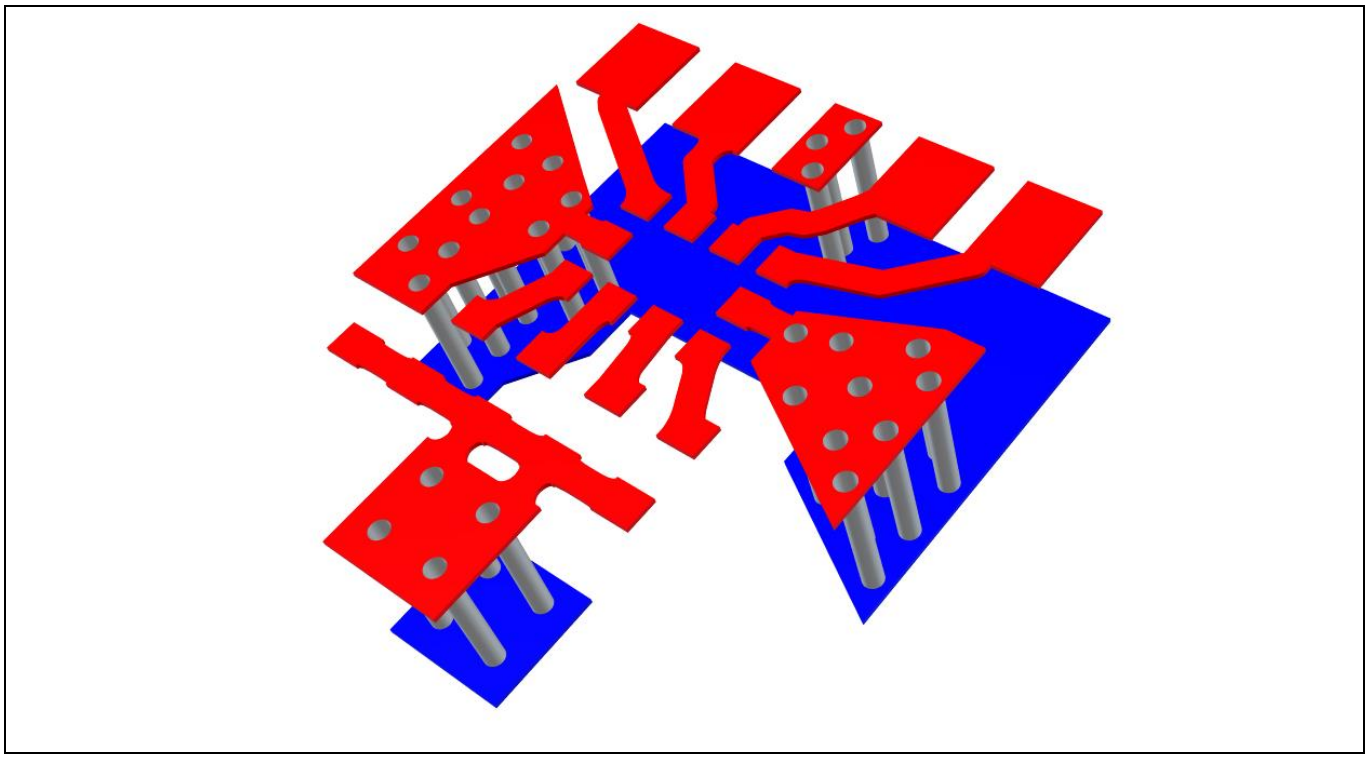


Figure 40 3D view of Mini EVB draft layout of BGSA403ML10

4.2 ESD recommendation

The device is designed to withstand 2 kV ESD human body model (HBM) performance in the worst case. To achieve higher SLT ESD levels it is recommended to use shunt inductors. The best compromise is the use of a 27 nH shunt inductor to achieve a higher SLT ESD robustness. The ESD shunt inductor should be placed as close as possible to the place where the ESD pulse enters the PCB.

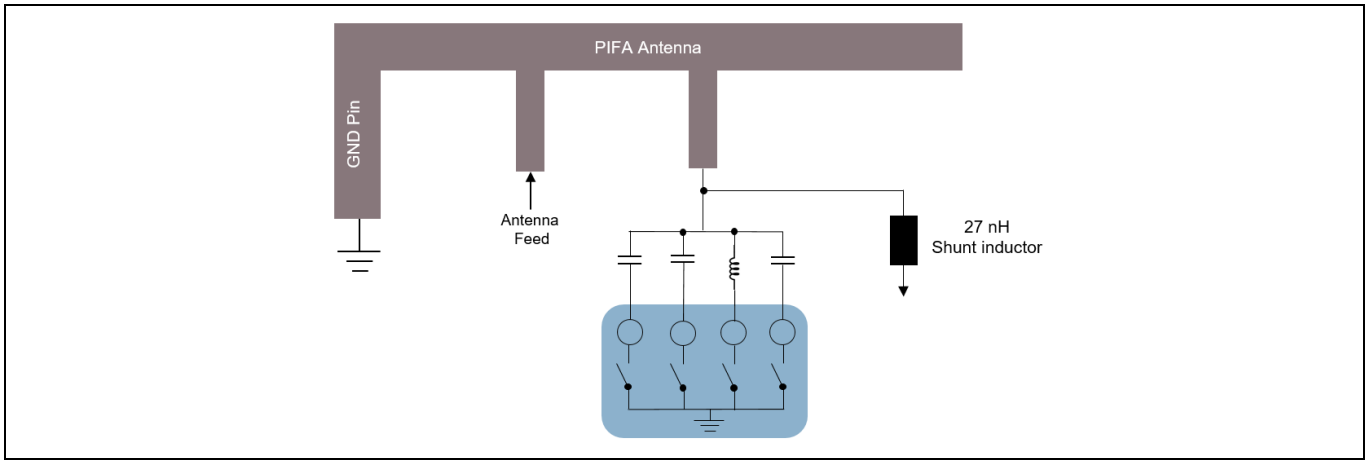


Figure 41 System level test ESD configuration

Table 1 Abbreviation table

EVB	Evaluation board
PCB	Printed circuit board
V_{RF}	RF voltage
C_{OFF}	OFF capacitance
R_{ON}	ON resistance
ESD	Electrostatic discharge
HBM	Human-body model
SLT	System level test
RF	Radio frequency
RFFE	RF Front-End

5 Authors

Ishrat Mahbub, RF application engineer of business unit RF and Sensors.

Lukas Rauh, Senior RF application engineer of business unit RF and Sensors.

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Document version	Date of release	Description of changes
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