# AN97119

# EZ-USB® GX3™ Hardware Design Guidelines

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**Associated Part Family: CYUSB3610**

**Related Application Notes: AN97116**

AN97119 provides hardware design and PCB layout guidelines for EZ-USB® GX3™, Cypress's high-performance SuperSpeed USB 3.0 to Gigabit Ethernet Bridge Controller. These guidelines will help to ensure best performance with respect to signal integrity and full electrical compliance with the USB 3.0 specification. This application note covers USB connector Type-A and Type-C based reference designs.

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## 1 Introduction

EZ-USB GX3 is a SuperSpeed USB to Gigabit Ethernet Bridge Controller that provides Ethernet connectivity over USB. GX3 is a low-cost, high-performance, plug-and-play solution that is easy to design. It enumerates as a standard network adapter on the PC, enabling existing software applications to be reused, and accelerates time to market.

GX3 is a single-chip bridge controller with an integrated USB 3.0 device controller, Energy Efficient Ethernet (EEE) physical layer (PHY) working at 10/100/1000 Mbps, and internal one-time programmable memory for configuration in a 68-pin QFN package. It supports dynamic power management to reduce power consumption during idle or low Ethernet traffic and enable USB disconnect when the Ethernet cable is unplugged. GX3 also supports a serial EEPROM interface to store USB descriptors, MAC ID, and so on in the external serial EEPROM.

This application note provides guidelines on external component selection, schematic design, and PCB design/layout for designing with the EZ-USB GX3 SuperSpeed USB to Gigabit Ethernet Bridge Controller. It is recommended that you read this application note before starting a hardware design.

GX3 is available in a 68-pin QFN (8 mm x 8mm) RoHS/REACH compliant package. A reference schematic for the CY4701 EZ-USB GX3 Reference Design Kit (RDK) is available at www.cypress.com/gx3.

# 2 Schematic Design Requirements

This section explains the schematic design requirements and PCB layout considerations for GX3.

## 2.1 Four-Layer PCB Design

Cypress recommends using a four-layer PCB for designing GX3 based solutions. Figure 1 shows the placement of the power, ground, and other planes of a four-layer PCB design using the GX3 SuperSpeed USB to Gigabit Ethernet Bridge Controller. Here the magnetic signals consist of the Ethernet differential pair of signals that run from the GX3 to the RJ45 connector.

Figure 1. Four Layers of GX3 PCB

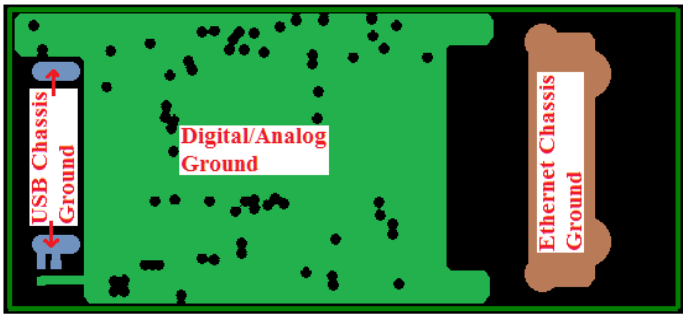
| | | |
|---|---|---|
| Layer 1 | Component (Top) | Magnetic and other signals |
| Layer 2 | Ground | Digital/analog ground planes |
| Layer 3 | Power | Digital/analog power planes |
| Layer 4 | Component (Bottom) | Magnetic and other signals |

## 2.2 Power and Ground Planes

GX3 operates with two external power supplies: 3.3 V and 1.2 V. Following are the recommendations for power and ground planes.

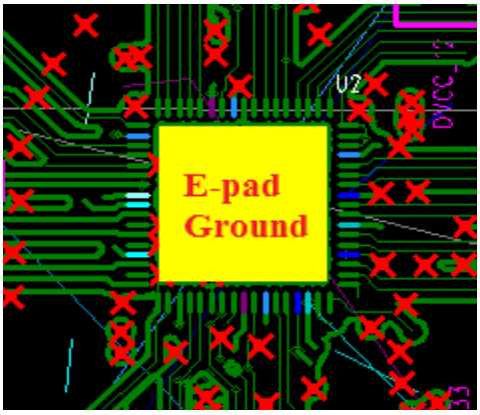
- Combine digital ground and analog ground planes to form one large ground plane to help noise dissipation, as shown in Figure 2.

Figure 2. Typical Digital/Analog/Chassis Ground Planes




- Connect the GX3 DVSS E-pad to the digital ground plane to dissipate the heat and reduce the chip's operating temperature, as shown in Figure 3.

Figure 3. E-Pad Ground



- Isolate the USB chassis ground and the digital ground with a 1-MΩ resistor and a ferrite bead in parallel (see Figure 4). Figure 4 represents a Type-A USB 3.0 to Gigabit Ethernet dongle reference design, and Figure 5 represents a Type-C USB 3.1 (Gen 1, 5.0 Gbps) to Gigabit Ethernet dongle reference design. For details on USB 3.1 specification, see www.usb.org. Isolate the Ethernet chassis ground and the digital ground with a 1-MΩ resistor and a 0.1-µF decoupling capacitor (see Figure 6). The gap between the chassis ground and digital ground must be wider than 35 mils. The isolation between the chassis ground and the digital ground helps to reduce the EMI.

Figure 4. Type-A USB 3.0 Chassis Ground Isolation

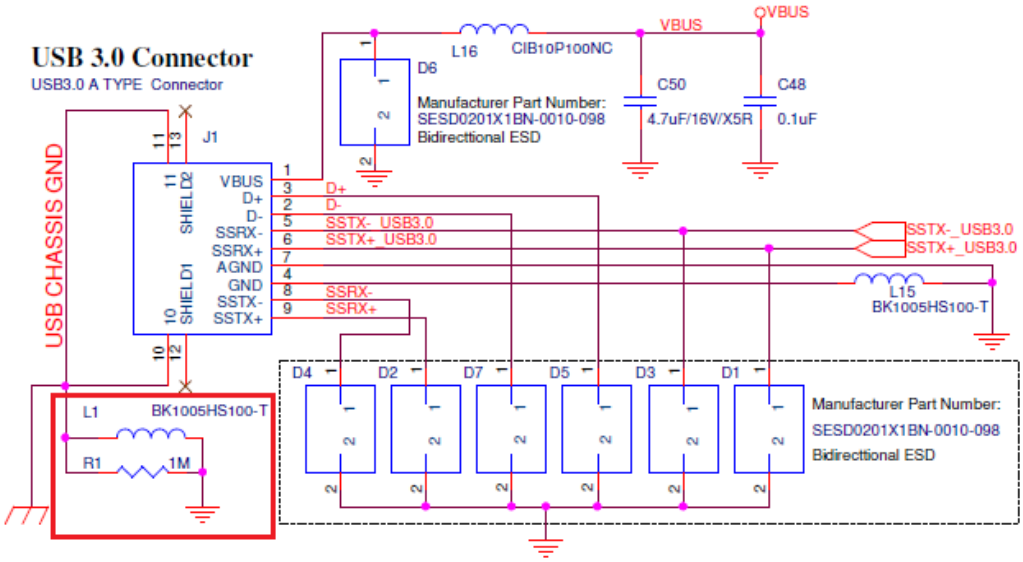
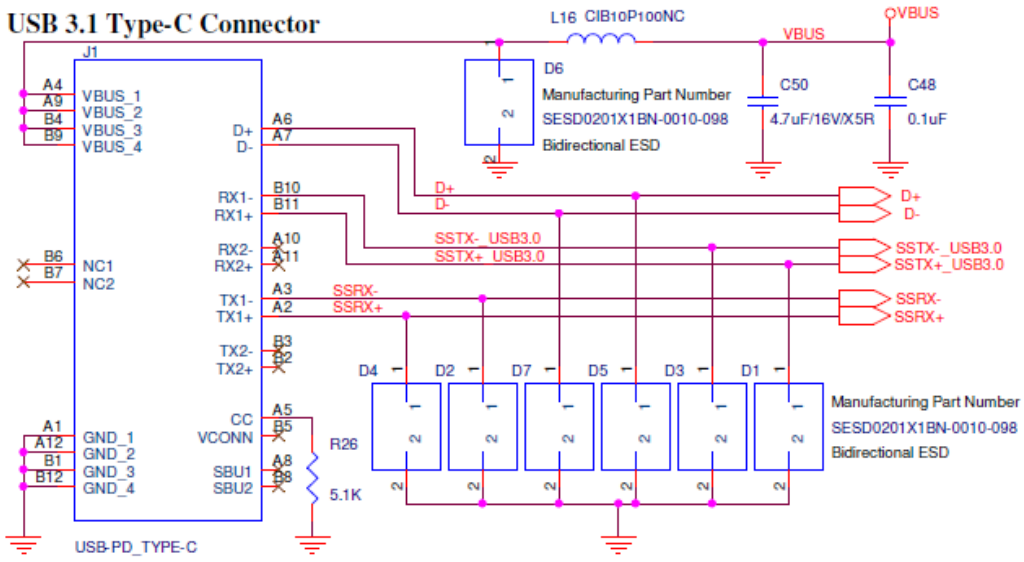
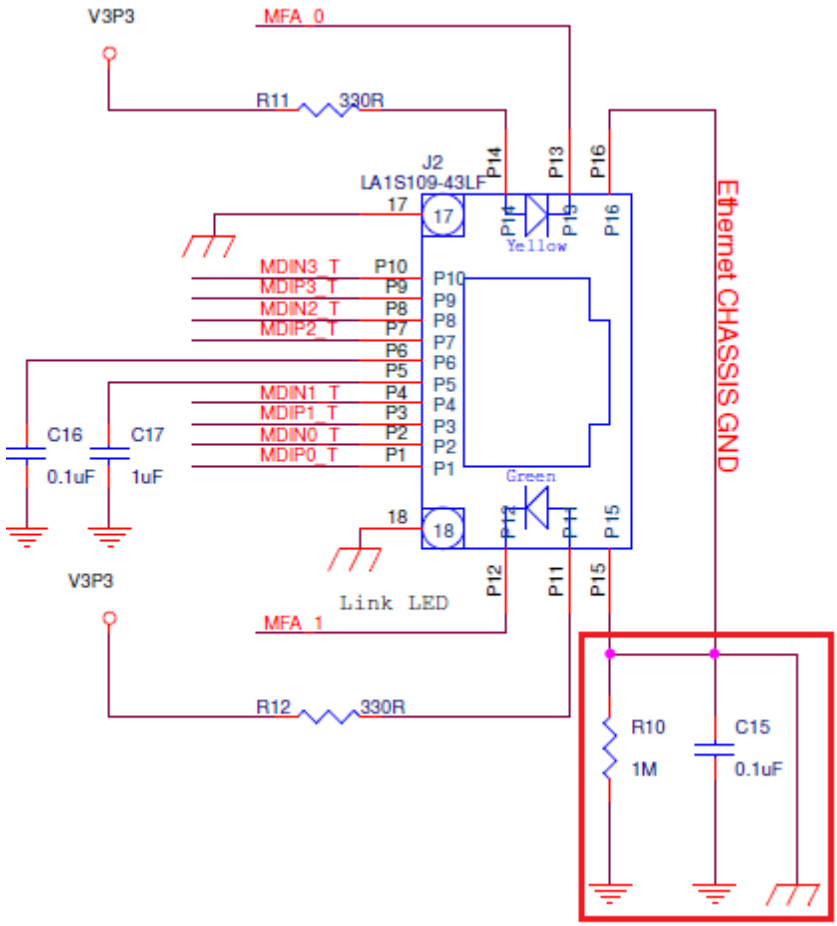



Figure 5. Type-C USB 3.1 Schematic



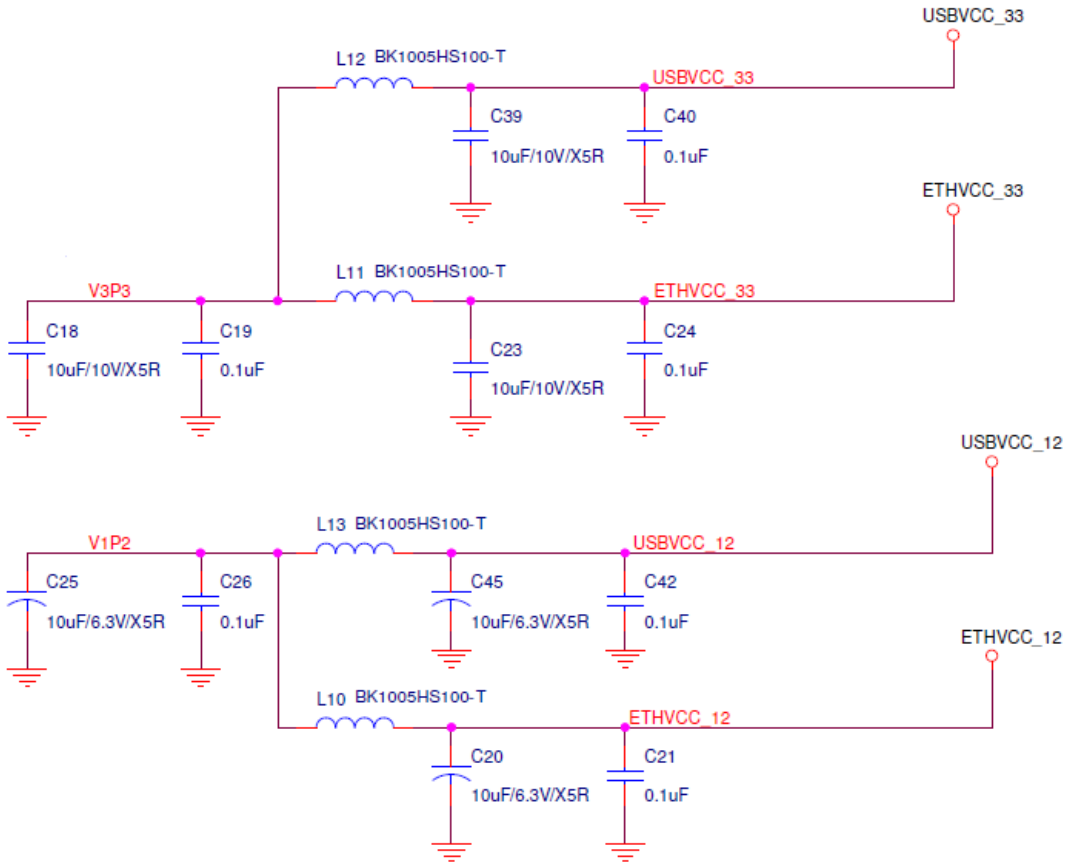

For information on Type-C signal definitions and detection of the Ethernet dongle's Type-C port (also known as Upstream Facing port (UFP)), see *Type-C Signal Definition* and *Configuration Channel: Cable Detect* sections in AN96527.

Figure 6. Ethernet Chassis Ground Isolation



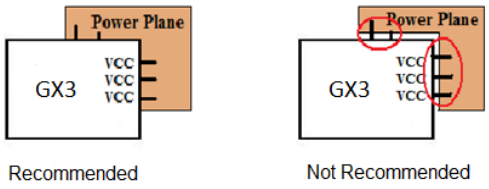

- Handle the USB and Ethernet power planes for different voltages separately for GX3 silicon and peripheral components. To see the exact layout pattern, refer to www.cypress.com/gx3 for the CY4701 GX3 RDK PCB layout and Gerber files.
- Separate the USB and Ethernet power planes with a ferrite bead to isolate the noise source, and implement all power planes with a large decoupling capacitor (10 µf) to provide a stable power source, as shown in Figure 7.

Figure 7. Power Plane Isolation Using Ferrite Bead




- Implement all power pins with a decoupling capacitor of 0.1 µf to suppress high-frequency noise. Place the capacitor close to the respective GX3 power pins.
- Provide a power plane below the GX3 silicon to enable the VCC pins to be connected to the power plane, as shown in Figure 8.

Figure 8. Power Plane Contact to VCC Pins




# 3 Crystal Selection

GX3 uses 25 MHz as the clocking source. Figure 9 shows the connection of the SMD crystal to the GX3. The recommended crystal part number is NXK25.000AC12F-KAB6 SMD 25-MHz crystal. Table 1 lists the crystal requirements.

Figure 9. Crystal Circuit

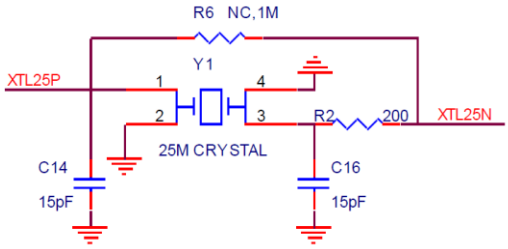



Table 1. Crystal Requirements

| Parameter | Specification | Unit |
|---|---|---|
| Nominal Frequency (Fo) | 25.000000 | MHz |
| Oscillation Mode | Fundamental | – |
| Frequency Tolerance (@ 25 °C) | ±30 | ppm |
| Frequency Stability Over Operating Temperature Range | ±30 | ppm |
| Equivalent Series Resistance (ESR) | 70 max. | ohm |
| Load Capacitance (CL) | 12 | pF |
| Drive Level | 350 | µW |
| Operation Temperature Range | 0–70 | ºC |
| Aging | ±3 | ppm/year |

**Notes:**

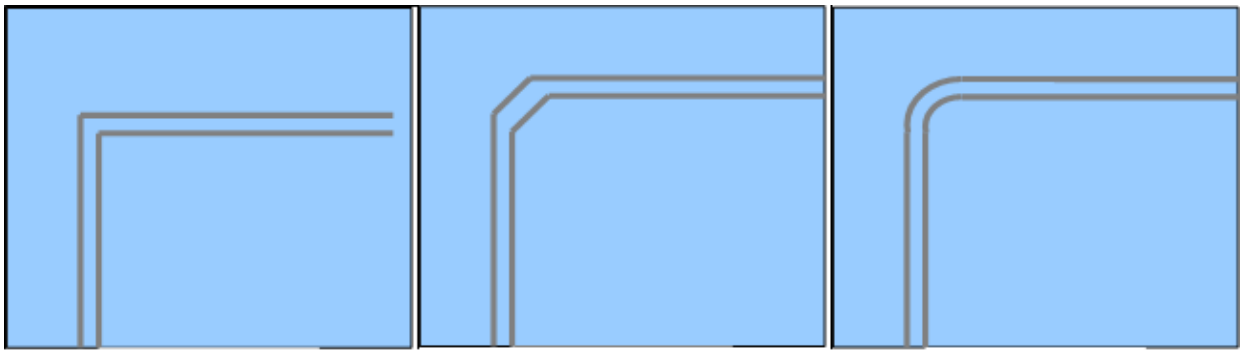
1. The 1-MΩ feedback resistor (R6) is optional for the GX3 25-MHz crystal circuit. It is useful to bias the input of the inverting amplifier. The provision is given in the layout to cater crystals from different sources.
2. The 200-Ω series resistor is added to avoid overdriving the crystal.
3. The XTALOUT 25-MHz clock output signals should be within 25 MHz ±50 ppm.

# 4 PCB Layout Guidelines

GX3 includes SuperSpeed and Hi-Speed USB lines. Use the following best practices when routing SuperSpeed and Hi-Speed lines.

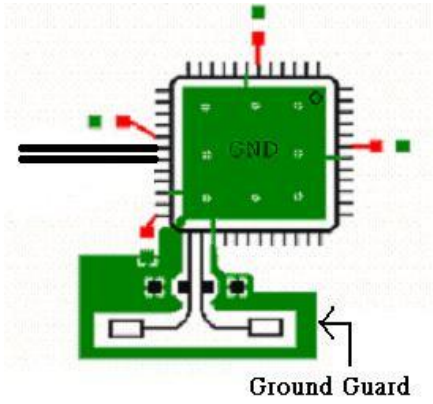
- Route the USB differential signals with a minimum trace length—as short as possible.
- Do not route the USB differential signal traces too close to the clock or noisy digital signals.
- Minimize the use of vias in the differential pair paths as much as possible. If this is not practical, make sure that the same type of vias and their placement are used for both signals in a pair. Place vias as close to the GX3 device as possible.
- Match the lengths of the differential pair traces (SSTX±/SSRX±/D±). There should be a difference of less than 8 mils between an SS differential pair signal and its complement. The USB 2.0 differential pairs should not exceed 50 mils of relative trace length difference.
- Place AC coupling capacitors close to each other to minimize extra trace length.
- Avoid routing the SuperSpeed and Hi-Speed signals close to the edge of the PCB or power planes.
- Avoid any stubs and remove any routing that causes signal discontinuity and a severe EMC noise issue.
- Do not put any metal between the SuperSpeed differential signal pair traces when using the USB 3.0 receptacle connector with pins stabbing the PCB.
- To minimize crosstalk, do not route the signal traces between the SSTX±/SSRX±/D± pairs close to each other.
- The trace spacing between SuperSpeed and Hi-Speed signals should be 8 mils.
- Route the differential pair traces parallel to one another and as close as possible. The traces should be symmetrical.
- Isolate different USB differential pairs by the appropriate wide ground traces.
- To ease routing, you can swap the polarity of the SS differential pairs. This means that SSTX+ can be routed to SSTX– or SSRX– can be routed to SSRX+ using the GPIO[2] pin. Refer to the “Settings” section of the GX3 datasheet for more details.
- Avoid any 90-degree turn in trace routing; instead, use two 135-degree turns, as shown in Figure 10.

Figure 10. Recommended USB Trace Routing



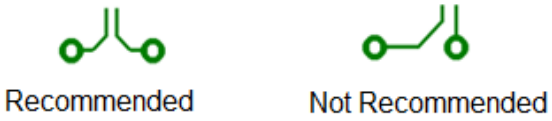

- The XTAL (oscillator) traces should be surrounded by a ground guard (Figure 11) to prevent interference with other signal wires. You can attain a better EMI effect with a one-piece GND underneath the IC, furnished with PTH holes to enlarge the GND area.

Figure 11. Ground Guard for Crystal Traces




- The XTAL traces should be symmetrical and parallel for a better signal and better EMI protection, as illustrated in Figure 12.

Figure 12. Recommendation for Clock Traces




- USB signal traces should be placed in parallel, as shown in Figure 13.

Figure 13. USB Signal Traces



## 4.1 PCB (FR4 Material) and Impedance

The recommended stackup for a standard 62-mil (1.6-mm) thick PCB is shown in Figure 14. When this stackup is used with two parallel traces, each with a width (W) of 5.75 mils and a spacing (S) of 12 mils, the calculated differential impedance is 90 Ω. Figure 14 shows the layers in the layout of the GX3 RDK.

Figure 14. Stackup Details

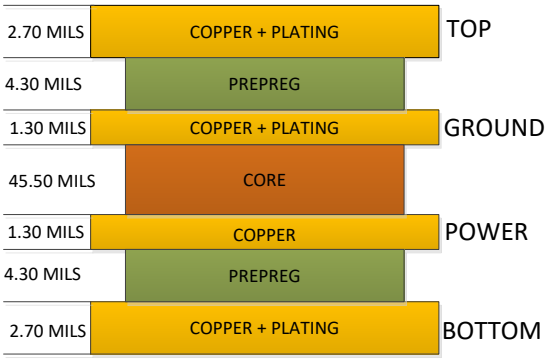



Table 2 gives the recommended values for the PCB parameters shown in Figure 15.

Figure 15. Cross-Sectional View of PCB and Its Parameters

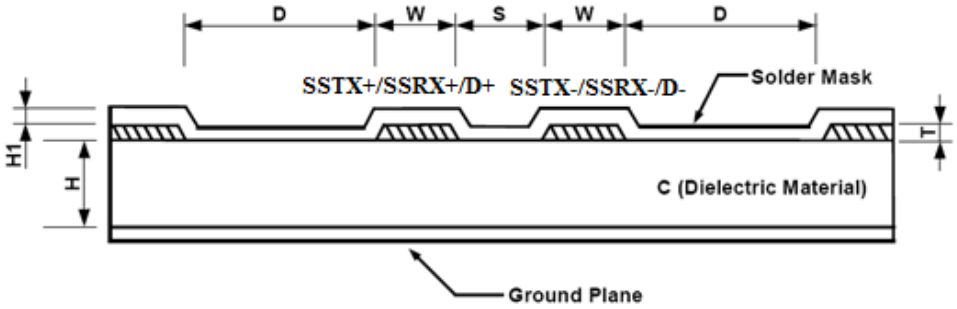



Table 2. PCB and Impedance Requirements

| Parameter | Recommended Value | Unit |
|---|---|---|
| W | 8 | mil |
| S (SSTX+/SSRX+/D+ to SSTX–/SSRX–/D–) | 8 | mil |
| T (thickness of the trace) | 1 | ounce copper |
| D (ground separation) | ≥ 30 | mil |
| Dielectric thickness, distance of trace from the ground plane (board thickness) | ≈ 63 | mil |
| USB differential impedance between SSTX+ and SSTX–, SSRX+ and SSRX–, and D+ and D– traces | 90 | ohm |
| USB differential impedance between SSTX+/SSTX–/SSRX+/SSRX–/D+/D– trace and GND | 45 | ohm |

**Note:** You can use the trace width of the SSTX+/SSTX–/SSRX+/SSRX–/D+/D– traces to fine-tune the USB differential impedance value (a wider trace has a smaller impedance value). If the PCB manufacturer provides the time-domain reflectometry (TDR) measurement, it helps you control the PCB impedance. TDR measures the reflections that result from a signal travelling through a transmission environment of some kind—a circuit board trace, a cable, a connector, and so on. You can fine-tune the width of the USB traces with 90-Ω impedance first and then fine-tune the width of the Ethernet traces with 100-Ω impedance.

## 4.2 USB Trace Routing for USB 3.0 PHY and Connector

Figure 16 and Figure 17 show the trace routing for SuperSpeed and Hi-Speed signals.

Figure 16. USB 3.0 SSTX±/SSRX± Trace Routing (Top Level)

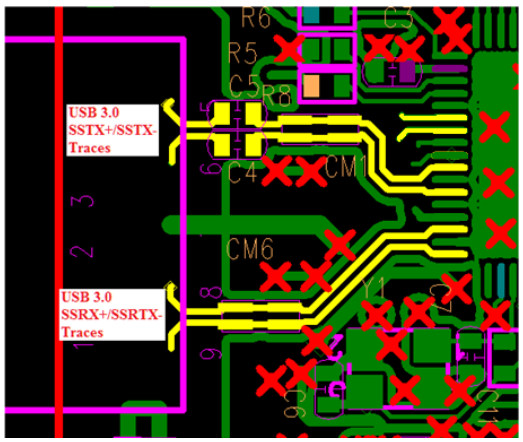
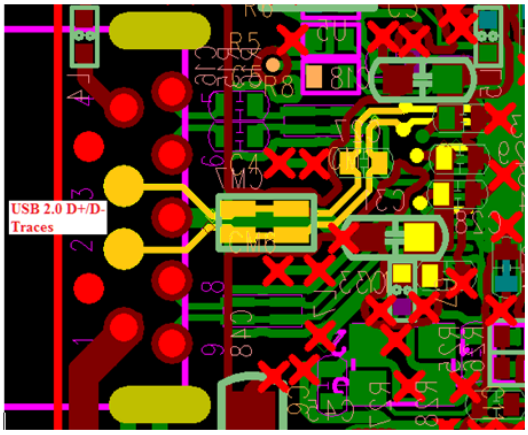



Figure 17. USB 2.0 D+/D– Trace Routing (Bottom Level)

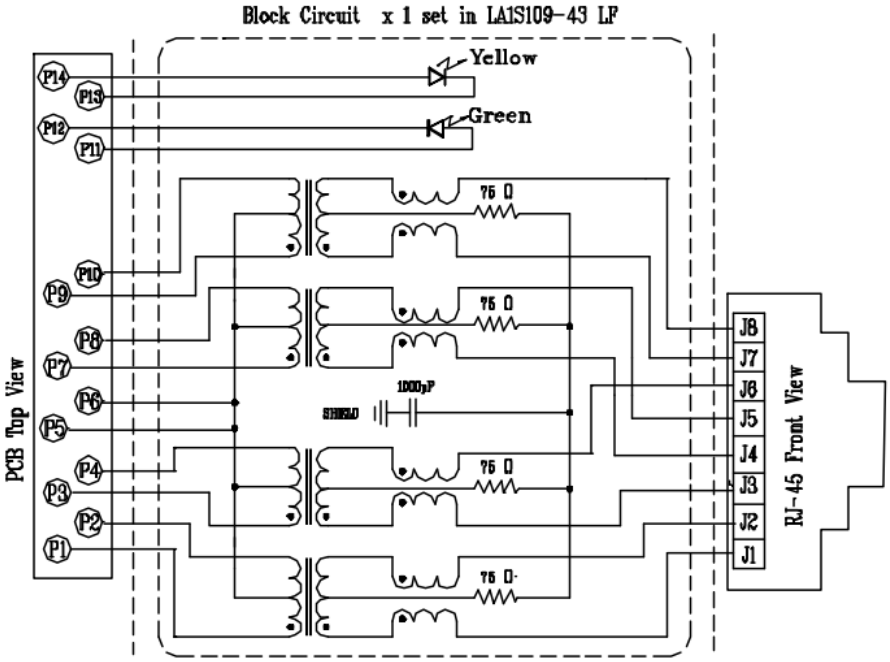


## 4.3 Ethernet Magnetic Selection

Figure 6 shows a reference Ethernet magnetic circuit (a single RJ45 connector integrated 10/100/1000M Base-T magnetic with Turns Ratio 1CT:1CT) used in the GX3 RDK. It is recommended to use the same.

The GX3 RDK uses an RJ45 connector (vendor: Bothhand LA1S109-43), as shown in Figure 18, with an integrated 10/100/1000M Base-T magnetic.

Figure 18. Bothhand LA1S109-43 RJ45 Connector

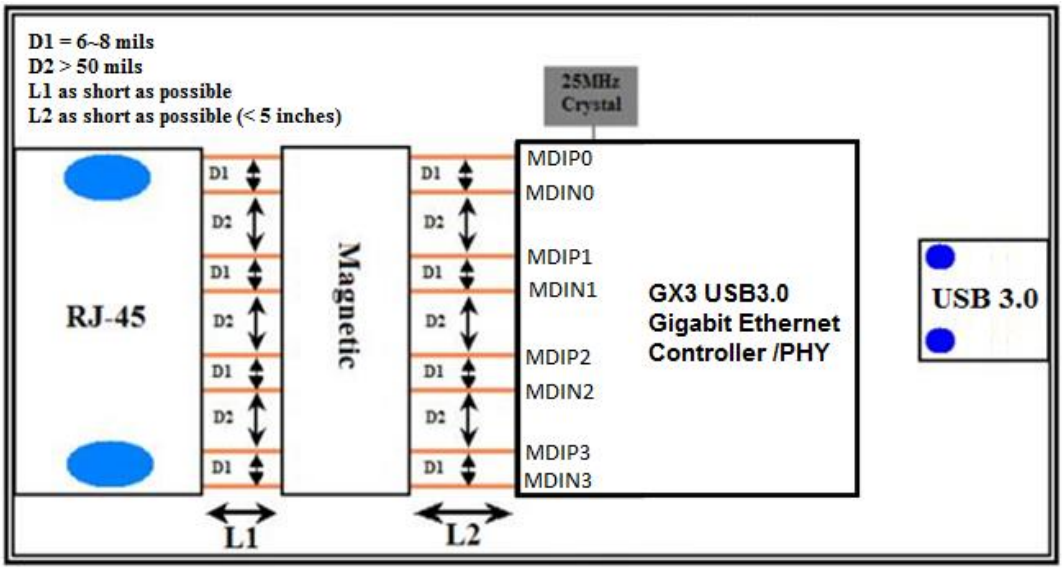


## 4.4 Ethernet Magnetic Layout Requirements

This section describes some general Gigabit Ethernet layout considerations for the differential signals of the Gigabit Ethernet controller/PHY, Gigabit Ethernet magnetic, and RJ45 connector.

All trace routes from the Gigabit Ethernet controller/PHY, Gigabit Ethernet magnetic, and RJ45 connector should be as short as possible. It is a best practice to maintain the same length for all differential pair signal traces, as shown in Figure 19. The design should have less signal crosstalk and a solid ground plane.

Figure 19. Gigabit Ethernet Differential Pair Layout

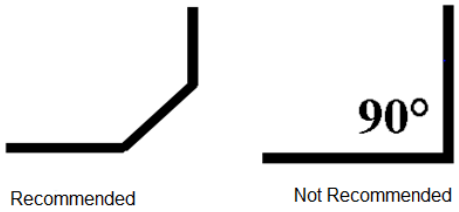



## 4.5 Ethernet Magnetic Layout Checklist

- The ideal Ethernet differential impedance between the MDIP0 and MDIN0, MDIP1 and MDIN1, MDIP2 and MDIN2, and MDIP3 and MDIN3 traces should be 100 Ω. The Ethernet differential impedance between the MDIP0 (or MDIN0, MDIP1, MDIN1, MDIP2, MDIN2, MDIP3, MDIN3) trace and GND should be 50 Ω respectively. You can use the trace width of the MDIP0/MDIN0/MDIP1/MDIN1/MDIP2/MDIN2/MDIP3/MDIN3 traces to fine-tune the Ethernet differential impedance value. A wider trace has a smaller impedance value. If the TDR measurement is known (provided by the PCB manufacturer), it helps to control the PCB impedance.
- Keep the crystal/oscillator clock source and the switching noises from digital signals away from the MDIP0/MDIN0, MDIP1/MDIN1, MDIP2/MDIN2, and MDIP3/MDIN3 differential pairs. Moreover, the crystal/oscillator is sensitive to stray capacitances and noise from other signals, so place the crystal far away from I/O ports, high-frequency signal traces, the magnetic, board edges, and so on.
- Place the Ethernet magnetic as close as possible to the RJ45 connector.
- Place the GX3 as close as possible to the magnetic. If there are some limitations on the PCB layout, the trace length from the GX3 to the magnetic should be no longer than 5 inches. Double-check this by running full network functionality testing.
- Route the MDIP0/N0, MDI1P1/N1, MDIP2/N2, and MDIP3/N3 differential pairs as close as possible. The trace spacing D1 (shown in Figure 19) between the MDIP0 and MDIN0, MDIP1 and MDIN1, MDIP2 and MDIN2, and MDIP3 and MDIN3 pairs should be in 6~8 mils.
- Keep the trace length difference between the MDIP0 and MDIN0 (or MDIP1 and MDIN1, MDIP2 and MDIN2, MDIP3 and MDIN3) pair within 200 mils.
- The spacing D2 (shown in Figure 19) should be larger than 50 mils. If this cannot be achieved, the D2 spacing should be kept as large as possible.
- Route the MDIP0/N0, MDI1P1/N1, MDIP2/N2, and MDIP3/N3 differential pairs as straight as possible, and keep the differential pairs parallel to each other.
- Isolate each Ethernet differential pair from other pairs with wide ground traces.

- Avoid using vias on the traces of the MDIP0/N0, MDI1P1/N1, MDIP2/N2, and MDIP3/N3 differential pairs. If the PCB layout cannot do without vias on the differential pairs, match the vias to keep the differential pairs balanced.
- Do not place the power plane and digital ground plane under the magnetic and RJ45 connector.
- Avoid routing the signal trace with a right angle; instead, route it with multiple 135-degree angles, as shown in Figure 20.

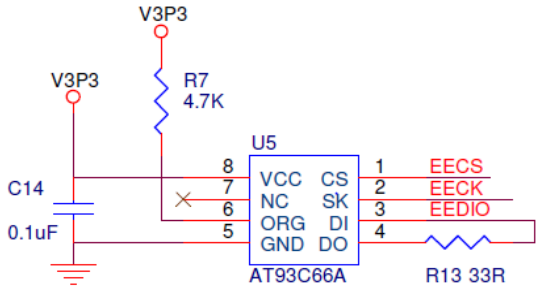
Figure 20. Recommended Signal Trace Angle



# 5 EEPROM Selection

GX3 supports the 3.3-V to 5-V 16-bit mode 93C56/93C66 serial EEPROM. The GX3 auto-loading EEPROM function can support only the instruction set format of 93C56/93C66, not 93C46. This is because the Address field of the 93C46 instruction set is A0–A5 for 16-bit data access, but the Address field of the 93C56/93C66 instruction set is A0–A7 for 16-bit data access. Figure 21 shows the reference EEPROM circuit used in the GX3 RDK.

Figure 21. 93C56A or 93C66A EEPROM




When the GX3 device is powered on, it checks for valid data in the EEPROM. If the EEPROM data is invalid, GX3 will load the internal default settings to communicate with the USB Host controller during enumeration. The default settings inside the GX3 silicon help you to program/update the EEPROM content using a PC (through a programming utility) during the testing or manufacturing process.

# 6 QFN Package PCB Layout Considerations

The QFN package is designed to provide superior thermal performance through an exposed thermal pad (E-pad) on its bottom surface. This provides an extremely low thermal resistance path between the die and the exterior of the package. You can easily mount the package using standard PCB assembly techniques and remove and replace it using standard repair procedures.

## 6.1 Solder Masking Design Considerations

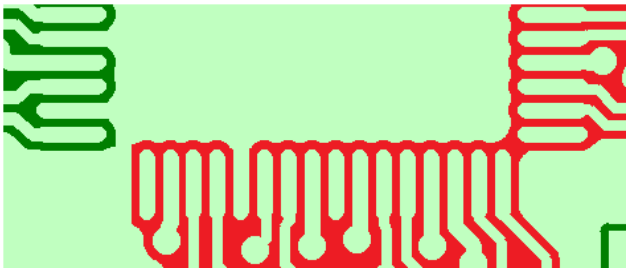
The pads on the PCB are either solder mask defined (SMD) or non solder mask defined (NSMD).

- SMD: Solder mask openings are smaller than the metal pads.
- NSMD: Solder mask openings are larger than the metal pads.

The SMD pads are recommended for the single-row QFN package with a center thermal pad, such as the GX3 QFN package. The NSMD pads are recommended for the multirow QFN package, since the copper etching process offers tighter control than the solder masking process and improves the reliability of solder joints.

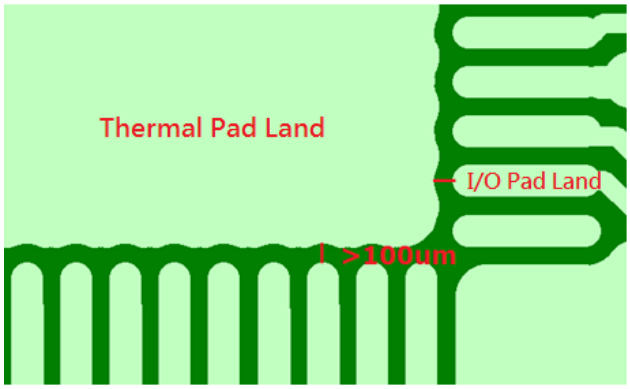
Typically, each land pad on the PCB should have its own solder mask opening, with a web between the adjacent pads. However, for a 0.4-mm pitch width part with a 0.23-mm I/O land pad width, the PCB space may not be available for a proper solder mask web between the adjacent pads. In practice, designers can use one big solder mask opening for all the pads on one side of the QFN package, as shown in red in Figure 22.

Figure 22. Solder Mask Opening (Shown in Red)



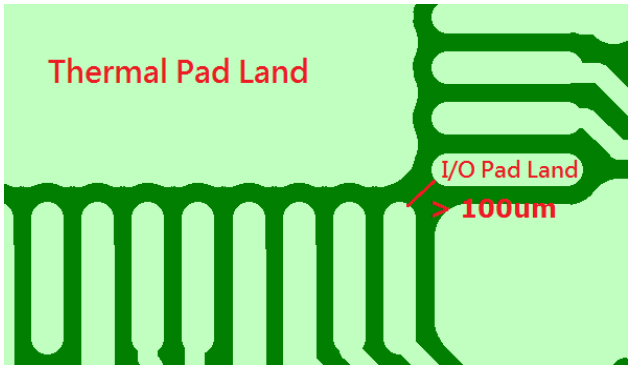
For the QFN package design, the exposed thermal pad size may extend very close to the maximum available size for that package, so the gap between the thermal pad land and I/O pad land may be small, as shown in Figure 23. Keep the gap between the thermal pad land and I/O pad land larger than 100 µm on all four sides to increase the solder mask web between the thermal pad and I/O pad land.

Figure 23. Thermal Pad Land Gap




Also, keep the solder mask opening gap between the two adjacent I/O pad lands at four corners of the QFN package larger than 100 µm, as shown in Figure 24.

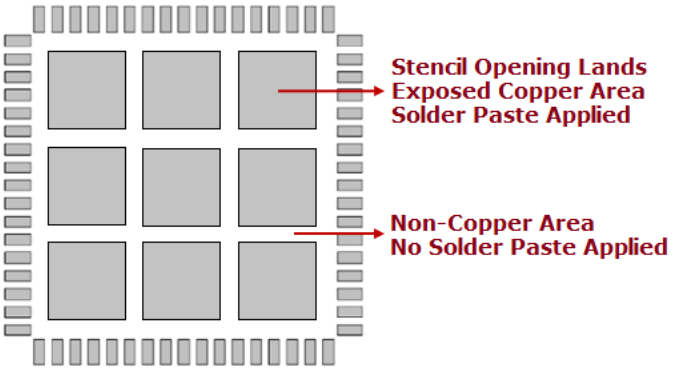
Figure 24. I/O Pad Land Gap at Corners



## 6.2 Stencil Design Considerations

To avoid possible overflowing of excessive solder paste to the pins, consider implementing the thermal pad land through cross-hatching stencil opening lands, as shown in Figure 25. The recommended width and height of each stencil opening land is 1.8~2.0 mm, and the recommended spacing between two stencil opening lands is 0.3 mm.

Figure 25. Stencil Design

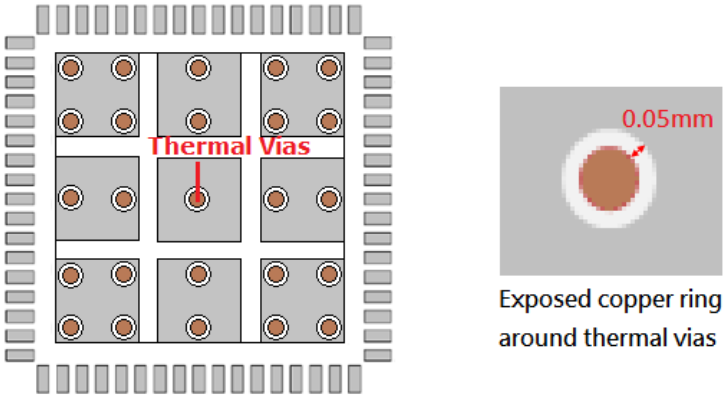



## 6.3 Thermal via Design Considerations

The thermal vias are designed to transfer the heat from the E-pad of the QFN package IC die to the top copper layer of the PCB (inner or bottom copper layers) to provide superior thermal dissipation performance. The recommended thermal via diameter is 0.3 mm or less, and the recommended spacing between two adjacent thermal vias is 1.0~1.2 mm.

The thermal vias should be well connected to the internal ground plane through an exposed copper ring around each thermal via, as shown in Figure 26. The exposed copper ring is not required on the exposed thermal pad land since the copper of the thermal pad land is already exposed. In practice, designers should adjust the location of the thermal vias to meet the possible PCB layout requirements, such as good power plane layout.

Figure 26. Thermal Vias and Exposed Copper Ring




## 6.4 Copper Area Design Considerations

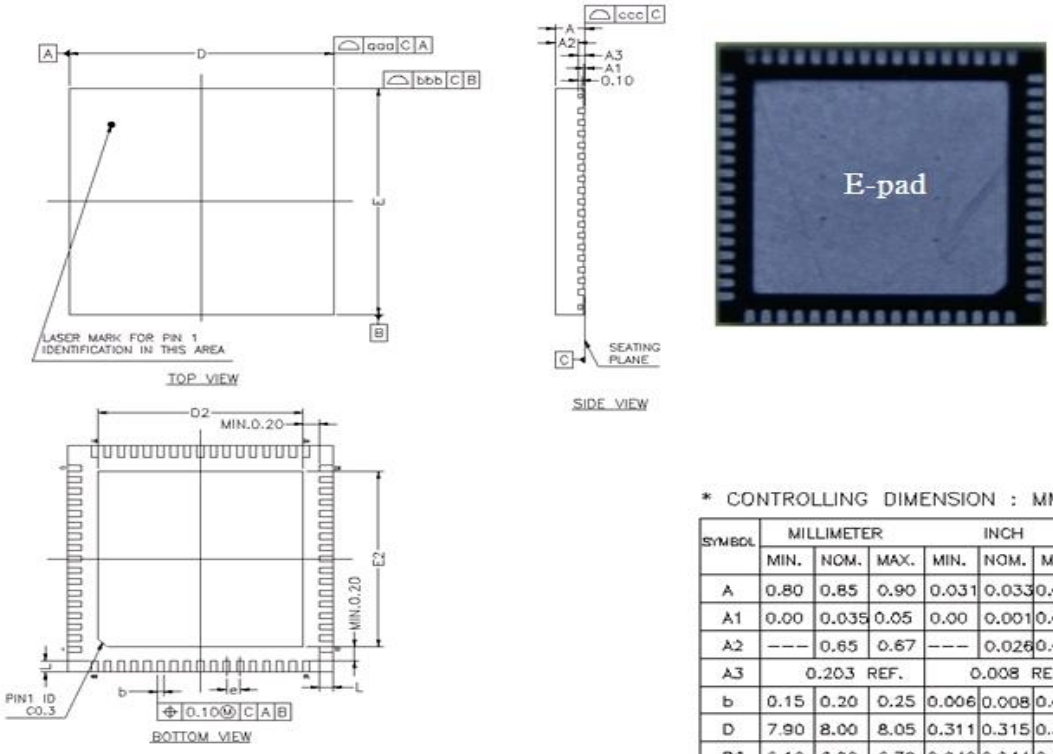
The top/inner/bottom copper areas of the PCB act as heat sinks for the QFN package PCB layout design. The top copper areas should be covered with a solder mask, leaving only the SMD thermal pad exposed. The top copper areas should be made as large as possible.

The inner and bottom layer copper planes can be connected to the exposed thermal pad through thermal vias and should be made as large as possible. The thermal pad is usually tied to the ground copper planes of the PCB, so you should double-check before connecting the copper planes to the thermal pad.

## 6.5 Package Information

Figure 27 shows the package outline details, and Figure 28 shows the details regarding the recommended PCB footprint for the QFN package. Table 3 describes the dimension details.

Figure 27. 68-Pin QFN E-Pad Package Outline (001-96836)




* CONTROLLING DIMENSION : MM

| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.80 | 0.85 | 0.90 | 0.031 | 0.033 | 0.035 |
| A1 | 0.00 | 0.035 | 0.05 | 0.00 | 0.001 | 0.002 |
| A2 | --- | 0.65 | 0.67 | --- | 0.026 | 0.026 |
| A3 | 0.203 REF. | | | 0.008 REF. | | |
| b | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D | 7.90 | 8.00 | 8.05 | 0.311 | 0.315 | 0.317 |
| D2 | 6.10 | 6.20 | 6.30 | 0.240 | 0.244 | 0.248 |
| E | 7.90 | 8.00 | 8.05 | 0.311 | 0.315 | 0.317 |
| E2 | 6.10 | 6.20 | 6.30 | 0.240 | 0.244 | 0.248 |
| L | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |
| e | 0.40 bsc | | | 0.016 bsc | | |
| TOLERANCES OF FORM AND POSITION | | | | | | |
| aaa | 0.10 | | | 0.004 | | |
| bbb | 0.10 | | | 0.004 | | |
| ccc | 0.05 | | | 0.002 | | |

NOTES :
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6.PACKAGE WARPAGE MAX 0.08 mm.
7.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8.APPLIED ONLY TO TERMINALS.

Figure 28. Recommended PCB Footprint for 68-Pin QFN 8x8 Package

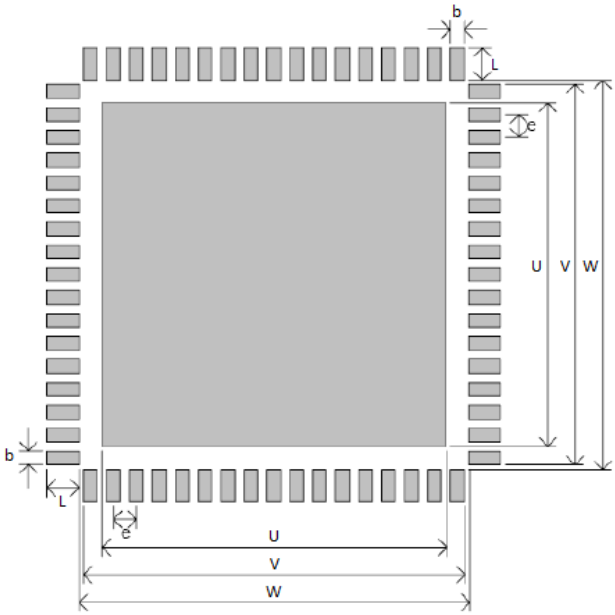


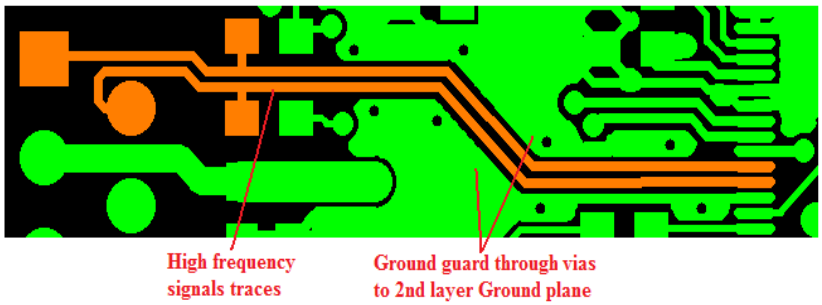

Table 3. GX3 Recommended QFN PCB Footprint Dimension

| Symbol | Description | Typical Dimension |
|---|---|---|
| e | Lead pitch | 0.40 mm |
| b | Pad width | 0.23 mm |
| L | Pad length | 0.80 mm |
| U | – | 6.30 mm |
| V | – | 6.63 mm |
| W | – | 7.20 mm |

# 7 EMI Considerations

The high-frequency signal traces such as Ethernet differential signals and clock signals should be surrounded by a ground guard to prevent interference with other signal wires, as shown in Figure 29. A better EMI effect can be attained with a one-piece GND underneath the IC, furnished with PTH holes to enlarge the GND area.

Figure 29. Ground Guard for High-Frequency Signals




The chosen RJ45 connector must be shielded so that the EMI integrity of the design is not compromised. The shield must be electrically connected to chassis ground to extend the chassis barrier for high-frequency emissions. If an unshielded connector is used, the EMI would pass through the nylon material of the connector. The shield will also prevent less external EMI from entering the chassis.

To reduce electromagnetic emissions and susceptibility, it is imperative that the traces from the transceiver to the RJ45 be routed as differential pairs. The objective is to close the loop area formed by the two conductors. The radiated field from the loop or the voltage picked up by the loop by external fields is governed by the field strength and the area formed by the two conductors. A reasonable board design uses 5~10-mil trace widths, separated by 10 mils. Transmit differential pairs should be routed adjacent to a power plane.

Do not cross differential signal traces over any split reference planes, as doing so may create unpredictable EMI problems.

You can consider implementing the choke components (Figure 30) on the Gigabit differential signal traces to avoid possible EMI issues, if necessary. Also, ensure Ethernet chassis ground isolation, as shown in Figure 6. EMI protection for the USB lines is shown in Figure 31.

Figure 30. EMI Protection on Gigabit Differential Signals

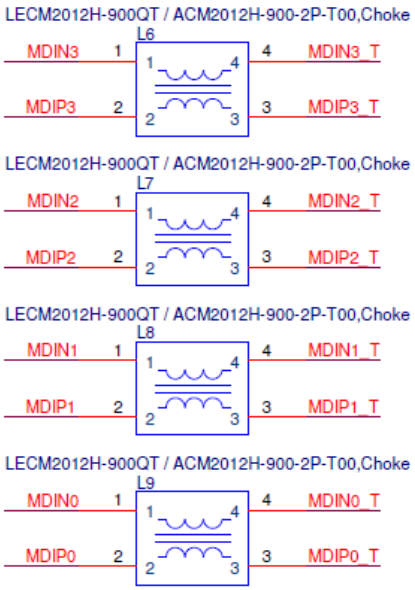
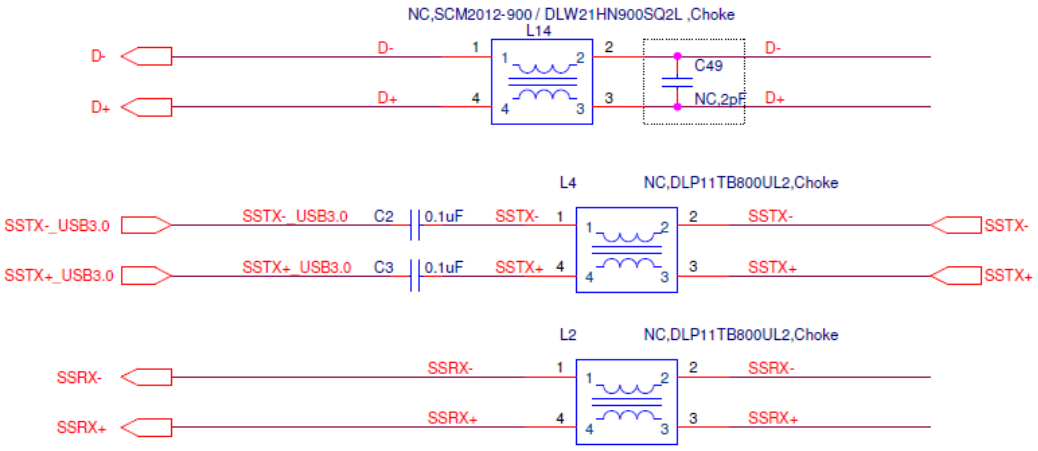


Figure 31. EMI Protection on USB Signals (Optional)

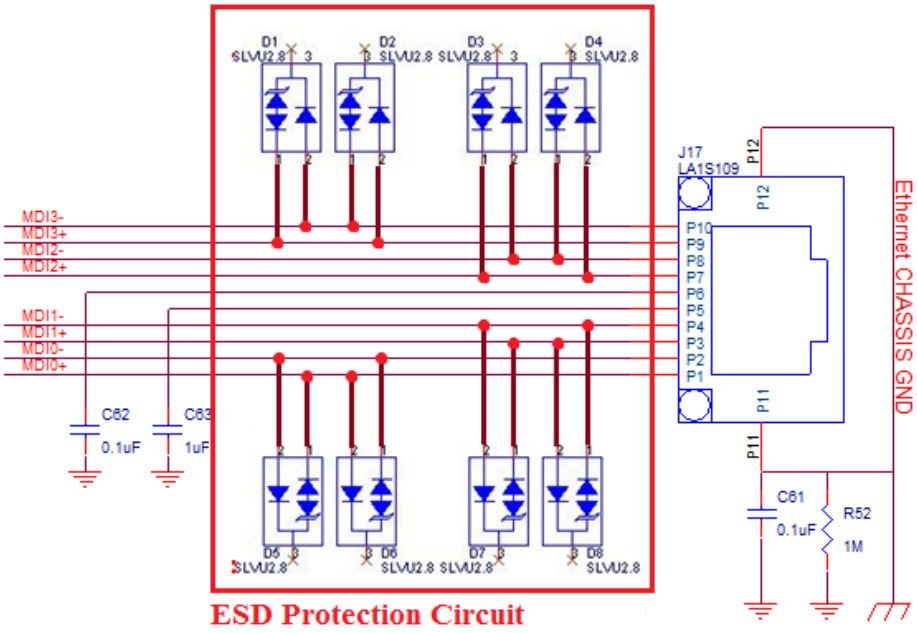



# 8 ESD Considerations

To reduce ESD, It is necessary to place a 1-MΩ resistor and a 0.1-µF capacitor (2 kV or 3 kV) to isolate the chassis ground and digital ground, as shown in Figure 6, and provide a gap of at least 35 mils between chassis ground and digital ground. Choose a fully shielded RJ45 connector that provides a low impedance path to ground for improved noise immunity performance.

Fatal discharge may be generated from various sources including a charged Ethernet cable, outside devices such as Power over Ethernet (POE), or a human body. Ethernet ICs become vulnerable to damage from ESD due to such unpredictable factors. Protecting Ethernet interfaces from cable discharges can pose a challenge for board designers. A good protective circuit must effectively fasten a transient to a safe voltage and also present an acceptable capacitive load on Hi-Speed differential transmission lines. Figure 32 show example ESD protection circuits.

Figure 32. Example ESD Protection Circuit for Single RJ45 with Integrated Magnetic (Optional)




# 9 Thermal Considerations

While designing the PCB, keep in mind thermal issues. The following methods can help reduce the operating temperature of GX3 applications.

## 9.1 Improve Cooling Plane

There are some major heat sources in GX3 based applications, including GX3 and external voltage regulators. You can connect the GX3 VCC/GND pins and the DVSS E-pad pin with wide traces to the respective power/ground planes to increase the cooling effect and reduce the GX3 operating temperature.

You can also add cooling planes on the external voltage regulators to reduce the operating temperature of the external voltage regulators.

## 9.2 Improve Air Convection

If GX3 is implemented in an embedded system, you can place it in a location with good air convection and avoid the high-operating-temperature ICs, such as voltage regulators or the MCU, to reduce the GX3 operating temperature.

# 10 Schematics and Layout Review Checklist

Table 4 is a checklist for all the important guidelines. Provide an answer to each checklist item to find out the extent to which your hardware design meets these guidelines.

Table 4. Schematics and Layout Review Checklist

| No. | Schematic Checklist | Answer (Yes/No/NA) |
|---|---|---|
| 1 | Are the decoupling capacitors and bulk capacitors connected per Figure 7? | |
| 2 | Does the crystal meet the specification in this application note? | |
| 3 | Do the USB precision resistors have one-percent tolerance? | |
| 4 | Are the serial EEPROM lines provided with pull-up resistors to the 3.3-V domain? | |
| 5 | Is the USB port provided with a 4.7-µF bulk capacitor? | |
| 6 | Are the USB and Ethernet connector shields terminated properly? | |
| 7 | Are the ferrite beads connected as shown in Figure 7? | |
| 8 | Is the gap between the USB/Ethernet shield ground and the digital ground more than 35 mils? | |
| 9 | Is the series resistor R2 added on the crystal signal? | |
| | **Layout Checklist** | |
| 1 | Is the crystal placed close to the chip (less than 1 cm)? | |
| 2 | Are the decoupling capacitors and bulk capacitors placed close to the GX3 power pins? | |
| 3 | Are the vias placed close to the GX3 power pins? | |
| 4 | Are the power traces routed away from the high-speed data lines and the clock lines? | |
| 5 | Are the USB SS and HS signal lines matched in length? | |
| 6 | Are the USB data lines provided with a solid ground plane underneath? | |
| 7 | Are the SS traces provided with the guard traces along the USB data trace with stitching vias? | |
| 8 | Are the SS traces provided with the AC decoupling capacitors (0.1 µF) on the TX lines? | |
| 9 | Are the USB traces kept as short as possible? | |
| 10 | Is it ensured that there are no stubs on all the USB traces? | |
| 11 | Is it ensured that there are no vias on the SS traces? | |
| 12 | Do the USB traces have few bends and no 90-degree bends? | |

# A Recommended Components List

This appendix lists the recommended components for reference purposes only. The component datasheets may not be available on public websites. Contact the vendors for detailed datasheet and design notes before implementing the components in your GX3 target applications.

## A.1 93C56/93C66 EEPROM

GX3 supports the 3.3-V to 5-V 16-bit mode 93C56/93C66 EEPROM. Refer to the EEPROM Selection section for more details.

| Vendor | Website | Part No. |
|---|---|---|
| Atmel Corporation | http://www.atmel.com | AT93C56/AT93C66 |
| Holtek Semiconductor Inc. | http://www.holtek.com.tw | HT93LC66 |
| ON Semiconductor | http://www.onsemi.cn | CAT93C66 |
| Fairchild Semiconductor | http://www.fairchildsemi.com | FM93C66A |
| Microchip Technology Inc. | http://www.microchip.com | 93AA66B/93C66B/ 93LC66B/93C66C |
| Seiko Instruments Inc. | http://www.sii-ic.com | S-93A56A/S-93A66A/ S-93C56B/S-93C66B |
| STMicroelectronics | http://www.st.com | M93C56/M93C66 |
| Giantec Semiconductor Inc. | http://www.giantec-semi.com | GT93C56A/GT93C66A |

## A.2 25-MHz Crystal

GX3 supports a 25-MHz crystal. Refer to the Crystal Selection section for more details.

| Vendor | Website | Part No. |
|---|---|---|
| JenJaan Quartek Corporation | http://www.nsk.com.tw | NSK NXK25.000AC12F-KAB6 SMD |
| ZHUOER ELECTRIC | http://www.dgze.com.cn | HC-49 |
| SHIN KOLN CO.,LTD | http://www.skctech.com | HC-49 |
| GUANGZHOU JINGYANG ELECTRONIC TECHNOLOGY CO., LTD. | http://www.gzdydz.cn | HC-50 |
| Interquip Electronics | http://www.interquip.com | SMHF-49 Series |
| CTS Corporation | http://www.ctscorp.com | ATS250BSM-1 |

## A.3 RJ45 Connector/Ethernet Magnetic

GX3 supports a 10/100/1000 Base-T Ethernet magnetic with TX/RX Turns Ratio 1CT:1CT. Refer to the Ethernet Magnetic Selection section for more details.

| Vendor | Website | Part No. |
|---|---|---|
| Bothhand Enterprise Inc. | http://www.bothhand.com.tw | LA1S109/KLA1S109 LF |
| LANKom Electronics Co., Ltd. | http://www.lankom.com.tw | LJ-G40B1C-00-F |
| TAIMAG Corporation | http://www.taimag.com | RJLBG-201TC1 |
| Allied Components International | http://www.alliedcomponents.com | AR11-3724/AR11-3726 |

**Note:** Verify if your preferred RJ45 connector is a single RJ45 connector module with an integrated 10/100/1000 Base-T magnetic. If not, you should implement an Ethernet magnetic with your preferred RJ45 connector.

## A.4 USB 3.0 Connector

The following are some recommended USB 3.0 connectors for your reference.

| Vendor | Website | Part No. |
|---|---|---|
| Foxconn Electronics, Inc. | http://nw.foxconn.com | UEA2010C-4EK1-4F |
| SMARTCONN Technology Co., Ltd. | http://smartconn.diytrade.com | USB3-AMAS-219 |
| Shenzhen ECH Technology Co., Ltd. | http://litkconn.en.alibaba.com | MNB032U02001 |

# Document History

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Document Number: 001-97119

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| ** | 4792871 | MDDD | 08/11/2015 | New application note. |
| *A | 5242181 | MDDD | 04/26/2016 | Edited links<br>Updated template |
| *B | 5711062 | AESATP12 | 04/26/2017 | Updated logo and copyright. |
| *C | 6294668 | VIKU | 08/29/2018 | Updated template |

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