AN96667

PSoC® Real-Time Clock Based on Power-Line Frequency

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Associated Code Example: CE96926

Associated Part Family: All PSoC 3, PSoC 4, and PSoC 5LP parts

Software Version: PSoC Creator™ 3.1

Related Application Notes: For a complete list of the application notes, click here.

To get the latest version of this application note, or the associated project file, please visit http://www.cypress.com/go/AN96667.

AN96667 describes how to design an accurate real-time clock for PSoC® 3, PSoC 4, and PSoC 5LP MCUs using the 50/60-Hz frequency of the mains (utility) AC power line as the time base. It also explains how to use a 32.768-kHz watch crystal as a backup time base in case of a mains power failure.

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Introduction

Accurate timekeeping is a vital requirement for applications that need to perform operations at a certain time of day (for example, automated control of street lights), store the timestamp of events (such as energy meters and data acquisition devices), or display the time and date (such as a digital wall clock).These applications use a real-time clock (RTC) to generate and keep track of time. RTCs should be accurate, low cost, and low power and consume minimal printed circuit board (PCB) space.

An RTC design includes two parts: an oscillator and a counter. Typically, the oscillator uses a 32.768-kHz crystal for frequency generation. The accuracy of the crystal-generated frequency depends on a number of factors such as aging of the crystal, tolerance, capacitive load, and nonlinear drift with temperature. For example, a 50-ppm frequency error will result in a drift of 2 minutes per month, which accumulated over several months would make the RTC inaccurate. Temperature compensation techniques can be applied to get accurate frequencies, but they increase cost, complexity, and PCB space.

This application note discusses a method of using the 50/60-Hz frequency of the mains (utility) power line as an alternative to the crystal-based frequency for accurate timekeeping over high temperature variations. For information on target applications where this technique is feasible, refer to the Target Applications section.

Code examples related to this application note are available in CE96926 – PSoC Real-Time Clock Based on Power-Line Frequency. This application note assumes that you are familiar with the basics of these devices and the PSoC Creator™ integrated design environment (IDE). If you are new to them, refer to AN54181 – Getting Started with PSoC 3, AN77759 – Getting Started with PSoC 5LP, AN79953 – Getting Started with PSoC 4, and the PSoC Creator home page.

Caution This application note involves the use of a high AC voltage supply, which poses an inherent risk of serious injury or death. Extreme care is necessary when you work with the mains AC power line. Accidental human contact with high voltage is dangerous. Cypress assumes no responsibility for death or injury resulting from exposure to high AC voltage or line power due to the user's negligence or use by someone inexperienced in dealing with power electronics.

Mains AC Power-Line Frequency Accuracy

Power companies in some countries maintain the average frequency of the 100-V to 240-V 50/60-Hz mains power line (utility frequency) for zero error over a period of approximately one week. The actual frequency at any instant may vary from the ideal frequency. But power operators maintain time using this frequency source and compare this time with the Coordinated Universal Time (UTC), which is based on International Atomic Time, to find the time error.

After a period of time, they adjust the frequency by a few millihertz so that the time error moves in the opposite direction and eventually reaches zero. Such corrections are aimed at maintaining the time error to be well within 1 minute at any instant in time. Thus, the mains AC power-line frequency in such countries may be used as a time base for building a real-time clock with high accuracy.

A comprehensive list of countries where power-line frequency correction is done is not available at this time. You can use the examples provided in CE96926 to check if correction is being done in your country. An example of the data collected is given in the Test Results section of this document. However, Cypress test results indicate that power-line frequency corrections are being done in the U.S. and UK. Also, the following excerpt from Wikipedia, the free encyclopedia, indicates that such corrections are being done in Europe and North America.

Note The following content is from Wikipedia. Cypress does *not* maintain this content for accuracy or guarantee that it is up to date. If you have access to the Internet, go to the Wikipedia website to read the latest version by clicking the following link or entering it in your browser.

"Utility frequency: Long-term stability and clock synchronization":
http://en.wikipedia.org/wiki/Utility_frequency#Long-term_stability_and_clock_synchronization

Today, AC-power network operators regulate the daily average frequency so that clocks stay within a few seconds of correct time. In practice the nominal frequency is raised or lowered by a specific percentage to maintain synchronization. Over the course of a day, the average frequency is maintained at the nominal value within a few hundred parts per million.[18] In the synchronous grid of Continental Europe, the deviation between network phase time and UTC (based on International Atomic Time) is calculated at 08:00 each day in a control center in Switzerland. The target frequency is then adjusted by up to ±0.01 Hz (±0.02%) from 50 Hz as needed, to ensure a long-term frequency average of exactly 50 Hz × 60 sec × 60 min × 24 hours = 4,320,000 cycles per day.[19] In North America, whenever the error exceeds 10 seconds for the east, 3 seconds for Texas, or 2 seconds for the west, a correction of ±0.02 Hz (0.033%) is applied. Time error corrections start and end either on the hour or on the half hour.[1]

Target Applications

Following are the prerequisites for an application to use this technique:

- The system is AC wall powered.
- The wall-powering comes from the direct mains supply. The application presented in this application note has not been tested with uninterruptible power supplies (UPS) or inverter-based supplies.
- The system is used in a country where power-line frequency corrections are done.

Note This technique is suitable for long-term accuracy but may not work for short-term accuracy, for example, generating a 1-second window for accurate measurement of a high-frequency digital signal. In this case, the 32.768-kHz crystal oscillator would be better suited.

Power-Line Interface

For using the power-line frequency as a time base, the power-line signal needs to be conditioned such that it can be used by PSoC. A power-line interface circuit is used for this purpose. Its functions are as follows:

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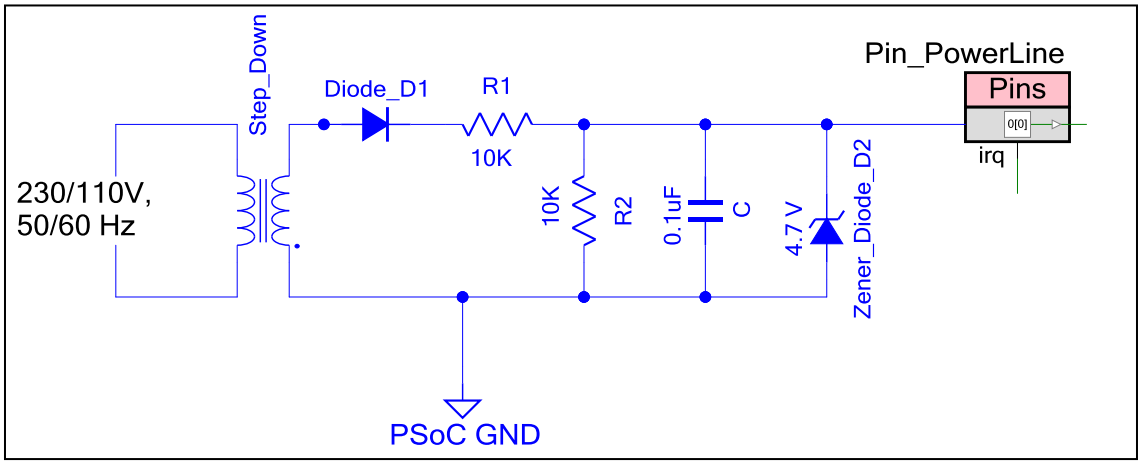
- Reduce the amplitude of the power-line signal within the operating voltage levels of the device (primary function)
- Filter out high-frequency noise that can occur on the power line, since the noise can introduce false counts in the RTC
- Suppress any voltage spikes in the power line, as they can damage the PSoC device

There are multiple ways of implementing such an interface circuit. Figure 1 shows one example.

Figure 1. Power-Line Interface Circuit Using a Step-Down Transformer



The step-down transformer reduces the 230-V/110-V power line to 12 V AC. Diode D1 performs half-wave rectification and ensures that negative cycles are not seen by the PSoC device. Resistors R1 and R2, along with capacitor C, filter high-frequency noise in the power line. R2 also provides a discharge path for the capacitor in the negative half cycle. Zener diode D2 ensures that the voltage remains within the allowed voltage levels on the PSoC general-purpose I/O (GPIO) pin.

The PSoC GPIO pin is configured as a digital input pin with an LVTTL threshold that guarantees a logic high at 2.1 V (VIH = 2.1 V for LVTTL). Thus, the conversion of the external analog waveform to a digital signal inside PSoC is achieved with a digital input pin, avoiding the need for a dedicated comparator resource.

Component values are calculated as follows for 5-V PSoC operation.

The Zener diode breakdown voltage should be within the Vdd (or Vddio) of the PSoC GPIO. So, a 4.7-V Zener diode (1N4732A) is chosen.

The maximum possible current in the circuit should be several times (50 to 100 times should be sufficient) the reverse leakage current of the Zener diode to ensure that the Zener diode does not clip the output voltage to a very low value. For a reverse leakage current of 10 uA, the required maximum circuit current would be about 1 mA. The peak half-wave rectified wave is nearly 10 V for a 12-V RMS output of the transformer. Hence, R1 is chosen as 10K using the following formula:

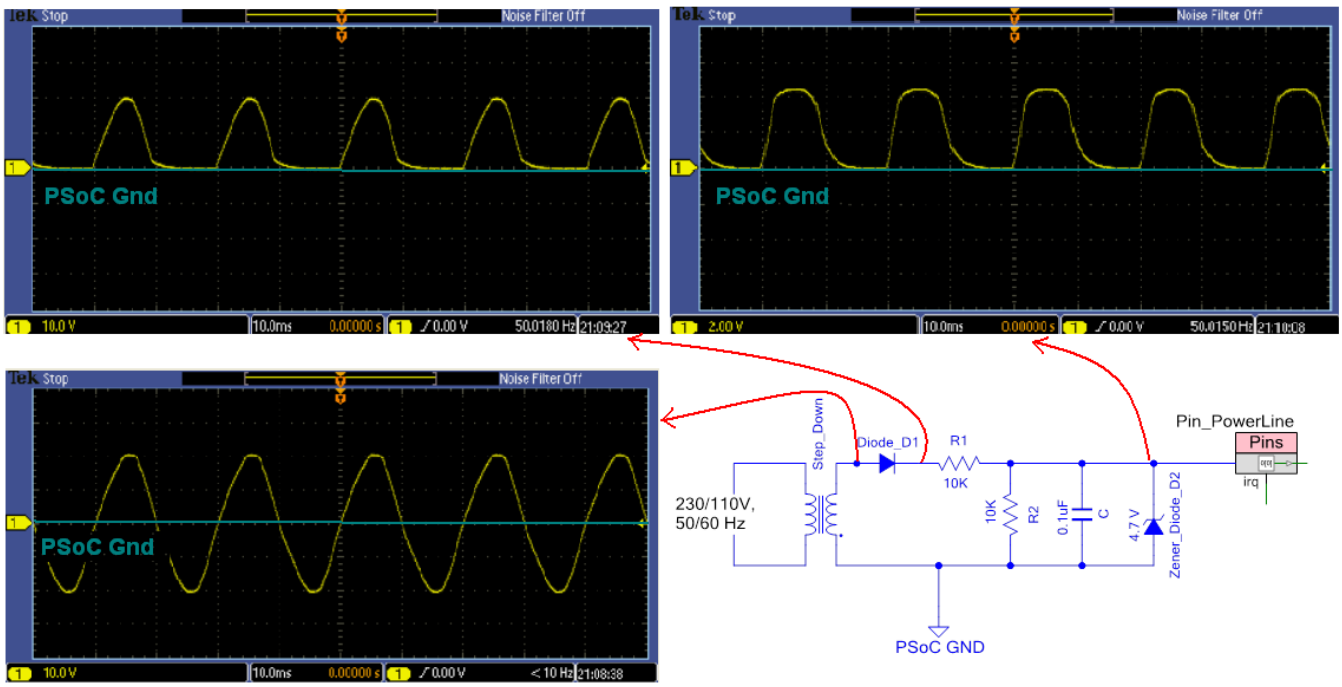
R1 = Peak output voltage of rectifier / max circuit current required

Assume the same values for R1 and R2 as R = 10K. Then the cutoff frequency of the low-pass filter formed by R1, R2, and C is as follows:

Fc = 1/(2*pi*0.5R*C)

A cutoff frequency of about 100 Hz to 500 Hz would ensure that high-frequency noise is rejected and the power-line frequency is accepted. The value of C is chosen as 0. 1 µF, yielding a cutoff frequency of 320 Hz. Note that the time constant for charging the capacitor (in a positive half cycle) is 0.5 RC and for discharging the capacitor (in a negative half-cycle) is RC. The chosen R2 and C values ensure complete discharge of the capacitor before the next cycle. Figure 2 shows the voltage waveforms at various points in the circuit.

Figure 2: Intermediate Signals in the Power-Line Interface Circuit



The power requirement of the step-down transformer is less than 100 mW. If a step-down transformer already exists in the product design, its secondary output can be tapped. If the existing transformer's output voltage differs from 12-V RMS, then the interface component values can be recalculated based on the previous discussion.

Note An optocoupler–based interface that performs the required functions may be used instead of the transformer-based interface.

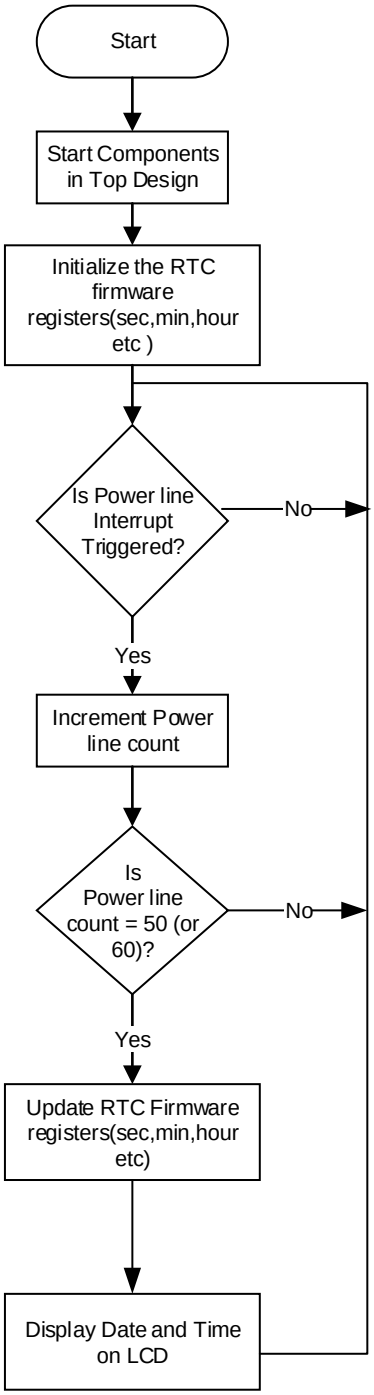
RTC Design Using Power-Line Frequency

An RTC maintains time and date values such as seconds, minutes, hours, day of the week, day of the month, and year. The occurrence of "1 second" is the fundamental unit on which all the other values are built. For implementing an RTC in PSoC, there must be a mechanism to detect the completion of each second. Then the firmware can increment the other values during the completion of each second. On completion of each second, the "seconds" variable is incremented, and if the "seconds" variable crosses 60, the "minutes" variable is incremented (and the "seconds" variable is reset). If the "minutes" variable crosses 60, the "hour" variable is incremented (and the "minutes" variable is reset) and so on.

In the power line–based technique, the completion of each second is detected by the occurrence of 50 or 60 rising edges (depending on a 50-Hz or 60-Hz power-line frequency) of the digital version of the power-line signal. A macro in the code is used to set the frequency to 50 Hz or 60 Hz. The Pin_Powerline digital input pin introduced in the previous section (see Figure 1) is configured to generate a GPIO interrupt on the rising edges. The count of the number of rising edges is maintained in the GPIO interrupt routine. When this count reaches 50 or 60, "1 second" is said to have been completed because the power-line frequency is 50 Hz or 60 Hz. This 1-second event is used to update the RTC values (RTC firmware registers). The flow chart in Figure 3 shows this logic.

Since the average value of the mains AC power-line frequency is kept accurately at 50 Hz or 60 Hz, the RTC time maintained by this technique would be accurate in the long term. Refer to the Test Results section for details.

Figure 3. Flow Chart of RTC Using Power-Line Frequency



RTC Design Using Power-Line Frequency with Crystal Backup

In the event of a power failure, RTC timekeeping using the power-line frequency would stop. So, in applications where PSoC would continue to operate during power failures by using a battery, a backup time base source must be used to keep the RTC running during power failures. A 32.768-kHz watch crystal oscillator can act as the backup source. Other options such as an external clock source can also be considered.

In this design, the firmware detects a power failure and accordingly switches the RTC timekeeping task to the backup source. The firmware also detects the return of the mains AC power-line signal and switches back the RTC timekeeping to the power-line time base.

The power failure is considered to be detected when the number of power-line interrupts over a 1-second period is less than a threshold, such as 45 (for a 50-Hz power line) or 55 (for a 60-Hz power line). The same logic is used to detect the return of power—when the number of power-line interrupts over a 1-second period is more than the threshold, power is considered to have returned.

To fill the need for a 1-second interval reference to detect the absence of the power line, the backup crystal source is always kept running, providing the 1-second interval source. RTC timekeeping is done as follows:

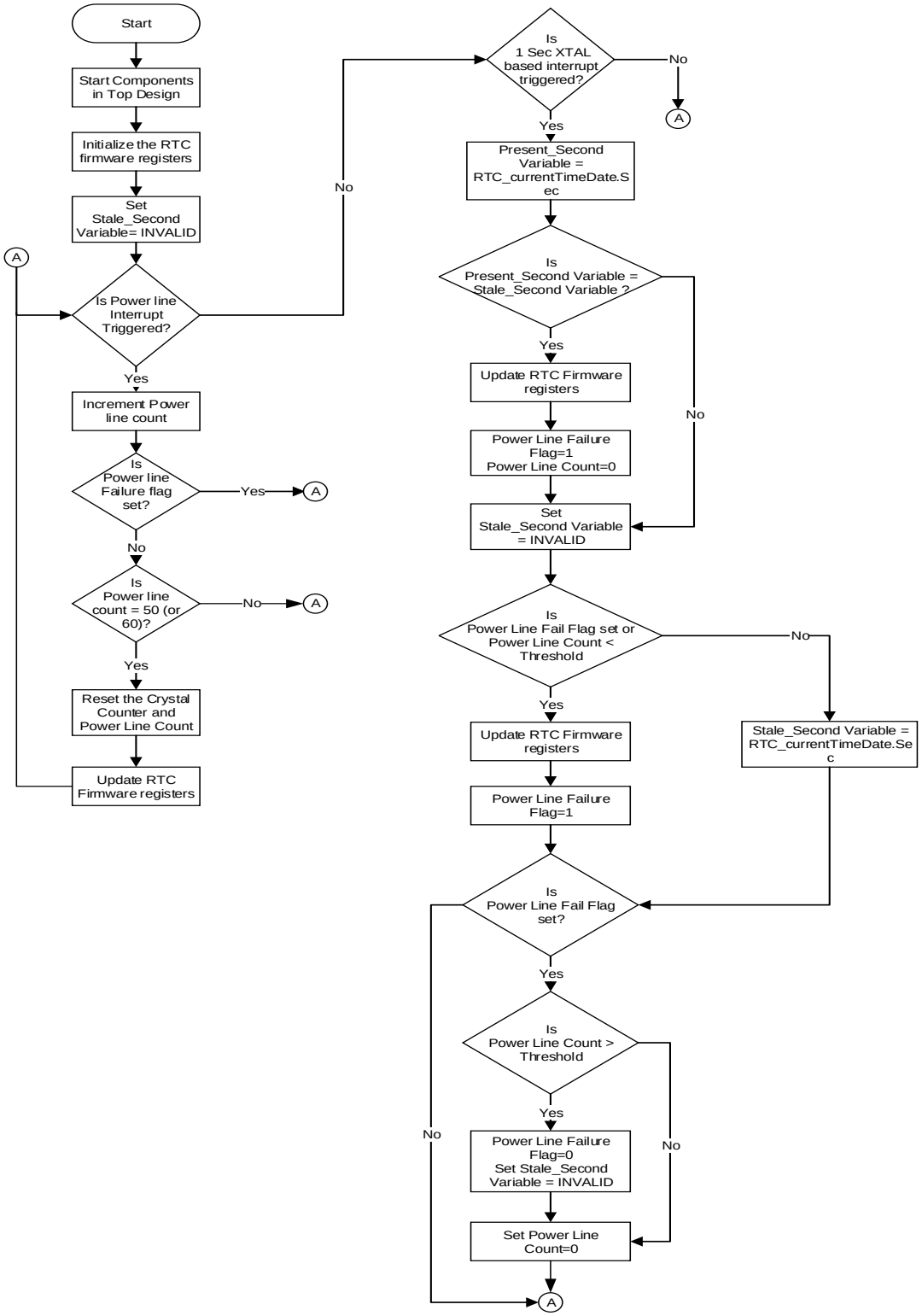
- A software counter is implemented to increment a variable on GPIO interrupts triggered by the power line. A 1-second event is considered to occur when the variable reaches 50 or 60.
- A timer with a period of 32768, also used to count the 32.768-kHz watch crystal frequency, generates one pulse per second (OPPS) events. Thus two 1-second event generators run in parallel.
- Either of the two 1-second event sources may present the 1-second event to the firmware.
- The OPPS timer is reset upon the completion of each second in the GPIO interrupt routine. So, if the power-line interrupt occurred first, then the OPPS interrupt would not occur for “that second.” Both the power line and crystal sources synchronously start measuring the “next second.”
- On the other hand, if the OPPS timer event occurs first, then the absence of the power line is detected by checking the value of the GPIO interrupt software counter in the OPPS crystal timer interrupt and comparing it with a threshold. If it falls below the threshold value (45 or 55), then power-line failure is considered to be detected.
- There is also a possibility that the GPIO interrupt software counter crossed the threshold, but the power line fails after the threshold comparison and before completing 50 or 60. In this scenario, a variable called “Stale_Second” is used. When the power line is present (threshold is crossed), the Stale_Second variable is updated with the RTC second value in the OPPS timer interrupt. During the next OPPS timer interrupt, the RTC second value (read into a Present_Second variable) is compared with the Stale_Second variable. If both values are the same, the RTC second was not incremented after the previous OPPS timer interrupt, which implies that the power failure occurred after the previous OPPS interrupt. In this way, the power failure is detected even if the power fails after the threshold comparison in the OPPS timer interrupt.

To summarize, the firmware logic chooses one of the two sources of 1-second events (power line–based GPIO interrupt routine or crystal-based timer interrupt) to update the RTC timekeeping registers. The firmware logic gives first preference to updating the RTC timekeeping registers using the GPIO interrupt software counter. Only if the firmware detects that the power line is off does it use the crystal OPPS source to update the RTC timekeeping registers.

When a power failure occurs, battery power consumption can be reduced by putting the device into a low-power mode, with the OPPS timer and GPIO interrupt as wakeup sources.

The flow chart in Figure 4 shows the firmware algorithm of the RTC design using power-line frequency with crystal backup.

Figure 4. Flow Chart of RTC Using Power-Line Frequency with Crystal Backup



Note that when executing from a backup source, the time error due to the crystal's frequency drift may add to the overall RTC time error. Also, since power-line counts are missed during this time, the average frequency of the power line may deviate from 50 Hz or 60 Hz, which can add more error to the overall RTC time error. This error depends on the duration of the power failure as well as the synchronization of the power failure duration with the frequency corrections done on the power-line frequency.

Project Implementation

Code example CE96926 – PSoC Real-Time Clock Based on Power-Line Frequency provides a PSoC 5LP–based PSoC Creator project for RTC design using a power line. This project can also be adapted to PSoC 3 and PSoC 4 devices since it requires only a GPIO pin interrupt and firmware code for the RTC timekeeping.

The same code example also provides a PSoC 4 BLE-based project for RTC design using a power line and crystal backup. The watch crystal oscillator (WCO) and the watchdog timer in PSoC 4 BLE are used to provide the OPPS events. This project can be adapted to PSoC 3 and PSoC 5LP devices by using a 32.768-kHz external crystal oscillator (ECO) and the dedicated low-power RTC timer available in these devices, which can be invoked using the RTC Component provided in PSoC Creator.

To develop a similar project for PSoC 41xx or PSoC 42xx devices, refer to the Knowledge Base article Implementing a 32-kHz ECO Interface with PSoC 4100/PSoC 4200 – KBA95848 for implementing a 32.768-kHz crystal oscillator and code example CE95915 – Implementing an RTC with PSoC 4100/PSoC 4200 Devices. Note, however, that it is not possible to operate PSoC 41xx or PSoC 42xx devices in a low-power mode when operating from the backup crystal source on power failure events.

Test Results

The RTC design using a power line with crystal backup was tested in the U.S. and UK for about 1 to 2 weeks. The test setup and procedure are explained in code example CE96926 – PSoC Real-Time Clock Based on Power-Line Frequency. The UTC time was used as the system reference time with which the RTC time was compared. There was no power failure during the tests, so RTC timekeeping was continuously performed using the power-line frequency, without having to switch to the crystal backup.

It was observed that the error in the RTC time kept returning to zero every few days. Also, the maximum error at any point in time was well within 1 minute.

Figure 5 and Figure 6 show the test results in the U.S. and UK respectively.

Figure 5. Test Results in U.S.

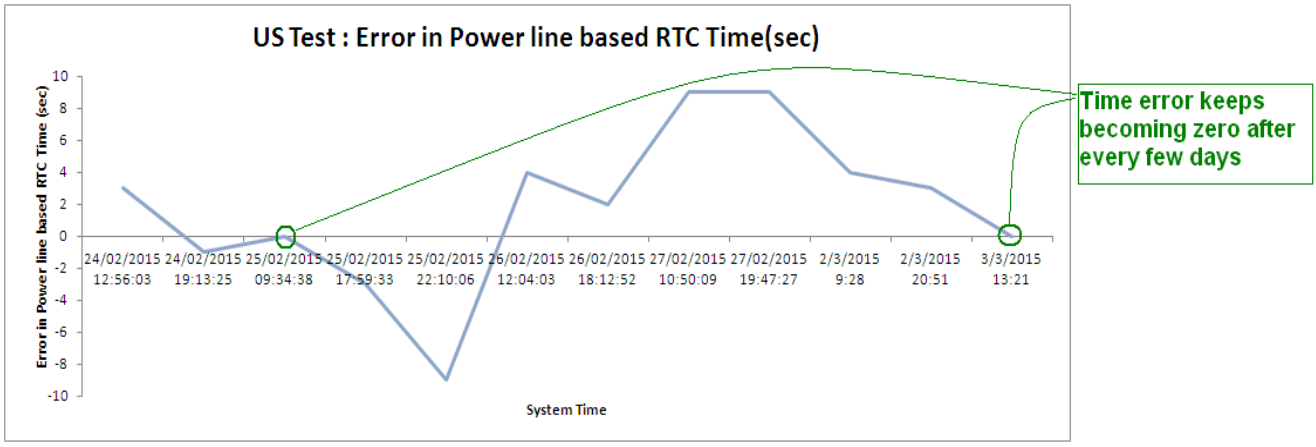
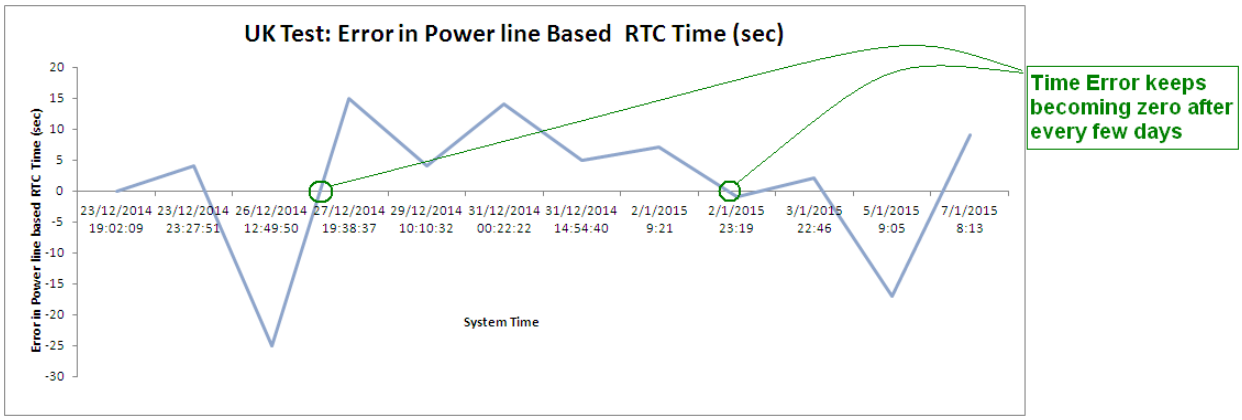


Figure 6. Test Results in UK



The test results confirm that power-line frequency corrections are being done in the U.S. and UK, and hence they can be used for maintaining RTC time.

Summary

This application note demonstrated how the mains AC power-line frequency (utility frequency) can be used to design an accurate RTC in PSoC 3, PSoC 4, and PSoC 5LP devices. The addition of this RTC functionality to PSoC may eliminate the need for an external RTC in some systems where PSoC is already being used for control and measurement purposes.

Related Application Notes

AN54181 – Getting Started with PSoC 3

AN77759 – Getting Started with PSoC 5LP

AN79953 – Getting Started with PSoC 4

AN91267 – Getting Started with PSoC 4 BLE

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Document History

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**	4710981	PSAI	03/26/2015	New Application Note
*A	5713187	AESATMP9	04/26/2017	Updated logo and copyright.

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