Hardware Design Guidelines for EMCA/Cable Design using EZ-PD CCG2

About this document

Scope and purpose

AN95599 provides hardware design and PCB layout guidelines for EMCA/Cable design using EZ-PD™ CCG2. These guidelines will help to ensure the best performance with respect to signal integrity and full electrical compliance with the USB Power Delivery and Type-C specification. For more reference designs and applications based on EZ-PD CCG2, please **click here**.

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1 Introduction

EZ-PD CCG2 is Cypress' second generation of USB Type-C electronically marked cable assembly (EMCA) controllers compliant with the USB Power Delivery (PD) specification 2.0. CCG2 provides a complete USB Type-C and USB PD solution for passive cables, active cables, and powered accessories. It combines an industry-standard, high-performance 32-bit ARM® Cortex®-M0 CPU, serial communication blocks (SCBs) to support standard serial communication protocols such as I^2C, SPI, UART, and an integrated USB Type-C transceiver including the termination resistors[1] R_D, R_P, and R_A.

In Type-C EMCA designs, active components including CCG2 are placed on a paddle card (**Figure 2**) – a card at each end of the cable, which holds the USB Type-C plugs and connects to the cable harness. The hardware guidelines in this application note apply to the design of the paddle card. **Table 1** lists the CCG2 product options available for different applications. For more details on these applications, see **AN95615**. For more details on USB Type-C and USB PD, see **www.usb.org**.

Table 1 EZ-PD CCG2 Product Options

Features	CYPD2103	CYPD2104	CYPD2105
Application	Passive Cable	Accessory[2]	Active Cable[3]
Package	20-ball WLCSP, 14-pin DFN	20-ball WLCSP	20-ball WLCSP

[1] See the **Type-C specification** for more details on termination resistors.

[2] An upstream facing port (UFP) with the form factor of a cable or dongle.

[3] Electronically marked cable assembly with a re-driver to condition USB data signals.

2 Introduction to USB Type-C

The USB Type-C Cable and Connector specification define a new 2.4-mm thin receptacle and plug. These plugs are designed with user convenience in mind and they can be plugged in either orientation. The USB Type-C cable provides up to 100 W of power. The USB **Type-C specification** also allows the cables to carry high-definition video in parallel with USB 3.0 communication.

The USB Type-C receptacle, plug, and cable provide a smaller, thinner, and more robust alternative to the existing USB 3.1 interconnects (standard and micro USB cables and connectors). The target applications range from ultra-thin notebook PCs to smart phones, where existing standard-A and micro-AB receptacles are deemed too large, too difficult to use, or inadequately robust.

Major advantages of the USB Type-C specification are as follows:

- Slim industrial design with a 2.4-mm plug height
- Reversible plug orientation and cable direction
- Transport of both USB signals and PCIe or DisplayPort signals on the same connector
- Easy implementation of low-cost power delivery up to 100 W

USB Type-C provides an all-in-one solution for today's applications supporting high bandwidth and power requirements as illustrated as follows:

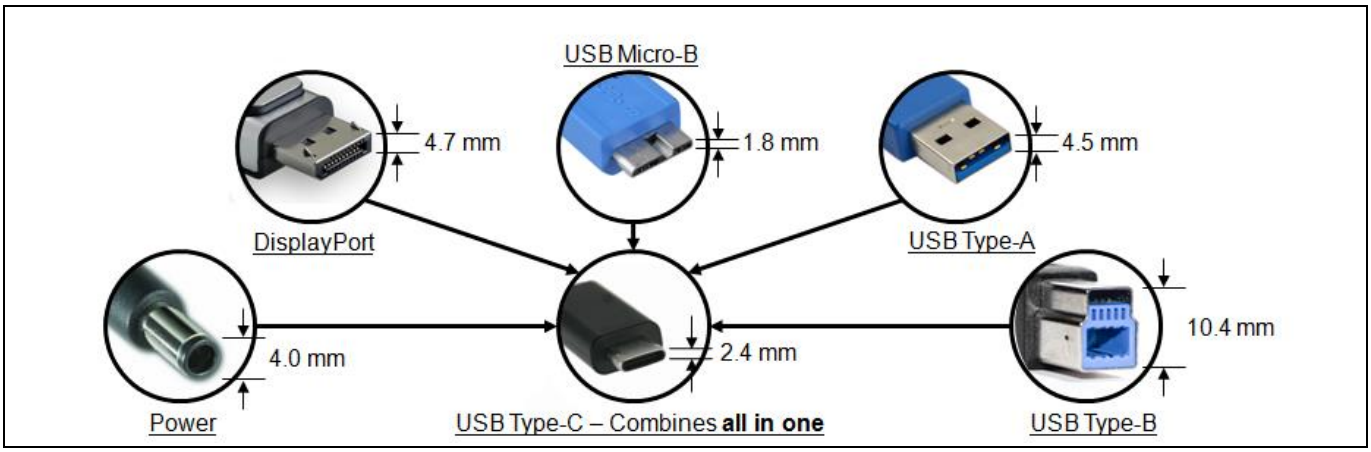


Figure 1 USB Type-C Combines It All

2.1 Signals in USB Type-C

A full-featured USB Type-C cable contains the following signals:

- V_{CONN}: Provides 5 V to power the active electronics inside the Type-C cable assembly. VCONN is sourced by the downstream facing port (DFP) or host initially and can be sourced by the upstream facing port (UFP) or device after a power-role swap.
- V_{BUS}: Power that can go as high as 20 V carrying 5 A depending on the power negotiation between the host and device as defined in the USB PD specification.
- CC: Configuration channel dedicated to USB-PD communications and shared between the USB host, cable, and device.
- Dn/Dp: Standard USB 2.0 lines used for USB 2.0 communication between a host and a device.

- RX/TX lines: Two pairs of RX and TX differential pairs in a full-featured USB Type-C cable assembly. At any time, only one set of RX and TX pairs is used for USB 3.0 communication, depending on the orientation in which the cable assembly is plugged in. See the section, **USB Type-C Connection Orientation Detection**.
- SBU1/SBU2: Sideband use signal lines used in alternate modes to transmit auxiliary signals such as audio. For more details on these signals, see the USB **Type-C specification**.

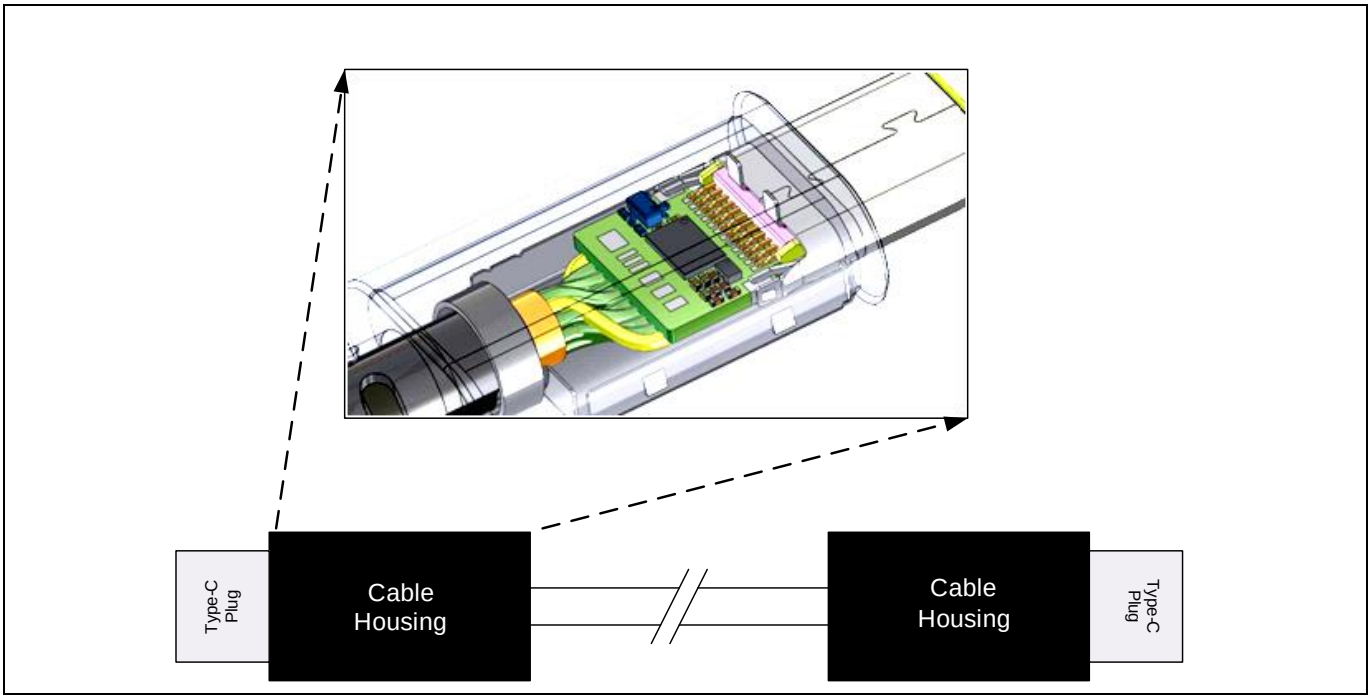


Figure 2 USB Type-C Connector Housing

2.2 Basic Terminology

SOP*: SOP stands for Start of Packet; A PD starts with an SOP* sequence. See the **USB PD specification**.

DFP: Downstream facing port (DFP) is a USB Type-C port on a host or a hub to which devices are connected.

UFP: Upstream facing port (UFP) is a USB Type-C port on a device or a hub that connects to a host or a hub DFP.

2.3 USB Type-C Connection Orientation Detection

A DFP exposes R_p terminations on its CC pins (CC1 and CC2), and a UFP exposes R_d terminations on its CC pins. The cables will expose R_a terminations on the VCONN pin. The purpose of R_p and R_d terminations on the CC pins is to identify the DFP to the UFP connection and the CC pin that will be used for communication. When the cable is connected, the DFP monitors both CC pins for a voltage lower than its un-terminated voltage.

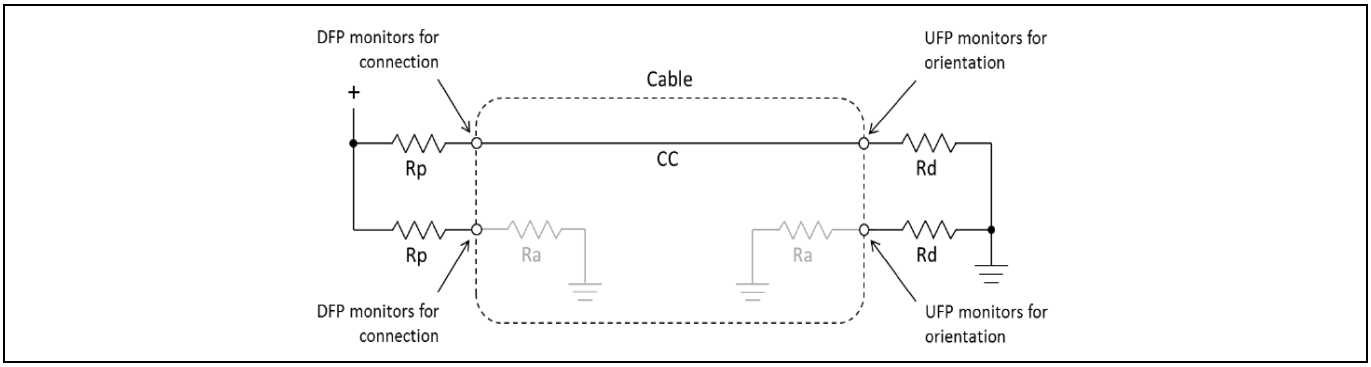


Figure 3 USB Type-C Connection/Orientation Detection[4]

By detecting the CC pin (CC1 or CC2) at the Type-C receptacle that is terminated by the R_d at the UFP, the DFP determines the SuperSpeed (SS) USB signals (from the two pairs) that are to be used for the connection and accordingly controls the functional switch to route the appropriate SuperSpeed USB signal pairs.

Similarly, the UFP detects the CC pin terminated by the DFP and accordingly controls the functional switch to route the appropriate SuperSpeed USB signal pairs. After a connection is established, the DFP will reassign CC1 or CC2 to provide cable power over the VCONN pin of the plug. See the **Type-C specification** for more details on the Type-C connection and orientation-detection mechanism.

[4] Illustration source: USB **Type-C specification**

3 Schematic Design Requirements

This section explains the schematic design requirements for CCG2-based EMCAs. Three application scenarios serve as a reference.

3.1 EMCA Solution with One CCG2 Chip per Cable

This EMCA solution contains a CCG2 chip in only one of its plugs. It requires running the VCONN wire through the cable (not through the chip), so that the chip (residing at one end of the cable) can be powered by either VCONN1 or VCONN2, regardless of which plug is connected to the host (DFP).

After the cable is enumerated, the host may shut down the VCONN supply. One of the key and unique requirements for this application is to power the chip from two separate VCONN pins. This solution needs a dedicated wire running between the plugs. The GPIO pin (ball D3 of the wafer-level chip scale package (WLCSP) or pin 13 of the DFN package) of the CCG2 device must be left floating for this application.

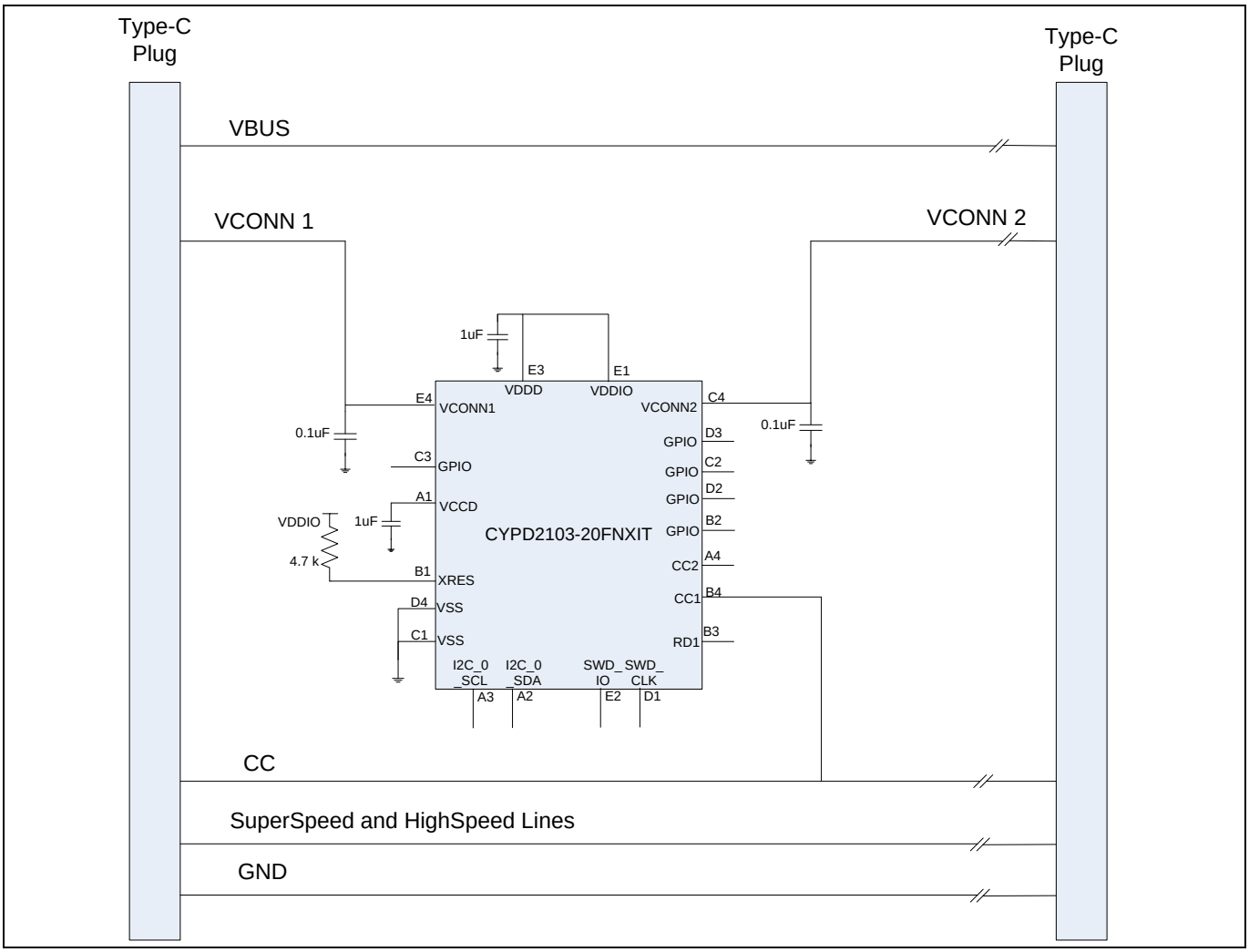


Figure 4 Power System Recommendation for a Single CCG2-based EMCA Cable Solution

Note: This diagram is for representative purpose and is based on the WLCSP package. For the DFN reference schematic, see the **Appendix**.

3.2 EMCA Solution with Two CCG2 Chips per Cable (one CCG2 active at a Time)

This EMCA solution contains two CCG2 devices, one in each plug, with only one powered at a time. In this solution, the VCONN signal does not run across the cable, but it breaks at the CCG2 device in each plug. Also, only the CCG2 device that is nearer to the DFP supplying VCONN is powered. After the cable is enumerated, the host may shut down the VCONN supply. This cable does not need the VCONN wire to run across from one end to the other, saving the cost of copper wire.

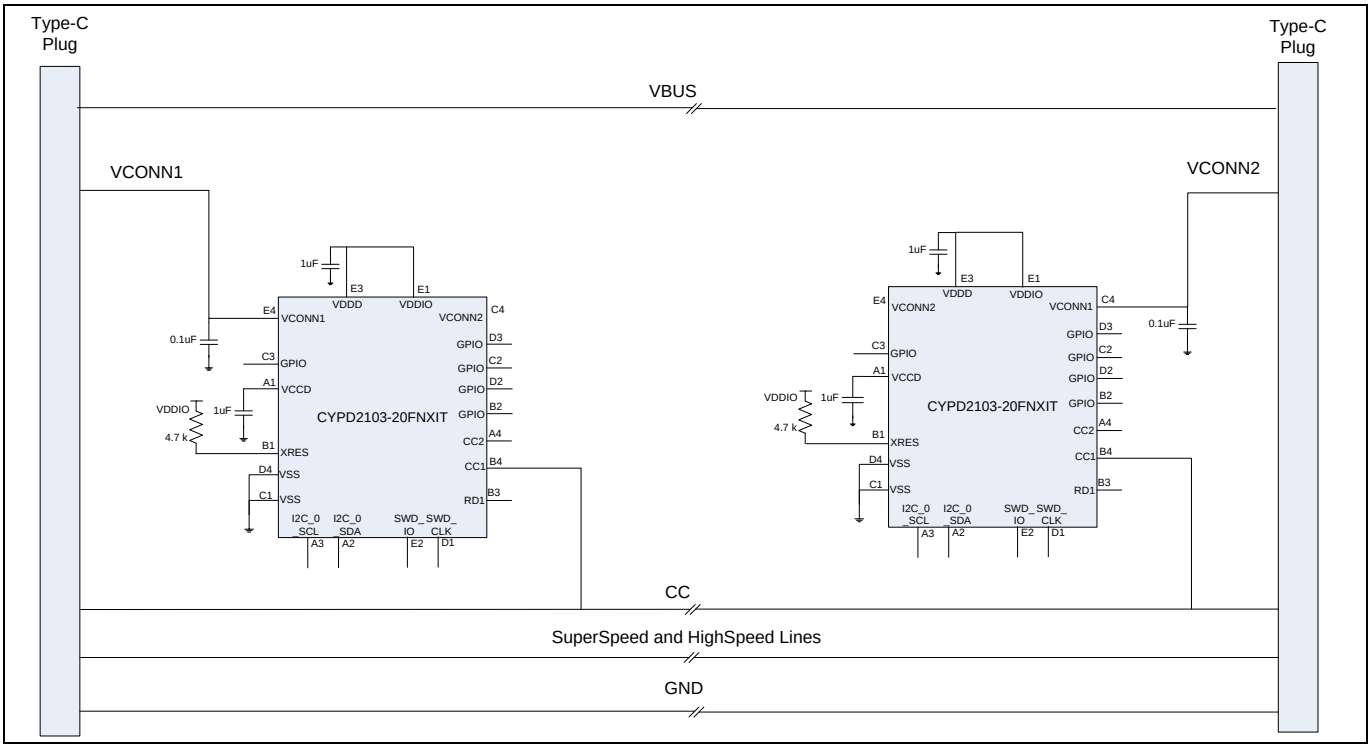


Figure 5 Power System Recommendation for Dual CCG2-based EMCA Cable Solution

Note: This diagram is for representative purpose and is based on the WLCSP package. For the DFN reference schematic, see the **Appendix**.

3.3 Active EMCA Solution with Two CCG2 Chips per Cable (Both CCG2s Active)

This EMCA solution contains two CCG2 devices, one in each plug, with both CCG2s powered at a time. The typical use case of this solution is in active cables. The main function of an active EMCA is to provide signal conditioning by adding a re-driver on the data path. Active cables that require configuration or signal conditioning are referred to as “managed active cables.” When a managed active cable requires independent management or signal conditioning at each end of the cable, separate USB PD controllers responding to USB PD structured vendor-defined messages (VDMs) must be located in each plug. For more details on VDMs, see the **USB PD specification**.

This active cable solution contains two CCG2 chips, one on each plug. VCONN is wired across the cable but is not shorted between the two connectors. In this solution, the wiring is done such that the cable is reversible. The GPIO pins (ball D3 of the WLCSP package or pin 13 of the DFN package) of both CCG2 devices must be pulled down to ground in this application.

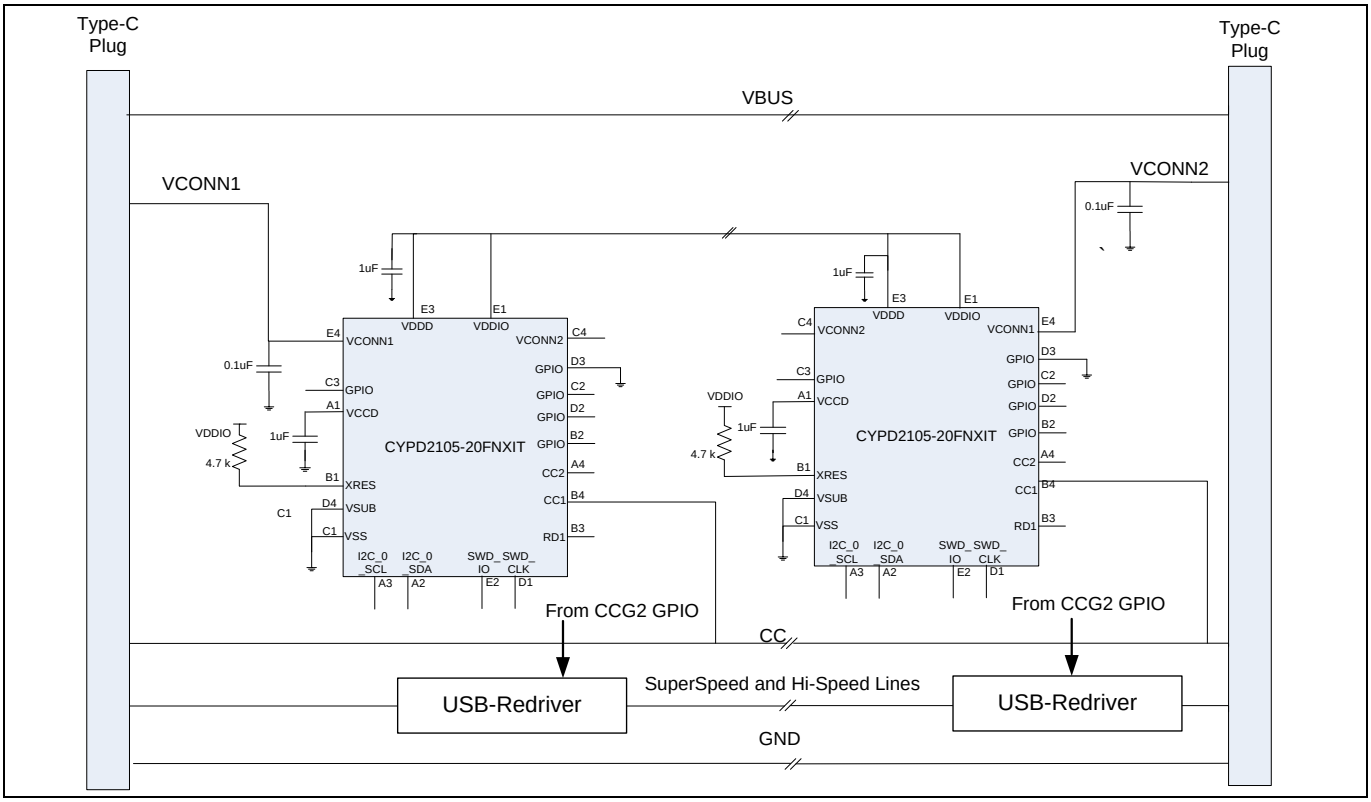


Figure 6 Power System Recommendation (Both Chips Powered)

Note: This diagram is for representative purpose and is based on the WLCSP package.

4 Power System

CCG2 can operate from one of the two power rails named VCONN1 and VCONN2. **Figure 4** and **Figure 5** show the recommended power supply-decoupling scheme for single- and dual-CCG2-based EMCA cables.

Each CCG2 chip needs a minimum of five passive components:

- Reset pull-up: This pull-up is required to ensure that the XRES line of the CCG2 chip is always pulled to the VDDIO rail so that the chip is not held in reset.
- Decoupling capacitor for VCONN rails: This 0.1-uF capacitor should be placed on the VCONN line to meet the ESD performance of the CCG2 chip (± 8-kV contact discharge and ±15-kV air gap discharge based on IEC61000-4-2 Level 4C).
- Decoupling capacitor for VDDD rail: CCG2 regulators and all peripherals are powered from the VDDD rails internally. To ensure reliable performance of the chip, a clean DC voltage is required at this pin. A 1 uF decoupling capacitor is required to reduce ripples in this rail.
- Decoupling capacitor for VCCD rail: VCCD is the 1.8-V internal regulator output. A 1-uF decoupling capacitor must be added to stabilize the supply and remove ripples from the rail.
- Decoupling capacitor for VDDIO rail: The internal GPIO buffers of CCG2 are powered from this rail. If the rail is powered from a dedicated supply, then it needs a 1-uF decoupling capacitor to reduce ripples. This rail can shorted to VDDD in cable applications as shown in **Figure 4**, **Figure 5**, and **Figure 6**.

Note: *In addition, four capacitors are needed on the VBUS pins of the Type-C connector according to the Type-C specification. A 10-nF bypass capacitor (minimum voltage rating of 30 V) is required for the VBUS pin in the full-featured cable at each end of the cable. The bypass capacitors should be placed as close as possible to the VBUS pins of the Type-C connector. See the* **Type-C Specification** *for more details.*

Table 2 Recommended Values of Passive Components

Passive Component	Recommended Value
XRES pull-up	4.7 kΩ
VCONN decoupling capacitor	0.1 µF per used rail
VDDD decoupling capacitor	1 µF
VCCD decoupling capacitor	1 µF
VDDIO decoupling capacitor (if powered from separate rail)	1 µF
VBUS bypass capacitor	10 nF per VBUS pin

For various CCG2 applications, the minimum number of components required is listed:

Table 3 BOM for CCG2 in Various Applications

Application	Figure Reference	Minimum Components	Description
EMCA Solution with One CCG2 per Cable	**Figure 4**	5	Four decoupling capacitors, one XRES pull-up resistor
EMCA Solution with Two CCG2 per Cable (Only One CCG2 Powered)	**Figure 5**	8	Three decoupling capacitors per chip, one XRES pull-up resistor per chip
Active EMCA Solution with Two CCG2 per Cable (Both Powered)	**Figure 6**	8	Three decoupling capacitors per chip, one XRES pull-up resistor per chip

4.1 VCONN Selection

CCG2 has two VCONNs (VCONN_1 and VCONN_2) with internal diode to power the VDDD pad of the chip, which in turn powers the rest of the chip:

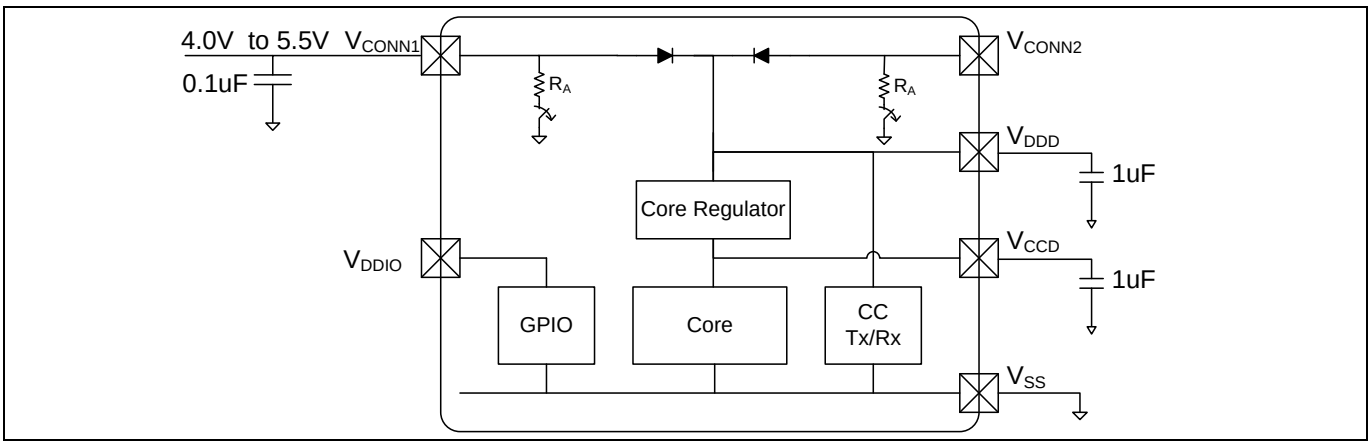


Figure 7 CCG2 Power and Bypass Scheme

4.2 Connecting an Authentication Chip

For applications that require tamper-proof authentication, CCG2 can be connected to an external authentication chip. This additional chip will ensure that only the specific vendor-provided cable works with the vendor's host and the host can terminate negotiations immediately if authentication fails. The authentication chip can be connected as shown in **Figure 8**, where U2 represents the authentication device with an I²C slave interface.

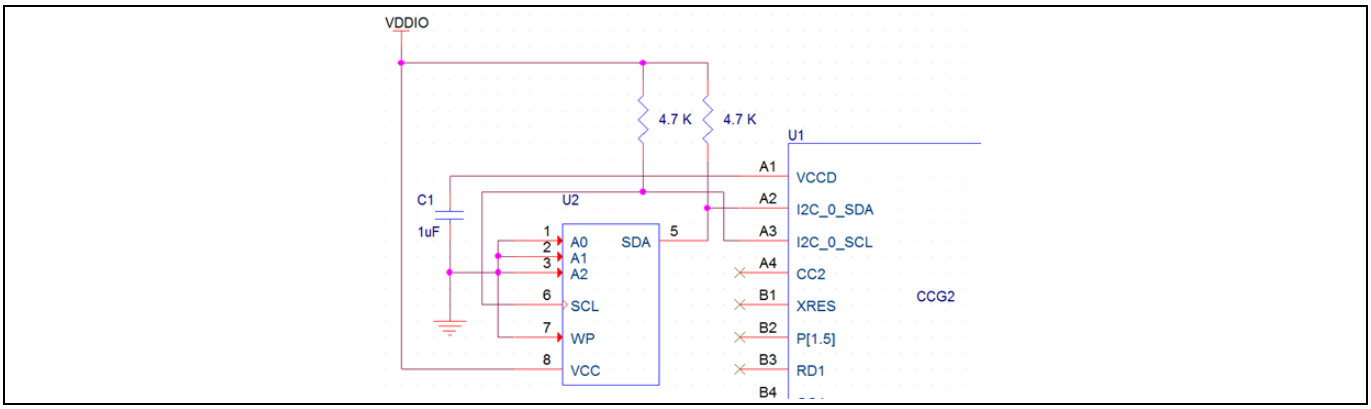


Figure 8 Authentication Chip Connection

5 PCB Layout Guidelines

This section explains PCB design guidelines for routing power signals and USB signals. It provides recommendations for placing components on the board. See the **Power System** section for recommendations on component values.

5.1 Power Domain

CCG2 devices are powered from the VCONN supply from the DFP. Consider the following while designing the power system network:

- Placement of bulk and decoupling capacitors
- Placement of power and ground planes

5.1.1 Placement of Bulk and Decoupling Capacitors

Place decoupling capacitors for high-frequency noise filtering close to the VCONN, VDDD, and VCCD pins as shown in **Figure 9**. Place the bulk capacitor, which acts as a local power supply to the power pin, close to the VDDD pin of CCG2.

Make the power trace width the same as the power pad width. To connect the power pins to the power plane, keep vias very close to the power pads. This helps to minimize stray inductance and IR drop on the line.

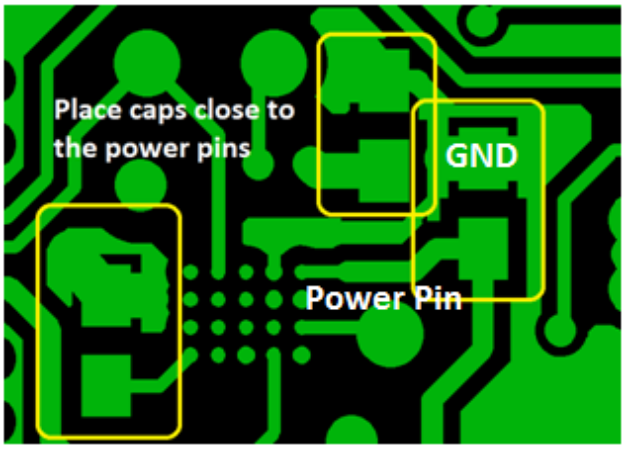


Figure 9 Placement of Capacitors

5.1.2 Placement of Power and Ground Planes

Place the power plane close to the ground plane for good planar capacitance. Planar capacitance between the planes acts as a distributed decoupling capacitor for high-frequency noise filtering, reducing electromagnetic radiation.

5.2 Routing of USB Data Lines

A USB Type-C cable consists of one or two PCBs, known as “paddle cards,” depending on the cable design. All full-featured Type-C cables must be electronically marked according to the Type-C specification and thus will be using these paddle cards.

PCB Layout Guidelines

Although the USB data lines are not directly connected to CCG2, you must pay careful attention to how they are treated in a paddle card design. The USB data lines are most critical to achieve good signal quality and reduce emission. Follow the guidelines below while designing a paddle card:

- Use a high-performance substrate material for paddle cards.
- Keep USB SuperSpeed traces as short as possible. Ensure that these traces have a nominal differential characteristic impedance of 90 Ω.
- Match the differential SS pair trace lengths within 0.12 mm (5 mils).
- Match the high-speed (Dp and Dn) signal trace lengths within 1.25 mm (50 mils).
- Ensure that the differential pairs have a minimum pair-to-pair separation of 0.5 mm.
- Adjust the high-speed signal trace lengths near the USB receptacle, if necessary.
- Make adjustments for SS Rx signal trace lengths near the USB receptacle. Make adjustments for SS Tx signal trace lengths near the device if necessary.
- Select a grounded coplanar waveguide (CPWG) system as a transmission line method as shown in **Figure 10**.

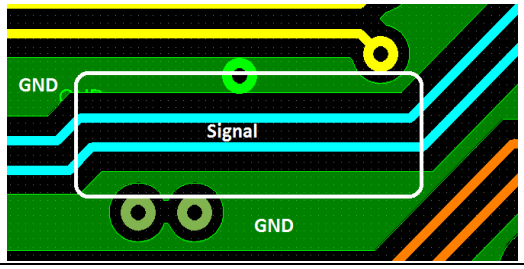


Figure 10 CPWG Example

- Minimize the use of vias.
- Group the V_{BUS} pins together (all V_{BUS} pins are brought out to the same plane using vias):

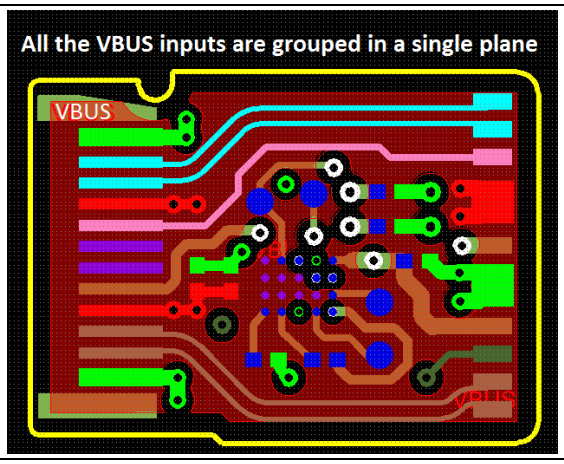


Figure 11 All VBUS Pins are Grouped Together

- Similarly, group the GND pins together (all GND pins are brought out to the same plane using vias).
- Additional ground pad is needed to solder the shield for a coax cable.

5.2.1 Typical 32-mil, Six-Layer PCB Example

Figure 12 shows the recommended stack up for a standard 32-mil-(0.8 mm) thick PCB. When this stack up is used with two parallel traces, each with a width (W) of 'x' mils and a spacing (S) of 'y' mils, the calculated differential impedance is 90 Ω.

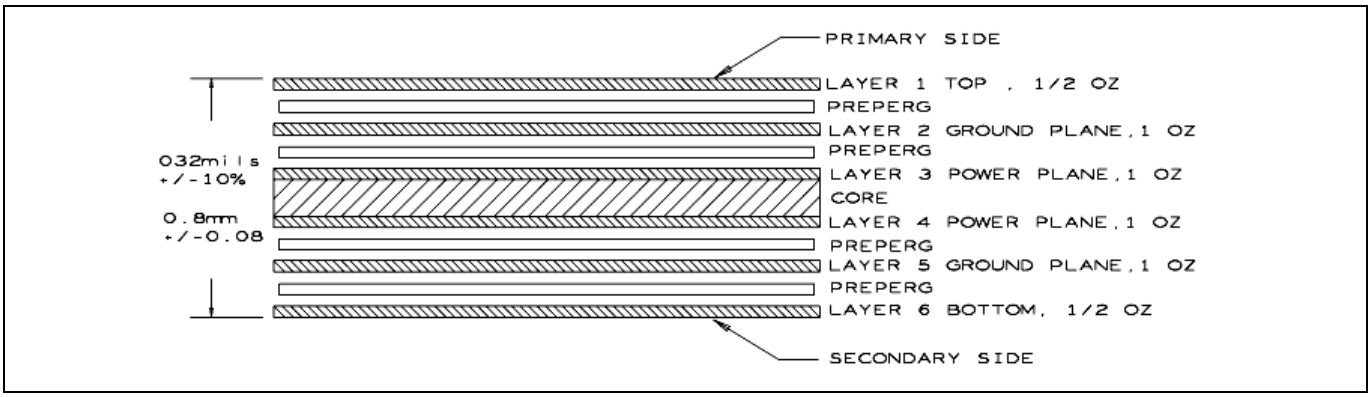


Figure 12 PCB Stack-Up

5.2.2 Impedance Matching

Maintain a constant trace width and spacing in differential pairs to avoid impedance mismatches:

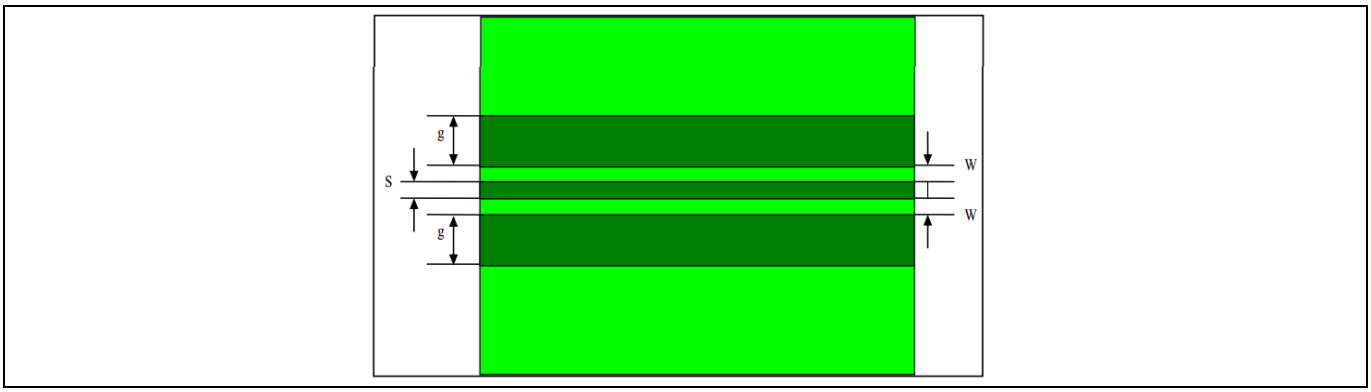


Figure 13 Differential Pair Placement

- 'g' is the minimum gap between the trace and other planes (8 mils)
- 'W' is the width of the signal trace
- 'S' is the gap between the differential pair signals

All SS signal lines should be routed over an adjacent ground plane layer to provide a good return current path.

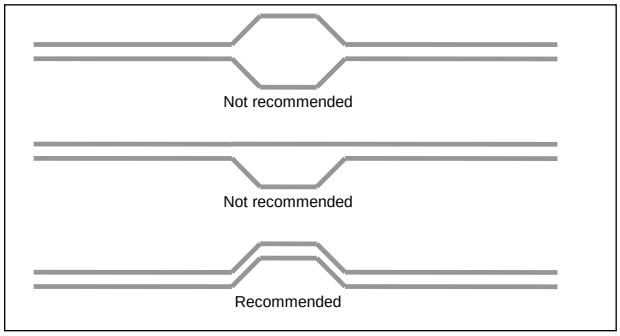


Figure 14 Differential Pair Impedance Matching Techniques

Splitting the ground plane underneath the SS signals introduces an impedance mismatch, thereby increasing the loop inductance and electrical emissions. **Figure 15** shows a recommended solid ground plane under the SS signal.

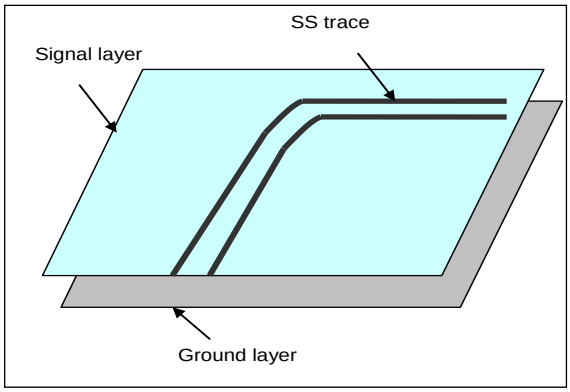


Figure 15 Solid Ground Plane Under SS Signal

Whenever two pairs of USB traces cross each other in different layers, a ground layer should run all the way between the two USB signal layers:

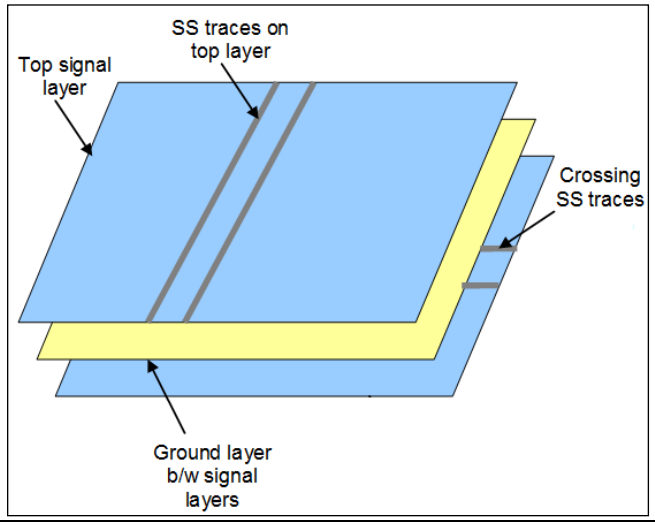


Figure 16 Ground Insertion

5.3 Signal Via Routing

This section discusses the general recommendations for routing the SS signals. In applications such as paddle cards for Type-C cables, it may not be possible to follow all these guidelines due to size constraint.

SS signals should be routed in a single layer. Vias introduce discontinuities in the signal line and affect the SS signal quality.

If you need to route the SS signal to another layer, maintain continuous grounding to ensure uniform impedance throughout. To do so, place ground vias next to signal vias, as shown in **Figure 17**. The distance between the signal and ground vias should be at least 40 mils.

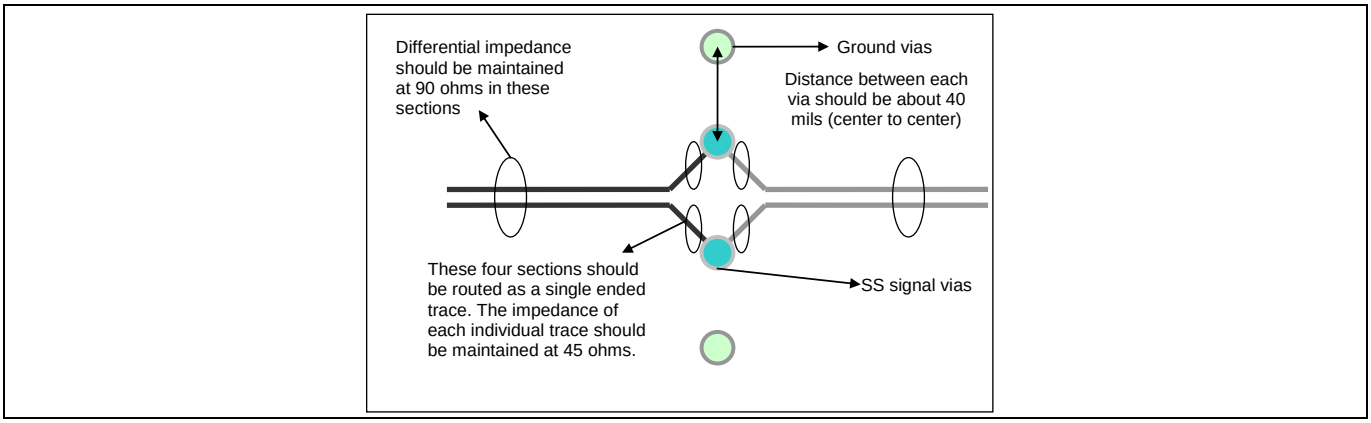


Figure 17 Ground Vias

Voids for vias on the SS signal traces should be common for the differential pair. A common void helps to match the impedance better than separate vias:

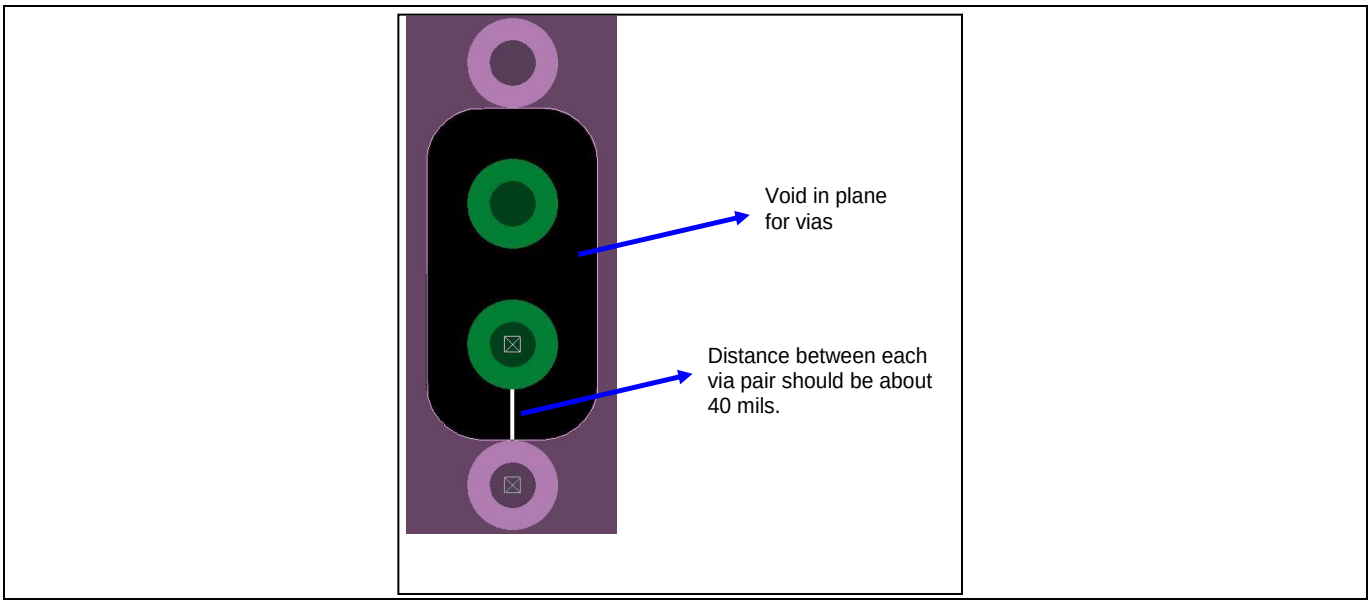


Figure 18 Void Vias Placement for SS Traces

On USB signal lines, use as few bends as possible. Do not use a 90-degree bend. Use 45-degree or rounded (curved) bends if necessary:

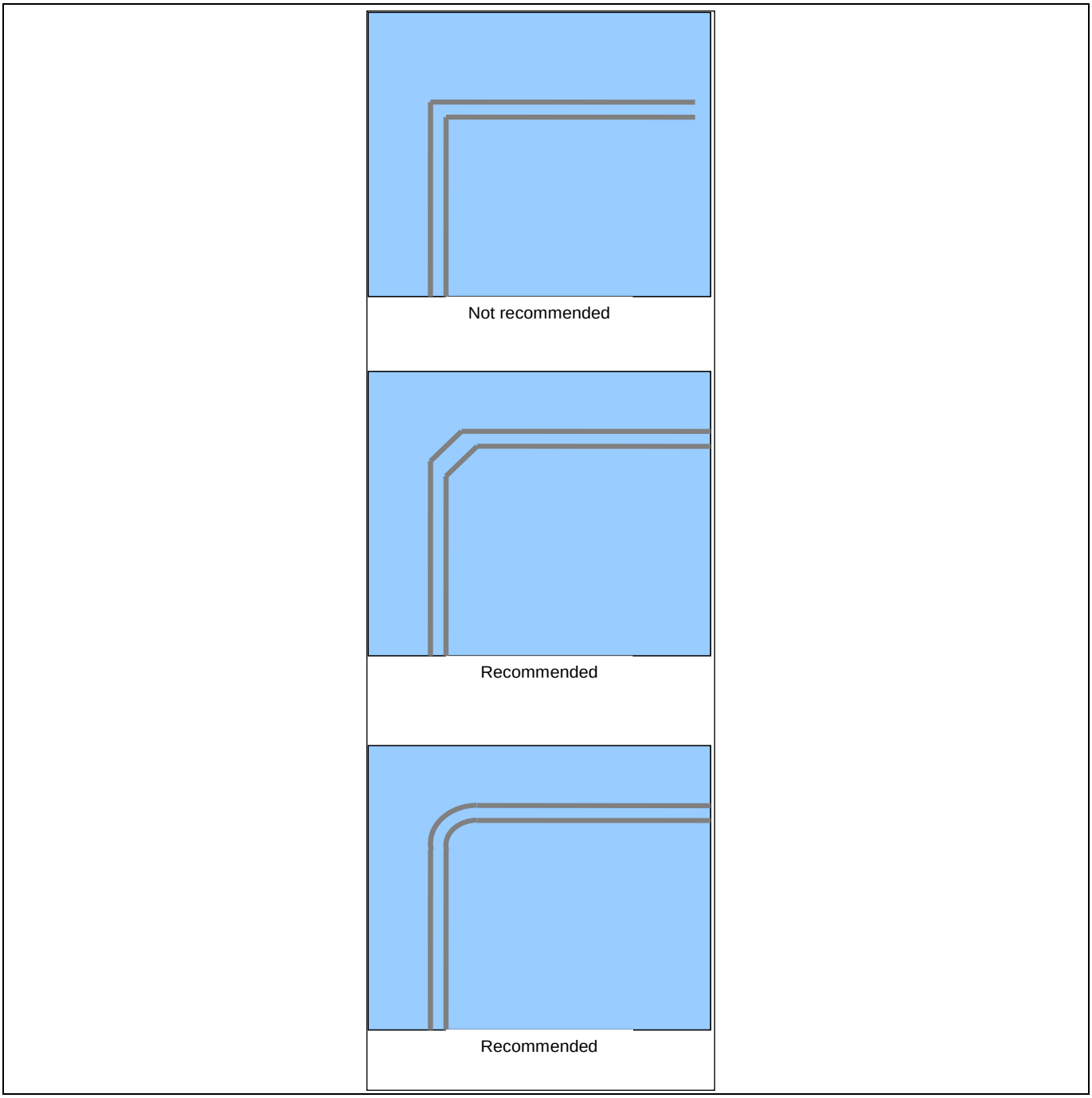


Figure 19 USB Signal Bends

6 Summary

USB PD operation demands careful hardware design. By following the guidelines in this application note, your CCG2-based cable design has a good chance of first-pass success.

7 Appendix - BOM and Schematics

7.1 Reference BOM for CCG2-based EMCA Paddle Card

Table 4 Reference BOM for CCG2-based Paddle Card

Item	Qty per Paddle Card	Reference Designator	Description
1	1	R1	Resistance 4.7 kΩ
2	1 (2*)	C3*, C4	Capacitor 0.1 µF 16 V
3	2	C1, C2	Capacitor 1 µF 16 V
4	1	U1	CCG2 Controller IC
5	1	J1	USB Type-C Plug-Connector
6	4	C5, C6, C7, C8	Capacitor 10 nF 35 V

* Applicable only to a single-chip CCG2 EMCA solution.

7.2 Paddle Card Reference Schematics for Single/Dual Chip CCG2 (CSP) EMCA – CYPD2103-20FNXIT

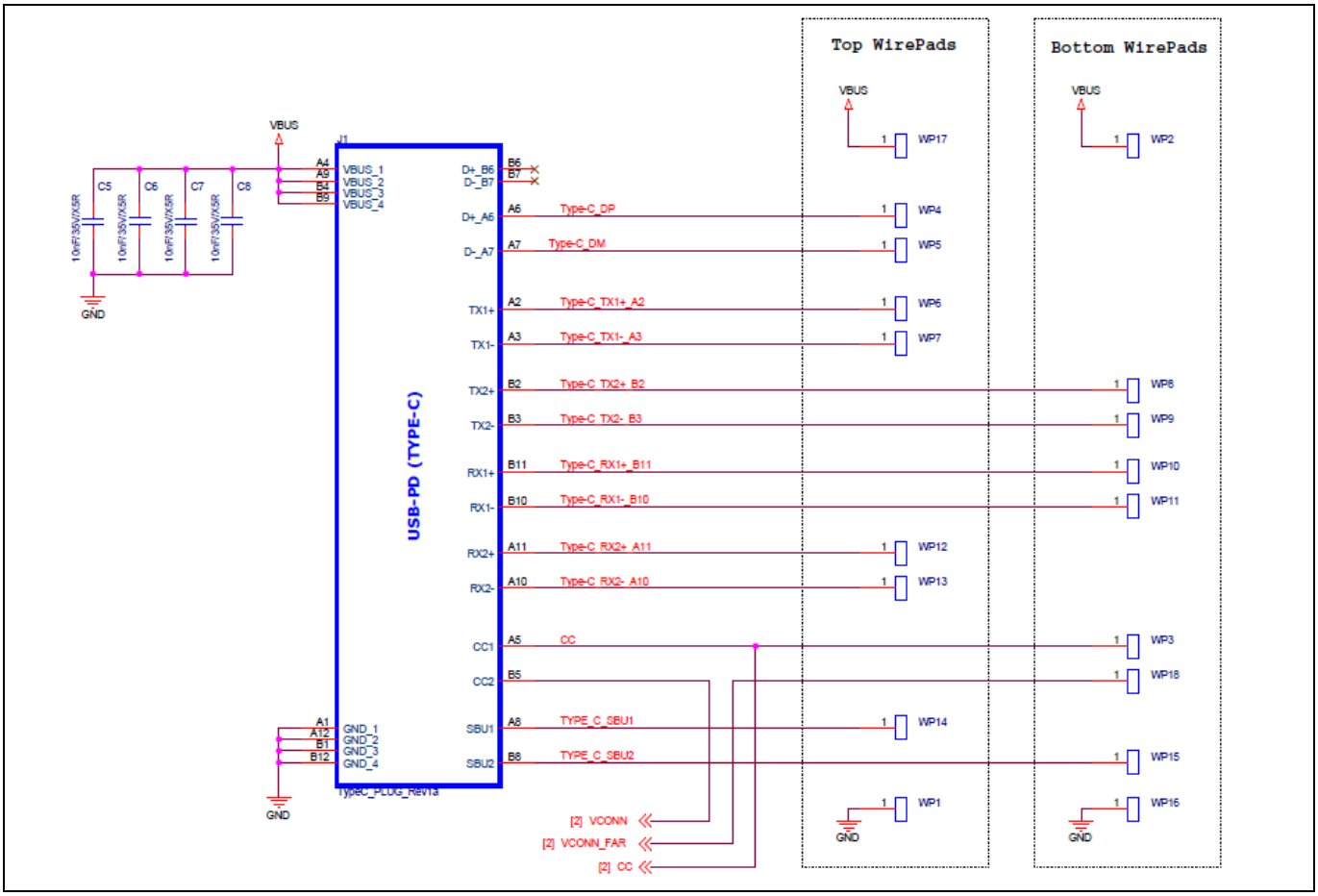


Figure 20 WLCSP-based Reference Schematics (Type-C connector portion)

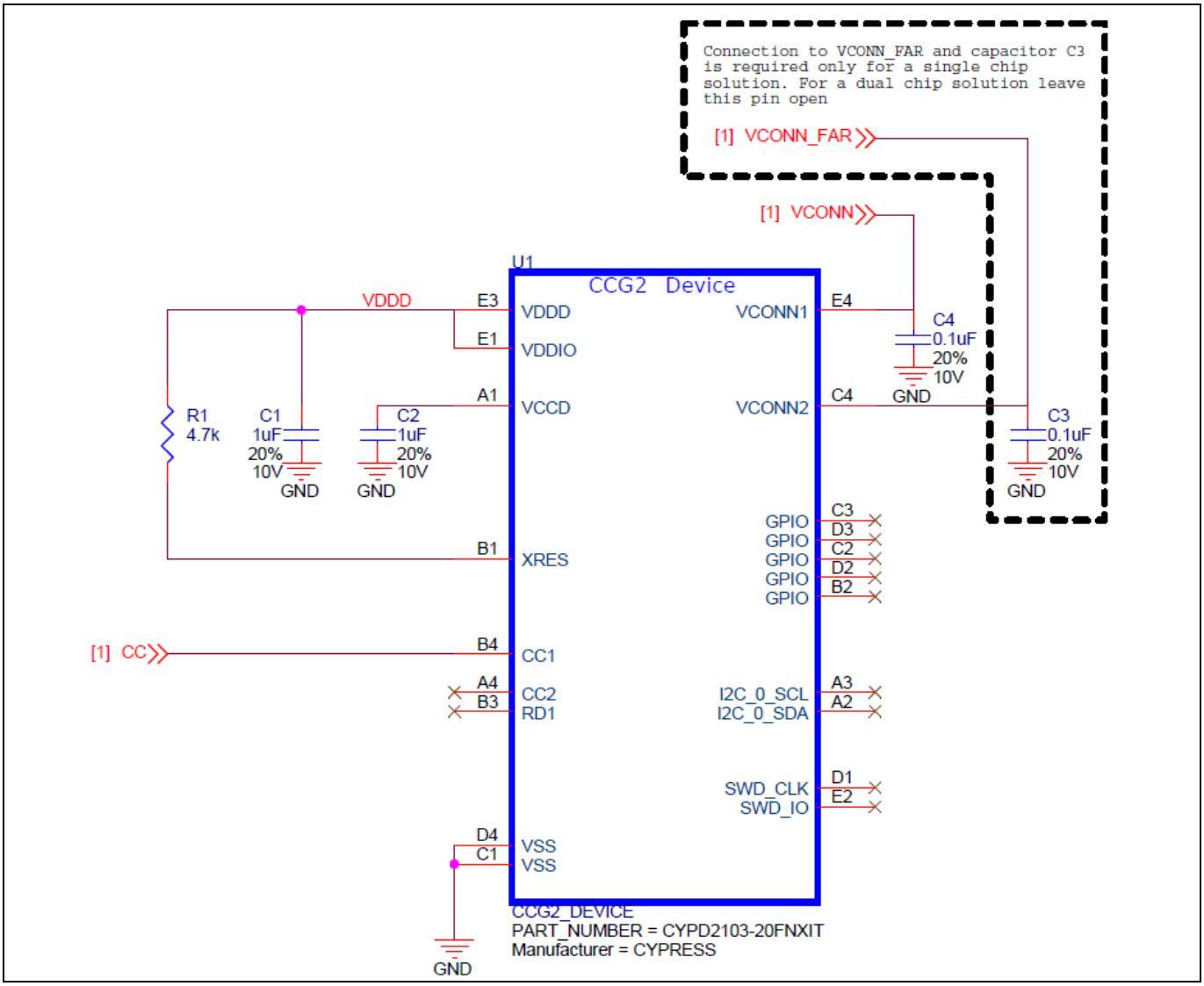


Figure 21 WLCSP-based Reference Schematics (CCG2 controller portion)

Note: Connection to VCONN_FAR and capacitor C3 is required only for a single-chip solution. For a dual-chip solution leave this pin open.

7.3 Paddle Card Reference Schematics for Single/Dual Chip CCG2 (DFN) EMCA – CYPD2103-14LHXIT

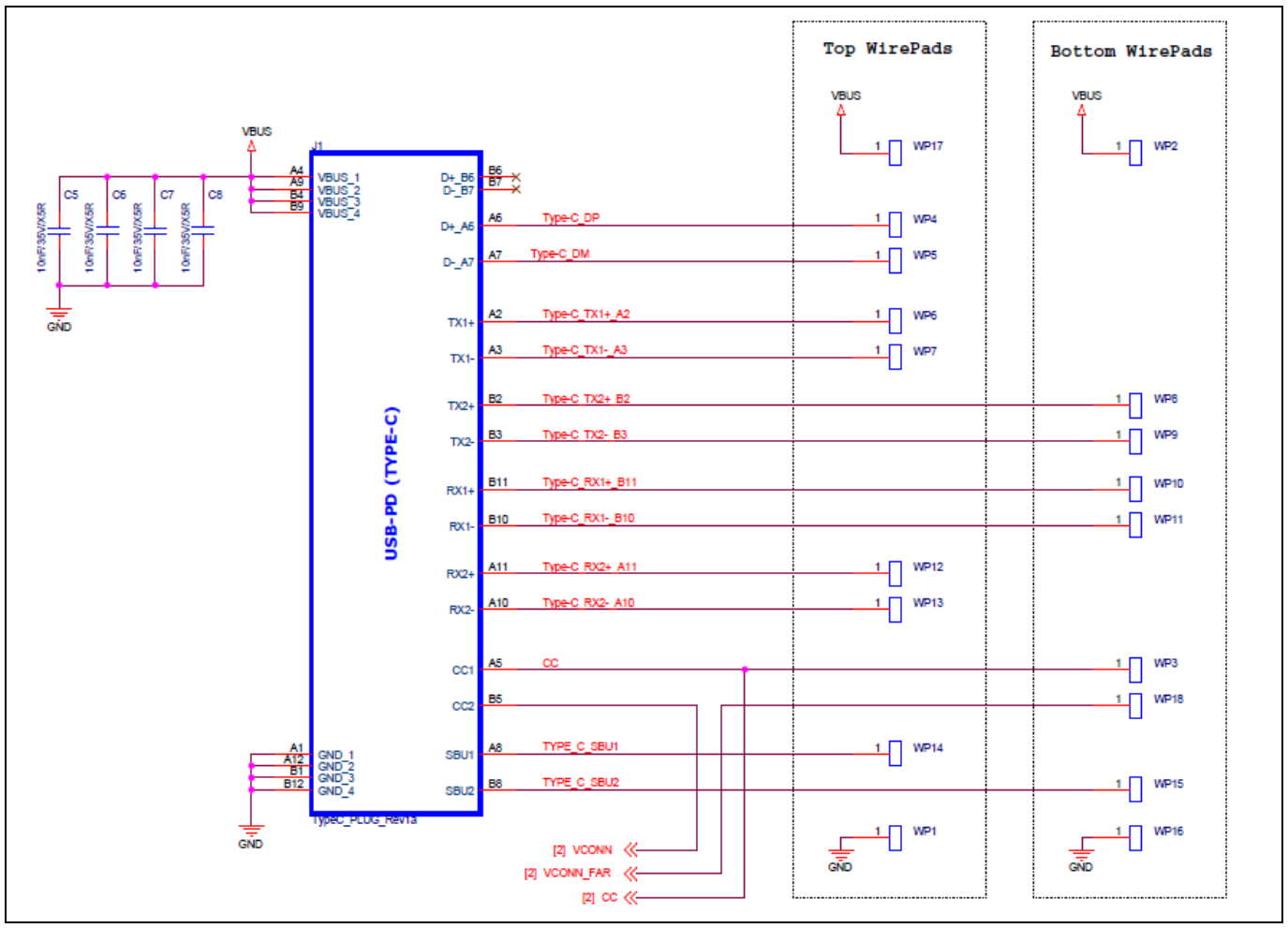


Figure 22 DFN-based Reference Schematics (Type-C connector portion)

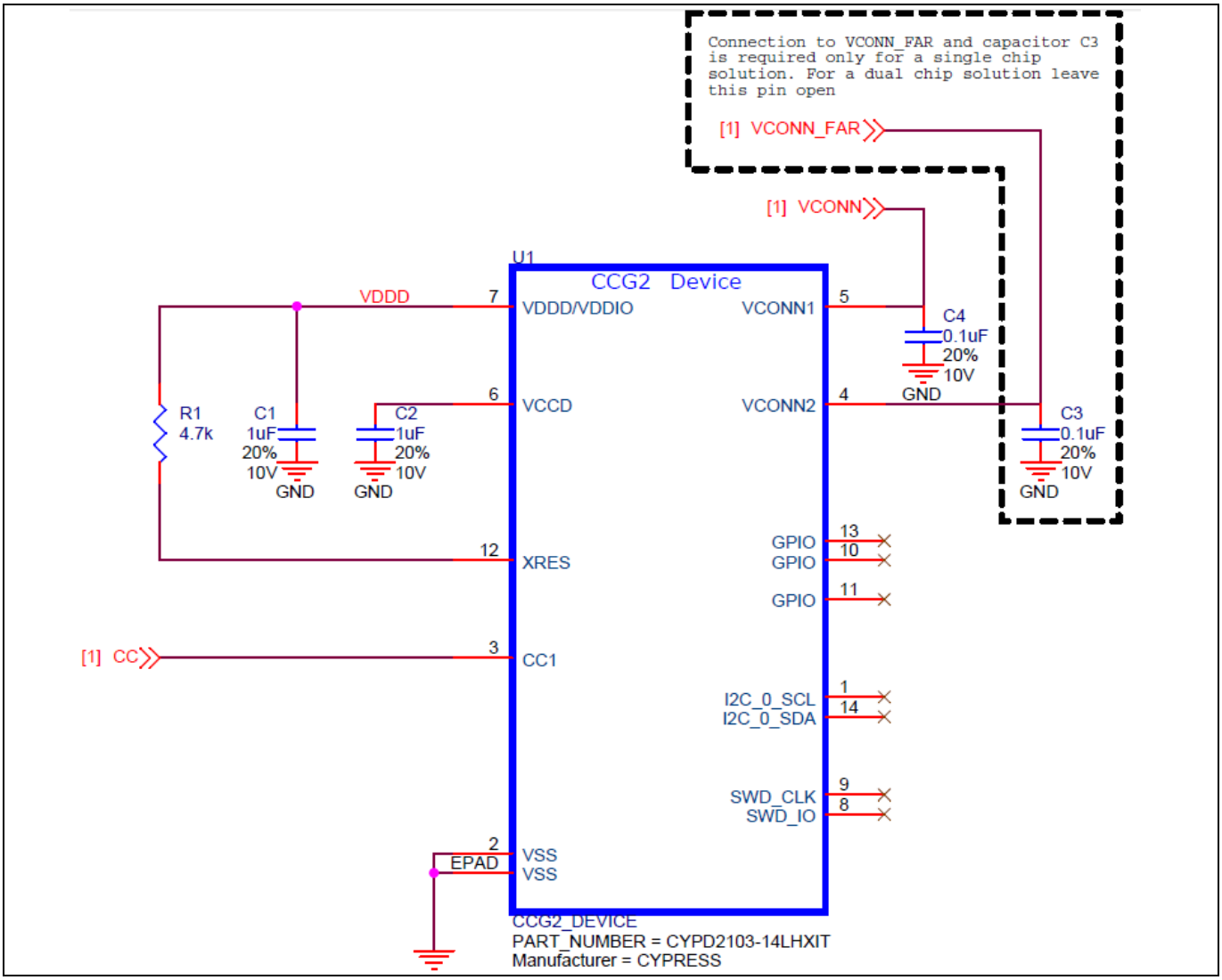


Figure 23 DFN-based Reference Schematics (CCG2 controller portion)

Note: Connection to VCONN_FAR and capacitor C3 is required only for a single-chip solution. For a dual-chip solution leave this pin open.

Revision history

Document version	Date of release	Description of changes
**	2015-04-03	Initial release
*A	2017-04-19	Updated logo and Copyright.
*B	2018-04-17	Updated the title to Hardware Design Guidelines for EMCA/Cable Design using EZ-PD CCG2. Updated the template.
*C	2021-03-01	Updated in Infineon template

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