AN94150

Designing a SuperSpeed Hub Using HX3 with Optimized BOM

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Software Version: NA

Related Application Notes: AN91378, AN92554

AN94150 briefly explains HX3-based SuperSpeed hub designs and gives recommendations for building an optimized SuperSpeed hub solution using HX3 with minimal active and passive components to reduce BOM cost.

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Introduction

HX3 is a family of USB 3.0 hub controllers from Cypress compliant with the USB 3.0 specification revision 1.0. HX3 supports SuperSpeed (SS), Hi-Speed (HS), Full-Speed (FS), and Low-Speed (LS) modes on all ports.

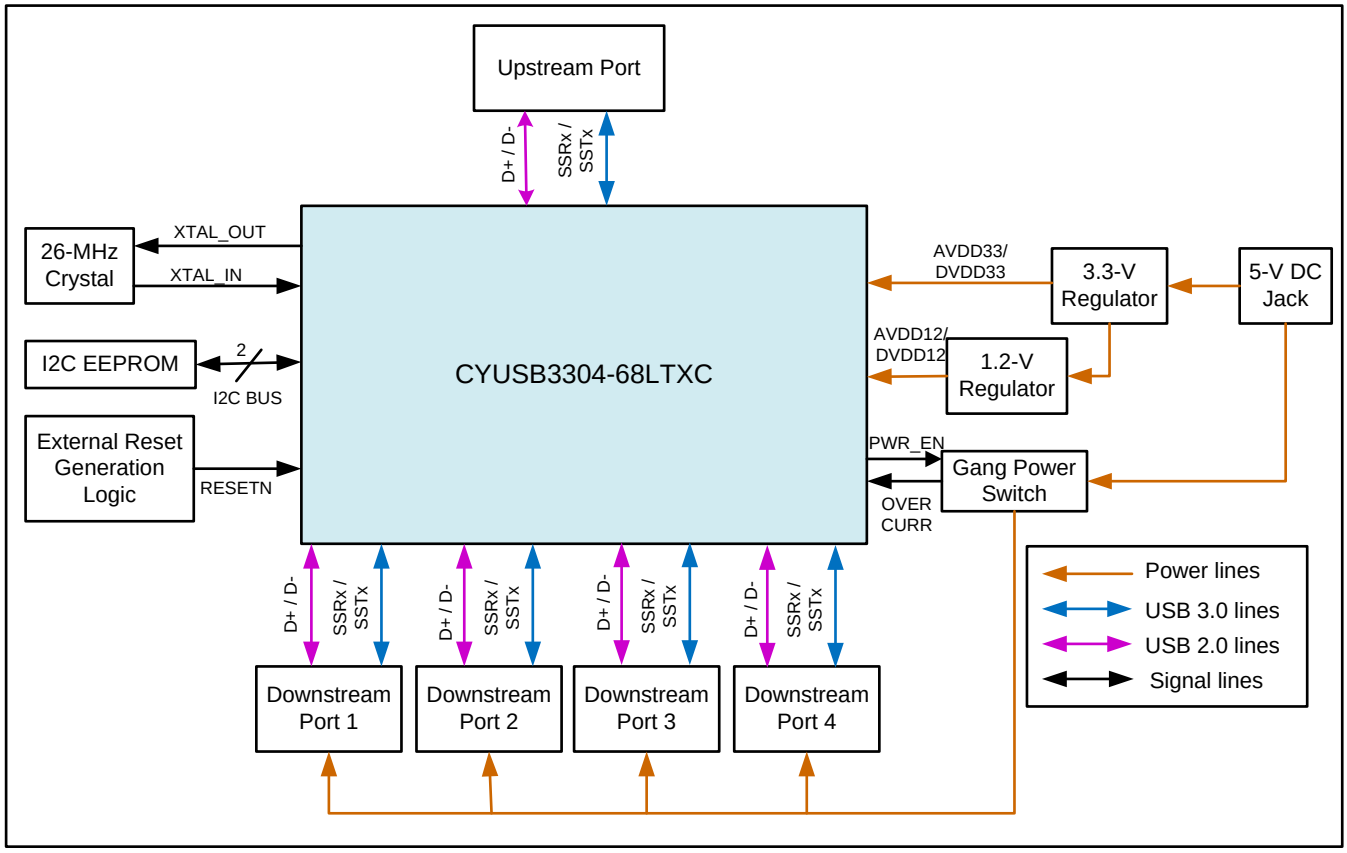
HX3 is available in three product families:

- **Basic:** CYUSB330x (Available in 68-QFN and 100-ball BGA packages): Supports basic hub operations, ganged port power and battery charging features. CY4609 is the reference design kit to evaluate the CYUSB330x family.
- **Intermediate:** CYUSB331x (Available in 88-QFN and 100-ball BGA packages): Supports GPIOs for port indicators, ganged/Individual port power and pin-strap configurations in addition to basic hub features. CY4603 is the development kit to evaluate the CYUSB331x family.
- **Advanced:** CYUSB332x (Available in 88-QFN and 100-ball BGA packages): Supports advanced features such as Shared Link and ACA-Dock. CY4613 is the development kit to evaluate the CYUSB332x family.

Refer to the HX3 datasheet for more details about product options, features, and configurations. Figure 1 shows a block diagram of the HX3-based SuperSpeed hub system using CYUSB3304.

BOM cost and PCB size are major challenges in SuperSpeed hub designs. This application note excludes optional and advanced features such as status indicator LEDs, configuration selection options, Shared Link, and ACA-Dock to reduce BOM cost. Refer to the CYUSB330x-68LTXC/I (68QFN package), CYUSB331x-88LTXC/I (88QFN package), CYUSB332x-LTXC/I (88QFN package) and CYUSB331x-BVXC/I (100-ball BGA package) reference designs for the complete BOM and schematics.

Figure 1. CY4609 (HX3 Reference Design Kit with CYUSB3304) Kit Block Diagram



Design Considerations

This section explains the hardware design requirements for the blocks in the HX3-based system design, including power supply, power domain decoupling, clock, reset, and port power control.

All descriptions and diagrams in this application note are based on the CYUSB330x family. Differences between CYUSB330x and other HX3 family part numbers are explained as applicable.

Power Supply Design

HX3 operates with two power supplies: 3.3 V and 1.2 V DC. They can be generated from a 5-V external power supply using either a switched mode power supply (SMPS) or a linear regulator (LDO). The maximum noise (peak-to-peak) specification on power supplies to the HX3 analog supply (AVDD) pins is 20 mV and to the digital supply (DVDD) pins is 100 mV. Table 1 provides details of the HX3 power domain and the corresponding block it powers.

Power Supply Design Using Switched Mode Power Supply

SMPSs are DC-DC converters. Since the output drivers of SMPS supplies are turned ON and OFF to improve efficiency, an inductor is required to provide continuous current at the output.

Figure 2 shows the schematic of the 5-V (VCC_5 V) to 3.3-V (V3P3) switching regulator.

Figure 2. 5-V to 3.3-V Switching Regulator

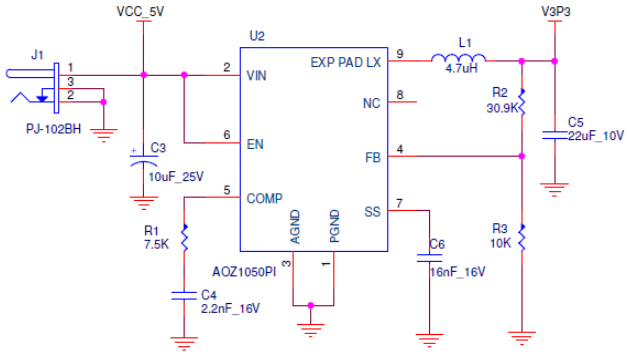
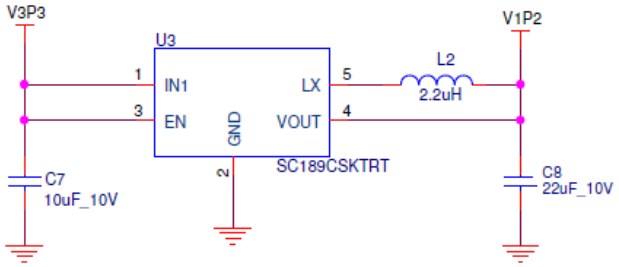


Figure 3 shows the schematic of the 3.3 V (V3P3) to 1.2 V (V1P2) switching regulator.

Figure 3. 3.3 V to 1.2 V Switching Regulator



Power Supply Design Using LDO Regulator

LDO regulators can be used to generate 3.3 V and 1.2 V power supplies from a 5-V power source. They provide regulated output with a low noise level compared to an SMPS. To meet the noise level or ripple requirements of HX3, the LDO output should be bypassed using 10-µF capacitors at both outputs. Figure 4 shows the schematic for 3.3-V (V3P3) power supply generation from a 5-V power source using an LDO voltage regulator.

Figure 4. 3.3 V (V3P3) Power Supply with LDO

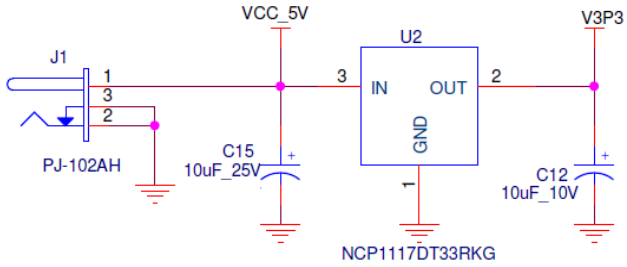
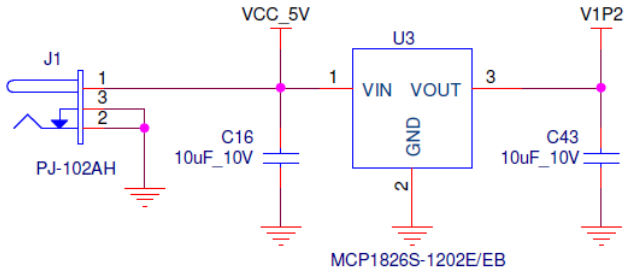


Figure 5 shows the schematic for 1.2 V (V1P2) power supply generation from a 5 V power source using an LDO voltage regulator.

Figure 5. 1.2 V Power Supply with LDO



Power supply design using LDO is considered for a low-BOM design. In summary, this section uses two regulators and four bulk capacitors.

Power Supply Decoupling

Table 1 lists the power domains of the HX3 IC and the corresponding block it powers. This section describes the required decoupling capacitor for each power pin and recommends an optimized solution for a SuperSpeed hub.

Table 1. HX3 Power Domains

Power Domain	I/O Name	Supply Description	I/O Pin Number			Allowed Noise pp (mV)	Voltage (V)			Max Current
			68-QFN	88-QFN	100-ball BGA		Min	Typ	Max	
1.2 V	AVDD12	Clock supply	53	67	A10, D8	20	1.14	1.2	1.26	526 mA from combined 1.2-V power supplies
	AVDD12	USB 3.0 RX	10, 16, 34, 46, 52	15, 21, 44, 56, 62	C9, F9, H1, H10, J2	20				
	DVDD12	USB 3.0 TX	7, 13, 37, 43, 49	12, 18, 47, 53, 59	B10, E1, E10, K3, K9	100				
	DVDD12	Core supply	1, 3, 27	8, 33, 83	D4, D6, F5	100				
	VDD_EFUSE	eFuse	19	24	H3	100				
3.3 V	AVDD33	USB 3.0 PHY	4	9	F3	20	3	3.3	3.6	286 mA from combined 3.3-V power supplies
	AVDD33	USB 2.0	56, 61, 66	70, 75, 80	A4, A7, B6	20				
	VDD_IO	I/O supply	28	34, 66, 88	B4, E7, G6	100				

AVDD12 Power Domain

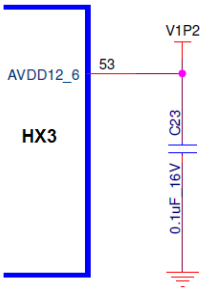
AVDD12 is the 1.2-V analog power supply that powers the blocks described in the following subsections. The recommended schematic for each block is provided.

AVDD12 (Clock)

AVDD12 powers the HX3 crystal oscillator block. Figure 6 shows the connection of the AVDD12 (Clock) line to HX3's crystal oscillator block.

Connect a 0.1-µF capacitor to this power pin to filter RF noise. The capacitor helps reduce the jitter on the reference clock signals.

Figure 6. AVDD12 (Clock)



AVDD12 (USB 3.0 RX)

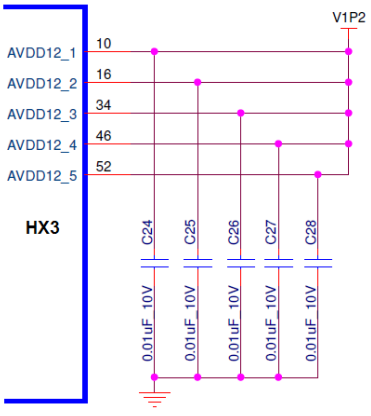
AVDD12 powers the USB 3.0 receiver block.

Figure 7 shows the connection of the AVDD12 (USB 3.0 RX) power domain required for the USB 3.0 RX section.

Connect 0.01-µF capacitors to all these AVDD12 lines to filter the RF noise.

Note A 10-µF bulk capacitor, shown in Figure 8, is shared between the DVDD12 TX and AVDD12 RX supplies. This capacitor protects against any voltage droop on the DS port.

Figure 7. AVDD12 (USB 3.0 RX)



In summary, the AVDD12 power domain uses six decoupling capacitors.

DVDD12 Power Domain

DVDD12 is the 1.2-V digital power supply. It powers the blocks described in the following subsections. The recommended schematic for each block is provided.

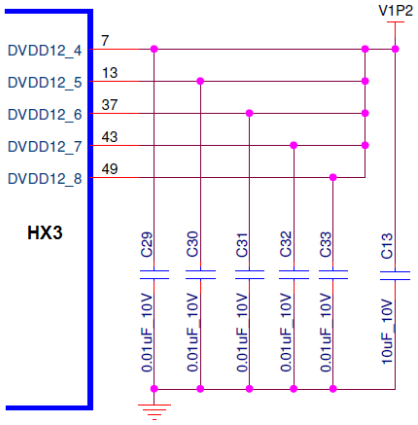
DVDD12 (USB 3.0 TX)

DVDD12 powers the transmit section of the USB 3.0 PHY block. Figure 8 shows the recommended connection for the DVDD12 (USB 3.0 TX) lines.

Connect 0.01-µF capacitors to all these lines to filter the RF noise. In addition, connect a 10-µF bulk capacitor on the DVDD12 (V1P2) supply to protect against voltage droop.

Note The 10-µF bulk capacitor, shown in Figure 8, is shared between the DVDD12 TX and AVDD12 RX supply.

Figure 8. DVDD12 USB 3.0 TX



DVDD12 (Core), VDD_EFUSE (eFuse)

Figure 9 shows the connection circuit of the DVDD12 (Core) and VDD_EFUSE (eFuse) lines. DVDD12 powers the HX3 digital core. VDD_EFUSE provides power to the one-time programmable (OTP) block.

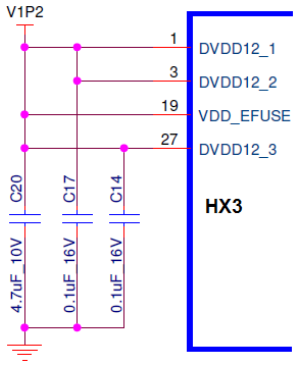
Connect 0.1-µF capacitors on all DVDD12 lines to filter the RF noise. These capacitors are required to meet the signal quality requirements of the USB 3.0 lines. The capacitor for pin 1 and pin 3 can be shared, as these pins are adjacent to each other in the HX3 package.

In addition, connect a 4.7-µF bulk capacitor to the DVDD12 supply to protect against voltage droop.

SMPS supplies are expected to have a ripple voltage higher than the HX3 ripple specification. A ferrite bead is required to isolate the 1.2-V (V1P2) supply from ripples. The ferrite bead can be removed if an LDO is used to generate the 1.2-V supply and this supply meets the HX3 ripple specification.

In summary, the DVDD12 power domain uses seven decoupling capacitors, two bulk capacitors, one 4.7 µF and one 10 µF.

Figure 9. DVDD12 Core, EFUSE



AVDD33 Power Supply

AVDD33 is the 3.3-V analog power supply that powers the blocks described in the following subsections. The recommended power supply connection for each section is provided.

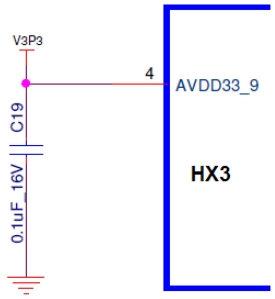
AVDD33 (USB 3.0 PHY)

The AVDD33 supply powers the CDR (clock and data recovery) block in USB 3.0 PHY. Figure 10 shows the schematic of the AVDD33 (USB 3.0 PHY) lines.

Connect 0.1-µF capacitors on all AVDD33 power pins to filter the RF noise.

SMPS supplies are expected to have a ripple voltage higher than the HX3 specification of 20 mV pp. A ferrite bead is required to isolate the analog supply from other sections of the design. The ferrite bead can be removed if an LDO is used to generate the 3.3-V (V3P3) supply, which provides an output with less than 20-mV ripple.

Figure 10. AVDD33 (USB 3.0 PHY)



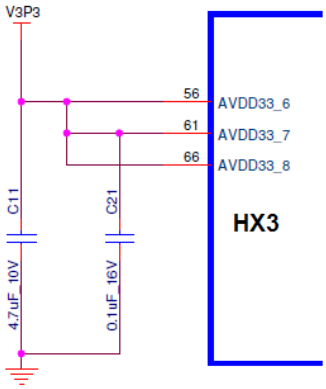
AVDD33 (USB 2.0)

AVDD33 (USB 2.0) powers the USB 2.0 transceiver. Figure 11 shows the connection of the AVDD33 (USB 2.0) lines.

Connect one 0.1-µF capacitor on the AVDD33 (USB 2.0) lines to filter the RF noise, as required to meet the USB-IF signal quality requirements of the USB 2.0 lines. The capacitor for pin 56, pin 61, and pin 66 can be shared, as these pins are adjacent in the HX3 package. See Table 1 for corresponding ball numbers of BGA package.

In addition, connect one 4.7-µF bulk capacitor to the AVDD33 supply to protect against voltage droop.

Figure 11. AVDD33 (USB 2.0)

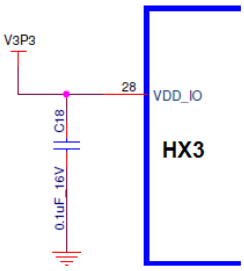


AVDD33 (VDD_IO)

The VDD_IO supply powers the I/O circuits in HX3. Figure 12 shows the connection of the VDD_IO line.

Connect one 0.1-µF capacitor on the VDD_IO line to filter the RF noise.

Figure 12. VDD_IO Supply Connection



Configuration Mode Selection

Refer to Table 4 in the HX3 datasheet for details on HX3 configuration mode select. By default, HX3 loads all configurations from an internal ROM (internal ROM mode). HX3 also provides an option to load custom configurations from an external I²C EEPROM (I²C EEPROM mode). These configuration parameters include VID, PID, number of active ports, number of removable ports, charging support enable/disable, and so on. Refer to Table 6 in the HX3 datasheet for a complete list of configuration options and default settings.

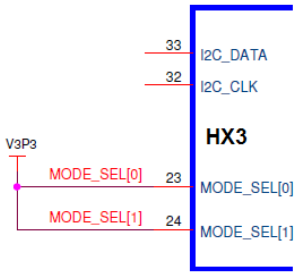
The following sections provide hardware design considerations for the internal ROM mode and external I²C EEPROM mode of configuration selection.

Internal ROM Mode

Figure 13 shows the schematic of the MODE_SEL [1:0] and I2C lines for the internal ROM mode selection.

MODE_SEL[1:0] pins should be connected HIGH (to V3P3 to select internal ROM configurations. I2C lines are not used during this configuration. The I2C_DATA and I2C_CLK lines can be left floating in this mode.

Figure 13. MODE_SEL and I2C Line Connection for Internal ROM Configuration



External I²C EEPROM Mode

In the external I²C EEPROM mode, HX3 MODE_SEL[1:0] should be set to 2'b01 (I²C master mode) to load custom configurations from an external EEPROM connected to the HX3 I²C interface. MODE_SEL[1] should be connected to GND, and MODE_SEL[0] should be connected to VDD_IO.

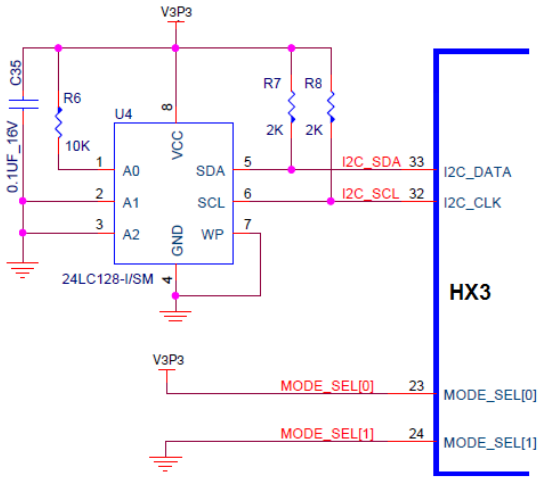
A custom configuration file can be generated using the GUI-based Blaster Plus tool provided by Cypress. Refer to the Blaster Plus User Guide for more details on generating this file.

The configuration data length can vary from 11 bytes to 197 bytes. The recommended EEPROM size is 256 bytes or more in this mode, and the recommended EEPROM type number is 24LC02B.

A custom firmware with configuration settings can also be loaded from an external EEPROM. The HX3 firmware image size is about 10 KB, the recommended EEPROM size is 16 KB, and the recommended EEPROM type number is 24LC128.

Figure 14 shows the schematic of the MODE_SEL and I2C lines for the External EEPROM configuration mode.

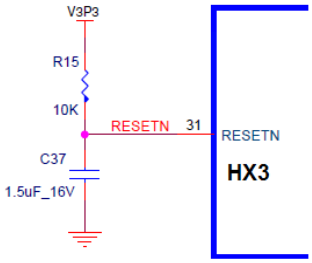
Figure 14. MODE_SEL and I2C Line Connection for EEPROM Configuration



Reset

The RESETN pin should be held LOW until both the 3.3-V (V3P3) and 1.2-V (V1P2) supplies become stable. The RESETN pin can be tied to the 3.3-V (V3P3) supply through an external resistor and to ground (GND) through an external capacitor, as shown in Figure 15. The RC circuit should have a minimum 5-ms time constant to create a clean reset signal for the power-on reset (POR) cycle.

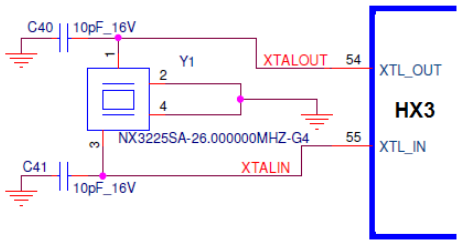
Figure 15. Reset Circuit



Clock

HX3 requires an external crystal with a frequency of 26 MHz and an accuracy of ±150 ppm in parallel resonant, fundamental mode. The crystal drive circuit is capable of a low-power drive level (<200 µW). Figure 16 shows the crystal connection to the XTL_OUT and XTL_IN pins.

Figure 16. Crystal Connection



Refer to the AN91378 – HX3 Hardware Design Guidelines and Schematic Checklist "Crystal Requirements" section for details on crystal power dissipation and calculating load capacitance values.

Downstream Port Power Management

Power Switch

Figure 17 shows the schematic of the port power connection in ganged mode operation. One power switch controls power to all the downstream ports. It is controlled by the HX3 power enable (PWR_EN) signal. The power switch also indicates an overcurrent condition to HX3 (through OVRCURR) to turn off power to downstream ports.

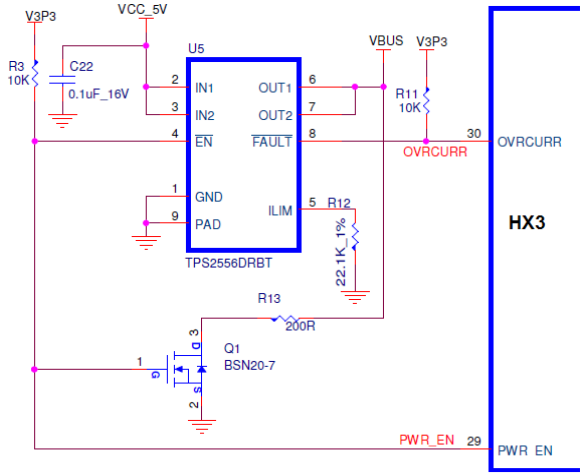
The HX3 CYUSB330x family (68-pin QFN and 100-ball BGA packages) supports ganged power switching in which the power to all four DS ports is controlled with one power enable (PWR_EN) signal. An advantage of ganged mode is that one power switch controls the power to all the DS ports, which helps in reducing the BOM.

A disadvantage of the ganged mode is that when an overcurrent condition occurs on a DS port , the power to all the DS ports is turned OFF because the port power control is connected in ganged mode.

The PWR_EN and OVRCURR pins are open-drain and therefore need to be pulled HIGH to VDD_IO using 10-kΩ resistors.

It is recommended to connect a MOSFET (Q1) at the power switch output for faster discharge of the potential across 150-µF capacitors connected on VBUS of the DS ports.

Figure 17. Power Switch for Ganged Mode



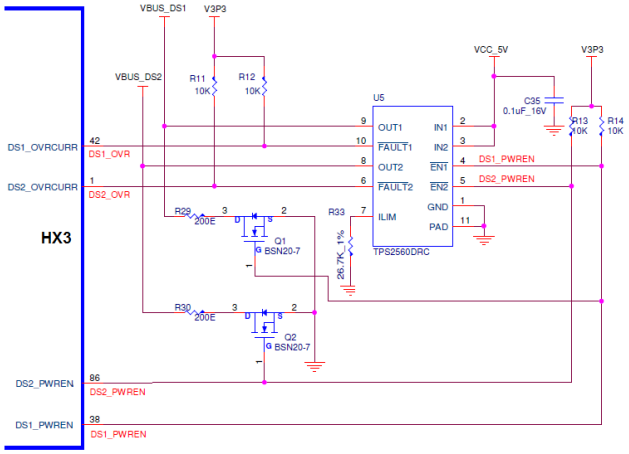
The HX3 CYUSB331x and CYUSB332x families (88-pin QFN and 100-ball BGA packages) support individual port power switching. In this mode, the power for each DS port is controlled by separate power enable signals. A dual-channel power switch is used to independently control the power to the DS ports.

Figure 18 shows the schematic of the power switch connection for the two DS ports in individual port power mode with a dual-channel power switch.

An advantage of the individual port power switching is that each DS port power is controlled independently, so that when an overcurrent condition occurs on a DS port, the power to that particular DS port alone is turned OFF while the remaining DS ports continue to function normally.

A disadvantage of individual port power switching is that because the DS ports need to be controlled independently, two control signals (PWR_EN_DS and OVCUR_DS) are required per DS port. This requires more power and overcurrent-detection ICs.

Figure 18. Port Power Switch for Individual Mode



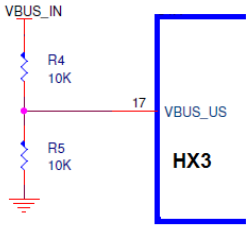
Polyfuse

A polyfuse can be used instead of the power switch on the downstream ports. When an overcurrent condition occurs, the resistance of the polyfuse increases and will eventually create an “OPEN” condition causing the power to the DS port turned OFF. When the overcurrent fault condition is removed, the resistance will reset automatically, and the power to the DS port resumes. When a polyfuse is used, there is a continuous VBUS on the downstream ports, which is cut off only when an overcurrent condition occurs. The continuous availability of VBUS on a downstream port causes the USB compliance test to fail. Therefore, it is recommended to use the port power switch to control DS port power.

Upstream VBUS Detection

HX3 detects a connection to the USB Host controller through the HX3 VBUS_US pin. This pin should be connected to the VBUS from the US port so that when the US port is connected to the USB Host, HX3 detects the VBUS connection. HX3 detects VBUS disconnection when the VBUS_US pin drops below 2.1 V. It is recommended to use a voltage divider as shown in Figure 19 on the VBUS_US pin for faster detection of VBUS connection and disconnection.

Figure 19. US VBUS Detection



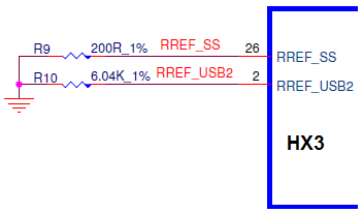
USB Precision Resistors

Figure 20 shows USB precision resistors used.

Connect RREF_SS to the precision resistor (200-Ω+/- 1%) for SuperSpeed PHY termination impedance calibration.

Connect RREF_USB2 pin to a precision resistor (6.04 kΩ+/- 1%) to generate a current reference to USB 2.0 PHY.

Figure 20. USB Precision Resistors

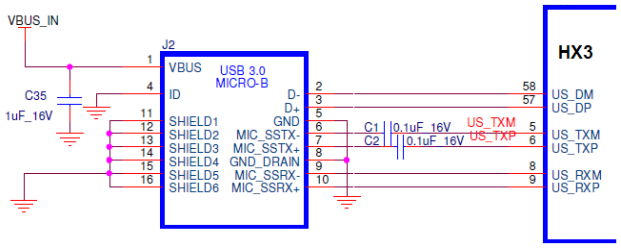


Upstream (US) Connector

Figure 21 shows the schematics for US (upstream) port connection.

Connect a 1-µF bypass capacitor to the VBUS input line. Connect 0.1-µF coupling capacitors to US_TXM and US_TXP lines.

Figure 21. US Connector



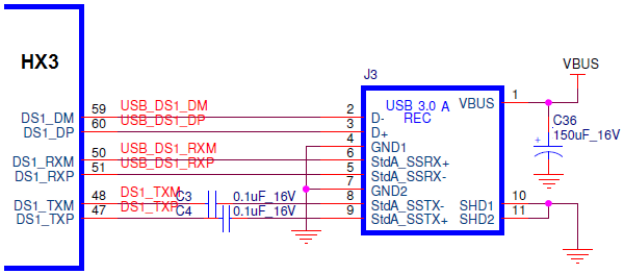
Downstream (DS) Connectors

Figure 22 shows the DS port connection for the DS1 port. Connection circuits remain similar for DS2, DS3, and DS4 ports.

Connect a 150-µF bypass capacitor on VBUS_DS output lines of all DS ports.

Connect 0.1-µF coupling capacitors in DS_TXM and DS_TXP lines of all DS ports.

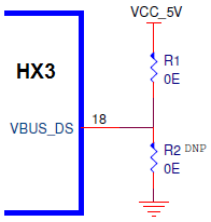
Figure 22. DS Connector



Apple Charging Enable

The HX3 VBUS_DS pin is used to enable Apple charging circuit in HX3. Battery charging v1.2 (BC v1.2) compliance test will fail when Apple charging circuit is enabled. Therefore, it is recommended to connect the VBUS_DS pin to a local 5-V supply for normal operation and to connect to GND for BC v1.2 compliance testing. Figure 23 provides the recommended connection for the VBUS_DS pin. R2 is DNP (Do not populate) for normal operation. See Application note on Battery Charging (AN92554) Features for more details.

Figure 23. Apple Charging Enable

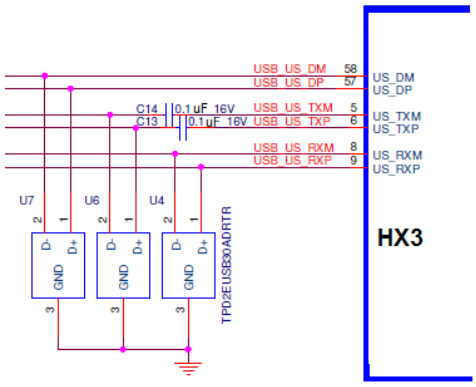


ESD Protection

ESD diodes are not mandatory for hubs because HX3 has a built-in ESD protection of 2.2-kV Human Body Model (HBM). If a higher level of ESD protection is required, an additional ESD diode can be added to all USB 2.0 and USB 3.0 lines.

Figure 24 shows a reference schematic for ESD protection on the USB 3.0 port. This ESD protection circuit is marked as “NL – No Load” by Cypress in the Reduced BOM Schematics.

Figure 24. ESD Diode Connection on USB Lines



Reduced BOM and Schematics

Table 2 provides an optimized BOM for an HX3-based hub design. Refer to the Reduced BOM Schematic of CYUSB330x-68LTXC/I (68-QFN package), CYUSB331x-88LTXC/I (88-QFN package), CYUSB332x-LTXC/I (88-QFN package) and CYUSB331x-BVXC/I (100-ball BGA package) for more details.

Table 2. BOM for HX3

Section	CYUSB3304		CYUSB3314		Recommended Part*	
	Component	Count	Component	Count	Manufacturer	Part Number
Power Regulator	Regulator	2	Regulator	2	ON Semiconductor	NCP1117DT33RKG
					Microchip Technology	MCP1826S-1202E/EB
	Capacitor - 10 µF	4	Capacitor - 10 µF	4	AVX Corporation	TPSB106K025R1800
					Taiyo Yuden	LMK212B7106KG-TD
Power Decoupling	Capacitor - 10 µF	1	Capacitor - 10 µF	1	Taiyo Yuden	LMK212B7106KG-TD
	Capacitor - 4.7 µF	2	Capacitor - 4.7 µF	2	Samsung Electro-Mechanics America, Inc.	CL21A475KPFNNNE
	Capacitor - 0.1 µF	6	Capacitor - 0.1 µF	8	Yageo	CC0402KRX7R7BB104
	Capacitor - 0.01 µF	10	Capacitor - 0.01 µF	10	Kemet	C0402C103K8RACTU
Reset Circuit	Capacitor - 1.5 µF	1	Capacitor - 1.5 µF	1	TDK Corporation	C1608X5R1C155K080AB
	Resistor - 10 kΩ	1	Resistor - 10 kΩ	1	Panasonic	ERJ-3EKF1002V
Clock	Crystal	1	Crystal	1	NDK	NX3225SA-26.000000MHZ-G4
	Capacitor - 10 pF	2	Capacitor - 10 pF	2	Kemet	C0603C100J4GACTU

Section	CYUSB3304		CYUSB3314		Recommended Part*	
	Component	Count	Component	Count	Manufacturer	Part Number
Power Switch	Power switch	1	Power switch	2	Texas Instruments	TPS2556DRBT
					Texas Instruments	TPS2560DRCT
	Capacitor - 0.1 µF	1	Capacitor - 0.1 µF	2	Yageo	CC0402KRX7R7BB104
	Resistor - 22.1 kΩ	1	Resistor - 26.7 kΩ	2	Panasonic	ERJ-2RKF2212X
	Resistor - 10 kΩ	2	Resistor - 10 kΩ	8	Panasonic	ERJ-3EKF1002V
	Resistor - 200 Ω	1	Resistor - 200 Ω	4	Stackpole Electronics, Inc.	RMCF0805JT200R
	MOSFET	1	MOSFET	4	Diodes Inc	BSN20-7
US VBUS Detect	Resistor - 10 kΩ	2	Resistor - 10 kΩ	2	Panasonic	ERJ-3EKF1002V
USB Precision Resistors	Resistor - 200 Ω	1	Resistor - 200 Ω	1	Panasonic	ERJ-2RKF2000X
	Resistor - 6.04 kΩ	1	Resistor - 6.04 kΩ	1	Panasonic	ERJ-2RKF6041X
US Connector	US Connector	1	US Connector	1	Hirose Electric Co. Ltd.	ZX360D-B-10P
	Capacitor - 1 µF	1	Capacitor - 1 µF	1	TDK Corporation	C1005X5R1C105M
	Capacitor – 0.1 µF	2	Capacitor – 0.1 µF	2	Yageo	CC0402KRX7R7BB104
DS Connectors	DS Connector	4	DS Connector	4	FOXCONN	UEA1112C-4HK1-4H
	Capacitor - 150 µF	4	Capacitor - 150 µF	4	Panasonic	EEE-FK1C151XP
	Capacitor - 0.1 µF	8	Capacitor - 0.1 µF	8	Yageo	CC0402KRX7R7BB104
Apple Charging Enable	Resistor - 0.0 Ω	1	Resistor - 0.0 Ω	1	Yageo	RC0603JR-070RL
DC Power Jack	Power Jack	1	Power Jack	1	CUI, Inc.	PJ-102BH
	Total	63	Total	80		

* **Note** Use the recommended manufacturer and part number as a guideline. You can choose alternative parts with equivalent specifications wherever applicable.

Summary

This application note provided the guidelines for designing a HX3-based SuperSpeed hub design with an optimized BOM reducing the cost of manufacturing and design. The consolidated BOM and schematics are available online.

Related Application Notes

AN91378 - HX3 Hardware Design Guidelines and Schematic Checklist

AN92554 - Implementing Battery Charging Features using HX3

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4606024	HBM	02/05/2015	Initial version
*A	5797719	AESATMP9	07/04/2017	Updated logo and copyright.
*B	6075116	HBM	02/19/2018	Sunset review; no content updates

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