AN91378

HX3 Hardware Design Guidelines and Schematic Checklist

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Related Application Notes: None

AN91378 provides hardware design and PCB layout guidelines for HX3, a high-performance USB 3.0 hub. These guidelines will help to ensure best performance with respect to signal integrity and full electrical compliance with the USB 3.0 Specification. Refer KBA96321 for Supporting ACA-Dock Feature in Smartphone and Tablet Docks with HX3 USB 3.0 Hub Controller.

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Introduction

HX3 is a family of USB 3.0 hub controllers compliant with the USB 3.0 specification revision 1.0. HX3 supports SuperSpeed (SS), Hi-Speed (HS), Full-Speed (FS), and Low-Speed (LS) on all the ports. It has integrated termination, pull-up, and pull-down resistors, and supports configuration options through pin-straps to reduce the overall BOM of the system.

HX3 includes the following Cypress-proprietary features:

Shared Link™: Enables extra downstream (DS) ports for on-board connections in embedded applications. Shared Link enables a USB 3.0 port to be split into an embedded SS port and a standard USB 2.0 port.

For example, if one of the DS ports is connected to an embedded SS device, such as a USB 3.0 camera, HX3 enables the system designer to reuse the USB 2.0 signals of that specific port to connect to a standard USB 2.0 device. In this way, you can

implement an application with up to a total of eight devices (four SS-only and four standard USB 2.0 devices) using a single HX3 enabled with Shared Link support.

Ghost Charge™: Enables charging of devices connected to the DS ports when no Host is connected on the upstream (US) port.

Table 1 lists the HX3 product options.

This application note provides hardware guidelines for a hub system based on HX3.

Table 1. HX3 Product Options

Features	CYUSB3302	CYUSB3304	CYUSB3312	CYUSB3314	CYUSB3326	CYUSB3328
Number of DS ports	2 (USB 3.0)	4 (USB 3.0)	2 (USB 3.0)	4 (USB 3.0)	6 (2 USB 3.0, 2 SS, 2 USB 2.0)	8 (4 SS, 4 USB 2.0)
Number of Shared Link ports	0	0	0	0	2	4
BC v1.2	Yes	Yes	Yes	Yes	Yes	Yes
ACA-Dock*	No	No	No	No	No	Yes
External Power Switch Control	Ganged	Ganged	Individual and Ganged	Individual and Ganged	Individual	Individual
Pin-Strap support	No	No	Yes	Yes	Yes	Yes
I^2C	Yes	Yes	Yes	Yes	Yes	Yes
Vendor command	Yes	Yes	Yes	Yes	Yes	Yes
Port indicators	No	No	Yes	Yes	No	No
Packages	68-pin QFN	68-pin QFN	88-pin QFN	88-pin QFN	88-pin QFN	88-pin QFN
Temperature range	Industrial and Commercial	Industrial and Commercial	Industrial and Commercial	Industrial and Commercial	Industrial and Commercial	Industrial and Commercial

Note

* Refer KBA96321 for Supporting ACA-Dock Feature in Smartphone and Tablet Docks with HX3 USB 3.0 Hub Controller.

Schematic Design Requirements

This section explains the schematic design requirements of HX3's various blocks.

Power System

HX3 operates with two external power supplies, 3.3 V and 1.2 V. Figure 1 and Figure 2 show the recommended power supply decoupling scheme for designs using HX3. Table 2 provides the maximum operating current for the two power supplies.

Table 2. HX3 Power Domains

Parameter	Description	Min	Typical	Max	Maximum Operating Current [1]
AVDD12	1.2-V analog supply	1.14 V	1.2 V	1.26 V	526 mA from combined 1.2-V power supplies
DVDD12	1.2-V core supply	1.14 V	1.2 V	1.26 V	
AVDD33	3.3-V analog supply	3 V	3.3 V	3.6 V	286 mA from combined 3.3-V power supplies
VDDIO	3.3-V I/O supply	3 V	3.3 V	3.6 V	

Note

1. Test condition: All SS and USB 2.0 ports are active with data transfer, at maximum voltage and temperature = 85 °C.

Figure 1. Power System Recommendation for 68-Pin QFN Package

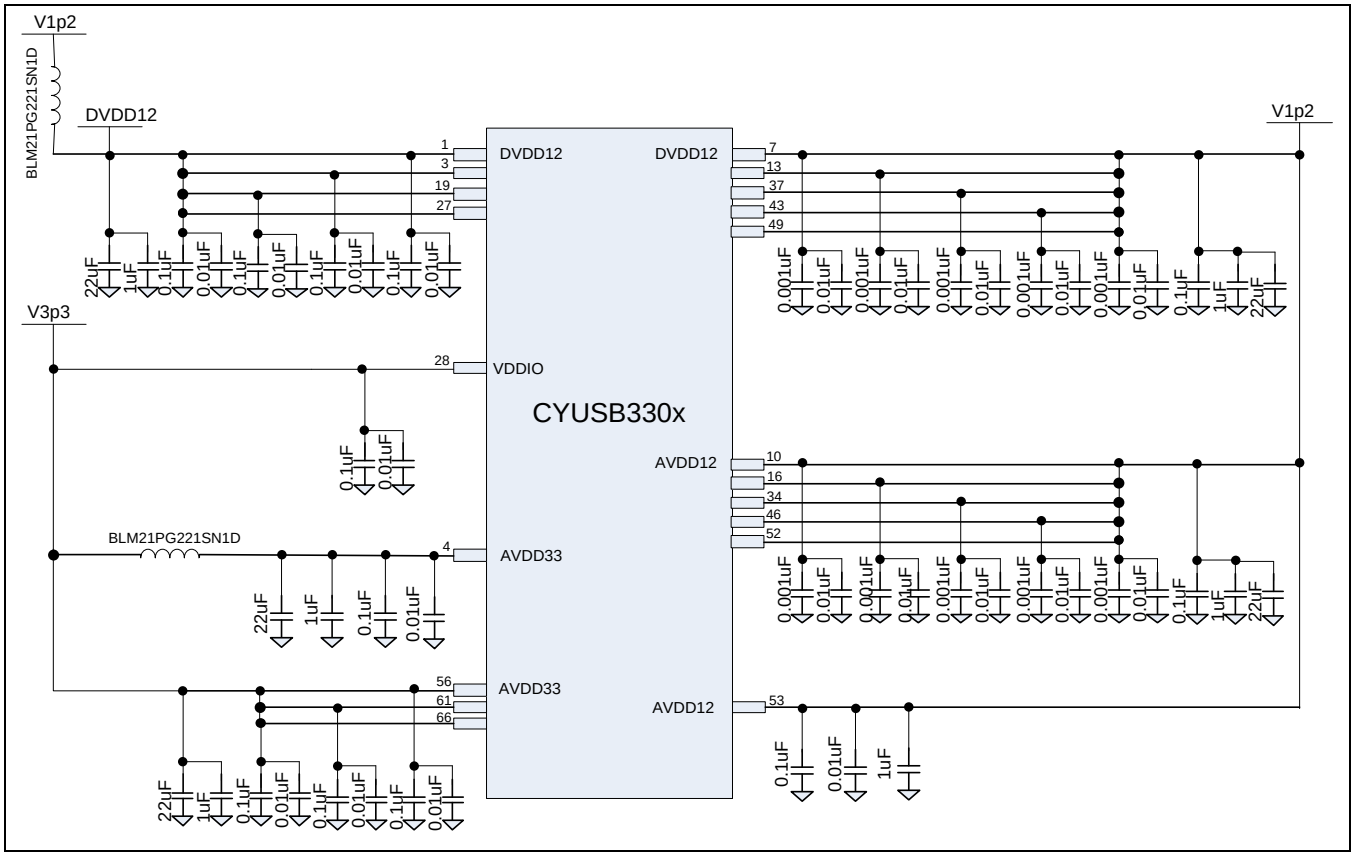


Table 3 lists the bulk capacitors that need to be connected for a group of power pins for a 68-pin QFN package along with the decoupling capacitors per power pin.

Table 3. Decoupling and Bulk Capacitor Requirements for 68-Pin QFN Package

Power Domain (Pin Numbers)	Description	Bulk Capacitors for Group	Decoupling Capacitors per Pin
AVDD12 (10,16,34,46,52)	1.2 V for SS Rx	0.1 µF, 1 µF, and 22 µF	0.001 µF and 0.01 µF
AVDD12 (53)	1.2 V for crystal oscillator	1 µF	0.01 µF and 0.1 µF
DVDD12 (1,3,19,27)	1.2 V for core	1 µF and 22 µF	0.01 µF and 0.1 µF
DVDD12 (7,13,37,43,49)	1.2 V for SS Tx	0.1 µF, 1 µF, and 22 µF	0.001 µF and 0.01 µF
AVDD33 (56,61,66)	3.3 V for USB 2.0 PHY	1 µF and 22 µF	0.01 µF and 0.1 µF
AVDD33 (4)	3.3 V for SS PHY	1 µF and 22 µF	0.01 µF and 0.1 µF
VDDIO (28)	3.3 V for GPIOs		0.01 µF and 0.1 µF

Note A ferrite bead is required to isolate AVDD33 (3.3-V USB 3.0 PHY) from the noisy supplies VDDIO (3.3 V for GPIOs) and AVDD33 (3.3 V USB 2.0 PHY), as shown in Figure 1. For the 1.2-V power supply, as shown in Figure 1, a ferrite bead is required to isolate the noisy power supply (1.2-V core supply) from the domains that need clean power supply (1.2 V for SS Rx, Tx and crystal oscillator). Failure to include these ferrite beads may result in compliance testing failure.

Figure 2. Power System Recommendation for 88-Pin QFN Package

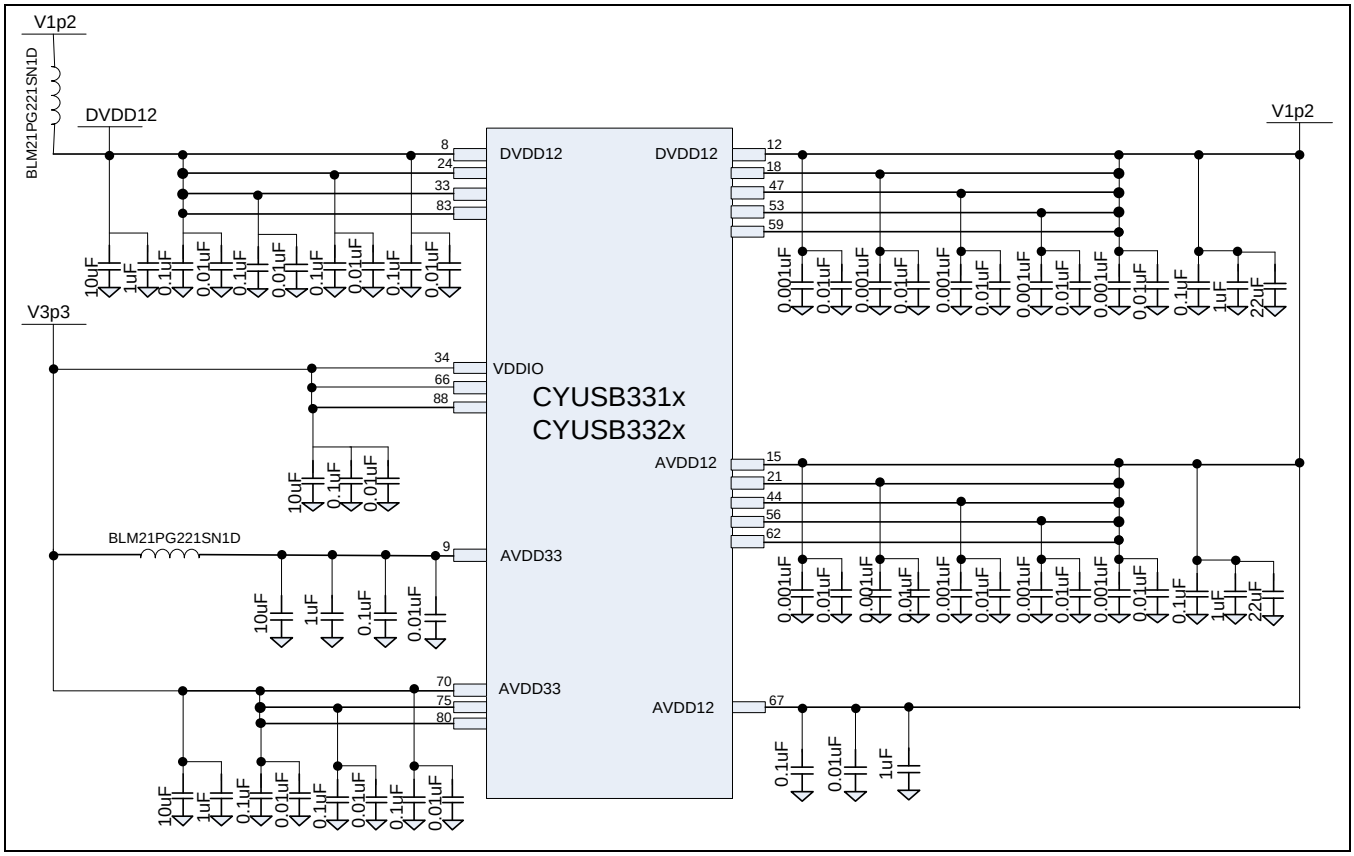


Table 4 lists the bulk capacitors that need to be connected for a group of power pins for an 88-pin QFN package along with the decoupling capacitors per power pin.

Table 4. Decoupling and Bulk Capacitor Requirements for 88-Pin QFN Package

Power Domain (Pin Numbers)	Description	Bulk Capacitor for Group	Decoupling Capacitor per Pin
AVDD12 (15,21,44,56,62)	1.2 V for SS Rx	0.1 µF, 1 µF, and 22 µF	0.001 µF and 0.01 µF
AVDD12 (67)	1.2 V for crystal oscillator	1 µF	0.01 µF and 0.1 µF
DVDD12 (8,24,33,83)	1.2 V for core	1 µF and 10 µF	0.01 µF and 0.1 µF
DVDD12 (12,18,47,53,59)	1.2 V for SS Tx	0.1 µF, 1 µF, and 22 µF	0.001 µF and 0.01 µF
AVDD33 (70,75,80)	3.3 V for USB 2.0 PHY	1 µF and 10 µF	0.01 µF and 0.1 µF
AVDD33 (9)	3.3 V for SS PHY	1 µF and 10 µF	0.01 µF and 0.1 µF
VDDIO (34,66,88)	3.3 V for GPIOs	10 µF, 0.01 µF and 0.1 µF	

Note A ferrite bead is required to isolate AVDD33 (3.3-V USB 3.0 PHY) from the noisy supplies VDDIO (3.3-V for GPIOs) and AVDD33 (3.3-V USB 2.0 PHY), as shown in Figure 2. For the 1.2-V power supply, as shown in Figure 2, a ferrite bead is required to isolate the noisy power supply (1.2-V core supply) from the domains that need clean power supply (1.2 V for SS Rx, Tx and crystal oscillator). Failure to include these ferrite beads may result in compliance testing failure.

Power Requirement

The power system must be designed to meet the power consumption requirement of HX3 and DS devices.

Table 2 shows the maximum power consumption of HX3 with four active DS ports. HX3's total power consumption will be less in applications requiring less than four ports. Refer Appendix A for the expected power consumption under various configurations. The power system must also provide the required power to each DS port, depending on the port configuration (whether BC is supported). Refer Table 5 for DS port current requirement.

Table 5. DS Port Current Requirement

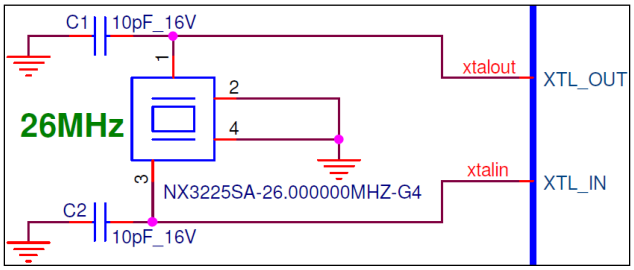
DS Port Configuration	Battery Charging	Current (mA)
USB 3.0	None	900
	BC v1.2	1500
	Apple	2100
USB 2.0	None	500
	BC v1.2	1500
	Apple	2100

Crystal Requirements

HX3 requires an external crystal with the following parameters:

- 26 MHz ±150 ppm
- Parallel resonant, fundamental mode
- 200 µW minimum drive level

Figure 3. Crystal Circuit



Crystal Power Dissipation

The power dissipation of the crystal depends on

- The voltage level of the XTL_OUT pin (maximum voltage on AVDD12 pin is 1.26 V)
- The operating frequency (26 MHz)
- The equivalent series resistance (ESR) of the crystal

Equation 1. Power Dissipation of the Crystal

$$P = I^2R = \left(\frac{V_x}{|Z|}\right)^2 R$$

$$= 2[\pi f\ (C_0 + C_L)\ V_x]^2\ R$$

Where:

f is the crystal frequency,

C_0 is the shunt capacitance of the crystal obtained from the crystal data sheet,

C_L is the load capacitance, for C_L calculation, refer next section,

R is the crystal ESR obtained from the data sheet of the crystal,

V_x is the maximum voltage on AVDD12 pin – 1.26 V.

The parameters of the crystal (NX3225SA-26.000000MHZ-G4 as shown in Figure 3) used in HX3's development kits are as follows:

f = 26 MHz, C_0 = 1.22 pF, C_L = 10 pF, R = 50 Ω.

Using Equation 1, the power dissipation for this crystal is 133 µW. This is less than the 200-µW crystal drive level.

Use of a crystal with a drive level less than the crystal's power dissipation may result in accelerated aging or even burnout of the crystal.

The other recommended crystals are:

- NX3225SA-26.000MHZ-STD-CSR-1
- TSX-3225 26.0000MF09Z-AC3

Note Do not connect any series resistor to the XTL_OUT and XTL_IN pins of the crystal. Placing a series resistor will add resistance to the crystal ESR, resulting in increased crystal power dissipation and startup time.

Calculating Load Capacitance Values

Load capacitance C_L plays a critical role in providing accurate clock source to HX3. The capacitors C1 and C2 (as shown in Figure 3) must be chosen carefully based on the load capacitance value of the crystal.

The load capacitance is calculated using the following equation:

Equation 2. Load Capacitance of a Crystal

$$C_L = \frac{C_1 * C_2}{C_1 + C_2} + C_s$$

Cs is the stray capacitance of XTAL_OUT and XTAL_IN traces on the PCB. Typically, Cs ranges between 2 pF and 5 pF.

For the crystal used in HX3 development kit, C_L = 10 pF. PCB C_s = 5 pF. From Equation 2, C_1 = C_2 = 10 pF.

External Clock Input Requirements

HX3 operates with the external clock input as well. HX3 needs to be configured to use the external clock input and this can be done using Cypress Blaster Plus tool. Blaster Plus is a GUI-based tool to configure HX3. This tool allows the following:

- Download the Cypress-provided firmware from a PC via HX3's US port and store it on an EEPROM connected to HX3's I2C port.
- Read the configuration settings from the EEPROM. These settings are displayed in the Blaster Plus GUI. Modify settings as required.
- Write back the updated settings on to the EEPROM. In addition, an image file can be created for external use.

The Blaster Plus tool, user guide, and the Cypress-provided firmware are available at www.cypress.com/hx3. Table 6 lists the external clock input requirements.

Table 6. External Clock Input Requirements

Parameter	Specification			Units
	Min	Typ	Max	
Amplitude	1.14	1.2	1.26	V
Maximum frequency deviation	-	-	150	ppm
Duty cycle	40	50	60	%
Rise time/Fall time	-	-	3	ns
Jitter (RMS)	-	-	18	ps

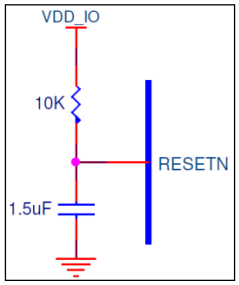
Reset Circuit

HX3 operates with two external power supplies, 3.3 V and 1.2 V. There is no power-sequencing requirement between these two supplies. However, the RESETN pin should be held LOW until both these supplies become stable.

The RESETN pin can be tied to VDD_IO through an external resistor and to ground (GND) through an external capacitor (minimum 5 ms time constant), as shown in Figure 4. This creates a clean reset signal for power-on reset (POR).

HX3 does not support internal brown-out detection. If the system requires this feature, an external reset should be provided on the RESETN pin when supplies are below their valid operating ranges.

Figure 4. Reset Circuit



Port Power Management

The USB specification requires overcurrent protection for all DS ports of the hub. HX3 requires an external power switch to detect over-current conditions and to turn off power to the DS ports.

HX3's 68-pin QFN package supports ganged power switching in which the power to all the four DS ports is controlled with one power enable signal. HX3's 88-pin QFN supports individual or ganged power switching. In individual power switching mode, each DS port power is controlled by separate power enable signals.

In the ganged power-switching mode, the hub turns OFF power to all the DS ports if the total current drawn by the DS ports exceeds a preset current limit set by the external power switch. In the individual power-switching mode, the hub turns OFF power to a DS port if the current drawn by that particular port exceeds the preset current limit set by its power switch.

The preset current limit of a power switch is set based on the port configuration. For example, if a DS port is configured to support BC v1.2, the preset current limit of the power switch should be set to 1.5 A.

In the 88-pin QFN, DSx_PWREN is used to control the external power switches in individual power switching mode. In ganged power-switching mode, DS4_PWREN is the power enable signal to the external power switch. For products supporting ACA-Dock (See Table 1), US_PWREN is used to control the power switch on US port.

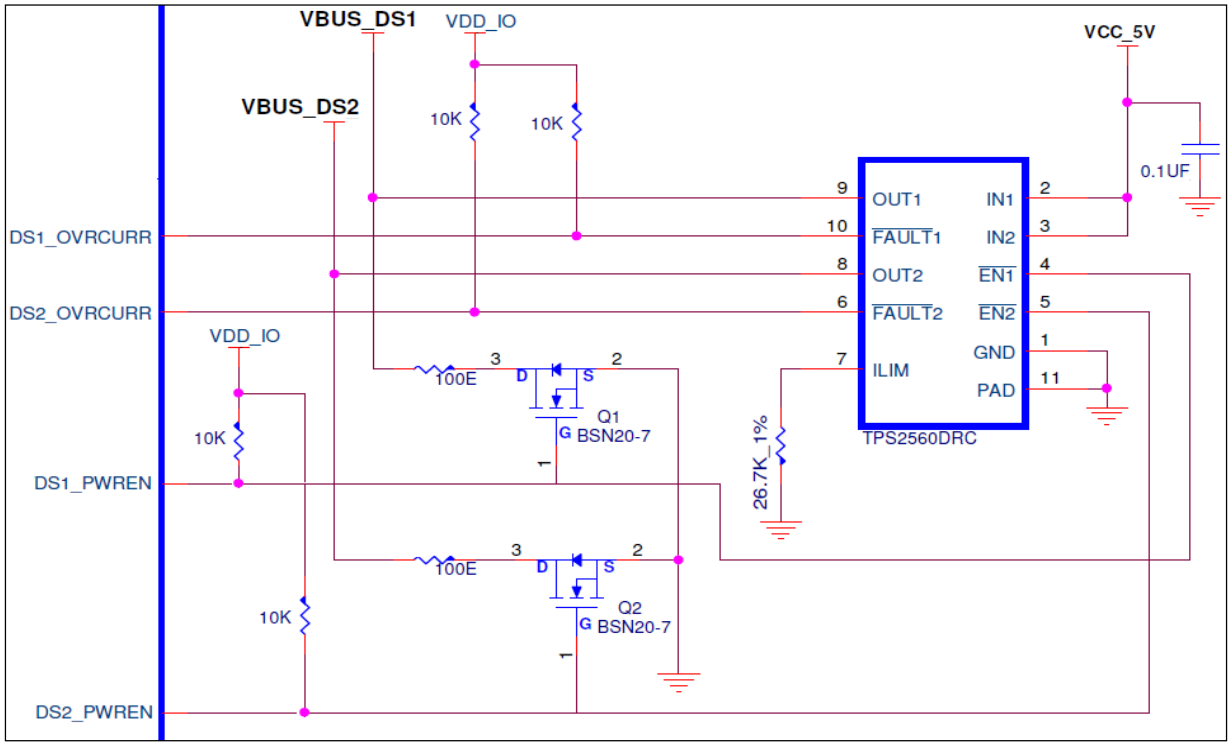
DSx_OVRCURR is the overcurrent indicator input to HX3 from the external power switches in individual power switching mode. DS4_OVRCURR is the overcurrent indicator input to HX3 from the external power switch in ganged power switching mode. For products supporting ACA-Dock (See Table 1), US_OVRCURR is the overcurrent indicator input from the power switch on the US port.

Figure 5 shows how to connect a power switch to HX3 in individual power switching mode.

Power switch schematic considerations:

- The overcurrent inputs (DSx_OVRCURR) may need a pull-up resistor because most switches provide an open-drain output. The recommended value of the resistor is 10 kΩ, as shown in Figure 5.
- A 10-kΩ pull-up or pull-down resistor is required on the power enable (DSx_PWREN) pin based on the external power switch. A 10-kΩ pull-up is used in Figure 5 as the external power switch inputs ($\overline{EN1}$ and $\overline{EN2}$) are active LOW.
- MOSFETs Q1 and Q2 are required for quick discharge of the 150-µF capacitors connected on VBUS of the DS ports (as shown in Figure 5) when the power switch is turned OFF.

Figure 5. Power Switch Connection to HX3

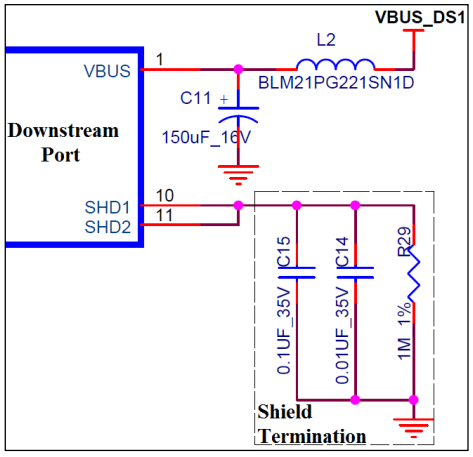


Downstream VBUS and Shield Termination

According to the USB specification, each DS port must have a minimum capacitance of 120 µF on the VBUS pin, to maintain stable voltage under maximum load condition.

The USB connector shield (SHD1 and SHD2) should be terminated to GND with a parallel RC circuit to reduce the EMI as shown in Figure 6.

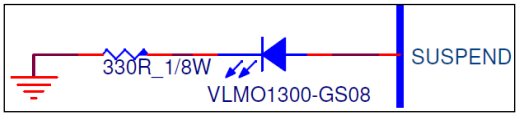
Figure 6. DS VBUS Connection and Shield Termination



Suspend LED

This pin is asserted (HIGH) when both the USB 2.0 and SS hub controllers are in suspend state. It is deasserted (LOW) when either of the hub controllers come out of the suspend state. The suspend status is indicated using an LED as shown in Figure 7. This pin should be connected to GND via a 330-Ω resistor in series to meet the current sourcing capability of this pin (4 mA, maximum).

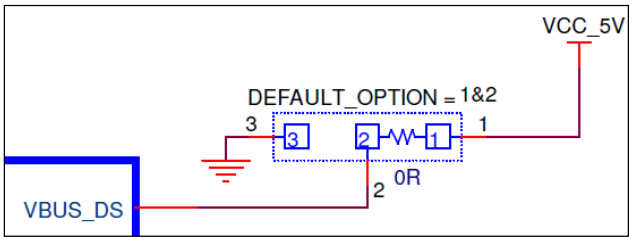
Figure 7. Suspend LED



VBUS_DS and VBUS_US

The VBUS_DS pin is used to power the Apple-charging circuit in HX3. For BC v1.2 compliance testing, this pin should be connected to GND. For normal operation, this pin should be connected to local 5-V supply. Figure 8 shows the VBUS_DS pin connections.

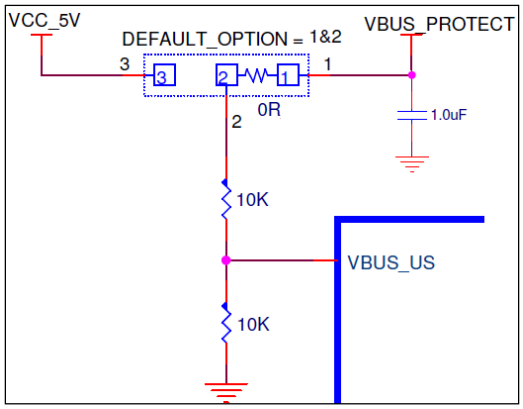
Figure 8. VBUS_DS Pin Connection



The VBUS_US pin should be connected to the VBUS from the US port. This signal is used to detect the US port connection to a Host or a hub.

For products supporting ACA-dock (see Table 1), connect VBUS_US to a local 5-V supply. It is recommended to connect a pair of resistors to the VBUS_US pin to discharge VBUS faster in case of a disconnection event (as shown in Figure 9).

Figure 9. Resistors Connected to VBUS_US Pin



VCC_5V is a 5-V local power supply. VBUS_PROTECT is the VBUS from the US port.

Refer KBA96321 for Supporting ACA-Dock Feature in Smartphone and Tablet Docks with HX3 USB 3.0 Hub Controller.

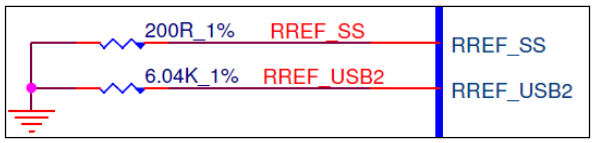
USB Precision Resistors

RREF_SS: This pin should be connected to a precision resistor (200 Ω ±1%) for SS PHY termination impedance calibration (as shown in Figure 10).

RREF_USB2: This pin should be connected to a precision resistor (6.04 kΩ ±1%) to generate a current reference for USB 2.0 PHY (as shown in Figure 10).

These resistors should be placed close to HX3 and the resistors should be connected to GND using the shortest path.

Figure 10. USB Precision Resistors



Configuration Options

HX3 is highly configurable to meet varying hub design requirements. The HX3 default configuration can be modified by one of the following:

1. Pin-strap (applicable to 88-pin QFN only)
2. External I²C slave such as an EEPROM
3. External I²C master

Pin-Strap Configuration

Pin-straps are supported for select product options (see Table 1) to provide reconfigurability without an additional EEPROM. The pin-strap configuration is enabled by pulling the Pin #63 of 88-pin QFN HIGH. Table 7 shows the configuration options supported through pin-straps and the function of the pins after the initial sampling at power-up and reset. Figure 11 and Figure 12 show how the pins need to be connected if pin-strap and LED connection are required or only pin-strap is required.

HX3 samples pin-strap GPIOs at power-up. Floating straps are considered as invalid and the default configuration is used. If PIN_STRAP (Pin #63 of 88-pin QFN) is floating, all strap inputs are considered invalid. A GPIO is considered strapped “1” or “0” when connected with a weak pull-up (10 kΩ) or pull-down (10 kΩ) respectively. After the initial sampling at power-up and reset, the GPIOs are used in their normal functions.

Figure 11. Pin-Strap and LED Schematics

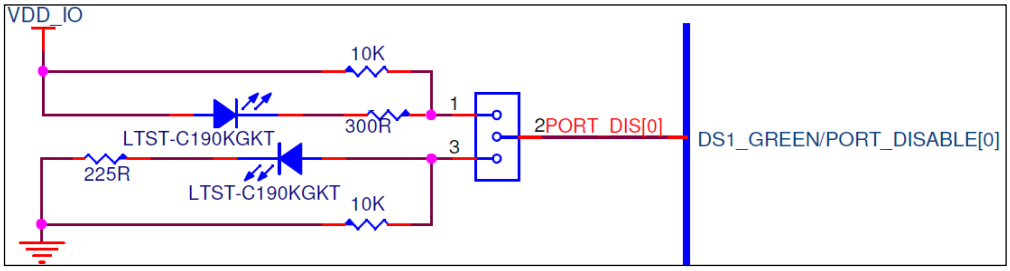


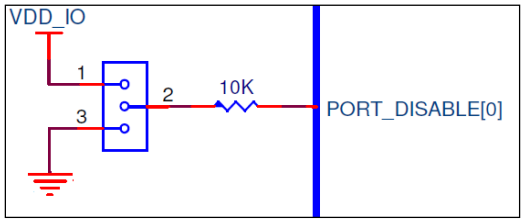
Table 7. Pin-Strap Pins

Number of Pins	Pin-Strap Name	Pin-Strap Purpose	Pin Functionality After Initial Sampling at Power-Up and Reset
1	PIN_STRAP	Enable pin-strap configuration	SS LED indicator for DS3 port
1	ACA_DOCK	Enable ACA-Dock	USB 2.0 AMBER LED indicator for DS1 port
2	PORT_DISABLE[1:0]	Select number of DS ports to be disabled	PORT_DISABLE[1] – SS LED indicator for DS1 port
			PORT_DISABLE[0] – USB 2.0 GREEN LED indicator for DS1 port
2	NON_REMOVABLE[1:0]	Select number of non-removable (hard-wired/embedded) devices	NON_REMOVABLE[1] – USB 2.0 GREEN LED indicator for DS2 port
			NON_REMOVABLE[0] – USB 2.0 AMBER LED indicator for DS2 port
3	VID_SEL[2:0]	Select preprogrammed custom VIDs	VID_SEL[2] – USB 2.0 AMBER LED indicator for DS3 port
			VID_SEL[1] – USB 2.0 GREEN LED indicator for DS3 port
			VID_SEL[0] – USB 2.0 GREEN LED indicator for DS4 port
1	PWR_SW_POL	Select overcurrent and power enable polarity	-
4	DSx_CDP_EN[3:0]	Enable/Disable CDP per DS port	-
1	PWR_EN_SEL	Select individual or ganged power switching mode for DS ports	SS LED indicator for DS2 port
1	I2C_DEV_ID	Select I^2C slave address	USB 2.0 AMBER LED indicator for DS4 port

Refer to the HX3 datasheet for more details on pin-strap configuration.

If pin-strap pin is also multiplexed as a port status LED indicator then that particular pin should be connected to VDD_IO or GND through a 10-kΩ resistor depending on the configuration (as shown in Figure 11). This will ensure that HX3 samples proper logic level (HIGH or LOW) on the pin-strap pins at power-on.

Figure 12. Pin-Strap Schematics

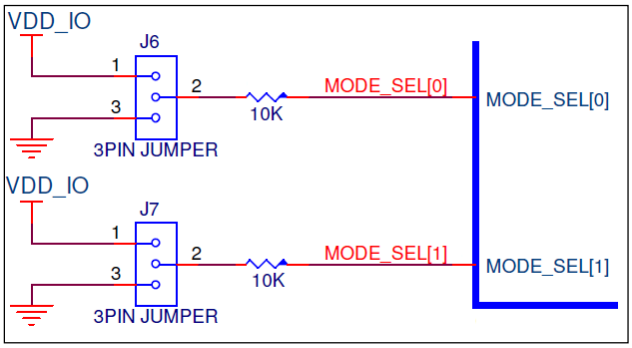


PORT_DISABLE[1:0], NON_REMOVABLE[1:0], DSx_CDP_EN[3:0], and VID_SEL[2:0] are group of pins and if any one pin in a group is left floating, then that specific group is invalid. For example, if PORT_DISABLE[1] pin is left floating then PORT_DISABLE[1:0] group is invalid and the default configuration will apply.

Configuration Using External I²C EEPROM

HX3 can be configured from external I²C slave such as an EEPROM by setting the MODE_SEL[1:0] pins appropriately. The MODE_SEL[1] should be pulled low using 10 kΩ to GND and MODE_SEL[0] should be pulled high using 10 kΩ to VDD_IO (as shown in Figure 13).

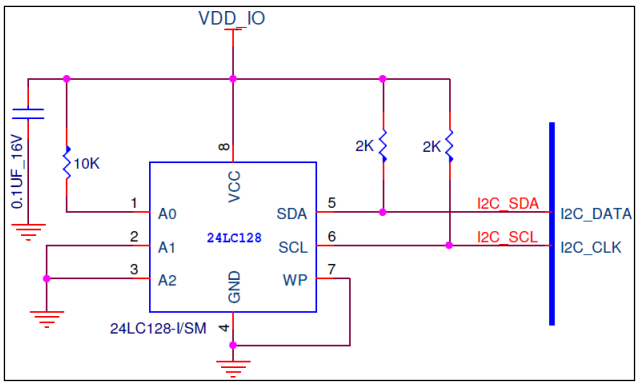
Figure 13. Selecting Configuration Using MODE_SEL



HX3 firmware image size is 10 KB and recommended EEPROM size ranges from 16 KB to 64 KB.

Recommended EEPROMs: 24LC128 and AT24C16A.

Figure 14. EEPROM Connection



For configuring HX3 using EEPROM:

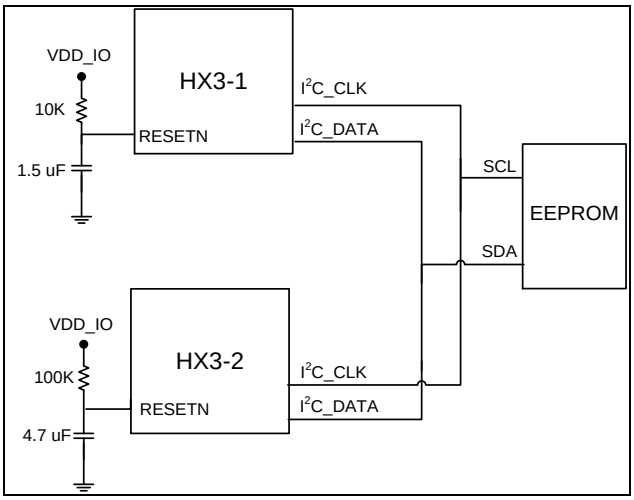
- Address pins A1 and A2 of the EEPROM should be tied LOW and address pin A0 should be pulled HIGH using 10 kΩ to VDD_IO (as shown in Figure 14).
- I2C_DATA and I2C_CLK lines should be pulled HIGH using 2 kΩ to VDD_IO.

Connecting Two HX3s with One EEPROM

In systems requiring two HX3s, one EEPROM can be used to configure both the HX3s sequentially.

To ensure sequential access to the EEPROM, the RESET deassertion of one HX3 should be delayed with respect to the other HX3.

Figure 15. Two HX3s Connected with One EEPROM



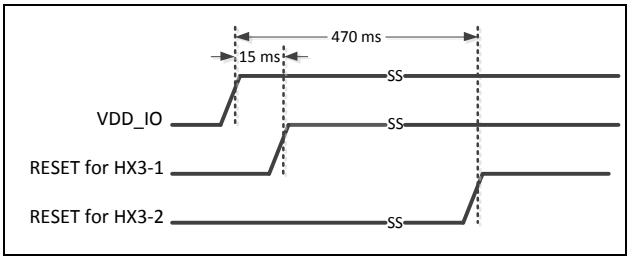
The RESET deassertion can be implemented as follows:

HX3-1: Use R = 10 kΩ and C = 1.5 µF (as shown in Figure 15) to generate a 15-ms RESET pulse.

HX3-2: Use R = 100 kΩ and C = 4.7 µF (as shown in Figure 15) to generate a 470-ms RESET pulse.

The RESET timing diagram is shown in Figure 16.

Figure 16. RESET Timing Diagram



Configuration Using External I²C Master

HX3 can be configured from external I²C master such as an ASSP by setting the MODE_SEL[1:0] pins appropriately. The MODE_SEL[1] should be pulled HIGH using a 10-kΩ resistor to VDD_IO and MODE_SEL[0] should be pulled LOW using a 10-kΩ resistor to GND.

Electrical Design Considerations

Take special care in component selection, location of power supply decoupling capacitors, signal line impedance, and noise when designing a board for USB 3.0. This section explains PCB design guidelines for routing power and USB signal lines.

Refer to Appendix C for general information on PCB layout techniques.

Power System Design

Power supply to the HX3 chip must be clean and stable for reliable hub operation. Improper layouts lead to poor signal quality, especially on the USB signaling, resulting in higher error rates and increased error-correction retries. These symptoms can lead to hub enumeration failure. Consider the following points while designing power system network.

- Placement of bulk and decoupling capacitors
- Power domain routing
- Placement of power and ground planes

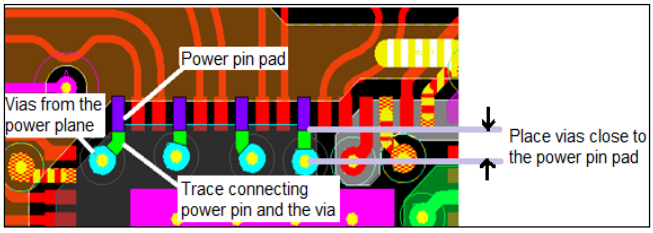
Placement of Bulk and Decoupling Capacitors

Place decoupling capacitors close to the power pins for high-frequency noise filtering. It is recommended to place them on the opposite side of the PCB directly under HX3 to reduce the planar inductance.

Place the bulk capacitor, which acts as a local power supply to the power pin, near the decoupling capacitors. Minimize the trace length between the bulk capacitor and the decoupling capacitors.

Make the power trace width to have the same size as the power pad size. To connect power pins to the power plane, keep vias very close to the power pads. This helps in minimizing the stray inductance and IR drop on the line (as shown in the Figure 17).

Figure 17. Power Delivery Network



Power Domain Routing

HX3 has four power domains: VDDIO, AVDD12, DVDD12, and AVDD33. Use split planes on the power layer for these domains. Use power traces for VDDIO and AVDD33 if the layer does not have enough space for split planes. The following guidelines are recommended for power traces:

- Keep the power traces away from HS data and clock lines.
- Power trace widths should be ≥ 25 mils to reduce inductance.
- Keep power traces short. Use larger vias (at least 30-mil pad, 15-mil hole) on power traces.

Placement of Power and Ground Planes

Place the power plane near to the ground plane for good planar capacitance. Planar capacitance that exists between the planes acts as a distributed decoupling capacitor for high-frequency noise filtering, thereby reducing the electromagnetic radiation.

Routing of USB Data Lines

Pay attention while routing USB signal lines to achieve good signal quality and reduced emission. Pay attention to the following key factors while routing USB signal lines during the PCB design phase.

Controlled Differential Impedance

The differential impedance of the USB signal lines should be 90 Ω ±10%. Otherwise, it affects the signal eye pattern, jitter, and crossover voltage measurements.

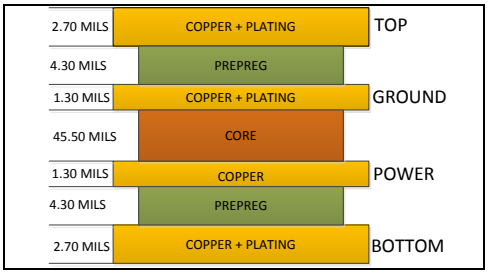
Refer to Appendix D to learn about the underlying theory of differential impedance.

Typical 62-Mil, 4-Layer PCB Example

The recommended stackup for a standard 62-mil (1.6-mm) thick PCB is shown in Figure 18. When this stackup is used with two parallel traces, each with a width (W) of 5.75 mils and a spacing (S) of 12 mils, the calculated differential impedance, Z_{diff}, is 90 Ω.

Figure 18 shows the different layers present in the layout of HX3 development kit.

Figure 18. Stackup Details



Impedance Matching

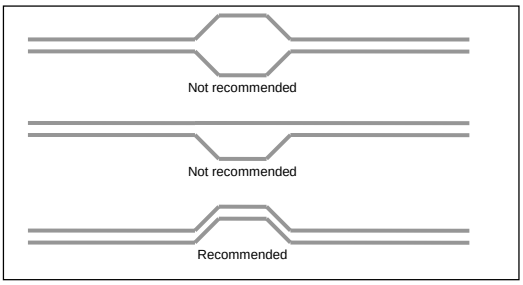
Maintain a constant trace width and spacing in differential pairs to avoid impedance mismatches, as shown in Figure 19 and Figure 20.

Figure 19. Differential Pairs Placements



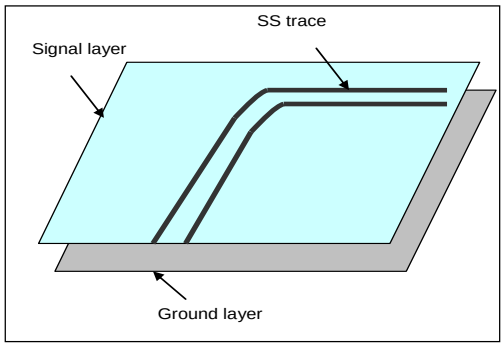
Where ‘g’ is the minimum gap between the trace and other planes (8 mils).

Figure 20. Differential Pairs Impedance Matching Techniques



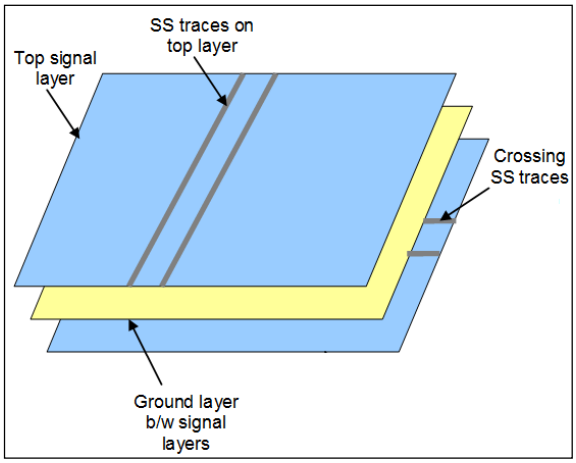
All SS signal lines should be routed over an adjacent ground plane layer to provide a good return current path. Splitting the ground plane underneath the SS signals introduces impedance mismatch, increasing the loop inductance and electrical emissions. Figure 21 shows a solid ground plane under the SS signal.

Figure 21. Solid Ground Plane under the SS Signal



Whenever two pairs of USB traces cross each other in different layers, a ground layer should run all the way between the two USB signal layers, as Figure 22 shows.

Figure 22. Ground Insertion



Trace Length

The USB signal trace length should be as short as possible. Long traces increase insertion loss and emission, and introduces Inter-Symbol Interference (ISI) to the far-end receiver.

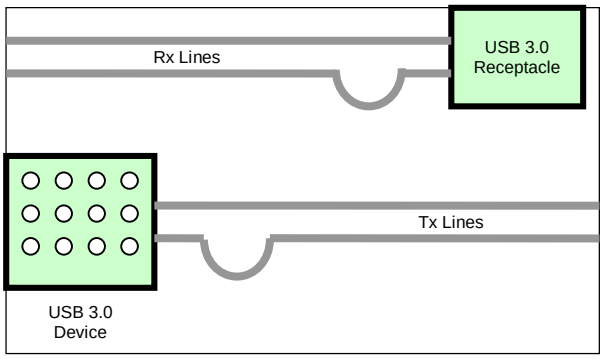
Note HX3 SS lines are characterized for a trace length of up to 11 inches. It is recommended that the length of the SS PCB traces be kept under 11 inches.

During PCB layout design, prioritize routing of USB signal lines. Ensure that the following recommendations are met:

- Match the differential SS pair trace lengths within 0.12 mm (5 mils).
- Match the Hi-Speed (D+ and D–) signal trace lengths within 1.25 mm (50 mils).
- Adjust the Hi-Speed signal trace lengths near the USB receptacle, if necessary.
- Make adjustments for SS Rx signal trace lengths near the USB receptacle, and adjustments for SS Tx signal trace lengths near the device, if necessary.

Figure 23 shows an example of length matching for the SS signal.

Figure 23. SS Signal Length Matching



Port-to-Port Isolation

Port-to-port isolation is required to minimize the effect of the interference fringes of SS Tx lines of one port over the Rx lines of another port.

Fill the space between two differential pairs with ground. Maintain a minimum of $2W$ space between the ground and the differential pairs, where W = trace width.

Provide via stitched guard traces along the SS and HS traces to ensure proper isolation between ports.

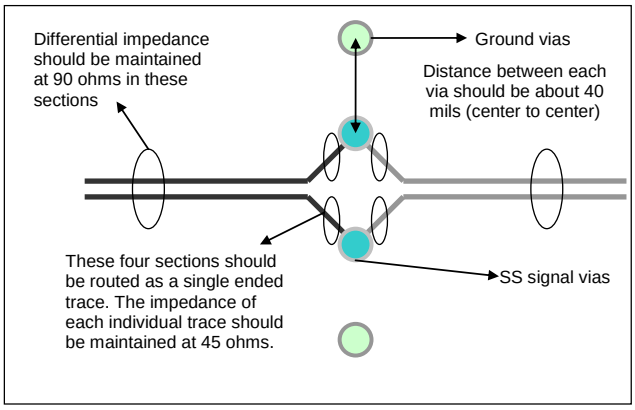
Figure 26 shows the routing of ground traces on both sides of the USB data line pairs with stitching vias.

Signal Via Routing

It is recommended that the SS signals be routed in a single layer. Vias introduce discontinuities in the signal line and affect the SS signal quality.

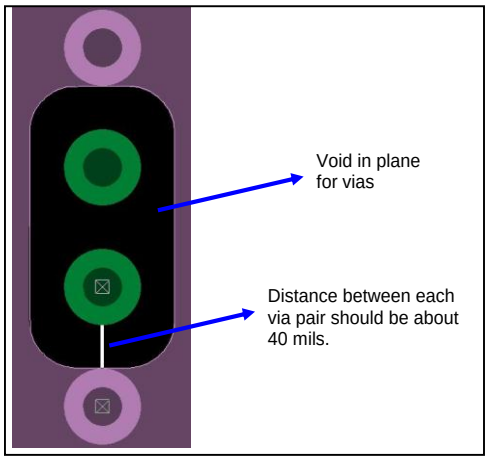
If you need to route the SS signal to another layer, maintain continuous grounding to ensure uniform impedance throughout. To do so, place ground vias next to signal vias as shown in Figure 24. The distance between the signal and ground vias should be at least 40 mils.

Figure 24. Ground Vias



Voids for vias on SS signal traces should be common for the differential pair. Common void, as shown in Figure 25, helps better in matching the impedance compared to separate vias.

Figure 25. Void Vias Placement for SS Traces



Other Recommendations

Place the capacitor used in the RC reset circuitry as close as possible to the reset pin of HX3.

Place the crystal less than 1 cm from the HX3. Also, make sure that there is a solid ground plane under the crystal trace.

When using a standard-B receptacle (through-hole receptacle), it is highly recommended that USB signal lines are connected to the receptacle pins on the opposite layer as the receptacle, as shown in Figure 27 and Figure 28. For example, if the standard-B receptacle is placed on the top layer, the signal lines should be connected to the receptacle pins on the bottom layer. This is to avoid pin stubs (antennas).

Figure 26. Port-to-Port Isolation

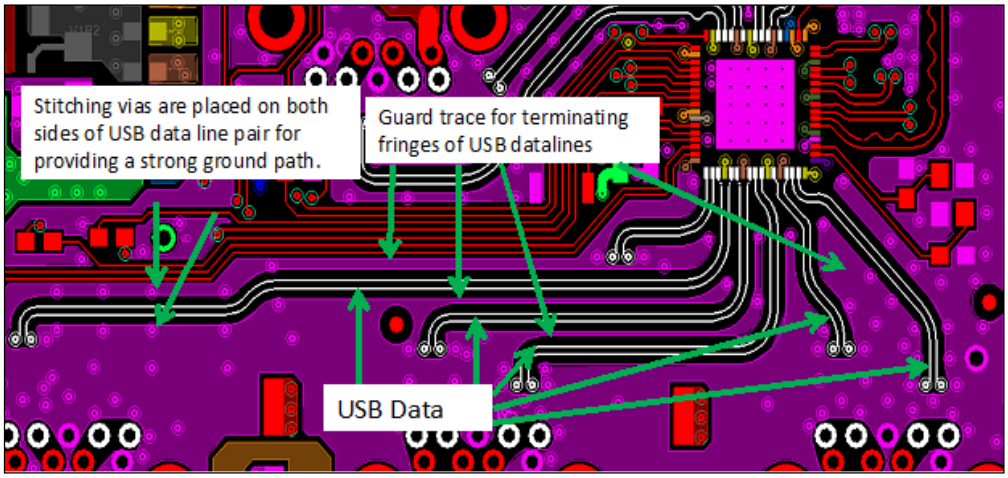


Figure 27. Standard-B Receptacle Placement

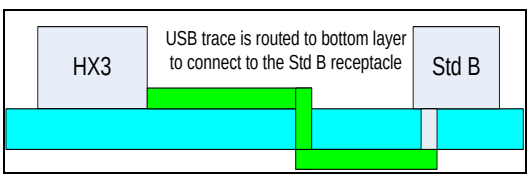


Figure 28. Standard-B Receptacle Layout

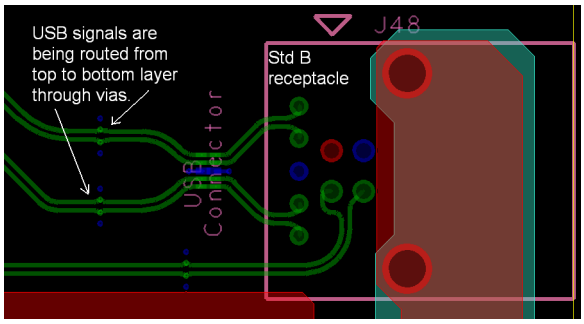
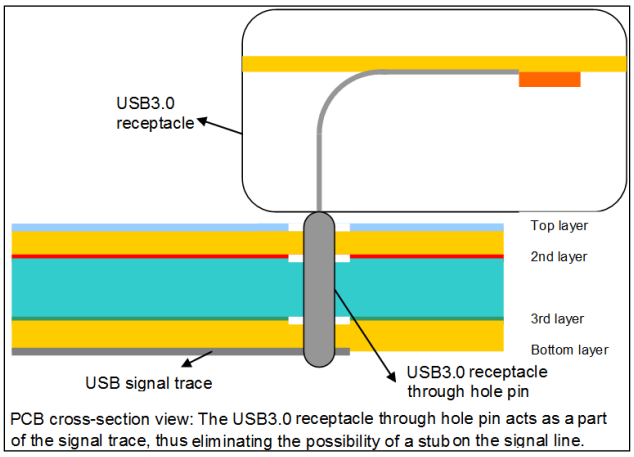


Figure 29 illustrates the recommended layout. To avoid vias, you can place the device on the opposite layer of the standard-B receptacle. In this case, you can route the USB traces entirely on the same layer.

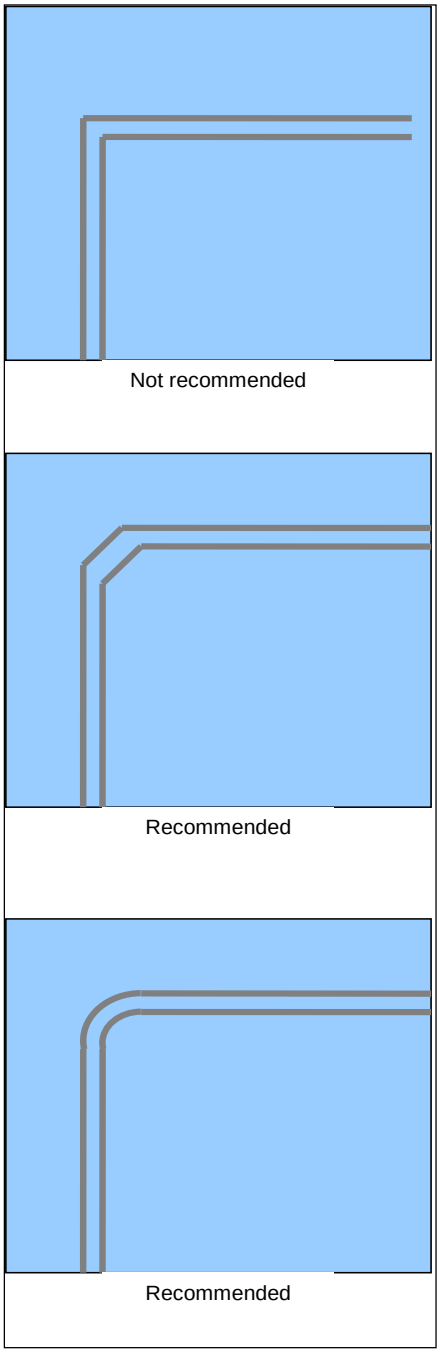
Figure 29. USB Signals Connected on the Opposite Side of the Standard-B USB Receptacle to Avoid Stub on Line



The polarity of the SS differential pairs can be swapped. Polarity detection is done automatically by the SS PHY during link training, as defined in the USB 3.0 Specification, section 6.4.2. The polarity inversion mechanism can be utilized to ensure that USB traces do not cross each other.

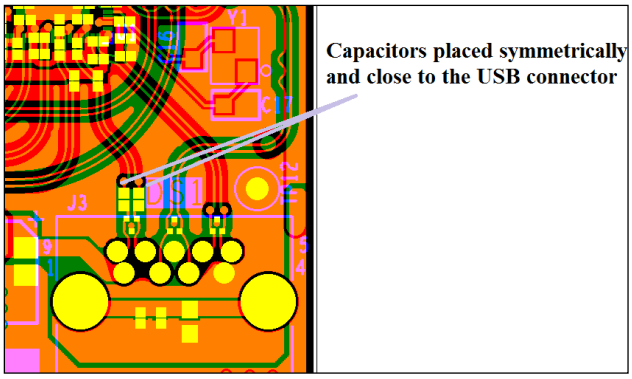
On the USB signal lines, use as few bends as possible. Do not use a 90-degree bend. Use 45-degree or rounded (curved) bends if necessary, as illustrated in Figure 30.

Figure 30. USB Signal Bends



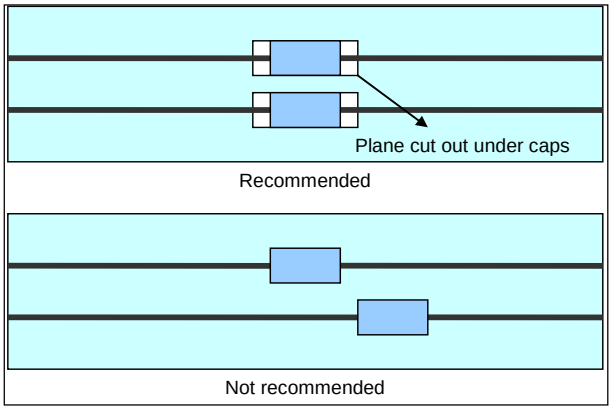
SS traces require additional AC coupling capacitors (0.1 µF) on the TX lines (on both US port and DS port as shown in Figure 31). For DS ports, place these capacitors symmetrically and near to the connector. For US ports, place them near the device.

Figure 31. SS TX Line AC coupling Capacitors



Two immediate planes underneath the AC coupling capacitors should have a cutout in the shape of these capacitors to avoid extra capacitance on the lines created by the capacitor pads. Figure 32 shows the proper layout of the decoupling caps.

Figure 32. SS TX AC Coupling Capacitors Layout



Schematics and Layout Review Checklist

Table 8 is a checklist for all the important guidelines. Provide an answer to each checklist item to find out the extent to which your hardware design meets these guidelines.

Table 8. Schematics and Layout Review Checklist

Sl. No	Schematic checklist	Answer (Yes/No/NA)
1	Are the decoupling capacitors and bulk capacitors connected as per Figure 1 and Figure 2?	
2	Does the crystal meet the specification in this application note?	
3	Are all DS ports provided with 150-µF bulk capacitors?	
4	Do the Power-on-Reset RC components meet the minimum reset time (5 ms)?	
5	Do the USB precision resistors have 1% tolerance?	
6	Are the I^2C lines provided with pull-up resistors to the 3.3-V domain?	
7	Do the LEDs connected to the pin-strap pins have a 10-kΩ parallel resistor?	
8	Is it ensured that the DS port power switch has a MOSFET connected to the OUTPUT pin or selected a power switch with fast discharge?	
9	Is the VBUS_US pin provided with a 10-kΩ voltage divider network?	
10	Is the US port provided with 1-µF bulk capacitor?	
11	Are all port shields terminated properly?	
12	Are the ferrite beads connected as shown in Figure 1 and Figure 2?	
13	Are MODE_SEL[1] and MODE_SEL[0] not pulled LOW when the pin-strap configuration is used with HX3? (For 88-pin QFN only).	
14	Are values of the resistors connected in series to the LEDs decided based on the HX3's I/O current source/sink capability (4 mA)?	
	Layout Checklist	
1	Is the crystal placed close to the chip (less than 1 cm)?	
2	Are the decoupling capacitors and bulk capacitors placed close to the HX3 power pins?	
3	Are the vias placed close to the HX3 power pins?	
4	Are the power traces routed away from the high-speed data lines and the clock lines?	
5	Is the capacitor in the RC reset circuitry placed close to the reset pin of HX3?	
6	Is the 150-µF capacitor placed close to the DS port connector?	
7	Are the USB SS and HS signal lines matched in length?	
8	Are the USB data lines provided with solid ground plane underneath?	
9	Are the SS traces provided with the guard traces along the USB data trace with stitching vias?	
10	Are the SS traces provided with the AC decoupling capacitors (0.1 µF) on the TX lines?	
11	Are the USB traces kept as short as possible?	
12	Is it ensured that there are no stubs on all the USB traces?	
13	Is it ensured that there are no vias on the SS traces?	
14	Do the USB traces have few bends and no 90-degree bends?	

Summary

USB SuperSpeed operation demands careful hardware design to preserve HX3 signal integrity. By following the guidelines in this application note, your HX3-based design has a good chance of first-pass success.

Acronyms

Table 9. Acronyms Used in this Document

Acronym	Description
ACA	Accessory Charger Adaptor
ASSP	Application Specific Standard Product
BC	Battery Charging
CDP	Charging Downstream Port
DCP	Dedicated Charging Port
DS	DownStream
EEPROM	Electrically Erasable Programmable Read-Only Memory
FS	Full-Speed
GND	Ground
HS	Hi-Speed
LED	Light-Emitting Diode
LS	Low-Speed
PCB	Printed Circuit Board
QFN	Quad Flat No-Lead
SDP	Standard Downstream Port
SS	SuperSpeed
SWD	Serial Wire Debug
US	UpStream
USB	Universal Serial Bus
VID	Vendor ID

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Appendix A: Power Consumption

Table 10 provides the power consumption estimates for HX3 under different conditions. Table 11 summarizes the power consumption for various combinations of devices connected to DS ports.

For example, to calculate the HX3 power consumption for three SS devices connected to DS ports (and no device connected to one DS port), and a US port connected to a USB 3.0 Host:

Power consumption = [a] + 2×[g] = 492.5 + 2×76 = 644.5 mW

[a] is the active power consumption for the US port connected to a USB 3.0 Host and the SS device connected to the DS port.

[g] is the incremental power consumption for an additional SS device connected to the DS port.

Table 10. Power Consumption Estimates for Various Usage Scenarios

Device Condition	Number and Speed of DS Ports Connected	Typical Consumption			Comments
		Supply Current (mA)		Power (mW)	
		1.2 V	3.3 V		
Host not attached	-	18.0	6.0	41.4	-
Suspend with Host attached [2]	No devices connected	42.0	12.0	90.0	-
Active power with USB 3.0 Host [3]	1 SS	204.1	75.0	492.5	[a]
	1 HS	51.2	45.2	210.7	[b]
	1 FS	51.2	34.0	173.7	[c]
	1 SS + 1 HS	218	103.4	602.9	[d]
Active power with USB 2.0 Host [3, 4]	1 HS	51.2	45.2	210.7	[e]
	1 FS	51.2	34.0	173.7	[f]
Incremental active power for additional DS port	1 SS	39.4	8.7	76.0	[g]
	1 HS	7.0	19.8	73.7	[h]
	1 FS	7.0	14.2	55.2	[i]
Active power saving per disabled DS port [5]	-	10.6	9.6	44.4	[j]

Table 11. Power Consumption under various Configurations

Device Condition	Number of DS Devices Connected with Data Transfer	Typical Consumption			Comments
		Supply Current (mA)		Power (mW)	
		1.2 V	3.3 V		
USB 3.0 4-port hub (USB 3.0 Host)	4 SS devices	322	101	720	[a] + 3×[g]
	3 SS + 1 HS devices	297	121	755	[d] + 2× [g]
	3 SS devices	283	92	644	[a] + 2× [g]
USB 3.0 4-port hub (USB 3.0 Host) with one port disabled	3 SS devices	272	83	600	[a] + 2× [g] –[j]
	2 SS + 1 HS devices	247	103	634	[d] + [g] – [j]
Shared Link with 8 DS ports	4 SS + 4 HS devices	357	189	1052	[d] + 3× ([g] + [h])
USB 3.0 4-port hub (USB 2.0 Host)	4 HS devices	72	105	432	[e] + 3× [h]
	3 HS + 1 FS devices	72	99	413	[e] + 2× [h] + [i]

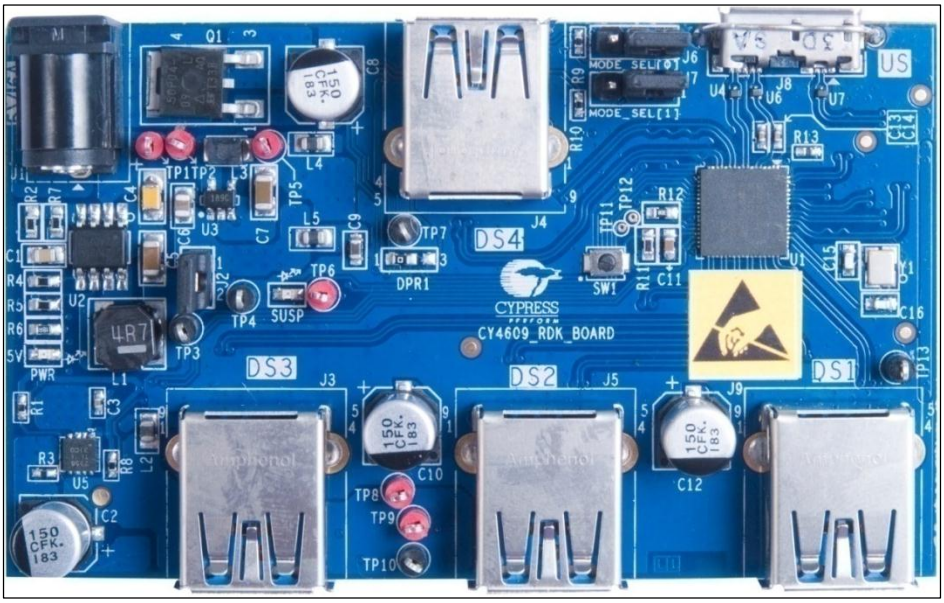
Notes

2. US port in low-power state (SS in U3 and USB 2.0 in L2).
3. All four DS ports are enabled.
4. US SS disabled using configuration options. Refer HX3 datasheet for configuration options.
5. Power saving applicable only with a USB 3.0 Host. DS ports can be disabled through configuration options. Refer HX3 datasheet for configuration options.

Appendix B: HX3 Development Kits (DVKs) and BOM

Cypress's HX3 DVK provides the hardware that you need to get started. CY4609 is the DVK for 68-pin QFN and CY4603 is the DVK for 88-pin QFN. CY4613 is also for 88-pin QFN, which helps in testing the Shared Link feature. The contents of these DVKs help in designing your final hub product using HX3. Figure 33 shows the picture of CY4609, Figure 34 shows the picture of CY4603 and Figure 35 shows the picture of CY4613. HX3 DVK schematics can be downloaded from the Cypress webpage.

Figure 33. HX3 68-Pin QFN DVK (CY4609)



BOM Reduction to CY4609

CY4609 is designed to have several configuration and debugging options. In your final product design, these options are not required. Also, HX3 design has been tested with the optimized decoupling capacitor values; thus in your final product, there is a scope for reducing the BOM. Table 12 shows you the list of components that can be removed or changed.

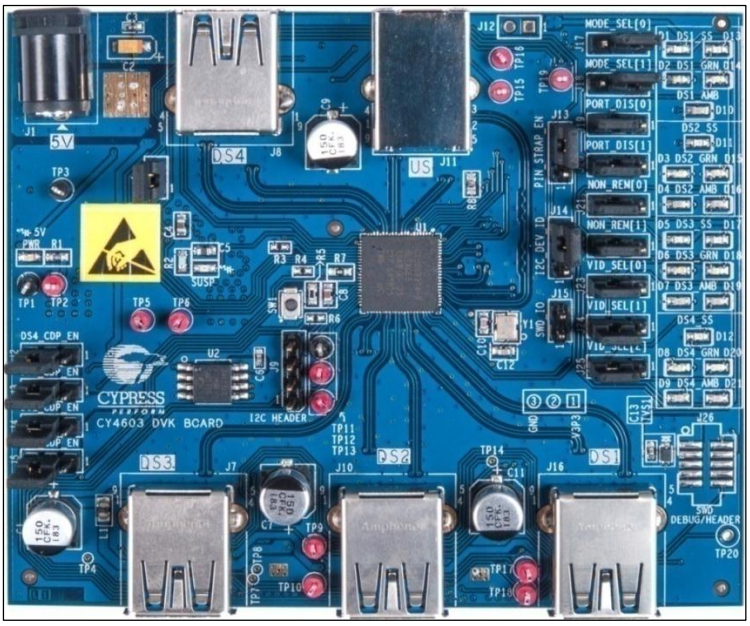
Table 12. BOM Reduction to CY4609

Recommended Components to be Removed	Component Value	Quantity	Schematic Reference	Reason
Decoupling capacitors	0.001 µF	10	C32, C39, C42, C43, C44, C46, C47, C50, C57, C63	One decoupling capacitor (0.01 µF) per pin is enough to filter out the high frequency noise on 1.2-V SS Rx and Tx domains
	0.01 µF	10	C27, C30, C34, C35, C36, C37, C38, C58, C60, C66	One decoupling capacitor (0.1 µF) per pin is enough to filter out the noise
	0.1 µF	2	C53, C61	The 22-µF bulk capacitor is enough for 1.2-V SS Rx and Tx domains
	1 µF	8	C21, C54, C65, C68	The 1-µF capacitor is not needed because the 22-µF bulk capacitor serves the purpose.
			C70, C72	The 22-µF bulk capacitor is enough for 1.2-V SS Rx and Tx domains
			C71, C77	On the DVK, an overvoltage protection IC is used to provide additional protection. This is an optional requirement and should be added only when needed. Input and output capacitors for overvoltage protection IC. These are needed only if overvoltage protection IC (U12) is used.

Recommended Components to be Removed	Component Value	Quantity	Schematic Reference	Reason
Resistors	0 Ω	1	R28	MOSFET(Q2) gate pin does not require a resistor and gate can be shorted to $\overline{EN}$ pin of power switch directly.
	1 MΩ	1	R19	This is needed only if an overvoltage protection IC (U12, $\overline{FLAG}$ pin) is used.
Reset switch	-	1	SW1	No manual reset is required for normal hub operation
MOSFET for reverse polarity	-	1	Q1 (SUD50P04-09L-E3)	On the kit, this is added to provide additional protection for reverse polarity power connection. This is only required if there is any chance of connecting negative supply voltage to the hub design.
ESD Diodes	-	15	U4, U6, U7, U8, U9, U10, U11, U13, U14, U15, U16, U17, U18, U20, U21	On the kit, ESD diodes are added to provide additional protection. This is optional; HX3 has a built-in ESD protection of 2.2 kV.
Test Points	-	11	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP13	Test points are only for debugging; they are not required in the final product design.
Headers	-	3	J6, J7	Headers are provided on the DVK to select the HX3 configuration options. These are not required in the final product design.
			J2	This header is provided for debugging and not needed for the final product design.
Overvoltage protection IC	-	1	U12 (NCP361SNT1G)	On the DVK, an overvoltage protection IC is used to provide additional protection. This is an optional requirement; it should be added only when needed.
Jumpers	-	3	881545-2 Mini Jumpers	Headers are provided on the DVK to select the HX3 configuration options. These are not required in the final hub design.
Ferrite Bead	-	5	L2, L6, L7, L8, L9	One ferrite bead is added on the VBUS line of US. Four are added on the VBUS line of the four DS ports. This depends on the system.
Total		72		
Recommended Components to be Replaced	**Component Value**	**Quantity**	**Schematic Reference**	**Reason**
Bulk Capacitors	22 µF to be replaced with 10 µF	3	C9, C82, C85	HX3 DVK has been tested with the optimized bulk capacitor values of 10 µF.
3.3 V Regulator	AOZ1021AI can be replaced with NCP3170ADR2G or AOZ1015AI	1	U2	Low-cost regulator

The components colored in green will be removed in the next revision of the DVK. Refer to http://www.cypress.com/hx3 for schematics with the reduced BOM.

Figure 34. HX3 88-Pin QFN DVK (CY4603)



BOM Reduction to CY4603

CY4603 is designed to have various configuration, debugging options and LED indicators. As listed in Table 13, there is a scope for reducing the BOM in your final product.

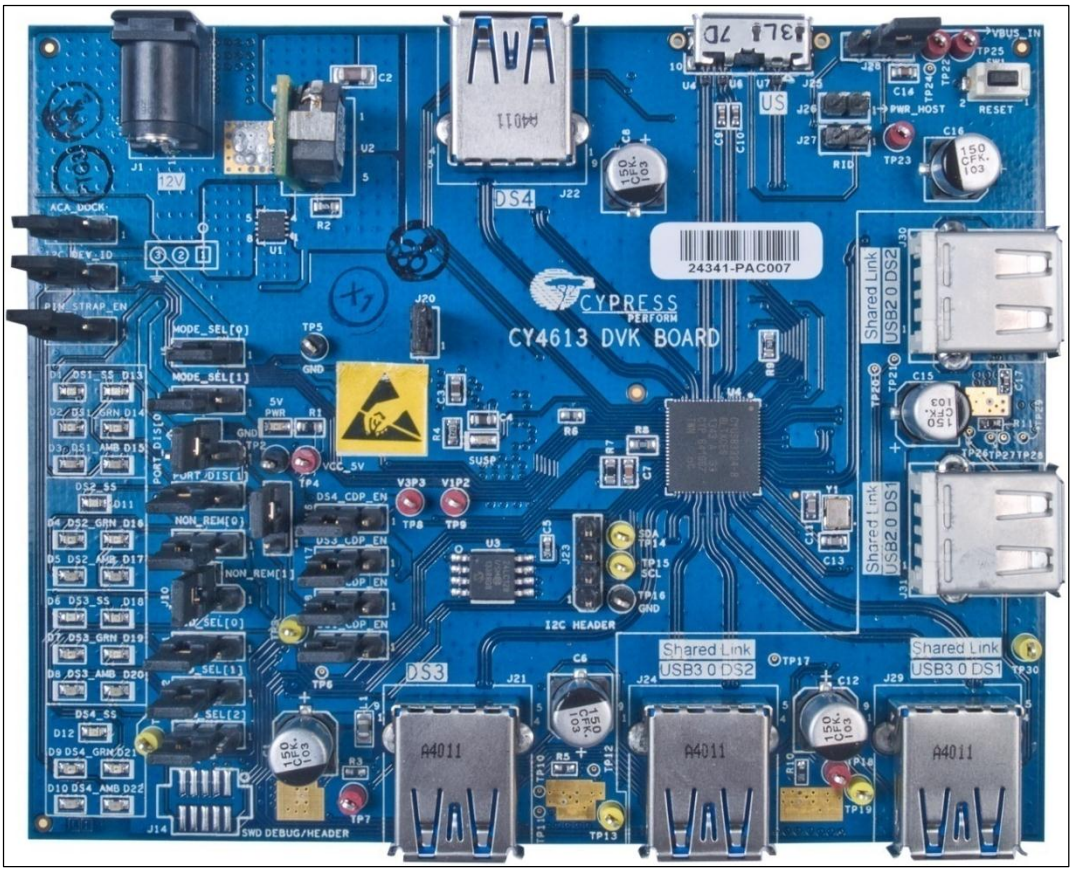
Table 13. BOM Reduction to CY4603

Recommended Components to be Removed	Component Value	Quantity	Schematic Reference	Reason
Decoupling capacitors	0.001 µF	10	C37, C40, C43, C44, C45, C50, C55, C56, C61, C62	One decoupling capacitor (0.01 µF) per pin is enough to filter out the high-frequency noise on 1.2-V SS Rx and Tx domains.
	0.01 µF	10	C25, C28, C29, C36, C38, C39, C42, C51, C66, C71	One decoupling capacitor (0.1 µF) per pin is enough to filter out the noise.
	0.1 µF	3	C58, C73	One 22-µF bulk capacitor is enough for 1.2-V SS Rx and Tx domains
			C13	Decoupling capacitor for the SWD interface. This SWD interface is not required in final product design.
	1 µF	8	C34, C68, C72, C75, C76, C77	The 1-µF capacitor is not needed because the 22-µF bulk capacitor serves the purpose
			C18, C19	Input and output capacitors for the overvoltage protection IC. These are required only if the overvoltage protection IC (U12) is used.
Resistors	10 kΩ	26	R15, R37, R41, R46, R50, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86	These resistors can be removed only if pin-strap configuration is not used. If you are using an external EEPROM firmware for configuration, then the pin-strap option has no effect.
	226 Ω	8	R9, R10, R12, R13, R17, R19, R20, R21	These resistors are used to limit the LED current and can be removed if port indicators are not required
	270 Ω	4	R11, R14, R16, R18	
	300 Ω	7	R22, R24, R25, R26, R27, R28, R34	
	0 Ω	4	R32, R38, R47, R56	MOSFET(Q2) gate pin does not require a resistor and gate can be shorted to the $\overline{EN}$ pin of power switch directly.

Recommended Components to be Removed	Component Value	Quantity	Schematic Reference	Reason
	1 MΩ	1	R36	This is required only if overvoltage protection IC (U12, $\overline{FLAG}$ pin) is used
Reset switch	-	1	SW1	No manual reset is required for normal hub operation.
MOSFET for reverse polarity	-	1	Q5 (SUD50P04-09L-E3)	On the kit, this is added to provide additional protection for reverse polarity power connection. This is only required if there is any chance of connecting negative supply voltage to the hub design.
ESD Diodes	-	15	U3, U4, U5, U8, U9, U10, U11, U12, U13, U15, U16, U17, U18, U19, U20	On the kit, ESD diodes are added to provide additional protection. This is optional; HX3 has a built-in ESD protection of 2.2 kV.
Test Points	-	16	TP1, TP2, TP3, TP5, TP6, TP9, TP10, TP11, TP12, TP13, TP15, TP16, T17, T18, T19, T20	Test points are only for debugging and they are not required in the final product design.
Headers	-	18	J2, J3, J4, J5, J6, J9, J13, J14, J15, J17, J18, J19, J20, J21, J22, J23, J24, J25	This header is provided for debugging and not required for the final product design.
LED	-	21	D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21	LEDs can be removed only if port indicators are not required
Overvoltage protection IC	-	1	U6 (NCP361SNT1G)	On the DVK, an overvoltage protection IC is used to provide additional protection. This is optional; it should be added only when required.
Diode	-	1	TVS1	
Jumpers	-	20	881545-2 Mini Jumpers	Headers are provided on the DVK to configure HX3. These are not required in the final hub design.
Ferrite Bead	-	5	L1, L2, L3, L4, L5	One ferrite bead is added on the VBUS line of US. Four of these are added on the VBUS line of the four DS ports. This depends on the system.
Total		180		
Recommended Components to be Replaced	**Component Value**	**Quantity**	**Schematic Reference**	**Reason**
Regulator	AOZ1021AI can be replaced with NCP3170ADR2G or AOZ1015AI	1	U22	Low-cost regulator

The components colored in green will be removed in the next revision of the DVK. Refer to http://www.cypress.com/hx3 for schematics with the reduced BOM.

Figure 35. HX3 88-Pin QFN DVK with Shared Link Feature Support (CY4613)



BOM Reduction to CY4613

CY4613 is designed to have various configuration, debugging options and LED indicators. As listed in Table 14, there is a scope for reducing the BOM in your final product.

Table 14. BOM Reduction to CY4613

Recommended Components to be Removed	Component Value	Quantity	Schematic Reference	Reason
Decoupling capacitors	0.001 µF	10	C51, C60, C56, C66, C67	One decoupling capacitor (0.01 µF) per pin is enough to filter out the high-frequency noise on 1.2-V SS Rx and Tx domains.
	0.01 µF	10	C31, C34, C35, C41, C43, C45, C48, C57, C71, C76	One decoupling capacitor (0.1 µF) per pin is enough to filter out the noise.
	0.1 µF	3	C80,C82	The 22-µF bulk capacitor is enough for 1.2-V SS Rx and Tx domains
			C106	Decoupling capacitor for SWD interface. This SWD interface is not needed in final product design.
	1 µF	8	C39, C40, C73, C77, C81, C82	The 1-µF capacitor is not required because the 22-µF bulk capacitor serves the purpose.
			C14,C26	Input and output capacitors for Overvoltage protection IC.
Resistors	10 kΩ	28	R6, R43, R44, R45, R46, R50, R54, R55, R56, R63, R64, R65, R71, R73, R75, R78, R88, R89, R90, R91, R92, R93, R94, R95, R96, R100, R101, R102	These resistors can be removed only if pin-strap configuration is not used. If you are using external EEPROM firmware for configuration, then the pin-strap option has no effect.

Recommended Components to be Removed	Component Value	Quantity	Schematic Reference	Reason
	226 Ω	8	R79, R80, R82, R84, R85, R87, R98, R99	These resistors are used to limit the LED current and can be removed if port indicators are not needed
	270 Ω	5	R4, R77, R81, R83, R86	
	300 Ω	8	R59, R60, R61, R67, R70, R72, R74, R76	
	0 Ω	6	R13, R21, R22, R26, R34, R62	MOSFETs (Q1, Q2, Q3, Q4) gate pin does not require a resistor and the gate can be shorted to the $\overline{EN}$ pin of the power switch directly.
	1 MΩ	1	R20	This is needed only if overvoltage protection IC (U12, $\overline{FLAG}$ pin) is used
Reset switch	-	1	SW1	No manual reset is required for normal hub operation
MOSFET for reverse polarity	-	1	Q7	On the kit, this is added to provide additional protection for reverse polarity power connection. This is only required if there is any chance of connecting negative supply voltage to the hub design
ESD Diodes	-	15	U4, U6, U7, U9, U10, U11, U12, U15, U16, U18, U19, U20, U21, U22, U23	On the kit, ESD diodes are added to provide additional protection. This is optional; HX3 has a built-in ESD protection of 2.2 kV.
Test Points	-	16	TP1, TP2, TP3, TP4, TP5, TP7, TP8, TP9, TP13, TP14, TP15, TP16, TP18, TP19, TP22, TP23, TP25, TP30	Test points are only for debugging and they are not required in the final product design.
Headers	-	18	J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J15, J16, J17, J18, J19, J20, J23, J26, J27, J28	This header is provided for debugging and not required for the final product design.
LED [7]	-	21	D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22	LEDs can be removed only if port indicators are not required.
Overvoltage protection IC	-	1	U13	On the DVK, Overvoltage protection IC is used to provide additional protection. This is an optional requirement; it should be added only when required.
Diode	-	1	TVS1	
Jumpers	-	20		Headers are provided on the DVK to configure HX3. These are not required in the final hub design.
Ferrite Bead	-	7	L1, L2, L3, L4, L5, L6, L7	One Ferrite bead is added on the VBUS line of US. Two of these are added on the VBUS line of two USB 3.0 DS ports. Four of these are added on Shared Link (2 USB 3.0 + 2 USB 2.0) DS ports. This depends on the system.
Total		195		
Recommended Components to be Replaced	**Component Value**	**Quantity**	**Schematic Reference**	**Reason**
Regulator	AOZ1021AI can be replaced with NCP3170ADR2G or AOZ1015AI	1	U25	Low-cost regulator

The components colored in green will be removed in the next revision of the DVK. Refer www.cypress.com/hx3 for schematics with the reduced BOM.

Appendix C: PCB Layout Tips

There are many classic techniques for designing PCBs for low noise and EMC. Some of these techniques include the following:

- **Multiple layers:** Although they are more expensive, it is best to use a multilayer PCB with separate layers dedicated to the V_{SS} and V_{DD} supplies. This provides good decoupling and shielding effects. Separate fills on these layers should be provided for V_{SSA}, V_{SSD}, V_{DDA}, and V_{DDD}.

  It is recommended to use at least a four-layer PCB for HX3.

- **Component position:** You should separate the different circuits on the PCB according to their EMI contribution. This will help reduce cross-coupling on the PCB. For example, separate noisy high-current circuits, low-voltage circuits, and digital components.

- **Ground and power supply:** There should be a single point for gathering all ground returns. Avoid ground loops, or minimize their surface area. All component-free surfaces of the PCB should be filled with additional grounding.

  The power supply should be close to the ground line to minimize the area of the supply loop. The supply loop can act as an antenna and can be a major emitter or receiver of EMI.

- **Decoupling:** The standard bulk decoupler for external power is a 100-µF capacitor. Supplementary 0.1-µF capacitors should be placed as close as possible to the V_{SS} and V_{DD} pins of the device to reduce high-frequency power supply ripple.

  Generally, decouple all sensitive or noisy signals to improve EMC performance. Decoupling can be both capacitive and inductive.

- **Signal routing:** When designing an application, analyze the following areas to improve EMC performance:
  - Noisy signals, for example, signals with fast edge times
  - Sensitive and high-impedance signals
  - Signals that capture events, such as interrupts and strobe signals

To increase the EMC performance, keep the trace lengths as short as possible and isolate the traces with V_{SS} traces. To avoid crosstalk, do not route them near to or parallel to other noisy and sensitive traces. For more information, consult these references:

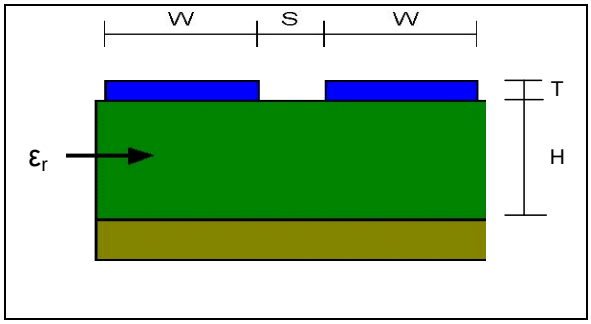
- *The Circuit Designer's Companion*, Second Edition (EDN Series for Design Engineers), by Tim Williams
- *PCB Design for Real-World EMI Control* (The Springer International Series in Engineering and Computer Science), by Bruce R. Archambeault and James Drewniak
- *Printed Circuits Handbook* (McGraw Hill Handbooks), by Clyde Coombs
- *EMC and the Printed Circuit Board: Design, Theory, and Layout Made Simple*, by Mark I. Montrose
- *Signal Integrity Issues and Printed Circuit Board D*
- *esign*, by Douglas Brooks

Appendix D: Differential Impedance of USB Traces

Microstrips are the copper traces on the outer layers of a PCB. A microstrip has an impedance, Z_0, which is determined by its width (W), height (T), distance to the nearest copper plane (H), and the relative permittivity ($\mathcal{E}_r$) of the material (commonly FR-4) between the microstrip and the nearest plane. When two microstrips run parallel to each other, cross-coupling occurs. The space between the microstrips (S) as related to their height above a plane (H) affects the amount of cross-coupling that occurs. The amount of cross-coupling increases as the space between the microstrips is reduced. As cross-coupling increases, the microstrips' impedances decrease. Differential impedance, Z_{diff}, is calculated by measuring the impedance of both the microstrips and summing them.

Figure 36 illustrates a cross-sectional representation of a PCB, showing (from top to bottom) the differential traces, the substrate, and the ground plane.

Figure 36. Microstrip Model of Differential Impedance



Equation 3 and Equation 4 provide the formulas necessary to estimate differential impedance using a 2D parallel microstrip model. Table 15 provides the definition of the variables. These formulas are valid for the ratios 0.1 < W/H < 2.0 and 0.2 < S/H < 3.0. Commercial utilities can obtain more accurate results using empirical or 3D modeling algorithms.

Equation 3. Differential Impedance Formula

$$Z_{diff} = 2 \times Z_0(1 - 0.48e^{-0.96S/H})$$

Equation 4. Impedance of One Microstrip

$$Z_0 = (87/(\mathcal{E}_r + 1.41)^{0.5}) \ln(5.98H/0.8W + T)$$

Table 15. Definition of Differential Impedance Variables

Variable	Description
Z_{diff}	Differential impedance of two parallel microstrips over a plane
Z_0	Impedance of one microstrip over a plane
W	Width of the traces
H	Distance from the ground plane to the traces
T	Trace thickness (1/2 oz copper ≅ 0.65 mils)
S	Space between differential traces (air gap)
$\mathcal{E}_r$	Relative permittivity of substrate (FR-4 ≅ 4.5)

Document History

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Document Number: 001-91378

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4298984	PRJI / RSKV	03/06/2014	New Application Note.
*A	4651225	PRJI	02/04/2015	Updated Schematic Design Requirements: Updated Power System: Updated Table 4. Updated to new template.
*B	5668493	PRVE	03/22/2017	Updated Abstract. Added a Note below Table 1. Updated VBUS_DS and VBUS_US (description). Updated to new template. Completing Sunset Review.

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