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PSoC® 5 to PSoC 5LP Migration Guide

Author: Mark Ainsworth
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For a complete list of related application notes, click here.

If you have a question, or need help with this application note, contact the author at mkea@cypress.com

AN84741 provides an overview of topics to consider when migrating from PSoC® 5 to PSoC 5LP devices. Device considerations and PSoC Creator topics are also discussed.

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Introduction

If, instead of PSoC 5, you want to migrate from a PSoC 3 design to PSoC 5LP, see AN77835, PSoC 3 to PSoC 5LP Migration Guide.

The PSoC 5 and PSoC 5LP devices are designed for easy migration from PSoC 5 to PSoC 5LP. Although there are some differences such as additional features in PSoC 5LP, the programmable analog, programmable digital, programmable routing, pin functions, and other features are quite similar. Furthermore, the PSoC Creator IDE handles a lot of the migration issues for you, automatically. Often, migrating a PSoC Creator design is as simple as specifying a new part and then rebuilding the project.

However, you should keep in mind some considerations when planning for migration. For example, additional features in PSoC 5LP may make it desirable to reassign pins on the PCB.

This application note discusses all of the topics that you should consider when migrating a project or product from PSoC 5 to PSoC 5LP. Both device level and PSoC Creator project level considerations are covered. If you are new to PSoC 5 or PSoC 5LP, see one of the PSoC 5 or PSoC 5LP datasheets or AN77759, Getting Started with PSoC 5LP. For hardware design topics, see AN61290, PSoC 3 and PSoC 5LP Hardware Starting Guide.

Device Differences

The major difference between PSoC 5 and PSoC 5LP is additional features, including boost, EMIF, CAN, temperature sensor, and faster SAR ADCs. For details see Table 1, and for more information see the specific device datasheets.

Note At this time all PSoC 5LP datasheet specifications are preliminary.

Table 1. Major Differences between PSoC 5 and PSoC 5LP

Consideration	PSoC 5	PSoC 5LP
Functional blocks available only in PSoC 5LP	Not available	Boost
		External Memory Interface (EMIF)
		CAN
		Die temperature sensor
Nonvolatile latches (NVLs) NOT available in PSoC 5	Fixed settings are: I/O ports always in high impedance analog configuration until they are configured. no configurable XRES - Pin P1[2] is always a GPIO boot speed is per 12 MHz FIMO always using SWD - no JTAG no ECC, that flash can only be used for configuration or general purpose storage	Full NVL-based configuration; for details see the PSoC 5LP datasheet.
Operating voltage	2.7 V–5.5 V	1.8 V–5.5 V
Operating frequency	67 MHz max (ES1 versions were formerly specified at 80 MHz)	67 MHz max
MHzECO	MHzECO pins cannot be used as GPIOs	Can be used as GPIOs
Low-power modes	Sleep: wakeup only from central time wheel (CTW) at 128 msec max intervals. No PICU (including USBIOs), I^2C, or comparator wakeup. 10-µF capacitors required on each Vccx for sleep. Only ILO can be used for timing during sleep. Watchdog timer (WDT) can only be used in active mode	Sleep: wakeup from a variety of sources including central time wheel (CTW) at 4096 ms max interval, RTC, I^2C, comparator, and pin interrupts (PICU). ILO or kHzECO can be used for timing during sleep.
	Hibernate: wakeup only from device reset. No PICU (including USBIOs) wakeup.	Hibernate: wakeup from PICU.
Internal main oscillator (IMO)	3 MHz to 48 MHz, 5% accuracy at 3 MHz. For communication functions such as UART it is recommended to use an external crystal instead of the IMO. With either IMO or crystal as a source, the PLL can be used to generate higher frequencies, with the same accuracy as the source.	3 MHz to 62 MHz, 1% accuracy at 3 MHz. With either IMO or crystal as a source, the PLL can be used to generate higher frequencies, with the same accuracy as the source.
USB	For USB a 24 MHz external crystal is required, and bus clock must be > 33 MHz.	IMO has a mode that adjusts to the USB signal as a reference, requiring no external crystal for USB.
Timers	Fixed-function timer interrupt outputs not available, can still route the TC output to an interrupt through the DSI. UDB-based timer, counter and PWM components can be created.	Four fixed-function timers that can operate in counter, timer or PWM mode. UDB-based timer, counter and PWM components can also be created.

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Consideration	PSoC 5	PSoC 5LP
UDBs	Sync and pulse modes not available in control registers	Sync and pulse modes are available in control registers
Debug	JTAG not available, only SWD. SWV is always on when SWD is being used; impacts usage of P1[3]. Pull-down required on SWDCK if doing SWD over USBIOs.	JTAG, SWD, SWV, TRACEPORT. JTAG support available from a variety of third party sources, see General PSoC Programming
Electrical specifications **(At this time, all PSoC 5LP datasheet specifications are preliminary.)**	Full-chip I_{DD} at 6 MHz: 6 mA typ	Full-chip I_{DD} at 6 MHz: 3.1 mA typ
	Each V_{DDIO} can source up to 20 mA through its pins, and sink up to 100 mA.	Each V_{DDIO} can source and sink up to 100 mA through its pins.
	Opamp: V_{OS} 3 mV max, max drive current 10 mA. Only one power mode (high),	Opamp: V_{OS} 2.5 mV max, max drive current 25 mA. Four power modes available.
	Del-sig ADC: Ge 0.6%, V_{OS} (buffered) ±0.65 mV, I_{DD} 4 mA. No rail-to-rail mode in the buffer, EOC signal cannot be routed through the DSI.	Del-sig ADC: Ge 0.2%, V_{OS} (buffered) ±0.2 mV, I_{DD} from 1.2 mA to 4 mA
	SAR ADCs: up to 700 ksps	SAR ADCs: up to 1 Msps
	Voltage reference: –0.7% / +0.9%	Voltage reference: ±0.1%
	Comparator: V_{OS} 15 mV	Comparator: V_{OS} 10 mV
	DAC: update rate 5.5 Msps, Ge ±5%, ZSe ±2.5 LSB, INL ±3 LSB, DNL ±1.6 LSB, glitches in response	DAC: update rate 8 Msps, Ge ±2.5%, ZSe ±1 LSB, INL ±1 LSB, DNL ±1 LSB
	SC/CT (PGA, TIA, mixer): TIA, PGA V_{OS} 20 mV, TIA input BW 1 MHz, PGA Ge ±2%	SC/CT (PGA, TIA, mixer): TIA, PGA V_{OS} 10 mV, TIA input BW 1.2 MHz, PGA Ge ±0.15%
	LCD: I_{DD} 63 µA, segment driver current 148 µA	LCD: I_{DD} 38 µA, segment driver current 260 µA
	USB: I_{USB} in configured mode 55 mA	USB: I_{USB} in configured mode 10 mA
	Flash: total device programming time 9 s typ.	Flash: total device programming time 5 s typ.

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Hardware Design Considerations

To plan for project migration, the first step is to review your overall system, focusing on the power system, PCB design, and the PSoC Creator project. As Table 1 shows, PSoC 5LP has some differences from PSoC 5.

Power System

Table 1 shows several considerations that may affect your product's power system design:

- The minimum operating voltage for PSoC 5 is 2.7 V, whereas PSoC 5LP can run down to 1.8 V. Note that PSoC V_{DDIO} voltages and pins can be set up for level shifting, to more easily interface PSoC with other ICs on the PCB.
- Depending on usage, PSoC 5 and PSoC 5LP consume different amounts of current. Generally PSoC 5LP consumes less than PSoC 5.
- PSoC 5 low-power modes and wakeup conditions are more restricted than for PSoC 5LP, so you should review your product's sleep and wakeup requirements.
- The boost feature is not available in PSoC 5.

Pin Assignment and PCB Design

Table 1 also shows considerations that may affect your PSoC pin assignments, as well as your overall PCB layout and design. Specifically:

- The PSoC 5 MHzECO pins cannot be used as GPIOs; they can with PSoC 5LP. Also with PSoC 5, many functions such as UART require a crystal (MHzECO) or other high precision clock source, which may not be needed with PSoC 5LP.
- JTAG is not available in PSoC 5, only SWD / SWV. This impacts usage of certain P1 pins, including P1[3]. All debug and trace functions, with corresponding pin usage, are available in PSoC 5LP.
- The EMIF, CAN, and temperature sensor features are not available in PSoC 5; they are in PSoC 5LP.

Analog Performance

Finally, Table 1 shows differences in the electrical specifications that may affect the analog performance of your PSoC Creator project. You should review your product's analog system requirements and make sure that they can be met by PSoC 5 and PSoC 5LP.

PSoC Creator Considerations

When you do change the device in your product, you must update your PSoC Creator project. This application note covers how to migrate PSoC Creator 2.1 SP1 projects. If you currently have a PSoC Creator 1.0 project, you should first migrate it to PSoC Creator 2.1 SP1. When you do, you may need to handle some issues, including:

- Obsolete devices
- Migrating components from PSoC Creator 1.0

Information on these topics can be found in the PSoC Creator 2.0 Migration Guide and the PSoC Creator 2.1 SP1 Migration Guide.

Once you have a stable and working project with PSoC Creator 2.1 SP1, you should save an archive or backup copy – this is always good practice. You can then change the device in that project. There are two steps involved:

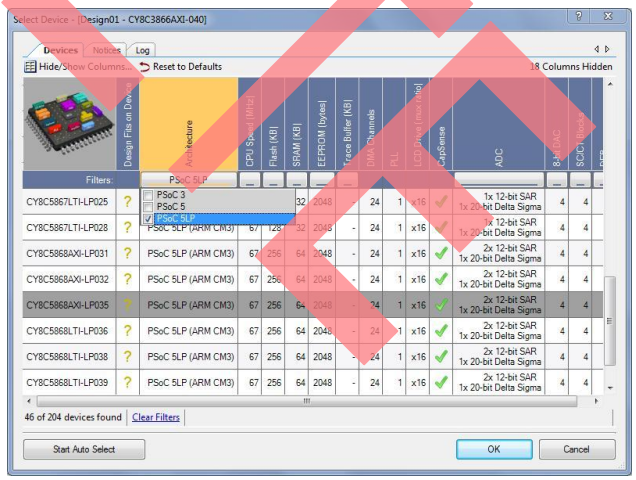
- Selecting the new device
- Clearing initial build errors

The remainder of this application note details how each of these steps should be done.

PSoC 5LP Device Selection

The first step to migrate a project is to select the appropriate device. The differences noted in Table 1 notwithstanding, all of the devices have similar packages, pinouts, peripheral blocks, and functions, so in many cases it is easy to find the right device. The best way to start is to review the various device family datasheets. In addition, PSoC Creator offers a handy dialog to assist with device selection, as Figure 1 shows.

Figure 1. PSoC Creator Device Selector Dialog



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Once you have selected your new device, you must change your PSoC Creator project from a PSoC 5 project to a PSoC 5LP project - do the following steps:

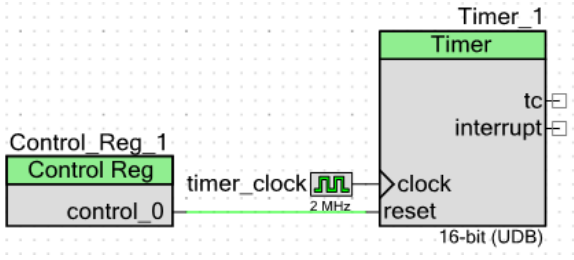
- Go to menu item Project > Device Selector
- In the dialog box (see Figure 1) click the button under the "Architecture" column, and make sure that "PSoC 5LP" is checked.
- Click on the row for the device you want, then click OK. The dialog box will close and the project in the Workspace Explorer window will show the new device.
- Rebuild the changed project.

Static Timing Analysis Warnings

One class of warnings that may come up when migrating a design is static timing analysis (STA). These occur when signals between digital blocks may not meet setup and hold time requirements-for more information, see AN81623, PSoC Digital Design Best Practices. Let us look at one example.

In Figure 2, a control register is driving the reset input of a UDB-based timer. What is not apparent is that the highest frequency clock in the design, that is, the bus clock, is clocking the control register. With a high frequency bus clock, you can get setup time violations between bus clock and the timer clock:

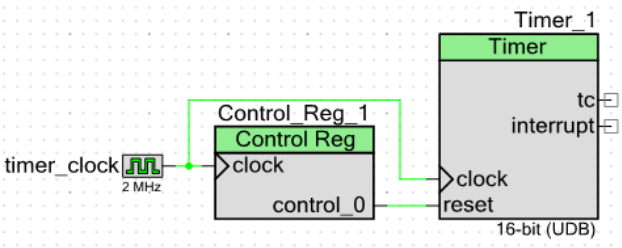
Figure 2. STA Errors from Multiple Clocks




```
Warning-1366: Setup time violation found in
a path from clock ( CyBUS_CLK ) to clock
( timer_clock ).
```

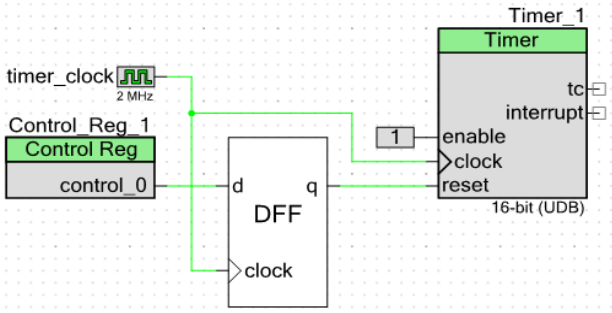
In PSoC 5LP, this is easy to fix by putting the control register in Sync mode, as Figure 3 shows:

Figure 3. PSoC 5LP Sync Mode



However, this solution cannot be used with PSoC 5 because the control registers are clocked only by bus clock. Therefore, an alternate solution, which works for all devices, is to use a DFF as Figure 4 shows:

Figure 4. PSoC 5 and PSoC 5LP DFF Solution



Note also that this design actually causes another STA warning due to another control register associated with the UDB datapaths in the Timer component. The best way to handle this warning is to turn on the Timer hardware enable and then, assuming you want the Timer to be always enabled, just tie it high.

The full STA report is provided as a standalone HTML report in the Results tab of the Workspace Explorer window.

Analog Routing Differences

The analog routing in PSoC 5 is different from that in PSoC 5LP. This is most easily seen at the inputs to the delta-sigma ADC and the SC/CT blocks. For details, see Figure 8-2 in the respective datasheets. PSoC Creator is aware of the routing differences, so in many cases you can just rebuild the project for the new device, and the project's functions and performance generally remain unchanged.

However, note that you can constrain or manually optimize the analog routing, by using the Manual Routing components or the Analog Editor in PSoC Creator 2.1. If your design has these constraints, it may not directly port to the new device. In this case, you must either change your usage of the Manual Routing components or re-route manually using the Analog Editor.

Porting Firmware

Because PSoC 5 and PSoC 5LP both have the Cortex-M3 CPU, there are no firmware porting issues. PSoC Creator supports the gcc and MDK compilers for both families.

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Summary

This application note has provided a detailed discussion of considerations for migrating designs from PSoC 5 to PSoC 5LP devices.

The best way to avoid problems when migrating designs is to plan ahead. The overall product requirements and system-level design should be reviewed to make certain that all device families can be used. Then, design the PCB so that parts from both families can be used. Finally, design the PSoC Creator project schematic, *.cydwr* file, and code such that the project can be rebuilt for all devices that you plan to use.

Related Application Notes

- AN77835 – PSoC 3 to PSoC 5LP Migration Guide
- AN77759 - Getting Started With a PSoC 5LP
- AN61290 - PSoC 3 and PSoC 5LP Hardware Starting Guide
- AN81623 – PSoC 3 and PSoC 5LP Digital Design Best Practices

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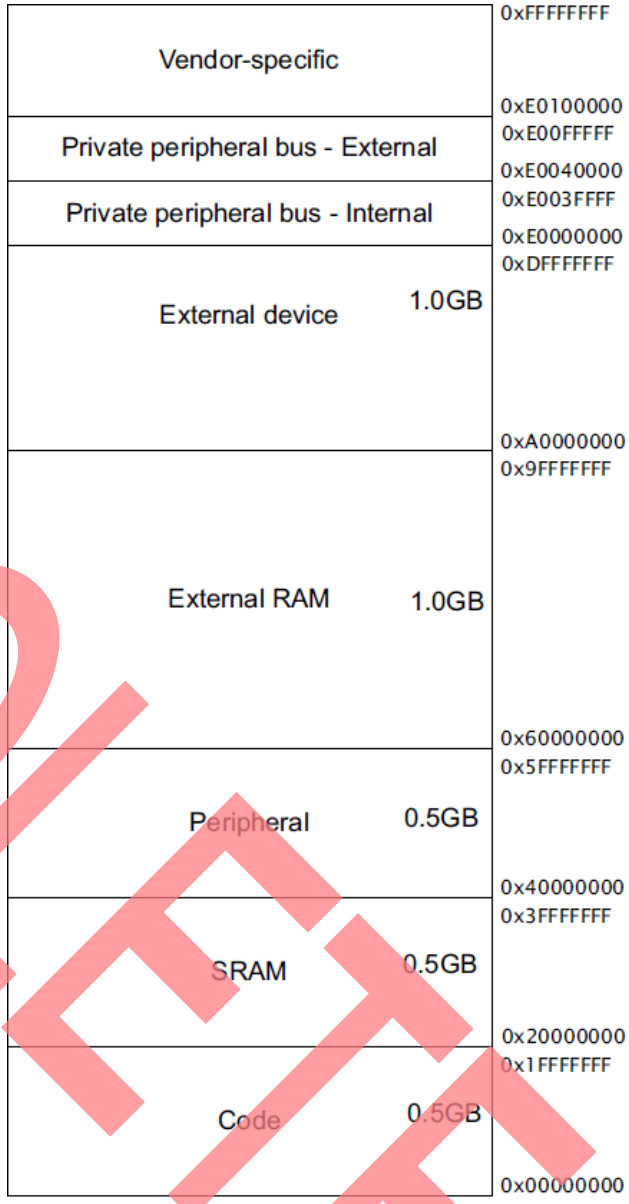
Appendix A – Memory Map

The ARM Cortex-M3 architecture uses a single 32-bit linear memory map, as Figure 5 shows. The SRAM in PSoC 5 and PSoC 5LP actually occupies the addresses 0x1FFF8000 to 0x20007FFF, centered on the boundary between the Cortex-M3 Code and SRAM spaces.

The remainder of the code space is occupied solely by flash, starting at address 0. The PSoC 5 and PSoC 5LP registers occupy the Cortex-M3 Peripheral space.

Figure 5. PSoC 5 Cortex-M3 Memory Map



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