AN72332

Guidelines on System Design Using Cypress' USB 2.0 Hub (HX2VL)

Associated Part Family: HX2VL
Related Resources: For a complete list, click here.

AN72332 provides guidelines on system design with HX2VL, a high-performance, low-power USB 2.0 high-speed hub that is optimized for low-cost designs. Recommended system design and PCB layout techniques are included to help ensure best performance and full compliance with the USB 2.0 specification.

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1 Introduction

HX2VL is Cypress's next-generation family of high-performance, low-power USB 2.0 hub controllers. It has integrated upstream and downstream transceivers, a USB serial interface engine (SIE), USB hub control and repeater logic, and transaction translator (TT) logic. The HX2VL portfolio has Single-TT and Multi-TT versions, low-cost options with high performance. Typical applications include standalone hubs, motherboard hubs, monitors, printers, set-top boxes, and docking stations. HX2VL has integrated external components, such as a voltage regulator, pull-up or pull-down resistors for the D+ and D– pins, and signal termination resistors. These built-in features help contain the system cost.

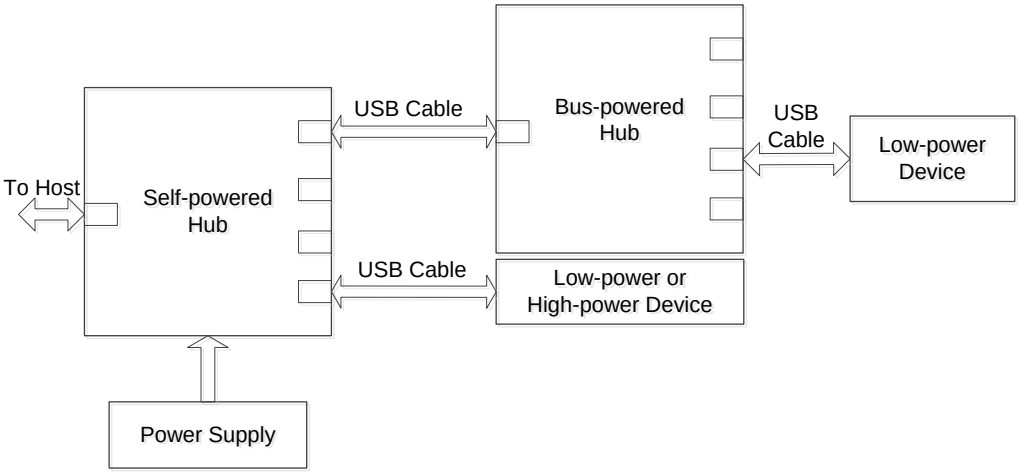
This application note covers hardware design guidelines and thermal design guidelines for HX2VL. An overview of the package options is also provided.

2 Overview of USB 2.0 Hub System

A USB hub supplies data and power to downstream USB ports. It also enables the USB Host to manage the power of the devices connected to its downstream ports using software. The HX2VL system design requires a basic understanding of some USB 2.0 concepts and terminology, such as self-powered device, bus-powered device, Gang mode, Individual mode, and so on.

Hubs can be either self-powered or bus-powered, as shown in Figure 1. This section provides an overview and design considerations for each type. Table 1 summarizes the differences between them.

Figure 1. Self-Powered and Bus-Powered Hub Configurations



2.1 Self-Powered Hub

A self-powered hub (Figure 2) distributes power from a local power supply to its downstream ports. Power for the hub's controller can come from either a local power supply or VBUS. Self-powered hubs can draw a maximum of 100 mA for their operation. A self-powered hub that uses VBUS to power its USB interface is called a "hybrid-powered hub." Using a hybrid-powered hub makes it possible to distinguish between a disconnected and powered off device.

2.1.1 Design Considerations

- Self-powered hubs need a mechanism to check for the presence of VBUS and drive the D+/D– lines accordingly.
- Self-powered hubs need overcurrent protection (500 mA) on the downstream ports for safety.
- Use self-powered hubs in systems that have more than four downstream ports.
- Use self-powered hubs in systems that include high-power devices.

2.2 Bus-Powered Hub

When designing a bus-powered hub (Figure 3), you should consider size, cost, and port configurations. The starting point should be the number of ports you want in the configuration. The HX2VL family can support at most four downstream ports; some applications may implement only two or three ports. In the bus-powered configuration, the power for both the hub's internal operation and its downstream ports is supplied from VBUS on the hub's upstream-facing port. This configuration eliminates the need for a local power supply.

For a bus-powered hub, the limiting factor is the amount of power available from the upstream port. In general, the upstream port has a five-unit load. After considering the number of ports, you must determine the power source for the hub. Since USB supplies bus power up to 500 mA (a five-unit load), it is possible to run a hub from this power source. The limitation is that the downstream ports are only allowed to have 100 mA each. If the device you are trying to run needs more power, it will not function under a bus-powered configuration.

2.2.1 Design Considerations

- Never connect two bus-powered hubs in series. Bus-powered hubs cannot provide more than 100 mA and therefore cannot power a hub connected to one of its downstream ports.
- Bus-powered hubs cannot power high-power devices.
- Bus-powered hubs are required to have power switches to prevent excessive current from being drawn from the upstream port.

Table 1. Self-Powered Hub Versus Bus-Powered Hub

Item	Self-Powered HX2VL	Bus-Powered HX2VL
Local power supply	Required	Not required
Maximum current from upstream port	100 mA	500 mA
Downstream devices	Low- or high-power devices	Low-power devices
Power switches	Not necessary	Required
Overcurrent protection	Required	Not necessary
VBUS monitoring	Required	Not required (as upstream VBUS is connected to RESET circuitry)

Figure 2. Self-Powered Hub Configuration (Source: www.usb.org)

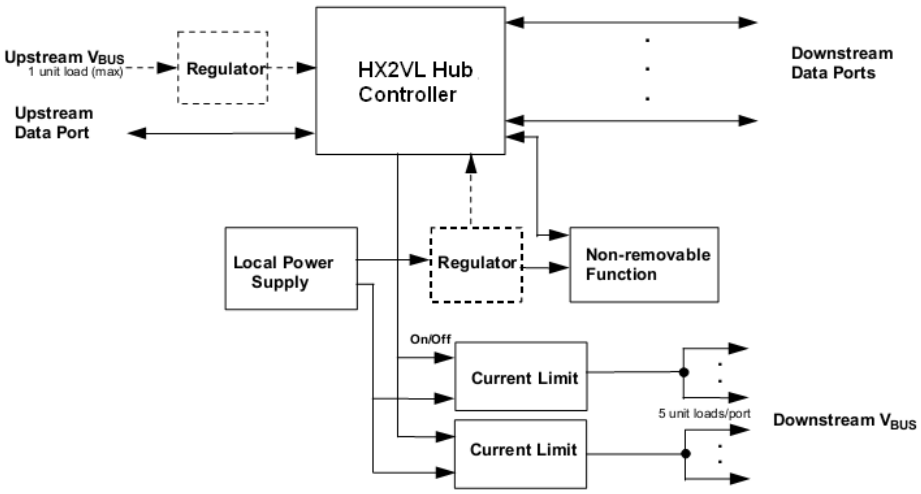
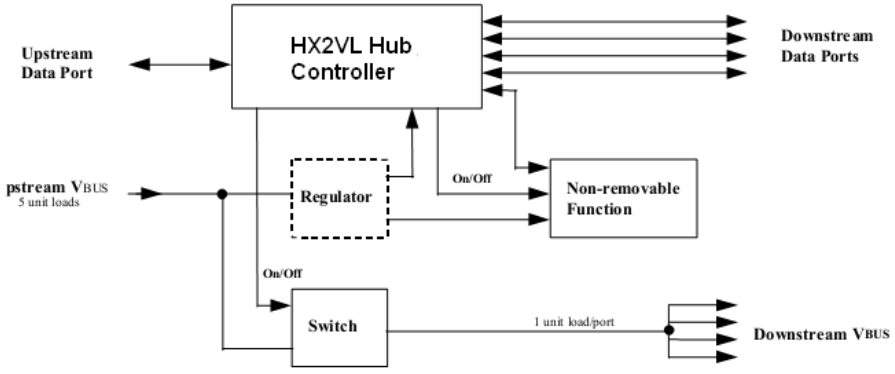


Figure 3. Bus-Powered Hub Configuration (Source: www.usb.org)



2.3 Gang Mode and Individual Mode Power Switching

For safety reasons, the USB specification (Rev. 2.0) requires overcurrent protection for all self-powered hub designs. An external power switch is required for overcurrent detection and power switching. Overcurrent protection can be implemented using polymeric PTC devices or solid-state switches.

Power switching means that the USB hub has the ability to turn power off to its downstream devices. Power switching is required for all bus-powered hub designs. Self-powered hubs can also implement power switching for downstream ports; however, it is not required (overcurrent protection is necessary in self-powered hubs). The power switch can be used for both power switching and overcurrent protection. Power switching can be implemented in Gang mode or Individual mode. In Gang mode, the hub turns off a group of ports if the total current drawn by all the ports together in the group exceeds a preset limit. In Individual mode, the hub turns off a single port if it exceeds its limit.

3 Hardware Design Requirements

The HX2VL USB 2.0 hub integrates the following:

- 1.5-kΩ pull-up resistor on the D+ line of the upstream port to notify the host that the device is connected
- 15-kΩ pull-down resistors on all downstream port D+ and D– lines
- Series termination resistors on all upstream and downstream port D+ and D– lines

These features optimize system cost by providing built-in support for the USB 2.0 specification.

3.1 Clock Requirements

HX2VL can accept a 12-MHz crystal or a 12/27/48-MHz oscillator as clock input, as indicated in Table 2. The SEL27 and SEL48 input pins are used to indicate the frequency of the clock input to HX2VL. The 28-pin QFN package does not have the SEL27 and SEL48 pins and supports only 12-MHz input.

Table 2. HX2VL Clock Selection

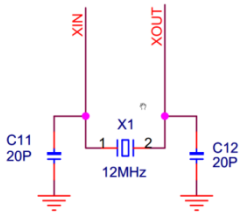
SEL48	SEL27	Clock Source
0	1	48-MHz oscillator
1	0	27-MHz oscillator
1	1	12-MHz crystal/oscillator

Following are the requirements based on the clock source.

3.2 Crystal Requirements

Crystal is a critical component for the proper functioning of HX2VL. The drive level of the crystal indicates how much power the crystal can tolerate. Figure 4 shows the crystal circuit.

Figure 4. Crystal Circuit



Consider the following parameters when you select the crystal:

- 12 MHz ± 0.05 percent
- Parallel resonant, fundamental mode
- 600-µW minimum drive level

The power dissipation of the crystal depends on the drive level of the XTAL-OUT pin (for HX2VL, this is 3.36 V), the desired frequency (12 MHz), and the equivalent series resistance (ESR) of the crystal.

3.2.1 Crystal Drive Level

Equation 1. Power Dissipation of the Crystal

$$P = I^2R = \left(\frac{V_x}{|Z|}\right)^2 R$$

$$= 2[\pi f\ (C_0 + C_L)\ V_x]^2\ R$$

Where:

f is the crystal frequency.

C_0 is the shunt capacitance of the crystal obtained from the crystal datasheet.

C_L is the load capacitance; for the C_L calculation, refer to the next section.

R is the crystal ESR obtained from the datasheet of the crystal.

V_x is the maximum voltage on the XTAL-OUT pin – 3.3 V.

A compatible crystal's power dissipation should not exceed the drive level limitation of the crystal. A crystal with a drive level less than the power dissipation will result in accelerated aging or even burnout of the crystal.

Calculating Load Capacitance Values

Load capacitance plays a critical role in providing an accurate clock source to HX2VL. Capacitors C11 and C12 (shown in Figure 4) must be chosen carefully based on the load capacitance value of the crystal. The load capacitance is calculated using Equation 2.

Equation 2. Load Capacitance of a Crystal

$$C_L = \frac{C_1 * C_2}{C_1 + C_2} + C_s$$

Cs is the stray capacitance of the XTAL_OUT and XTAL_IN traces on the PCB. Typically Cs ranges from 1 pF to 5 pF.

3.3 Oscillator

The XOUT pin should be left floating when an oscillator is used as the clock source.

Table 3. External Clock Input Requirements

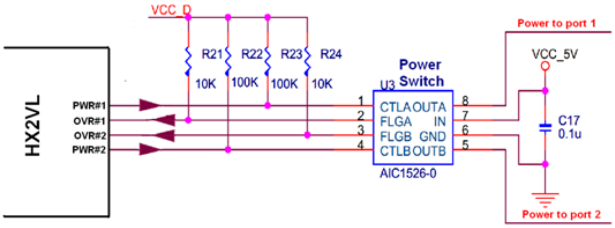
Parameter	Specification			Unit
	Min	Typ	Max	
Amplitude	3.15	3.3	3.6	V
Maximum frequency deviation	–	–	500	ppm
Duty cycle	45	50	55	%
Rise time/fall time	–	–	3	ns
Jitter (RMS)	–	–	260	ps

3.4 Downstream Power Switch and Overcurrent Protection

The downstream port power of the hub is allowed to have different configurations according to the USB specification. One basic requirement is that all ports must be protected. For port projection, a power switch with a current limit of 500 mA is used. A power switch monitors the current through the downstream ports and alerts HX2VL (OVR# pin) if there is an exception in the downstream port. Upon receiving an overcurrent alert, HX2VL disables the downstream port power using the PWR# pin.

- The overcurrent (OVR#) inputs need a pull-up resistor because most switches do not have an internal pull-up resistor. The recommended value of the resistor is 10 kΩ, as shown in Figure 5.

Figure 5. Power Switch Implementation



- If the power enable (PWR#) output is active high, a pull-down resistor is required. If the power enable (PWR#) output is active low, a pull-up resistor is required. The recommended value of the resistor is 100 kΩ. Since an active high PWR# pin requires a pull-down resistor on the pin, it is not recommended to use I^2C communication with PWR# as active high (applicable to the pin where the PWR# signal is multiplexed with the I2C_SDA signal).
- To configure power enable outputs (PWR# pin) as active high, the PWR_PIN_POL should be pin-strapped to logic high. To configure power enable outputs as active low, the PWR_PIN_POL should be pin-strapped to logic low, as indicated in Table 4.

Table 4. PWR_PIN_POL

PWR_PIN_POL	PWR#
Logic high	Active high
Logic low	Active low

- There are two power management modes: Gang mode and Individual mode. The GANG pin is used to configure the power management mode of the hub. It is reflected in the descriptor of the hub. In Individual mode, power switching is done on a per-port basis; in Gang mode, it is done for all the downstream ports. The GANG pin is connected to logic high for Gang mode and logic low for Individual mode, as indicated in Table 5.

Table 5. Gang Pin

Gang Pin	Power Mode
Logic high	Gang mode
Logic low	Individual mode

- Each port must have a minimum capacitance of 120 µF on the downstream VBUS according to the USB 2.0 specification. Otherwise, not enough current is supplied at inrush time to the device.

3.5 Power Configuration

A SELF_PWR pin is used to indicate whether the design is a self-powered or bus-powered design. This is reflected in the descriptor of the hub. SELF_PWR is tied to logic low for a bus-powered design and logic high for a self-powered design, as indicated in Table 6.

Table 6. SELF_PWR Pin Configuration

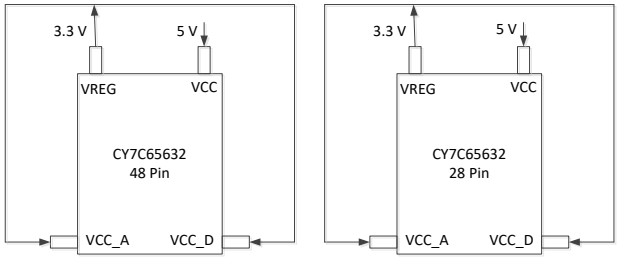
SELF_PWR	Power Configuration
Logic high	Self-powered
Logic low	Bus-powered

3.6 Power System

3.6.1 Internal Regulator

HX2VL has an option for an internal regulator. If an internal regulator is used, connect a 5-V supply to the VCC, and use VREG to supply the VCC_A and VCC_D pins, as shown in Figure 6. VCC_A and VCC_D provide 3.3-V analog and digital power to the chip.

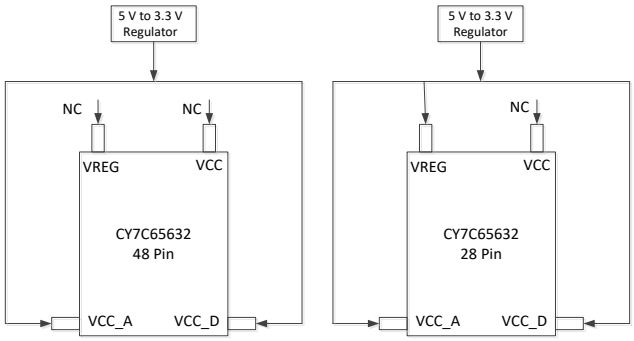
Figure 6. Internal Regulation Scheme



3.6.2 External Regulator

As shown in Figure 7, if an external regulator is used, VCC is a no-connect. Connect a 3.3-V supply to VCC_A and VCC_D. For a 48-pin TQFP package, VREG is a no-connect. For a 28-pin QFN package, VREG is connected to the 3.3-V supply.

Figure 7. External Regulation Scheme

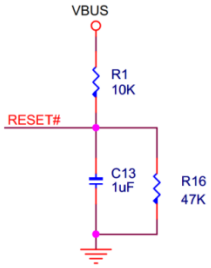


3.7 Reset Circuit

Per the USB specification, in the absence of VBUS, the upstream pull-up resistor should not be driven. The hub chip does not have a separate pin for monitoring VBUS. The reset pin divider circuit is used to achieve VBUS monitoring. In the absence of VBUS, the hub is in reset; as a result, the upstream port bus pull-up resistor is not driven.

RESET# is normally tied to VBUS through a 10-kΩ resistor and to GND through a 1-µF capacitor with a 47-kΩ resistor in parallel, as shown in Figure 8. No special power-up procedure is required.

Figure 8. Reset Circuit



3.7.1 HX2VL Device Supply Decoupling

Decoupling capacitors must be of the ceramic type with a stable dielectric. For a lower value capacitance, it is appropriate to use Class 1 dielectric capacitors: C0G (also referred to as NPO). Class 2 X7R must be used for the larger capacitance values. It is recommended to mix the 0.1-µF and 1-µF X7R capacitors to decouple the supply pins. The 0.1-µF capacitor must be C0G dielectric. This will help decouple the power supply at the frequency range of high-speed USB switching. Use a 10-µF bulk capacitor on the VREG pin and place it close to the pin. Table 7 summarizes the capacitor recommendations.

Table 7. Capacitor Recommendations for HX2VL

TQFP Pin Number	Capacitor Value	QFN Pin Number	Capacitor Value
12	0.1 and 1 µF	9	0.1 and 1 µF
16	0.1 and 1 µF	14	0.1 and 1 µF
VCC_A	0.1 µF	VCC_A	0.1 µF
VCC_D	0.1 µF	VCC_D	0.1 µF

3.8 Configurations

HX2VL is available in different packages and configurations. The 48-pin parts have full functionality, where features such as green/amber LED indicators, pin strapping, and Gang/Individual modes are supported on top of bare 28-pin parts that support self-power or bus power. There are four-port and two-port hubs.

This section describes how to set the HX2VL parameters using I^2C/SPI EEPROM and/or pin strapping. It also notes conditions under which an EEPROM is not required.

The configurable parameters of HX2VL are the following:

- VID
- PID
- Vendor string
- Product string
- Serial number
- Maximum power reported to host
- Number of active ports
- Removable/nonremovable port setting

Table 8 indicates how each parameter can be configured in a particular part. For more details on the pin map and alternate pin configurations, refer to the HX2VL datasheets.

Table 8. HX2VL Parts and Configuration Options

Device	No. of Ports	EEPROM Access		Method of Configuring Parameters			
		I^2C	SPI	Fixed Port 1 Fixed Port 2	Fixed Port 3 Fixed Port 4	Select Number of Ports	VID/PID, Strings, Maximum Power
CY7C65632-48	4	R/W	R	EEPROM/Pin Strap	EEPROM/Pin Strap	EEPROM/Pin Strap	EEPROM
CY7C65642-48	4	R/W	R	EEPROM/Pin Strap	EEPROM/Pin Strap	EEPROM/Pin Strap	EEPROM
CY7C65632-28	4	R/W	N/A	EEPROM	EEPROM	EEPROM	EEPROM
CY7C65642-28	4	R/W	N/A	EEPROM	EEPROM	EEPROM	EEPROM
CY7C65634-48	2	R/W	R	EEPROM/Pin Strap	N/A	EEPROM	EEPROM
CY7C65634-28	2	R/W	N/A	EEPROM	N/A	EEPROM	EEPROM

Table 9. Parameters and Default Values

Parameter	Default Value
VID	04B4h
PID	6572h (for CY7C65642) 6570h (for CY7C65632/34)
Number of ports	4 (2 for 2 port hubs CY7C65634-xx)
Port 1	Removable
Port 2	Removable
Port 3	Removable (N/A for 2 port hubs)

Parameter	Default Value
Port 4	Removable (N/A for 2 port hubs)
Maximum power	100 (32h)

3.8.1 Configuring HX2VL Using Pin Strapping

The removable/fixed port attribute of an active port and the number of active ports can only be set using this method and only in 48-pin packages. The 28-pin packages do not support pin strapping. In two-port hubs, only the removable/fixed port attribute can be set using pin strapping; changing the number of active ports is not supported. Table 10 indicates which pins can be used for pin strapping.

Table 10. Pins Used for Pin Strapping in 48-Pin Package

Pin Name	Pin No.	Function at POR
Fixed Port 1	45	0: Port 1 is removable 1: Port 1 is fixed
Fixed Port 2	35	0: Port 2 is removable 1: Port 2 is fixed
Fixed Port 3 (NC in 2-port hub)	32	0: Port 3 is removable 1: Port 3 is fixed
Fixed Port 4 (NC in 2-port hub)	23	0: Port 4 is removable 1: Port 4 is fixed
Set port num2	33	Refer to Table 11 for details.

Table 11. Number of Active Ports Using Pin Strapping

POR Logic State of Pins		Active Ports
Set port num2	Set port num1	
1	1	Port 1
1	0	Ports 1, 2
0	1	Ports 1, 2, 3
0	0	Ports 1, 2, 3, 4

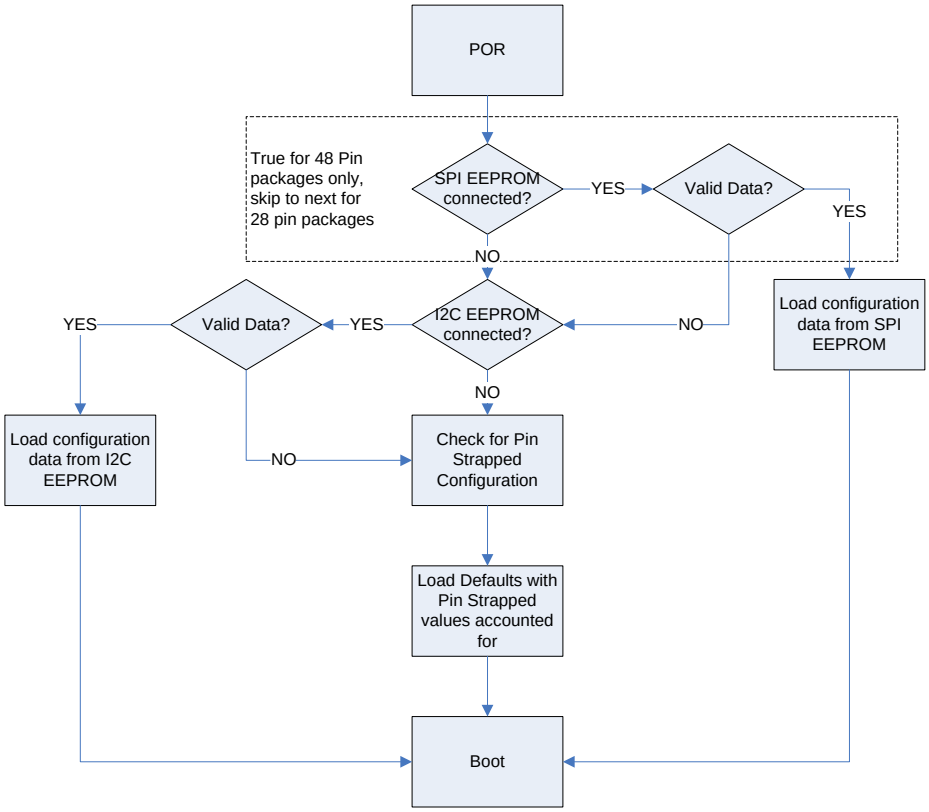
To pin strap a pin to logic high, connect it with a 10-kΩ resistor to V_{CC} (3.3 V). To pin strap a pin to logic low, connect it with a 10-kΩ resistor to GND.

Note The alternate function of these pins as a LED indicator is not available if the pins are strapped to logic high, unless a separate circuit is designed to support logic high disconnect after 60 ms of power-on reset (POR), when these pins are reconfigured as outputs.

3.8.2 Configuring HX2VL Using EEPROM

The HX2VL family of hubs supports booting from SPI and I^2C EEPROMs for loading configuration parameters. EEPROM contents, if valid, have a higher priority over the pin-strapping configuration. HX2VL first checks for SPI EEPROM and then for I^2C EEPROM if a valid configuration is not found via the SPI interface. Figure 9 shows the boot sequence.

Figure 9. HX2VL Boot Sequence



If I²C EEPROM is used:

- Address input pins (A0, A1, and A2) of the EEPROM should be tied to logic low.
- Connect a 10-kΩ pull-up resistor on the I2C_SDA line.

If SPI EEPROM is used, connect the pins from HX2VL to the corresponding pins of the EEPROM directly. No pull-up/ pull-down resistor is needed.

SPI EEPROMs are supported only in the 48-pin packages, as indicated in Table 12. HX2VL has only read access to these EEPROMs; hence, an external programmer is needed for loading the EEPROM with the parameters. ATMEL/AT93C46DN-SH-T is an example of an SPI EEPROM supported by HX2VL. To prevent the configuration contents of the SPI EEPROM from being overwritten, amber LED functionality is disabled when an SPI EEPROM is present.

Table 12. SPI EEPROM Connection

SPI EEPROM Pin	HX2VL Pin
CS	AMBER[1], pin 46
SK	GREEN[1], pin 45
MOSI	AMBER[2], pin 36
MISO	GREEN[2], pin 35

I²C EEPROMs are supported in all packages, as indicated in Table 13. HX2VL has read and write access to them. Thus, I²C EEPROMs are field programmable through the USB interface. ATMEL 24C02N_SU27 D, MICROCHIP 4LC028 SN0509, and SEIKO S24CS02AVH9 are examples of I²C EEPROMs supported by HX2VL. An I²C EEPROM programming utility (Blaster) is available with the HX2VL DVK.

Figure 10. I²C EEPROM

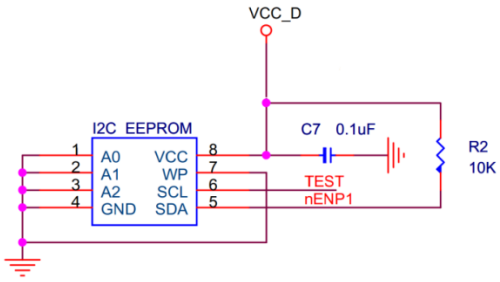


Table 13. I²C EEPROM Connection

I²C EEPROM Pin	HX2VL Pin	
	48-pin hub	28-pin hub
A0	GND	GND
A1	GND	GND
A2	GND	GND
SCL	TEST, pin 27	TEST, pin 18
SDA	PWR, pin 43	SDA, pin 26
WP1	V_{DD}/GND[1]	V_{DD}/GND1

The EEPROM content structure is shown in Table 14.

Table 14. EEPROM Contents

Byte Address	Value
00h	VID_LSB
01h	VID_MSB
02h	PID_LSB
03h	PID_MSB
04h	Check Sum
05h	Reserved – FEh
06h	Removable ports
07h	Number of ports
08h	Maximum power
09h - 0Fh	Reserved – FFh (except 0Bh, which is FEh)
10h	Vendor string length
11h - 3Fh	Vendor string (ASCII code)
40h	Product string length
41h - 6Fh	Product string (ASCII code)
70h	Serial number length
71h - 7Fh	Serial number string (ASCII code)

[1] WP should be tied high if the I²C EEPROM will not be programmed in the field. It should be tied low or left floating if the I²C EEPROM needs to be programmed in the field by BLASTER or other means.

- **Vendor ID/Product ID**: The least significant byte of the vendor ID is stored in byte 0, the most significant byte of the vendor ID is stored in byte 1, the least significant byte of the product ID is stored in byte 2, and the most significant byte of the product ID is stored in byte 3. For applications in which the USB Host is an embedded host such as an ASIC or SOC, there is no need to report a different VID/PID than the default Cypress VID/PID. In all other use cases, it is recommended that you have a user-specific VID/PID. You can obtain a VID from USB-IF (http://www.usb.org/developers/vendor/). Users maintain their own PID list.
- **Check Sum**: HX2VL checks for the condition "Check Sum = VID_LSB + VID_MSB + PID_LSB + PID_MSB + 1" on power cycle. If Check Sum passes, HX2VL loads the parameters from the EEPROM; otherwise, it ignores the EEPROM and loads the default parameters or as defined by pin strapping.
- **Removable ports**: This parameter configures each port either as a removable or fixed port. If bit x (x is 1, 2, 3, or 4) is set, port x is a fixed port; otherwise, it is a removable port. Bits 0, 5, 6, and 7 are set to 0.
- **Number of ports**: This parameter allows HX2VL to report and activate a subset of downstream ports if needed. A value of y (y is 1, 2, 3, or 4) means that downstream ports 1, 2, .., y are active. Other values of y will result in undefined behavior.
- **Maximum power**: The value of maximum power required by the hubs is reported in the Configuration Descriptor: bMax-Power field. A value of z (z is 00h to FAh) reports a maximum power field value of 2*z. In bus-powered mode, HX2VL must provide up to 100 mA per port. Therefore, its descriptor will limit the number of ports HX2VL can support. In self-powered mode, the power to the hub should be limited to 100 mA.
- **Strings**: The vendor, product, and serial number strings must comply with the USB specification, where the first byte of the string is the length of the string, and the string itself is in ASCII. HX2VL by default reports the language ID as 0409 (English). The language ID is not configurable. Therefore, the strings are decoded by the host accordingly.

3.8.3 Example

Table 15 shows the EEPROM contents for Cypress VID/PID, port 2 removable, ports 1 and 3 fixed, total 3 ports active, max power 200 mA, and strings "Cypress" "HX2VL" and "001E0007006D" for vendor, product, and serial.

Table 15. EEPROM Contents Example

Byte Address	Value
00h	B4h
01h	04h
02h	60h
03h	65h
04h	7Eh
05h	FEh
06h	0Ah
07h	03h
08h	64h
09h - 0Fh	Reserved – FFh (except 0Bh, which is FEh)
10h	07h
11h - 17h	43h, 79h, 70h, 72h, 65h, 73h, 73h
18h - 3Fh	Don't care (FFh)
40h	05h
41h - 45h	48h, 58h, 32h, 56h, 4Ch
46h - 6Fh	Don't care (FFh)
70h	0Ch
71h - 7Ch	30h, 30h, 31h, 45h, 30h, 30h, 30h, 37h, 30h, 30h, 36h, 44h
7Dh - 7Fh	Don't care (FFh)

3.9 Inputs/Outputs

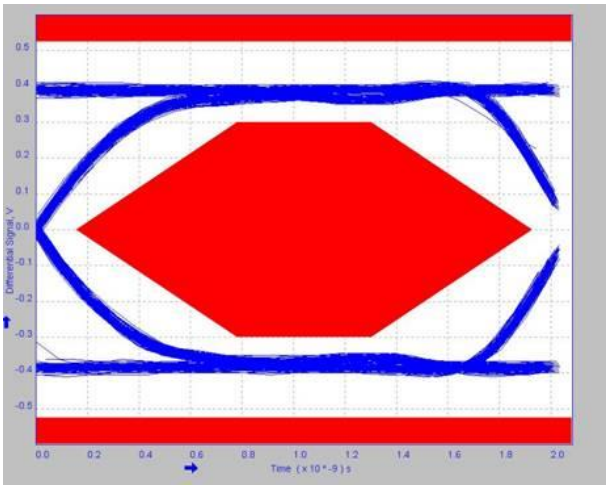
- Connect a 650-Ω USB 2.0 precision resistor with 1 percent precision to the RREF pin.
- For pin strapping pins, use a 10-kΩ pull-up resistor while connecting the pin to logic high. Use a 10-kΩ pull-down resistor while connecting the pin to logic low.

3.10 Electrical Design Recommendations

USB 2.0 high-speed signaling is used to transfer data at 480 Mbps. This rate is 40 times faster than the fastest speed of the USB 1.1 specification (full-speed signaling: 12 Mbps). High-speed signaling requires a greater level of attention to electrical design. Component selection, supply decoupling, signal line impedance, and noise are important considerations when designing for high-speed USB. Many of these considerations are influenced by the PCB design, as discussed in the PCB Design Recommendation section.

One key measurement of USB data signal quality is the eye pattern. The eye pattern is a representation of USB signaling that provides minimum and maximum voltage levels as well as signal jitter. Section 7.1 of the USB 2.0 specification provides a detailed explanation of and requirements for a compliant eye pattern. Figure 11 is an eye diagram of high-speed signaling as measured on the HX2VL component.

Figure 11. CY7C65642 Eye Diagram of High-Speed Signaling



In the diagram, notice how no signal traces overlap the central, six-sided, shaded area. In addition, no trace overlaps the extremes of permissible voltage, as shown in the shaded lines at the top and bottom of the figure. An overlap of signal trace over the shaded areas would be a violation of the USB 2.0 specification. Overlap can be caused by excessive data jitter, mismatched impedance, and improper EMI filtering.

4 PCB Design Recommendations

PCB design for high-speed signaling requires careful attention to component placement, signal routing, layer stackup, and selection of board material. These characteristics affect the electrical signal quality of the USB data pairs and the efficient dissipation of heat from the HX2VL hub component. This section offers guidelines for designing controlled impedance, high-speed USB boards to comply with the USB 2.0 specification.

High-speed USB PCBs are typically four-layer or more boards. Cypress does not recommend using a two-layer board for high-speed USB PCB design. The PCB design influences the USB signal quality test results more than any other factor. This section addresses four key areas of high-speed USB PCB design and layout:

- Controlled differential impedance
- USB signals
- Power and ground
- Crystal or oscillator

4.1 Controlled Differential Impedance

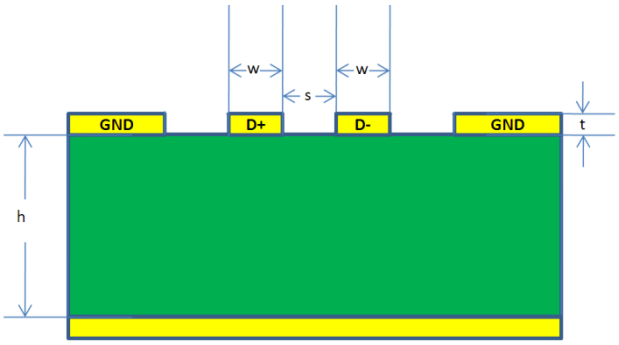
The controlled differential impedance of the D+ and D– traces is important in USB PCB design. The impedance of the D+ and D– traces affects the signal eye pattern, end-of-packet (EOP) width, jitter, and crossover voltage measurements. It is important to understand the underlying theory of differential impedance to achieve a 90 Ω ± 10 percent impedance.

4.1.1 Theory

A microstrip is a copper trace on the outer layers of a PCB. It has an impedance, Z_0, that is determined by its width (W), height (T), distance to the nearest copper plane (H), and the relative permittivity (ε_r) of the material (commonly FR-4) between the microstrip and the nearest plane. When two microstrips run parallel to each other, cross-coupling occurs. The space between the microstrips (S), as related to their height above a plane (H), affects the amount of cross-coupling. The amount of cross-coupling increases as the space between the microstrips is reduced. As cross-coupling increases, the microstrips' impedances decrease. Differential impedance, Z_{diff}, is calculated by measuring the impedance of both microstrips and summing them.

Figure 12 shows a cross-sectional representation of a PCB. From top to bottom, it shows the differential traces, substrate, and GND plane. Differential impedance can be estimated according to Equation 3 using a 2D parallel microstrip model.

Figure 12. Microstrip Model of Differential Impedance



Equation 3

$$Zdiff = 2Zo\left(1 - 0.48e^{-0.96*\frac{s}{h}}\right)\ ohms$$

Equation 3 is valid for 0.1 < W/H < 2.0 and 0.2 < S/H < 3.0. Commercial utilities can obtain more accurate results using empirical or 3D modeling algorithms.

Table 16. Parameters for Setting Impedance

Term	Description
h	Height of signal traces above ground plane
ε_r	Material dielectric constant
t	Trace thickness
w	Trace width
s	Spacing between each trace of a differential pair, inside edge to edge

Parameters h, t, w, and s may be any unit but must be consistent. For example, the HX2VL design referenced in this application note shows these units in mil (an English unit, 1/1000th of an inch). ε_r is a parameter with no units; it is dimensionless.

For an edge-coupled, surface microstrip, these five parameters (h, ε, t, w, and s) set the value for the differential impedance (Z_{diff}). The differential pair impedance, (Z_{diff}), is given in terms of the impedance of each line of the pair, (Z_o). The equations approximating impedance are as follows:

Equation 4

$$Zo = \left(\frac{87}{\sqrt{(Er + 1.41)}}\right) ln(\frac{5.98h}{0.8w + t}) ohms$$

Equation 3 and Equation 4 are good estimates when the following conditions are true:

Equation 5

$$\left(\frac{w}{h}\right) \leq 2.0$$

Equation 6

$$0.20 \leq \left(\frac{s}{h}\right) \leq 3.0$$

Table 17. Recommended Values for Four-Layer Board

Parameter Description	Tolerances	Recommended Value
Material thickness (mils)	±0.2	4.5
Material dielectric (mils)	±0.2	4.0
Trace thickness, 1 oz. (mils)	±0.1	1.2
Width (mils)	±0.5	8.0
Spacing (mils)	±1.0	8.0

Using the dimensions from the table, the Z_{diff} for the USB data pairs of the HX2VL Development Kit is 90 Ω +10 percent, –10 percent.

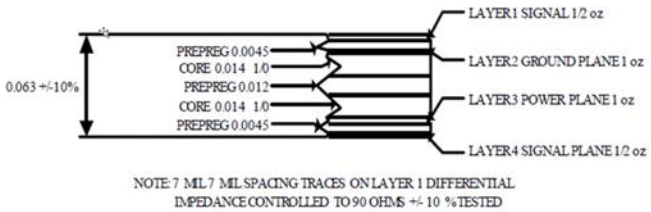
You should take advantage of any help available from the PCB manufacturer. The key dimensions and tolerances should be available from them. Some manufacturers will perform the impedance calculations for the designer, and others will provide a service to measure the impedance after the PCB is fabricated.

4.1.2 PCB Layer Stackup

For a USB 2.0 high-speed design, use at least a four-layer PCB for the best signal characteristics. With the primary components placed on the topside layer, the next layer must be a solid signal ground plane. A third voltage plane and fourth bottom side layer are typically the other two layers. The HX2VL component and its crystal must be placed on layer one, the top side. If you attempt a two-layer board, you will need to reduce the thickness of the PCB as well as increase the separation of traces and increase the trace widths to maintain the impedance match of the data lines.

The dielectric material thickness, “prepreg,” between layers 1 and 2 and the thickness between layers 3 and 4 are shown in Figure 13. This dimension is a key element in the design to set the proper characteristic impedance for the USB data traces. This is the “h” term mentioned in the previous section on PCB impedance design. Note that between layers 2 and 3 is the PCB's core material; this is not critical to characteristic impedance but is used to determine the overall board thickness.

Figure 13. Recommended PCB Stackup (HX2VL DVK)



When designing with a two-layer board, control of the trace impedance becomes more difficult. To maintain the same impedance on a two-layer board, the board must become thinner, and trace spacing and width will increase. Typically, since the thickness of the dielectric is the board thickness, the board must become thinner to hold down the trace width. Using half the thickness of the four-layer board will still result in traces that are 60-mil wide. A typical set of dimensions is listed in Table 18.

Table 18. Recommended Values for Two-Layer Board

Parameter Description	Tolerance	Min	Nominal	Max
Material thickness (mils)	±1.0	30.0	31	32
Material dielectric (mils)	±0.2	3.8	4.0	4.2
Trace thickness, 1 oz.(mils)	±0.1	2.3	2.4	2.5
Width (mils)	±0.5	59.5	60	60.5
Spacing (mils)	±1.0	59	60	61

4.2 USB Signals

There are five USB signals: VBUS, D+, D–, Shield, and GND.

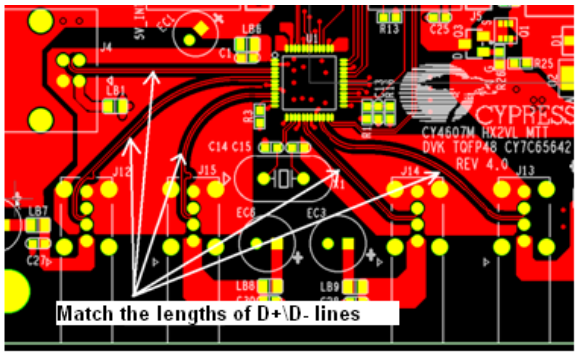
4.2.1 D+ and D–

Properly routing D+ and D– yields a high-quality signal eye pattern, EOP width, jitter, crossover voltage, and receiver sensitivity test results. The following recommendations improve signal quality:

1. Place the Cypress high-speed USB chip on the signal layer adjacent to the GND plane.
2. Route D+ and D– on the signal layer adjacent to the GND plane.
3. Route D+ and D– before other signals.
4. Keep the GND plane solid under D+ and D–. Splitting the GND plane underneath these signals introduces impedance mismatch and increases electrical emissions.
5. Avoid routing D+ and D– through vias; when vias are necessary, keep them small (25-mil pad, 10-mil hole) and keep the D+ and D– traces on the same layers.
6. Keep the length of D+ and D– less than three inches (75 mm). A 1-inch length (25–30 mm) or less is preferred.

   Match the lengths of D+ and D– to be within 50 mils (1.25 mm) of each other to avoid skewing the signals and affecting the crossover voltage, as shown in Figure 14.

Figure 14. D+\D– Lines Routing



7. Keep the D+ and D– trace spacing, S, constant along their routes. Varying the trace separation creates impedance mismatch.
8. Keep a 250-mil (6.5-mm) distance between D+ and D– and other non-static traces wherever possible.
9. Use two 45° bends or round corners instead of 90° bends.
10. Keep the common mode choke at the D+ and D– opening of the connector.
11. Keep the differential pair parallel and guarded by the ground.

Figure 15 shows the ESD diodes. Little fuse PGB1010603MR is supported by HX2VL.

12. Place the common mode chokes in a differential pair path, as shown in Figure 16.

Figure 15. ESD Connection

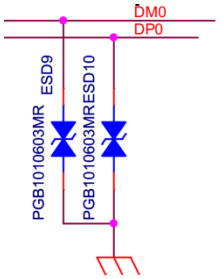


Figure 16. VBUS Filtering and Common Mode Choke on Differential Pair

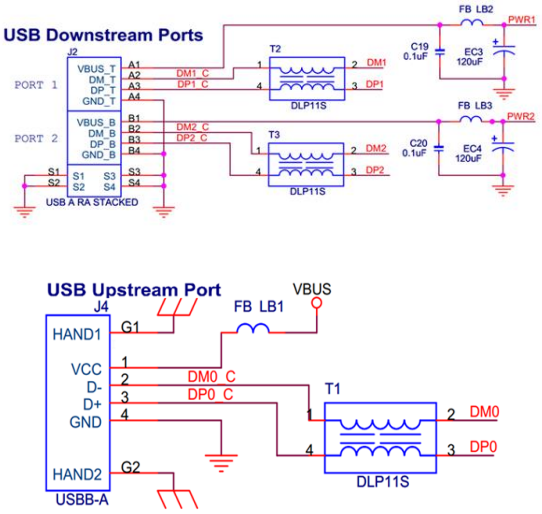
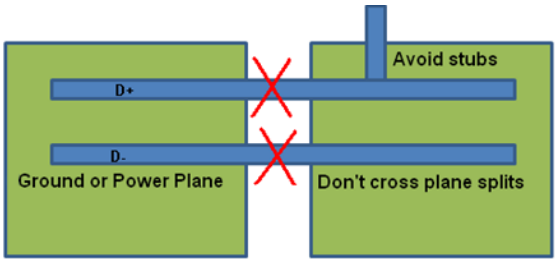


Figure 17. Improper Routing



4.3 VBUS, GND, and SHIELD

These recommendations for the VBUS, GND, and SHIELD signals improve inrush current measurements and reduce susceptibility to EMI, RFI, and ESD.

- Filter VBUS to make it less susceptible to ESD events. This is especially important if HX2VL uses VBUS to determine whether it is connected to or disconnected from the bus. A simple PI filter along with a bead for the downstream port and a single bead for the upstream port do well. See Figure 16 for details. The filter should be placed closer to the USB connector than the USB chip.
- Connect the shield to the GND.

4.4 EMI and EMC Considerations

EMI and ESD need to be considered on a case-by-case basis relative to the product enclosure, deployed environment, and regulatory statutes. This application note does not give specific recommendations regarding EMI.

The HX2VL requires an external 12/27/48-MHz crystal. The HX2VL hub includes circuitry to step up that frequency to support the 480-MHz bit rate of high-speed USB signaling.

Solid ground planes and short connections can help keep emissions low. Common mode chokes on the USB data pair will reduce emissions at the expense of signal quality. Other forms of EMI filtering such as ferrite beads in line with USB data lines and adding capacitance to the data lines are strongly discouraged, as significant corruption of signal quality may occur.

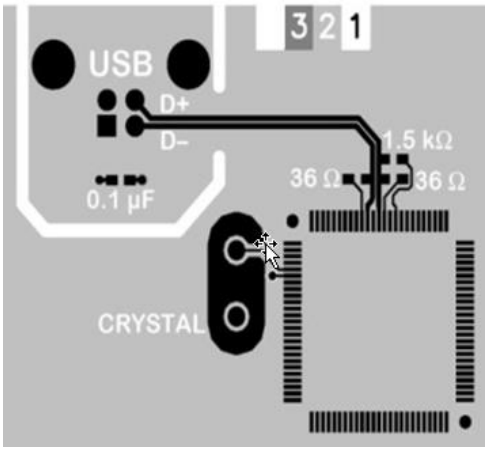
4.4.1 Power and Ground

It is important to provide adequate power and ground for high-speed USB designs. V_{CC} and GND planes are required for high-speed USB PCB design. They reduce jitter on USB signals and help minimize susceptibility to EMI and RFI.

The following guidelines are recommended:

- Use dedicated planes for V_{CC} and GND.
- Use cutouts on the V_{CC} plane if more than one voltage is required on the board (for example: 2.5 V, 3.3 V, and 5.0 V).
- Do not split the GND plane. Do not cut it except in the “USB Peninsula” shown in Figure 18. This reduces electrical noise and decreases jitter on the USB signals.

Figure 18. USB Peninsula



4.4.2 Power Traces

For situations in which it is not necessary to dedicate a split plane to a voltage level (for example, 5 V or 12 V), but the voltage is required on the board, route a trace instead.

The following guidelines are recommended for power traces:

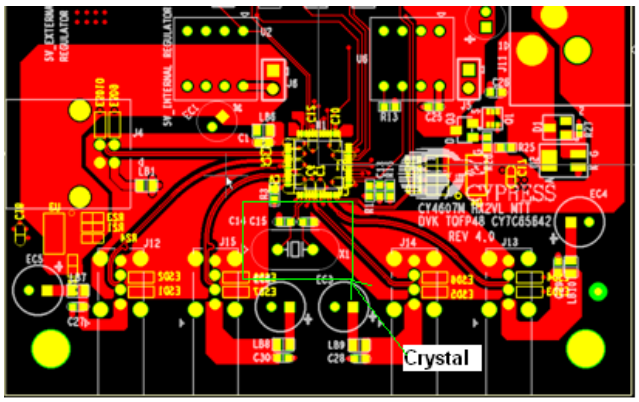
- Keep the power traces away from high-speed data lines and active components.
- Keep trace widths at least 40 mils to reduce inductance.
- Keep power traces short. Keep routing minimal.
- Use larger vias (at least 30-mil pad, 15-mil hole) on power traces.
- Provide adequate capacitance.

4.5 Crystal or Oscillator

A crystal or oscillator provides the reference clock for the HX2VL chip. It is important to provide a clean signal to the USB chip and not interfere with other high-speed signals, such as D+ and D–.

- Use a crystal or oscillator whose accuracy is +/-500 ppm with a drive level of 600 µW.
- Place the crystal or oscillator near the clock input and output pins of HX2VL.
- Keep the traces from the crystal or oscillator to the USB chip short.
- Keep the crystal or oscillator traces away from D+ and D–.
- Both the crystal pins must be guarded by the ground to avoid noise interference.
- Maximum suggested trace length between the crystal trace and the Cypress high-speed chip is 1 cm.
- Do not route the crystal trace underneath the IC, as it may trigger high-frequency oscillations over the PCB.
- Keep the coupling capacitors very close to the HX2VL part.

Figure 19. Reference Design for Crystal Placing, Differential Pair Routing, and VBUS Filter



5 Thermal Design Considerations

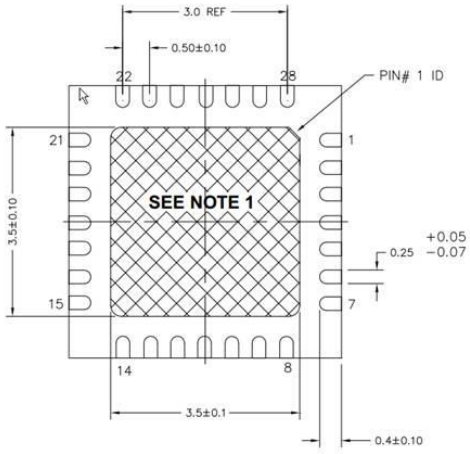
The QFN is a package with a small footprint and low profile. It has excellent thermal properties: a very low Θ_{ja} of approximately 25 °C per watt. These thermal properties are ideal for high-performance hubs.

The appropriate thermal design for use with the HX2VL component will help dissipate heat from the QFN package by conduction, not airflow. Heat is conducted away from the package through its bond to the PCB. From there, it is dissipated into the signal ground plane. Special attention to the heat transfer area below the package is required.

On the bottom of the package is a metal pad, referred to as the exposed die attach paddle (or simply exposed paddle). The exposed paddle is the means by which most of the HX2VL component thermal energy is dissipated away from the package. The exposed paddle is a square metal area approximately 5 mm on a side.

The design of the land area for the exposed paddle is critical to proper thermal transfer. The HX2VL component can operate without the thermal pad, but the results will cause the Θ_{ja} to increase to about 50 °C per watt. This is within the operating limits of the chip, but you will notice the heat difference on the chip. Maintaining the thermal pad and its connection will result in a much cooler die temperature. This thermal pad is a copper fill, which is to be designed into the PCB and under the QFN to assist thermal transfer. The HX2VL must have this thermal connection.

Figure 20. Diagram of the PCB Land Area for CY7C65642



The signal ground plane provides the major area for thermal dissipation. The HX2VL uses the large internal layer of the PCB devoted to signal ground. This is a large board intended for demonstration and evaluation of the HX2VL component.

For a fielded product, some developers may need a much smaller board size than the HX2VL DVK. To maximize the area devoted to thermal dissipation, you must use the bottom layer of the PCB. This is in addition to the internal solid ground plane, which must be kept to maintain proper signal impedance.

The enclosure for the circuit board assembly affects the thermal performance. This application note does not give a specific example of an enclosure design. However, following the guidelines for PCB design described in this application note will help ensure the most efficient method to conduct heat away from the QFN package without the use of heat sinks. A large, solid ground plane with no large gaps close to the QFN mounting area will efficiently conduct heat through the PCB.

6 Package Description

The hub controllers are available in two packages:

- 28 QFN (5 mm x 5 mm x 0.75 mm) Pb-free package
- 48 TQFP (9 mm x 9 mm x 1.4 mm) Pb-free package

See the latest HX2VL datasheets for detailed package drawings.

7 HX2VL Development Kit

HX2VL development kits are available in four options:

- CY4607 (48 TQFP package)
- CY4608 (28 QFN package)
- CY4607M (48 TQFP package Multi-TT)
- CY4608M (28 QFN package Multi-TT)

The DVK board designs follow the recommendations mentioned in this application note. You can download the reference schematics and the DVK design files from the Cypress website.

Figure 21. DVK Four-Port Hub



8 Related Resources

- Schematics
  - Schematic_CY7C65632-QFN28.pdf
  - Schematic_CY7C65632-TQFP48.pdf
- HX2VL datasheets
- AN15456 - Guide to a Successful EZ-USB® FX2LP™ Hardware Design
- AN69235 - Migrating from HX2/HX2LP to HX2VL

9 References

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*B	3489291	PRVE	01/10/2012	Updated Cypress Semiconductor’s HX2VL (CYC65632/34 and CY7C65642): Updated diagram. Minor text edits. Updated to new template.
*C	3756128	PRVE	09/26/2012	Updated Hardware Design Requirements: Updated Reset Circuit: Updated HX2VL Device Supply Decoupling: Updated description. Updated Table 7. Updated to new template.
*D	3848026	PRJI	12/20/2012	Updated Document Title to read as “AN72332 – Guidelines on System Design using Cypress' USB 2.0 Hub (HX2VL)” Merged contents of Application Notes AN73052, AN69025, and AN15454 into this application note.
*E	4085307	PRJI	08/05/2013	Updated Hardware Design Requirements: Updated Reset Circuit: Updated HX2VL Device Supply Decoupling: Updated Table 7.
*F	4958585	PRJI	10/14/2015	Updated Hardware Design Requirements: Updated Crystal Requirements: Updated description. Updated Crystal Drive Level: Updated description.
*G	5473820	RAJV	10/20/2016	Updated Related Resoures: Removed AN1168 and AN69025 from the list as these ANs are obsolete. Included AN15456 in the list. Updated to new template. Completing Sunset Review.
*H	5702100	GNKK	04/19/2017	Updated the Cypress logo and copyright information.
*I	6060390	HBM	08/01/2018	Removed a note from page 10 Updated template

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