AN69235

Migrating from HX2/HX2LP to HX2VL

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Associated Part Family: CY7C65640A, CY7C65630/20,CY7C65642/32/34

Associated Code Examples: None

Related Application Notes: None

AN69235 is intended to help the developer migrate a hub design based on EZ-USB® HX2 (CY7C65640A) and HX2LP (CY7C65630/20) to use the HX2VL (CY7C65642/32/34) hub. It also provides a feature comparison between HX2, HX2LP, and HX2VL to aid in selecting the appropriate part number for migration. Note that HX2 (TetraHub) is now not recommended for new designs.

1 Introduction

The HX2VL family is the next generation of USB high-speed hubs. This family of hubs includes:

- Four-port hubs:
  - CY7C65632 with a single transaction translator (TT)
  - CY7C65642 with four TTs
- Two-port hub: CY7C65634 with a single TT

The HX2VL family is not pin-compatible with HX2/HX2LP and it consumes less power than HX2/HX2LP. This application note highlights the difference between the products, and aids the designer in migrating existing designs to the HX2VL family.

For designs in which downstream devices are all high-speed or just a single full-speed/low-speed device, the performance of single TT and four TTs is the same. For this reason, a single TT hub should be considered for these designs.

Both the HX2LP and HX2 families are 56-pin, QFN packaged parts. The HX2VL family of chips is available in two package options:

- 48-pin TQFP package
- 28-pin QFN package

Both are the same in terms of the core hub functionality. This allows the designer to migrate to an appropriate package based on the requirement. All comments pertaining to HX2VL are applicable to package options. Accordingly, the appropriate part number (CY7C65642 or CY7C65632/34) in the HX2VL family can be chosen for migration.

For more details on HX2VL, refer to the HX2VL datasheet and application note AN72332 - Guidelines on System Design using Cypress's USB 2.0 Hub (HX2VL).

Note In this application note, HX2LP is used to refer to HX2 and HX2LP, except where noted. HX2VL is used to refer to CY7C65642 and CY7C65632/34, except where noted.

2 Hardware Changes

This section presents information on the required changes when using either configuration of the HX2VL chip.

2.1 Changes to the Crystal Specification

When using HX2VL, a primary change required is the crystal. When a crystal is used in the design, the load capacitance of the crystal must change for proper operation. This affects both the load capacitors and the crystal being used. HX2LP uses a crystal with the following specifications:

- 24 MHz ± 100 ppm
- Parallel resonant
- Fundamental mode
- 500-µW drive level

HX2 requires a crystal with load capacitors that are between 20 pF and 33 pF (5 percent tolerance). The HX2LP requires a crystal with load capacitors of 12 pF (5 % tolerance).

Following are the specifications for the crystal used with HX2VL:

- 12 MHz ± 500 ppm
- Parallel resonant
- Fundamental mode
- 600-µW drive level (maximum)
- 20-pF (5 percent tolerance) load capacitor

These specifications must be considered when selecting both the load capacitors and the crystal. Using a different crystal load capacitance with a crystal specified for 20 pF may affect the frequency shift. The designer should always ensure that the power dissipated by the crystal is within the crystal manufacturer's specifications. Overdriving the crystal may damage it.

HX2VL supports a clock source of 12-, 27-, and 48-MHz oscillators in the 48-pin TQFP package (28-pin QFN part supports only 12 MHz). The frequency tolerance remains the same regardless of the clock source.

2.2 EEPROM

HX2LP supports loading of configuration data from SPI EEPROM. The size of configuration data for HX2LP can be up to 512 bytes.

HX2VL supports loading of configuration data from either I^2C EEPROM or SPI EEPROM (only by 48-pin TQFP package). The size of configuration data for HX2VL can be up to 128 bytes. The size and type of EEPROM can be changed based on the requirement.

2.3 Regulator

HX2LP can be powered from a single 3.3-V supply. For a bus-powered design or a self-powered design with a supply other than 3.3 V, this mandates an external regulator.

HX2VL supports a 5-V to 3.3-V internal regulator. For a bus-powered or self-powered design with a 5-V supply, this results in system cost reduction. HX2VL can be powered from a single 3.3-V supply as well. The internal regulator of HX2VL can supply only up to 150 mA. This can be a bottleneck if the output of this regulator is used to supply other components of the design. The regulator configuration can be chosen based on these considerations.

2.4 Pin-strapping

Pin-strapping is the method of configuring HX2VL based on the state of certain pins at power-on reset (POR) or at a strapping period after POR. This is used to configure power management mode (ganged or individual), power enable switch polarity, number of ports, and non-removable port configuration. Through pin-strapping, the 28-pin QFN package supports only power management mode configuration.

3 Features

To understand the trade-offs during migration, Table 1 shows a comparison between HX2, HX2LP, and HX2VL.

Table 1. Feature Comparison between HX2, HX2LP, and HX2VL

Item	HX2	HX2LP	HX2VL (48-pin TQFP Package)	HX2VL (28-pin QFN Package)
Power consumption**	High (460 mA)	Lower than HX2 (231 mA)	Lower than HX2LP (82 mA)	Lower than HX2LP (82 mA)
Bus-powered mode	Not supported	Can support up to three downstream ports	Can support up to four downstream ports	CY7C65632/42 can support up to four downstream ports CY7C65634 can support up to two downstream ports
Power management mode	Yes (EEPROM configuration data)	Yes (EEPROM configuration data)	Yes (pin-strapping GANG pin)	Yes (pin-strapping GANG pin)
Self-powered mode	Yes (SELFPWR pin)	Yes (SELFPWR pin)	Yes (SELFPWR pin)	Yes (SELFPWR pin)
VBUS monitoring	Yes (VBUSPOWER pin)	Yes (VBUSPOWER pin)	Yes (RESET# pin)	Yes (RESET# pin)
Multiple TT	Yes	No	Yes for CY7C65642 No for CY7C65632 and CY7C65634	Yes for CY7C65642 No for CY7C65632 and CY7C65634
Number of ports	Yes (EEPROM configuration data)	Yes (EEPROM configuration data)	Yes (pin-strapping SET_PORT_NUMx (x = 1, 2) pins or EEPROM configuration data)	Yes (EEPROM configuration data)
Non-removable port	Yes (EEPROM configuration data)	Yes (EEPROM configuration data)	Yes (pin-strapping FIXED PORTx (x = 1..4) pins or EEPROM configuration data)	Yes (EEPROM configuration data)
Suspend indication	No	No	Yes (GANG pin)	Yes (GANG pin)
EEPROM	SPI	SPI	I^2C and SPI	I^2C
Power enable pin	Yes	Yes	Yes	Yes
LED indicators	Yes	Yes	Yes	No
Modulated indicators	No	Yes	No	No
Power polarity control	No	Yes (EEPROM configuration data)	Yes (pin-strapping PWR_PIN_POL pin)	No
Dual power descriptors	No	Yes	No	No
Multiple string descriptors	No	Yes	No	No

**These are typical values of supply current (I_{CC}) when the device is connected to a high-speed host and all four downstream ports are connected to high-speed peripherals.

4 Summary

This application note discusses the migration of an HX2/HX2LP-based hub design to an HX2VL-based hub design and the considerations associated with the migration.

Document History

Document Title: AN69235 - Migrating from HX2/HX2LP to HX2VL

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3237432	AASI	04/21/2011	New application note.
*A	3551005	PDAV	03/15/2012	Included CY7C65634 related information in all instances across the document. Updated Abstract: Updated description. Updated Introduction: Updated description. Updated Hardware Changes: Updated Regulator: Updated description. Updated Features: Updated Table 1: Added values in all columns corresponding to “Power consumption” item. Added a note below the table and referred the note in “Power consumption” item. Replaced “SET_PORT_NUM1 and SET_PORT_NUM2 pins” with “SET_PORT_NUMx (x = 1, 2) pins” in “HX2VL (48-pin TQFP package)” column corresponding to “Number of ports” item. Replaced “SET_PORT_NUM1 and SET_PORT_NUM2 pins” with “FIXED PORTx (x = 1..4) pins” in “HX2VL (48-pin TQFP package)” column corresponding to “Non-removable port” item. Replaced “No” with “Yes” in “HX2VL (28-pin QFN package)” column corresponding to “Power enable pin” item. Updated to new template. Completing Sunset Review.
*B	4764192	PRJI	05/13/2015	Updated Introduction: Removed reference of AN1071 (as it is an obsolete application note). Removed reference of AN69025 (as it is an obsolete application note). Added reference of AN72332 instead of AN69025. Completing Sunset Review.
*C	5792735	RUPA	07/27/2017	Updated Cypress logo and Copyright information.
*D	6199364	HBM	06/06/2018	Updated to new template. Completing Sunset Review.

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