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Spec No: 001-61668

Spec Title: BOOST TOPOLOGY FOR HB-LEDS - AN61668

Sunset Owner: Madhan Kumar Kuppaswamy

Replaced by: 001-52699

Boost Topology for HB-LEDs

AN61668

Author: Mukund Krishna
Associated Project: Yes
Associated Part Family: CY8CLED0xD/G01
Software Version: PSoC® Designer™ 5.0
Associated Application Notes: AN51012, AN60142, AN52209, AN53781, AN53127, AN52699

OBSOLETE

Application Note Abstract

PowerPSoC® introduces a new standard of designing power management systems for LED lighting solutions and other high power applications. This application note provides the details on implementing a grounded load Boost topology to drive LEDs with constant current control. Circuit topology is presented with explanation of basic operation and design equations. The note ends with description of firmware flow with an example project attached.

Introduction

High Brightness LEDs (HB-LEDs) are gaining a lot of importance as a replacement for incandescent and fluorescent lamps. Their reduced usage of energy for the same amount of light output, significantly longer life, and flexibility of use due to form factor are the driving factors for their adoption. However, HB-LEDs are unique amongst the light sources; they need a DC current to be regulated through them versus a constant voltage.

Switching regulators are the efficient method of regulating current through a HB-LED load. The choice of topology to use depends on the relationship between the input and output voltage. PowerPSoC supports the floating load buck, boost, and floating load buck-boost topologies. A 'buck' topology is used when the load voltage is lower than the input voltage; a 'boost' topology is used when the load voltage is higher than the input. Refer to the application notes, Floating Load Buck Topology for HB-LEDs – AN52699 for details on implementing a floating load buck topology using PowerPSoC, and Floating Load Buck-Boost topology for HB-LEDs – AN60142 for details on implementing buck-boost using PowerPSoC.

In the boost topology, the circuit operates when the input voltage is lower than the load voltage. The PowerPSoC family of devices has the capability to implement such a circuit topology.

This application note addresses the design of a 'grounded load boost circuit' to drive High Brightness LEDs using PowerPSoC. The topology accompanied by an explanation of the circuit is explained, followed by the design equations for the circuit, for choosing the external components. An example firmware project is included as an example of the implementation described. Note that the topology, circuit and equations presented in this note are similar to those presented in the application note, Floating Load Buck-Boost topology for HB-LEDs – AN60142. However, there are some key equations that are different. Another noticeable effect of using a 'Boost' vs. 'Buck-Boost' topology is that, the stresses on components such as the MOSFET and diode are decreased.

In PowerPSoC, the classic PSoC core is combined with high performance power electronics. This results in an integrated intelligent power electronics solution in a single QFN package. This family of devices (CY8CLED04D01) combines up to four independent channels of constant current drivers. These drivers feature hysteretic controllers with the Programmable System-on-Chip (PSoC®) which has an 8-bit microcontroller, configurable digital and analog peripherals, and embedded flash memory.

PowerPSoC is designed to operate at voltages from 7V to 32V, drive up to 1A of current per channel using internal MOSFET switches, and higher than 1A of current with external MOSFETs. For a detailed introduction on PowerPSoC and its features, refer to the application note, PowerPSoC Firmware Design Guidelines - AN51012 and the device datasheet.

Boost Topology

The topology discussed here is the 'grounded-load boost'. This topology can be used for systems where the input voltage is lower than the load voltage. Some variation is allowed but the essential condition must remain true.

Figure 1. Boost Regulator Using PowerPSoC

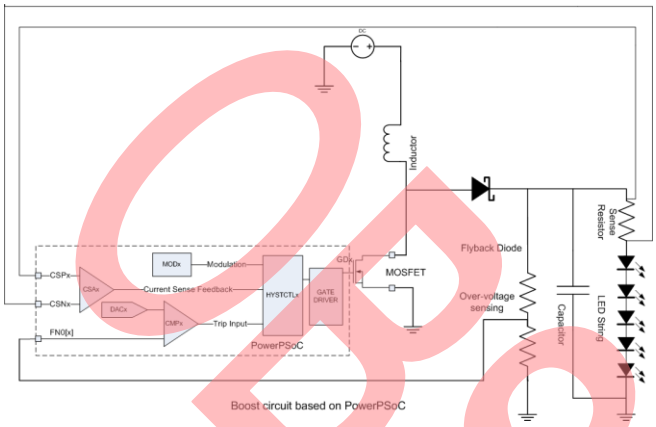


Figure 1 shows the simple schematic of a constant current boost regulator using PowerPSoC. There are two main parts to this circuit:

- **The Power Converter:** The transistor, diode, inductor, and capacitor form the power converter part of the circuit.
- **The Control:** The combination of the sense resistor, the Pulse Width Modulator (PWM) block, and the hysteretic controller inside PowerPSoC form the control section.

This topology is referred to as 'grounded load' because, the load which are the LEDs in this case are connected to ground.

Note: This is different from the 'floating-load buck' and 'floating-load buck-boost' topologies.

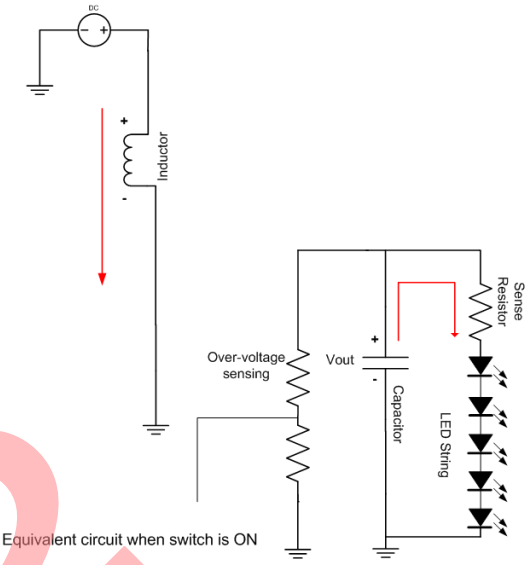
Circuit Operation

The qualitative explanation is as follows. Figure 4 on page 5 shows the snapshot of an oscilloscope of a boost system in operation.

- The PWM is a setup with a duty cycle higher than that is required for a boost (the calculation is explained later) so that, the output capacitor's voltage keeps increasing rather than settling at a voltage. This also causes the load current to increase, allowing the system to regulate it. Therefore, it constantly turns the switch ON and OFF periodically.
- When the switch is ON, the current through the inductor rises and the capacitor supplies current to the load. This is illustrated in Figure 2.

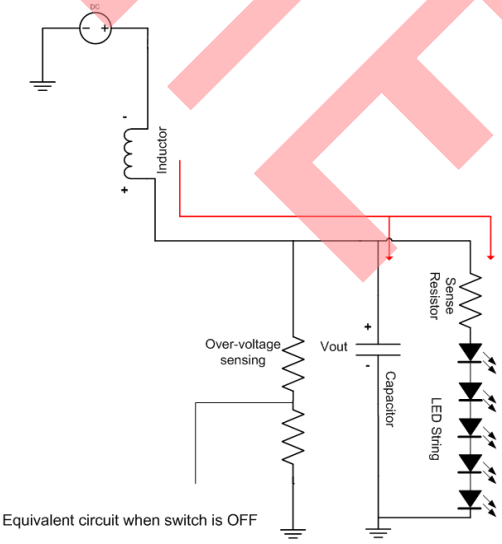
  Note: The FET and diode are present, although not shown in the figure for the sake of simplicity.
- When the switch gets turned OFF, the current in the inductor continues to flow and therefore the inductor switches its polarity, and the magnitude of the voltage across its terminals increases until the diode's threshold voltage is crossed.

Figure 2. Equivalent Circuit When Switch is ON



- When this occurs, the current flowing through the inductor flows into the capacitor and the load. The capacitor's voltage increases as the current flows into it. This is illustrated in Figure 3.
- The duty cycle of the PWM is chosen to be larger than required to just boost the voltage to the required value; therefore when the switch is turned ON, the increase in current through the inductor is larger than the decrease in current when the switch is turned OFF. As a result, the current through the inductor keeps increasing.

Figure 3. Equivalent Circuit When Switch is OFF



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- This causes the capacitor voltage to keep increasing and results in an increase in the load current.
- When the load current crosses the upper threshold set in the hysteretic controller (sensed by a resistor), the hysteretic controller turns the switch OFF independent of the PWM's output.
- This causes the inductor to discharge completely into the capacitor after which the capacitor is the sole supplier of current through the load.
- The current gradually decreases as the capacitor discharges its energy into the load. When the load current crosses the lower threshold set in the hysteretic controller, the switch is allowed to operate again as per the PWM's output. The cycle then repeats.

When the switch is off, the energy being driven into the capacitor is from a source resulting of a summation of the input voltage and the voltage across the inductor. Hence, a boost function is achieved.

Mathematical Model

This section describes the mathematical model for this topology.

Primary Circuit Parameters

These are the initial parameters of the system to be decided before the rest of the circuit components can be worked out. They are the following at a minimum:

1. **Input Voltage:** V_{in}
2. **Load Voltage:** V_o (this depends on number of LEDs in the string)
3. **Load Current:** I_o (this is the current that needs to be regulated)

Secondary Circuit Parameters

These are parameters derived from the initial parameters.

1. Boost Ratio

The boost ratio is defined as the ratio of the boosted voltage to the input voltage. In this case, it is,

$$B = \frac{Vo}{Vin} \qquad \text{Equation 1}$$

This demonstrates that the boost ratio of this topology is smaller than the buck-boost topology (described in AN60142).

For a V_{in} of 24V, and V_{out} = 31V,

You get,

B = (31)/24 = 1.29.

2. Duty Cycle

The duty cycle with which the FET is switched, decides the output voltage. Since the PWM signal gates the switching operation, the duty cycle of it is determined as follows.

$$D = 1 - \frac{Vin}{Vo} \qquad \text{Equation 2}$$

This is the standard duty cycle equation for a boost topology. However, for the system to operate as intended, the PWM must be operated at a duty cycle greater than this value 'D' so that the capacitor voltage (load voltage) increases gradually. This increase in load voltage causes the current to increase, which then allows the system to regulate it. The highest duty cycle occurs at the lowest input voltage (including input variation) and the obtained value is used in the final firmware to run the PWM.

For example, with V_{in} of 24V, V_{out} of 31V, the duty cycle is 1-(24/31) which equals to 0.23. For example, a PWM with 6-bit resolution (period value of 63) can have a pulse width of 19-22 that translates to a D of 0.3-0.35.

3. Resolution of Modulator (R)

The modulator in this topology is used to run the boost function by switching the FET at a constant frequency and duty cycle. It is constantly running and is used to gradually increase the energy built up in the inductor and there by the boost voltage. The key here is to select the resolution (R in bit count) such that the change in current through the inductor during the 'ON' time and 'OFF' time is low. In general, a change in current less than 100 mA is acceptable. Large oscillations of current are not good for the system in terms of noise/EMI and make it difficult to select the component ratings.

Now,

$$Fout = \frac{Fin}{2^R}$$

$$Tout = \frac{1}{Fout}$$

$$Ton = D \times Tout$$

$$Toff = (1 - D) \times Tout \qquad \text{Equation 3}$$

Note: The 'D' mentioned in the equations must be the actual value of duty cycle used.

With F_{in} = 48 MHz, a resolution R of 6 bits yields,

Fout = 750 KHz.

The Duty Cycle of 0.3 (used in the previous example) sets T_{on} to be 0.4 uS and T_{off} to be 0.9 uS.

With a V_{in} of 24V, V_{out} of 31V, the change in current during the on-time is 102 mA and change in current during the off-time is 69 mA.

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According to the equations,

$$di(ON) = Vin \times T(ON) / L \quad \text{Equation 4}$$

$$di(OFF) = (Vout - Vin) \times T(OFF) / L \quad \text{Equation 5}$$

Making the resolution higher than 6 bits, lowers the frequency and increases T_{on} and T_{off}.

4. I_o(peak)

This is the peak of the load current as decided by the reference set on the upper DAC in the hysteretic controller

$$Io(peak) = Io + (\frac{Ru}{100} \times Io) \quad \text{Equation 6}$$

Where, Ru is the upper ripple in percentage. With Io = 0.7A, and Ru = 7%, Io (peak0) = 0.75A.

5. I_o(valley)

This is the lower limit for the load current as decided by the reference set on the lower DAC in the hysteretic controller.

Note: This is usually also greater than the desired average current Io because, after the hysteretic controller is turned ON (subsequent to hitting the lower threshold), the capacitor continues to discharge while the inductor charges up enough to transfer sufficient energy to charge up the capacitor voltage. Therefore, by allowing the hysteretic controller to turn ON at a point higher than the average value, there is some margin (while the current continues to reduce) before it starts to rise again. This ensures the average current is not lower than what it should be.

$$Io(valley) = Io + (\frac{Rl}{100} \times Io) \quad \text{Equation 7}$$

Where, Rl is the lower ripple in percentage.

For example, with Io at 0.7A and Rl = 3%,

Io(valley) = 0.721A.

6. I_{in}(peak)

This is the maximum value of the inductor current that is reached, before the hysteretic controller is turned OFF (due to hitting the upper DAC threshold).

$$Iin(peak) = \frac{Io(peak) \times B}{\eta} \quad \text{Equation 8}$$

Here, η is the assumed efficiency of the system (pessimistic). The output current peak is scaled by the boost ratio to estimate input current. A typical value to assume for efficiency is 75%.

With I_o(peak) = 0.75A, B = 1.29, and efficiency = 75%, I_{in}(peak) works out to be 1.38A.

7. I_{in}(valley)

This is the lowest value of input current while the system is operating right before the hysteretic controller is turned ON again.

$$Iin(valley) = Iin(peak) - \Delta(Iin) \quad \text{Equation 9}$$

Here, the final current I_{in}(valley) must be above 0A, so that the inductor does not go into discontinuous mode of operation.

For example, with I_{in}(peak) being 1.38A, assuming a $\Delta(I_{in})$ of 1A, I_{in}(valley) = 0.38A. $\Delta(I_{in})$ is chosen such that there is some minimum current flowing through the inductor when the switch comes ON again.

8. V(cap)

This is the final voltage on the capacitor at the end of the period, when the hysteretic controller is OFF and turned ON again.

$$V(cap) = Vo + \Delta(vcap) \quad \text{Equation 10}$$

The amount by which the voltage across the capacitor is increased (Δ(vcap)), is the change in voltage allowed during the period while the hysteretic controller is OFF.

To keep the voltage across the capacitor more or less constant, Δ(vcap) is chosen to be 70 mV. This makes V_{cap} = 31 + 0.07 = 31.07V.

Circuit Component values

9. C – Load Capacitor Value

The equation to determine the capacitor value needed for the circuit comes from the basic capacitor equation,

$$i \times t = C \times V \quad \text{Equation 11}$$

Here,

i – The average current through the load.

t – Time period during which the capacitor is required to supply the current i at the load voltage.

V – Output voltage change during the time period t.

Now, the switching time period is given by,

$$Tout = \frac{1}{Fout} \quad \text{Equation 12}$$

The time period during which the capacitor is required to supply the load current is the time during which the switch is ON. This is given by,

$$t = D \times Tout \Rightarrow t = \frac{D}{Fout} \quad \text{Equation 13}$$

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During this time period, the voltage on the capacitor changes by a certain amount and you call this, V_o(ripple).

Therefore,

$$i \times t = C \times V \Rightarrow C = \frac{i \times t}{V} \Rightarrow C = \frac{Io \times D}{Fout \times Vo(ripple)}$$

Equation 14

The duty cycle D, output frequency F_{out} and I_o are determined as shown previously. This leaves V_o(ripple) as a selectable value to determine C.
Using an example of 4 mV for V_o(ripple), D of 0.23, F_{out} of 750 KHz, and I_o of 700 mA, you get, C of 52.69 uF. The closest standard value is used which is 44 uF (using two 22 uF capacitors). Using a smaller capacitor has the effect of allowing a larger ripple. Usually, this is not a major difference as long as the closest practical capacitance value is chosen.

10. L – Inductance Value

The inductor is the other energy storage element. The inductor captures energy from the input at a certain voltage and current and transfers it to the output which is at a different voltage, making it the component of choice in many kinds of switching circuits used to transfer energy.

From the section Circuit Operation on page 2 and points Duty Cycle and Resolution of Modulator (R) on page 3 of this note, the FET is turned ON and OFF at a duty cycle greater than what is required to boost the voltage. Therefore, the increase in current through the inductor during T_{on} is greater than the decrease in current during T_{off}. This means the current through the inductor is gradually increasing. This also causes the load current to increase constantly. .

Figure 4. Screen Capture of Boost Circuit in Operation



Figure 4 shows the operation of the circuit captured from a real system. The green waveform at the top is the inductor current. The magenta signal at the bottom is the load current. The yellow signal is the FET gate drive signal. The blue signal is the input voltage.

When the load current hits the upper threshold of the hysteretic controller, the controller turns OFF which means the inductor is now continuously in the discharge cycle (FET is OFF).

During this period, the inductor is transferring its energy primarily into the bulk capacitor and some to the load. This transfer of energy into the capacitor causes its voltage to increase. The amount by which the capacitor voltage increases during this period is called Δ(vcap).

Therefore, repeating the V_{cap} equation on page 4 here,

$$V(cap) = Vo + \Delta(vcap)$$

Equation 15

V_{cap} denotes the final voltage on the capacitor. If the energy used to drive the load current is ignored (since the inductor current is significantly larger than load current) to make it simpler, the energy discharged by the inductor during the hysteretic controller's OFF time is the energy gained by the capacitor.

Energy stored in inductor is,

$$E_L = \frac{L \times i^2}{2}$$

Equation 16

And, energy stored in a capacitor is,

$$E_C = \frac{C \times V^2}{2}$$

Equation 17

Now, equating the change in energy in the inductor to that of the capacitor, you get,

$$\frac{L \times Iin(peak)^2}{2} - \frac{L \times Iin(valley)^2}{2} = \frac{C \times V(cap)^2}{2} - \frac{C \times Vo^2}{2}$$

Equation 18

Rearranging this equation to denote L in terms of everything else,

$$L = C \times \frac{V(cap)^2 - Vo^2}{Iin(peak)^2 - Iin(valley)^2}$$

Equation 19

Using the calculated value of C (52.69 uF), the inductance value becomes 129.76 uH. On a real board, a 47 uH and a 68 uH inductor are connected in series to achieve 115 uH which is the closest value to the required inductance. Choosing an inductor value lower than the calculated, is acceptable, if the actual capacitance value chosen is also lower than the calculated value.

Special Notes

From the equations for capacitor and inductor in section C – Load Capacitor Value on page 4 and L – Inductance Value respectively, increasing V_o(ripple) decreases the capacitance needed. A lower capacitance value also results in a lower inductance value.

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This leads to the thought that, one could make the V_o(ripple) as large as possible to have lower capacitance and inductance values. There are two ways in which this can create problems for you.

- Increasing the allowed ripple beyond a certain point causes large oscillations in the output (load) voltage which LEDs are sensitive to. For instance, if the required forward voltage for a certain drive current is not available, the drive current has to decrease which misses the point of this exercise.
- When the inductor value decreases, the following is the implication using the equation,

$$V_L = L \, di/dt \Rightarrow \frac{di}{dt} = \frac{V_L}{L}$$ Equation 20

From this equation, when the inductance value decreases, the rate of change of current through the inductor increases. For a given modulator resolution and frequency, during T_{on} and T_{off} (calculated in section Resolution of Modulator (R) on page 3) the change in current is larger.

From the fact that dt is constant, di has to therefore increase, for increasing the di/dt, for the corresponding decrease in inductance. To counter this, the modulator resolution can be reduced further, (to increase output frequency) but, this results in poor control of the duty cycle.

To summarize, while attempting to increase V_o(ripple) in the quest to decrease the C and L values, the change in current must be calculated. If this change is larger than approximately 100-150 mA (as a thumb rule) for a time period, the ripple should be reduced to increase the C and L values.

Ultimately, the tolerance to the oscillations in current through the inductor is your choice but, having large current oscillations results in two undesirable results.

1. Increased noise and EMI
2. Potentially higher saturation current ratings for the inductor increasing its package size – which ultimately defeats the purpose of trying to reduce the inductance size.

Component Selection

In a power system, there is more to component selection than determining its electrical value. For example, an inductor needs to have a certain saturation current rating or a capacitor needs to have a certain voltage rating.

There are five external components apart from the load.

Sense Resistor

Value: The sense resistor is in the path of the load current. The value needs to be chosen such that the current flowing through it (load current) produces a voltage across it approximately in the range of 100 mV. This translates to a CSA output of 2.0V (CSA gain is 20). If there are a range of currents, it is a good practice to size the sense resistor so that the differential voltage is between 30 and 100 mV.

Package: The resistor has to be able to dissipate the power generated by the current flowing through it. $P = I^2 \times R$. Usually, packages such as 1206, 1210, 2010 or 2512 suit the power requirements. The power rating should be higher than the expected power dissipation.

Inductor

Value: The equation under section L – Inductance Value on page 5 generates an inductor value. Determine the closest standard value available and use that as shown in the example.

Saturation Current Rating: As inductors saturate, their inductance value decreases. They are usually rated at a certain percentage drop in inductance such as 20-30% at a particular current (I_{sat}). The value calculated as I_{in}(peak) is a deciding factor. The saturation current rating of the chosen inductor should approximately be 1.5 to 2 times the value of I_{in}(peak). This is to have a safe margin and to account for the fact that inductor current is high at startup.

DCR: The equivalent DC resistance of the inductor plays a role in the power loss when current flows through it. This should be as low as possible to increase efficiency.

MOSFET (Switch)

VDS(max): The maximum drain to source voltage rating is the maximum voltage that the MOSFET can block when it is OFF without breaking down. In the boost circuit, the voltage at the drain node when the switch is OFF is (V_{out} + Vf(diode)). There is usually also a 15-20% overshoot when the MOSFET turns OFF and the diode turns ON. The selected MOSFET must have a VDS(max) rating of at least 1.5 times the expected voltage on the drain.

If(max): The current flowing through the MOSFET when it is ON is the current flowing through the inductor, and its maximum value is calculated with the equation in section Iin(peak). As mentioned earlier, the inductor current at startup is usually higher than this by at least 50-100%. Therefore, the selected MOSFET's current rating must be at least twice the expected value.

RDS(on): Every MOSFET has some ON resistance when it is in saturation mode and conducting mode. The selected MOSFET should have a low RDS(on) so that, the power loss through the MOSFET is reduced. This is important since the MOSFET is switching in the range of 100s of KHz and the power loss through the FET is directly proportional to the frequency of switching.

Diode

Schottky diodes are preferable for this since they have low Vf and low reverse recovery times.

Reverse Voltage (peak): When the MOSFET is ON, this diode is required to block the voltage at the capacitor (with respect to ground). This is given by V_{out}. Therefore, the reverse voltage rating of the selected diode should be at least 1.5 to 2 times higher to allow some variation in input and output.

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Average Rectified Forward Current: The current that flows through the diode when it is ON is the current through the inductor. This is generally given by I_{in}(peak) but the startup current is higher by 50-100%. The selected diode must have a forward current rating of at least twice of the maximum inductor current.

Forward Voltage: The chosen diode should also have the lowest possible forward voltage. This is to ensure reduction in power loss through the diode.

$$P = V_F \times I_F \times (1 - D)$$ Equation 21

Load Capacitor

Voltage Rating: The capacitor is expected to work at the load voltage. Therefore, its voltage rating should be at least 1.5 times of the maximum expected load voltage.

Type: Usually, electrolytic capacitors are acceptable for this application and are cheaper than ceramic equivalents.

The Boost 'Glow'

The boost topology comes with a possibly undesirable aspect. This specially occurs when the input and output voltage do not differ significantly from each other. In quantitative terms, if the input voltage is sufficient to provide a forward voltage drop (across the entire string) at a drive current that can result in noticeable illumination from the LEDs, then this 'glow' occurs. For example, a flow of current between 5-10 mA through the LEDs causes an illumination of less than 10% of the rated luminosity. However, the capability of the human eye to be able to detect very small light levels in dark environments will make this visible. This can be an undesirable effect in a dark environment like a movie hall or theater.

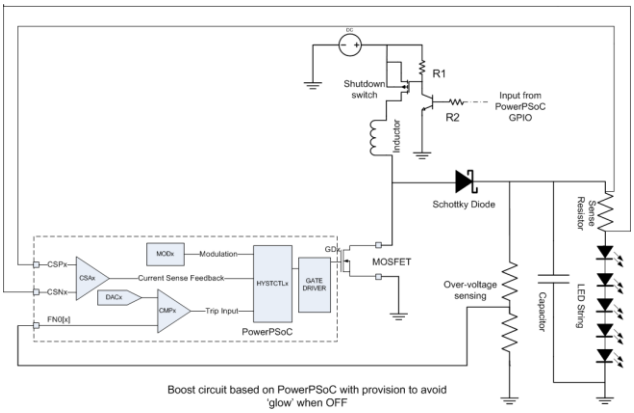
In a situation when the system is to remain OFF, but with the input power supply present, the LEDs could 'glow' at low intensity. Although the system is not actively boosting the input to the output (switch is permanently OFF), the fact that there is a diode in the path between the input and output causes this condition. The diode gets forward biased when the capacitor is discharged or its voltage is lower than the input by the diode forward voltage (V_f). This causes current from the input supply to flow into the capacitor through the inductor and diode until the capacitor voltage rises sufficiently to turn the diode OFF.

At this point, the capacitor is charged up to a voltage lower than V_{in} (V_{in}-V_f). This causes a current to flow through the LEDs at a forward voltage through them that is in accordance with their forward characteristics. For example, in a 24V input system and a load of 8 LEDs, if the capacitor voltage is (24-0.7) 23.3V, it results in a drop of 2.9V across each LED. This is sufficient for the LEDs to glow, as they allow sufficient current to flow through them.

Solution

One way to solve this issue is to place an additional switch in the input path, such that it is turned OFF when the system is not operating.

Figure 5. Boost Circuit Showing P-FET to Overcome Glow



The circuit shown is a repetition of Figure 1 but with an extra MOSFET in the path of the input current. This is a P Channel MOSFET so that, it is easier to turn it ON/OFF by referencing the source to supply voltage. The drive circuit to turn this MOSFET ON or OFF is achieved using a NPN bipolar transistor and 2 resistors. The base of the bipolar transistor is driven by a General purpose I/O pin (GPIO) from PowerPSoC.

When the output of the pin is high, the current flows into the base and turns it ON. This pulls the gate of the P-MOSFET to ground, thereby turning it ON. As a result the boost circuit is now connected to the power supply. When the signal at the GPIO goes low, the vice versa happens and the P-MOSFET gets turned OFF. This essentially isolates the boost circuit from the power supply. The load capacitor discharges all its energy into the load and subsequently does not get charged up since there is no energy source to do so.

In firmware, the behavior should be such that when the LEDs are supposed to be turned OFF with the presence of system power, the GPIO driving the bipolar transistor has its output configured low.

Note: However, this must be done after turning the hysteretic controller OFF. When the system is to be turned ON, the GPIO signal must be made high first, and then the hysteretic controller has to be turned ON subsequently. This is to allow the capacitor to charge up first and then start the switching circuit.

PROOF OF PERFECT

Component Selection

MOSFET

This is a P-Channel MOSFET so that, it can be referenced to power supply and conveniently turned ON/OFF.

VDS(max) - If it is turned OFF, the MOSFET blocks the entire input supply voltage. Therefore, the VDS(max) rating of it is at least 1.5 to 2 times higher than the input voltage.

RDS(on) - The entire input current flows through this MOSFET when the system is operating. Considering that the input current is high in boost system, the power loss through this FET ($P=I^2R$) is important. The MOSFET should have a low RDS(on) as possible.

If(max) - The maximum forward current rating of the MOSFET should be higher than the expected maximum input current.

Example Part Number - NTP2955G (60V, 12A PMOS)

BJT

A standard small signal NPN bipolar junction transistor can be used for this application.

I_c(max) - The collector current rating can be in the order of 100 mA or less. The current through this transistor and the resistor should not exceed 5-10 mA to control the power loss in this circuit.

V_{CEO} - The transistor must have the ability to sustain the input supply across its collector and emitter. Therefore, the maximum collector-emitter voltage has to be higher than the expected input supply voltage.

Example Part Number - BC547BTA (45V, 100 mA).

Resistors

R1 is connected between collector of NPN transistor and HV supply. The aim is to dissipate minimal power in this path because there is a continuous flow of current when the system is ON. If a 10K resistor is selected, the current through it when the transistor is on is Vin/10K. For a Vin of 25V, the current is 2.5mA. The power dissipated in this resistor is then given by

$$P = I^2R = 2.5^2 \times 10K = 62.5mW$$ Equation 22

This is acceptable since it is a small fraction of the total output power. The 0603 package for this resistor is sufficient.

R2 is on the base of the NPN transistor (connected to GPIO). After selecting R1, look up the h_{fe} for the NPN transistor from its datasheet. This is the gain value of the transistor.

For the selected part, minimum h_{fe} is 110. A factor of 1.3 is used to overestimate the base current to some extent, to ensure that the NPN definitely turns ON when it is attempted.

$$I_{base} = (I_{collector} / h_{fe}) \times 1.3 = (2.5mA/110) \times 1.3 = 30uA$$

Equation 23

$$R2 = 5V / I_{base} = 5V/30uA = 167Kohms$$

Equation 24

Therefore, the closest standard value resistor in a 0603 package can be used.

Firmware Design

The main aspect about firmware design for this boost topology is the configuration of the user modules in a safe operating state.

Potential dangerous conditions that the firmware can help protect against are,

- Continuous switching of MOSFET and turning it ON without any control could result in constant increase in load voltage and hence the load current. This can also cause increase in inductor current beyond its saturation value.
- Open circuit of load due to damage to load or loose connector can cause rapid buildup of very high voltage on the capacitor. This crosses the absolute maximum ratings of the Current Sense Amplifier pins and result in permanent damage.

The following simplified flow diagram illustrates the order and list of things to configure in firmware. This application note assumes that you are familiar with the PSoC Designer environment which is the IDE, used to configure, write firmware for and program the PowerPSoC device. For an introduction to PSoC Designer, refer to the On-Demand training on the web.

PSoC Designer and PSoC Programmer can be downloaded from the web.

Refer to the application note AN51012 – Firmware Design guidelines for PowerPSoC for a detailed description on configuring PowerPSoC using PSoC Designer however, it describes a floating load buck circuit.

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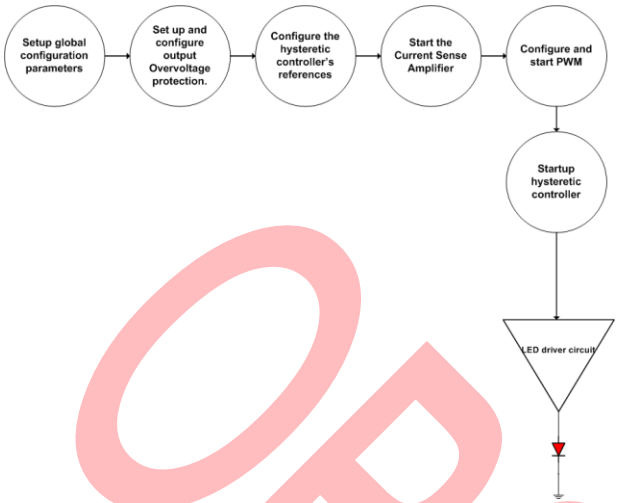
Figure 6. Firmware Flow Diagram



1. The device is first configured using the 'chip view' which enables global configuration of the device, picking and placing pre-defined user modules, connecting them as desired and configuring them.

   Figure 7 on page 9 shows the snapshot of the global resources tab in the chip view that is suitable for this project.

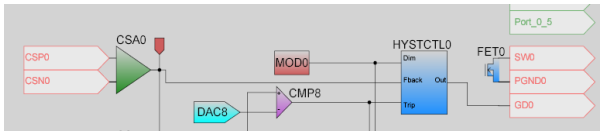
   Figure 7. Global Resources Configuration

Global Resources - buck_boost_basic

Power Setting [Vcc / S	5.0V / 24MHz
CPU_Clock	SysClk/1
Sleep_Timer	512_Hz
VC1= SysClk/N	12
VC2= VC1/N	16
VC3 Source	VC2
VC3 Divider	256
SysClk Source	Internal
SysClk*2 Disable	No
Analog Power	SC On/Ref Low
Ref Mux	(Vdd/2)+/-(Vdd/2)
Op-Amp Bias	Low
A_Buff_Power	Low
Trip Voltage [LVD]	4.81V
LVDThrottleBack	Disable
AINX Connection	CSA0
AINX Mode	IREF
MOD Clock	SysClk*2
Bias Generator	Enable
Switching Regulator	Enable

The following figure shows the snapshot of the chip view of the user modules that are placed and connected to each other.

Figure 8. Chip View of Placed User Modules



- The Current Sense Amplifier CSA0's output is the feedback to the hysteretic controller.
- MOD0's output (PWM) feeds the modulator input to the hysteretic controller.
- CMP8 is the hardware trip comparator whose output forms the trip input to the hysteretic controller. This comparator is responsible for turning the system off in case of over voltage.
- CMP8's reference on its negative input is supplied by DAC8 and its other input comes from pin FN_0_1 which carries the load voltage signal on it.
- Refer to the attached PSoC Designer project for a reference on the properties of each module.

2. After the modules are connected and their properties defined, generate the project using the 'generate' option from the build menu.
3. In the *main.c* file, the following is the order of code.

- The digital code for DAC8 (that supplies the reference to CMP8) is written using an API. The module is then started, followed by the trip comparator CMP8. This in effect sets up the protection feature first.
- The hysteretic controller's DAC voltage range is setup and the digital codes for the 2 DACs are configured. These two represent the high and low level of the load current.
- The Current Sense amplifier is then started. Note that this module **must** be started before the hysteretic controller, since it is the feedback element.
- The modulator (PWM) is configured (period and pulse width) and subsequently started. The period is set according to the desired output frequency and resolution of the PWM. Refer to the equations described earlier in this note on how to decide these values. The pulse width is initially set to 0. There is a loop later in the firmware to soft-start the PWM. If the PWM is started directly with its final pulse width value, the current in the inductor rises to very large levels rapidly. In the first few periods of switching as soon as the system is turned ON, the load voltage is very close to 0. This ensures that the inductor hardly discharges its energy in the time that the switch remains OFF (since the energy discharge depends on the voltage).
- The hysteretic controller (which controls the switch) is now started after all other modules are started.
- A loop starting with the starting pulse width to the final pulse width is run in which:
  - ❑ The PWM's pulse width is set to the current value of the loop.
  - ❑ A delay is executed to let the PWM run at that pulse width for that delay.

At the end of this, for basic boost functionality, the program runs in an infinite loop. The hardware controls itself.

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Additional Firmware Options

Although the general rule in a boost system is that the input voltage is always lower than the output, slight variation in the input voltage can occur depending on the source of power. Additionally, because of tolerances in the load capacitor, it can charge to slightly different voltages and drive different current into the load.

In cases where the load current needs to be controlled tightly, an Analog-to-Digital (ADC) converter can be configured inside the device to have a closed loop feedback system to drive the desired current through the load.

As shown in the example project attached, a simple incremental ADC can be placed. Its positive input is setup to be connected to the Analog Input Multiplexer (AINX) Multiplexer. This multiplexer's output can be any of the four Current Sense Amplifiers in the device and is setup in the global resources menu shown in Figure 7.

The ADC is setup as an 8-bit output. In the code, the ADC is initialized and started to sample continuously. This initialization is not critical to the operation and safety of the circuit and can be performed anywhere in the process described earlier.

In the infinite while loop, at the end of all the initializations, the program execution waits for the next ADC sample. This is stored in a temporary variable and the ADC proceeds to gather the next set of samples. As shown in the project, an average of a certain number of samples can be performed to filter out short-term fluctuations.

If this final result (average of the current measured over a period) is away from the desired load current by more than the accepted tolerance, the DAC references of the hysteretic controller are changed.

- If the current is to be increased, the upper reference should be increased first followed by the lower reference.
- If the current is to be decreased, the lower reference should be decreased first followed by the upper reference.

Note: Although the attached project implements an ADC to measure the load current, it does not implement any function based on the measured value. It is left to you to implement this part based on the desired behavior.

To ensure a gradual movement of current, it is recommended to change the references' (for the hysteretic controllers) one value at a time.

To enable a convenient method to monitor the measurement of the ADC real time, an EzI^{2}C user module (that is an I^{2}C slave) is also configured in the firmware project. This can be used in conjunction with the CY3240 I^{2}C-USB bridge to watch the graphical movement of the ADC output on a PC using the GUI that comes with the kit.

Other Considerations

In a high power system like this circuit is bound to be used in, the PCB layout is of prime importance. Some of the important aspects to take care of are,

- Kelvin and differential connections for the sense resistor (that feeds the load current back to the controller).
- Short loops for de-coupling capacitors connected to the gate drive VDD pins on the device.
- Short loops between the gate driver on the controller and the MOSFET (if an external one is used).
- Use of a 4-layer board to enable good power and ground connections.

For detailed recommendations on layout, follow the application note AN52209 – PCB Guidelines for PowerPSoC as a LED Driver.

Summary

This application note and the firmware presented with it provide sufficient information on implementing a boost constant current regulator using PowerPSoC. However, like in many power systems, the final circuit might require minor modifications in component values or firmware configuration for PWM pulse width or the current thresholds, to perform exactly to the expectations.

PowerPSoC presents a powerful new standard of designing high power systems together with intelligence using software tools. The combination of the well established PSoC core along with high performance power electronics enables highly integrated, low cost, small designs that differentiate products using it from ones that use conventional methodologies.

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2931721	UKK	05/13/10	New Application Note.
*A	3152084	MKKU	03/19/2013	Obsolete spec.

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