AN6076

# Differences between EZ-USB® FX2LP™ and MoBL-USB™ FX2LP18

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**Software Version: NA**

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This application note explains the differences between the EZ-USB® FX2LP™ (CY7C68013A/14A/15A/16A) and MoBL-USB™ FX2LP18 (CY7C68053) USB Microcontroller. This application note will be useful to engineers experienced with EZ-USB FX2LP who are switching to the MoBL-USB FX2LP18, as well as engineers starting off with the MoBL-USB FX2LP18.

## Introduction

This application note explains the major differences between the EZ-USB FX2LP™ and the MoBL-USB™ FX2LP18 from the perspective of a user. In summary:

- The MoBL-USB FX2LP18 has a variable I/O voltage (1.8 V–3.3 V). The EZ-USB FX2LP has fixed I/O voltage at 3.3 V.
- The MoBL-USB FX2LP18 comes out of reset with the DISCON bit of the USBCS register set to 1. Hence, it is effectively disconnected from the USB bus and requires firmware to connect it to the USB bus. Consequently, it supports only C2 boot load from an EEPROM or a processor emulating an I2C™ slave.
- The EZ-USB FX2LP by default has the DISCON bit cleared. Hence, it comes out of reset connected to the USB bus. Therefore, it also supports both C0 boot load and No EEPROM boot load.
- The EZ-USB FX2LP is available in a 128-pin package that exposes the address and data bus of the 8051. Hence this package can support memory-mapped external peripherals such as FLASH, RAM, and others.
- The MoBL-USB FX2LP18 is not available in the 128-pin package; hence, there is no option of connecting an external memory-mapped peripheral.
- The EZ-USB FX2LP is available in a 100-pin package, which offers additional 8-bit ports (Ports C and E) and two UARTs over the 56-pin package. Since the MoBL-USB FX2LP18 is available only in a 56-pin package, it does not have these available externally.
- Four timing parameters are different between the EZ-USB FX2LP and the MoBL-USB FX2LP18.

To keep the suspend current as low as possible when working with the MoBL-USB FX2LP18, more caution needs to be taken with regard to floating IO pins. The differences listed above are elaborated in this application note.

## Operating Voltage

In the MoBL-USB FX2LP18 part, the core operates at 1.8 V, the PHY and the oscillator operate at 3.3 V, and the I/O domain can be powered up from 1.8 V up to 3.3 V. This makes this part ideal for applications such as cellular phones, Smart phones, PDAs, MP3 players, and others.

The EZ-USB FX2LP core operates at 1.8 V from an internal regulator, the PHY and the oscillator operate at 3.3 V, and the I/O voltage is fixed at 3.3 V. For specific parameters, refer to the datasheet.

## Boot-up Differences

The EZ-USB FX2LP supports different methods of boot load including the C0 Load, C2 Load, and No EEPROM boot load. The MoBL-USB FX2LP18 supports only the C2 boot load.

During the power-up sequence, internal logic of the MoBL-USB FX2LP18 checks the $I^2C$ port for the connection of an EEPROM whose first byte is 0xC2. If a C2 formatted EEPROM containing firmware is attached to the I2C bus, the firmware is automatically loaded from the EEPROM into the MoBL-USB FX2LP18's on-chip RAM, and then the CPU is taken out of reset to execute this boot-loaded code. In this case, the VID/PID/DID values are encapsulated in the firmware; the RENUM bit is automatically set to '1' to indicate that the firmware, not the Default USB Device, handles device requests from the host PC. The EEPROM must contain the value 0xC2 in its first byte to indicate this mode to MoBL-USB FX2LP18, so this mode is called a 'C2 Load'.

**Note** Although the MoBL-USB FX2LP18 can perform C2 Loads from EEPROMs as large as 64 KB, code can only be downloaded to the 16 K of on-chip RAM. It is important to EEPROMs as large as 64 KB, code can only be downloaded to the 16 K of on-chip RAM. It is important to note that the MoBL-USB FX2LP18 comes out of reset with the DISCON bit set. This means that the device is effectively disconnected from the USB bus. Firmware is required to connect to USB, so the device will not enumerate without an EEPROM (a C2 Load) to download firmware that at least connects the device to USB. If no EEPROM is present on the $I^2C$ port, an external processor must emulate an $I^2C$ slave. The MoBL-USB FX2LP18 does not enumerate using internally stored descriptors (for example, Cypress's VID/PID/DID is not used for enumeration). It is still possible to download firmware over the USB bus once the initial C2 Load from EEPROM occurs. In this case, the firmware loaded from the EEPROM can be as simple as a one line code to clear the DISCON bit and RENUM bit in the USBCS register. This will connect the device to USB and indicate that the Default USB Device will handle USB requests.

The EZ-USB FX2LP chip comes out of reset connected to the USB bus, so a C0 boot load or a No EEPROM boot load is permitted (generally used for development purposes or applications that need to download firmware from the PC).

For the EZ-USB FX2LP, it is recommended that 2.2 K pull-up resistors be connected to the SCL and SDA lines even if no EEPROM is connected to the I2C port.

For the MoBL-USB FX2LP18, the value of the pull-up resistors required may vary, depending on the combination of VCC_IO and the supply used for the EEPROM. The pull-up resistors used must be such that when the EEPROM pulls SDA low, the voltage level meets the VIL specification of the FX2LP18. For example, if the EEPROM runs off a 3.3 V supply and VCC_IO is 1.8 V, the recommended pull-up resistors are 10 kW resistors. This requirement may also vary depending on the devices being run on the $I^2C$ pins. Refer to the $I^2C$ specifications for details.

## Differences due to Package Options

The EZ-USB FX2LP is available in a 56-pin, 100-pin or 128-pin package. The MoBL-USB FX2LP18 is currently available only in a 56-pin package. So all the additional features offered on the EZ-USB FX2LP 100-pin and 128-pin parts are not available on the MoBL-USB FX2LP18. These are detailed in the following section.

## Features not available on MoBL-USB FX2LP18

**Note** The following features on the 100-pin/128-pin EZ-USB FX2LP are not available on MoBL-USB FX2LP18.

The 100-pin and 128-pin EZ-USB FX2LP provide two additional 8-bit ports that the 56-pin part does not provide. These are Port C and Port E. Port C can be used as either GPIOs or as GPIF address lines when the part is in GPIF mode. Port E can be used as either GPIOs or as interrupts.

The 100-pin and 128-pin EZ-USB FX2LP also provide two UARTs, Serial I/O 0, and Serial I/O 1. These extra GPIOs and UARTs are not available on the MoBL-USB FX2LP18.

The 128-pin EZ-USB FX2LP also brings out the address and data bus of the 8051. This enables the option of connecting a memory-mapped peripheral like FLASH, EPROM, external RAM, and others.

If a Flash, EPROM, or other memory is attached to the EZ-USB FX2LP's address/data bus (128-pin package only) and a properly formatted EEPROM is not present, and the EA pin is tied high (indicating that the EZ-USB FX2LP starts code execution at 0x0000 from off-chip memory), the EZ-USB FX2LP begins executing firmware from the off-chip memory. In this case, the VID/PID/DID values are encapsulated in the firmware; the RENUM bit is automatically set to 1 to indicate that the firmware, not internal EZ-USB FX2LP logic, handles device requests. The MoBL-USB FX2LP18 does not allow this, as it does not bring out the address and data bus of the 8051.

This also affects the recommended value of 'stretch' explained as follows:

The EZ-USB FX2LP can execute a MOVX instruction in as few as two instruction cycles. However, it is sometimes desirable to stretch this value (for example to access slow memory or slow memory-mapped peripherals such as USARTs or LCDs). The EZ-USB FX2LP's 'stretch memory cycle' feature enables EZ-USB FX2LP firmware to adjust the speed of data memory accesses (program-memory code fetches are not affected). Since the MoBL-USB FX2LP18 cannot support memory-mapped external peripherals, stretch does not apply. Hence it is recommended that programmers set this to 0.

## Differences in Timing Parameters

Four timing parameters are different between the EZ-USB FX2LP and MoBL-USB FX2LP18. These are listed in Table 1.

Table 1. Timing Parameters

| Parameter | EZ-USB FX2LP™ | MoBL-USB™ FX2LP18 |
|---|---|---|
| GPIF Synchronous Signals with Externally Sourced IFCLK - $t_{XCTL}$ (Clock to CTL Output Propagation Delay) | 10.7 ns (max) | 13.06 ns (max) |
| Slave FIFO Synchronous Read with Externally Sourced IFCLK - $t_{XFD}$ (Clock to FIFO Data Output Propagation Delay) | 15 ns (max) | 17.31 ns (max) |
| Slave FIFO Synchronous Write with Internally Sourced IFCLK – $t_{SFD}$ (FIFO Data to Clock Set-up) | 9.2 ns (min) | 10.64 ns (min) |
| Slave FIFO Synchronous Packet End Strobe with Externally Sourced IFCLK - $t_{PEH}$ (Clock to PKTEND Hold) | 2.5 ns (min) | 3.04 ns (min) |

## Lowering Suspend Current

Good design practices for CMOS circuits dictate that any unused input pins must not be floating between VIL and VIH. Floating input pins will not damage the chip, but can substantially increase suspend current. To achieve the lowest suspend current, any unused port pins must be configured as outputs. Any unused input pins must be tied to ground. Some examples of pins that need attention during suspend are:

- Port pins. For Port A, B, D pins, extra care must be taken in shared bus situations.
- Completely unused pins must be pulled to VCC_IO or GND.
- In a single-master system, the firmware must output enable all the port pins and drive them high or low, before FX2LP18 enters the suspend state.
- In a multi-master system (FX2LP18 and another processor sharing a common data bus), when FX2LP18 is suspended, the external master must drive the pins high or low. The external master may not let the pins float.
- CLKOUT. If CLKOUT is not used, it must be tri-stated during normal operation, but driven during suspend.
- IFCLK, RDY0, RDY1. These pins must be pulled to VCC_IO or GND or driven by another chip.
- CTL0-2. If tri-stated via GPIFIDLECTL, these pins must be pulled to VCC_IO or GND or driven by another chip.
- RESET#, WAKEUP#. These pins must be pulled to VCC_IO or GND or driven by another chip during suspend.

These recommendations should be adhered to for both the EZ-USB FX2LP and the MoBL-USB FX2LP18. However, the MoBL-USB FX2LP18 is less tolerant of violations of the above.

## Summary

MoBL-USB FX2LP18 is similar to EZ-USB FX2LP, specifically designed to support lower I/O voltages. Engineers who have experience with the EZ-USB FX2LP will find MoBL-USB FX2LP18 familiar and easy to work with. MoBL-USB FX2LP18 is an excellent solution for high speed USB on mobile devices.

## Additional Resources

For more information on EZ-USB and MoBL-USB, refer to the following documents available at Cypress website:

- EZ-USB® TRM
- MoBL-USB™ FX2LP18 TRM
- CY3684 EZ-USB® Development Kit
- CY3687 MoBL-USB™ FX2LP18 Development Kit
- MoBL-USB™ Bridge Reference Design

## Document History

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| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
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| ** | 1408704 | EYB | 08/18/2008 | Obtain Spec# for note to be added to Spec system.<br>This note had no technical updates. |
| *A | 3126395 | RSKV | 01/03/2011 | Added Additional Resources. |
| *B | 3342498 | RSKV | 08/11/2011 | No technical updates.<br>Completing Sunset Review. |
| *C | 4485830 | AKSL | 08/27/2014 | Updated in new template.<br>Completing Sunset Review. |
| *D | 5790547 | AESATMP9 | 06/29/2017 | Updated logo and copyright. |

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