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High Speed Layout Guidelines (LUPA 1300-2)

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Application Note Abstract

This application note discusses the high speed LVDS interface and layout guidelines for the LUPA 1300-2 image sensor. In addition to the specific recommendations for LUPA 1300-2 listed here, users must also consider common high speed layout techniques for achieving high performance and effective PCB design.

Introduction

Designing high speed systems requires fast components and intelligent and careful design. The analog aspect of the devices is as important as the digital. In high speed systems, noise generation is a prime concern. High frequencies can radiate and cause interference. The corresponding fast edge rates can result in ringing, reflection, and crosstalk. If unchecked, this noise seriously degrades system performance.

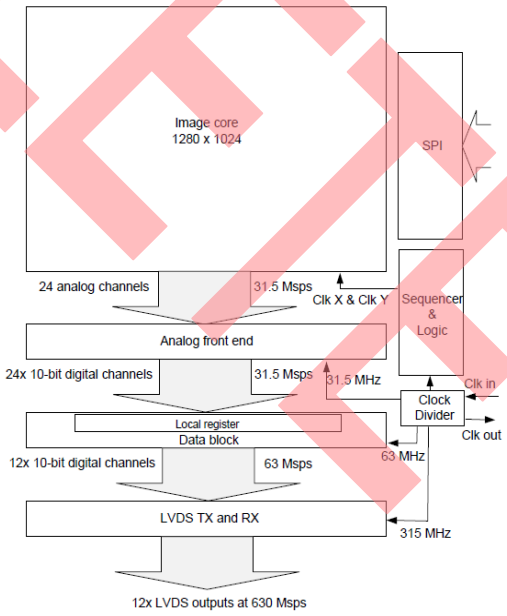
The LUPA 1300-2 is a high speed CMOS image sensor with 1280 by 1024 pixels. The pixels are 14 µm x 14 µm in size and all consist of high sensitivity 6T pipelined snapshot shutter capability (exposure during readout is possible). The key features of this product are:

- **500 FPS:** True snapshot shutter (pipelined and triggered) with fixed pattern noise (FPN) correction, rolling shutter with correlated double sampling (CDS). Frame rate can be boosted by sub sampling and windowing.
- **On-chip FPN Correction:** All modes have FPN correction on-chip. Channel offsets are corrected by an on-chip calibration.
- **High Optical Dynamic Range:** Extended dynamic range is achieved by the multiple slope functionality (up to 90 dB).
- **On Chip Sequencer:** All driving pulses and timings are generated on chip. All sensor functionality can be set by uploading the SPI.
- Randomly programmable region of interest (ROI) readout. Implemented as scanning of lines or columns from an uploaded position.
- Programmable readout in X and Y directions
- **LVDS Outputs:** Low voltage differential signaling (LVDS) outputs reduce on-chip noise, simplify the transport of sensor data over long distances, and simplify overall camera design. The sensor has 12 data channels, Sync, Input clock, and output clock.

LUPA 1300-2 Image Sensor Architecture

The sensor consists of a pixel array, analog front end, data block, and LVDS transmitters and receivers. Separate modules for the SPI, clock division, and sequencer are also integrated. The image sensor of 1280 x 1024 pixels is read out in progressive scan. The analog front end (AFE) prepares the signal for the digital data block where the data is multiplexed and prepared for the LVDS interface.

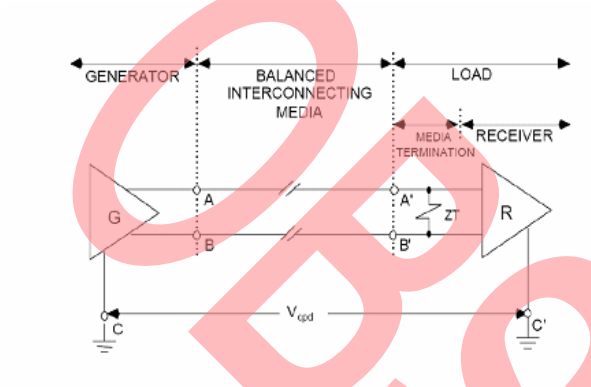
Figure 1 LUPA 1300-2 Architecture



LUPA 1300-2 High Speed LVDS Interface

LUPA 1300-2 uses LVDS I/O. LVDS offers low power and low noise coupling. It also offers low EMI emissions that are essential for the high data readout rates. LVDS voltage swings range from 250 mV to 450 mV with a typical of 350 mV.

Figure 2 LVDS Setup Overview



Because of the low voltage swings, rise and fall times are reduced, enabling higher operating speeds than CMOS, TTL, or other drivers operating at the same slew rate. It uses a common mode voltage ~1.2 to 1.25V above ground, and as a result is more independent of the power supply level and less susceptible to noise. Differential transmission also reduces EMI levels. The 2-pin differential output drives a cable with approximately 100 ohm characteristic impedance, which is “far-end” terminated with 100 ohm.

The driver is designed in compliance with the ANSI/TIA/EIA-644 and IEEE 1596.3 standard.

LVDS outputs consist of a current source (nominal 3.5 mA) that drives the differential pair lines. The basic receiver has a high DC input impedance, so the majority of driver current flows across the 100 ohm termination resistor generating about 350 mV across the receiver inputs. When the driver switches, it changes the direction of current flow across the resistor, thereby creating a valid “one” or “zero” logic state.

The circuit consists of a programmable current sink that defines the drive current, a dynamically controlled current source, a 4-transistor bridge that steers these currents to the differential outputs, and a common mode feedback circuit to balance the sink and source currents.

The LVDS standard defines the drive current between 2.5 to 4.5 mA. The termination resistance is specified from 90 to 132 ohms.

LVDS Data Channels

LUPA 1300-2 has 12 LVDS data output channels operating at a DDR (Double Date Rate) of 630 Mb per second (max) using a 315 MHz input clock. The LVDS data channels have a high speed parallel to serial converter logic function (serializer) that serializes the 63 mega samples per second 10-bit parallel data from a time multiplexed odd and even kernel ADC pair. The high speed serial bit stream drives a LVDS output driver.

The LVDS driver must deliver true and complement signals through a 2-pin differential output to represent a logical 1 and logical 0 states respectively.

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Table 1 LVDS Driver Specifications

Parameter	Description	Specification			Units
		Min	Typ	Max	
Vddlvds	Analog power supply	2.25	2.5	2.75	V
I_{IA} , I_{IB}	Input leakage current			1	µA
I_{IA} - I_{IB}	Input leakage current imbalance	0.1			µA
Z_T	Required termination	90	100	132	Ω
ZC(f)	Characteristic impedance of the interconnect	90		132	Ω
$\|V_{ID}\|$	Differential input	100		600	mV
Power consumption				320	mW
$\| V_T \|$	Differential logic voltage	247	350	454	mV
$\| V_T(1) - V_T(0) \|$	Delta differential voltage			50	mV
V_{OS}	Common mode offset	1.125	1.25	1.375	V
d $\|V_{OS}\|$	Difference in common mode for logic 1 and 0			50	mV
I_{SA}/I_{SB}	Output currents in short to ground condition			10.9	mA
I_{SA}/I_{SB}	Output currents in short to vdd condition			7.6	mA
I_{SAB}	Output current in differential short condition			7.58	mA
I_{OFF}	Off-state current			1.5	µA
$d\|V_{OS}\|$	Dynamic common mode offset	43		141	mVpp
t_{SKD1}	Differential skew			0.25	ns
t_{SKD2}	Differential channel to channel skew			0.5	ns
tSKCD1	Differential clock out to data skew			1	ns
tSKCD2	Differential clock in to data skew			3	ns
*tjit_rms	Random jitter			50	ps
tjit_det	Deterministic jitter – (jitter wrt LUPA 1300-2 input clock)			500	ps
fMAX	Maximum operating frequency			315	MHz
**fMIN	Minimum operating frequency	1			Mhz
tr	Differential rise time	250		600	ps
tf	Differential fall time	250		600	ps
|Vring|	Differential over/undershoot	0		0.13	|V|/VT
fDR	Data rate	250		630	Mbps

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Notes:

***The driver output swing is tuned through the LVDS driver bias current settings in the SPI register. This feature also reduces power consumption. Alternatively, decrease the termination resistor to boost the speed and keep the swing identical by increasing the bias current.

**This is from LVDS point of view, from sensor point of view fMIN is 4 MHz (about 10 fps). At lower speeds dark current and discharge of the storage node starts influencing the image quality.

To enable flexibility in power consumption, the output drive current is programmed through the SPI register interface. Settings are available for operation outside the specified ANSI standard to enable custom settings for power and speed enhancements. These settings may require the use of nonstandard termination resistance. Current drive programming is accomplished using bits 3:0 of SPI register 72 (decimal – LVDS Trim). Table 2 defines the programmable LVDS output current settings.

Table 2 LVDS Driver Programmable Drive Current Settings

reg_lvds_trim[3:0]	I_{out} [mA]	R_T [Ω]	V_{out} [mV]	Comments
0000	1.26	100	126	
0001	1.68	100	168	Low power range
0010	2.1	100	210	
0011	2.52	100	252	
0100	2.94	100	294	
0101	3.36	100	336	Standard range
0110	3.78	100	378	
0111	4.2	100	420	
1000	4.62	72.97	337	
1001	5.04	68.75	347	
1010	5.46	68.75	375	High power range
1011	5.88	68.75	404	
1100	6.3	50	315	
1101	6.72	50	336	
1110	7.14	50	357	
1111	7.56	50	378	

Output trace characteristics affect the performance of the LUPA 1300-2 interface. Use controlled impedance traces to match trace impedance to the transmission medium. The best practice regarding noise coupling and reflections is to run the differential pairs close together, limit skew due to receive end limitations, and for EMI reduction. Matching the differential traces is very important.

LVDS Sync Channel

LUPA 1300-2 includes a LVDS output sync channel to encode sensor synchronization control words such as Start of Frame (SOF), Start of Line (SOL), End of Line (EOL), idle words, and the sensor line address.

The frame related codes are transmitted to reconstruct the full frame format at the receiving end.

This channel includes a “serializer” logic section but receives its input directly from the image core sequencer. An additional synchronization control logic block ensures proper data alignment of the synchronization codes to account for the latency incurred in the other 12 data channels (due to AFE and ADC signal processing). The LVDS output driver is similar to that used in other data channel outputs.

LVDS Clock Output

The LVDS clock output is an additional LVDS output channel that produces a copy of the input clock that is skew matched to the data. The input clock to the sensor is buffered and source aligned with the data channels. This is achieved by hard wiring the serializer in test mode, which produces a clock waveform with the output passing through the same circuit path as the data in a data channel.

The output clock signal recovers the data on the receive end without the need for clock recovery. The receiver has per-channel skew correction to account for on-chip mismatches, intrinsic delays, and interconnect medium mismatches.

The LVDS clock output driver is similar to that used in other data channel outputs. The “group delay” of the output clock and data channels relative to the incoming master clock is ~2.5 ns.

LVDS Clock Input

LUPA 1300-2 includes a differential LVDS receiver for the master input clock. The input clock rate is typically 315 MHz and also complies with the ANSI LVDS receiver standards.

The input clock drives the internal clock generator circuit that produces the required internal clocks for image core and sequencer, AFE and ADCs, CRC insertion logic, and serializes. LUPA 1300-2 requires the following internal clock domains (all internal clock domains are 2.5V CMOS levels):

Table 3: LVDS Internal Clock Domains

Sensor module	Frequency
Analog front end	31.5 MHz
Data Block	63 MHz
LVDS Transceivers	315 MHz

All clock domains are designed with identical clock buffer networks to ensure equal “group delays” and maintain maximum channel to channel clock variation less than 100 ps.

The jitter specification for sensor input clock is deterministic jitter 500 ps and the Random jitter is 50 ps. Because LVDS data is DDR, use special care to minimize duty cycle distortion. It is advisable to make the duty cycle between 45 percent and 55 percent. Do not enable the overall jitter to exceed the budget available.

This means that the total jitter expected to be added due to thermal noise, input clock jitter, connector, flex, packages, and so on at the input of the receiver cannot exceed the jitter tolerance of the concerned device (in this case, it is 500 ps for LUPA 1300-2).

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PCB Design and Layout Guidelines

Layer Stackup Guidelines

A successful PCB design depends heavily on the stackup design. A good stackup enables designers to optimize their designs for signal integrity, crosstalk, and EMI. For signal integrity, it is important for designers to minimize discontinuities in their topologies. They can reduce crosstalk on their PCBs if they tightly couple (where possible) signal to reference planes. They can also reduce EMI by increasing coupling to their reference planes and (where possible) shielding signal by routing them partially or completely as striplines. Carefully choosing materials for stackup also reduces PCB manufacturing cost.

- The LUPA 1300-2 sensor has 12 LVDS outputs running at 622 Mbps. Therefore, it is important to tightly control the trace impedance to meet signal integrity requirements. Make certain that there are consistent reference planes to meet the electromagnetic compatibility requirements. Control board impedance to 100 ohms for differential signals and 50 ohms for single ended signals.
- When designing for a specific differential ZO (ZDIFF) for edge-coupled lines, adjust the trace width "W" to alter ZDIFF. In addition, do not adjust "S". Make this the minimum spacing specified by your PCB vendor for line-to-line spacing.
- To calculate ZO and ZDIFF, use the following equations for edge-coupled differential lines:

Microstrip

$$Z_{DIFF} = 2 \times Z_0 (1 - 0.48e^{-0.96 s/h})\Omega \qquad \text{Equation 1}$$

Stripline

$$Z_{DIFF} = 2 \times Z_0 (1 - 0.374e^{-2.9 s/h})\Omega \qquad \text{Equation 2}$$

Microstrip

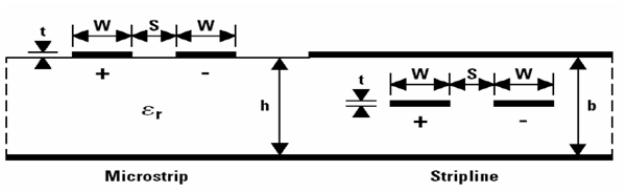
$$Z_0 = 60 \times \ell n[(4h/0.67(0.8W + t)]/\sqrt{0.457\varepsilon_r + 0.67\ell n} \qquad \text{Equation 3}$$

Stripline

$$Z_0 = 60 \times \ell n[(4b/0.67(0.8W + t)]/\sqrt{\varepsilon_r} \qquad \text{Equation 4}$$

Note For edge coupled striplines, the turn “0.374” may be replaced with “0.748” for lines which are closely coupled (S <12 mils)

Figure 3 Microchip and Stripline Transmission Lines in PCB Design



- A good stackup design can significantly reduce the amount of crosstalk that is seen on a PCB. In digital designs, inductive crosstalk usually dominates capacitive crosstalk. Inductive coupling results from return currents, which generate magnetic fields in other traces leading to crosstalk. To minimize the crosstalk, a common rule is to make the spacing between the traces three times the dielectric height. For example, if you have a 5 mil dielectric height, you need a minimum of 15 mils between traces on the layer.
- It is advisable to route LVDS as stripline between ground planes or edge coupled offset striplines. The signals that are routed on striplines reduce crosstalk problems as compared to microstrips.
- Energy radiation from one electronic device to another capable of disrupting the proper functioning of the latter is electromagnetic interference (EMI). Compliance with EMI standards, such as FCC, CISPR, or VCCI are influenced by signal integrity and crosstalk performance of a given PCB. Controlling signal integrity and crosstalk reduces the EMI on a PCB. In designing a stackup, a guideline to reduce EMI is to reduce the current loop area, around which a high speed signal propagates. The return path should lie just beneath the signal track and not encounter slot or splits in ground plane
- It is important for designers to work with PCB material vendors and fabrication facilities to determine what type of materials are available to meet design needs at the lowest costs.
- The number of different power supplies going to the sensor also governs the number of power layers required and hence the stack up. Power plane split up must not result in complex current loop formation.
- Use at least four PCB board layers (top to bottom): LVDS, ground, power, and TTL signals. Dedicating planes for VCC and ground are typically required for high speed design. The solid ground plane is required to establish a controlled (known) impedance for the transmission line interconnects. A narrow spacing between power and ground also creates an excellent high frequency bypass capacitance.

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- The LUPA 1300-2 rider board is a controlled impedance 8 layer board
- Single ended is 50 ohms impedance. (6.5 mil trace and 9 mil isolation)
- Differential pair is 100 ohms impedance. (5 mil trace and 9 mil isolation)
- Layer stack up used for LUPA 1300-2 Demo Kit:
  - Layer 1: TOP (No controlled impedance)
  - Layer 2: GND1
  - Layer 3: SIGNAL1 (Single ended and Diff Signal)
  - Layer 4: GND2
  - Layer 5: POWER
  - Layer 6: SIGNAL2 (Single ended and Diff Signal)
  - Layer 7: GND3
  - Layer 8: Bottom (No controlled impedance).

Board Thickness

The sensor is available in uPGA package, the length of sensor pins are 2+/-0.2 mm. In case of direct mounting of sensor on board; there is a limitation on board thickness. A board thickness of 1.6 mm or less is better. This is because pins are not visible from the outside and might not be soldered properly

Sensor Placement Guidelines

- Place the sensor on board so that the pixel array center coincides with the lens /optics
- Avoid placing power supply regulators, inductor, crystals, or any other component just beneath the sensor.

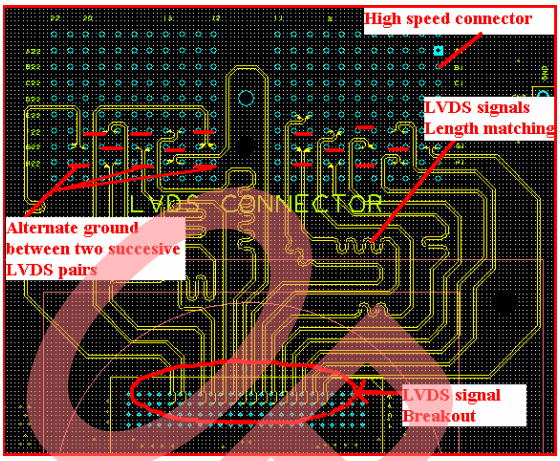
LVDS Interface Guidelines

Controlled interconnect impedance, proper driver load, and interconnect termination are the key points to consider when designing low jitter signal transmission. Remember the following points while designing and routing LVDS signals:

- LVDS signals have very fast edges and are very sensitive to any impedance discontinuities and demands careful interconnect designs. Use controlled impedance PCB traces, which match the differential impedance of the transmission medium (such as cable) and termination resistor. A multi-layer printed circuit board with controlled transmission line impedances is required. Traces for LVDS signals should be closely coupled and designed for 100Ω differential impedance.
- Reference all transmission lines between LVDS drivers and receivers to a common ground plane except when routed through a balanced differential transmission line such as twisted pair. For twisted pair and other balanced lines, a grounded shield enables common mode return current. Connect the shield to the ground planes at thge beginning and end of the twisted pair cable. If no shield connection is available, take extra care to use symmetric and equal length routing. Balancing the capacitive load on the differential pair reduces the conversion of common mode noise to differential signal. Make certain that the ground plane has no breaks under the signal path to avoid large discontinuities from increased inductance.
- Routing LVDS as stripline or microstrip transmission line:
  - Edge coupled microstrip line offers the advantage that a higher differential ZO is possible (100 to 150Ω). It may also be possible to route from a connector pad to the device pad without any via. This provides a "cleaner" interconnect. A limitation of microstrip lines is that these can only be routed on the two outside layers of the PCB, thus limiting routing channel density.
  - Stripline may be either edge coupled or broad-side lines. Because they are embedded in the board stack and typically sandwiched between ground planes, they provide additional shielding. This limits radiation and also coupling of noise to the lines. They also require the use of via to connect to them.
- Differential pair termination - Differential signal I/O standards require a termination resistor between the signals at the receiving device For the LVDS standard, the termination resistor should match the differential load impedance of the bus (typically 100 ohm +/-1% tolerance).
- Surface mount resistors are the best. The PCB stubs, component leads, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be <7 mm (12 mm max).
- The LVDS signal lines should have equal length with symmetric routing between source and destination to maximize common mode rejection. The two LVDS signals should run close together on the PCB. Keep the distance between the differential traces (*S*) constant over the entire trace length

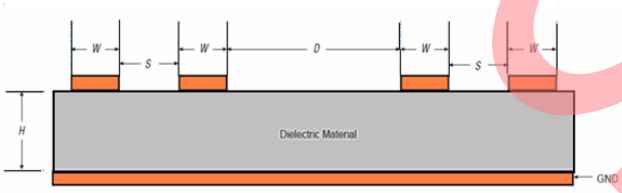
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Figure 4 Breakout of Sensor LVDS Signals in LUPA 1300-2 Demo Kit



- Match electrical lengths between traces of a pair to minimize skew. Skew between the signals of a pair result in a phase difference between the signals. That phase difference destroys the magnetic field cancellation benefits of differential signals and results in EMI. (Note that the velocity of propagation, v = c/er where c (the speed of light) = 0.2997 mm/ps or 0.0118 in./ps). A general rule is to match lengths of the pair to within 100 mils.

Figure 5 Differential Trace Routing

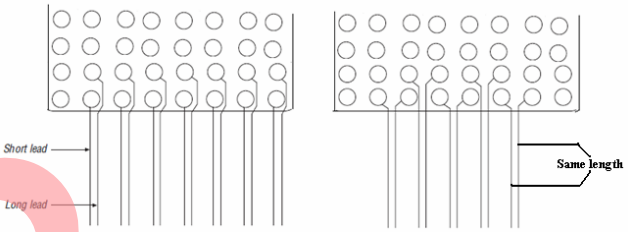


Note

- D=Distance between two differential pair signals.
- W=Width of trace in differential pair.
- S= Distance between the trace in differential pair.
- H= Dielectric height above the ground plane.
- Make sure D is greater than 2S to minimize the crosstalk between the two differential pairs.
- To minimize reflection noise, place the differential traces S = 3H as they leave the device.
- The distance between a pair and a TTL/CMOS signal should be >3S at a minimum. Even better, locate the TTL/CMOS signals on a different plane isolated by a ground plane.
- If a guard ground trace or ground fill is used, it should be >2S away.
- Avoid using multiple vias, because they can cause impedance mismatch and inductance. Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° levels instead.
- Within a pair of traces, the distance between the two traces should be minimized to maintain common mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable. The key to "imbalances" is to make as few as possible and as small as possible. Differential transmission works best on a balanced interconnect. For the best results, both lines of the pair should be as identical as possible.

Routing LVDS Signals over a Connector

Figure 6 LVDS Connectors



Use these guidelines while selecting connectors for LVDS applications:

- Connectors must have low skew with matched impedance.
- Select connectors with same length leads for lower skew and crosstalk.
- Place two members of the same differential pair adjacent to each other on the connector.
- Place ground pins between differential pairs.
- End pins of the connectors should preferably be grounded and must not be used for high speed signals.
- Properly terminate all unused pins of the connector.

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LUPA 1300-2 Power Supply

The various blocks of the sensor such as on-chip column amplifier, output stage, digital module, driver, ADC, LVDS, and so on, have their own power supply and ground. Table 4 is an overview of the power supplies and the required DC and the peak currents.

Table 4 LUPA 1300-2 Power Supplies

Name	DC Current (mA)	Typ	Description
Vsamp	2	2.5V	Power supply of sampling circuitry
Vres	0	3.5	Power supply of reset drivers
Vres_ds	0	3.5	Power supply of dual slope
Vres_ts	0	1.8	Power supply of triple slope
Vmem_l	0	2.5	P.S of pixel memory element (low)
Vmem_h	0	3.3	P.S of pixel memory element (high level)
Vadc	185 mA	2.5V	P.S of on chip ADCs
Vpix	26 mA	2.5V	P.s of pixel array
Vpech	0 mA	0.7V	Anti-blooming P.S
Vana	6 mA	2.5V	
Vdig_lvds	241 mA	2.5V	Digital power supply
Vbuf	40 mA	2.5V	PS of onboard buffers
Vresab	0 mA	0.7V	Anti-blooming P.S
GNDlvds		0V	LVDS module ground
GNDadc		0V	ADC module ground
GNDdig		0V	Digital module ground
GNDana		0V	Analog Drivers Ground
GNDpix		0V	Pixel array ground
GNDbuf		0V	Analog buffers ground

On chip, the ground lines of every module are kept separate to improve shielding and electrical crosstalk between them. Off-chip the grounds can be combined, but not all power supplies may be combined. This results in several different power supplies, but this is required to reduce electrical crosstalk and to improve shielding, dynamic range, and output swing.

Power supplies can be combined according to the following rules. For power supply naming, see Table 4.

- All ground pins can be combined.
- Vsamp, Vres_ds, Vmem_l, Vadc, Vpix, Vana, Vbuf (all analog or almost all analog supplies) can be combined to one analog power supply.
- Combine Vlvds and Vdig to one digital power supply.
- Reduce system noise by providing clean, evenly distributed power to all the devices on board. Follow the guidelines mentioned in the next section for distributing and filtering power supply.

Decoupling Capacitors

- Reduce the system noise by filtering and evenly distributing power to all devices. To decrease the low-frequency (<1 kHz) noise caused by the power supply, filter the noise on power lines at the point where the power connects to the PCB and to each device. Place a 100 µF or more value electrolytic capacitor/bulk cap where the power supply lines enter the PCB.
- In case of voltage regulator, place the capacitor immediately after the output pin that provides the VCC signal to the device(s). Capacitors not only filter low-frequency noise from the power supply, but also supply extra current when many outputs switch simultaneously in a circuit.
- To filter the high frequency noise at the device, place decoupling caps (0.1 µF for each pin) close to the respective power supply pin. The goal is to minimize the amount of line inductance and series resistance between the decoupling capacitor and that device.

Table 5 LUPA 1300-2 Recommended Decoupling Caps

Device	Decoupling Requirements
LUPA 1300-2	0.1 uF ceramic capacitor for each power supply pin as close as possible to the device.
	For every 4-5 power supply pin, place a 1 uF capacitor, as close as possible to the VCC and Ground pins.
	Place 10 uF capacitor close to the device.
	Vpix is an analog supply with high duty cycle; to meet the fast transient on vpix power supply, it is recommended to use twice decoupling caps as compared to digital supplies

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- It is recommended to give preference to LDO regulators over a switching regulator. Try not to use switching regulators. It is very important to have spike-free supplies, especially for analog blocks of the sensor. Otherwise the blanking pulses rolling in vertical directions are seen in the image.
- A system can distribute power throughout the PCB with either power planes or a power bus network. The power plane maintains VCC and distributes it equally to all devices. Power planes provide very high current-sink capability, noise protection, and shielding for the logic signals. Use power planes instead of thick track to uniformly distribute power with less IR drop.
  - In case of LUPA1300-2 use planes for the supply rails (2.5V, 5V). In case of other supplies (0.7V, 1.8V, 3.5V and so on) which require less current, use thick and broad traces)
- Use separate analog and digital power planes or create partitioned islands (split planes). Take care during power plane splitting; it should not result in complex current loop formation.

Summary

This application note lists the layout guidelines for LUPA 1300-2 .Follow the recommended layout guidelines along with the high speed best practices for effective PCB design.

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*A	2748140	08/04/2009	SEMA	Post to external web.
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