# Jitter Generation and Jitter Tolerance of Independent Channel HOTLink II™ Devices for Datacom Applications - AN5077

## AN5077

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**Associated Application Notes**: None

## Abstract

The HOTLink II™ family of physical layer (PHY) devices is a point-to-point or point-to-multipoint communications building block that provides serialization, deserialization and optional 8B/10B encoding/decoding as well as framing functions within the same device. A HOTLink II device is a frequency agile transceiver with the ability to transport data at rates between 0.195 and 1.54 Gigabits per second (Gbps) per channel. These devices are compliant with datacom standards such as Open Base Station Architecture Initiative (OBSAI-RP3), Common Public Radio Interface (CPRI), Gigabit Ethernet (GigE), Fibre Channel (FC), Digital Video Broadcasting-Asynchronous Serial Interface (DVB-ASI) and Enterprise System CONnection (ESCON). All of these standards specify a limit on the intrinsic jitter that can be present at the output port of a serial transmitter in the absence of applied input jitter. These standards also specify the amount of jitter in serial data that can be tolerated by a serial receiver without generating bit errors.

## Introduction

This application note describes the jitter generation of the HOTLink II transmitter and the jitter tolerance of the HOTLink II receiver measured on independent channel HOTLink II devices.

## Jitter Generation of HOTLink II Transmitters

Jitter generation is defined as intrinsic jitter present at the output port of a device in the absence of applied input jitter. This section describes the measurement methodology, test procedure and the results for the jitter generation of the Independent channel HOTLink II devices for Gigabit Ethernet (GigE), Fibre Channel (FC), Digital Video Broadcasting-Asynchronous Serial Interface (DVB-ASI) and Enterprise System CONnection (ESCON).

### Measurement Methodology

The objective is to measure the transmit jitter from the HOTLink II transmitters in the absence of applied input jitter using the CYV15G0404DXB Evaluation Board [Reference 1]. The output jitter is dependent on the intrinsic jitter present in the reference clock and on the characteristics of the internal PLLs of the HOTLink II transmitter. The intrinsic power supply noise and the noise generated due to switching of different devices on the board also contribute to the measured jitter. Hence, the contribution of jitter from external sources like power supply noise, reference clock, switching noise is kept to a minimum through proper board design techniques and by choosing an extremely low phase noise reference source.

The measurement equipment used to measure jitter is the Wavecrest SIA 3000. This equipment was chosen because it has the capability to separate RMS random jitter and peak-to-peak deterministic jitter.

To qualify the amount of phase noise allowed in the reference clock, the total jitter at the serial outputs needs to be measured. Separate values of random and deterministic jitter are needed to calculate the total jitter for the data communication standards supported by the HOTLink II device.

Total Jitter (TJ) is composed of two basic elements, Random and Deterministic Jitter. It is given by $TJ = (RJ(1\sigma) \times N) + DJ$

where

$RJ(1\sigma)$ is the standard deviation of the random jitter distribution,

N is the scaling factor which depends on the Bit Error Rate (BER) specification for the given standard.

Random Jitter is unbounded and can be described by a gaussian probability distribution. RJ is characterized by its standard deviation (rms) value.

$RJ(pk\text{-}pk) = RJ(1\sigma) \times N$.

where

RJ (pk-pk) is the peak-to-peak random jitter

Deterministic jitter has a non-gaussian probability density function. DJ is characterized by its bounded peak-to-peak value.

DJ = DCD + ISI,

where

DCD is duty cycle distortion,

ISI is intersymbol interference.

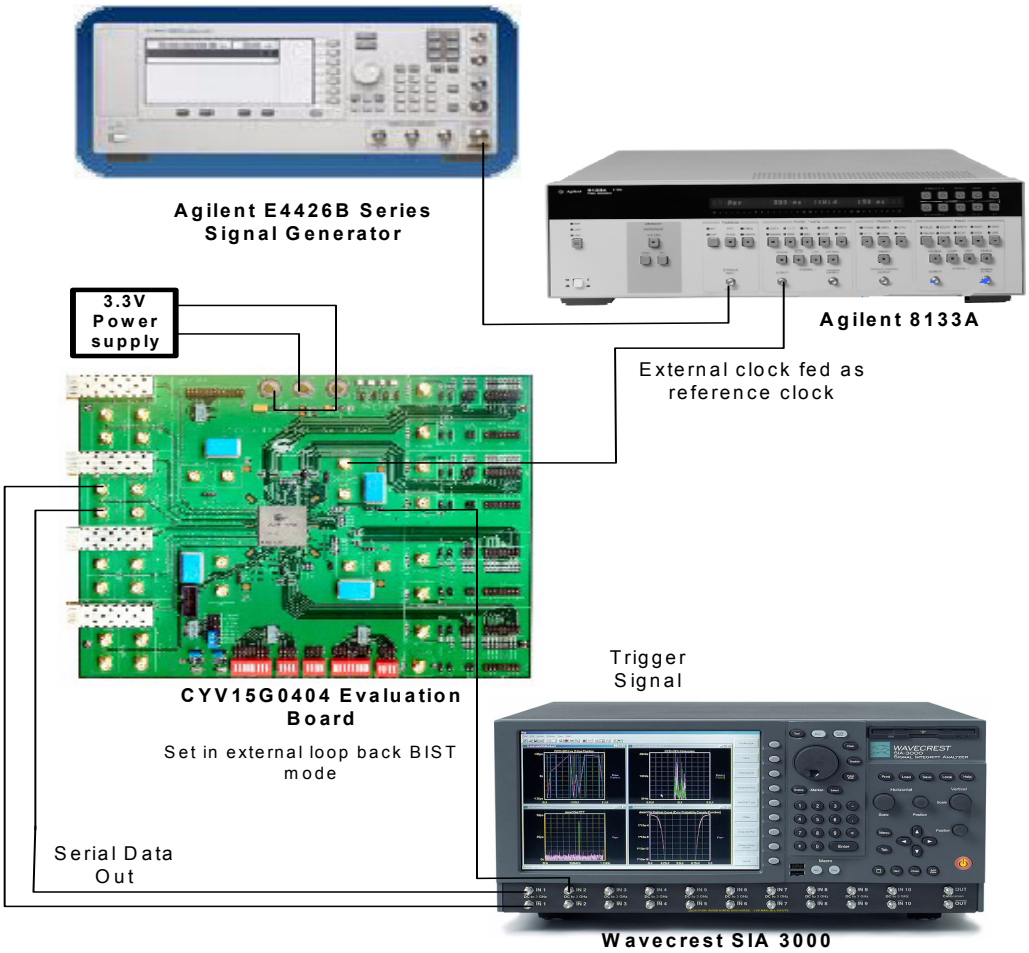
Table 1. Scaling Factor N Depending on BER

| BER | N |
|---|---|
| $10^{-10}$ | 12.723 |
| $10^{-11}$ | 13.412 |
| $10^{-12}$ | 14.069 |
| $10^{-13}$ | 14.698 |
| $10^{-14}$ | 15.301 |
| $10^{-15}$ | 15.883 |

The Wavecrest SIA 3000 has the capability to separate random and deterministic jitter when the “Known Pattern with Marker” (KPWM) method is used. In this method, the Wavecrest SIA 3000 is expected to detect a known pattern that is repeated after a certain number of clock cycles. It is also expected to detect a pattern marker that marks the beginning of the pattern.

The HOTLink II transmitters have an internal Built-in Self Test (BIST) pattern generator that generates a repetitive 527 word long pattern. A channel-specific TXERRx signal generates a pulse at the beginning of every BIST cycle. The BIST pattern output, along with the TXERRx marker, are used as inputs to the Wavecrest SIA 3000 to measure random and deterministic jitter. The BIST pattern resembles real-world 8B/10B encoded data.

Figure 1. Set-up for Jitter Generation Measurement of HOTLink II Transmitter




## Test Procedure

The test set-up for jitter generation is shown in Figure 1 on page 2. The output of the Agilent E4426B ESG-AP Series signal generator is connected to the Agilent 8133A pulse generator. The output from the Agilent 8133A is connected as a reference clock to the HOTLink II device. The Agilent

E4426B and Agilent 8133A are cascaded, because the clock obtained from this set-up has a lower phase noise than the clock obtained from the Agilent 8133A alone.

The board is powered up and the transmitter is set up to transmit BIST data through the serial output. The serial BIST data from the channel under test is differentially fed to the Wavecrest SIA 3000. TXERRx is connected to the other channel of the Wavecrest SIA 3000 in order to mark the beginning of every BIST cycle as a trigger.

To measure jitter generation for various standards, the output of the Agilent E4426B is set to an appropriate frequency (bit rate/10). The bit error rate (BER) and corner frequencies in the Wavecrest SIA 3000 are changed to appropriate values, as specified by the associated standards. BER values are specified by the datacom standards. Corner frequency is usually equal to data-rate/1667 [Reference 7], and it sets the cut off frequency for the high pass filter applied to the jitter measurements. This filter is used to exclude the low frequency jitter, while measuring jitter in the Wavecrest SIA 3000, because such low frequency jitter can be tracked well by the Receiver Clock and Data recovery PLLs.

Jitter measurements are performed for each standard by setting the appropriate reference clock frequency, bit error rate (BER) values, and corner frequency values. Table 2 to Table 5 on page 4 present the measurement results for each of the standards across voltage and temperature.

Table 2. Jitter Generation Values of HOTLink II Device for Gigabit Ethernet [Reference 3]

| Temp | $V_{CC}$ | Frequency | Corner Frequency | BER | DCD + ISI | DJ | RJ (1σ) | TJ |
|---|---|---|---|---|---|---|---|---|
| °C | V | MHz | kHz | – | ps | ps | ps | ps |
| GigE Spec | GigE Spec | 125 | 750 | $10^{-12}$ | – | 80 | – | 192 |
| –40 | 3.14 | 125 | 750 | $10^{-12}$ | 47.21 | 47.2 | 4.34 | 108.37 |
| –40 | 3.47 | 125 | 750 | $10^{-12}$ | 50.62 | 50.62 | 4.74 | 117.31 |
| 85 | 3.14 | 125 | 750 | $10^{-12}$ | 54.6 | 54.6 | 5.11 | 126.49 |
| 85 | 3.47 | 125 | 750 | $10^{-12}$ | 49.16 | 49.16 | 5.44 | 125.69 |

Table 3. Jitter Generation Values of HOTLink II Device for Fibre Channel Standard [Reference 4]

| Temp | $V_{CC}$ | Frequency | Corner Frequency | BER | DCD + ISI | DJ | RJ (1σ) | TJ |
|---|---|---|---|---|---|---|---|---|
| °C | V | MHz | kHz | – | ps | ps | ps | ps |
| FC Spec | FC Spec | 106.25 | 637 | $10^{-12}$ | – | 103 | – | 198 |
| –40 | 3.14 | 106.25 | 637 | $10^{-12}$ | 43.02 | 43.02 | 4.96 | 112.8 |
| –40 | 3.47 | 106.25 | 637 | $10^{-12}$ | 45.24 | 45.24 | 4.66 | 110.8 |
| 85 | 3.14 | 106.25 | 637 | $10^{-12}$ | 45 | 45 | 5.27 | 119.14 |
| 85 | 3.47 | 106.25 | 637 | $10^{-12}$ | 42.83 | 42.83 | 5.58 | 121.33 |

Table 4. Jitter Generation Values of HOTLink II Device for DVB-ASI Standard [Reference 6]

| Temp | $V_{CC}$ | Frequency | Corner Frequency | BER | DCD + ISI | DJ | RJ (1σ) | TJ |
|---|---|---|---|---|---|---|---|---|
| °C | V | MHz | kHz | – | ps | ps | ps | ps |
| DVB spec | DVB Spec | 27 | 162 | $10^{-13}$ | – | 370 | 20.138 | 666 |
| –40 | 3.14 | 27 | 162 | $10^{-13}$ | 45.61 | 45.6 | 6.73 | 144.5 |
| –40 | 3.47 | 27 | 162 | $10^{-13}$ | 43.15 | 43.15 | 7.55 | 154.11 |
| 85 | 3.14 | 27 | 162 | $10^{-13}$ | 48.49 | 48.49 | 8.36 | 171.36 |
| 85 | 3.47 | 27 | 162 | $10^{-13}$ | 55.79 | 55.79 | 7.63 | 167.93 |

Table 5. Jitter Generation Values of HOTLink II Device for ESCON Specification [Reference 5]

| Temp | $V_{CC}$ | Frequency | Corner Frequency | BER | DCD + ISI | DJ | RJ (1σ) | TJ |
|---|---|---|---|---|---|---|---|---|
| °C | V | MHz | kHz | – | ps | ps | ps | ps |
| ESCON spec | ESCON Spec | 20 | 120 | $10^{-15}$ | – | – | – | 800 |
| –40 | 3.14 | 20 | 120 | $10^{-15}$ | 54.99 | 85.23 | 9.94 | 243.11 |
| –40 | 3.47 | 20 | 120 | $10^{-15}$ | 55.88 | 87.87 | 10.23 | 250.35 |
| 85 | 3.14 | 20 | 120 | $10^{-15}$ | 56.382 | 78.57 | 8.389 | 211.81 |
| 85 | 3.47 | 20 | 120 | $10^{-15}$ | 59.38 | 82.75 | 9.3 | 230.46 |

# Jitter Tolerance of HOTLink II Receiver

Jitter tolerance is the ability of the receiver clock and data recovery phase locked loop (CDR PLL) to track the jitter in the incoming serial data stream. The jitter tolerance value indicates the amount of input jitter that can be tolerated by the receiver so that the bit errors in the incoming serial data stream do not exceed the specified bit error rate.

## Measurement Methodology

The objective of this test is to measure the jitter tolerance of HOTLink II receivers for the Gigabit Ethernet, FibreChannel and ESCON standards. These standards specify a limit on the amount of total jitter and its components present in the incoming serial data that can be tolerated by the serial receiver without generating bit errors. ESCON has specifications for the total jitter alone. The standards with specifications are summarized in Table 6 on page 5.

To test the jitter tolerance of the serial receiver, we should be able to increase the amount of random and deterministic jitter that is introduced in the serial data. Random jitter can be increased by using a random noise modulated clock input to the serial data generator. Deterministic jitter can be increased by passing the data through a transmission line (such as a Printed Circuit Board or coaxial cable) and through jitter injection modules and Transition Time Converters (TTC). In order to measure the amount of random jitter and deterministic jitter introduced, appropriate jitter measurement equipment is required. To ensure that the serial data from the HOTLink II receiver is recovered error free in the presence of added jitter, an error detector is used. A block diagram of the jitter measurement methodology is shown in Figure 2 on page 5.

## Test Procedure

For jitter tolerance testing, jitter greater than that specified by the standard is introduced in the serial data. This serial data is fed to the HOTLink II receiver and reclocked through the receiver clock and data recovery phase locked loop (CDR PLL). The Anritsu 1632C Digital Data Analyzer consists of a serial data generator and an error detector module. The Anritsu 1632C is used to transmit serial data and check bit errors. It requires an external bit rate clock, which is available from the Agilent E4426B signal generator. The bit rate clock is passed through the NoiseCom UFX-7107 box so that a controlled amount of random jitter can be added before the clock is fed to the Anritsu 1632C. This is done by changing the noise attenuation levels on the NoiseCom box.

Serial data from the Anritsu 1632C is passed through the backplane, transition time convectors (TTC) and the jitter injection modules to introduce deterministic jitter.

The test set-up for jitter tolerance is shown in Figure 3. To measure jitter tolerance, the HOTLink II device is set up in the reclocker mode. Serial data that has random and deterministic jitter added to it, is fed to the HOTLink II

receiver. Serial data from the HOTLink II transmitter is then checked for bit errors, using the Anritsu MP1632C Digital data analyzer.

The frequency of the reference clock on the HOTLink II board and the frequency of the reference clock input to the Anritsu 1632C determine the standard for which the jitter tolerance is being measured. The serial data input to the HOTLink II device is also connected to the Wavecrest SIA 3000. This is done to measure the amount of jitter in the serial data and to check that it exceeds the jitter tolerance specification of the association standard.

Table 6. Jitter Tolerance Specification for GigE, Fibre Channel and ESCON Standards

| Standard | BER | Frequency | DJ | RJ(1σ) | TJ |
|---|---|---|---|---|---|
| – | – | MHz | ps | ps | ps |
| GigE | $10^{-12}$ | 125 | 370 | 16.4 | 600 |
| Fibre Channel | $10^{-12}$ | 106.25 | 348 | 20.75 | 640 |
| ESCON | $10^{-15}$ | 20 | – | – | 3600 |

Figure 2. Block Diagram for Jitter Measurement of HOTLink II Device

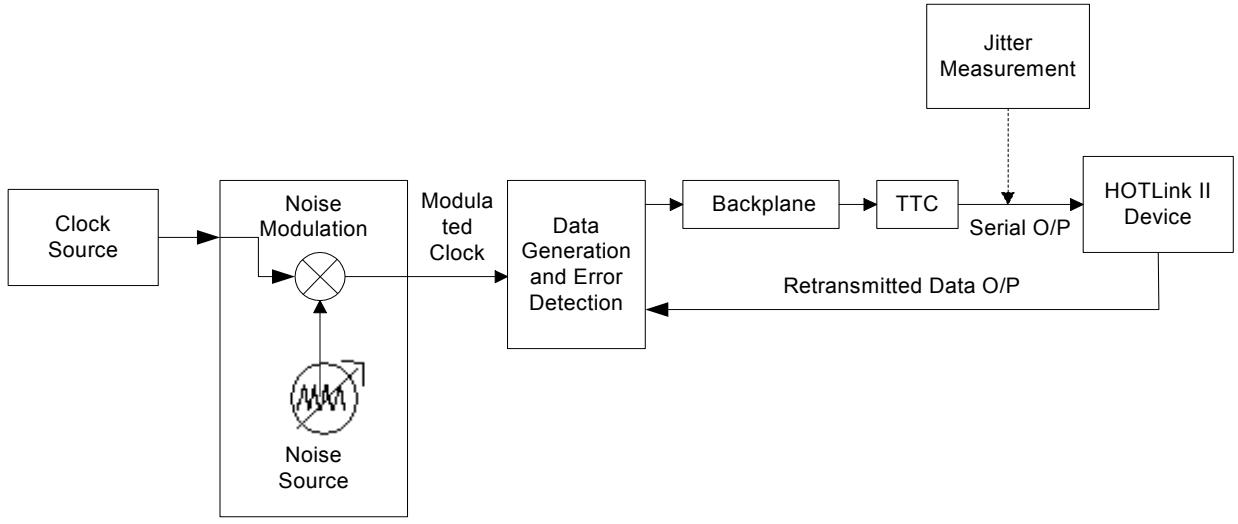
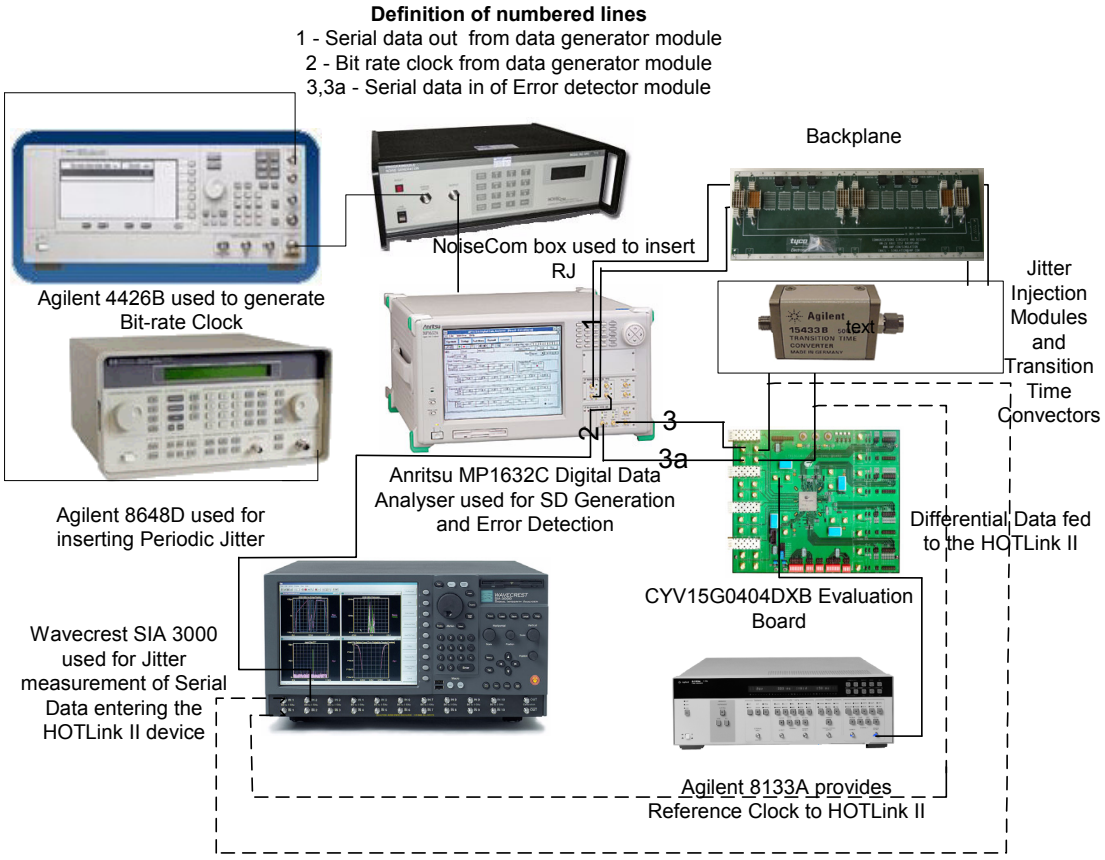


Figure 3. Test Set-up for Jitter Tolerance Measurement of HOTLink II Device




The retransmitted serial data output from the HOTLink II transmitter (as HOTLink II is set up in the reclocker mode) is fed to the Anritsu 1632C error detector module to ensure that there are no bit errors for the given amount of random and deterministic jitter.

The HOTLink II receiver can potentially achieve an even higher jitter tolerance than that mentioned in this document but it was tested only for the amount of jitter documented in the associated standards.

To measure jitter tolerance of the HOTLink II receiver for different standards, the output frequency of the Agilent 4426B and the Agilent 8133A are changed according to the corresponding standard. By changing the noise modulation level of the reference clock to the Anritsu 1632C, and by changing the backplane length and values of jitter injection modules, a jitter value that exceeds the corresponding specification can be obtained.

The jitter tolerance test conditions are shown in Table 7.

Table 7. Test Conditions for Jitter Tolerance

| Condition | Temperature | Part Voltage |
|---|---|---|
| Hot Corner | 85 °C | 3.314 V |
| Typical | Ambient | 3.3 V |
| Cold Corner | –40 °C | 3.465 V |

## Gigabit Ethernet

The output frequency of the Agilent 4426B and Agilent 8133A are set to 1250 MHz and 125 MHz, respectively. The noise attenuation of the NoiseCom box and the jitter injection modules are altered to add jitter above the Gigabit Ethernet specification3 for jitter tolerance.The jitter value is then incremented until a bit error is observed on the Anritsu 1632C. The jitter tolerance values of the HOTLink II receiver across different corners for Gigabit Ethernet are shown in Table 8 on page 7.

## Fibre Channel

The output frequency of the Agilent 4426B and Agilent 8133A are set to 1062.5 MHz and 106.25 MHz, respectively. For jitter tolerance tests for the Fibre Channel standard4, the bit rate clock from the Agilent E4426B is not modulated. Instead, an additional intersymbol interference (ISI) is added in place of sinusoidal jitter (SJ). At high frequency, additional intersymbol interference (ISI) has the same effect as sinusoidal jitter (SJ). In this case, intersymbol interference deterministic jitter is generated by using 60 inches of backplane, two 0.5 UI jitter injection modules and two 250 ps transition time convectors. The results across different corners are presented in Table 9.

## ESCON

The output frequency of the Agilent 4426B and Agilent 8133A are set to 200 MHz and 20 MHz, respectively. The signal from the pattern generator is looped through 240 inches of backplane, two 2000 ps transition time convectors (TTC), two 1000 ps TTCs, one 500 ps TTC and two 250 ps TTCs to add jitter to the serial data stream. The signal is then amplified using the Colby PG5000A pulse generator (in normal mode) to produce differential outputs with a magnitude of 0.66 V (pk-pk). When measured using the Wavecrest SIA 3000, a total jitter (Tj) value of 4.037 ns is reported for a BER of 10E-12, greater than the jitter requirement of 3.6 ns, as per ESCON specification. The jitter tolerance values of HOTLink II device for ESCON across different corners are shown in Table 10 on page 8.

Table 8. Jitter Tolerance Values of HOTLink II Receiver for Gigabit Ethernet Standard [Reference 3]

| Condition | Case | Frequency | BER | DJ | RJ (1σ) | TJ |
|---|---|---|---|---|---|---|
| – | – | MHz | – | ps | ps | ps |
| GigE Spec | GigE spec | 125 | $10^{-12}$ | 370 | 16.4 | 600 |
| Hot | Worst | 125 | $10^{-12}$ | > 432 | > 18.4 | > 690 |
| Hot | Average | 125 | $10^{-12}$ | > 461 | > 25.04 | > 813.28 |
| Hot | Best | 125 | $10^{-12}$ | > 531 | > 22.48 | > 847.27 |
| Typical | Worst | 125 | $10^{-12}$ | > 433 | > 24.40 | > 776.28 |
| Typical | Average | 125 | $10^{-12}$ | > 477 | > 26.02 | > 843.07 |
| Typical | Best | 125 | $10^{-12}$ | > 531 | > 22.48 | > 847.27 |
| Cold | Worst | 125 | $10^{-12}$ | > 432 | > 18.40 | > 690.86 |
| Cold | Average | 125 | $10^{-12}$ | > 460 | > 23.32 | > 788.08 |
| Cold | Best | 125 | $10^{-12}$ | > 531 | > 22.48 | > 847.27 |

Table 9. Jitter Tolerance Values of HOTLink II Receiver for Fibre Channel Standard [Reference 4]

| Condition | Case | Frequency | BER | DJ | RJ (1σ) | TJ |
|---|---|---|---|---|---|---|
| – | – | MHz | – | ps | ps | ps |
| FC Spec | FC Spec | 106.25 | $10^{-12}$ | 348 | 20.75 | 640 |
| Hot | Worst | 106.25 | $10^{-12}$ | > 470 | > 27.8 | > 861.11 |
| Hot | Average | 106.25 | $10^{-12}$ | > 474 | > 30.22 | > 899.16 |
| Hot | Best | 106.25 | $10^{-12}$ | > 479 | > 36.5 | > 992.51 |
| Typical | Worst | 106.25 | $10^{-12}$ | > 470 | > 27.8 | > 861.11 |
| Typical | Average | 106.25 | $10^{-12}$ | > 476.5 | > 33.15 | > 942.88 |
| Typical | Best | 106.25 | $10^{-12}$ | > 479 | > 36.5 | > 992.51 |
| Cold | Worst | 106.25 | $10^{-12}$ | > 470 | > 27.8 | > 861.11 |
| Cold | Average | 106.25 | $10^{-12}$ | > 476.25 | > 31.98 | > 926.17 |
| Cold | Best | 106.25 | $10^{-12}$ | > 479 | > 36.5 | > 992.51 |

Table 10. Jitter Tolerance Values of HOTLink II Receiver for ESCON Specification [Reference 5]

| Condition | Frequency | BER | TJ (HOTLink II) |
|---|---|---|---|
| – | MHz | – | ps |
| ESCON Spec | ESCON Spec | $10^{-15}$ | 3600 |
| Hot | 20 | $10^{-15}$ | > 4037 |
| Typical | 20 | $10^{-15}$ | > 4037 |
| Cold | 20 | $10^{-15}$ | > 4037 |

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# Document History

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**Document Number: 001-14945**

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|---|---|---|---|---|
| ** | 1000600 | NVNS | 04/20/2007 | Existing Application Note in the web - Added Spec No. and new disclaimer and also updated the copyright date<br>Please post in the web- overwrite the existing AN5077 file |
| *A | 3248643 | NVNS | 05/04/2011 | Updated in new template. |
| *B | 4384601 | NVNS | 05/20/2014 | No technical updates.<br>Completing Sunset Review. |

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