Guidelines for Selecting Reference Clock Input of the HOTLink II™ Device in Datacom Applications - AN5076

AN5076

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Abstract

The HOTLink II™ family of physical layer (PHY) devices is a point-to-point or point-to-multipoint communications building block that performs serialization, deserialization and optional 8B/10B encoding/decoding and framing functions within a single device. A HOTLink II device is a frequency agile transceiver with the ability to transport data at rates between 0.195 and 1.54 Gigabits per second (Gbps) per channel. These devices are compliant with datacom standards such as Open Base Station Architecture Initiative (OBSAI-RP3), Common Public Radio Interface (CPRI), Gigabit Ethernet (GigE), Fibre Channel (FC), Digital Video Broadcasting - Asynchronous Serial Interface (DVB-ASI) and Enterprise System CONnection (ESCON).

These standards specify a limit on the jitter present on the serial data output from a serial transmitter. Common contributors to jitter at the serial output are power supply noise, serial trace layout, line driver performance, performance of the TXPLL, and quality of the reference source for the TXPLL.

Introduction

The purpose of this application note is to analyze one of the contributors of jitter in the serial output, namely the phase noise present in the reference source. The bit-rate clock that clocks the shift register is a multiple of the reference clock. Hence, a portion of the jitter on the reference clock is transferred to the serial bit rate clock which in turn translates to jitter at the serial data output. This is illustrated in Figure 1 on page 2.

This document presents phase noise of nine sample crystal oscillators for which the HOTLink II serial data output meets the jitter specifications for serial output jitter.

The nine sample oscillators tested have frequencies of interest in the corresponding standards:

OBSAI-RP3:

1. Valpey Fisher (VF161BL) 153.6 MHz oscillator

Gigabit Ethernet:

2. Valpey Fisher (VF161BL) 125 MHz oscillator
3. Connor Winfield (P143) 125 MHz oscillator

Fibre Channel:

4. Valpey Fisher (VF161BL) 106.25 MHz oscillator
5. Connor Winfield (P143) 106.25 MHz oscillator

DVB-ASI:

6. Valpey Fisher (VF140BL) 27 MHz oscillator
7. Connor Winfield (HSM913) 27 MHz oscillator

ESCON:

8. Valpey Fisher (VF140BL) 20 MHz oscillator
9. Connor Winfield (HSM943) 20 MHz oscillator

To qualify the amount of phase noise allowed in the reference clock, the total jitter at the serial outputs needs to be measured. Separate values of random and deterministic jitter are needed to calculate the total jitter for the data communication standards supported by the HOTLink II device.

Total Jitter (TJ) is composed of two basic elements, Random and Deterministic Jitter. It is given by $TJ = (RJ(1\sigma) \times N) + DJ$

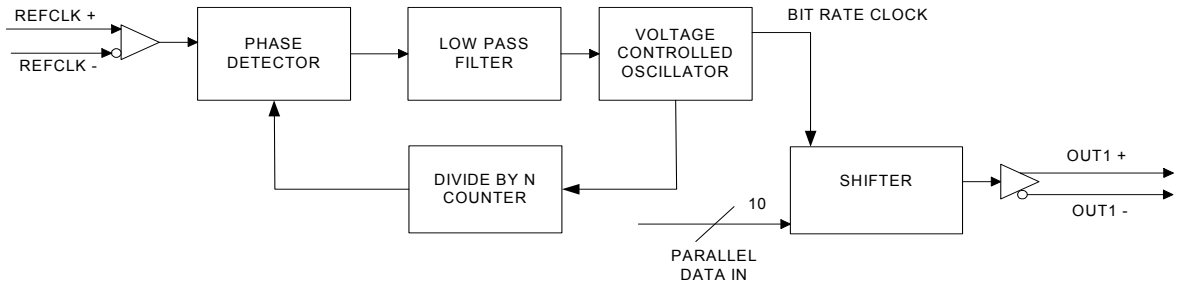
where

$RJ(1\sigma)$ is the standard deviation of the random jitter distribution.

N is the scaling factor which depends on the Bit Error Rate (BER) specification for the given standard.

DJ is the deterministic jitter.

Figure 1. Serial Data Output Shift-Register Clocking Scheme in HOTLink II Transmit Path



Random Jitter is jitter that is not bounded and can be described by a gaussian probability distribution. RJ is characterized by its standard deviation (rms) value.

RJ(pk-pk) = RJ(1σ) × N.

where

RJ (pk-pk) is the peak to peak random jitter.

Deterministic jitter is jitter with a non-gaussian probability density function. DJ is characterized by its bounded peak-to-peak value.

DJ = DCD + ISI,

where

DCD is duty cycle distortion.

ISI is intersymbol interference.

Set-up

The aim is to measure the phase noise of the crystal oscillators under three different levels of noise modulation:

1. No noise modulation.
2. Maximum noise modulation until the serial output jitter is marginally below the specifications.
3. Intermediate noise modulation that yields a serial output jitter that is in between the previous two jitter measurements.

To measure the maximum phase noise tolerated, we need to develop a setup which has the capability to:

- Insert and increase the noise modulation of the reference clock.
- Measure the phase noise of the noise modulated clock fed to the HOTLink II device.
- Measure serial output jitter, as per the associated standards.

The measurement set-up is illustrated in Figure 2 on page 4. The output of the crystal oscillator under test is connected to the external input of UFX7107 NoiseCom box. If the oscillator has a differential output, then the unused output is terminated to a 50 Ω load. The NoiseCom box is used to modulate noise into the clock generated from the crystal oscillator under test. The external modulated output of the NoiseCom box is connected to the external input of the Agilent 8133A pulse generator. The Agilent 8133A is used for two reasons:

1. To generate a low voltage differential output for HOTLink II transceiver.
2. To remove amplitude noise from the noise modulated clock.

The external differential output of the Agilent 8133A is fed as the reference clock to the HOTLink II transceiver in the CYV15G0404DXB evaluation board [Reference 7]. Using the above set-up with no noise modulation, the phase noise of the standalone crystal oscillator and the clock signal obtained from the outputs of Agilent 8133A are found to be equal. Hence the presence of UFX7107 NoiseCom box and Agilent 8133A do not affect the phase noise results in the absence of noise modulation.

This set-up will allow a noise modulated version of the crystal oscillator output to be connected as reference clock input to the HOTLink II transceiver. The HOTLink II device is capable of being set up in the Built-In Self Test (BIST) mode. In this mode the HOTLink II transmitter generates the BIST pattern continuously. This set-up uses the TXERRx as the marker to the Wavecrest SIA 3000 to measure random and deterministic jitter.

The serial output of the channel under test is connected to the Wavecrest SIA 3000 to measure the serial data output jitter. For more details on the

measurement methodologies for serial output jitter refer to the application note on Jitter Generation and Jitter Tolerance of Independent channel HOTLink II™ devices.

The phase noise of the clock output from Agilent 8133A is measured using the Agilent E5500 phase noise measurement system. The reference input to the Agilent E5500 is obtained from the Agilent E8251A signal generator. The phase noise plots of the oscillator under test versus Agilent E8251A are shown in Figure 3 on page 6 to Figure 11 on page 10.

Test Procedure

Test procedure with no noise modulation

In the set-up described, serial data output jitter of the HOTLink II transceiver is first measured without noise modulation from the UFX7107 NoiseCom box (maximum noise attenuation). The phase noise of the reference clock fed to the HOTLink II transceiver is then measured using the Agilent E5500 phase noise measurement system.

Test procedure with maximum noise modulation

In this set-up, the noise modulation is increased (noise attenuation is decreased) and serial data output jitter is measured as above. The noise modulation is further increased until the measured jitter marginally meets the specifications. At this point the phase noise of the reference clock from the Agilent 8133A is measured.

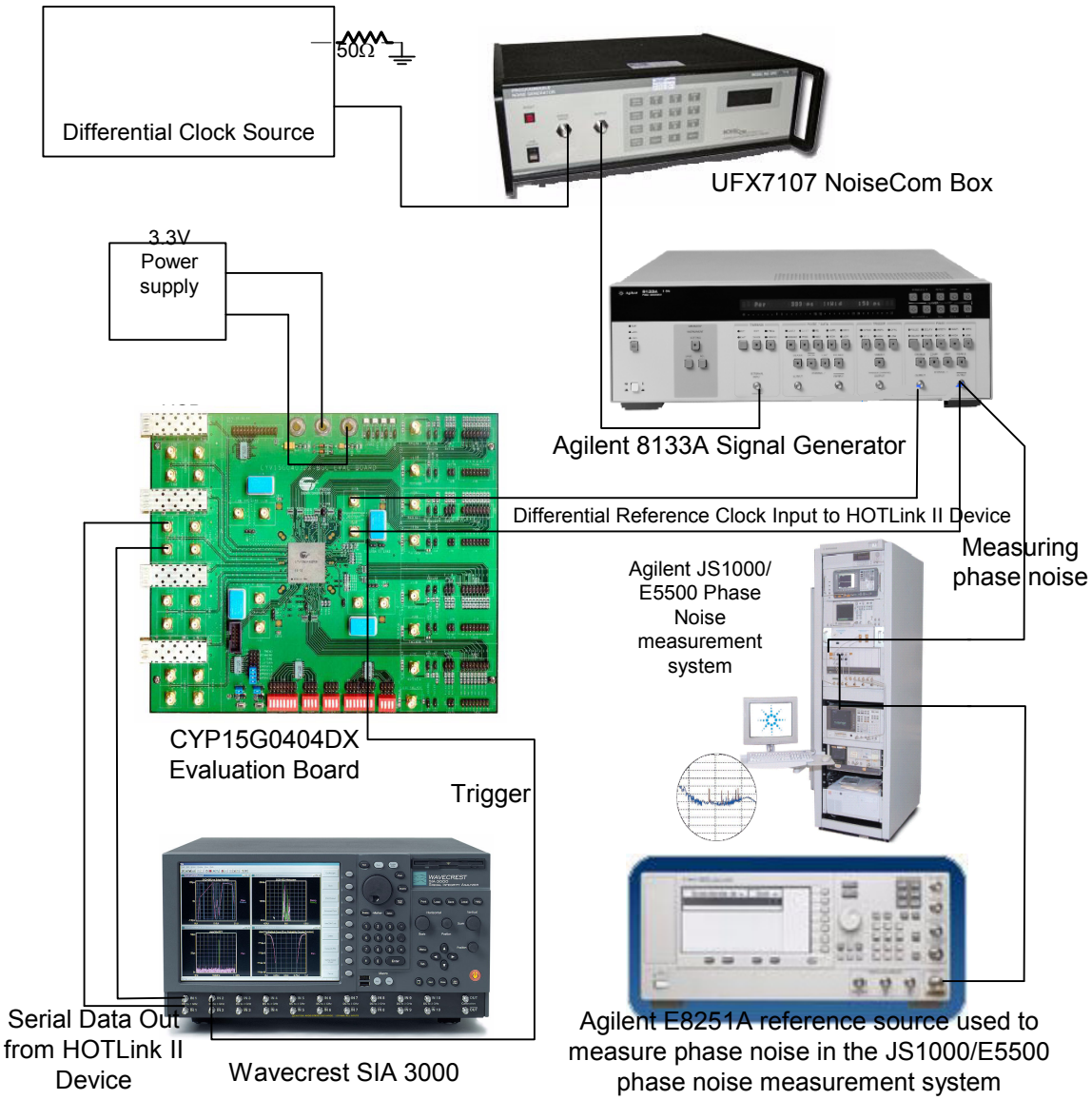
Test procedure with intermediate noise modulation

Using the serial data output jitter values measured from the above mentioned two methods, an intermediate jitter value is determined. Phase noise plot of the reference clock that generates this intermediate jitter is also determined. This procedure is followed for each of the following standards:

1. OBSAI-RP3 [Reference 6]
2. Gigabit Ethernet [Reference 2]
3. Fibre Channel [Reference 3]
4. ESCON [Reference 4]
5. DVB-ASI [Reference 5]

The results from the above measurements are shown graphically in Figure 3 on page 6 to Figure 11 on page 10.

Figure 2. Set-up for Measuring Crystal Oscillator Phase Noise and Serial Data Output Jitter



Conclusion

An oscillator with a phase noise plot that is equal to or lower in amplitude than the ones shown in Figure 3 on page 6 to Figure 11 on page 10, can be used as the Reference Clock Input to the HOTLink II Transmitter device. However, the reader must realize that jitter in the serial data output is the result of integration of phase noise amplitude of the reference clock at all the frequencies in the entire bandwidth. An oscillator with a higher phase noise amplitude than the illustrated sample plots at certain frequencies, but with a lower phase noise amplitude at other frequencies, may still meet the serial output jitter specification.

Table 1 on page 5 shows serial output jitter of the HOTLink II device under test for different levels of noise modulation, using the nine clock sources mentioned. Phase noise plots of these crystal oscillators are shown in Figure 3 on page 6 to Figure 11 on page 10. The plot legend specifies the corresponding noise attenuation levels of the NoiseCom box and the serial data output jitter. The device meets serial data output jitter specifications for each of the cases presented. This application note provides results that

can be used as a guideline for selecting reference clock sources to be used with the HOTLink II device.

Table 1. SDI Output Jitter Values for Oscillators Tested at Different Noise Attenuation Levels

Oscillator	Freq	Noise Attenuation	Deterministic Jitter (DJ = DCD + ISI)	Random Jitter RJ(pk-pk)	Total Jitter TJ = DJ + RJ (pk-pk)	Total Jitter Spec	Margin to Total Jitter
–	MHz	dB	UI	UI	UI	UI	%
Valpey Fisher VF161BL	153.6	127	0.1	0.098	0.198	0.35	43.42
Valpey Fisher VF161BL	153.6	27	0.104	0.164	0.268	0.35	23.42
Valpey Fisher VF161BL	153.6	23	0.105	0.243	0.348	0.35	0.57
Valpey Fisher VF161BL	125	127	0.065	0.077	0.142	0.24	40.83
Valpey Fisher VF161BL	125	29	0.062	0.127	0.189	0.24	21.25
Valpey Fisher VF161BL	125	28	0.066	0.139	0.205	0.24	14.58
Connor Winfield P143	125	127	0.065	0.079	0.144	0.24	40.00
Connor Winfield P143	125	22	0.067	0.142	0.209	0.24	12.91
Connor Winfield P143	125	21	0.095	0.144	0.239	0.24	0.41
Valpey Fisher VF161BL	106.25	127	0.048	0.069	0.117	0.21	44.28
Valpey Fisher VF161BL	106.25	31	0.051	0.122	0.173	0.21	17.61
Valpey Fisher VF161BL	106.25	28	0.051	0.155	0.206	0.21	1.90
Connor Winfield P143	106.25	127	0.049	0.07	0.119	0.21	43.33
Connor Winfield P143	106.25	17	0.049	0.121	0.170	0.21	19.04
Connor Winfield P143	106.25	15	0.050	0.156	0.206	0.21	1.90
Valpey Fisher VF140BL	27	127	0.013	0.030	0.043	0.18	76.11
Valpey Fisher VF140BL	27	24	0.015	0.055	0.070	0.18	61.11
Valpey Fisher VF140BL	27	20	0.016	0.079	0.095	0.18	47.22
Connor Winfield HSM913	27	127	0.014	0.037	0.050	0.18	72.22
Connor Winfield HSM913	27	20	0.015	0.065	0.080	0.18	55.55
Connor Winfield HSM913	27	18	0.016	0.077	0.093	0.18	57.22
Valpey Fisher VF140BL	20	127	0.011	0.033	0.044	0.16	72.50
Valpey Fisher VF140BL	20	20	0.013	0.084	0.097	0.16	39.37
Valpey Fisher VF140BL	20	16	0.016	0.132	0.148	0.16	7.50
Connor Winfield HSM943	20	127	0.011	0.030	0.041	0.16	74.37
Connor Winfield HSM943	20	16	0.019	0.116	0.135	0.16	15.62
Connor Winfield HSM943	20	15	0.019	0.130	0.149	0.16	6.87

References

1. http://www.wavecrest.com/technical/VISI_6_Getting_Started_Guides/6dataWithMarker.pdf
2. IEEE STD 802.3zTM __ 2002, IEEE Computer Society, 2002.
3. Fibre Channel---Physical and Signaling Interface, Rev 4.3, 1994
4. Single-Byte Command Code Sets CONnection Architecture, Rev 2.3, 1996
5. Cabled Distribution Systems for Television, Sound and Interactive Multimedia Signals, Part 9: Interfaces for CATV/SMATV Headends and Similar Professional Equipment for DVB/MPEG-2 Transport Streams, European Standard EN 50083-9:March 1997
6. OBSAI --Open Base Station Architecture Initiative--Reference point 3 specification, Ver 2.0, 2004
7. CYV15G0404DXB Evaluation Board User's Guide (http://www.cypress.com)

Figure 3. Valpey Fisher (VF161BL) 153.6 MHz Oscillator Vs Agilent E8251A Signal Generator

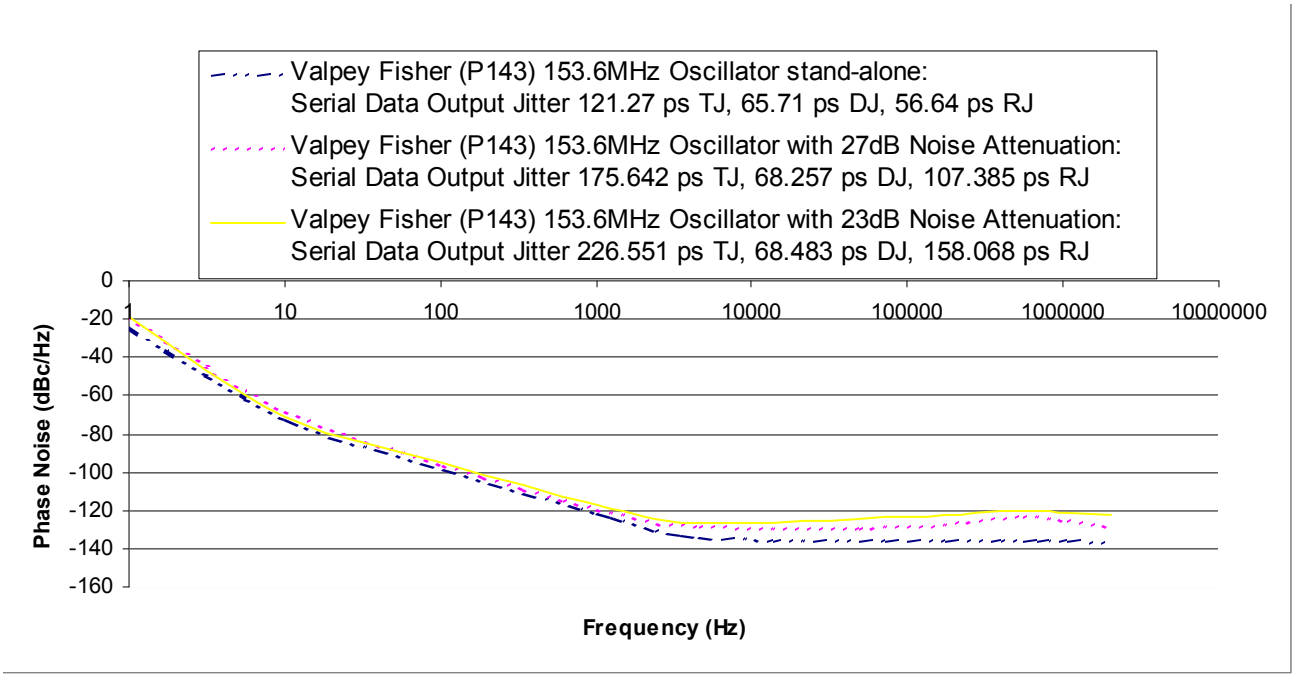


Figure 4. Valpe y Fisher VF161BL 125 MHz Oscillator Vs Agilent E8251A Signal Generator

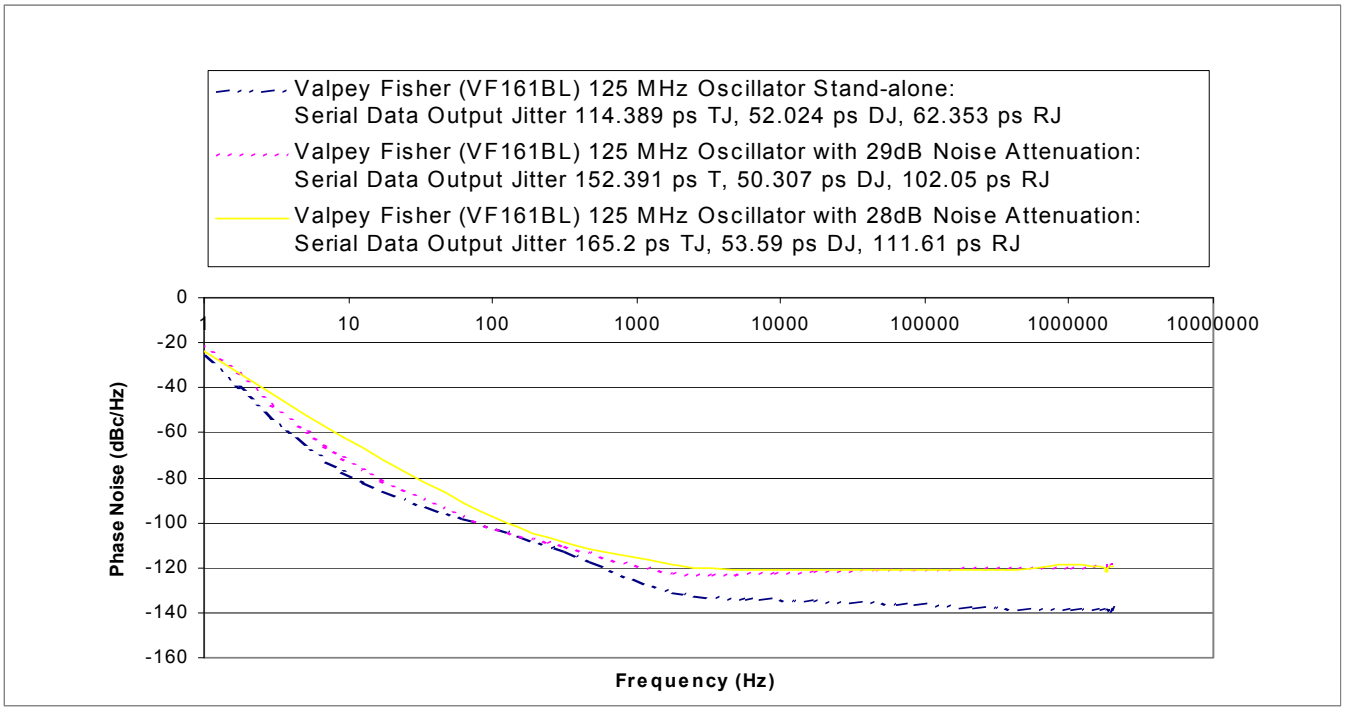


Figure 5. Connor Winfield P143 125 MHz Oscillator Vs Agilent E8251A Signal Generator

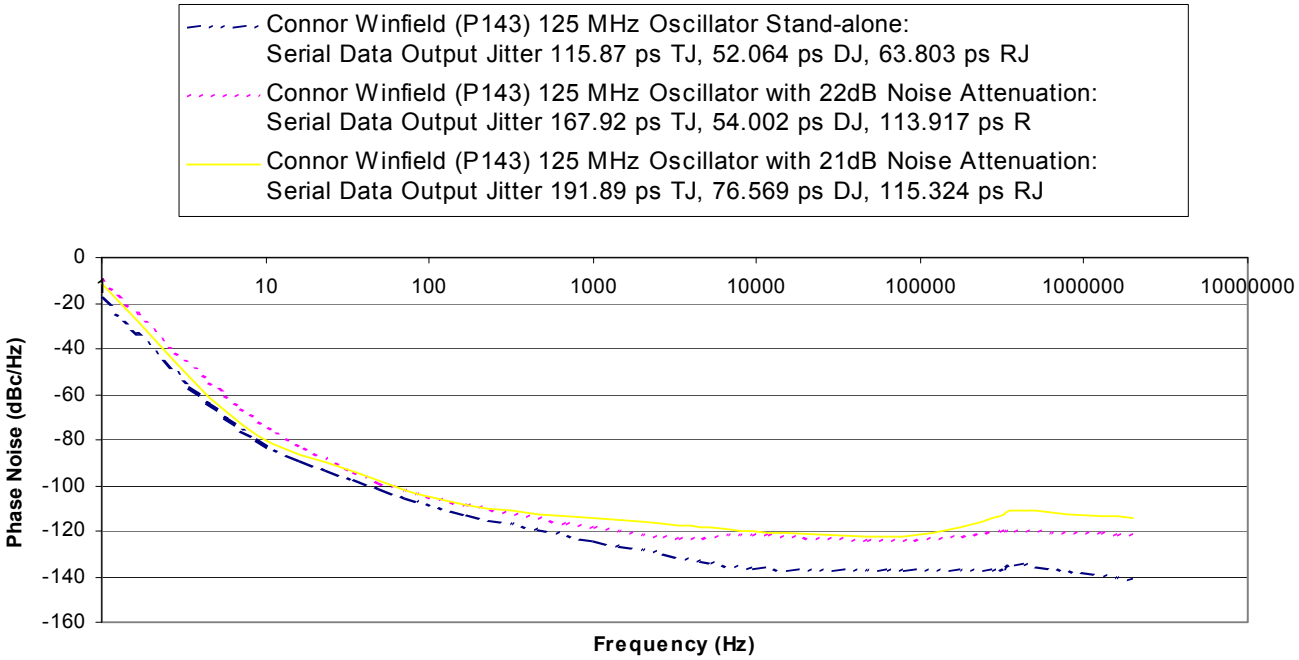


Figure 6. Valpey Fisher VF161BL 106.25 MHz Oscillator Vs Agilent E8251A Signal Generator

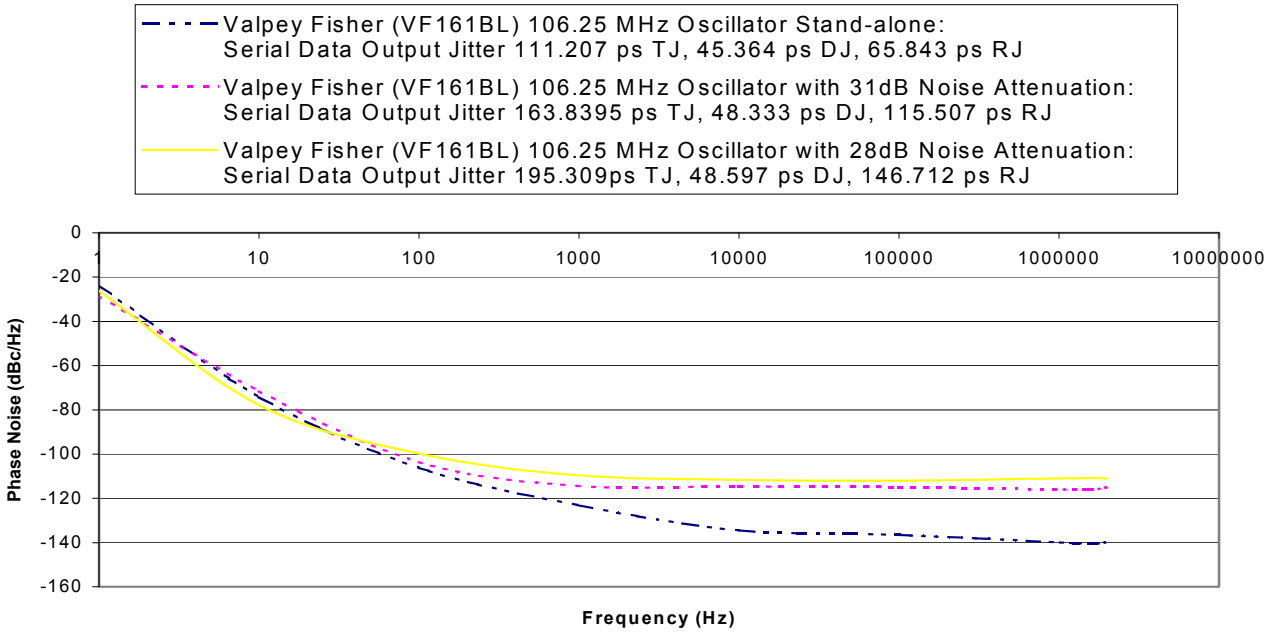


Figure 7. Connor Winfield P143 106.25 MHz Oscillator Vs Agilent Signal Generator

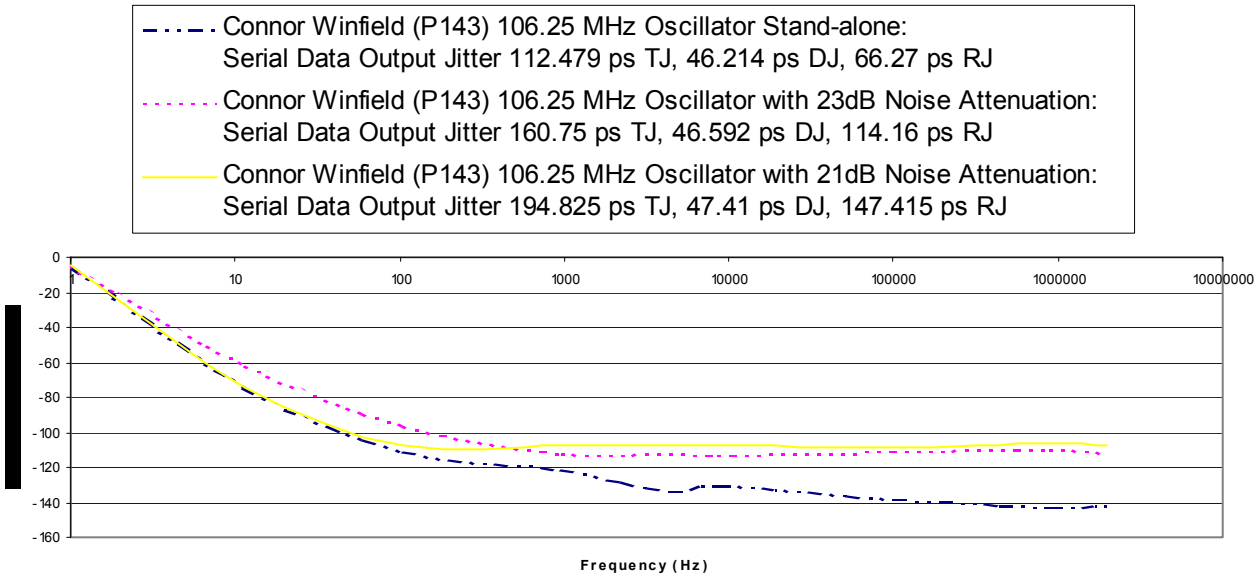


Figure 8. Valpey Fisher VF140BL 27 MHz Oscillator Vs Agilent E8251A Signal Generator

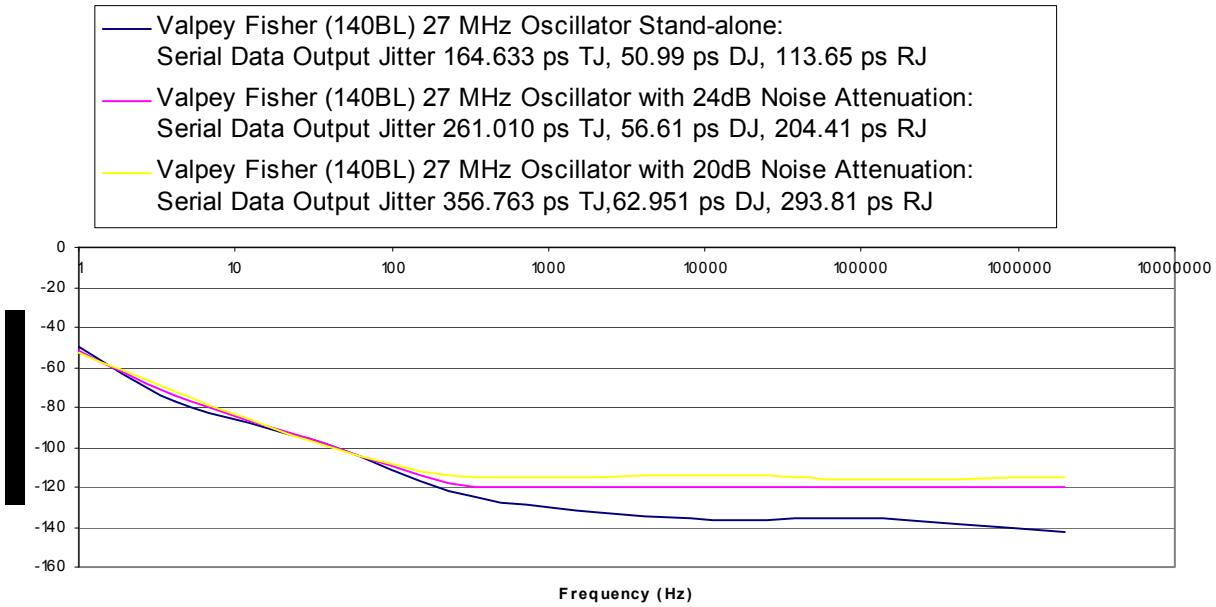


Figure 9. Connor Winfield HSM913 27 MHz Oscillator Vs. Agilent E8251A Signal Generator

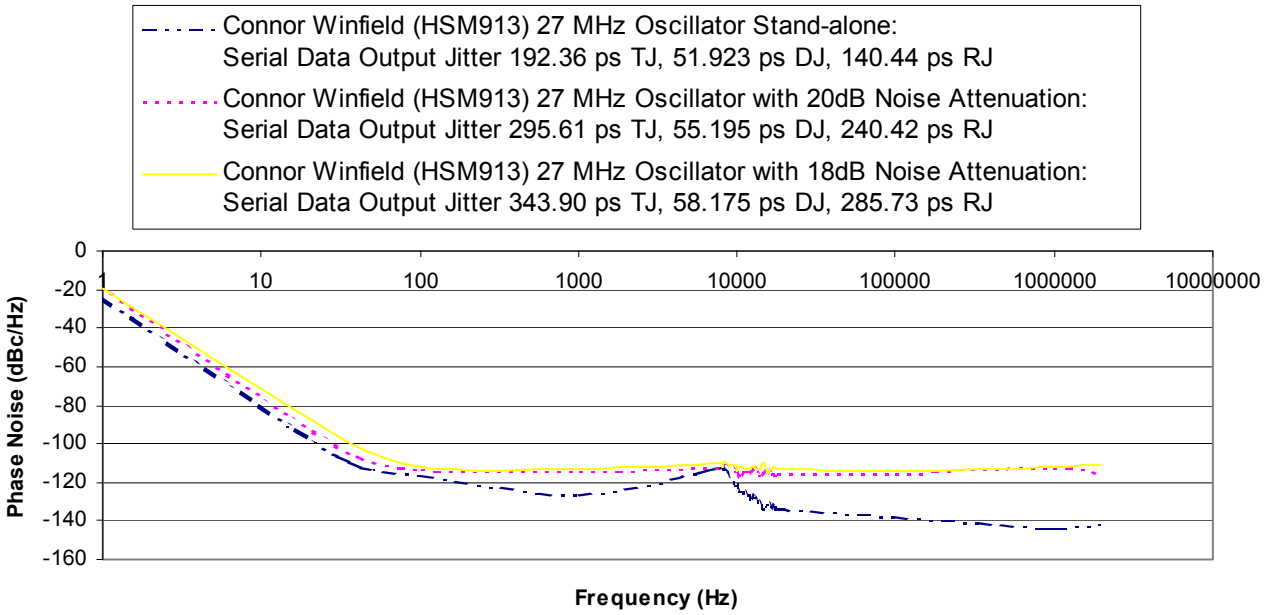


Figure 10. Valpey Fisher VF140BL 20 MHz Oscillator Vs Agilent E8251A Signal Generator

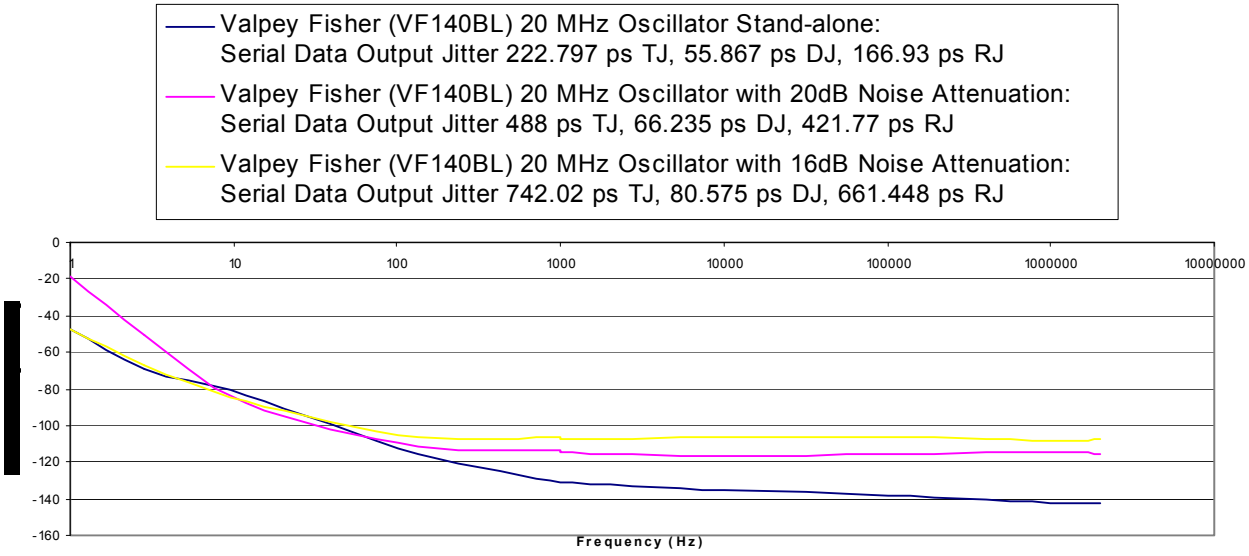
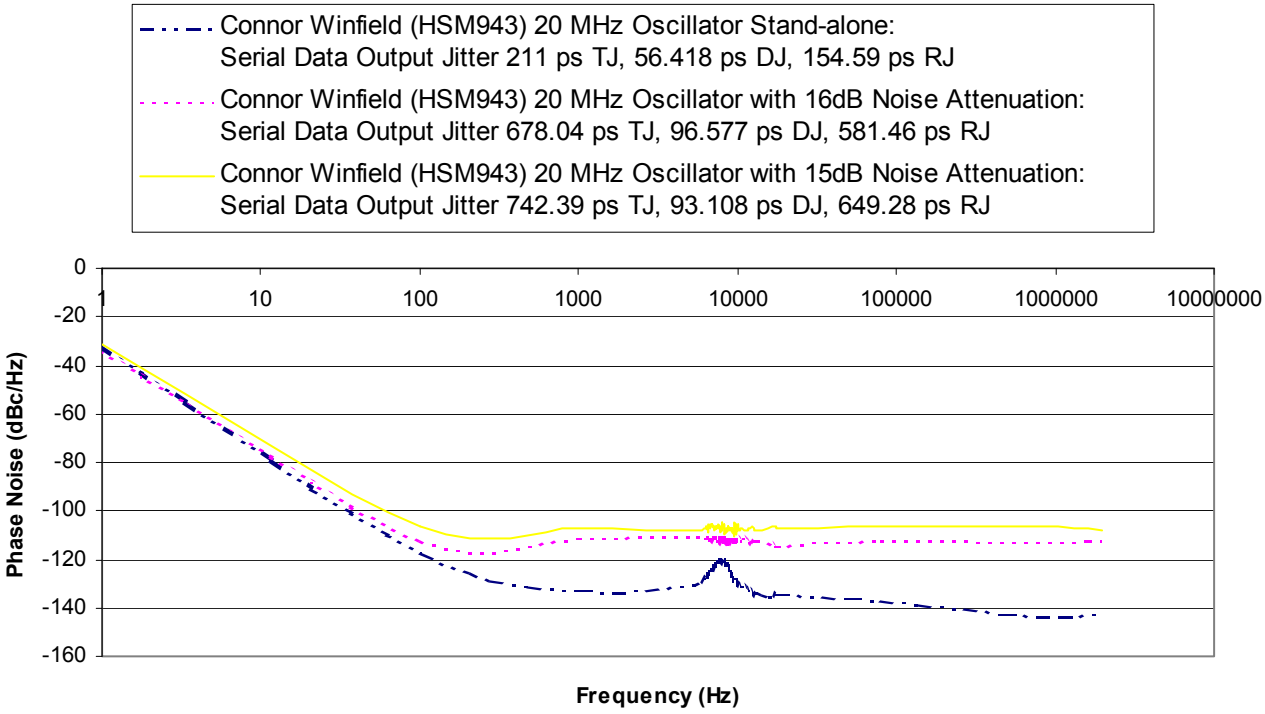


Figure 11. Connor Winfield (HSM943) 20 MHz Oscillator Vs Agilent E8251 Signal Generator



Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1000640	NVNS	04/20/2007	Existing Application Note in the web - Added Spec No. and new disclaimer and also updated the copyright date Please post in the web- overwrite the existing AN5076 file
*A	3246334	NVNS	05/04/2011	Updated in new template.
*B	4384601	NVNS	05/20/2014	No technical updates. Completing Sunset Review.

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