Guidelines for Selecting the Reference Clock Input of the HOTLink II™ Device in SMPTE SDI Video Applications - AN5073

AN5073

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Associated Project: No
Associated Application Notes: None

Abstract

The HOTLink II™ family of physical layer (PHY) devices is a point-to-point or point-to-multipoint communications building block that performs serialization, deserialization, optional 8B/10B encoding/decoding, and optional framing functions within a single device. The HOTLink-On-Demand™ family of physical layer devices, a subset of the HOTLink II family, supports video broadcast applications for both SD (Standard Definition) and HD (High Definition) SDI (Serial Digital Interface). The standards supported by the HOTLink II that define HD-SDI and SD-SDI are SMPTE 259M-CD (operating at 270 Mbps and 360 Mbps), SMPTE 292M (operating at 1.485 Gbps and 1.485/1.001 Gbps) and SMPTE 344M (operating at 540 Mbps). SMPTE standards specify a limit on the jitter present on the serial data output from an SDI. Common contributors to jitter at the SDI output are power supply noise, serial trace layout, line driver performance, performance of the TXPLL, and quality of the reference source for the TXPLL.

Introduction

The purpose of this application note is to analyze one of the contributors of jitter in the serial output, namely the phase noise present in the reference source. The bit-rate clock that clocks the shift register is a multiple of the reference clock. Hence, a portion of the jitter on the reference clock is transferred to the serial bit rate clock which in turn translates to jitter at the serial data output. This is illustrated in Figure 1 on page 2.

This document presents the phase noise of five sample clock sources for which the HOTLink II serial data output meets the SMPTE jitter specifications for both alignment and timing jitter.

The sample oscillators tested include:

1. Valpey Fisher (VF161BL) 74.25-MHz oscillator
2. Vectron (VCC6-QAB) 74.25-MHz oscillator
3. Connor Winfield (P143) 74.25-MHz oscillator
4. Micrel (SY87729) Programmable clock at 27 MHz
5. Pletronics (P1145-3S) 27-MHz oscillator

Set-up

The aim is to measure the phase noise of the crystal oscillators under three different levels of noise modulation:

1. No noise modulation.
2. Maximum noise modulation until the serial output jitter is marginally below the specifications.
3. Intermediate noise modulation that yields a serial output jitter that is in between the previous two jitter measurements.

To measure the maximum phase noise tolerated, we need a set-up that has the capability to:

- Insert and increase the noise modulation of the reference clock.
- Measure the phase noise of the noise modulated clock fed to the HOTLink II device.
- Measure serial output jitter, as per the associated standards.

The measurement set-up is illustrated in Figure 2 on page 2. The output of the crystal oscillator under test is connected to the external input of UFX7107 NoiseCom box. If the oscillator has a differential output, then the unused output is terminated to a 50 Ω load. The UFX7107 NoiseCom box is used to modulate noise into the clock generated from the crystal oscillator under test. The external modulated output of the UFX7107 NoiseCom box is connected to the external input of Agilent 8133A pulse generator. The Agilent 8133A is used for two reasons:

1. To generate a low-voltage differential output for the HOTLink II transceiver.
2. To remove amplitude noise from the noise modulated clock.

Figure 1. Serial Data Output Shift-Register Clocking Scheme in HOTLink II Transmit Path

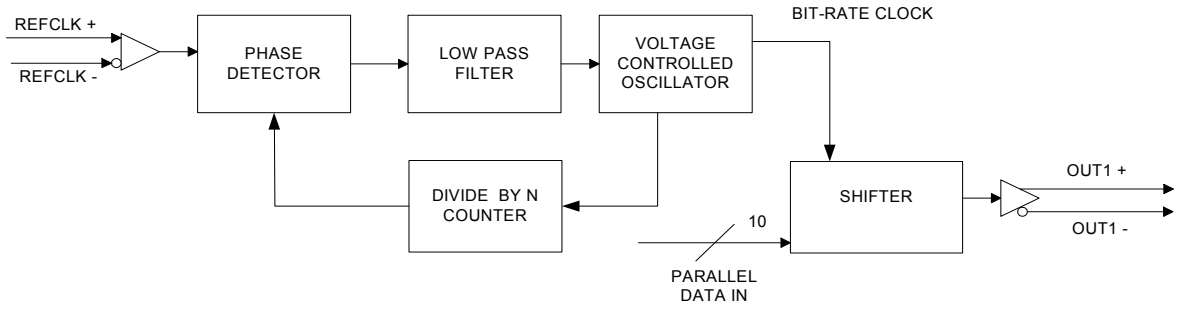
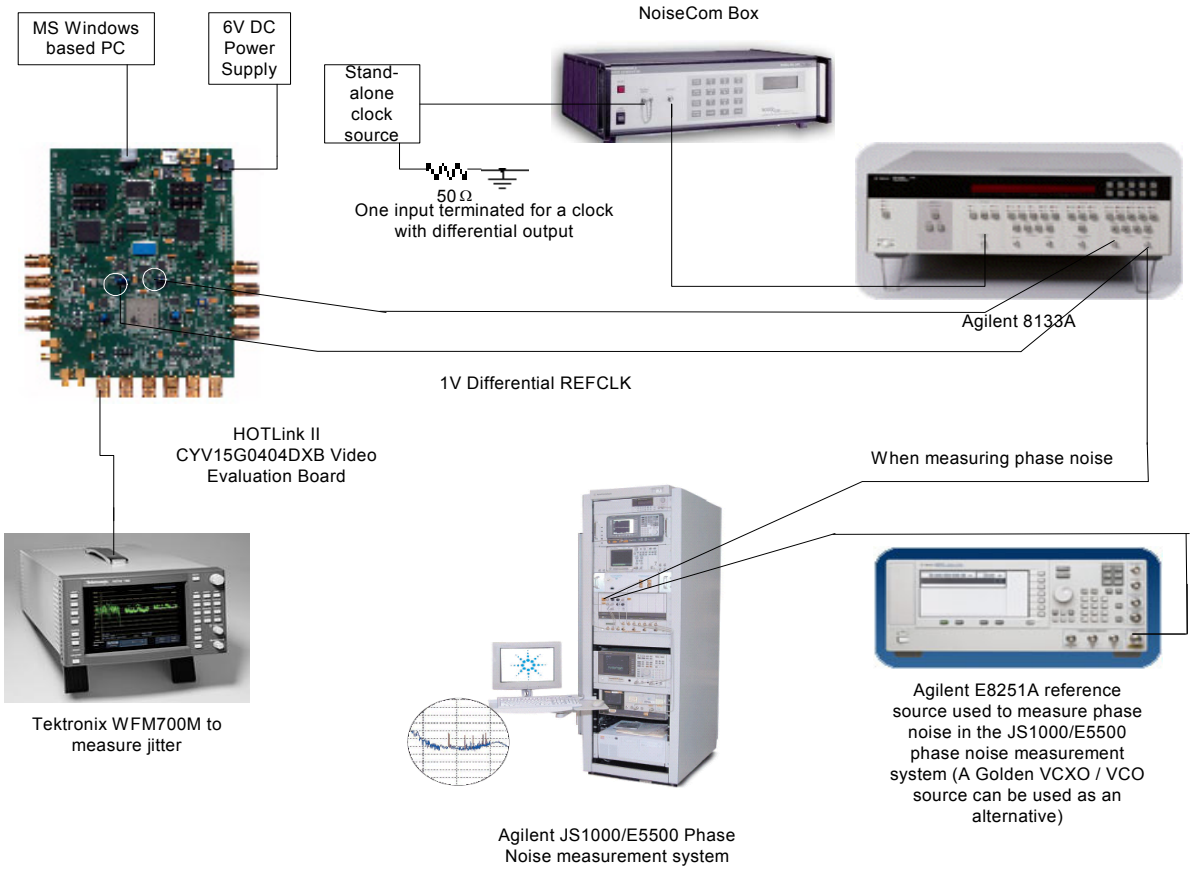


Figure 2. Set-up for Measuring Crystal Oscillator Phase Noise and Serial Data Output Jitter



The external differential output of the Agilent 8133A is fed as the reference clock to the HOTLink II transceiver in the CYV15G0404DXB video evaluation board [Reference 4]. Using the above set-up with no noise modulation, the phase noise of the standalone crystal oscillator and the clock signal obtained from the outputs of Agilent 8133A are found to be equal. Hence the presence of the UFX7107 NoiseCom box and Agilent 8133A do not affect the phase noise results in the absence of noise modulation.

This set-up will allow a noise modulated version of the crystal oscillator output to be connected as reference clock input to the HOTLink II transceiver. The CYV15G0404DXB video evaluation board [Reference 4] is connected to a Windows-based PC through a USB cable and is set to transmit color bars on the channel to which the reference clock from the Agilent 8133A is provided. The serial output of the channel under test is connected to a Tektronix WFM700M to measure the serial data output jitter.

If the measured serial data output jitter meets the specifications for both SMPTE 259M and 292M, the phase noise of the clock output from the Agilent 8133A is measured using the Agilent E5500 phase noise measurement system. The reference input to the Agilent E5500 is obtained from the Agilent E8251A signal generator. The phase noise plots of the oscillator are obtained by comparing the phase of the oscillator under test versus the Agilent E8251A. These plots are shown in Figure 3 on page 4 to Figure 7 on page 8. A Golden VCXO / VCO can be used instead of the Agilent E8251A to obtain more accurate results.

Test Procedures

Test Procedure with No Noise Modulation

In the set-up described, serial data output jitter of the HOTLink II transceiver is first measured without noise modulation from the UFX7107 NoiseCom box (maximum noise attenuation). The phase noise of the reference clock fed to the HOTLink II transceiver is then measured using the Agilent E5500 phase noise measurement system

Test Procedure with Maximum Noise Modulation

In this set-up, the noise modulation is increased (noise attenuation is decreased) and serial data output jitter is measured as above. The noise modulation is further increased until the measured jitter marginally meets the SMPTE specifications. At this point the phase noise of the reference clock from the Agilent 8133A is measured.

Test Procedure with Intermediate Noise Modulation

Using the serial data output jitter values measured from the above mentioned two methods, an intermediate jitter value is determined. Phase noise plot of the reference clock that generates this intermediate jitter is also determined. This procedure is followed for each of the following standards:

1. SMPTE 259M-C 1
2. SMPTE 292M 2

The results from the above measurements are shown graphically in Figure 3 on page 4 to Figure 7 on page 8.

Figure 3. Valpey Fisher (VF161BL) 74.25-MHz Oscillator vs. Agilent E8251A Signal Generator

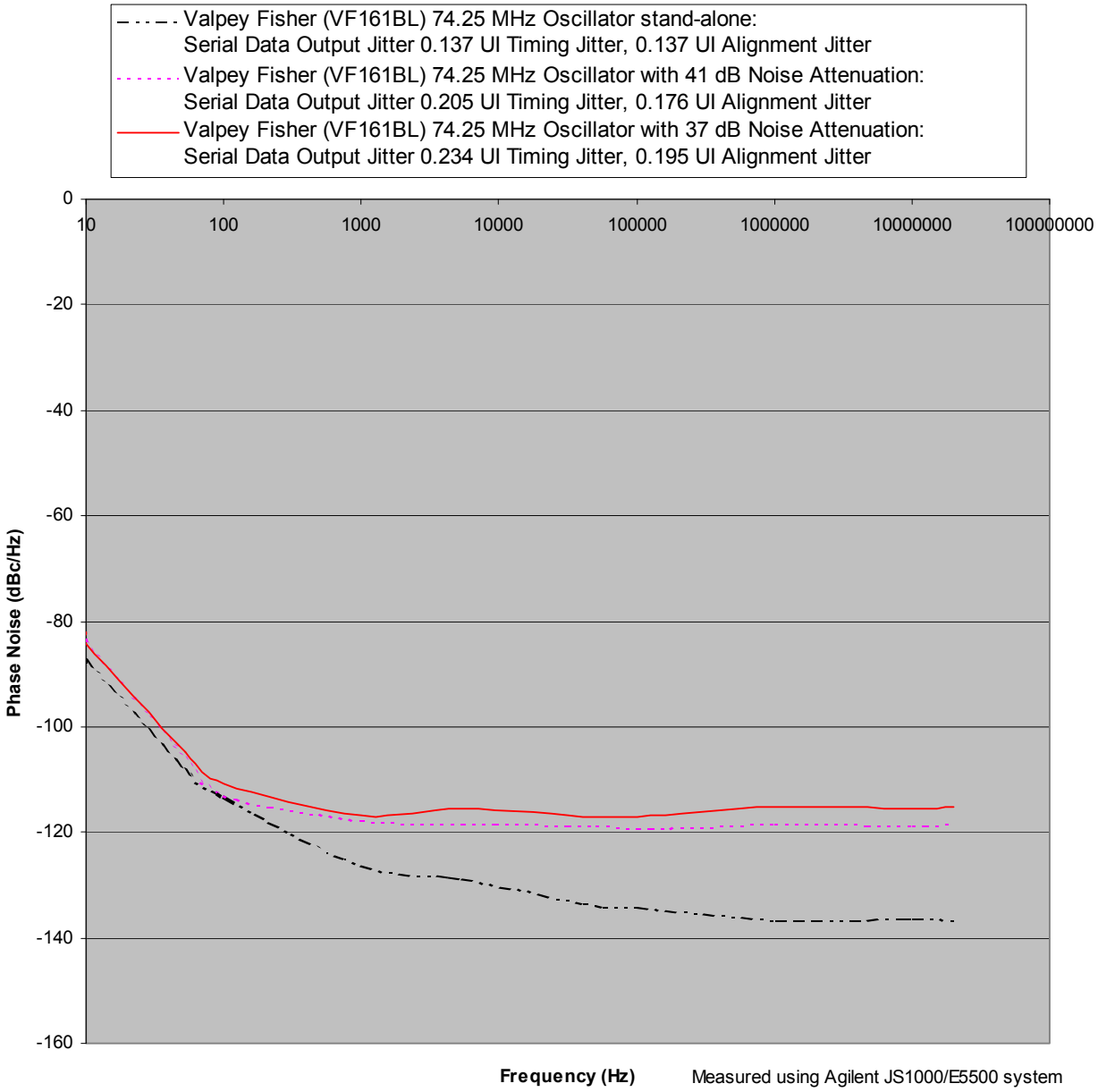


Figure 4. Connor Winfield (P143) 74.25-MHz Oscillator vs. Agilent E8251A Signal Generator

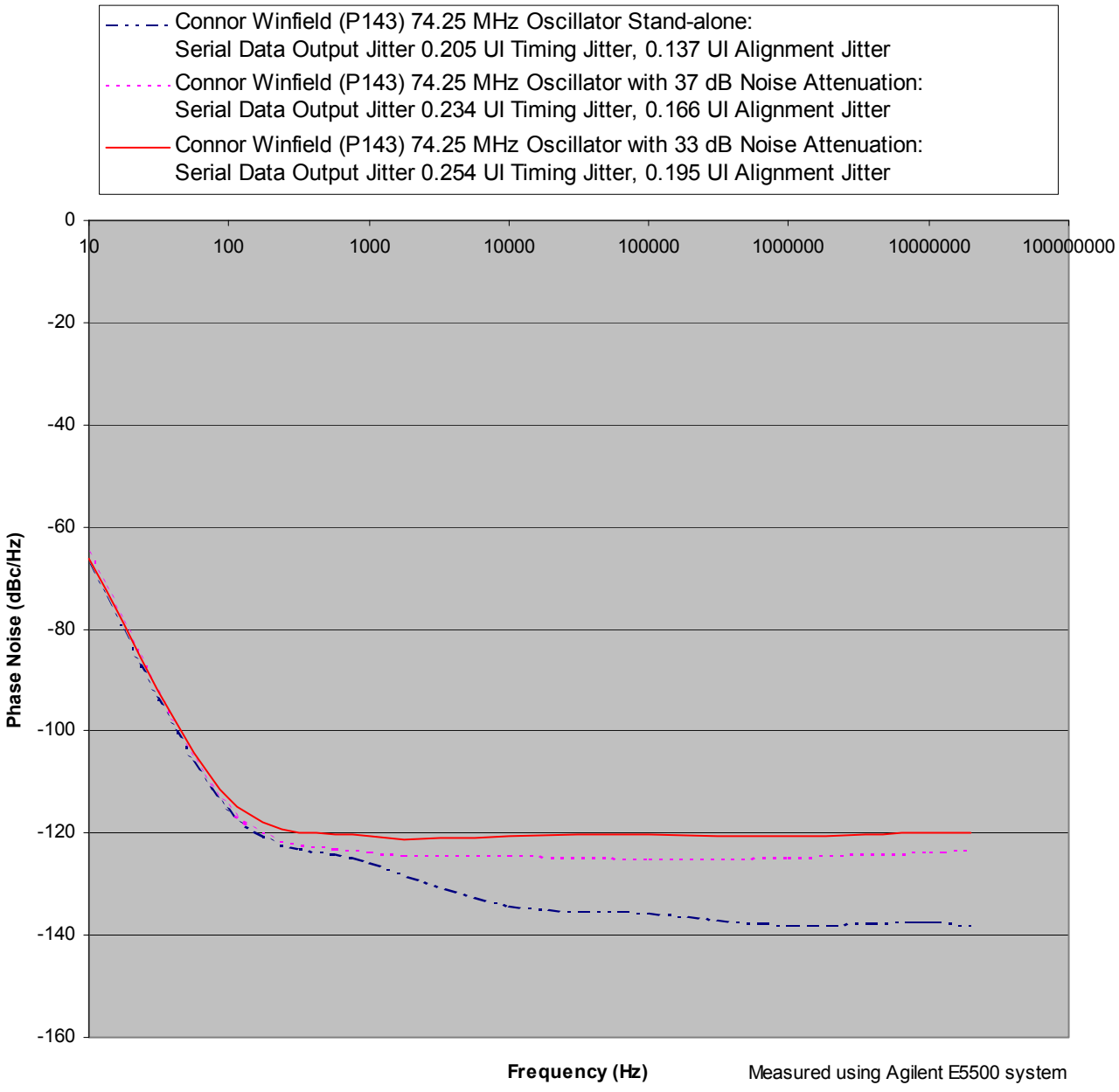


Figure 5. Vectron (VCC6-QAB) 74.25-MHz Oscillator vs. Agilent E8251A Signal Generator

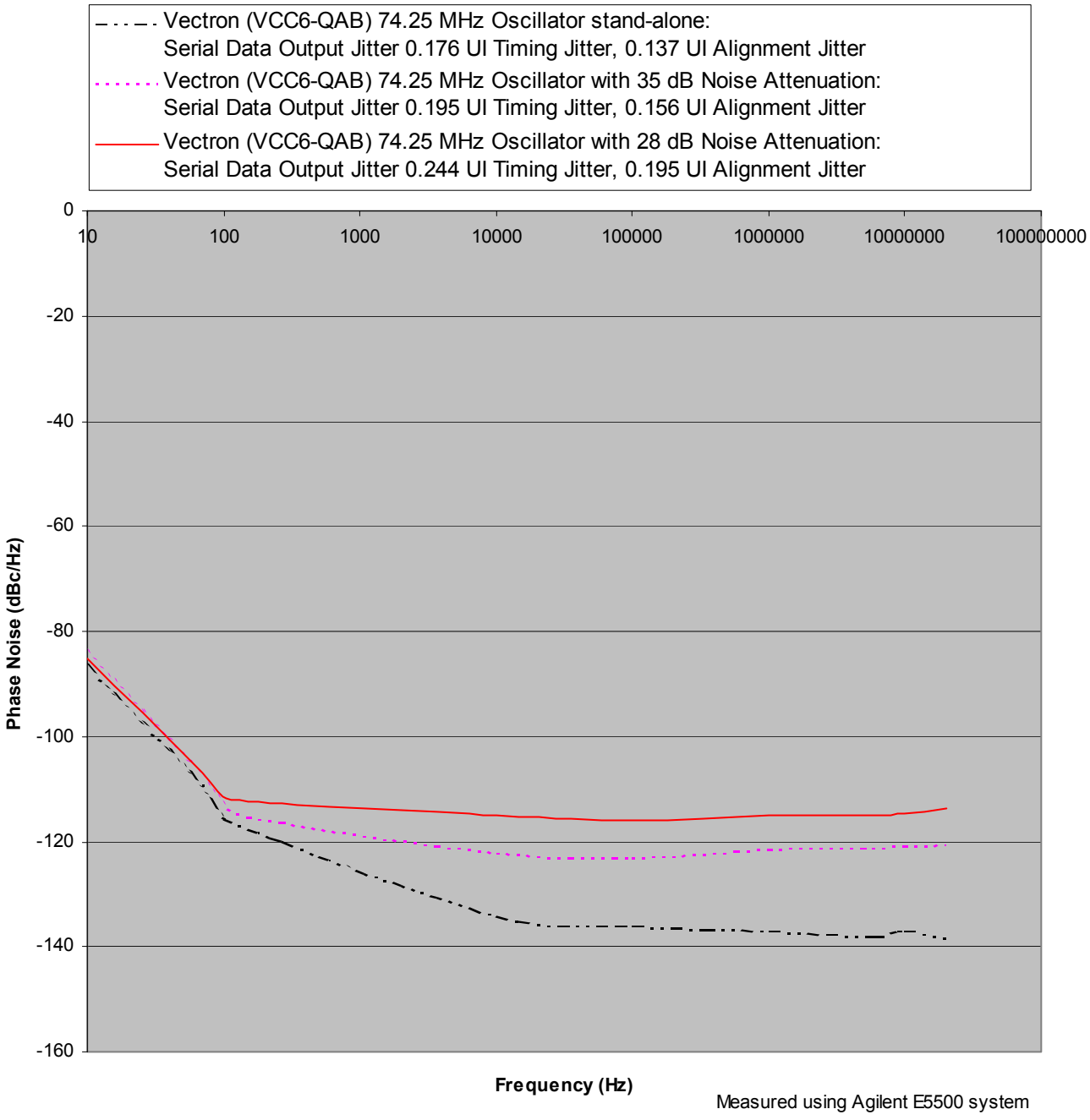


Figure 6. Micrel Programmable Clock (SY87729) at 27 MHz vs. Agilent E8251A Signal Generator

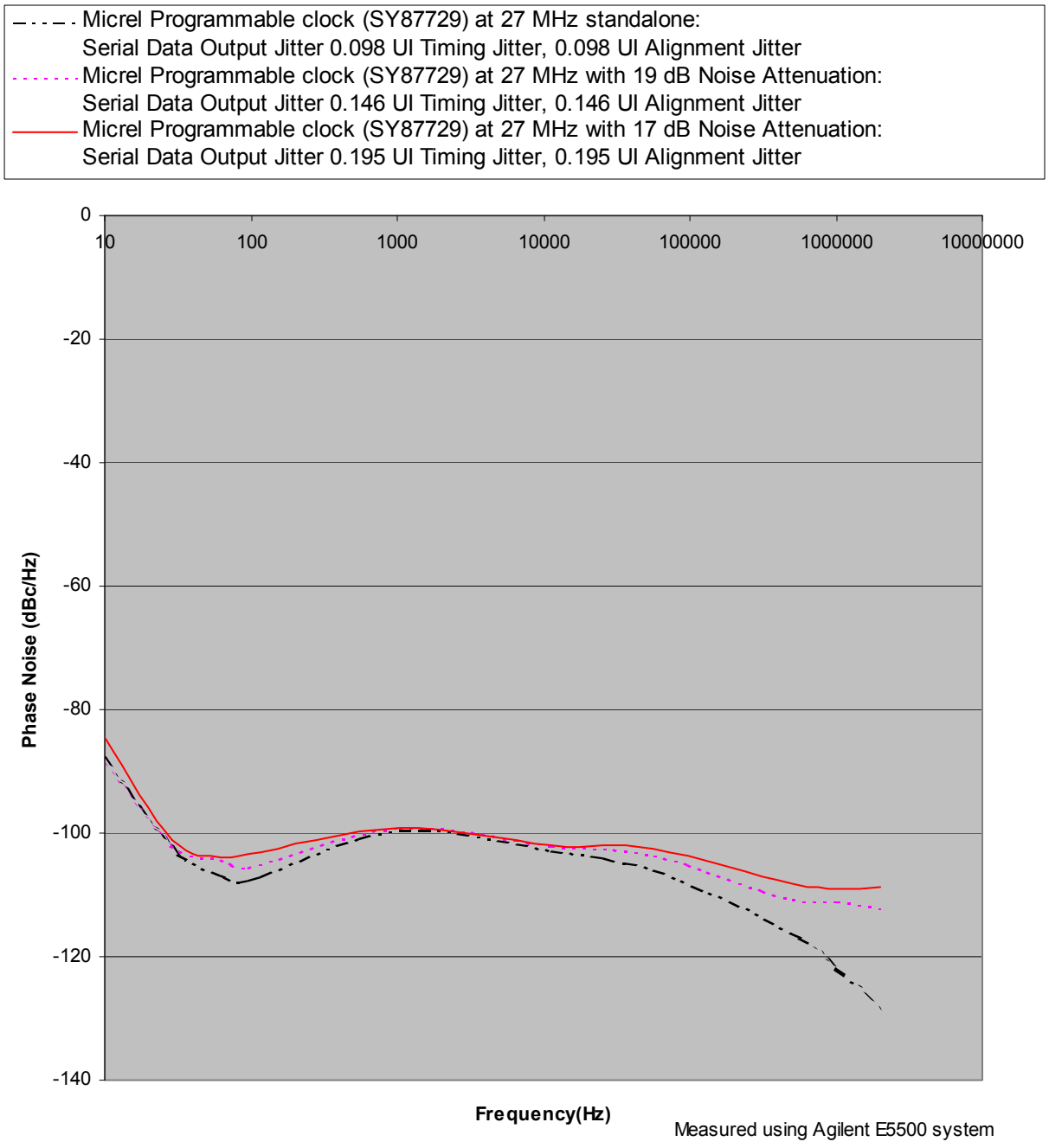
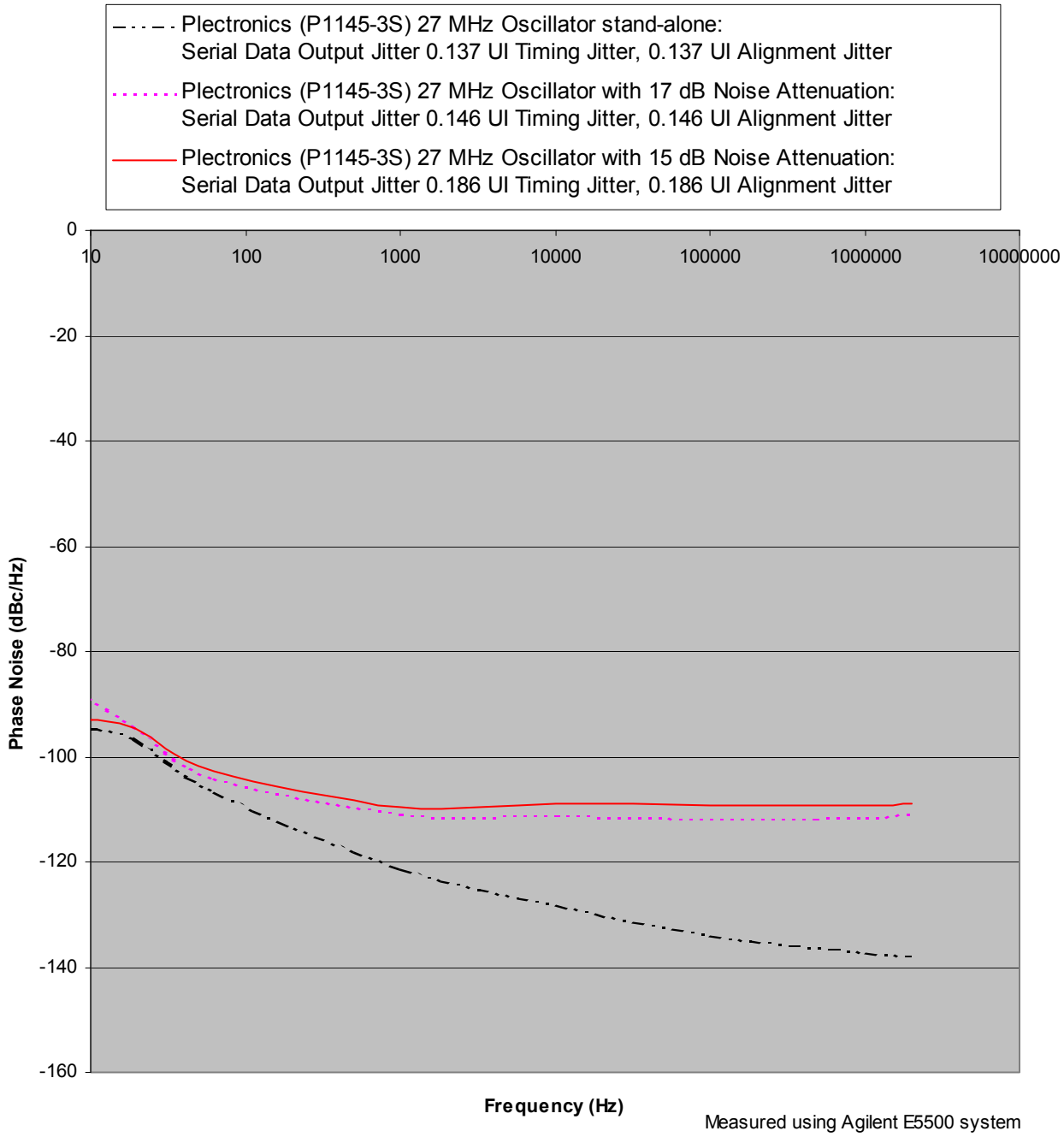


Figure 7. Pletronics (P1145-3S) 27-MHz Oscillator vs. Agilent E8251A Signal Generator



Conclusion

An oscillator with a phase noise plot that is equal to or lower in amplitude than the ones shown in Figure 3 on page 4 to Figure 7 on page 8, can be used as the Reference Clock Input to the HOTLink II Transmitter device. However, the reader must realize that jitter in the serial data output is the result of integration of phase noise amplitude of the reference clock at all the frequencies in the entire bandwidth. An oscillator with a higher phase noise amplitude than the illustrated sample plots at certain frequencies, but with a lower phase noise amplitude at other frequencies, may still meet the serial output jitter specification.

Table 1 shows the SDI output jitter of the HOTLink II device under test for different levels of noise modulation, using the nine clock sources mentioned. Phase noise plots of these crystal oscillators are shown in Figure 3 on page 4 to Figure 7 on page 8. The plot legend specifies the corresponding noise attenuation levels of the NoiseCom box and the serial data output jitter. The device meets SMPTE serial data output jitter specifications for each of the cases presented. This application note provides results that can be used as a guideline for selecting reference clock sources to be used with the HOTLink II device.

Table 1. SDI Output Jitter Values for Oscillators Tested at Different Noise Attenuation Levels

Oscillator	Freq	Noise Attenuation	Measured Timing Jitter	Measured Alignment Jitter	Timing Jitter Spec	Alignment Jitter Spec	Margin to Spec Timing Jitter	Margin to Spec Alignment Jitter
n/a	MHz	dB	UI	UI	UI	UI	%	%
Valpey Fisher VF161BL	74.25	127	0.137	0.137	1	0.2	86.3	31.5
Valpey Fisher VF161BL	74.25	41	0.205	0.176	1	0.2	79.5	12
Valpey Fisher VF161BL	74.25	37	0.234	0.195	1	0.2	76.6	2.5
Vectron VCC6QAB	74.25	127	0.176	0.137	1	0.2	82.4	31.5
Vectron VCC6QAB	74.25	35	0.195	0.156	1	0.2	80.5	22
Vectron VCC6QAB	74.25	28	0.244	0.195	1	0.2	75.6	2.5
Connor Winfield P143	74.25	127	0.205	0.137	1	0.2	79.5	31.5
Connor Winfield P143	74.25	37	0.234	0.166	1	0.2	76.6	17
Connor Winfield P143	74.25	33	0.254	0.195	1	0.2	74.6	2.5
Micrel SY87729	27	127	0.098	0.098	0.2	0.2	51	51
Micrel SY87729	27	19	0.146	0.146	0.2	0.2	27	27
Micrel SY87729	27	17	0.195	0.195	0.2	0.2	2.5	2.5
Pletronics P1145-3S	27	127	0.137	0.137	0.2	0.2	31.5	31.5
Pletronics P1145-3S	27	17	0.146	0.146	0.2	0.2	27	27
Pletronics P1145-3S	27	15	0.186	0.186	0.2	0.2	7	7

References

1. ANSI/ SMPTE 259M - 10-Bit 4:2:2 Component and 4fsc Composite Digital Signals -- Serial Digital Interface,1995
2. SMPTE 292M - for Television -- Bit-Serial Digital Interface for High-Definition Television Systems,1998
3. SMPTE 344M - for Television -- 540 Mb/s Serial Digital Interface,2000
4. HOTLink II™ CYV15G0404DXB Video PHY Demonstration Board User's Guide (http://www.cypress.com)

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1000520	NVNS	04/20/2007	Existing Application Note in the web - Added Spec No. and new disclaimer and also updated the copyright date Please post in the web- overwrite the existing AN5073 file
*A	3246334	NVNS	05/04/2011	Updated in new template.
*B	4383720	NVNS	05/19/2014	No technical updates. Completing Sunset Review.

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