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Spec No: 001-50092

Spec Title: AN5047C - MIGRATING FROM CY7C68300A TO CY7C68300C

Sunset Owner: Rich Peng (LIP)

Replaced by: 001-89897

Migrating from CY7C68300A to CY7C68300C

AN5047C

Associated Project: No
Associated Part Family: CY7C68300C, CY7C68301C, CY7C68320C, CY7C68321C
Software Version: None
Associated Application Notes: None

OBSOLETE

Application Note Abstract

This application note describes the process of migrating existing designs that use the CY7C68300A (AT2™) to the CY7C68300C (AT2LP). AT2LP is Cypress's next-generation high speed USB to ATA/ATAPI bridge. The AT2LP enhances the functionality of the AT2 and minimizes the effect on existing designs that migrate to the AT2LP. The AT2LP's backward compatibility mode enables it to be used as a pin-for-pin replacement for the AT2, with no EEPROM or board layout changes.

Overview

This application note discusses the following:

- Backward compatibility mode
- EEPROM configuration and programming
- Required crystal changes
- Forcing AT2LP into manufacturing mode
- Bus-powered operation
- USB certification

Details

Backward Compatibility Mode

The AT2LP features a backward compatibility mode that enables it to be a pin-for-pin replacement for the AT2. During startup, the AT2LP checks the I^2C bus for an EEPROM with a valid signature in the first two bytes. If the signature is 0x4D4D, the AT2LP configures itself for pin-to-pin compatibilmity with the AT2 and begins normal mass storage operation. Because the AT2LP recognizes this signature, the EEPROM does not need to be changed when using the AT2LP in an AT2-based design.

If an EEPROM with no valid signature is found on the I^2C bus, the AT2LP enters Manufacturing Mode, enabling the EEPROM to be programmed using the Cypress AT2LP manufacturing software. The valid EEPROM signatures for the various AT2LP modes are described in the AT2LP data sheet.

EEPROM Configuration and Programming

As mentioned in the previous section, existing EEPROM images can be used with the AT2LP in backward compatibility mode. To edit the EEPROM image, use the AT2 Blaster software. The format for the EEPROM contents should follow the pattern outlined in the AT2 data sheet; do not use the AT2LP format for backward compatibility mode. After the EEPROM is modified, use the AT2LP Blaster or Primer tools to program the EEPROM. The CY4615B reference design kit files contain the user guides for these tools.

Note The AT2 and AT2LP EEPROM files use different formats. Cypress provides a tool, *CfgToIIC.exe*, for converting AT2 EEPROM images into a format that the AT2LP Blaster software uses to program an EEPROM. The program and its user guide are available in the CY4615B reference design files.

The AT2 Blaster tool can be used to access the EEPROM for an AT2LP that is already running in backward compatibility mode. But for all other EEPROM programming, use the newer AT2LP Blaster tool.

Required Crystal Changes

When the AT2LP is used in an existing AT2 design, the only required BOM change is for the crystal circuit. The recommended load capacitance of the crystal used with the AT2LP is different from that of the AT2. The crystal specified for the AT2LP is a 500 µW, 24 MHz (±100 ppm, 12 pF, parallel resonant fundamental mode) crystal, and its load capacitors should be 12 pF. All other BOM items can be similar to existing AT2 designs.

Forcing AT2LP Into Manufacturing Mode

There is a convenient method available for starting the AT2LP in Manufacturing Mode. This allows reprogramming of the EEPROMs without a mass storage device attached. If the ATA Reset (ARESET#) line is LOW on power-up, the AT2LP enters Manufacturing Mode. It is recommended that a 10 k resistor be used to pull ARESET# to LOW. An easy way to pull the ARESET# line LOW is to short pins 1 and 3 on the 40-pin ATA connector with a 10k resistor, that ties the ARESET# line to the required pull down on DD7.

Unlike the AT2, disabling the EEPROM on an AT2LP does not force it to enter Manufacturing Mode. The previous method for putting the AT2 into Manufacturing Mode was to disable the EEPROM at startup, causing the chip to use the default descriptors contained in ROM space. The AT2LP supports the option of fusing some configuration data during factory manufacturing. If no EEPROM is detected at startup, it reads the fuse area of memory. When the fuse option is not used, the fuse area contains all zeros. This results in the AT2LP returning invalid configuration data and it does not enter Manufacturing Mode. To avoid this, use a blank EEPROM or an EEPROM that does not contain a valid signature. This causes the AT2LP to enter Manufacturing Mode.

Refer to the CY7C68300C data sheet for additional information on Operational Mode Selection.

Bus-powered Operation

The 56-pin AT2LP packages use the value in the bMaxPower field of the USB descriptors stored in the EEPROM to determine whether to operate in bus-powered mode. This is true even when the AT2LP is operating in backward compatibility mode. A value of 0x00 or 0x01 in bMaxpower causes the AT2LP to report as self-powered, but with a value greater than 0x01, the AT2LP reports as bus-powered.

Since the AT2 does not comply to USB-IF bus-powered requirements, the backward compatibility mode of AT2LP does not support bus-powered operation. A value of 0x00 or 0x01 for bMaxPower is the only valid setting when using AT2LP in backward compatibility mode. Ensure that the bMaxPower values are 0x00 or 0x01 in the existing AT2 EEPROM files.

USB Certification

When changing the USB controller silicon in a certified design, the USB-IF requires the certification tests to be rerun. The license agreement for the USB-IF logo requires designs that change the USB data path be resubmitted for USB certification. Questions about USB certification can be directed to the USB-IF (http://www.usb.org)

Summary

Migrating from the AT2 to the AT2LP is straightforward. Design changes are minimal, and the new features in the AT2LP enhance existing designs.

As with Cypress's AT2, the AT2LP is available with world class development tools and software support. Visit http://www.cypress.com for more information.

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Document History

Document Title: AN5047C - Migrating from CY7C68300A to CY7C68300C
Document Number: 001-50092

Revision	ECN	Submission Date	Description of Change
**	2604665	11/13/08	Migrate 001-15298 into new Cypress Document Control System.
*A	3103804	12/07/2010	Removed CY7C68300B. Changed CY4615 to CY4615B Title Changed “Migrating from CY7C68300A to CY7C68300B/C to Migrating from CY7C68300A to CY7C68300C” Hyperlink added CY4615B Reference Design kit and CY4615B Reference Design on EEPROM
*B	4194267	11/18/2013	Obsolete document. Completing Sunset Review.

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Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
Phone: 408-943-2600
Fax: 408-943-4730
http://www.cypress.com

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