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Spec No: 001-14460

Spec Title: AN5038 - MIGRATING FROM EZ-USB(R) HX2(TM) TO EZ-USB HX2LP(TM)

Replaced By: NONE

AN5038

Migrating from EZ-USB® HX2™ to EZ-USB HX2LP™

Associated Project: No
Associated Part Family: CY7C65620/30
Software Version: NA
Related Application Notes: None

AN5038 is intended to expedite the developer's learning curve regarding the migration of a CY7C65640A (EZ-USB® HX2™) design to use the CY7C65630 (HX2LP™) hub.

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Introduction

The HX2LP family is the next-generation USB high-speed hub. This family of hubs includes a two-port hub (CY7C65620) with a single transaction translator (TT), and a 4-port hub with a single TT (CY7C65630). The HX2LP family reduces the power consumption of HX2 while minimizing the effects on existing designs. This application note highlights the difference between the products and aids the designer in migrating existing designs to the HX2LP family.

Hardware Changes

This section presents information on the required changes when using either configuration of the HX2LP chip.

Multiple Configurations

The HX2LP family consists of two different configurations of the hubs with the same package and pinouts. The configurations are:

- CY7C65620: 2-port single TT hub (HX2LP 2-port)
- CY7C65630: 4-port single TT hub (HX2LP 4-port)

Both parts are in the same package with compatible pinouts between them and HX2 (CY7C65640A). This allows the designer to change the configurations without changing the board layouts. All the following comments are applicable to both of these configurations.

Changes to the Crystal Specification

With the use of HX2LP one change is required. When a crystal is used in the design, the load capacitance of the crystal must change for proper operation. This affects both the load capacitors and the crystal being used. The CY7C65640A requires a crystal with load capacitors that are between 20 pF and 33 pF. The CY7C65620/30 requires a crystal with load capacitors of 12 pF. If redesigning an HX2 application with HX2LP, the crystal must change to a load capacitance of 12 pF, and the matching load capacitors must change to 12 pF. This is a requirement of all designs using HX2LP.

The following are the crystal specifications:

- 24 MHz ± 100 ppm
- Parallel resonant
- Fundamental mode
- 500 µW drive level
- 12-pF (5% tolerance) load capacitor

Crystals compatible with this requirement, such as the FX2400026 or GC2400010 crystals, are available from eCERA ComTek Corporation.

The above specifications must be taken into consideration while selecting both the load capacitors and the crystal. Using a different crystal load capacitance with a crystal specified for 12 pF is expected to have some effect on the frequency shift. The designer should always ensure that the power dissipated by the crystal is within the crystal manufacturer's specifications. Overdriving the crystal may damage the crystal. An alternative to using a crystal is to use a low ppm resonator, such as the Murata resonator that Cypress has tested. The part number is CSTCE24M0XK2.

An article on crystal design and selection from Ecliptek's site (http://www.ecliptek.com/crystals/glossary.html) states the following:

"The rate of aging is typically greatest during the first 30 to 60 days, after which the aging rate decreases. The following factors affect crystal aging: adsorption and desorption of contamination on the surfaces of the quartz, stress relief of the mounting and bonding structures, material outgassing, and seal integrity."

Choosing the wrong capacitor will cause problems with the crystal. One of the effects of overdriving the crystal may be aging of the crystal. Another effect is a slight frequency shift. From speaking to various crystal manufacturers, we have been informed that the majority of the shift due to aging usually occurs in the first 45–60 days.

In general, the designer should always make sure that the power dissipated by the crystal is within the crystal manufacturer's recommendations.

The CY7C65640A requires a crystal with load capacitors that are between 20 pF and 33 pF, while the CY7C65620/30 requires a crystal with load capacitors of 12 pF. During some customers' development phases, they have taken an existing BOM that has a crystal with 20 pF to 33 pF and have used it to operate a CY7C65620/30 at room temperature. They reported that this does not seem to cause problems. Some have even lowered the value of the capacitor attached to the crystal to a 16-pF load capacitance. Be informed that even though the crystal with load capacitance of 16 pF or 20 pF appears to work (and most probably will work for some time), Cypress is unable to provide test reports or any test data on this, as the part was designed and tested to use the crystal as specified above.

Using a 16 pF or higher rated crystal, or any other standard load capacitance other than 12 pF, may and most probably will work as indicated by the discussions we had with various crystal manufacturers. But use this is at the customers' discretion because this will affect aging and the HX2LP part was only tested and designed for a 12-pF, 24-MHz crystal. Consult with the specific crystal manufacturer for information on the various effects of driving a crystal beyond its specified values. When a crystal is used in the design using HX2LP, Cypress recommends that for proper operation the load capacitance of the crystal should be 12 pF.

Feature Changes

An overview of the feature changes/additions in the HX2LP (CY7C65620/30) is listed below:

- Lower power
- Internal 1.8-V regulator
- Bus powered
- 0xD4 EEPROM load option
  - Dual Power Descriptors
  - Modulated Indicators
  - Power Polarity Control
  - Multiple Supported String Languages

Lower Power

The HX2LP uses a different production process than the HX2. The major result of this change is to reduce the power consumption of the chip. The lower current is obtained just by using the HX2LP with the required crystal modifications. This configuration meets all USB bus powered requirements of unconfigured current (100 mA) and suspend current (500 μA).

Internal 1.8 V Regulator

To obtain the power savings, the CY7C65620/30 uses a core that is powered from 1.8 volts. To maintain common power sources with the CY7C65640A this voltage is derived from the 3.3 V input. To properly power the internal regulator the 3.3 V input is required to have limits on the ramp rate on the power. This means the input must turn on to a valid voltage (3.0 to 3.6 volts) over a 200-μs period. This equates to an 18-volts-per-millisecond ramp rate. Powering the input up too quickly will latch the internal regulator and cause problems powering up the core. Many 3.3-V regulators have a turn-on time that is long enough to properly power up the internal regulator. One such regulator is the LT1763CS8-3.3.

Bus Powered

The HX2 power consumption does not allow for a bus-powered configuration. The HX2LP power consumption does permit the possibility of configuring the part for bus-powered operation. The maximum power consumption for the HX2LP hub controller in a configured mode will use more than a 100-mA allotment. This limits the amount of power for downstream ports. Therefore, implementing one less downstream port does configure the hub in a mode that fits within the power allocations for bus-powered hubs. A two-port hub (up to three ports) is a configuration that fits the power allotment of 500 mA for the hub (200 mA for the hub controller and 100 mA for each available downstream port with a limit of three ports).

To enable the hub to enumerate properly, pin 45 was changed from a V_{CC} pin to SELFPWR. If it is connected in an existing design it will be a high input, which puts the chip in the self-powered mode. If this pin is connected to a low input (Ground) then the part will be in a bus-powered mode.

0xD4 EEPROM Load Option

The 0xD4 EEPROM load option was added to enable additional features within the HX2LP. These features include multiple power consumption values for full-speed and high-speed modes, power control polarity, over current polarity, over current reporting modes, and multiple string language support.

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Dual Power Descriptors

The first of these features is the ability to load power consumption parameters for the hub's descriptor for both full-speed and high-speed modes. The entries of MaxPower (for both hub and ports) and HubControllerPower (for hub only power) now have an entry for full speed and another one for high speed.

Modulated Indicators

The second feature that was added was additional control bits in a second control byte value. This second byte allows the EEPROM to define whether the hub has the ability of being self powered. This allows the hub to switch between self power and bus power via the SELFPWR pin.

The control byte also allows for additional power savings via LED indicators. This bit, if set; will modulate the LED indicators with a square wave instead for turning them on. This feature will reduce the indicators' power consumption by half.

Power Polarity Control

The third feature within this control byte is the ability to control the polarity of both the power control pins and the over current input pins. Additionally, this new control byte gives the ability to disable the over current detection or to gang the port's status.

Multiple Supported String Languages

The last item added to this load option is the ability to add multiple string language support. The EEPROM contains up to 31 languages. See the CY7C65620/30 datasheet for more details.

Summary

When changing components such as the USB controller, the USB-IF will require the certification test to be rerun. The USB controller and the board traces will have the most effect on the electrical characteristics of the device and therefore the USB-IF will require the device to be retested.

This application note has introduced you to the differences between the HX2 and the HX2LP. As discussed in this application note, the only change required when using the HX2LP in place of the HX2 is the alteration of the crystal load capacitors and the load capacitance of the crystal. With exception of the load capacitance on the crystal, the crystal for the HX2LP contains the same requirements as that for the HX2. Additional features are also highlighted, but are defaulted to function as the HX2 would. This enables use of HX2LP in prior designs without changes to the board layout.

As with Cypress' HX2, the HX2LP is made available with world-class development tools. Visit www.cypress.com for more device details and datasheet information.

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Document History

Document Title: AN5038 - Migrating from EZ-USB® HX2™ to EZ-USB HX2LP™

Document Number: 001-14460

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	919660	VED	04/06/2006	New Application Note.
*A	1641210	XSG	12/18/2007	OLD APP. NOTE: Updated copyright. Revision disclaimer. Added Samples Request Form link in Associated Part Family in page 1.
*B	3121916	DBIR	12/28/2010	Updated to new template.
*C	3483803	DBIR	01/05/2012	Converted from FrameMaker to Word. No technical updates. Updated to new template.
*D	4591434	DBIR	12/09/2014	Updated to new template. Completing Sunset Review.
*E	5836309	GNKK	07/28/2017	Updated the Cypress logo and copyright information.
*F	6065614	HBM	02/14/2018	Obsolete document

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