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Spec No: 001-49150

Spec Title: AN49150 - SCHEMATIC AND LAYOUT REVIEW CHECKLIST FOR HX2LP

Replaced by: 001-72332

AN49150

Schematic and Layout Review Checklist for HX2LP

Author: Vihang Trivedi
Associated Project: No
Associated Part Family: CY7C65620, CY7C65630
Software Version: NA
Related Application Notes: AN5044

AN49150 discusses the schematic and layout review checklist for the EZ-USB HX2LP™ family.

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Introduction

The Cypress CY7C65620 and CY7C65630 USB 2.0 hubs are high performance, low cost solutions for USB. The CY7C656xx USB 2.0 hubs integrate 1.5 kΩ upstream pull-up resistors for host notification. All downstream 15 kΩ pull-down resistors and series termination resistors are also integrated by the hubs on all upstream and downstream D+ and D- pins. This results in system cost optimization by providing built in support for the USB 2.0 specification.

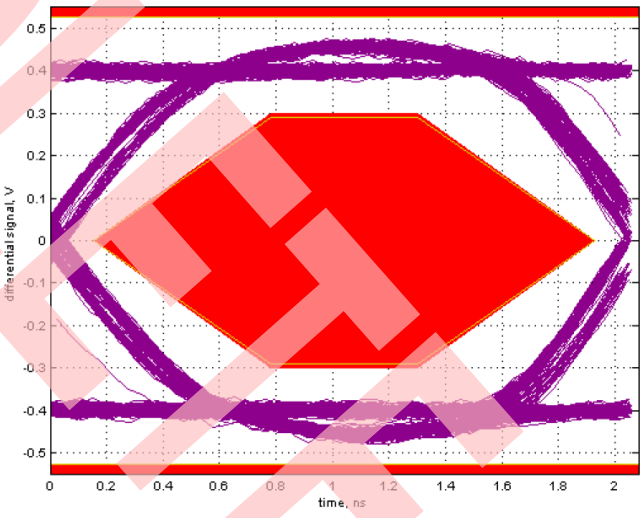
Hardware Considerations

The hardware considerations for using HX2LP in your design are as follows.

Trace Length and Width

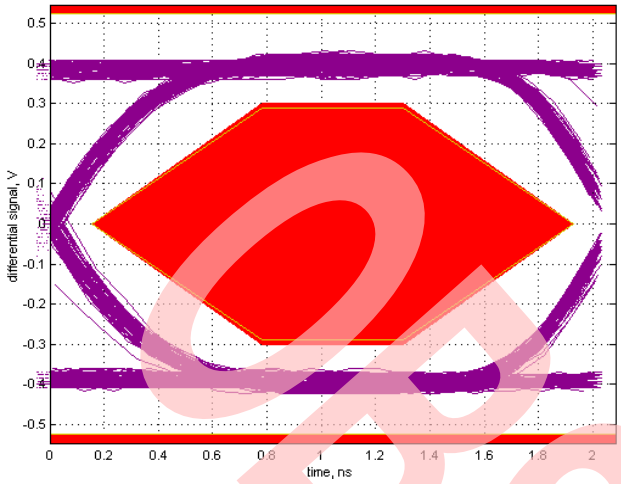
- It is important to check the data lines (D+ and D-) and verify how the traces are laid out and to which part they are nearer. Make sure they stay within the impedance matching.
- The trace length and width, and their impedance matching play a significant role in signal quality. Figure 1 shows the eye diagram results of the high speed signal quality test of a two layer board with thin and short traces; no impedance matching is performed. The traces' lengths are less than an inch. It passes the test, although it shows overshoot and undershoot in the eye diagram that causes excessive voltages. The eye diagram also shows phase differences between the two traces resulting in jitter.

Figure 1. Eye Diagram Result 1



- Figure 2 shows the eye diagram results of the high speed signal quality test of a four layer board with long traces; impedance matching is performed. The traces' lengths went up to about 9 inches. It passes the signal quality test and the eye diagram did not show any overshoot or undershoot (Figure 2).

Figure 2. Eye Diagram Result 2



Crystal Requirements

The crystal is one component that must be checked thoroughly. Some requirements such as crystal drive strength are often overlooked. This indicates how much power the crystal can tolerate. A crystal with a low drive level may result in accelerated aging or may burn out and not function.

Also, load capacitance is not in the normal parallel design. In a parallel design with equal load caps, load rating minus the stray capacitance is taken. The result is doubled to arrive at the load capacitance. This means that for a 12 pF load rating with 3 pF stray capacitance, there are 18 pF capacitors. However, this part uses a crystal with a load capacitance rating of 12 pF and still requires both these capacitors to be 12 pF. In a normal parallel design, you end up driving more than 500 µW into the crystal. Depending on the crystal, it may age early or burn out.

This is not a typical crystal design, but it works perfectly for the chip. It is slightly off the center frequency but maintains a lower drive power into the crystal and still stays within the bit rate specification from the USB-IF.

Following are the parameters to remember when selecting the crystal:

- 12 pF rating on the crystal
- 24 MHz ± 0.05%
- Parallel resonant, fundamental mode
- 12 pF capacitors for load caps
- 500 µW drive

The 500 µW value is the power that is driven into the crystal. This rating is typically overlooked, with designers using 100 µW or 10 µW, which is not allowed.

Power Requirements

Downstream Power Switching

The downstream port power of the hub is allowed to have different configurations according to the USB specification. One basic requirement is that all ports must be protected. Most vendors use a power switch to do that. They have a current limit of 500 mA. In the case of low cost hubs, designers use a fuse to meet this requirement. Other options are ganged power and individually controlled power.

The over current inputs in its default configuration need a pull-up resistor and most switches do not have an internal pull-up resistor. A pull-up resistor is required only if you are doing an active low on the signal. If the over current is high, then a pull-down is required. Each port must have some capacitance, according to the USB 2.0 specification, (minimum of 120 µF). Otherwise, enough current is not supplied at in-rush time to the device. Each capacitor must have enough out-rush current to be able to supply enough in-rush current to the device, while maintaining voltage levels to the device.

3.3 V Regulator

It is important that the power from a 3.3 V regulator is noise free. If the circuit does not have sufficient bypass capacitors on the chip, then the noise generated by the switching frequency of the regulator shows up on the eye diagram as jitter. The specific recommendations for ceramic capacitors nearest to the regulator are mentioned in Table 1 of AN5044.

VBUS Power Monitoring

The hub chip has a VBUS pin called VBUSPower. This pin must be connected to VBUS through a resistor bridge to ground. The resistor to ground allows the power to bleed when you unplug the hub; otherwise, it still considers the hub as connected. The hub may be powered by the host supply (that is, designed with the host and only D+ and D- routed). In this case the hub is powered when the host is on and switched off when the host is off. In this case, it is best to tie the VBUSPOWER pin to the reset pin and have it high only after reset.

Reset Design

One use of the VBUS pin is to inform the hub chip when the cable is connected to the upstream port. If the cable is hardwired and no longer removable and the power is directly derived from the upstream power source, it is better to tie the VBUS power pin to the reset pin. This helps to avoid issues with the delays on the regulators.

SPI Interface

SPI_SD line must be pulled low using a 15 kΩ pull-down resistor.

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Debugging HX2LP Chips

To bring up the HX2LP chips, the board must have the load capacitors for the crystal, the crystal itself, and pull-up resistors for the over-current attached to the HX2LP. This must be the minimum amount of hardware provided on the board to enumerate as a hub. It brings up the chip in its default hub configuration because the board does not have an EEPROM assembled on it.

After the communication between the host and hub is established, the next step is to attach an EEPROM with its external resistors so that you can test the programming of the EEPROM. If a blank EEPROM is connected initially, the hub chip enumerates as a vendor specific device and not a hub. After that you can program the EEPROM using the Blaster program from the CY4605/4606 kits and enumerate it as a hub defined by the EEPROM configuration by cycling the power to the hub. When this is done, start adding the downstream components to the hub to finish the rest of the circuit design.

Summary

This application note helps you to produce a compliant high performance USB 2.0 hub design. It also provides an overview of probable design issues and remedies.

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Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2572965	VGT	09/30/2008	New application note.
*A	3468951	DBIR	12/19/2011	Updated Hardware Considerations: Updated Power Requirements: Added SPI Interface. Updated to new template.
*B	4590229	DBIR	12/09/2014	Updated to new template. Completing Sunset Review.
*C	5812859	AESATMP9	07/12/2017	Updated logo and copyright.
*D	6079663	HPPC	02/23/2018	Sunset Review Obsoleted

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