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Spec No: 001-44208

Spec Title: AN44208 - CAPSENSE(R) EXPRESS(TM) - I2C COMMUNICATION TIMING ANALYSIS

Replaced by: None

AN44208

CapSense® Express™ - I²C Communication Timing Analysis

Associated Project: No
Associated Part Family: CY8C201xx
Software Version: PSoC Designer 5.0 SP6
Related Application Notes: For a complete list, click here.

To get the latest version of this application note, or the associated project file, please visit http://www.cypress.com/go/AN44208.

This application note provides the I²C timing requirements for CY8C201xx CapSense® Express™. It includes information on boot up time of the CapSense Express device, time to execute different configuration commands, time to enter sleep and deep sleep modes, and wakeup time.

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1 Introduction

CapSense Express provides a multifunctional, flexible, and cost effective solution for low I/O capacitive sensing applications. It supports I/Os configurable as capacitive sensing inputs or as GPIOs for LED drive, interrupt output, wakeup on interrupt input, and other digital I/O functionality. The device supports I²C serial communication interface.

The I²C bus is an industry standard, two-wire hardware interface developed by Philips. The master device initiates communication with the slave device. This supports data transfer at byte-by-byte level, where the slave device acknowledges the master after every byte is processed successfully. The data transfer is initiated with a start condition, followed by slave address, data to read or write, and stop condition.

2 Overview

This application note provides the following details:

- I²C background information
- Format for register read and write
- Setup and Normal modes of operation
- Write acknowledgment time in Normal mode
- Read acknowledgment time in Normal mode
- Read/Write acknowledgment time in Setup mode
- Non accessible time of CapSense Express after acknowledgment
- Boot up time for CapSense Express
- Time to enter sleep and deep sleep modes
- Wakeup time from sleep and deep sleep modes

2.1 I²C Background Information

2.1.1 Clock Stretching Mechanism

In I²C communication protocol, when the master reads or writes from or to the slave bytes, a situation known as “clock stretching” or “bus stalling” may occur. This happens if the slave cannot receive or transmit another complete byte of data until it has performed some other function such as servicing an internal interrupt. In such a situation, the slave can hold the clock line SCL LOW to force the master into a wait state, thus effectively “stalling” the bus (or “stretching” one clock from the master). Data transfer continues when the slave is ready for another data byte and releases clock line SCL.

2.1.2 CapSense Express as Slave

When a master device communicates with the slave CapSense Express device, the slave device stalls the I²C bus at each byte until processing of the byte is complete and any critical internal function is executed. In an I²C write operation, CapSense Express releases the SCL line and sends an ACK only when it is ready to receive another byte. If the master is fully I²C compliant, it supports the forced wait state and stops transmission until the SCL line is released and an ACK is received.

If the master is not fully I²C compliant, the master must wait for a specific amount of time before sending the next byte. In such systems, the master does not wait for an acknowledgment from the slave and continues to communicate even if the slave (CapSense Express device) is stalling the bus, often resulting in erroneous communication.

The objective of this application note is to provide a detailed analysis of the read and write acknowledgment time of the registers. This enables to program the master to wait for a specified amount of time to get the acknowledgment. For details on registers, refer to the CY8C201xx Register Reference Guide.

2.1.3 Test Environment for Timing Analysis

Master Device: PSoC® device CY8C2744324PXI

Slave Device: CapSense Express CY8C20110

For I²C speed of 100 Kbps, the slave configurations analyzed in Normal and Setup modes with pulse width modulator (PWM) output enabled for GPIO are:

- 10 CapSense buttons
- 5 CapSense buttons and 5 GPIOs with PWM functionality enabled for GPIO

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2.2 Format for Register Read or Write

Register write format. Write, device address, register address, data, data, and so on.

Slave addr +W	Ack (S)	Reg. addr	Ack (S)	Data	Ack (S)	Data	Ack (S)

Register read format. Write, device address, register address, read, device address, data, data, and so on.

Slave addr +W	Ack (S)	Reg. addr	Ack (S)	Slave addr +R	Ack (S)	Data	Ack (M)

S: acknowledgment from slave

M: acknowledgment from master

2.3 Setup and Normal Modes of Operation

2.3.1 Normal Mode

In Normal mode of operation, the acknowledgment time is optimized. The timings remain approximately the same for different configurations of the slave.

To reduce the acknowledgment times in Normal mode, the registers 0x08, 0x09, 0x0C, 0x0D, 0x10 to 0x13, 0x14 to 0x17, 0x57 to 0x60, and 0x7E are given only read access. Write to these registers must be done in Setup mode.

2.3.2 Setup Mode

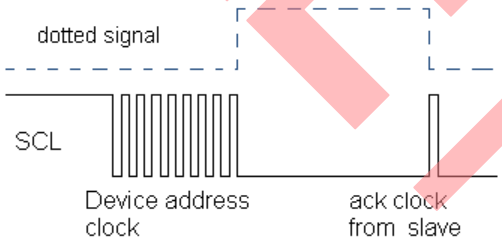
All registers have read and write access (except those which are read only) in this mode. The acknowledgment times are longer compared to Normal mode.

When CapSense scanning is disabled (command code 0Ah in command register A0h), the acknowledgment times can be improved to values similar to the Normal mode of operation.

2.3.3 Device Address Acknowledgment Timing

The device address acknowledgment time is measured separately from the register acknowledgment times and results are tabulated in Table 1 (Normal operating mode) and Table 3 (Setup operating mode). In Figure 1, the timing of high (dashed signal) shows the time to receive acknowledgment from slave after sending the address. This time remains approximately the same across different configurations of the slave.

Figure 1. Address Recognition Time



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2.4 Write Acknowledgment Time in Normal Mode

Write acknowledgment time is the time required by CapSense Express to acknowledge the data received, as shown in Figure 2. The dotted (high) signal shows the write acknowledgment time. Write acknowledgment time is different for different registers in the Normal mode. Table 1 gives the details of acknowledgment times for all registers.

All configurable registers are characterized in groups where the set of registers in the same group has the same acknowledgment times in Normal mode.

Table 1. Write Acknowledgment (Ack.) Time in Normal Mode with PWM Functionality Enabled for GPIO.

Register Details	Ack. Time (in µs)	
	Max (5 Button-5 GPIO)	Max (10 Button)
Device address ack. time	100	100
GPIO status registers (04h–05h)	100	100
GPIO operation settings (1Ch–4Dh)	120	120
Scan position, finger threshold, and IDAC settings(57h–74h)	140	140
CapSense read back (81h–89h)	120	120
Other configuration registers	110	100
Command register A0	100	100

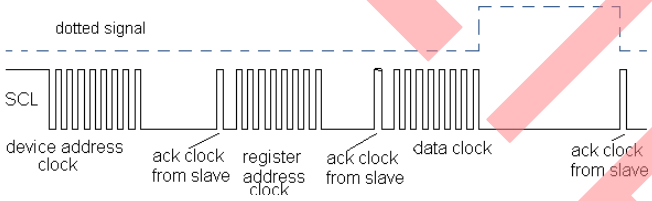
Note Read only registers in Normal mode are 00h-03h, 06h-09h, 0Ch-0Dh, 10h-17h, 50h-51h, 57h-60h, 7Ah-7Bh, 7Eh, and 82h-8Ch. To optimize the acknowledgment time in Normal mode, writing to these registers is allowed only in Setup mode.

Write only registers in Normal mode are 04h-05h, A0h.

All other registers are read and write in Normal mode.

All timings are measured with PWM output enabled. If the PWM output for GPIO is disabled, then acknowledgment times are reduced approximately by 30 µs for read and write in Normal mode.

Figure 2. Write Acknowledgment Time



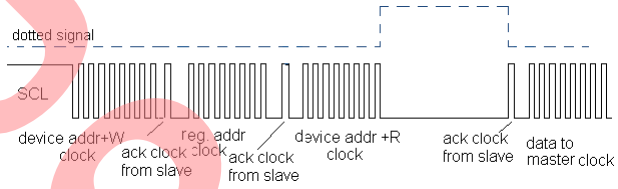
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2.5 Read Acknowledgment Time in Normal Mode

To read CapSense Express slave device registers, the master device must initiate a start command with the slave address in write operation mode. The next byte is the register address from which the master reads the data. The communication is restarted by sending I²C address with read bit to the slave and the data is read from the slave. Refer to the section Format for Register Read or Write for the read and write protocol.

First data read time. This is the time the master has to wait after sending the read instruction for the first data byte (device address). The timing waveform is shown in Figure 3. The dashed (high) signal shows the read time. Table 2 gives the maximum values of the read acknowledgment time in Normal mode for two different configurations. For any other configurations the CapSense Express acknowledgment times remains constant.

Figure 3. Read Acknowledgment Time for First Data Byte



Successive data read time. This is the time the master has to wait for successive data read after it has acknowledged the previous data read. This time is as shown in Figure 4. The dotted (high) signal shows the time of read. Table 2 gives the maximum values of the read acknowledgment time in Normal mode of operation.

The read timings are similar for first byte and second byte for different configurations of CapSense Express device.

Figure 4. Read Acknowledgment Time for Successive Data

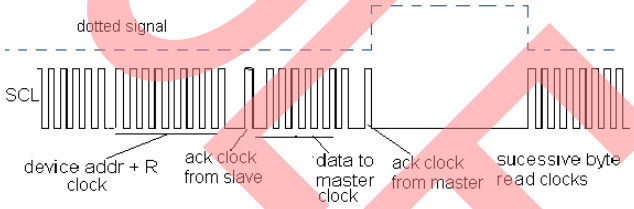


Table 2. Read in Normal Mode with PWM Functionality Enabled

Register Details	Ack. Time (in µs)	
	MAX 5 Button-5 GPIO	MAX 5 Button-5 GPIO
Device address ack. time	100	100
GPIO status registers (00h–03h)	100	100
GPIO operation settings (1Ch–4Dh)	120	120
Scan position, finger threshold, and IDAC settings(57h–74h)	140	140
CapSense read back (81h–89h)	120	120
Other configuration registers	100	100
Command register A0	NA	NA

Note All the above timings are given with PWM functionality enabled. If the PWM functionality is disabled for GPIO, then the acknowledgment times are reduced approximately by 30 µs.

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2.6 Read and Write Acknowledgment Time in Setup Mode

In Setup mode, read and write acknowledgment time of all registers is longer compared to the Normal mode when CapSense scanning is active. When CapSense scanning is stopped, the acknowledgment time is approximately the same as in Normal mode.

2.6.1 CapSense Filtering

Two user-configurable CapSense filters are implemented in CapSense Express:

I²C "Drop the Sample" helps reduce the "noise" induced by I²C communication occurring when a CapSense scan is in progress.

Averaging Filter averages 2, 4, 8, or 16 CapSense scan (raw counts) for each "sample".

Table 3 gives the acknowledgment time measurements in Setup mode for no scan and averaging filter with an average of two samples (Avg1) and an average of 16 samples (Avg16.). Write and read acknowledgment times (for first byte and successive byte) are the same.

Table 3. Read/Write Acknowledgment Times in Setup Mode with PWM Functionality Enabled

Register No.	Ack. Time (in ms)					
	No Scan		Avg1		Avg16	
	Max	Min	Max	Min	Max	Min
Device address ack. time	0.1	0.03	0.4	0.3	0.4	0.3
CapSense input (06–07)	0.11	0.09	0.4	0.15	11	0.25
Select GPIO (08–09)	0.55	0.38	0.98	0.38	11	.03
Inversion, port status, drive mode (0A–17)	0.25	0.19	0.58	0.03	11	.09
Settling time (50–51)	0.41	0.38	22	0.04	35	.03
Scan position (57–60)	0.25	0.07	0.5	0.07	11	0.1
FT, IDAC settings (61–6Ah), (6B–74h)	0.14	0.13	0.7	0.13	11	0.14
GPIO operation setting (1C–4D)	0.13	0.06	0.6	0.05	11	0.05
Button select (88–89)	0.12	0.04	0.5	0.04	11	0.07
Other registers	0.1	0.05	0.5	0.05	11	0.07
A0	0.1	0.06	0.5	0.06	11	0.09

Note Read only registers in Setup mode are 00-03h, 7A-7Bh, and 81-8Ch. Read Ack timing is given for these registers.

Write only registers in Setup mode is A0. Write Ack timing is given for this register.

All other registers are read and write registers in Setup mode.

Additional register information:

- PWM registers - 0x18-0x1B
- CapSense filtering registers - 0x56.

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2.7 Non Accessible Time of CapSense Express after Acknowledgment

Some CapSense Express I²C commands (written to register A0h), especially those involving non-volatile memory (Flash) operations, require long execution times. To maintain short acknowledgment times, the I²C bus is released before the command is fully executed (for example, before a Flash write is done). The acknowledgment times are as described in Table 1, Table 2, and Table 3, but the CapSense Express device cannot be accessed until the sent command (for example, A0 03 for a Flash write) is executed completely.

Table 4 gives complete details of these times for the given commands.

Table 4. CapSense Express Commands and Device Not Accessible Times after Acknowledgments

Command	Description	Executable Mode	Duration (Device is not Accessible after Acknowledgement)
W 00 A0 00	Get firmware revision	Setup/Normal	0
W 00 A0 01	Store current configuration to NVM	Setup/Normal	120 ms
W 00 A0 02	Restore factory configuration	Setup/Normal	120 ms
W 00 A0 03	Write NVM POR defaults	Setup/Normal	120 ms
W 00 A0 04	Read NVM POR defaults	Setup/Normal	5 ms
W 00 A0 05	Read current configurations (RAM)	Setup/Normal	5 ms
W 00 A0 06	Reconfigure device (POR)	Setup	200 ms
W 00 A0 07	Set Normal mode of operation	Setup/Normal	0
W 00 A0 08	Set Setup mode of operation	Setup/Normal	1.2 * (loop time[1] + 1 ms)
W 00 A0 09	Start scan	Setup/Normal	10 ms
W 00 A0 0A	Stop scan	Setup/Normal	5 ms
W 00 A0 0B	Get CapSense scan status	Setup/Normal	0

2.8 Boot Up Time Measurement

Boot up time is the time taken to initialize the configuration and initiate reliable I²C communication.

2.8.1 Boot Up Time for Corrupted User Configuration

If the user configuration stored in Flash is corrupted, the firmware restores to default factory settings (no GPIO and CapSense enabled) and rewrites the Flash with the factory configuration. Refer to CY8C201xx datasheet for details on factory defaults. Table 5 gives the details of boot up time for two different configurations of the CapSense Express device.

Table 5. Test Results for Boot Up Time

User Configuration	Boot Up Time (in ms)
1 GPIO enabled; CapSense buttons disabled	24
1 GPIO; 9 CapSense buttons enabled	100
Corrupted configuration	25

[1] Loop time can be measured by probing any sensor using an oscilloscope and measuring the time between two consecutive scans.

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2.9 Time to Enter Sleep Mode for CapSense Express

Sleep configuration for CapSense Express depends on three registers: sleep control pin (7Eh), sleep control (7Fh), and stay awake counter (80h). For more details on sleep mode and deep sleep mode refer to AN44209.

2.9.1 Normal Sleep Mode

Normal sleep mode provides an intermediate power consumption operation mode. It is enabled by configuring the corresponding device register. When enabled, the device enters sleep mode and wakes up after a specified sleep interval. The sleep interval can take one of the following values - 1.95 ms, 15.6 ms, 125 ms, 1 s. It scans the capacitive sensors before going back to sleep again. The device can also wake up from sleep mode with a GPIO interrupt.

The device enters normal sleep mode if it is idle for **stay awake counter (SAC) * 15.6 ms**. SAC can have a value from 0 to 255. The idle time out counter (SAC) is reset if there is any button press or IIC interaction.

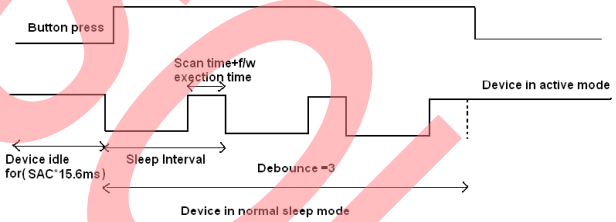
Device sleep time = Sleep interval - (scan time + firmware execution time).

Worst case response time in normal sleep mode is calculated as follows:

Response time = (D * sleep interval) + scan time + firmware execution time

Where,D refers to debounce

Figure 5. Normal Sleep Operation



Consider the following scenario

Number of sensors is 2

Debounce is 3

Sleep interval is 15.6ms

Scan time for each sensor is 700 us

Then the worst case response time with the firmware execution time of 2 ms is

Response time = (3 * 15.6) + 1.4+2

= 50.2 ms

2.9.2 Deep Sleep Mode

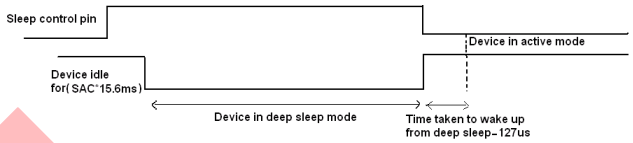
Deep sleep mode provides the lowest power consumption operating mode. The device enters into deep sleep mode if it is idle for **SAC * 15.6 ms**. In this mode, the device is woken up only by an external GPIO interrupt or by the sleep control pin being pulled LOW. When deep sleep mode is entered, CapSense Express state is that of permanent sleep. In this low power state, CapSense Express does not monitor any activity on the board.

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2.10 Wakeup Time from Sleep and Deep Sleep

This is the time taken to wake up the device from sleep; that is, the time required to start reliable I²C communication with the device after pulling the sleep control pin to LOW.

Figure 6. Deep Sleep Operation



Response time when the device is in deep sleep mode is calculated as follows:

Response time = 127 µs + baseline initialization time + D * (scan time + firmware execution time)

where D refers to debounce

Consider the following scenario:

Number of sensors is 2

Debounce is 3

Scan time for each sensor is 700 µs

Baseline initialization time is 1400 µs

The worst case response time with the firmware execution time of 2 ms is calculated as follows:

Response time = 0.127 + 1.4 + 3 * (1.4 + 2)

=11.727 ms

0.127 ms is the processing time taken before the device wakes up from deep sleep mode.

3 Summary

The various timing information given in this application note can be used as reference for reliable communication between a non I²C compliant master and the slave CapSense Express device.

4 Related Application Notes

AN44207 – CapSense Express™: APIs for Register Configuration

AN44209 – CapSense® Express™ Power and Sleep Considerations

AN42137 – CapSense™ Express Software Tool

AN48303 – CapSense® Express™ – Migrating from Firmware Rev 0x15 to Rev 0x1B

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Document History

Document Title: AN44208 - CapSense® Express™ - I2C Communication Timing Analysis

Document Number: 001-44208

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2279587	MOHD / DZU	04/02/08	New application note.
*A	2543451	MOHD	07/25/08	Updated Overview: Removed “Device address acknowledgment timing”. Removed “Write acknowledgment timing for registers 06h–07h”. Removed “Read acknowledgment timings for registers” Removed “Write acknowledgment timings for Command Register (A0)”. Added Setup and Normal Modes of Operation. Added Write Acknowledgment Time in Normal Mode. Added Read Acknowledgment Time in Normal Mode. Added Read and Write Acknowledgment Time in Setup Mode. Added Non Accessible Time of CapSense Express after Acknowledgment. Updated Wakeup Time from Sleep and Deep Sleep: Added Table 4. Updated content in other sections.
*B	2919277	SSHH	04/20/10	Updated Overview: Updated Time to Enter Sleep Mode for CapSense Express: Updated Normal Sleep Mode: Updated description. Added Figure 5. Updated Deep Sleep Mode: Updated description. Updated Wakeup Time from Sleep and Deep Sleep: Updated description. Added Figure 6. Updated Table 4: Updated details in “Duration” column corresponding to “w 00 A0 06” command.
*C	3243369	SSHH	04/28/11	Updated Software Version as “PSoC Designer 5.0 SP6” in page 1.
*D	4385995	PRIA	05/21/2014	Updated Introduction: Updated Non Accessible Time of CapSense Express after Acknowledgment: Updated Table 4: Updated details in “Duration” column corresponding to “W 00 A0 08” Command. Updated Related Application Notes: Removed references of AN44203, AN47716, and AN48398 as these application notes are obsolete. Updated to new template. Completing Sunset Review.
*E	5043430	PRIA	12/30/2015	Updated hyperlinks across the document. Updated to new template.
*F	5092581	PRIA	01/19/2016	Obsoleting the Application Note

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