AN4059

Clocking Options When Using HOTLink II™ Devices in HD-SDI Video Applications

Author: Cypress
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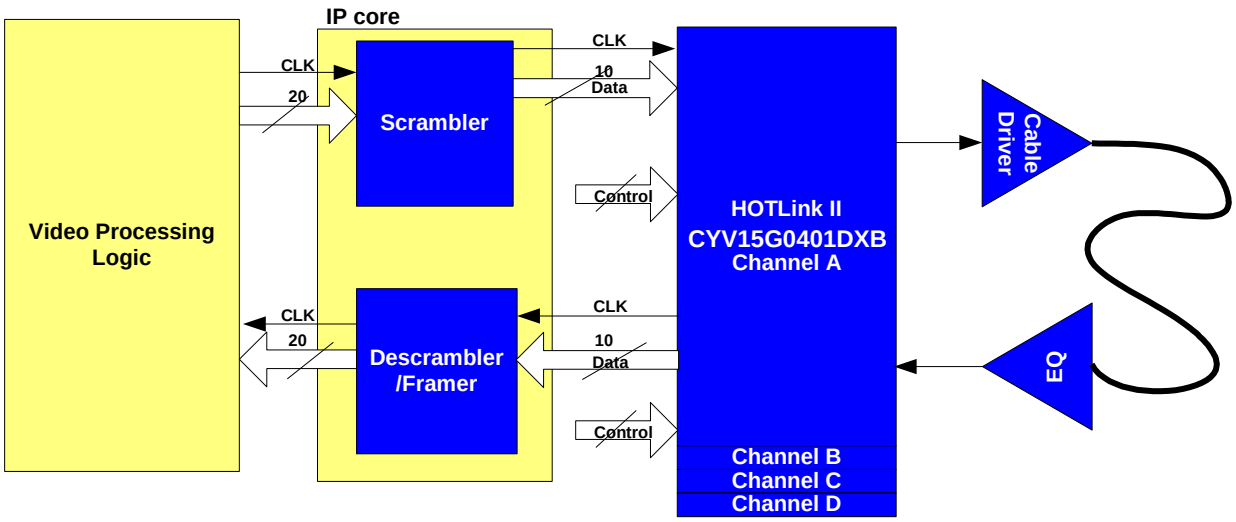
AN4059 discusses the various clocking options that can be used in these applications when using the HOTLink II device. This application note focuses on HD-SDI applications at the 1.485 Gbps.

Introduction

The HOTLink II™ family of physical layer (PHY) devices is a point-to-point or point-to-multipoint communications building block that provide serialization, deserialization, selectable 8B/10B encoding/decoding and framing functions. The family of devices are used in both SD (Standard Definition) and HD (High Definition) SDI (Serial Digital Interface) applications, that is, SMPTE 259M-CD (270 and 360 Mbps), and SMPTE 292M (1.485 and 1.485/1.001 Gbps). This application note discusses the various clocking options that can be used in these applications when using the HOTLink II device. The application note focuses on HD-SDI applications at the 1.485 Gbps data rate, but can equally be applied in SD- and HD-SDI 1.485/1.001 Gbps environments by simply substituting the appropriate frequency for REFCLK, via a clock oscillator or VCXO.

The application note first covers the transmit side clocking options when using one channel of the Independent Channel CYV15G0401DXB HOTLink II device as an example, followed by the receive side clocking options of the same device. The same ideas may be applied to any of the devices in the HOTLink II family. Three transmit, and two receive path options are available for HD-SDI applications. Each clocking option may be applied in SD-SDI, and HD-SDI 1.485/1.001 Gbps environments, by simply substituting the appropriate frequency for REFCLK, via the clock oscillator or VCXO. Figure 1 shows a block diagram of a single-channel HD-SDI system using a HOTLink II device.

Figure 1. HD-SDI Application Block Diagram



Transmit Path Clocking Solutions

Three clocking solutions for using the HOTLink II family of devices in an HD-SDI application follow.

Transmit Path clocking when a local global clock is present

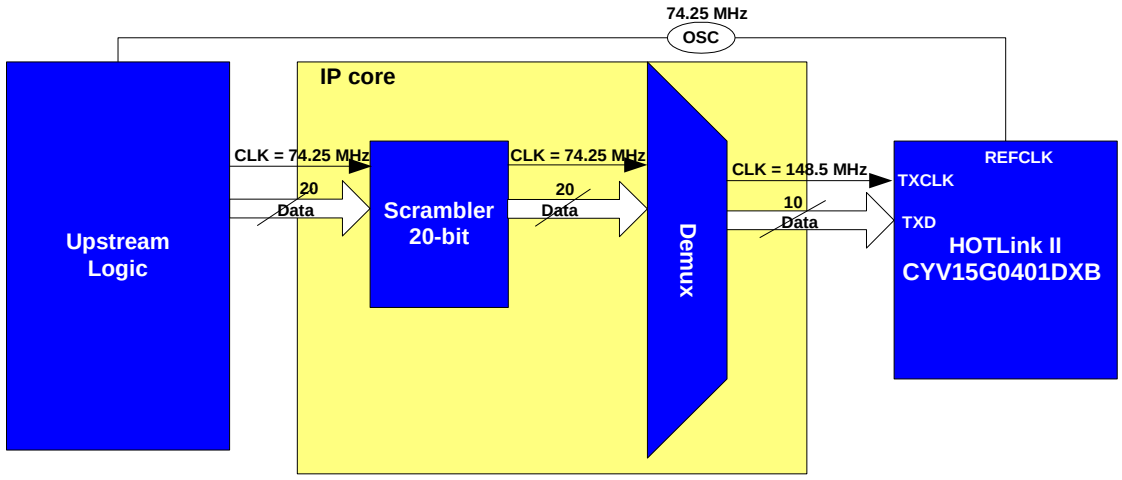
In this application, the card uses a global system clock oscillator at 74.25 MHz, which is used as the reference clock (REFCLK) for the applicable channel of the HOTLink II device, as well as for the FPGA (or ASIC) logic. In this case, the entire card operates from a single clock source and so data transfer from the upstream device to the HOTLink II device is synchronous to the transmit path of the HOTLink II device.

TXRATEx is used to select the clock multiplier for the Transmit PLL. When TXRATE = 0, the transmit PLL multiples the associated REFCLK± input by 10 to generate the serial bit-rate clock. When TXRATE = 0, the TXCLKO output clocks are full-rate clocks and follow the frequency and duty cycle of the associated REFCLK± input. When TXRATE = 1, the transmit PLL multiplies the associated REFCLK± input by 20 to generate the serial bit-rate clock. When TXRATE = 1, the TXCLKO output clocks are twice the frequency rate of the REFCLK± input.

TXCKSELx selects the clock source used to write data into the Transmit Input Register. When TXCKSEL = 1, the associated input register for TXDx[7:0] and TXCTx[1:0] is clocked by REFCLK. In this mode, the phase alignment buffer in the transmit path is bypassed. When TXCKSEL = 0, the associated TXCLKx is used to clock TXDx[7:0] and TXCTx[1:0] into the input registers.

Therefore TXRATE = 1 and TXCKSEL = 0 for the example illustrated in Figure 2.

Figure 2. Transmit Path Clocking when a Local Global Clock is Present



Transmit Path clocking using back clocking

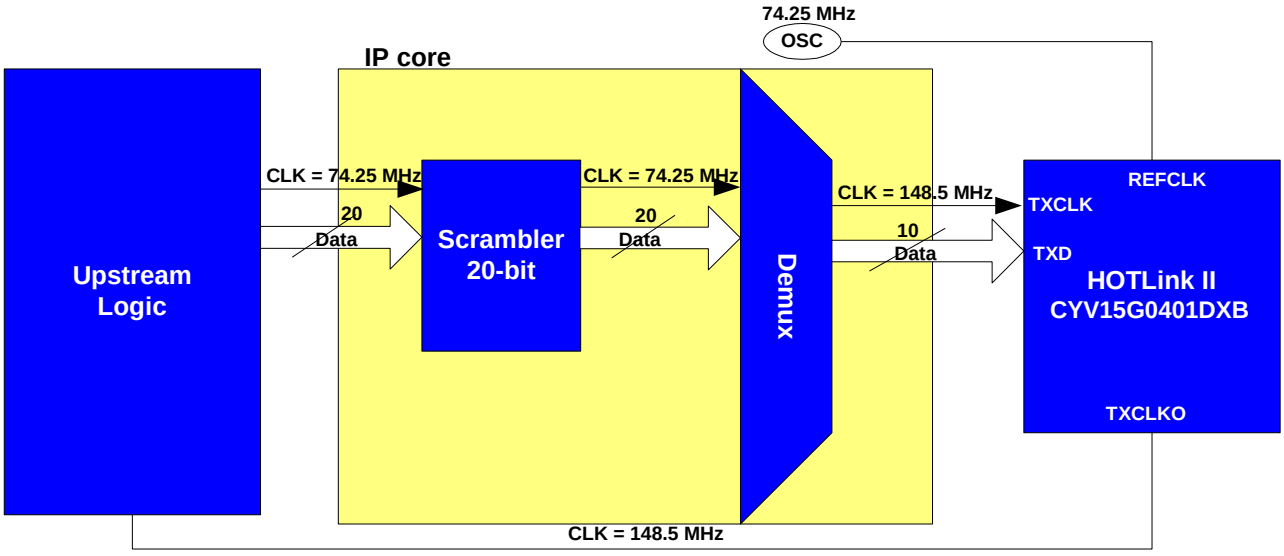
With this option the reference clock (REFCLK) for the HOTLink II device is provided by a clean source such as a crystal oscillator to ensure optimal jitter performance. TXCLKO (a derivative of REFCLK) of the HOTLink II device, which is synchronous to REFCLK is used to provide the reference clock for the FPGA upstream, thereby making the system synchronous.

TXRATE = 1 and TXCKSEL = 0 for the example shown in Figure 3.

Transmit Path clocking when a source synchronous clock is used

This clocking solution could be used for example in switchers, where a video stream is switched from one port to another. The recovered clock from the source data will be used to provide the clock for the entire path, in order to keep everything synchronous. In this case, the REFCLK from the HOTLink II will be supplied by the FPGA. This clock will not be a low-jitter clean clock and as such will be fed through a VCXO or PLL, that has an adjustable or known skew (to ensure setup and hold time requirements can be met). REFCLK clocking is used in this application, so setup and hold times between REFCLK and TXDx[9:0] will be an important factor.

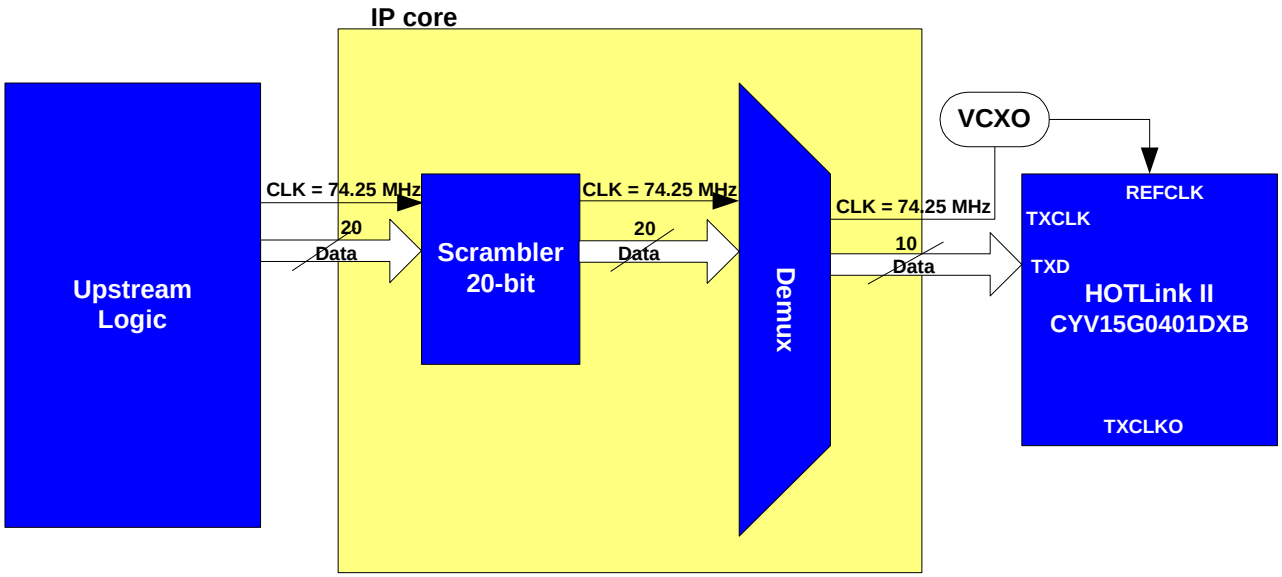
Figure 3. Transmit Path Clocking Using Back Clocking



The HOTLink II device requires a low-jitter reference clock (REFCLK) source, as it is this REFCLK (and a derivative) that is used to clock the entire transmit path. Therefore, in order to maintain a low-jitter signal on the output it is necessary to clean up the jitter from the FPGA clock before supplying it to REFCLK.

The data bus switches at 148.5 Mbps in this application and as such, the data will be clocked in to the upstream device on both the rising and falling edges of REFCLK. This is achieved with TXCKSEL = 1 and TXRATE = 1.

Figure 4. Transmit Path Clocking when a Source Synchronous Clock is Used



Receive Path Clocking Solutions

Two clocking solutions for using the HOTLink II family of devices in an HD-SDI application follow.

Receive Path clocking using half rate clocking on RXCLKx

In the receive path, everything upstream should be synchronous to the recovered clock, and so RXCLKx will provide the clock to the upstream devices. With half rate clocking a 74.25 MHz, clock is provided to the upstream device. The data, however, switches at 148.5 Mbps, and therefore it is clocked into the upstream device using both the rising and falling edges of RXCLKx, (mimicking a DDR interface), or alternate bytes are clocked in using the rising edges of RXCLKx+ and RXCLKx-. This allows customers to use a slower speed clock in their upstream logic provided by RXCLKx.

When RXRATE = 1 and RXCKSEL = 0, the RXCLKx± clock outputs are complementary clocks that follow the recovered clock operating at half the character rate. Data for the associated receive channels should be latched alternately on the rising edge of RXCLKx+ and RXCLKx–.

Receive Path clocking using full rate clocking on RXCLKx

This is similar to the previous clocking option, except that full rate clocking is used, that is a 148.5 MHz clock is supplied to the upstream logic with the data also switching at 148.5 Mbps. One data character per clock period is clocked out of the HOTLink II device to the upstream logic, and depending on whether RXCLKx+ or RXCLKx- is being used (complementary clocks), a rising or falling edge latching scheme can be accomplished.

When RXRATE = 0 and RXCKSEL = 0, the RXCLKx± clock outputs are complementary clocks that follow the recovered clock operating at the character rate. Data for the associated receive channels should be latched on the rising edge of RXCLKx+ or falling edge of RXCLKx–.

Figure 5. Receive Path Clocking Using Half Rate Clocking on RXCLKx

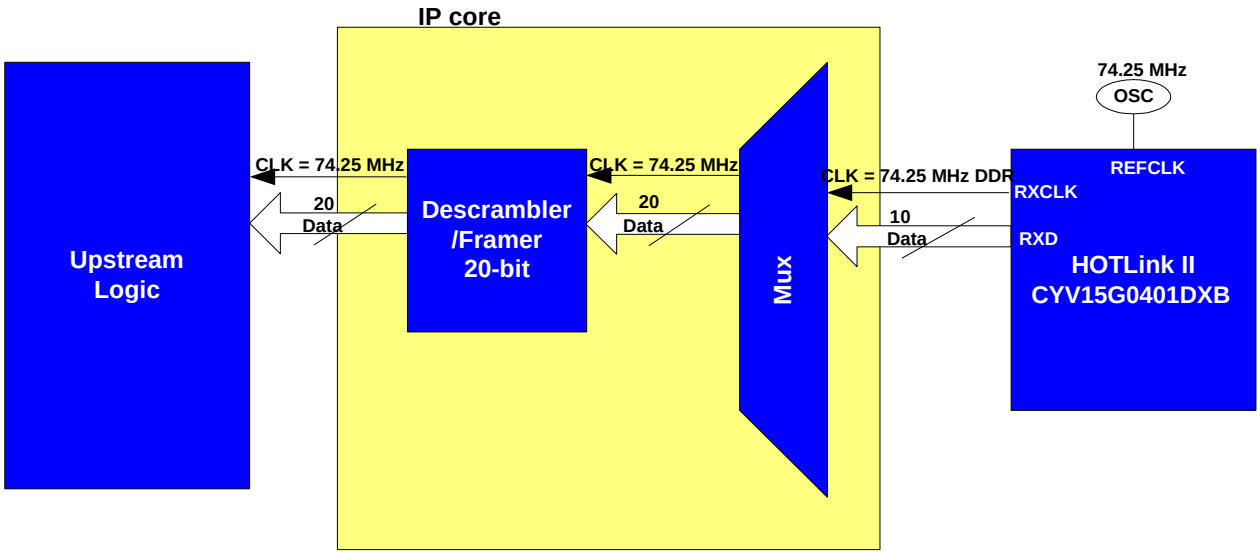
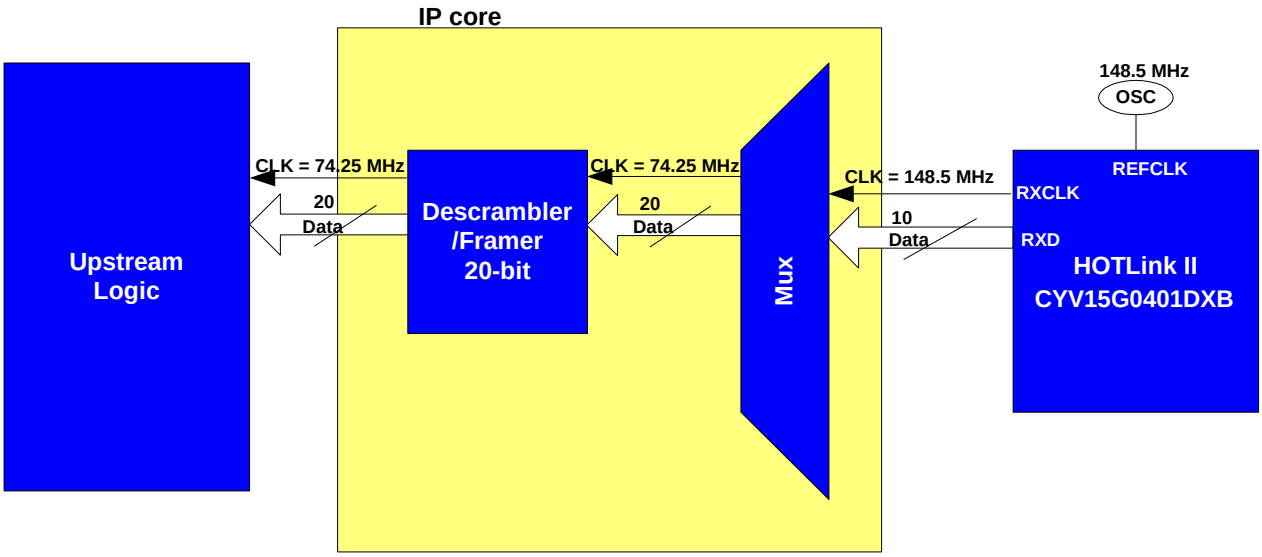


Figure 6. Receive Path clocking using full rate clocking on RXCLKx



Summary

This application note discusses the various clocking solutions available to customers when designing SDI interfaces. The solution used will depend on the clocking architecture that is required. Three transmit and two receive path options are discussed. It is to be used as a guideline when designing with HOTLink II devices in video applications. Should you require assistance with a particular design please, contact Cypress' customer support, which can be found at www.cypress.com.

References

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Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1574444	FRE	10/11/2007	New application note.
*A	3396207	SAAC	10/05/2011	Updated template according to current CY standards. Updated Abstract. Changed part number CYV15G0403DXB to CYV15G0401DXB. Replaced the following: REFCLKx → REFCLK REFCLKx+ → REFCLK+ REFCLKx → REFCLK- TXRATEx → TXRATE TXCLKOx → TXCLKO TXCKSELx → TXCKSEL RXRATEx → RXRATE RXCKSELx → RXCKSEL Removed reference to AN4052 from the references section.
*B	4546027	YLIU	10/20/2014	Sunset Review Updated template
*C	5840648	RUPA	08/07/2017	Updated Cypress logo and Copyright information.

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