# AN35159

# TAXI™ to Cypress CY7C9689 HOTLink® Transceiver Conversion Series Two-Serial Interface

**Author: Cypress**
**Associated Project: No**
**Associated Part Family: CY7C9689A**
**Associated Application Notes: AN1162**

AN35159 shows the design considerations when interfacing to the serial inputs and outputs of the CY7C9689.

## Introduction

The Cypress CY7C9689 HOTLink® Transceiver integrates all the functions necessary to create TAXI™ compatible bidirectional data communication links. Systems built with the CY7C9689 are directly compatible with legacy systems made using AMD™ TAXIchip™ devices. The CY7C9689 HOTLink Transceiver is functionally equivalent to an AMD AM7968 TAXI transmitter and AM7969 receiver pair, with numerous technology enhancements and extensions.

In addition to being able to interoperate with legacy TAXI devices, the CY7C9689 incorporates a number of improvements over the original AMD TAXI chipset. The TAXI chipset is a full bipolar design and consumes approximately 3 W of power. The CY7C9689 is designed on 0.35-µm CMOS technology and consumes only 30% of the power of the AMD chipset. The CY7C9689 contains both the transmit and receive functions, and integrates separate transmit and receive FIFOs in the same device. The CY7C9689 is available in a 100-pin TQFP package, offering significant board real estate savings. It operates from 50 MBd to 200 MBd, while the TAXI chipset has a maximum serial signaling rate of 175 MBd. In addition, the AMD TAXI chipset has been discontinued, leaving numerous designs and products in jeopardy.

Fortunately, the CY7C9689 is designed for simple replacement of existing TAXI chipset designs, and generally requires little change in surrounding system logic. The CY7C9689 allows the continued use and manufacturing of these legacy systems with minimal impact to the equipment, and enables new designs with up-to-date technology. By replacing the TAXIchip devices with the CY7C9689, it is possible to maintain compatibility with systems deployed in the field, while increasing integration, lowering power requirements, and improving reliability.

Although the CY7C9689 is not a pin-for-pin replacement of the original TAXI devices, the CY7C9689 parallel interface and serial interface can be mapped onto the TAXI functional pins with minimal external logic. Since the CY7C9689 was designed with modern systems in mind, it has many enhanced functions that the TAXI lacks. The objective of this document is to show the design considerations when interfacing to the serial inputs and outputs of the CY7C9689.

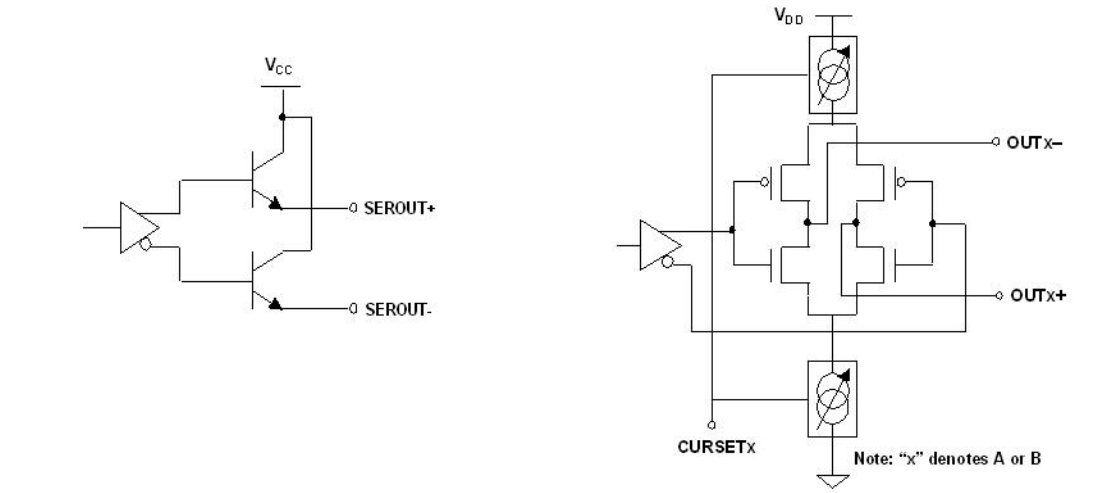
## Overview

The serial output and input structures of the CY7C9689 and the AMD TAXI chipset are significantly different. The TAXI serial outputs are traditional +5 V Emitter Coupled Logic (ECL) outputs as shown in Figure 1*a*. The CY7C9689 high-speed serial outputs are differential current drivers which are compatible with PECL signal levels. This differential current driver is shown in Figure 1*b*.

The serial inputs of the TAXI and the CY7C9689 are both high-impedance differential receivers, where the CY7C9689 has both higher sensitivity and a wider common mode range. This application note concentrates on the different methods of biasing and terminating the serial interfaces on the CY7C9689.

**Note** The device CY7C9689 is Obsolete, the equivalent drop in replacement is CY7C9689A. No changes to form, fit or function of the devices have been made. The ‘A’ simply indicates the silicon revision.

Figure 1. TAXI and CY7C9689 Serial Output Structures




a) TAXI Differential PECL High Speed Serial Output

b) CY9689 Differential PECL Compatible Serial Output

## CY7C9689 Serial Output Drivers

PECL output drivers, such as ones that are found on the TAXI transmitter and CY7B923 HOTLink Transmitter, are well understood. Their biasing and terminating methods can be found in the Cypress application note "HOTLink Design Considerations" and other related literature.

The differential PECL-compatible drivers found on the CY7C9689 are unique to Cypress. These high speed serial output drivers can be viewed as push-pull current drivers. The amount of current driven is controlled by an external resistor.

To drive the attached load HIGH, the PMOS transistor is driven into the saturation region and the NMOS transistor is turned off. Here the variable current source connected to $V_{DD}$ determines the amount of current sourced through the output. This current source is controlled by an external resistor (current-set resistor, $R_{CURSET}$).

When one output is driving HIGH (sourcing current), the complementary output is driving LOW (sinking current). In this case, the complementary output PMOS transistor is turned off and the NMOS transistor is in saturation. The current sinking into this complementary output is controlled by the variable current source connecting to GND. This current source is also controlled by the same $R_{CURSET}$ resistor.

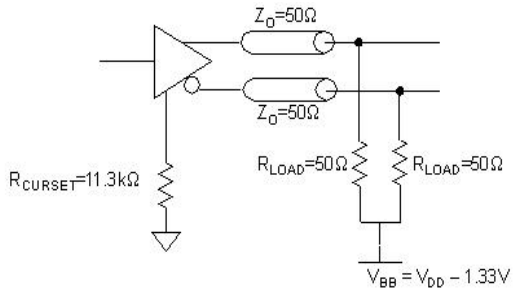
Since this is a current driver, the output voltage is determined by the output current and the load impedance $Z_{LOAD}$. The desired output voltage swing is therefore controlled by the current-set resistor $R_{CURSET}$ associated with that driver. Different $R_{CURSET}$ values are required for different line impedance/amplitude combinations. The output swing is designed to center around $V_{DD}$ – 1.33 V. Each output must be externally biased to $V_{DD}$ – 1.33 V.

This differential output-swing can be specified two ways: either as a peak-to-peak voltage into a single-ended load, or as an absolute differential voltage into a differential load.

When specified into a single-ended load (one of the outputs switching into a load), the single output will both source and sink current as it changes between its HIGH and LOW levels. The voltage difference between this HIGH level and LOW level determine the peak-to-peak signal-swing of the output. This amplitude relationship is controlled by the load impedance on the driver, and by the resistance of the $R_{CURSET}$ resistor for that driver, as listed in Equation 1.

$$R_{CURSET} = \frac{180 \times Z_{LOAD}}{V_{OPP}} \quad \text{Equation 1}$$

Figure 2. Single-Ended Transmission Line Model




In Equation 1, $V_{OPP}$ is the difference in voltage levels at one output of the differential driver when that output is driving HIGH and LOW, and $Z_{LOAD}$ is that load seen by the one output when it is sourcing and sinking current. With known load impedance and a desired signal swing, it is possible to calculate the value of the associated CURSETA or CURSETB resistor that sets this current.

For example, if each output drives terminated boards trace having an impedance of 50 Ω (as shown in Figure 2), to achieve an output swing of 800 mV across this 50 Ω termination impedance the $R_{CURSET}$ value would calculate to 11.25 kΩ. The closest standard resistor value to this is 11.3 kΩ.

When the interconnect and load are more appropriately viewed as a differential or balanced transmission line, the absolute differential voltage $V_{ODIF}$ and the balanced load impedance are used to calculate the value of $R_{CURSET}$. The relationship between this absolute differential voltage swing and load impedance is expressed in Equation 2.

$$R_{CURSET} = \frac{90 \times Z_{LOAD}}{V_{ODIF}} \qquad \text{Equation 2}$$

For example, when driving a terminated 100 W balanced transmission line (as shown in Figure 3), to generate the same 800 mV of output voltage across a differential 100 W load, the $R_{CURSET}$ value would calculate to 11.25 kW.

Note that both examples generated the same $R_{CURSET}$ value. Keep in mind that in a balanced transmission line model, the dynamic differential voltage swing ($(V_{OH+} - V_{OL-}) - (V_{OL+} - V_{OH-})$ = 1600 mV) is twice the static voltage delivered between the true and complement outputs.

## Driving Optical Modules

All *de facto* standard optical transceiver modules have either ECL or PECL differential data inputs or outputs. Differential signaling provides high immunity to common-mode noise and the lowest signal jitter. The PECL-compatible differential output drivers and receivers on the CY7C9689 are designed to interface to either PECL or ECL optical modules.

Figure 3. Balanced Transmission Line Model

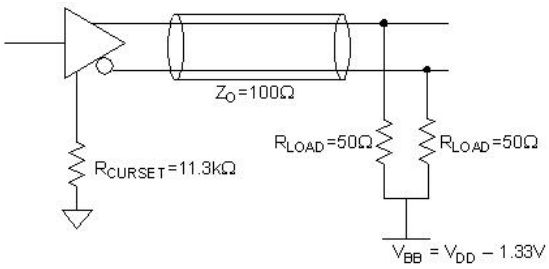
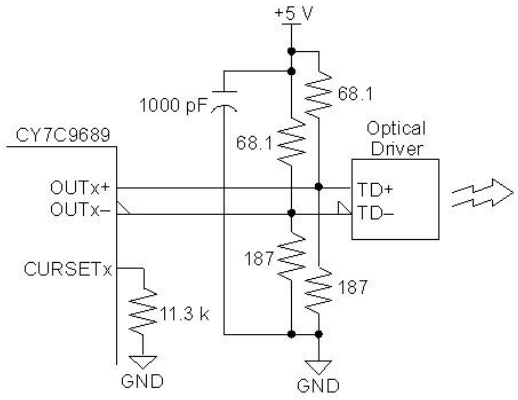



Figure 4. CY7C9689 Transmitter to PECL Optical Module: Thévenin Termination




To reduce the impact of impedance mismatches, stub effects, and reflections, the signal-trace routing from the CY7C9689 serial output to the optical module data inputs should be kept as short as possible. To maintain proper balance in the transmission line, the length of the two traces must remain equal (both physically and electrically), such that minimal skew exists between the differential signals.

Thévenin or H-bias termination is recommended for these high-speed differential signals at the destination-end of the transmission line (close to the optical-module inputs). For more detailed information and theory on both of these termination methods, please refer to the Cypress application note “HOTLink Design Considerations”.

### Connecting to PECL Optical Modules

Interfacing to a PECL interface optical module requires only five passive parts. The schematic in Figure 4 illustrates the connections and components necessary for this type of connection. Note that these Thévenin termination resistor values only apply to board trace impedances of 50 Ω. For other trace or transmission line impedances, the termination resistor value can be calculated using the equations Equation 3 and Equation 4.

$$R_{pu} = \frac{V_{DD} \times Z_o}{V_{DD} - 1.33} \quad \text{Equation 3}$$

$$R_{pd} = \frac{V_{DD} \times Z_o}{1.33\ V} \quad \text{Equation 4}$$

Where,
Rpu = Pull-up resistor value
Rpd = Pull-down resistor value
Zo = trace or transmission line impedance
VDD = power supply voltage

There is a 1000 pF bypass capacitor specified in the schematic. This capacitor is necessary because the base frequency and harmonics of the CY7C9689 outputs are far beyond any frequency the power supply itself could pass. The type of capacitor specified should be a good high-frequency RF-type. Either NPO or C0G type dielectric capacitor can be used in this type of application.

Figure 5 illustrates the H-bias termination method. The two 50 Ω resistors terminate the transmission line, while the voltage-divider network provides a DC biasing point of $V_{DD}$ – 1.33 V. The 0.01-µF capacitor is used to stabilize the bias point. For differential signaling, the H-bias termination is preferred over Thévenin termination because it consumes less power, and provides less duty-cycle distortion. With Thévenin terminations, each output is treated like a single-ended signal, which introduces a constant differential offset due to finite tolerance of the resistors.

Figure 5. CY7C9689 transmitter to PECL Optical Module: H-Bias Termination

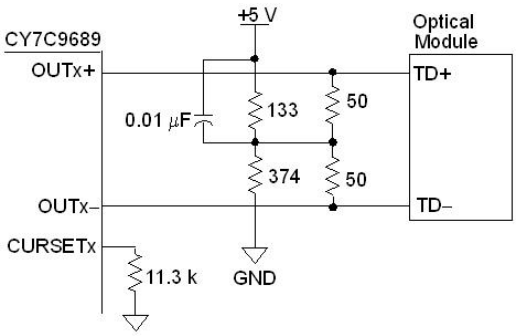
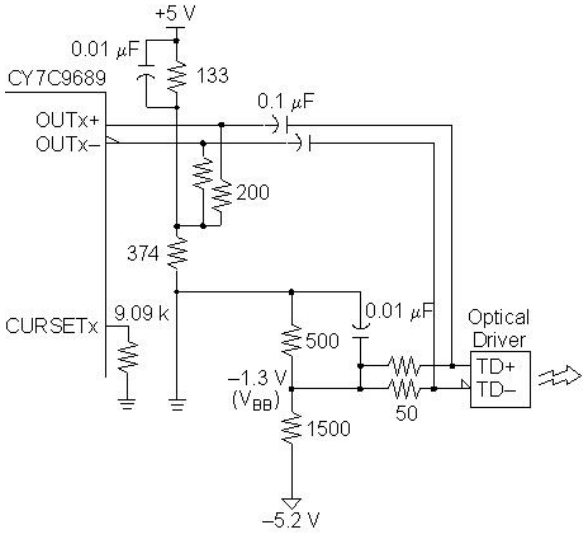



Figure 6. CY7C9689 Transmitter to ECL Optical Module




## ECL Optical Modules

Those optical modules with the case connected to $V_{CC}$ are designed for use in a negative DC supply system. These types of modules may also be driven by the CY7C9689 Transmitter.

If the optical module is used below ground, it must be AC-coupled to the HOTLink Transmitter. This type of connection is shown in Figure 6.

The CY7C9689 Transmitter outputs are biased into the same $V_{DD}$ – 1.33 V load-point as a PECL optical module, however, the DC-current load is located directly adjacent to the source end of the transmission line. The DC current-load at this point is quite light, and is required to keep the internal current sources stable.

The recommended value for this DC-current load is equivalent to one fourth that of the actual attached transmission-line load. When used with 50 Ω transmission lines (as shown in Figure 6), the associated DC-load impedance would be four times this or 200 Ω.

Following the DC load, AC-coupling capacitors are used to connect the CY7C9689 Transmitter PECL-compatible outputs to the negative-referenced ECL inputs of the optical module. Due to their parasitics, these coupling capacitors actually operate as a bandpass filter, centered around their series resonant frequency. To pass additional low- or high-frequency components, additional capacitors should be placed in parallel with the coupling capacitors.

Capacitively coupled signals require DC restoration and, if the connection length warrants, transmission line termination. DC restoration is necessary to place the signal swings in the input range of the ECL receiver. Unlike true open-emitter ECL outputs, which are biased to a level slightly below their $V_{OL}$(min.) level ($V_{CC}$ – 2 V), AC-coupled ECL inputs need to be biased to the center of the receiver's input range. For standard ECL this is generally the same as the $V_{BB}$ reference point of $V_{CC}$ – 1.3 V. In Figure 6, this reference point is created from a resistive divider network, and bypassed with a 0.01-µF capacitor to provide the dynamic current response needed for the differential inputs.

## LED vs. LASER Optical Module Usage

The signaling rates supported by the CY7C9689 can be supported completely by LED-based optical modules. These LED modules are generally lower in cost and have fewer safety concerns than LASER-based optical modules. All LED-based optical modules are used with large diameter core optical fiber (200-µm step-index or 62.5-µm graded-index multimode fiber).

For operating environments where long distances are required, it may be necessary to use LASER-based optical modules. For shortwave LASERs (780–850 nm), the preferred media is 50-µm core graded-index multimode fiber, but they can also be used with 62.5-µm core fiber.

In specific operating environments, LASER-based optical modules may also require that the LASER light output be disabled or turned off to meet all safety or signaling requirements. Forcing the input data stream to a constant logic-0 condition will not necessarily disable the light output from an optical module. Many optical modules, even those driven by a DC-coupled source signal, are AC-coupled internally. When presented with a static input, the AC-coupled signal eventually loses all reference to the actual DC value of its inputs, and the LASER driver is enabled at some power level.

In DC- or AC-coupled LASER modules, the only safe way to disable light output is at the optical module itself. This requires either the selection of an optical module with an external LASER disable input, or the ability to remove power from the module.

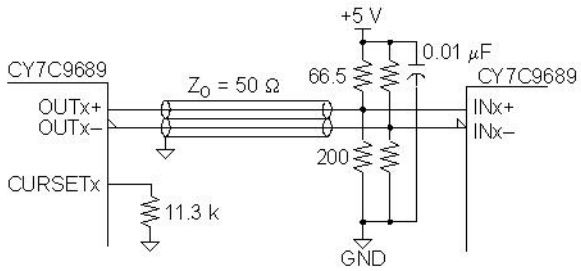
# Driving Copper Media

The CY7C9689 Transmitter can easily interface to many types of copper media, and allows communication between systems much further than other signaling technologies like LVDS.

Numerous characteristics determine how far a signal can be transmitted on copper media. The most important of these are:

- Voltage amplitude of the signal fed into the cable
- Jitter and ringing on the source signal
- Attenuation characteristics of the cable
- Length of the cable
- What (if any) equalization is used in the system
- Receiver loading and sensitivity

Figure 7. Direct-Coupled Copper Interface Thévenin Bias




Coupling to the cable or circuit board traces may be done in multiple ways, depending on the media type and distances involved.

### Direct Coupled

For those instances where the signal never leaves the same chassis (or even the same board) it is possible to directly couple to the media. Here the media is effectively the circuit board traces, runs of twisted-pair, twinax, or dual coax. The main criteria here is that there must be no chance for a significant $V_{DD}$ reference difference (transient or DC) between the CY7C9689 Transmitter and far-end Receiver, including any common-mode induced noise. For the CY7C9689 Receiver, this maximum difference is around 1 V. Under these conditions the CY7C9689 Transmitter and Receiver may be connected as shown in Figure 7 and Figure 8.

While both Figure 7 and Figure 8 show 50 Ω transmission lines, the actual impedance can be higher than this. For other impedances, the termination resistors values must be changed to match the characteristic impedance of the medium.

When sent through twin coaxial cables (as shown in Figure 7 and Figure 8) or separate traces on a circuit board, care must be taken to ensure that both lines are electrically the same length. Any difference in length causes one of the two signals to arrive at the receiver input either leading or lagging the other. This difference manifests itself as jitter in the receiver. If twisted-pair or twinax is used instead, both the OUTx+ and OUTx– signals combine to form a single signal sent down a balanced transmission line.

Figure 8. Direct-Coupled Copper Interface, H-Bias

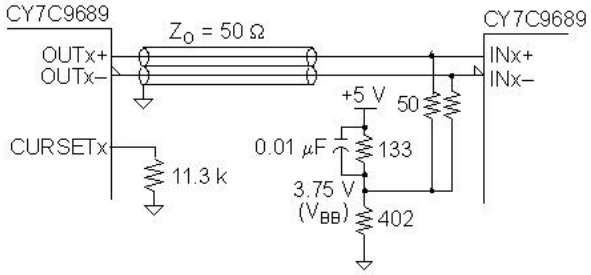
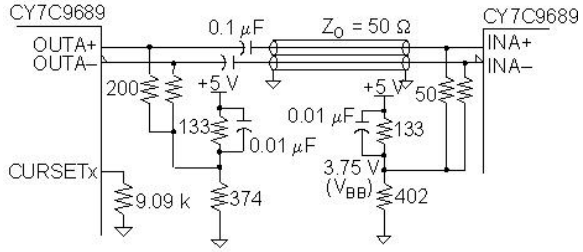



Figure 9. Capacitive-Coupled, Copper Interface




For either type of DC-coupled transmission line (dual unbalanced or single balanced), either the dual Thévenin or the H-bias termination may be used. For the lowest power dissipation, H-bias should be used.

## Capacitor Coupled

For configurations where it is possible to have significant ground or reference differences, some form of AC coupling becomes necessary. If the signals remain in a well protected environment (minimal EMI/ESD exposure) this AC coupling can be performed with capacitors. When this is done, bias/termination networks are required at both ends of the cable. A schematic detailing this type of connection is shown in Figure 9.

The transmit end uses an H-bias network to provide a minimal DC load to the driver. This is the same DC-load network used with AC-coupled optical transmit interfaces. When coupled with the terminated transmission line, this allows the desired voltage swing to be delivered, and at the same time provides the output buffer a DC load point of $V_{DD}$ – 1.33 V. Each output of the driver sees load impedance that is equal to the transmit-end load resistance in parallel with the receive end terminating resistance.

When calculating the current setting resistor value for this interface type it is necessary to take the total current load in to account. In the circuit shown in Figure 9, for an 800-mV output swing, the current set resistor value required would be 9.09 kΩ, as shown in Equation 5.

$$R_{CURSET} = \frac{180 \times (\frac{200\,\Omega \times 50\Omega}{200\,\Omega + 50\Omega})}{0.8} = 9\ K\Omega$$

Equation 5

Care must be taken in choosing the AC-coupling capacitors. Good low-loss RF-grade capacitors should be used for this application. These parts are available in many different case types and voltage ratings. The capacitors used must be able to withstand not just the voltage of the signals sent, but of any DC difference between the transmitter and receiver and the maximum ESD expected. Because the 4B/5B or 5B/6B encoded signals generated by the CY7C9689 are not DC-balanced, the coupling capacitors must also have a fairly large amount of capacitance to allow them to propagate the near-DC content in the signaling. A typical 0.1-µF 50-WV X7R capacitor would be available in a 0805 surface mount case size (0.08″L x 0.05″W). For on-board applications a 50-WV rating should be sufficient. While capacitors with much higher breakdown voltages are available, both cost and space make their use prohibitive.

This type of coupling is very similar to that used to drive an AC-coupled optical module. Since the CY7C9689 Receiver and an optical module both operate with ECL 100 K-level compatible signals, this should be expected.

In this configuration, the receiver reference point is set slightly different from that for a standard ECL receiver. Part of this is due to the CY7C9689 Receiver being designed for operation at +5 V rather than –5.2 V or –4.5 V. The other is that the CY7C9689 Receiver has a wider common-mode range than standard 100 K ECL parts. To allow operation over the widest range of signal conditions, the DC restoration network on the receive end of the transmission line is set to the center of the CY7C9689 Receiver common-mode range at $V_{DD}$ – 1.25 V.

This capacitive-coupled interface is not recommended for cabling systems that leave a cabinet or extend for more than a few feet. This is primarily due to:

- Limited voltage breakdown under ESD situations of the coupling capacitors
- ESD susceptibility of the receiver due to transients induced in the cable
- Limited common-mode rejection at the receiver end

Addition of a second set of coupling capacitors at the receive end may improve some of these characteristics, but it will not remove them.

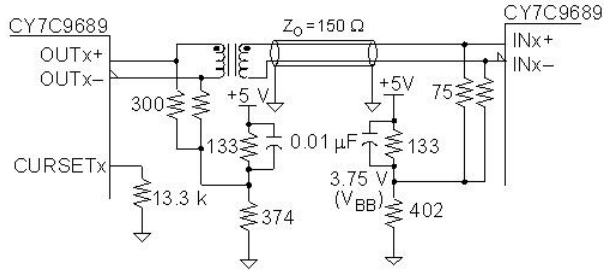
## Transformer Coupled

The preferred copper attachment method is transformer coupling. Transformers have multiple advantages in copper-based interfaces. They provide:

- High primary-to-secondary isolation
- Common-mode cancellation

- Balanced-to-unbalanced conversion.

Figure 10. Transformer-Coupled, Copper Interface




The transformer is similar to a capacitor in that it also has passband characteristics, limiting both low- and high-frequency operation. Proper selection of a coupling transformer allows passing of the frequencies necessary for HOTLink serial communications. A schematic detailing a transformer coupled interface is shown in Figure 10.

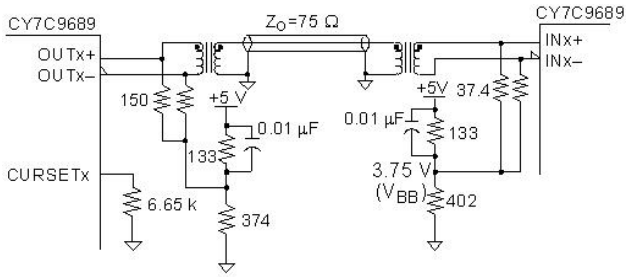
This transformer-coupled configuration has many similarities to a capacitively-coupled interface. It still provides DC isolation between the CY7C9689 Transmitter and Receiver, and requires the DC restoration and termination network at the receiver.

The connections at the CY7C9689 Transmitter and Receiver are similar to the biasing used in the capacitor coupling scheme. In Figure 10, the balanced transmission line impedance is 150 Ω. With this cable load, the DC load resistors at the transmit end change to 300 Ω(4 x 75 Ω) and 75 Ω on the receive side. For an 800-mV launch amplitude, the current set resistor value is set to 1.33 kΩ.

The configuration shown in Figure 10 uses only a single transformer and either 150 Ω twinax or twisted-pair as the transmission line. This can be done because the transmission system remains balanced from end to end. Here the primary functions of the transformer are to provide isolation and common-mode cancellation. In a single transformer configuration the transformer should be placed at the source end of the cable.

In Figure 11 a second transformer is added to the transmission system at the receiver end of the cable. This configuration allows use of either balanced or unbalanced (coaxial) transmission lines. The configuration shown here is a 75 Ω coaxial cable system. Here the first transformer is used for balanced-to-unbalanced conversion, while the second transformer provides unbalanced-to-balanced conversion. Note that the change in media impedance requires corresponding changes in the transmitter DC-load resistors, transmission line termination resistors, and the $R_{CURSET}$ resistor.

Figure 11. Dual Transformer-Coupled, Copper interface




## CY7C9689 Receiver ECL Inputs

The CY7C9689 Receiver has five PECL compatible inputs: INA+, INA–, INB+, INB–, and CARDET. The INA± differential input is normally used for the primary received data input. This input is only functional as a differential receiver. To use it as a single-ended receiver, a $V_{BB}$ reference would have to be attached to one of the INA± inputs. Since the CY7C9689 Receiver does not provide a $V_{BB}$ output, this must come from either an external PECL gate or a resistive divider. Because neither of these sources can be guaranteed to be at the exact internal $V_{BB}$ reference of the HOTLink Receiver (and will thus introduce jitter into the system), operation of INA+ in single-ended mode is not recommended. Also, operation in single-ended mode generally takes twice the input signal swing (400 mV for the CY7C9689) for a receiver to properly detect data.

The INB± differential input is expected to be used as a redundant data input in a fault tolerant system, or for attachment of alternate media types. The operation of the INB± inputs is identical to INA±.

The CARDET input is a dedicated single-ended PECL input primarily designed to be driven by an optical module's Signal Detect (SD) output. As a single-ended PECL input, it should not be directly connected to the signal detect outputs of optical modules that present a TTL-level Signal Detect output.

To interface a TTL-level Signal Detect to the CARDET input, a two-resistor divider can be added between the optical module and the CARDET input. If the media interface does not present a signal detect status, the CARDET input should be pulled HIGH to allow the remaining signal status monitors to affect the LFI status output.

### ECL Input Levels

Unlike standard 100 K ECL logic, the CY7C9689 PECL inputs are designed to operate substantially beyond the full 100 K ECL voltage and temperature range.

Normally 100 K ECL inputs should never be raised above $V_{DD}$ – 700 mV. If this occurs, the input transistor saturates and can damage other internal structures in the gate. Because the CY7C9689 receiver is designed for use in a communications environment, its input structures are more robust and can be taken all the way up to $V_{DD}$ with no degradation in performance. This provides a common mode operating range more than twice that of standard ECL/PECL.

The CY7C9689 PECL receivers also provide compatible gain to that available from standard 100 K ECL. The receiver is able to fully detect 1s and 0s with as little as 200 mV of differential signal at the inputs, where the TAXI receiver requires 300 mV

The CY7C9689 PECL inputs are also robust on the $V_{IL}$(min.) side. When operated in differential modes these inputs provide full functionality down to $V_{DD}$ – 2.5 V, yielding a full 2.5 V common-mode operating range. The AMD TAXI receiver common mode-range only spans from $V_{CC}$ – 0.55 to 3.05 V, a total of 1.4 V. The CY7C9689 common-mode range is more than 1 V wider than the TAXI Receiver.

## CY7C9689 Receiver Biasing

Unlike the CY7C9689 PECL-compatible outputs, which require an output DC load point to create the center-of-swing level, the CY7C9689 PECL inputs instead require levels within their input range to allow them to switch. When the CY7C9689 Receiver is directly connected to the biased output of either a 10 K, 10 KH, or 100 K ECL driver these conditions are satisfied.

### PECL Optical Modules

Connecting a PECL optical module to the CY7C9689 Receiver is the same as connecting two ECL parts together. This connection is shown in Figure 12.

A bias network is required on the output of the optical module to allow it to switch. A Thévenin or Y-bias network should be used on the high-speed serial lines (RD+ and RD– as shown in Figure 12) to keep induced jitter to a minimum. The signal- or carrier-detect output (SD) of the module is considered a logic level signal and only requires a pull-down (shunt) type of biasing to allow the output to switch.

If the distance between the optical module and the HOTLink Receiver is short (refer to "HOTLink Design Considerations" application note, Transmission Line Termination section) then the bias network may be placed anywhere between the optical module and the HOTLink Receiver. If this distance is long, then the interconnect traces must be treated as a transmission line and the bias network must be moved to the receive-end of the transmission line to also terminate the transmission line. If the transmission line impedance is other than 50 Ω, then different values of resistors are necessary (see Equation 3 and Equation 4).

Figure 12. PECL Optical Module to CY7C9689 Receiver

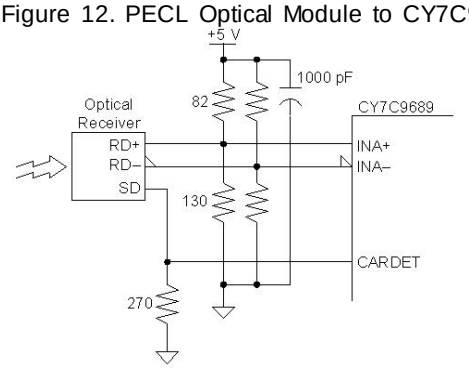
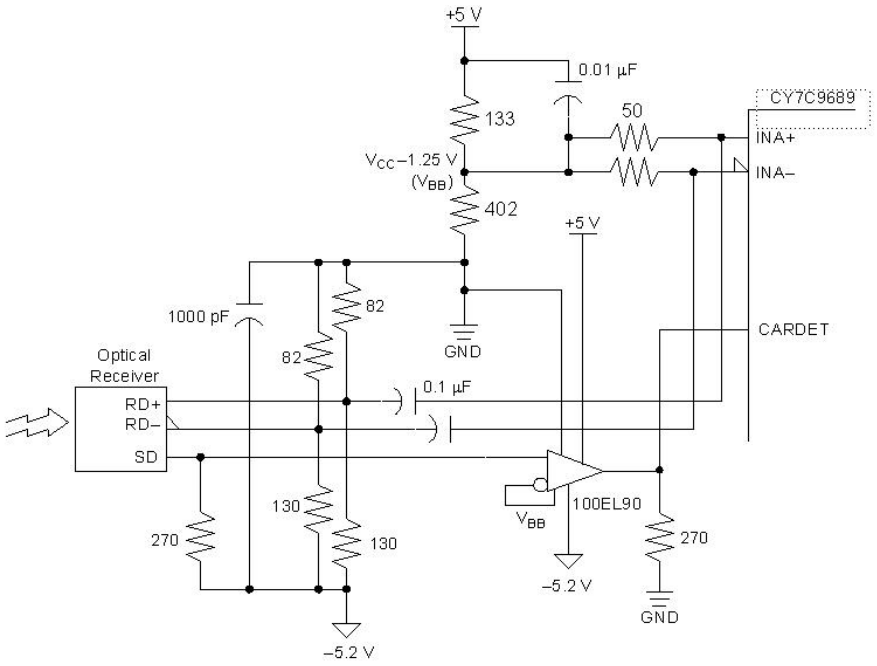


Figure 13. ECL Optical Module to CY7C9689




## Standard ECL Optical Modules

Optical modules with the Case pins connected to $V_{CC}$ are designed for use in a negative DC supply system. These types of modules may also drive a CY7C9689 Receiver.

By far the simplest method to interface to these modules is to connect it the same as a PECL module, with the exception of the Case pins. Here, instead of attaching the Case pins to ground ($V_{EE}$), they are attached to the positive supply ($V_{CC}$ or $V_{DD}$). If the case is metallic in nature, care must then be exercised such that it does not come into direct contact with ground.

If the optical module is used below ground it must be AC-coupled to the CY7C9689 Receiver. A schematic detailing this type of connection is shown in Figure 13. From a parts count standpoint this type of connection should be avoided if at all possible. Just as when connecting the CY7C9689 transmitter to negative referenced ECL optical modules, this interface requires biasing on both sides of the AC-coupling capacitors.

Because the signal detect output of the optical module is not an AC signal, capacitive coupling cannot be used to feed this signal into the CY7C9689 CARDET input.

The simplest thing to do here is to use an external ECL-to-PECL translator (as shown in Figure 13) to convert the signal-detect output to a PECL environment. An ECL-to-TTL translator may also be used if external resistors are added to shift the TTL switching level to the equivalent PECL levels.

The INA± differential inputs must be biased to near the midpoint of the common-mode range of the CY7C9689 Receiver. The two 50 Ω resistors tied to this synthesized reference point are sized to properly terminate the transmission line impedance of the interconnect.

## Receiving from Copper Media

The direct-coupled, capacitor-coupled, and transformer coupled configurations for copper interconnect are covered in the driving copper interface section of this document, with schematics of these connections shown in Figure 7 through Figure 11.

## Conclusion

The CY7C9689 TAXI Compatible HOTLink can be interfaced to any medium which the AMD TAXI is capable of driving. When compared to the TAXI chipset, the CY7C9689 has superior drive capability, wider common mode range and improved receiver sensitivity. This application note illustrates how to interface the CY7C9689 to standard media types and optical modules.

## .Document History

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| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| ** | 1509343 | SAAC | 09/25/2007 | New spec. |
| *A | 3388800 | SAAC | 10/05/2011 | Updated to latest template<br>Converted from FrameMaker to Word<br>Added Abstract |
| *B | 4546199 | YLIU | 10/21/2014 | Sunset Review<br>Updated template |
| *C | 5815605 | AESATMP9 | 07/13/2017 | Updated logo and copyright. |

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