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AN2405

PSoC® 1 I/O Power Structure - Determining V_{OH} and V_{OL} at Partial Load

Author: Dennis Seguine

Associated Project: No

Associated Part Family: CY8C20x34, CY8C21x34, CY8C24x23A, CY8C24x94, CY8C27x43, CY8C28x45, CY8C29x66

Software Version: PSoC® Designer™ 5.x

Related Application Notes: None

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AN2405 outlines a means to calculate the output voltages of the PSoC® device digital GPIO, when loaded at less than the rated maximum current. The internal routing resistances are presented for each of the listed PSoC 1 devices.

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Introduction

Most PSoC applications use GPIO connections to drive resistive loads. Worst case logic level outputs at maximum rated current are clearly specified in the target device datasheet. This may be insufficient information when the absolute value of the output level is important to the performance of the user's circuit. Examples include using a PWM as a source to a BPF2 User Module, using a PWM to implement a DAC, or when the loading device has V_{IL} or V_{IH} thresholds that are more restrictive than the specified maximum values for PSoC outputs.

The logic output levels (high and low) are functions of the output devices and the power routing on the device. A power distribution model of the PSoC is outlined that includes the geometric, voltage and temperature characteristics of the output devices, and routing.

There are four components of the resistance that limit output current delivery: lead frame, bonding wire, output devices, and power rail routing.

Bonding Wires

Bonding wires connect the device pads to the lead frame and have a typical resistance of 100 mΩ. V_{SS} and V_{DD} connections have multiple pads in some devices and multiple bonding wires in others.

Lead Frame

The lead-frame resistance varies with the package selected and each specific pin. Compared to the bonding wire, the output device, and the on-chip power rail routing, these values are very small. Smaller packages (QFN and BGA) have lead resistances in the range of 3 to 15 mΩ. Larger packages (SSOP, TQFP, SOIC, and PDIP) have lead resistances in the range of 10 to 70 mΩ. Longer leads have higher resistance, so pins in the corners have higher resistance than pins in the center of the part.

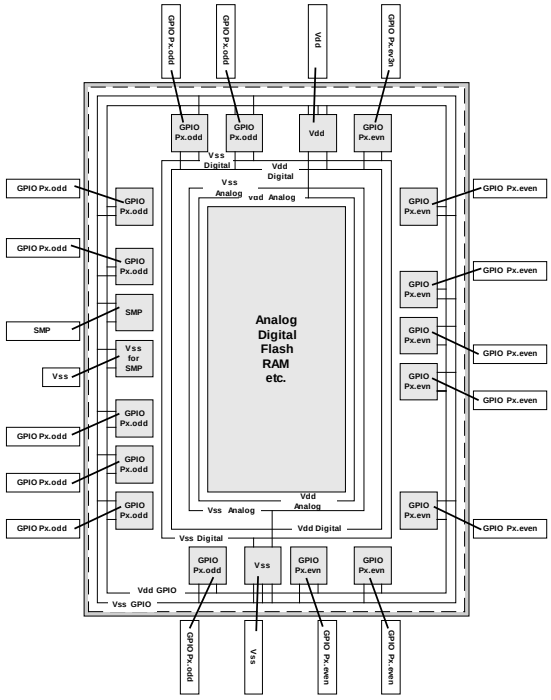
Power (V_{SS} and V_{DD}) Rails

The V_{SS} and V_{DD} power rails on the PSoC are concentric rings. Analog power and digital power are routed separately. An outline of typical PSoC power routing is shown in Figure 1.

The buses for digital, analog and I/O power systems come together at the V_{SS} and V_{DD} pad connections. This on-chip connection method has clear advantages. The interaction between load, digital, and analog signal currents is only at the power connection pads. This means that internal (logic, CPU, analog) currents have minimal effect on the GPIO output voltages. Correspondingly, the load currents have a minimal effect on the performance of the precision analog sections. The PSoC power distribution on-chip consists of three pairs of power rails for analog, digital, and I/O structures. The V_{DD} power rails are tied together at the bonding pad. The bonding pad is connected to the device's lead frame using a bonding wire.

Some devices (generally larger ones) and packages have multiple V_{SS} connections. This enables lower resistance V_{SS} connections, reducing noise in the analog section. Some connections are direct to individual pins. Other devices have V_{SS} wire-bonded to the main part of the lead frame (called the “paddle”) to reduce the resistance of the ground connection. This is seen in the CY8C24x23A example of Figure 11 in the Appendix A.

Figure 1. Typical PSoC Power Routing



The resistance of the power rails is identical for both V_{SS} and V_{DD}. The bonding pads on the device are not uniformly spaced; other features share the outer ring of the device with the bonding pads. The metallization on the device is aluminum, which has a resistance of the form:

$$R = R_{REF}\left(1+\alpha(T-20°)\right)$$

- α is the temperature coefficient of resistivity, equal to 0.004308.
- R_{REF} is the resistance at 20 °C

The routing resistance of the V_{SS} and V_{DD} rails shown in Figure 2 and Figure 3 is the worst case value at 25 °C, calculated from the design and layout detail, and confirmed by measurements taken during the device characterization process. The routing resistance at 100 °C will be about 33 percent higher than the values listed.

The details of the V_{DD} and V_{SS} output rail routing resistance for PSoC 1 devices is included in the Appendix A.

Output Devices

The output devices on each GPIO port are N-channel FETs driving (sinking) current to V_{SS} and P-channel FETs driving (sourcing) current from V_{DD}. Separation of the threshold voltages of these devices guarantees that they are never on at the same time.

FETs operating in the linear region (i.e., not turned fully on) source (or sink) a current that is dependent on the gate-to-source voltage (V_{GS}) and the device's threshold voltage (V_{TH}):

$$I_D = I_{DD} * (V_{GS} - V_{TH})^2$$

The internal logic levels swing from rail-to-rail, thus the V_{GS} is equal to V_{DD} for the N-FET and -V_{DD} for the P-FET. V_{DD} is considerably higher than the V_{TH}, so for the operating range of V_{DD} for the PSoC and the purposes of this model, the on-resistance is modeled as a first order equation with a negative coefficient on the supply voltage term.

The threshold voltage of a FET has a positive temperature coefficient. As temperature increases, the difference between V_{GS} and V_{TH} drops. At a fixed V_{GS} (=V_{DD}) then, the device conducts less current as the temperature increases. Thus the output resistance increases with the temperature.

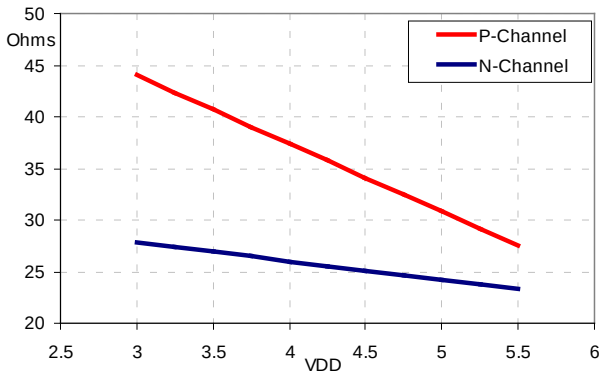
Based on characterization data for the CY8C24x23A, the output resistance of the N-channel devices (sinking current) and the P-channel devices can be modeled as:

$$R_{DS-N} = 33.2 - 1.8Vdd + 0.04(T - 25)$$

$$R_{DS-P} = 63.8 - 6.6Vdd + 0.066(T - 25)$$

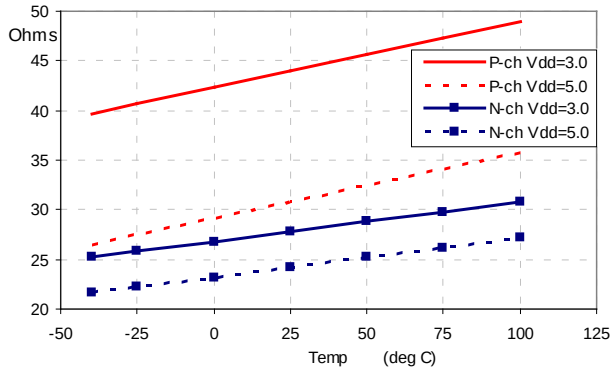
At room temperature, the voltage dependence of the FET's resistance can be seen in Figure 2.

Figure 2. FET Resistance vs V_{DD} at Room Temperature



The temperature dependence of the FET's resistance can be seen in Figure 3. Again, these values are estimates based on the design and the characterization data.

Figure 3. FET Resistance vs Temperature



The layout of the PSoC I/O cell is symmetrical; the N-channel and the P-channel devices are the same size. For the same size devices, the on-resistance of the N-channel device is lower than that of the P-channel device. Typical applications require more sinking current than sourcing current. This is a design hold-over from the (good old) days of TTL logic. The use of like-sized devices for N- and P-output drivers is a reasonable design choice for almost all applications.

The GPIO cells of all PSoC 1 devices are identical. They all have the same output resistance. The power distribution rails are equal width and vary only in length.

Ohm's Law Manipulation

Calculating the output voltage for a given pin with a given load is a matter of applying Ohm's law, Kirchhoff's law, and simple algebra to a large, simple network. The output voltage on unloaded pins may be of importance. An example is an LED on one pin and unloaded logic levels on other pins. You could enter the network into a SPICE simulation, or have that summer intern build it into a spreadsheet.

Let us do rough numerical calculation for an example at the room temperature:

Example: CY8C24423 PDIP 28

V_{DD} = 5.0 V, T = 25 °C

20 mA load into P1[6]

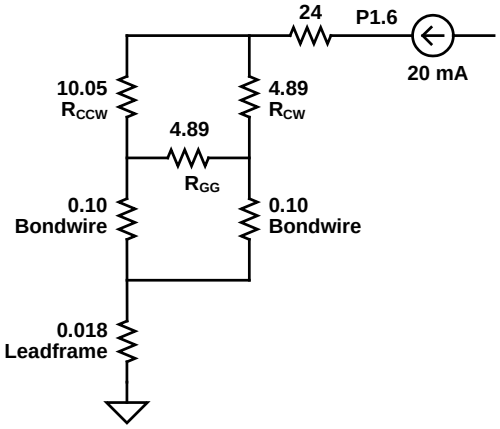
Find V_{OL} at P1[6]

V_{OL} at P2[0] unloaded

V_{OL} at P1[0] unloaded

We will start with a simplified schematic, reduced from Figure 11 to summed resistances in Figure 4. The resistance from the pin to V_{SS} is split, clockwise around the chip from the pin to V_{SS} (R_{CW}) and counter-clockwise around the chip from the pin to V_{SS} (R_{CCW}). These values will vary as a result of the pin location.

Figure 4. Simplified Routing Resistance



Resistance from P1[6] to V_{SS} pad (the short way - clockwise) is summed from the listed values in Figure 11 in the appendix, routing resistance for CY8C24x23.

$$R_{CW} = 1.35 + 0.27 + 0.27 + 3.0 = 4.89\Omega$$

Resistance from P1[6] to V_{SS} pad (the long way - counter clockwise), accounted in the same manner, is

$$R_{CCW} = 0.27 + 0.27 + ... + 0.81 = 10.05\Omega$$

Bond wire resistance (R_{BW}) = 0.1 Ω each path

Lead frame resistance = 0.018 Ω

P1[6] N-FET output resistance = 24.0 Ω

Initially let us neglect the resistance between the V_{SS} pads (R_{GG}), which amounts to about 5.0 ohms.

The V_{SS} resistance from P1[6] N-FET source to PCB is the resistance clockwise around the short side of the loop in parallel with the resistance counter-clockwise around the long side of the loop.

$$R_{OUT} = (R_{CW} + R_{BW}) \| (R_{CCW} + R_{BW}) + R_{LF}$$

$$R_{OUT} = \frac{1}{\frac{1}{4.89 + 0.1} + \frac{1}{10.05 + 0.1}} + 0.018$$

$$R_{OUT} = 3.36\Omega$$

$$V_{OL_P1.6} = 0.02A(24 + 3.36) = 0.547V$$

Let us go back and check the accuracy of the assumption that we could neglect the resistance of the route between the two V_{SS} connections.

The voltage at the top end of short-side bond wire is

$$V_{BWShort} = \frac{0.1}{0.1 + 4.89}(0.547 - 0.02A * 24) = 1.34mV$$

The voltage at the top end of long-side bond wire is

$$V_{BWLong} = \frac{0.1}{0.1 + 10.05}(0.547 - 0.02A * 24) = 0.66mV$$

The voltage drop between these two points is

= (1.34 mV - 0.66 mV) = 0.68 mV

So, the current between them is

= 0.68 mV/4.89 Ω

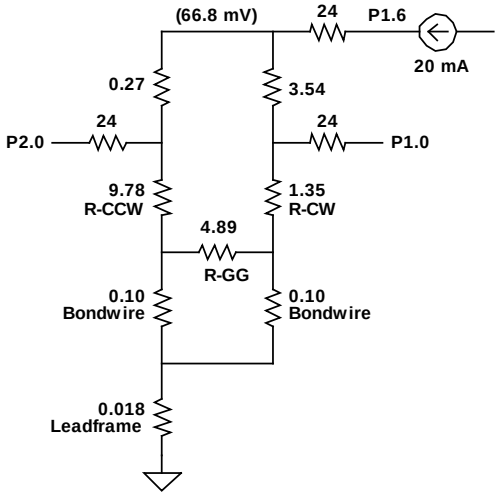
= 0.139 mA

This is small compared to the total current (20 mA) and means that the earlier estimate that this part of the routing loop could be neglected is correct.

Voltage at Unloaded Pin

The V_{SS} rail at the source of P1[6]'s output FET is at 3.36 Ω * 20 mA = 67.2 mV. Thus, other output pins in question, P1[0] and P2[0] will not be at zero volts. We will use a slightly more complex version of the V_{SS} routing resistance, shown in Figure 5.

Figure 5. Routing Resistance for Unloaded Pins



P1[0] is between P1[6] and V_{SS}. The voltage at P1[0] for no load current is the voltage at the source of P1[0]'s N-FET.

$V_{OL_P1.0}$ = (1.35+0.1)/(3.54+1.35+0.1)*67.2 mV = 19.5 mV

P2[0] is very close to P1[6] (... it is a long way around to loop the V_{SS} terminal next to P2[1]). The voltage at P2[0] for no load current is the voltage at the source of P2[0]'s N-FET.

$V_{OL_P2.0}$ = (9.78+0.1)/(9.78+0.27+0.1)*67.2 mV = 65.4 mV

V_{OL} at both P1[0] and P2[0] is not at zero volts even when there is no load current into these pins because the voltage on the bus is non-zero and distributed. More load currents raise the bus voltage even more. Since there is no load current on these pins, the 24-Ω N-FET resistance does not affect the output voltage.

This was obviously a trivial example; distributed loads beget more complex calculations. This is a simple exercise for SPICE; it is strictly a matter of data entry.

Summary

Calculation of PSoC logic output voltage under load is a straight-forward but tedious exercise. The V_{OH} and V_{OL} values on any pin can be calculated to assure that logic level and other requirements of external loads can be met. From the structure of the power routing, we can infer obvious design steps to drive the unloaded outputs closer to the rails if this is an issue in the user's application.

1. Most of the drop comes from the FET output resistance . . . NOT the metal routing resistance. For high current applications, use the multiple pins in parallel.
2. It is clear that to deliver high currents without degrading the V_{OH} and V_{OL} of unloaded outputs, these unloaded outputs must be placed as close to the V_{SS} pins as possible.
3. Calculate your outputs at the full range of temperature and voltage expected in your product. Add some margin. While the estimates on routing and output FET resistance were made in good faith, they are still estimates.

Author's Note

After years of study and practice, the author is still messing around with Ohm's law. It is still fundamental; software has not completely taken over the world.

About the Author

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Title:	Applications Engrg MTS

Appendix A

Figure 6. CY8C20x34 V_{DD} Routing

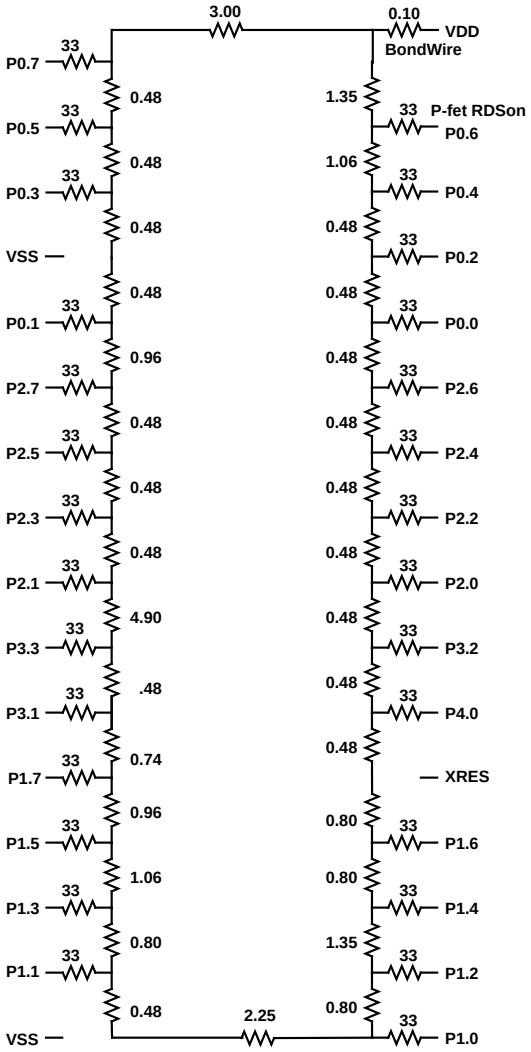


Figure 7. CY8C20434 V_{SS} Routing

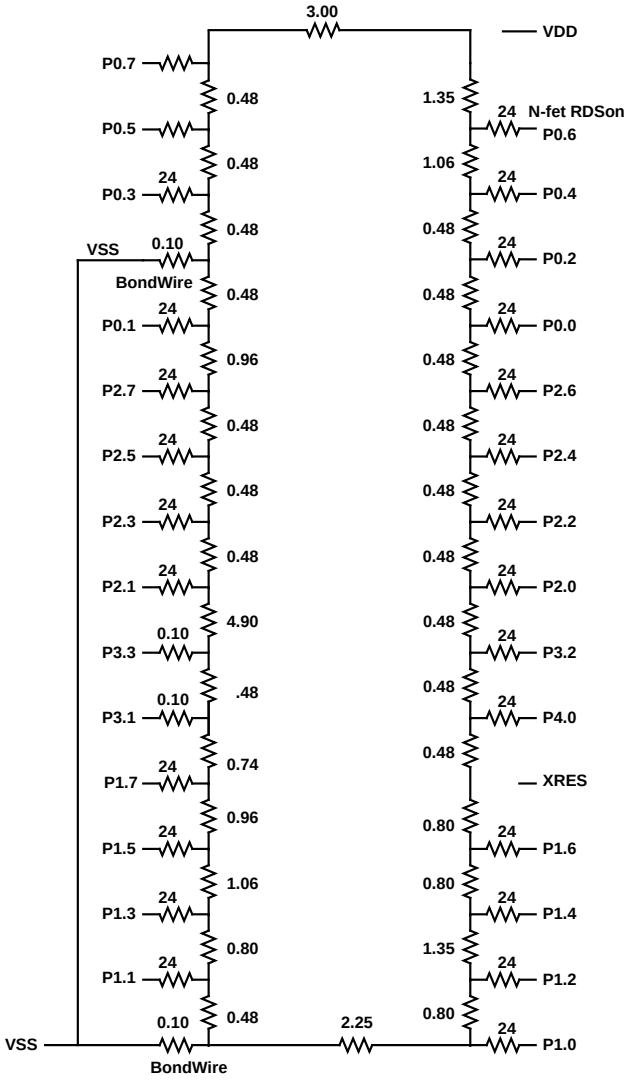


Figure 8. CY8C21434 V_{DD} Routing

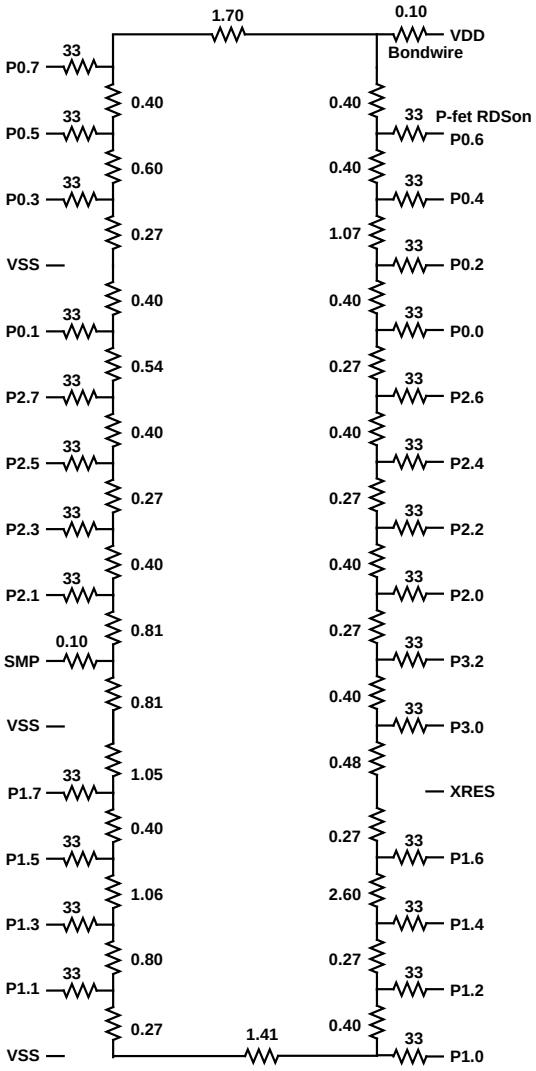


Figure 9. CY8C21434 V_{SS} Routing

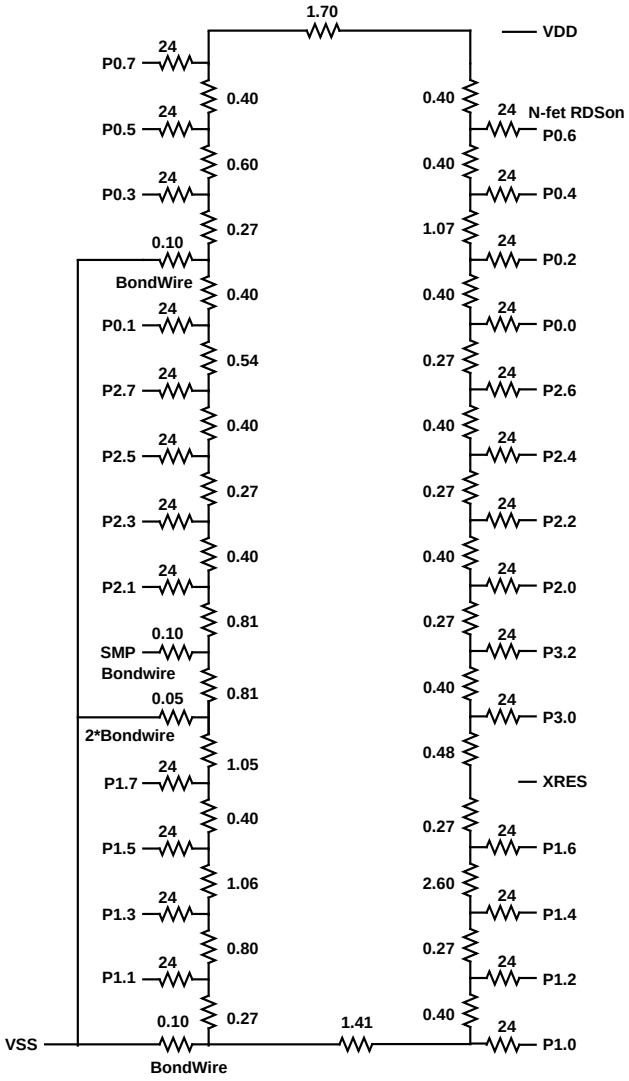


Figure 10. CY8C24x23A V_{DD} Routing

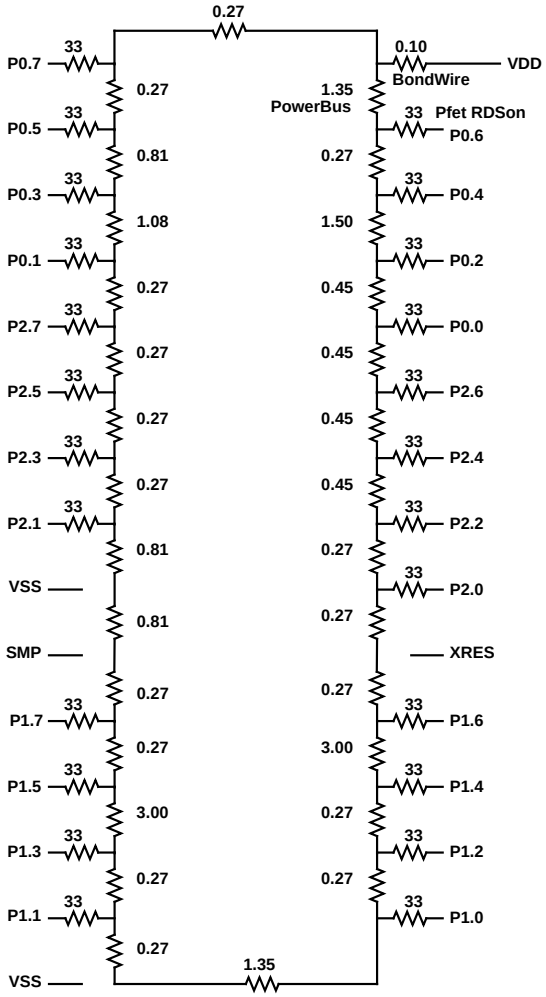


Figure 11. CY8C24x23A V_{SS} Routing

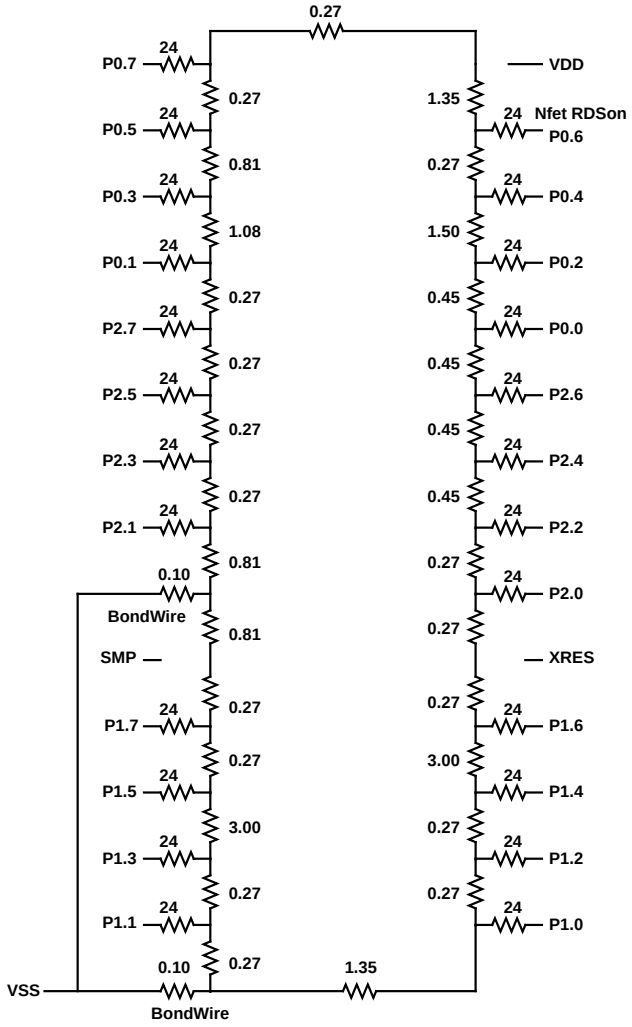


Figure 12. CY8C24x94 V_{DD} Routing

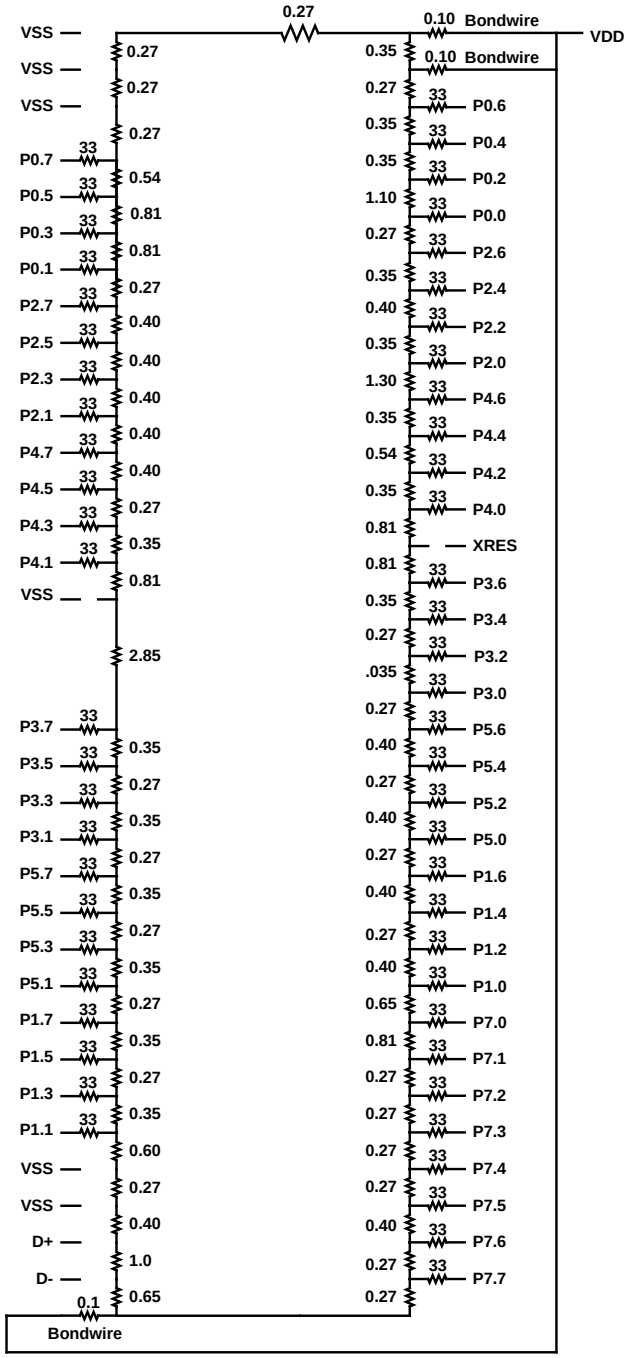


Figure 13. CY8C24x94 V_{SS} Routing

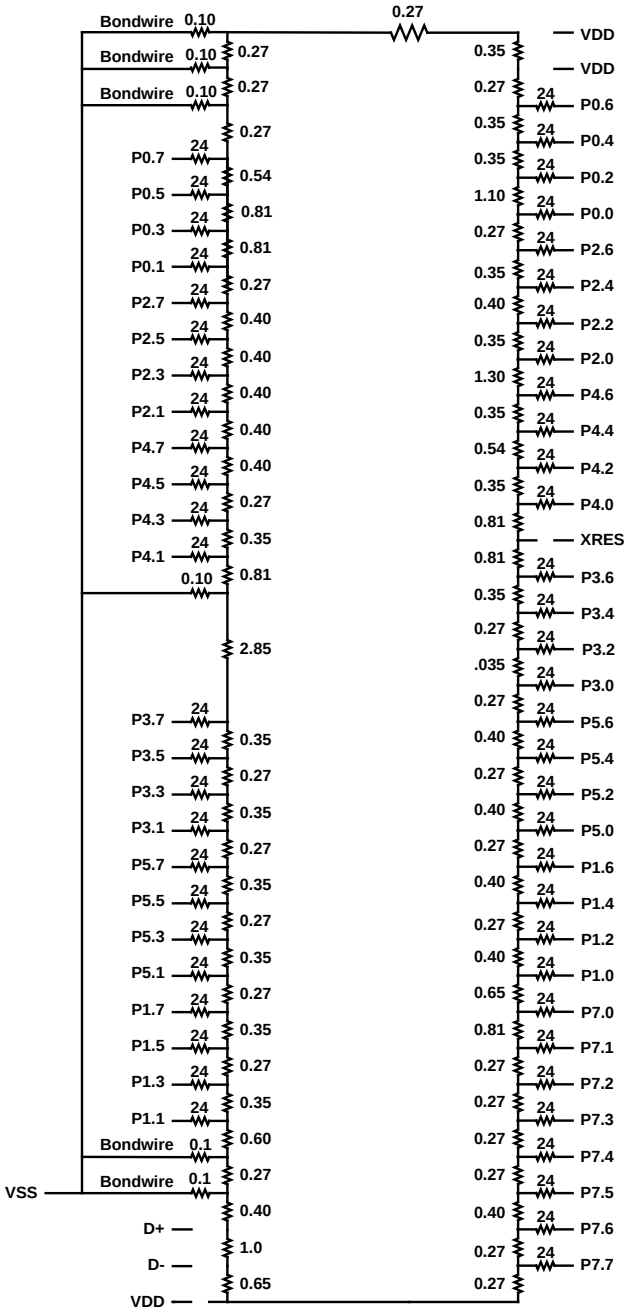


Figure 14. CY8C27x43 V_{DD} Routing

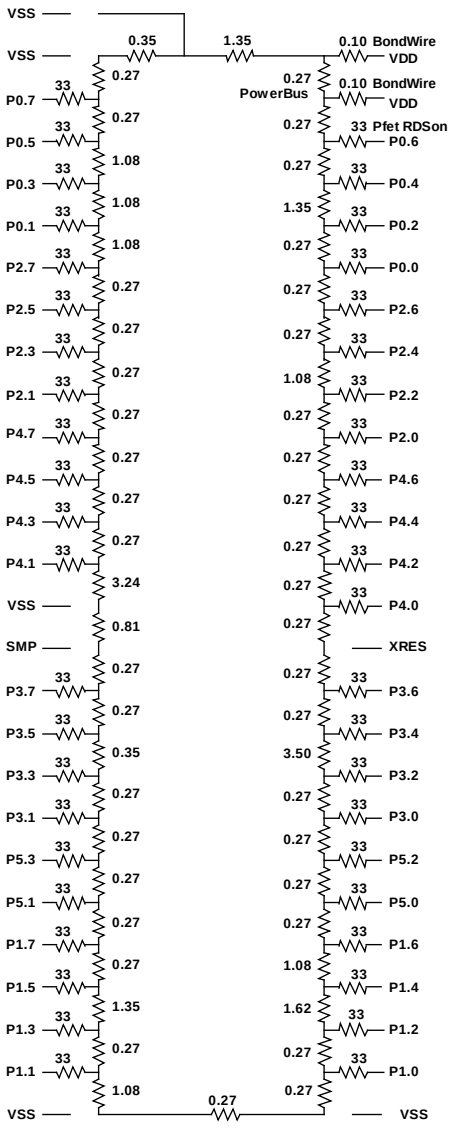


Figure 15. CY8C27x43 V_{SS} Routing

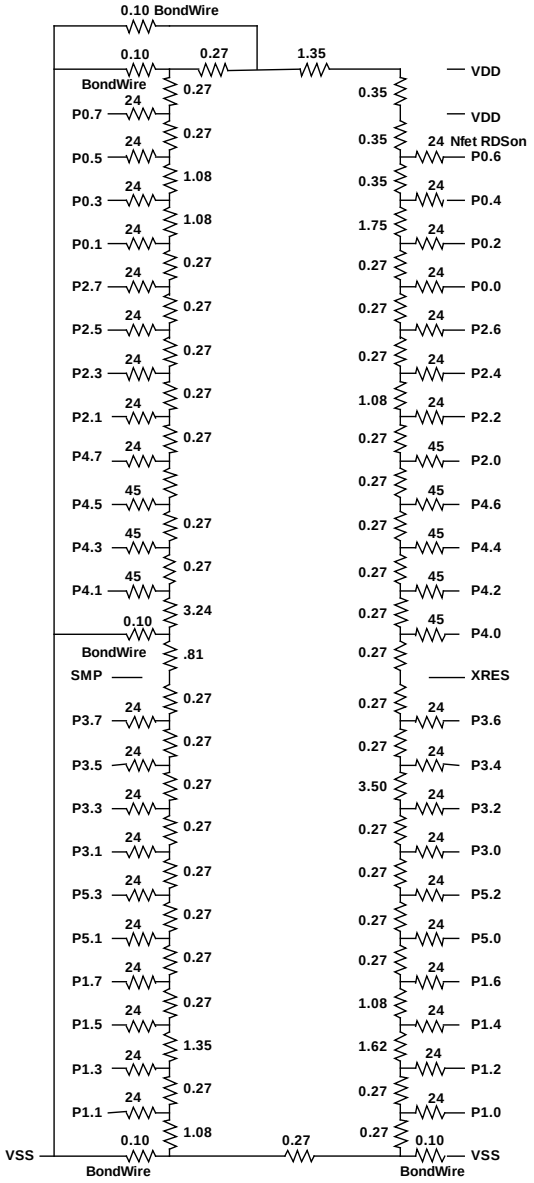


Figure 16. CY8C28x45 V_{DD} Routing

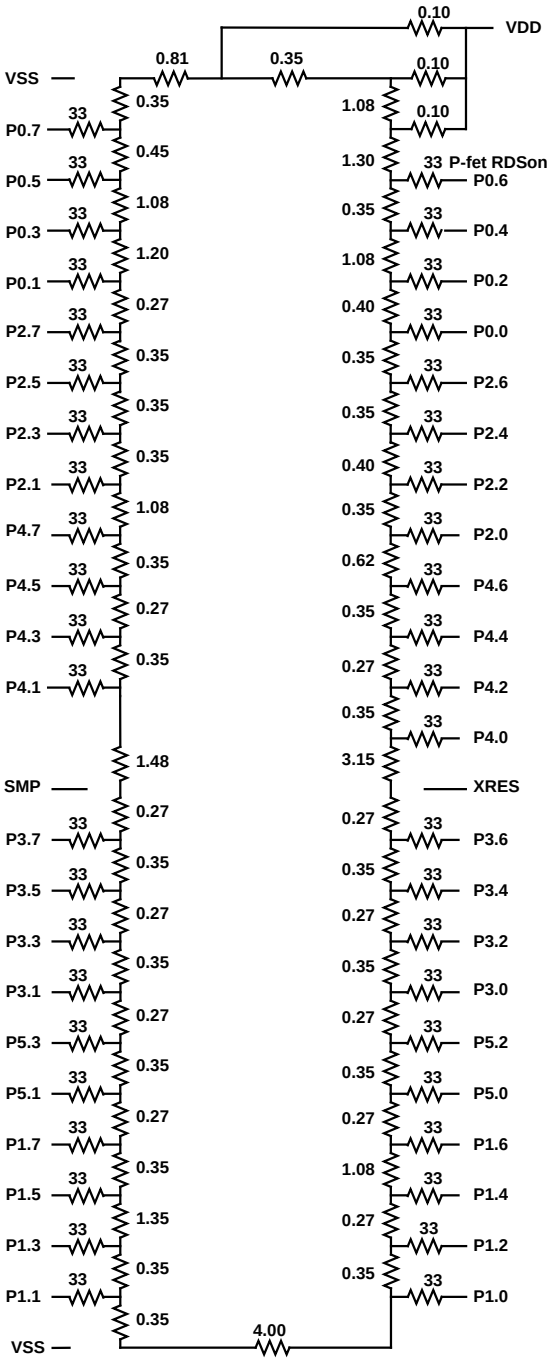


Figure 17. CY8C28x45 V_{SS} Routing

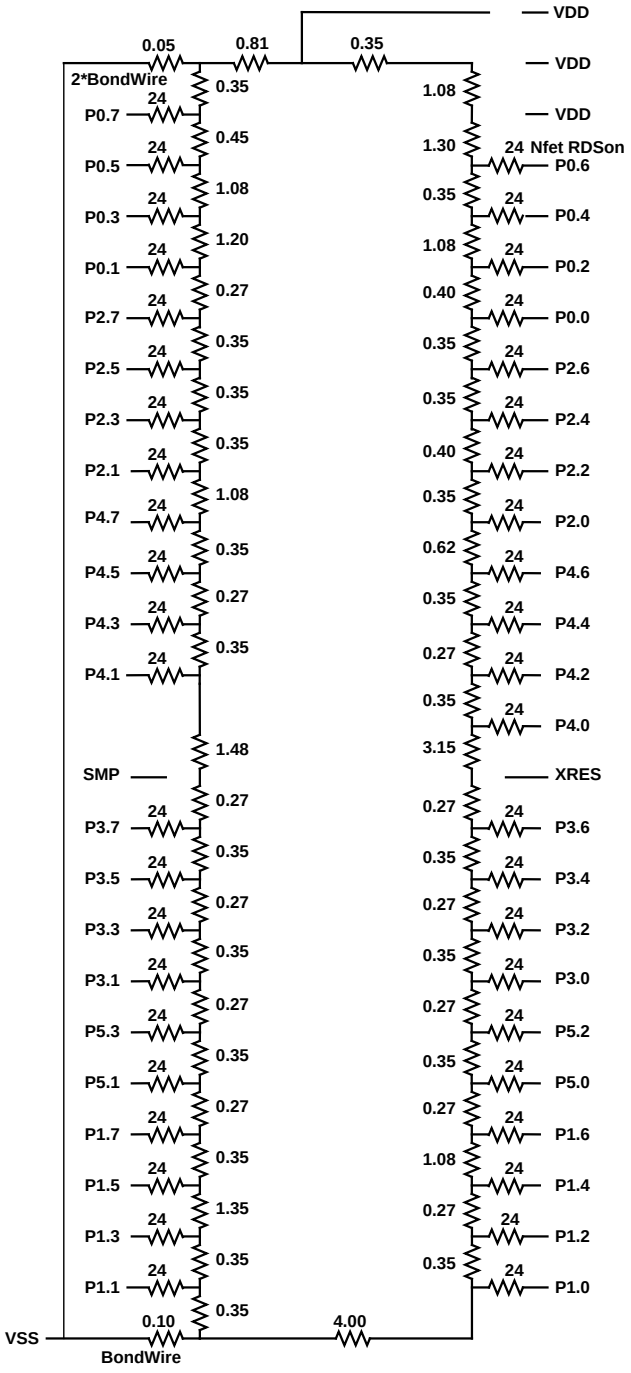


Figure 18. CY8C29x66 V_{DD} Routing

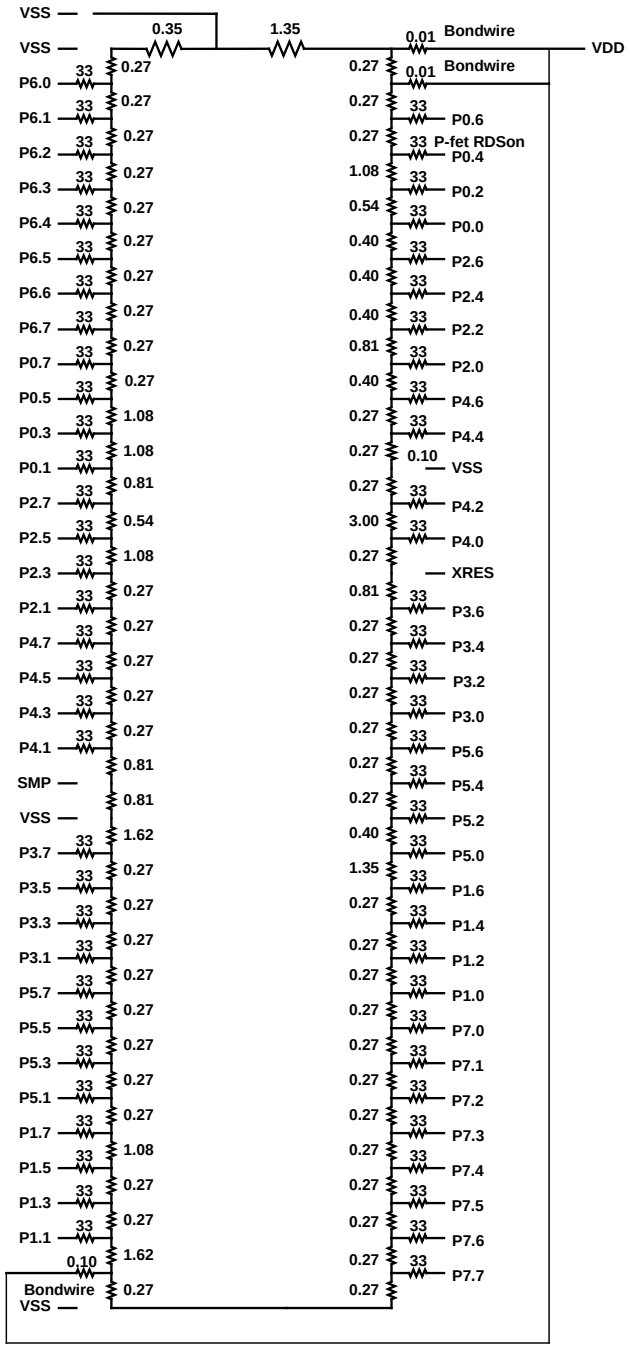
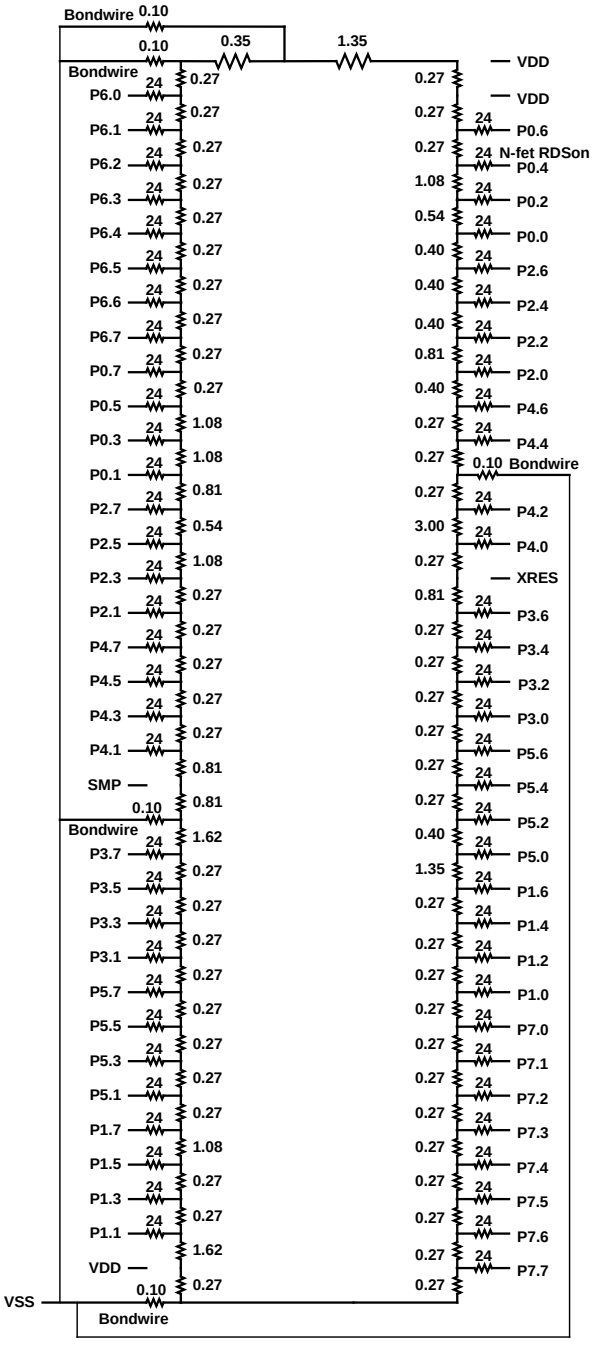


Figure 19. CY8C29x66 V_{SS} Routing



Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1541089	SEG	10/03/2007	New Spec.
*A	3247371	SEG	05/03/2011	Update text on lead frame, reformat graphics, add appendix for more chips.
*B	3432728	SEG	11/08/2011	Updated text for clarification and updated template.
*C	4390198	SEG	05/26/2014	Updated in new template. Completing Sunset Review.

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