Digital control strategies to improve the light load efficiency of phase-shift full-bridge converters

Using XMC4200 to realize hybrid control technique

About this document

Scope and purpose

Phase-shift full-bridge (PSFB) converters are popularly used in medium- or high-power applications nowadays because PSFB has the inherent zero-voltage-switching (ZVS) characteristic with no additional circuits. However, PSFB has some drawbacks: its lagging leg hardly achieves ZVS at light loads, and higher circulating current losses for primary switches especially in high input voltage and light-load conditions. This application note discusses how to address these issues and reduce the circulating current loss using hybrid digital control strategies.

Intended audience

This application note is intended for design engineers who wish to use digital control strategies with XMC™ microcontrollers to control high-power SMPS such as PSFB converters, and learn about the design process.

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1 Introduction

Compared to other traditional isolated topologies, full-bridge converters have lower voltage and current stress, and therefore are generally applied to medium- or high-power and high-voltage applications. PSFB converters with their intrinsic ZVS functionality with no additional auxiliary circuits provide a higher overall efficiency above a certain load compared to conventional full-bridge converters with PWM control. However, these full-bridge converters have a few drawbacks such as the following:

- **Circulating current loss:** PSFB generates a specific circulating current interval during its control period; the energy in the primary side in this circulating interval is not transmitted to the secondary side. It is consumed only in the primary side during this circulating interval. This is called the “circulating current loss” – a major issue with PSFB.
- **Limitations on ZVS across the load range:** It is hard for PSFB to expand its ZVS in the entire load range; in addition, its ZVS functionality is lost especially at light-load conditions, leading to lower efficiency.
- **Parasitic ringing:** The primary-side energy cannot be effectively transferred to the secondary side because of the duty cycle loss, leading to parasitic ringing of the voltage surge in the secondary side.

This application note focuses on how to enhance the overall efficiency and performance of PSFB. Some literature ([4], [5]) adopts the PWM method to control the conventional full-bridge converter at light loads. This is because the PWM method does not generate as much circulating interval as PSFB (which has a larger circulating current loss at light loads). On the contrary, because the conventional PWM full-bridge converter does not have ZVS, it decreases the efficiency as the output load becomes heavier. Therefore, conventional PWM full-bridge converter is not suitable to apply to medium- or high-power applications.

Based on these reasons, this application note proposes a hybrid control technique, accomplished using Infineon’s XMC4200-Q48x256 MCU as the digital controller. At light loads, the digital controller executes conventional PWM control to improve light-load efficiency by reducing the circulating current loss. When the load gets heavier, its operating mode switches to phase-shifted modulation mode, enhancing the efficiency for higher loads using its ZVS characteristic.

1.1 Full-bridge converter with PWM control and phase-shift control

As shown in Figure 1:

The full-bridge converter architecture has the following components:

- Four main power switches in the primary side (Q1, Q2, Q3, Q4)
- Main transformer (T1)
- Secondary-side output diodes (D1, D2, D3, D4)
- Output inductance (L_O)

The following parameters are indicated in the diagram:

- V_{in}: Input voltage
- V_{pri} and V_{sec}: Primary-side and secondary-side output voltages of the transformer
- QD1 – QD4 and CS1 – CS4: Body diodes and the parasitic capacitance of the four main power switches
- C_b: Blocking capacitor used to avoid flux imbalance
- L_r: Resonant inductance or the leakage of transformer T1
- V_{AB}: Voltage difference between the center of the two bridge legs

- N_p,N_s: Transformer turns of the primary and secondary sides. n = N_p/N_s represents the turns ratio of the transformer
- C_O, R_O: Equivalent output capacitor and output resistance of this circuit

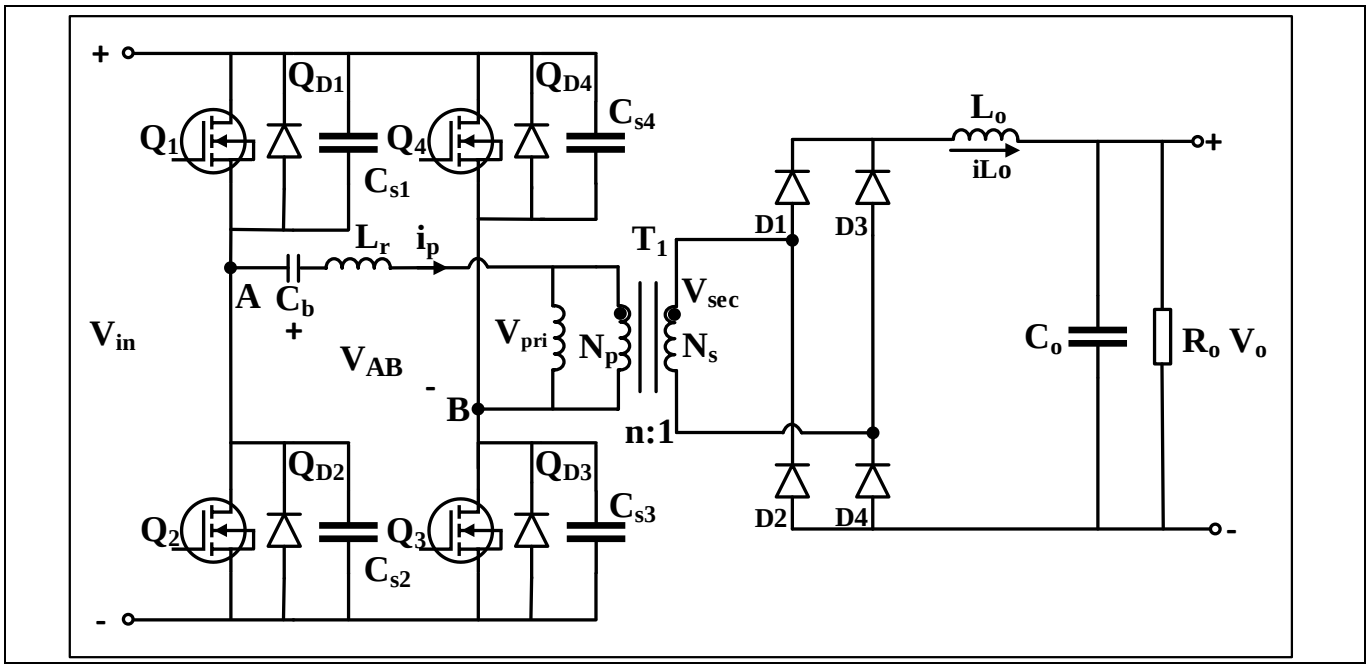

Figure 1 Conventional full-bridge converter with full rectification output

1.1.1 Full-bridge converter with PWM control

The PWM control method is widely used in conventional full-bridge converters, and is achieved by the driver signal synchronal conduction or cut-off of two diagonal power switch pairs (Q1, Q3) and (Q2, Q4) as shown in Figure 1.

The duty cycle width (DTs) of each diagonal power switch pair will be not greater than half of its switching period (T_S). Therefore, this switching mechanism generates alternate positive and negative square wave voltage (V_{pri}) in the primary side and then transfers this energy to the secondary side, making the secondary side generate a similar AC square voltage waveform relative to the primary side. Lastly, you can get a stable DC voltage by outputting the rectification of diode D1~D4, output inductance L_O, and output capacitor C_O. Furthermore, the amplitude of this stable DC output voltage can be accomplished by designing the DTs and the turns ratio (n) of the main transformer. Figure 2 shows the typical controlling waveform of the PWM full-bridge converter.

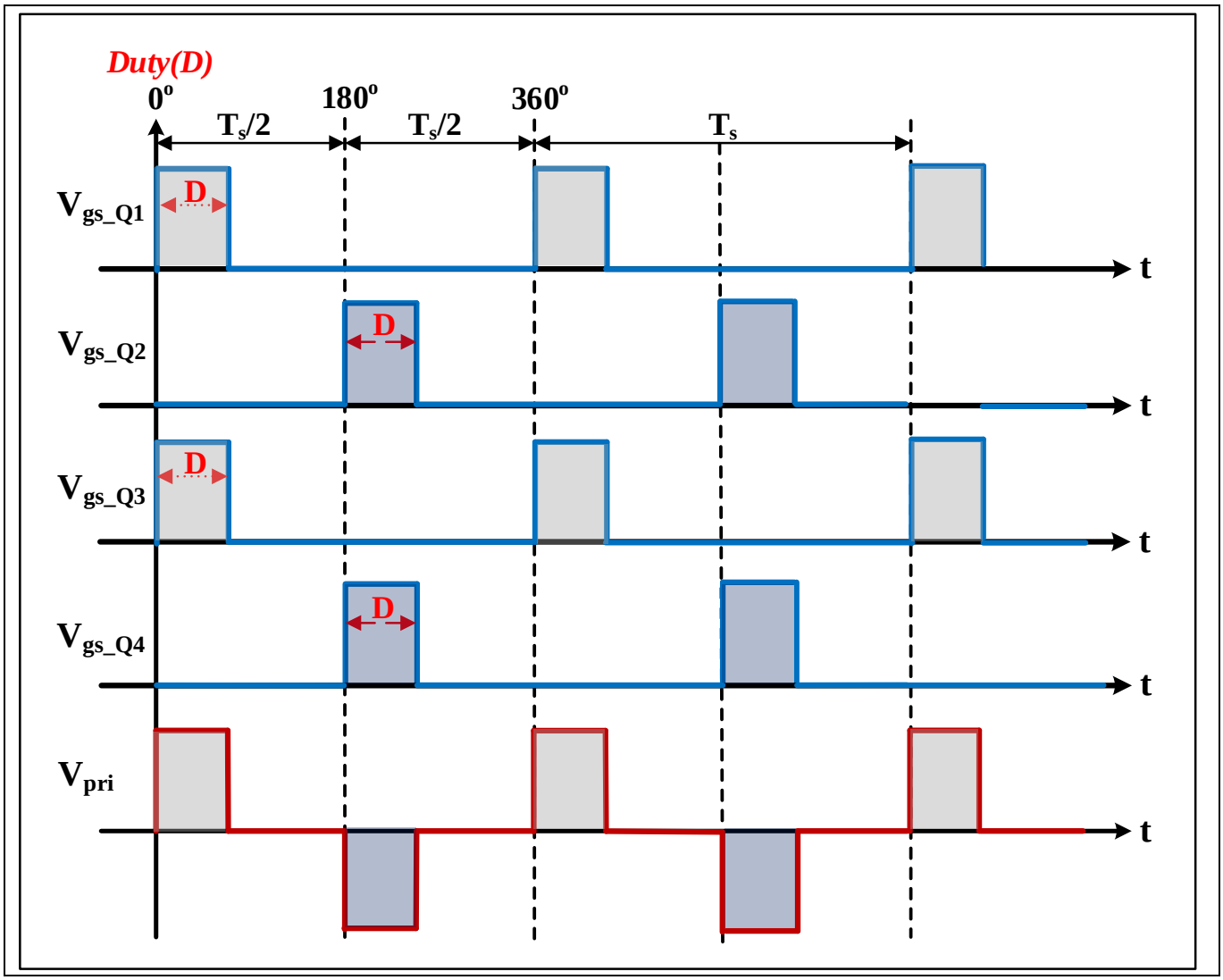

Figure 2 Typical control waveform of a full-bridge converter with PWM control method

1.1.2 Full-bridge converter with phase-shift control

Another common strategy to control a full-bridge converter is phase-shift control. The drive signals of power switches Q1 and Q2 are in fixed-frequency and approximately in the 50 percent fixed duty cycle. These two power switch signals are entirely complementary. Simultaneously, a dead-time exists between Q1 and Q2 driver signals in their switching moments.

The control pattern of Q3 and Q4 power switches is the same as Q1 and Q2 power switches. Still, the timing of the driver signal between (Q1, Q3) or (Q2, Q4) is designed with an adjustable duty cycle overlap width and the adjustable range is from 0 to $T_S/2$. Sometimes, the adjustable range is also called “controllable phase shift angle (ψ)”, which ranges from 0 to 180 degrees.

Through this controllable duty cycle overlap width or the phase shift angle (ψ), you can control the output voltage of a full-bridge converter and maintain its stability. The typical controlling waveform of PSFB is shown in Figure 3.

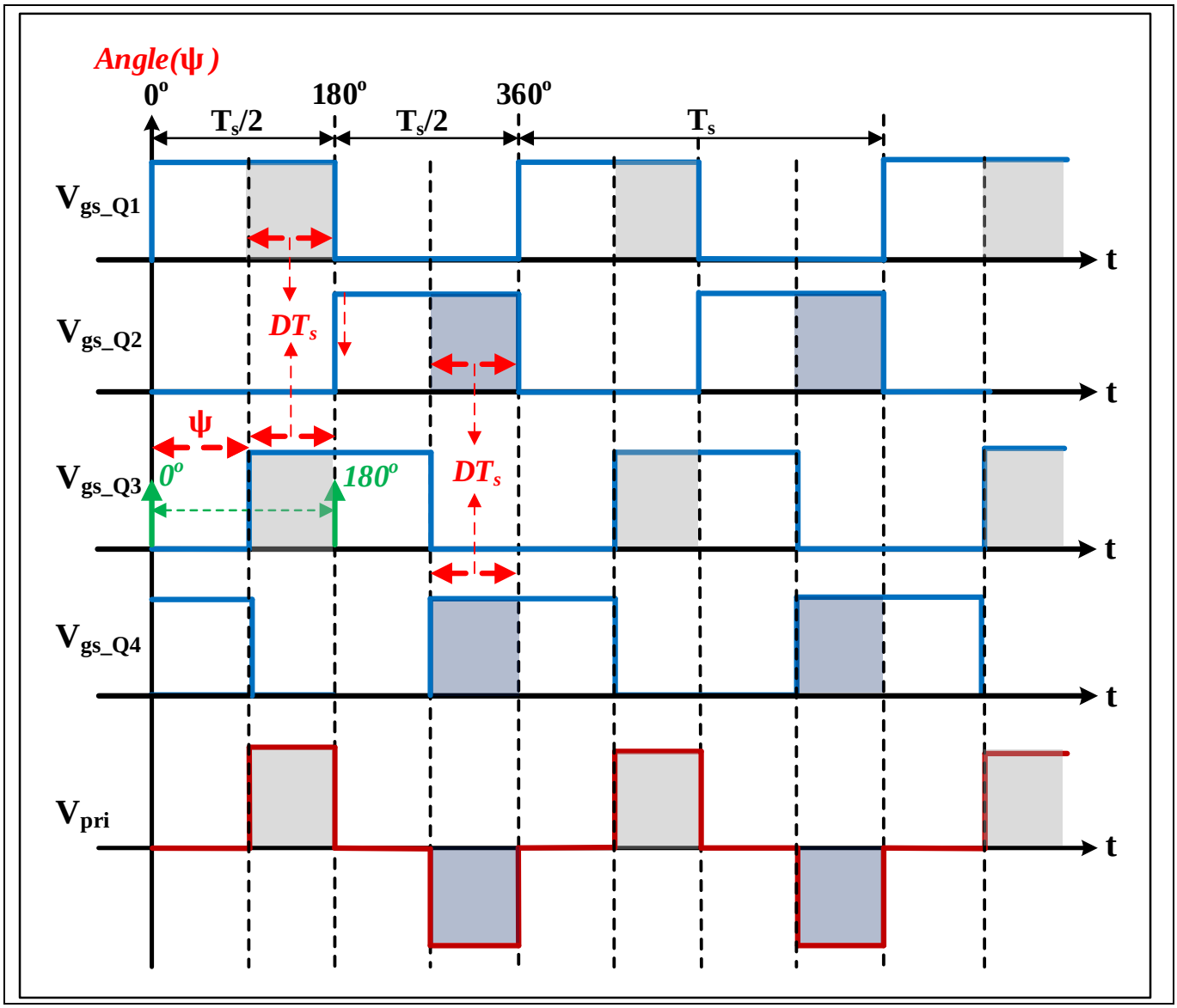

Figure 3 **Typical control waveform of a full-bridge converter with the phase-shift control method**

2 Circulating current interval in PSFB

The circulating current phenomenon is a specific interval generated in the PSFB controlling sequence, as shown in Figure 4. Comparing between PSFB and PWM control, the latter does not generate a circulating current area. In the figure, [t0, t2] is the duty cycle overlap area of driver signals for Q1 and Q3, an interval where the positive half-period energy can be transferred. On the other hand, [t5, t7] is the duty cycle overlap area of driver signals for Q2 and Q4, an interval where the negative half-period energy can be transferred.

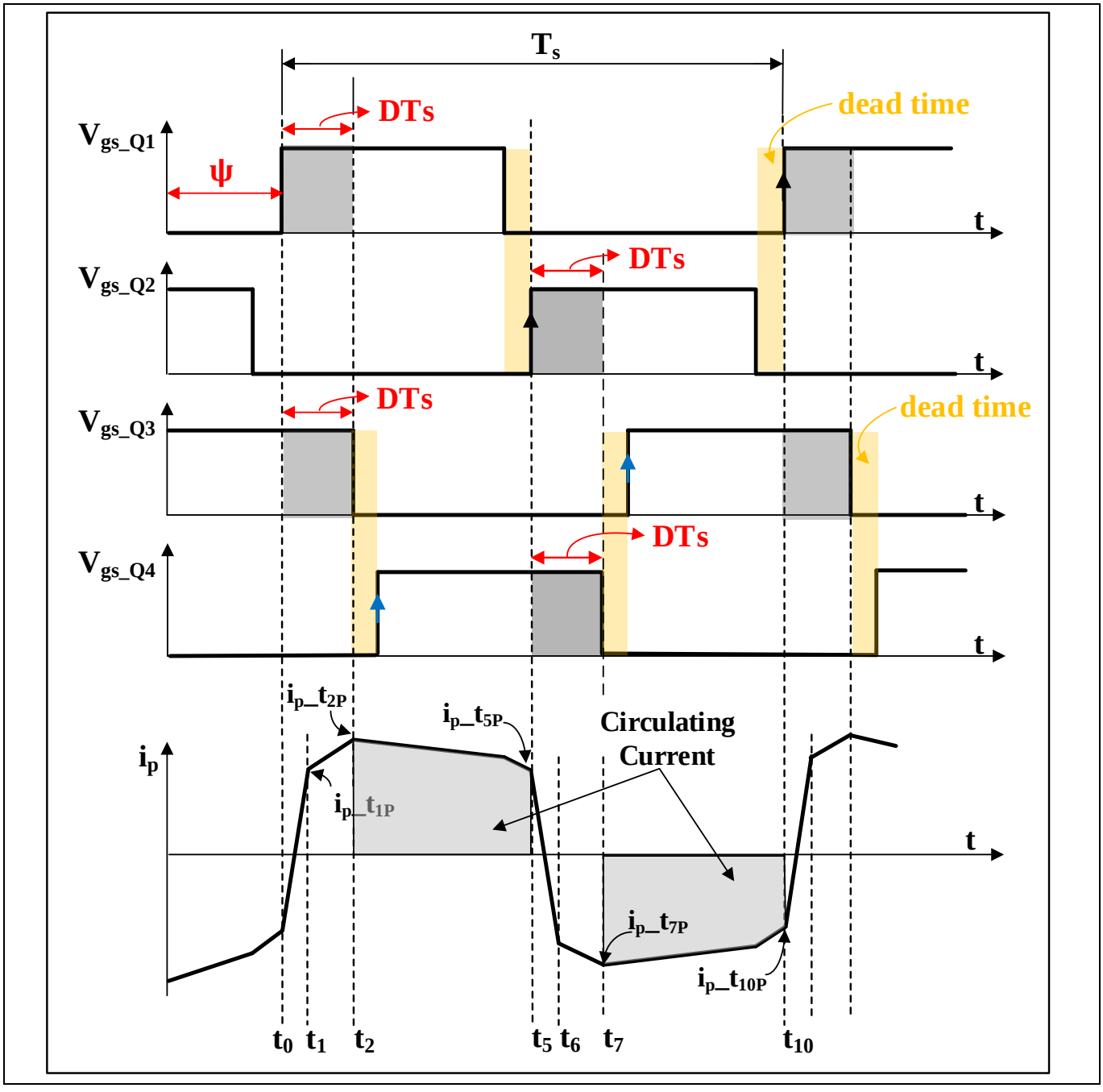

Figure 4 PSFB circulating current intervals

Moreover, in [t2, t5] and [t7, t10] intervals, the current circulates only in the primary side. The circulated energy does not transfer to the secondary side, which is regarded as a redundant loss. This is called the “circulating

current loss" in the primary side. In addition, a higher circulating loss is generated at light-load conditions because a smaller DT is obtained. In other words, a smaller duty cycle is equivalent to a larger circulating current interval existence.

In general, the leading leg of the PSFB converter consists of power devices that turn on after a circulating current interval. As for the lagging of the PSFB leg, it is defined as the power devices that get turned on after the energy transfer. In Figure 4, the driver signal pair (Vgs_Q1-Vgs_Q2) is the leading leg as they are turned on after a circulating current interval, while the driver signal pair (Vgs_Q3-Vgs_Q4) is the lagging leg as they are turned on after the energy transfer. The phase shift angle (ψ) can be generated from the driver signal pair (Vgs_Q1-Vgs_Q2) with respect to the driver signal pair (Vgs_Q3-Vgs_Q4), as shown in Figure 4. On the other hand, the phase shift angle (ψ) can also be generated from the driver signal pair (Vgs_Q3-Vgs_Q4) with respect to the driver signal pair (Vgs_Q1-Vgs_Q2).

2.1 Circulating current loss in [t_2~t_5] and [t_7~t_{10}] intervals

Figure 5 is the current path and equivalent circuit diagram of a PSFB positive half-period circulating current interval [t2, t5]. In this case, the primary side current only flows through Q1 to Q4, and the secondary side turns into a short-circuit condition; the output energy is provided only by the output capacitance.

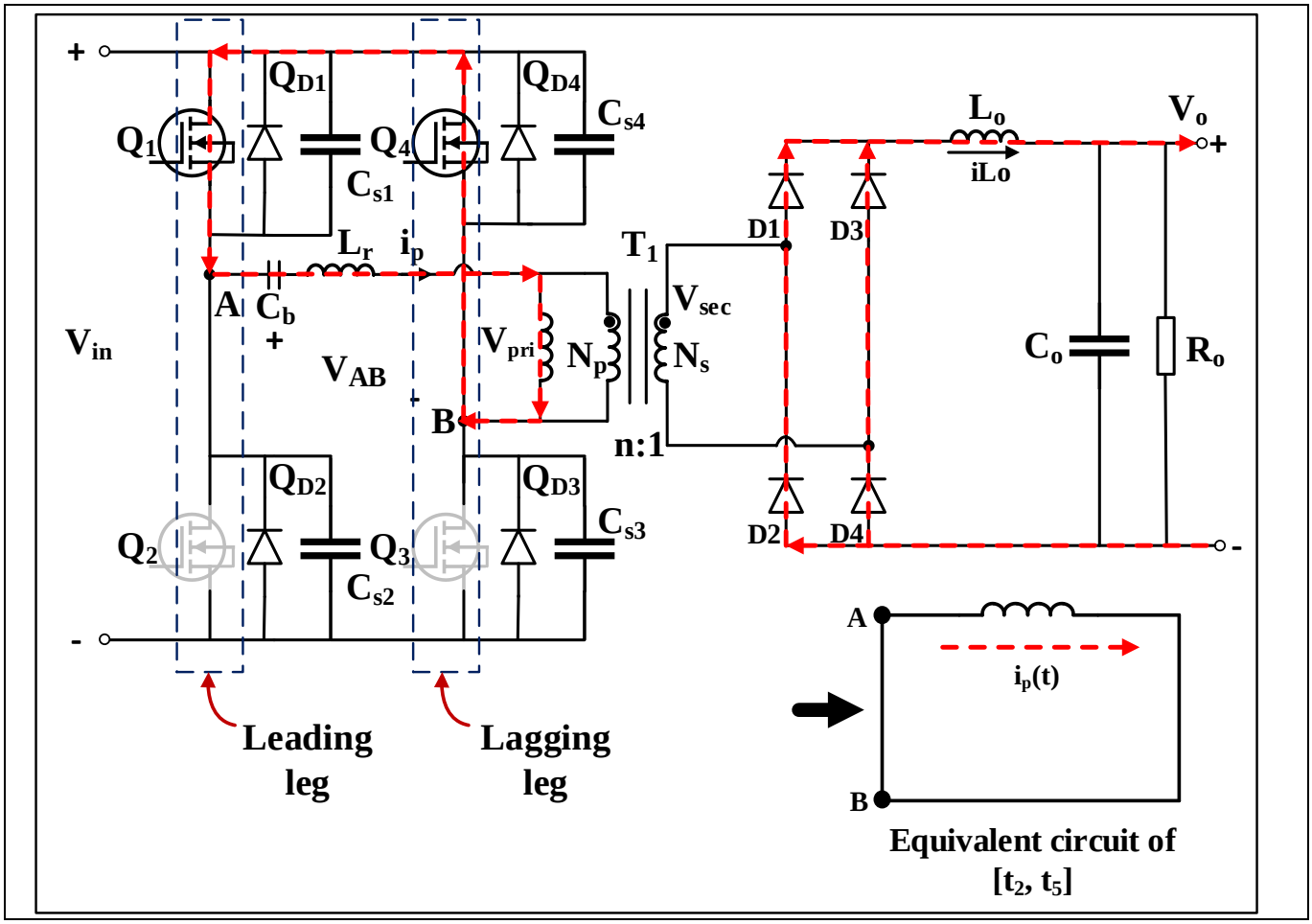

Figure 5 Current path and equivalent circuit diagram of circulating current interval [t2, t5]

Figure 6 is the current path and equivalent circuit diagram of a PSFB negative half-period circulating current interval [t7, t10]. In this case, the primary side current flows only through Q2-Q3, and only the circulating current direction is contrary to that of the positive half-period; the rest of the characteristics are the same.

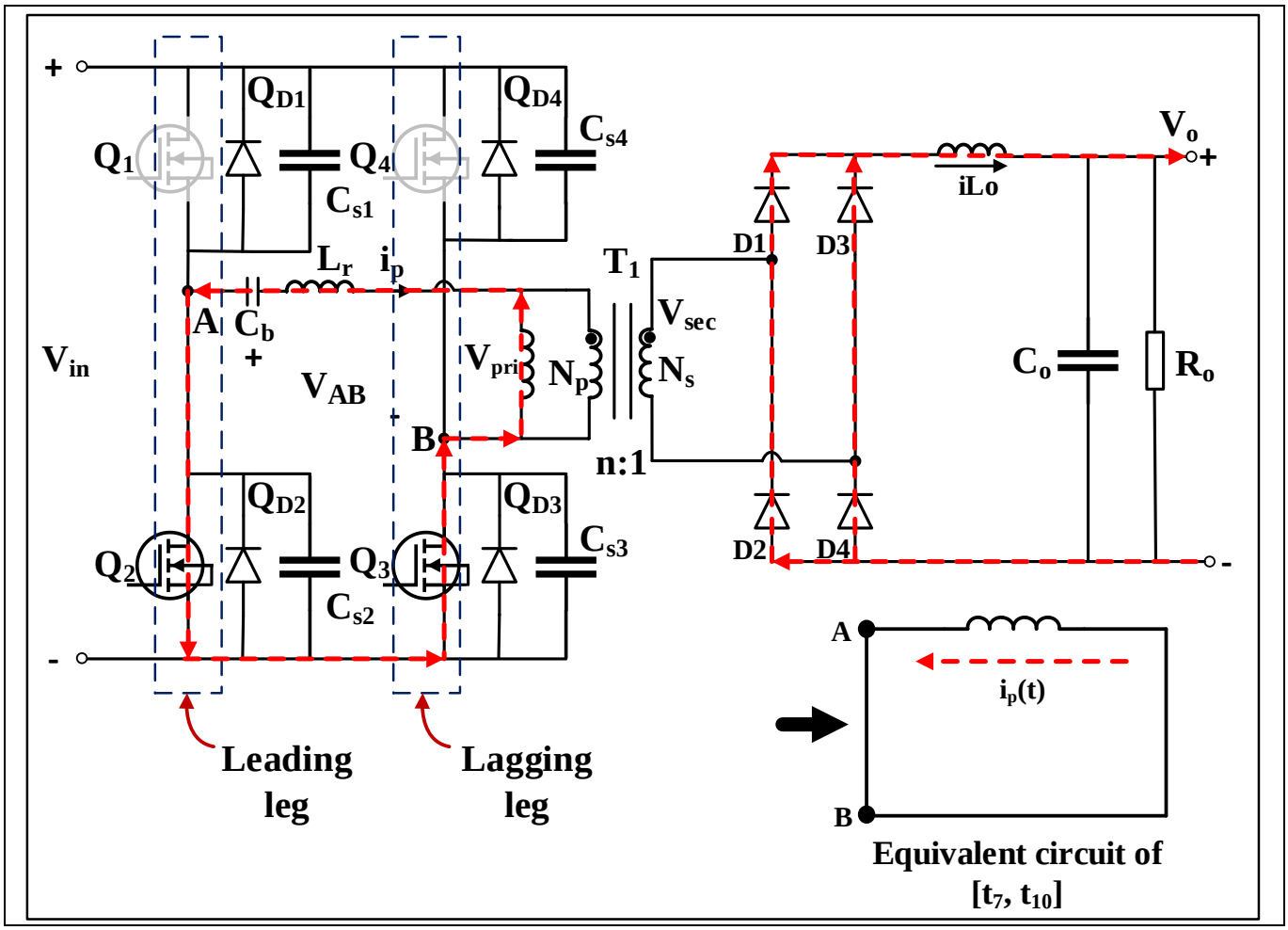

Figure 6 Current path and equivalent circuit diagram of circulating current interval [t7, t10]

As noted from the analyses above, if the DTs of the PSFB becomes higher, its circulating current interval becomes lower. It highly depends on the output load. Therefore, the circulating current losses become serious at light-load conditions as the circulating current interval increases. Apart from the difficulty to reach ZVS at light loads, the circulating current loss is another reason for PSFB's inefficiency at light loads.

According to the literature, the root mean square (RMS) of the circulating current can be calculated as follows:

For the RMS value of [t2, t5] circulating current interval:

$$I_{cir_cur_rms} = \sqrt{\frac{1-2D}{2}} \sqrt{(i_p_t_{2p})(i_p_t_{5p}) + \frac{1}{3}(i_p_t_{5p} - i_p_t_{2p})^2}$$

Equation 1

For the RMS of [t7, t10] circulating current interval:

$$I_{cir_cur_rms} = \sqrt{\frac{1-2D}{2}} \sqrt{(i_p_t_{7p})(i_p_t_{10p}) + \frac{1}{3}(i_p_t_{10p} - i_p_t_{7p})^2}$$

Equation 2

Therefore, based on Equation 1 and Equation 2, the power loss of the circulating current interval can be calculated as follows:

$$P_{cir_loss} = I^2_{cir_cur_rms} \cdot R_{DS_ON}$$

Equation 3

According to Equation 3, when D is lower, the circulating current loss increases and when D is higher, the circulating current loss decreases.

In Equation 1 to Equation 3, ip_t2p, ip_t5p, ip_t7p, and ip_t10p represent each corner point of the different time-interval current and D is the overlap interval where the positive and negative half-periods can transfer the energy. All these symbols above are marked in Figure 4. $R_{DS(ON)}$ is the conduction resistance of the power switch. Icir_cur_rms is the RMS value of the positive or negative half-period circulating current.

2.2 How to decrease circulating current losses in PSFB

This application note adopts the PWM and phase-shift hybrid method to control the full-bridge converter. During light load conditions, the digital controller uses conventional PWM control and aims to eliminate circulating current loss to improve light-load efficiency. When the load current is heavier than a certain level, phase-shift control is adopted to enhance the output load efficiency through its ZVS characteristic.

The conceptual diagram of the proposed hybrid control method is shown in Figure 7. When the output load is light, the duty cycle of the PWM is also small. As the output load becomes heavier, the duty cycle of the PWM increases from D to D' to maintain a stable output voltage.

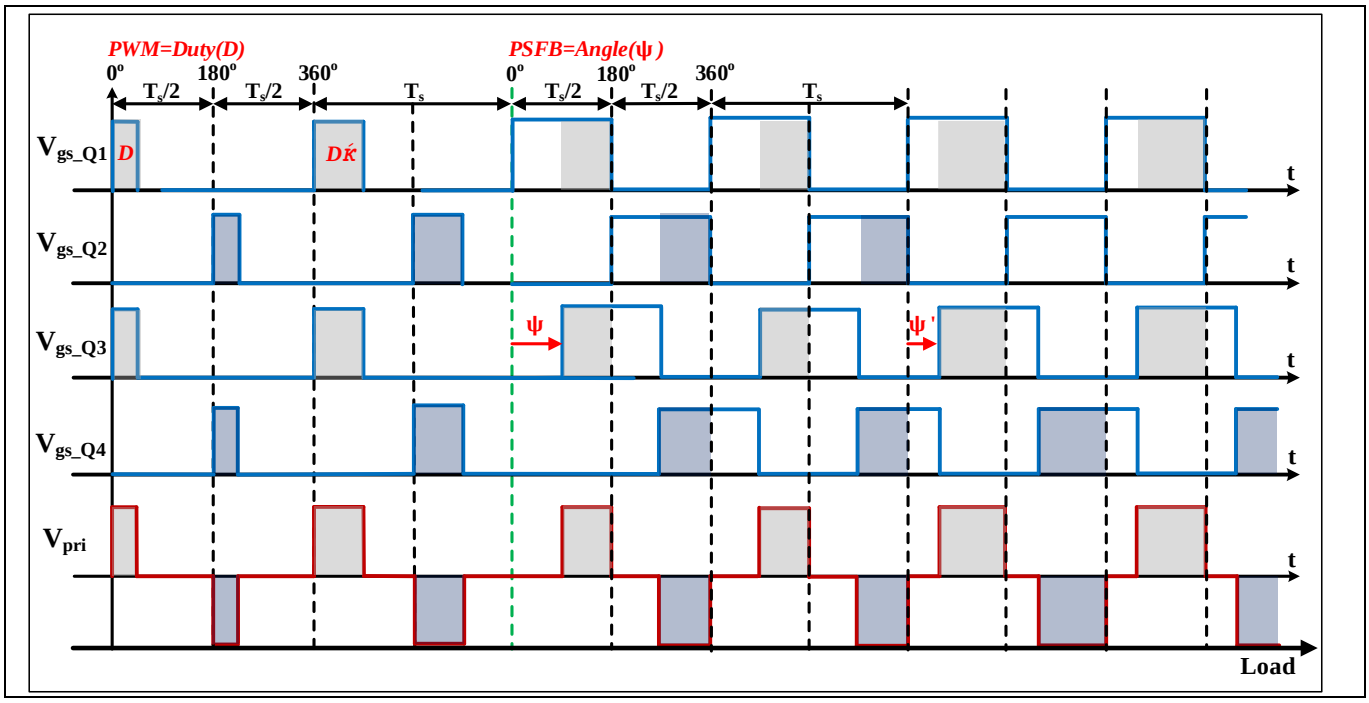

Figure 7 Switching between PWM control and phase-shift control modes

If the output load keeps getting heavier, the conventional PWM control method switches to the phase-shift control method and the control parameter switches from the duty cycle D to the phase-shift angle (ψ). If the output load becomes even heavier, the phase-shift angle changes from ψ to ψ' to keep a stable output voltage. Through this hybrid control method, you can eliminate the circulating current loss at light loads and easily achieve ZVS when the load current is higher than a certain level.

Smooth control is essential at the moment of switching between the two controlling modes mentioned. Due to different MCU designs, some MCUs need reinitialization of their peripherals to accomplish different control switching, but this can lead to output voltage instability. This instability can be avoided using Infineon's XMC4200 MCU ([1], [2]) to achieve hybrid mode control. XMC4200 can solely expand the PWM duty cycle D to nearly 50 percent in the switching moment and change it into phase-shifted control simultaneously – without the MCU reinitialization process. This smoothens the switching process between these two control modes and makes the output voltage stable.

3 How to achieve smooth hybrid mode control using XMC4200

3.1 XMC4200 features

XMC4200 combines Infineon's advanced peripheral modules with an industry-standard Arm® Cortex®-M4F core.

Controlling SMPS is a strong focus for XMC™ microcontrollers, with features such as smart analog comparators, high-resolution PWM timers, and the Arm® Cortex®-M4F DSP instruction set, including floating-point or high-precision analog-to-digital converters. It offers a high-resolution PWM unit with a resolution of 150 ps. This unique peripheral makes it especially suitable for digital power conversion in applications such as solar inverters, SMPS, and UPS.

XMC4200 is supported by Infineon's DAVE™ integrated development platform, which includes an IDE, debugger, and other tools to enable fast, free, and application-oriented software development.

Summary of key features

- Arm® Cortex®-M4F 80 MHz, including single-cycle DSP MAC and floating-point unit (FPU)
- CPU frequency: 80 MHz
- High ambient temperature range: –40°C to 125°C
- Wide memory size options: up to 512 KB of Flash and 80 KB of RAM
- High-resolution PWM (HRPWM) enabling PWM adjustment in steps of 150 ps
- 12-bit ADC, 2 Msps, flexible sequencing of conversions including synchronous conversion of different channels
- Fast, smart analog comparators offer protections such as overcurrent protection (OCP), including filtering, blanking, and clamping of the comparator output
- A 10-bit DAC with a conversion rate of 30 MHz provides an internal reference for the comparators that can be configured to be a negative ramp for slope compensation purposes
- A flexible timing scheme due to Capture and Compare Unit (CCU) timers and HRPWM (high resolution PWM). These timers allow creating any PWM pattern and accurately synchronize PWM signals with ADC measurements
- Interconnection matrix to route signals from one peripheral to another. For example, the comparator output can connect to the PWM timer to indicate an OCP event to immediately switch off the PWM output
- Supports communication protocols, including USB, UART, I^2C, and SPI

3.2 XMC4200 CCU4x and CCU8x timer modules

XMC4200 offers two types of timer modules: CCU4x and CCU8x. Each timer module has its own sub-timer slice called CCU4x.CC4y or CCU8x.CC8y [xx]. The main difference between these two timers is shown in Figure 8 and Figure 9.

Figure 8 takes the edge-aligned timing pattern of CCU4x as an example. In this mode, the timer is incremented until it matches the value programmed in the period register CC4yPR. When the period match is detected, the timer is cleared to 0000h and continues to be incremented. Besides, the CCU4x timer only has one compare register (CC4yCR), and the status bit CC4yST is set one clock cycle after the timer hits the value that has been programmed into the compare register. The status bit CC4yST is cleared one clock cycle after the timer reaches 0000h.

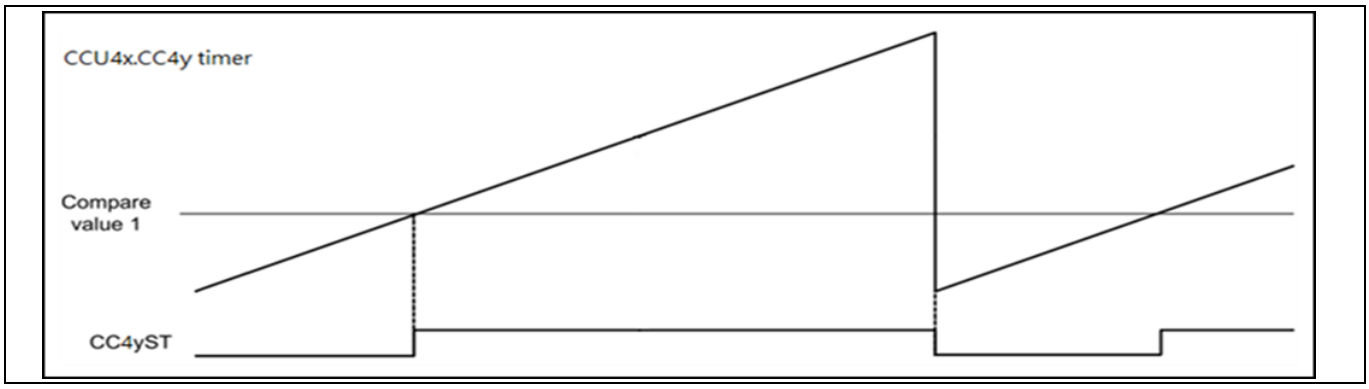

Figure 8 CCU4x timer count and comparison pattern (edge-alignment mode)

For CCU8x, it still takes edge-aligned mode as an example. In this mode, the CCU8x timer's behavior is exactly the same as the CCU4x timer. On the other hand, CCU8x has two compare registers, and each compare register decides two complementary status bit pairs (see Figure 9). The status bit CCU8yST1 is set one clock cycle after the timer hits the value programmed into the first compare register (CC8yCR1) and its complementary status bit activates simultaneously. Similar to CCU8yST1, the status bit CCU8yST2 is set one clock cycle after the timer hits the value programmed into the second compare register (CC8yCR2). Its complementary status bit activates at the same time as well. In fact, there are various kinds of timer operating modes in XMC4200, but this application note only discusses the edge-aligned operating mode.

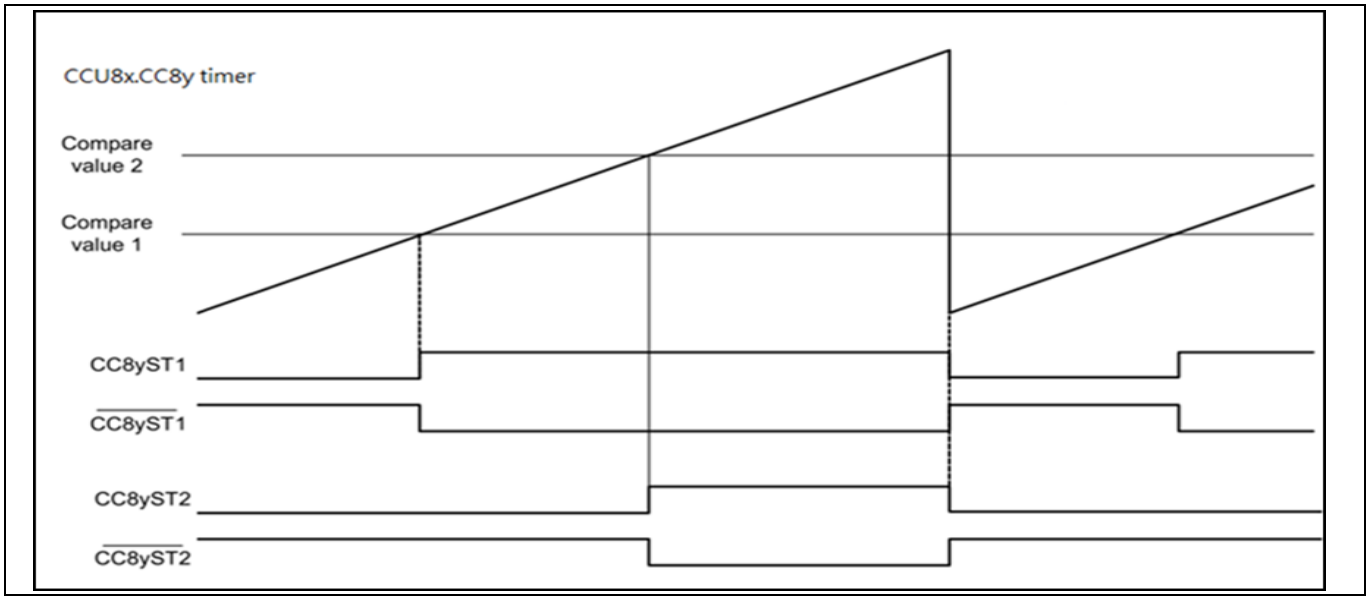

Figure 9 CCU8x timing and comparison pattern (edge-alignment mode)

3.3 CCU4x and CCU8x PWM output generation

The following subsections discuss some important concepts – CCU4x and CCU8x timer settings for the PWM output.

3.3.1 CCU4x PWM output generation

Each CCU4x timer has its corresponding PWM output pin, which is called CCU4x.OUTy, as shown in Figure 10. In XMC™ series MCUs, the PWM output pin CCU4x.OUTy can connect to its status bit CC4yST or the inverse of its

status bit directly. Besides, CCU4x.OUTy can also be configured to its output level by writing the passive level (PSL) register as passive level LOW (PSL LOW) or passive level HIGH (PSL HIGH) status. **Table 1** is the truth table of the relation between status bit and the PSL status.

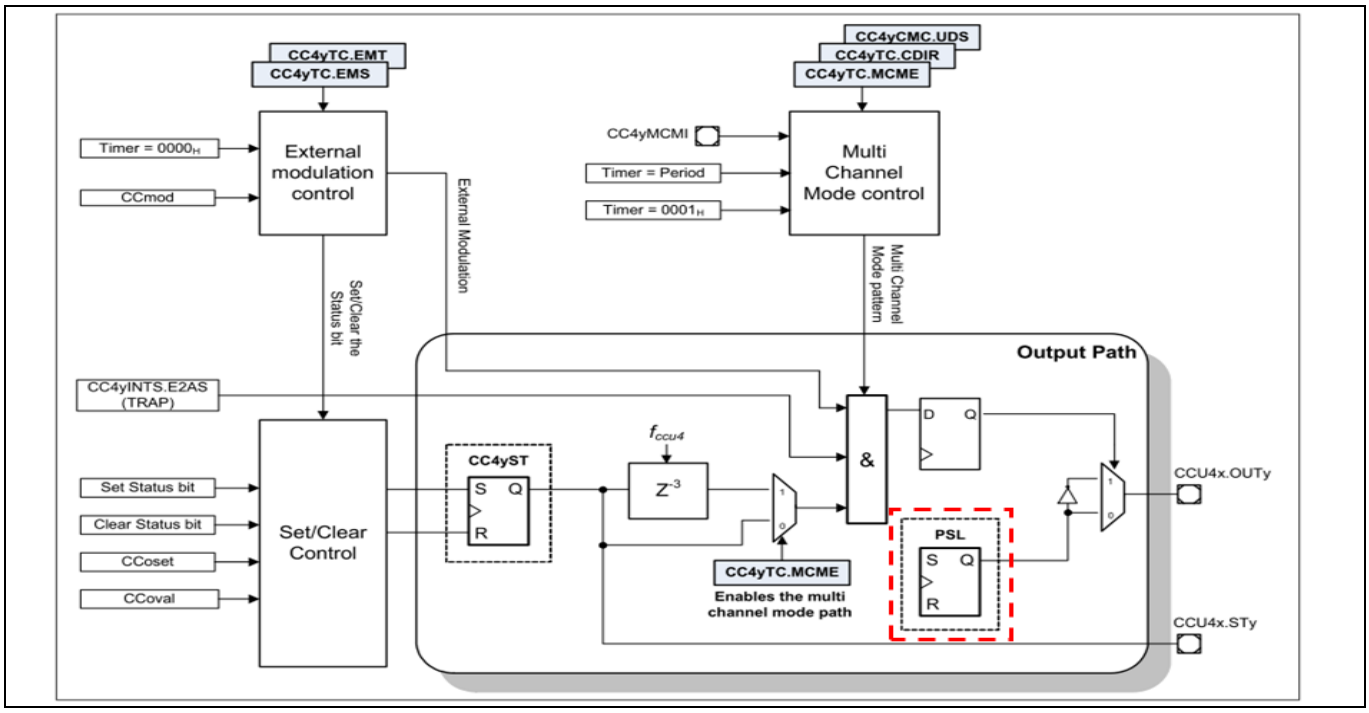

Figure 10 Relationship between CCU4x and its corresponding PWM output

Table 1 Truth table of CCU4x status bit and PSL register settings

CC4yST/ $\overline{\text{CC4yST}}$	PSL	CCU4x.OUTy
HIGH	LOW	HIGH
LOW	LOW	LOW
HIGH	HIGH	LOW
LOW	HIGH	HIGH

3.3.2 CCU8x PWM output generation

Each CCU8x timer has its corresponding PWM output pin called CCU8x.OUTy0~CCU8x.OUTy3, as shown in Figure 11. As mentioned in the previous section, a pair of the complementary status bit CCU8yST1 and $\overline{\text{CCU8yST1}}$ can be determined by CCU8x's comparison register 1 (CC8yCR1). Similarly, CCU8x's comparison register 2 (CC8yCR2) determines the complementary status bit CCU8yST2 and $\overline{\text{CCU8yST2}}$.

Alternatively, CCU8yST1 and $\overline{\text{CCU8yST1}}$ can be connected to CCU8x.OUTy0 or CCU8x.OUTy1, while CCU8yST2 and $\overline{\text{CCU8yST2}}$ can be connected to CCU8x.OUTy2 or CCU8x.OUTy3. It depends on their register setting. Besides, CCU8x.OUTy can also be determined its output level by writing the PSL register as PSL LOW or PSL HIGH status.

The CCU8x timer has two passive level registers, one for the CCU8yST1 setting and the other for the CCU8yST2 setting. **Table 2** shows the truth table of the relation between the status bit and the PSL status .

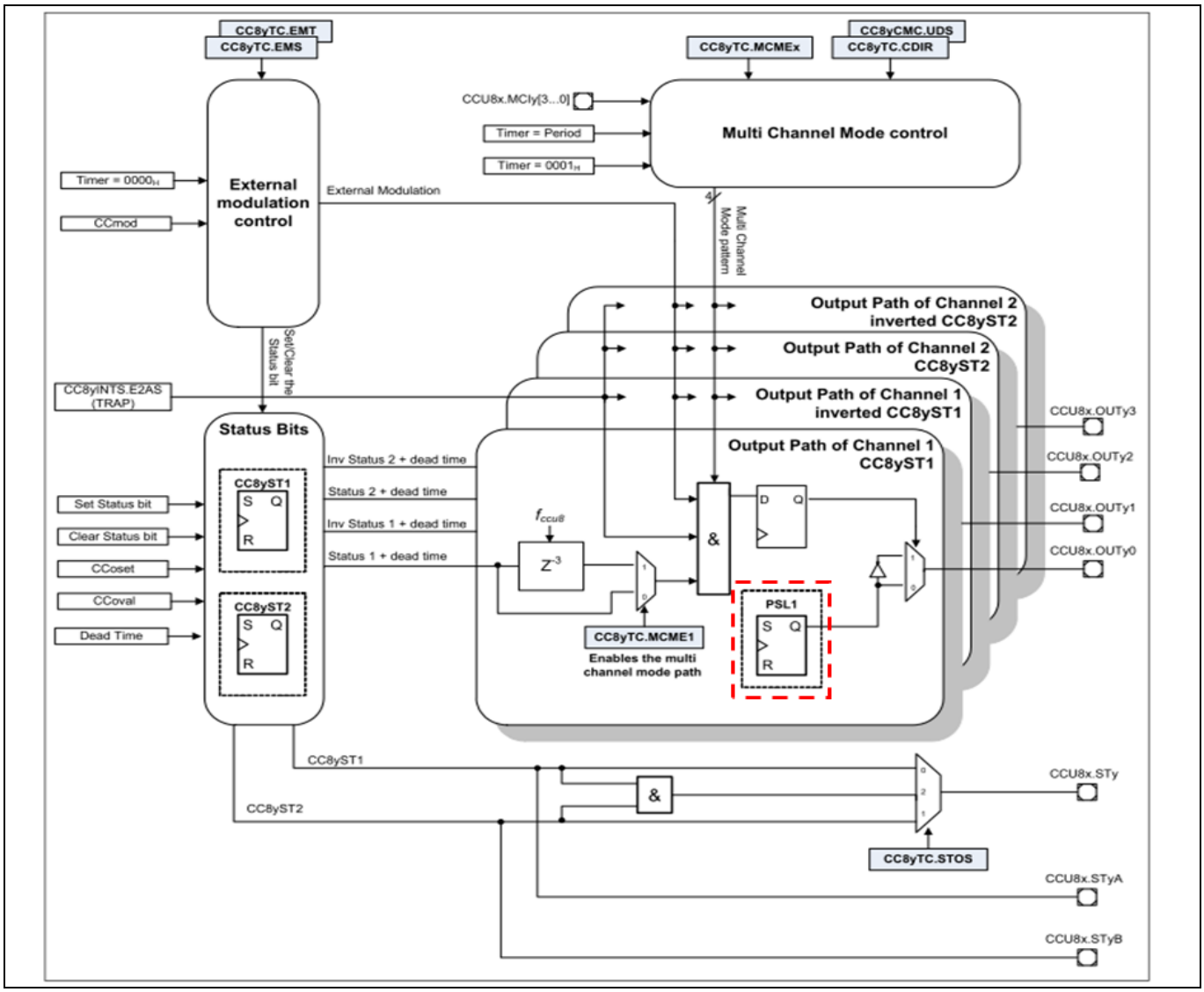

Figure 11 Relationship between CCU8x and its corresponding PWM output

Table 2 Truth table of CCU8x status bit and PSL register settings

CC8yST1/ $\overline{\text{CCU8yST1}}$ **CC8yST2/** $\overline{\text{CCU8yST2}}$	**PSL**	**CCU8x.OUTy**
HIGH	LOW	HIGH
LOW	LOW	LOW
HIGH	HIGH	LOW
LOW	HIGH	HIGH

3.4 Complementary PWM and interleaved PWM setting

In the conventional PWM mode full-bridge converter, although the high- and low-side MOSFET of each leg cannot conduct simultaneously, they should not be in a complementary switching pattern. In some control sequences of the conventional PWM mode full-bridge converter, the high- and low-side MOSFET of each leg is

turned off synchronously. This is a kind of an interleaved switching pattern instead of a complementary switching pattern.

Based on the discussion above, if the CCU8x.OUTy0 and CCU8x.OUTy1 are adopted intuitively to control the conventional PWM mode full-bridge converter without extra timer setting skills, it is not a suitable solution as CCU8x.OUTy0 and CCU8x.OUTy1 have totally complementary outputs.

On the other hand, in a PSFB switching mode full-bridge converter, the high- and low-side MOSFET of each leg cannot conduct simultaneously, but they are completely in complementary operation modes. Therefore, due to PSFB's complementary characteristics, each complementary control output pair such as CCU8x.OUTy0/CCU8x.OUTy1 or CCU8x.OUTy2/CCU8x.OUTy3 is suitable for controlling one of the PSFB's legs intuitively. Figure 12 shows the interleaved and complementary switching patterns discussed above.

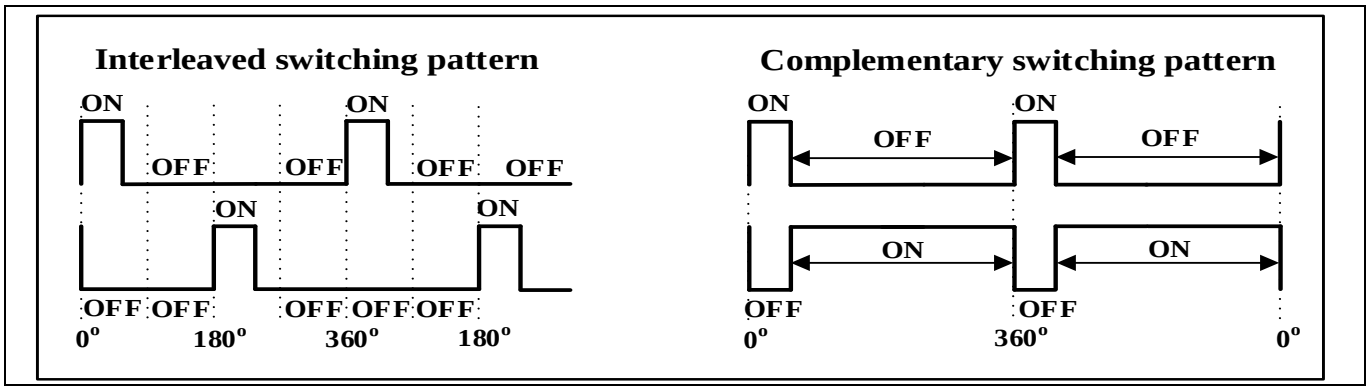

Figure 12 Interleaved and complementary switching patterns

As Figure 12 and discussions above indicate, an intuitive and easy-to-use complementary output pair (CCU8x.OUTy0/CCU8x.OUTy1 and CCU8x.OUTy2/CCU8x.OUTy3) cannot meet the switching patterns of both conventional PWM and PSFB simultaneously. Therefore, this application note proposes a practical switching pattern that can simultaneously satisfy both conventional PWM and PSFB switching patterns.

3.5 Design to generate PWM and phase-shift drive signals

The following is a step-by-step example of how to design PWM and phase-shift drive signals in the same timer slice. You can design your own timer once you understand the design concept, as shown in Figure 13.

1. Take CC80~CC83 sub-slices of CCU80, which includes four timer sub-slices (CC80~CC83), as timers of each driver signal to the four power switches of the full-bridge converter.
2. Set CC80 and CC82 timers as the control driver signals to the power switches Q_1 and Q_2.

   CC82 starts counting when the CC80 counter reaches its half-period. Therefore, CC82 has a 180° phase shift with respect to CC80; this mechanism does not let CC80 and CC82 conduct at the same time. If the duty cycle D of CC80 and CC82 are less than 50 percent, CC80 and CC82 remain in an interleaved switching pattern, turning on and off consecutively. Once the duty cycle of CC80 and CC82 are equal to 50 percent, CC80 and CC82 turn entirely into a complementary switching pattern. For both these switching patterns, the duty cycles of CC80 and CC82 are limited to 50 percent.

   CC81 and CC83 timers are the control driver signals to the power switches Q_3 and Q_4. CC83 starts counting when the CC81 counter reaches its half-period. Therefore, CC83 has a 180 degree phase shift relative to CC81. Similar to CC80 and CC82, CC81 and CC83 do not turn on at the same time. For the rest of the functions

and operating principles, CC81 and CC83 are the same as those of CC80 and CC82.

On the other hand, CCU40.CCU40 and CCU41.CCU40 are designed as phase-shift control timer modules.

3. Set CCU40.CC40 and CCU41.CC40 in a synchronous startup pattern, with the same frequency but with an adjustable compare value.

   CCU80.CC80 starts counting according to the rising edge of the comparison status bit (CCU40.ST0) of CCU40.CC40; CCU80.CC81 starts to count based on the rising edge of the comparison status bit (CCU41.ST0) of CCU41.CC40.

4. If CCU40.CC40 and CCU41.CC40 have the same value in their compare match registers, there will be no phase shift between CC80 and CC81. If CCU40.CC40 and CCU41.CC40 have different values in their compare match registers, there will be a phase shift between CC80 and CC81.

Note: *In this design, a fixed value is written in CCU40.CC40 compare match registers; their value can be adjusted to generate a phase shift relative to CCU40.CC40.*

For example, assume all timers have the same period setting. The comparison match point of CCU40.CCU40 is written at the 20 percent period; therefore, the starting point of CCU80.CC80 starts at the 20 percent period of CCU40.CC40. On the other hand, the comparison match point of CCU40.CCU41 is written at the 40 percent period; therefore, the starting point of CCU80.CC81 starts at the 40 percent period of CCU40.CC41. Because CCU40.CC40 and CCU40.CC41 start synchronously, CCU80.CC81 starts counting after the 20 percent period of CCU80.CC80. In other words, CCU80.CC81 has a 20 percent period phase shift compared to CCU80.CC80.

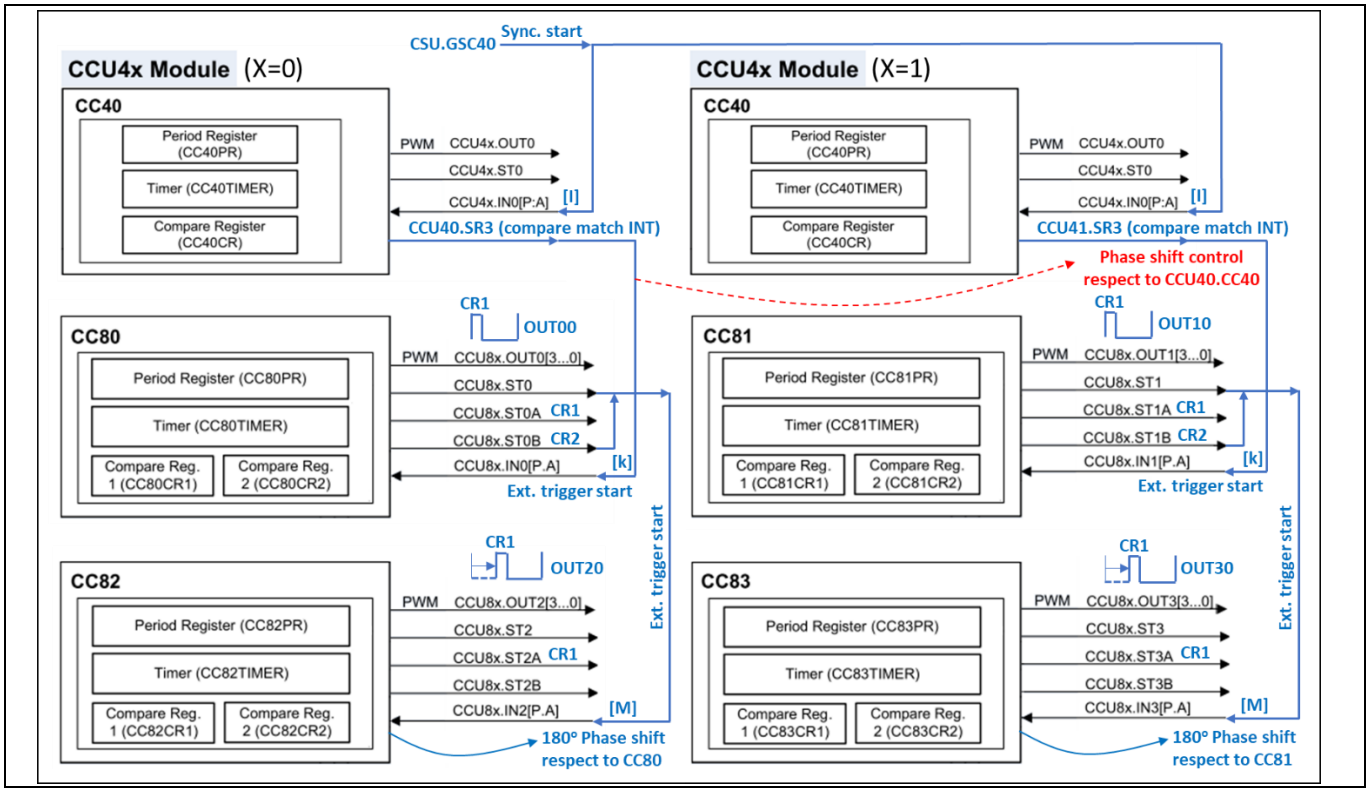

Figure 13 PWM and phase-shift driver signals for a full bridge converter design concept

Based on the design above, CCU40.CC40 and CCU41.CC40 settings have a zero phase difference at light loads. Therefore, (CC80, CC82) and (CC81, CC83) are in phase while (CC80, CC82) and (CC81, CC83) possess a duty cycle D less than 50 percent in this mode. Moreover, as the load becomes heavier, the duty cycle D becomes larger (D') to meet larger load requirements. The whole switching pattern of the light load is shown in Figure 14.

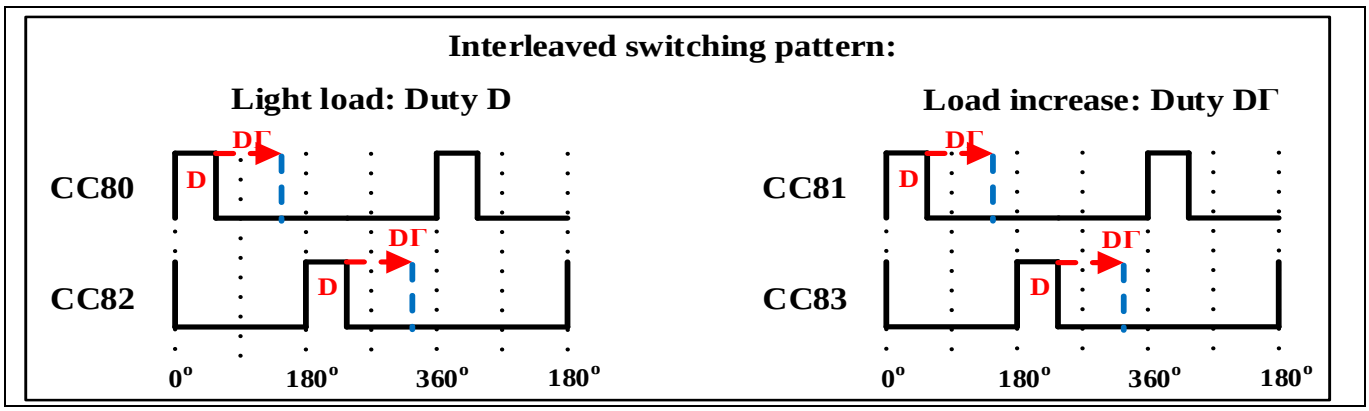

Figure 14 Interleaved pattern at light-load condition

When the load becomes heavier, using a conventional PWM full-bridge converter ends up reducing the efficiency. Therefore, PWM control should be changed into the phase-shift control to improve efficiency. The adopted method is to expand the duty cycle of (CC80, CC82) close to the 50 percent period initially and then adjusting the phase-shift angle of CCU41.CC40 to ψ, allowing the same phase-shift angle ψ to be generated between (CC81, CC83) and (CC80, CC82). Lastly, the duty cycle of (CC81, CC83) should be near the 50 percent period. Through these steps, the phase-shift angle ψ can be adjusted to adapt different load conditions and the process of switching from the PWM mode to the phase-shift mode is accomplished, as shown in Figure 15.

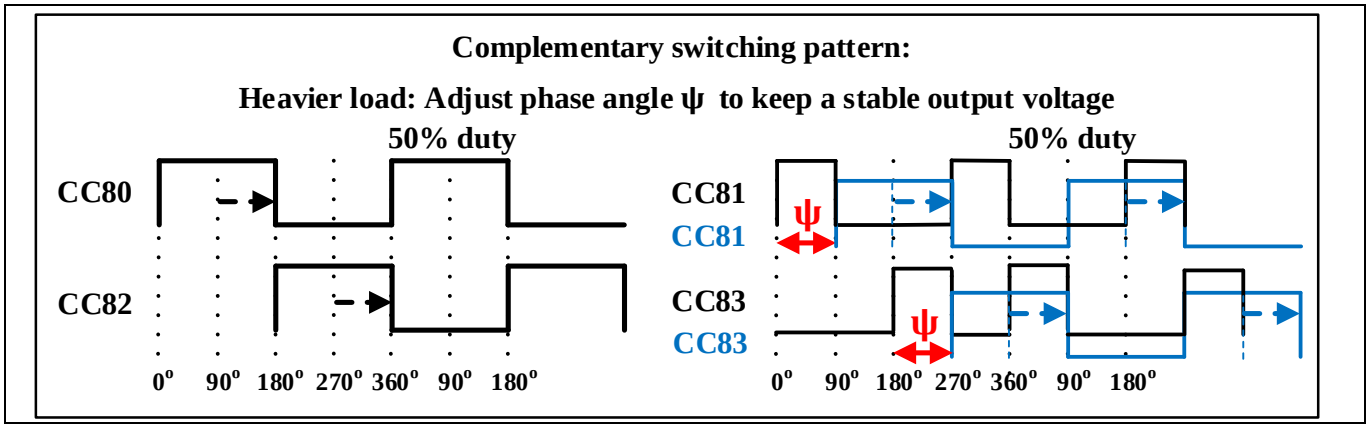

Figure 15 Complementary switching pattern at heavier load condition

When the output load is back to the light load condition, the duty cycle of (CC80, CC82) is first reduced to an appropriate duty cycle D . Then, the phase-shift angle between CCU41.CC40 and CCU40.CC40 is adjusted to zero. Meanwhile, there is no phase shift between (CC81, CC83) and (CC80, CC82). Lastly, the duty cycle of (CC81, CC83) is reduced to an appropriate duty cycle D. Through these steps, the transient process of switching the phase-shift pattern to a conventional PWM pattern is accomplished.

As the switching pattern above shows, neither expanding (CC81, CC83) to the 50 percent period nor reducing them to an appropriate duty cycle D influences the output voltage excessively because the drive signals of (CC81, CC83) do not have a significant change. Similarly, changes in the phase shift angle, from zero to an

appropriate angle ψ or from ψ to zero, have insignificant influence on the output voltage. As a result, the transient switching process of these two controller modes are smoother.

4 Experimental verification

The following experimental waveforms are divided into four test conditions to be discussed, including:

1. PWM mode
2. PSFB mode
3. Switching from PWM to PSFB
4. Switching from PSFB to PWM

In the following figures (Figure 16 to Figure 19), the CH1 waveform is for the CC80 PWM output, the CH2 waveform is for the CC82 PWM output, the CH3 waveform is for the CC81 PWM output, and the CH4 waveform is for the CC83 PWM output.

4.1 PWM control mode

Figure 16 is the PWM controlling strategy proposed in this document. In this mode, CCU40.CC40 and CCU41.CC40 timers are controlled with a zero phase shift. Therefore, timers (CC80, CC82) and (CC81, CC83) have the same duty cycle without a phase difference. However, there is a 180 degree phase difference between (CC80, CC82) and (CC81, CC83).

When CC80 and CC81 are simultaneously conducted, they transfer energy during the positive half-period and when CC82 and CC83 are simultaneously conducted, they transfer energy during the negative half-period. The duty cycle of the positive and negative half-periods increase linearly as the loads become heavier. Figure 16 (a) shows the switch conduction duty cycle at light loads and Figure 16 (b) shows the duty cycle when the load becomes heavier but the control method is still PWM mode. This is because PWM mode is used in light loads as it provides better efficiency than PSFB mode.

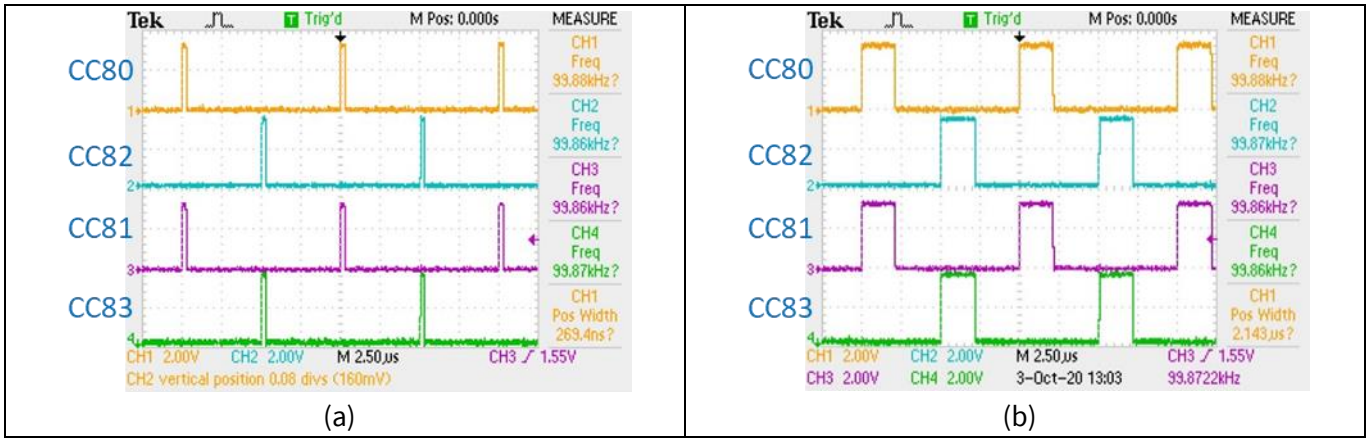

Figure 16 Control waveform of PWM mode control at light loads

4.2 Phase-shift control mode

Figure 17 shows the PSFB controlling strategy proposed by this application note. In this mode, CC80 and CC82 become a complementary pair. It means that CC80 and CC82 extends their duty to 50 percent, and a 180° phase difference remains between CC80 and CC82. Similarly, CC81 and CC83 also become a complementary pair. Meanwhile, CCU41.CC40 and CCU41.CC40 are controlled with a 0 to 180 degree phase shift. Thus, an adjustable phase difference lies between the two control pairs (CC80, CC82) and (CC81, CC83).

The overlapping degree of CC80 and CC81 or CC82 and CC83, which is the degree of phase shift, varies with the changing output load. Figure 17 (a) is the initial operation for the mode switching from PWM to PSFB and the overlapping part is the maximum duty cycle that connects the PWM operating range. Figure 17 (b) is an example of how the phase-shifted angle is kept adjusted until the operation is completely overlapped, responding to the output load variation.

However, in the actual case, the overlapping angle varies linearly based on load current changes until the output voltage becomes stable.

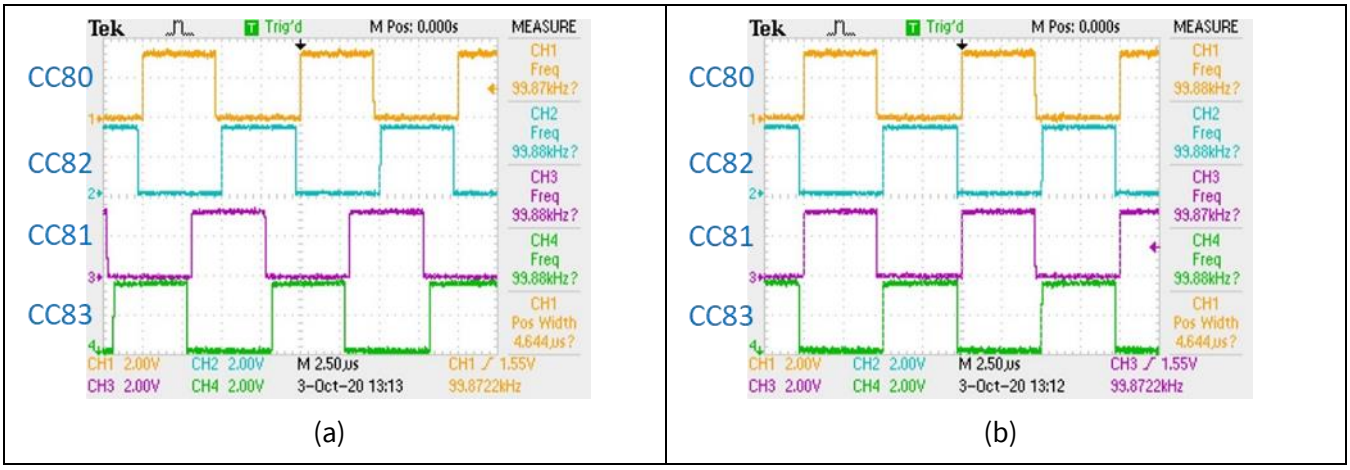

Figure 17 Phase-shift control mode at heavier load

4.3 Transient processes of switching from PWM to PSFB

Figure 18 shows the transient processes of switching from PWM to PSFB mode. Figure 18 (a) shows the status before switching from PWM mode, where the power switch drive signal is still in two diagonal pairs (CC80, CC81) and (CC82, CC83), synchronal conduction, and cut-off.

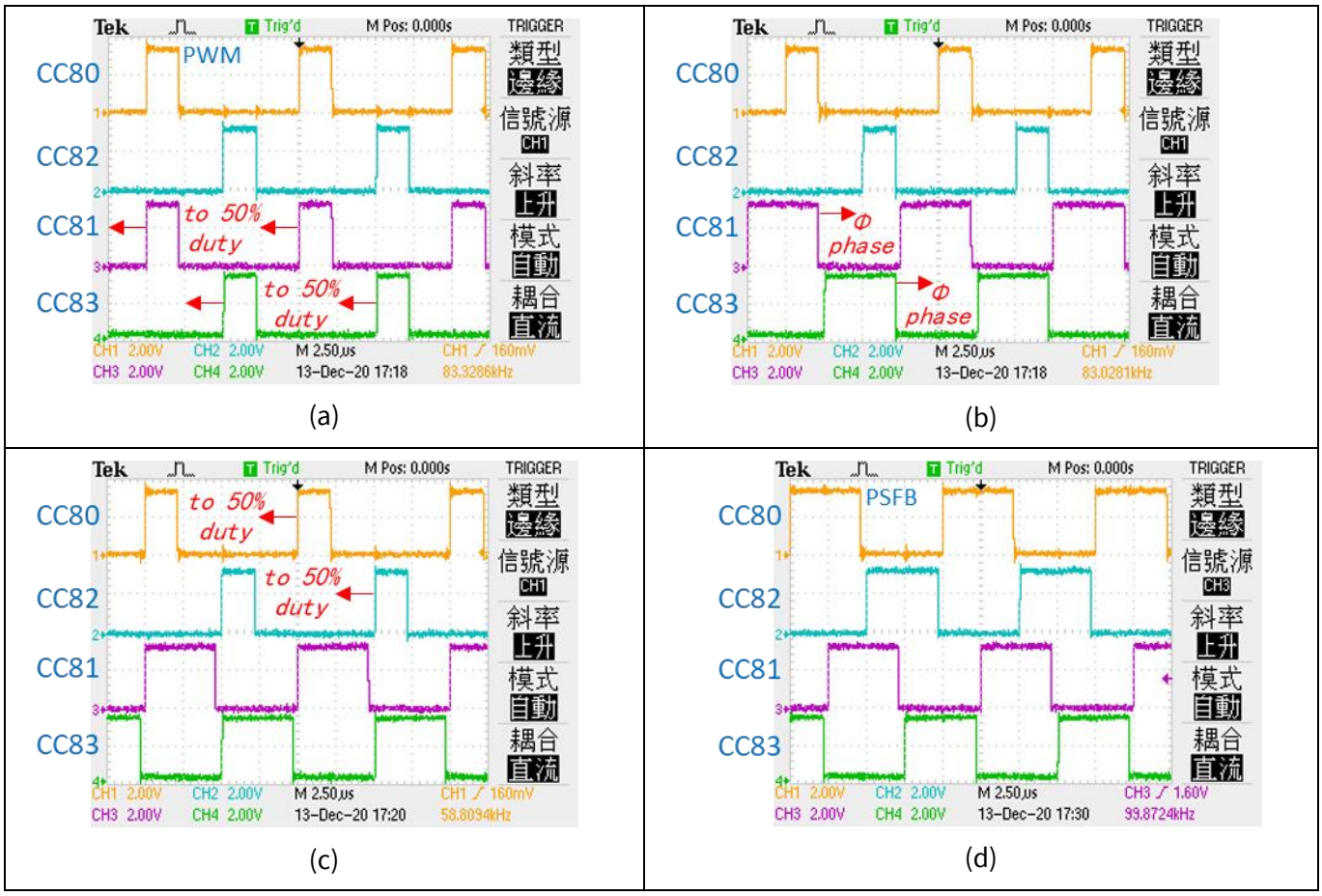

Figure 18 Software design process of switching from PWM to PSFB mode

The following is the software design process to switch from PWM mode to PSFB mode:

1. Expand the duty cycle of CC81 and CC83 to nearly 50 percent, as shown in Figure 18 (a) and (b).
2. Adjust the phase shift of CC81 and CC83 to the appropriate phase degree. The phase adjustments do not affect the output voltage because the overlapping region of CC80 and CC81, and CC82 and CC83 remain fixed, as Figure 18 (b) and (c) show.
3. Expand the duty of CC80 and CC82 to nearly 50 percent, as Figure 18 (c) and (d) show.

The above processes convert the PWM mode into PSFB mode smoothly. After the conversion, output voltage stabilization can be maintained by adjusting the phase difference between CCU40.CC40 and CCU41.CC40, which is the compensating action of a typical PSFB mode.

4.4 Transient processes of switching from PSFB to PWM

Figure 19 shows the transient processes of switching from PSFB to PWM. Figure 19 (a) shows the status before switching from PSFB mode, where the power switch drive signal is still PSFB.

Use the following software design process to switch from PSFB mode to PWM mode:

1. Shorten the duty cycle of CC80 and CC82 from near the 50 percent period to their designed maximum duty cycle in the PWM mode, as shown in Figure 19 (a) and (b).

2. Phase-shift CC81 and CC83 to the appropriate phases. The phase adjustments do not affect the output voltage because the overlapping region of CC80 and CC81, and CC82 and CC83 remain fixed, as Figure 19 (b) and (c) show.
3. Shorten the duty cycle of CC81 and CC83 from the 50 percent period to their maximum duty cycle designed in the PWM mode, as Figure 19 (c) and (d) show.

These processes convert PSFB mode into PWM mode. After the conversion, output voltage stabilization can be maintained by adjusting the duty cycle of the two diagonal pairs (CC80, CC81) and (CC82, CC83), which is the compensating action of a typical PWM mode.

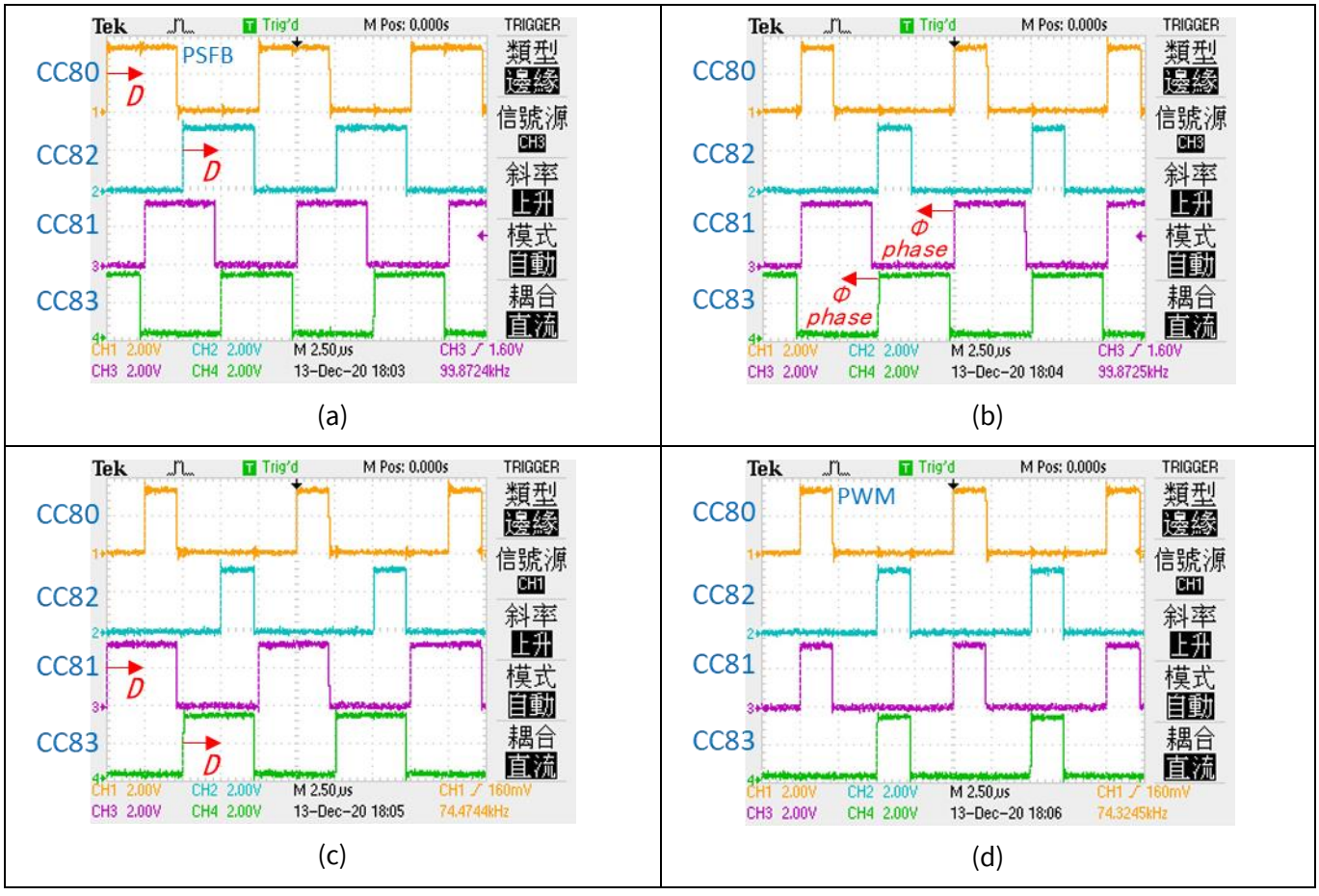

Figure 19 Software design process of switching from PSFB to PWM mode

5 Conclusion

This application note proposes a digital hybrid mode control method for a full-bridge converter using Infineon's XMC4200-Q48x256 microcontroller, which switches different control modes according to the load condition.

This application note emphasizes the smooth switching of the two control methods, made possible through the peripheral functions of the XMC4200-Q48x256 MCU, leading to enhanced efficiency of conventional full-bridge converters.

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Revision history

Document revision	Date	Description of changes
**	2024-08-20	Initial release

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