EZ-PD™ PAG2x: Designing power adapters using CYPAx2xx

About this document

Scope and purpose

This application note provides guidelines for designing a flyback controller using Infineon EZ-PD™ PAG2x second-generation integrated flyback and USB Power Delivery (PD) controllers, and focuses on design elements surrounding EZ-PD™ PAG2P and EZ-PD™ PAG2S. The required firmware development tools and hardware design calculator are also covered in this document. This application note, along with the system design guidelines [1] is intended to cover all the key elements of designing a flyback system using EZ-PD™ PAG2x.

Intended audience

This document is intended for anyone who uses the EZ-PD™ PAG2x for designing power adapters.

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1 Introduction

EZ-PD™ PAG2x is Infineon's second-generation integrated flyback and USB PD controllers. PAG2P is the primary startup controller, and PAG2S is the secondary side flyback and USB PD controller. PAG2S is available in three variants – secondary-side synchronous rectifier (SR) controller (CYPAS213), secondary-side QR-ZVS controller (CYPAS211), and secondary-side active clamp flyback (ACF) controller (CYPAS212). See References section for PAG2P and PAG2S datasheets.

PAG2x is targeted towards USB-C power adapters; it fits well into high-efficiency AC-DC flyback designs with USB PD, Qualcomm Quick Charge, and other standard charging protocols.

Figure 1 shows a power adapter application diagram implementing a secondary-side controlled synchronous flyback system. This application note uses an ACF system with PAG2S (CYPAS212) and PAG2P (CYPAP212) for illustration, but the design guidelines are equally applicable for a QR-ZVS system with PAG2S (CYPAS211).

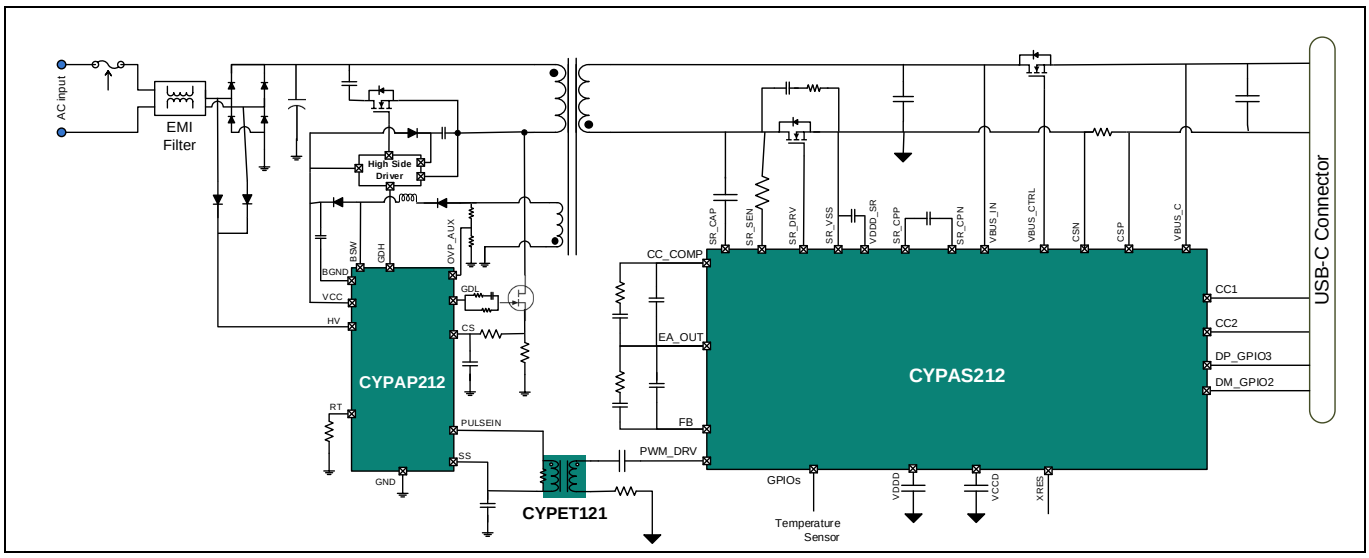


Figure 1 PAG2P-PAG2S USB PD adapter with secondary-side flyback control

2 Key design elements

This section provides design guidelines for circuits specific to PAG2x. Generic power adapter design guidelines are covered in the system design guidelines [1].

2.1 PAG2P power-up

PAG2P can operate in two different modes: x-cap and non-x-cap. In x-cap mode, the AC input is directly fed into the HV pin. In non-x-cap mode, the rectified DC output is fed into the HV pin.

2.2 PAG2P soft start

PAG2P does soft-start at power-up. The soft-start frequency is determined by the external timing resistor connected to the RT pin and the soft-start ramp rate is determined by the external capacitor connected to the SS pin. The recommended value of the RT resistor is 50 kΩ and the recommended value of SS capacitor is 1 µF in parallel with 0.1 µF. The soft-start ramp rate can be controlled by varying the SS capacitor; the higher the capacitor, the slower the ramp rate, and vice versa. PAG2P implements periodic retries for soft-start; see the PAG2P datasheet for more details.

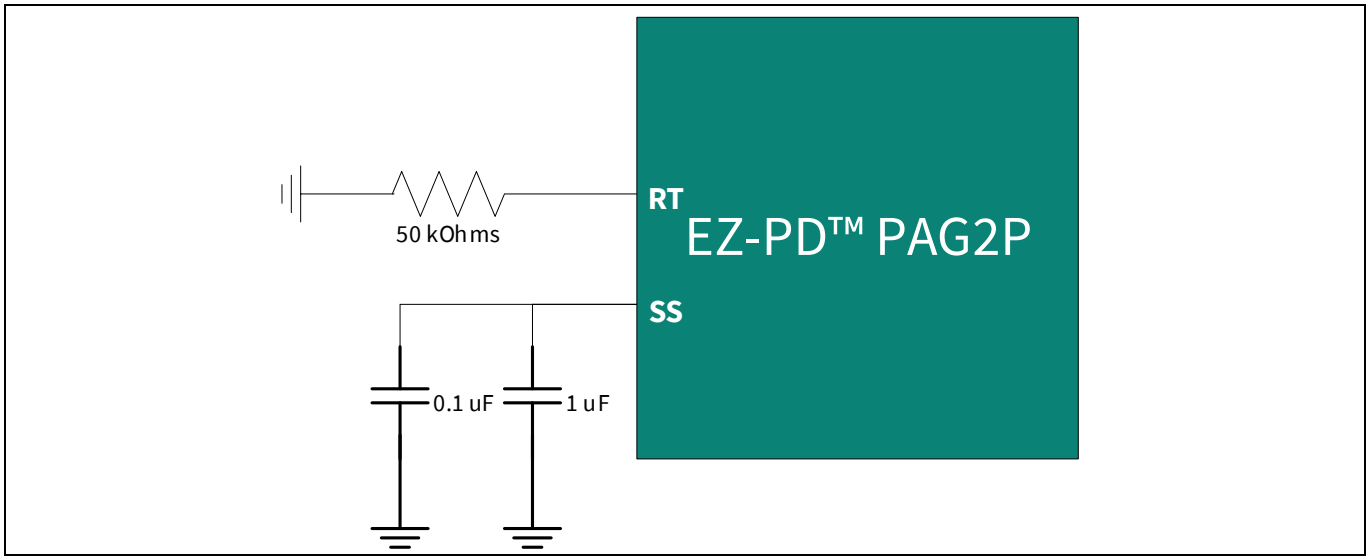


Figure 2 PAG2P soft start

2.3 PAG2P VCC boost circuit

PAG2P uses the auxiliary winding voltage to boost it to VCC; the boost switch is integrated into PAG2P, as shown in Figure 3. It is recommended to use a fast switching diode like SS110LW for D1 to ensure immediate energy transfer from the auxiliary winding to the capacitor C1. The recommended values for C1, C2, C3, and L are 10 µF, 44 µF, 22 µF, and 10 µH respectively.

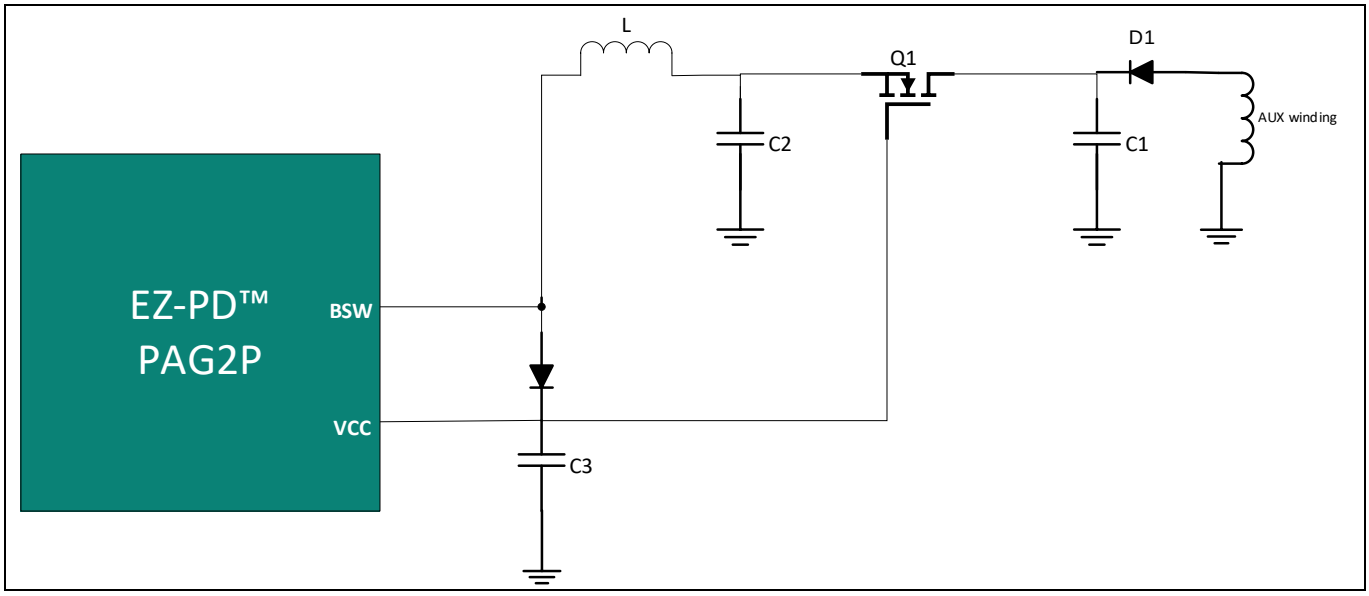


Figure 3 PAG2P VCC boost circuit

The NFET clipper Q1 ensures that the voltage at VCC is within the safe operating range, irrespective of the voltage variations at C1. The gate of Q1 is tied to VCC, and the source is connected to capacitor C2. As the voltage at C2 increases and gets close to VCC, switch Q1 will be turned off, ensuring the voltage at C2 is limited to below VCC. The voltage at C2 will start to deplete because of boost switching. After the delta between C2 voltage and VCC becomes greater than the V_{GS} of Q1, FET Q1 will be turned back on. This cycle continues, thus ensuring the voltage at VCC is within the safe operating range.

2.4 PAG2P overvoltage protection (OVP)

PAG2P OVP limits the secondary voltage by monitoring the voltage on the auxiliary winding. In open-loop mode, PAG2P monitors the voltage at the OVP_AUX pin and goes into OVP when the voltage at this pin exceeds 1.2 V.

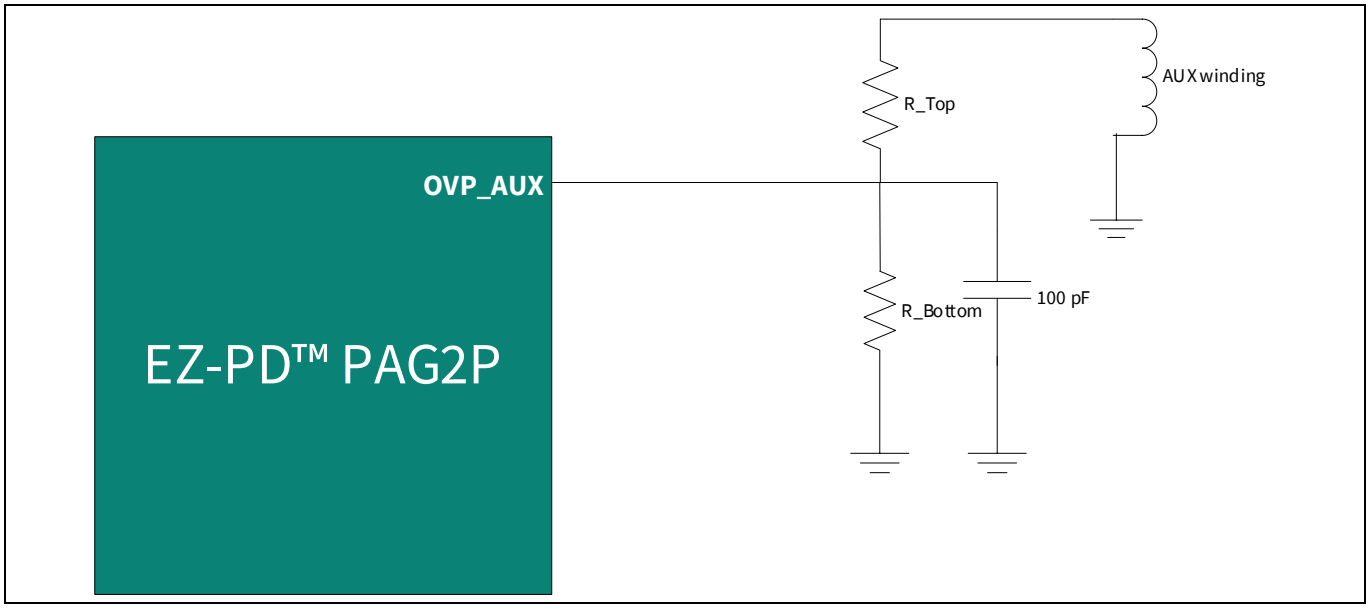


Figure 4 PAG2P OVP

The OVP_AUX resistor divider values must be calculated depending on the auxiliary to secondary winding turns ratio.

$V_{AUX} = (N_{AUX}/N_{SEC)} * V_{SEC}$

$1.2\ V = \{V_{AUX}/(R_{TOP} + R_{BOTTOM})\} * R_{BOTTOM}$

Limiting the secondary voltage to ~7 V in open-loop mode is recommended. For example, consider an auxiliary: secondary winding ratio of 4:5. When the secondary voltage is ~7 V, the auxiliary winding voltage is ~5.6 V. The recommended value for R_{BOTTOM} is 3 kΩ; from the above-mentioned equations, the calculated value for R_{TOP} is 12 kΩ.

2.5 PAG2P overcurrent protection (OCP)

PAG2P supports OCP by monitoring the voltage on the CS pin. There are two overcurrent limit thresholds: V_CSTH1 and V_CSTH2. V_CSTH1 is pulse-by-pulse protection set at typical 300 mV while V_CSTH2 is shutdown protection set at 600 mV (typical).

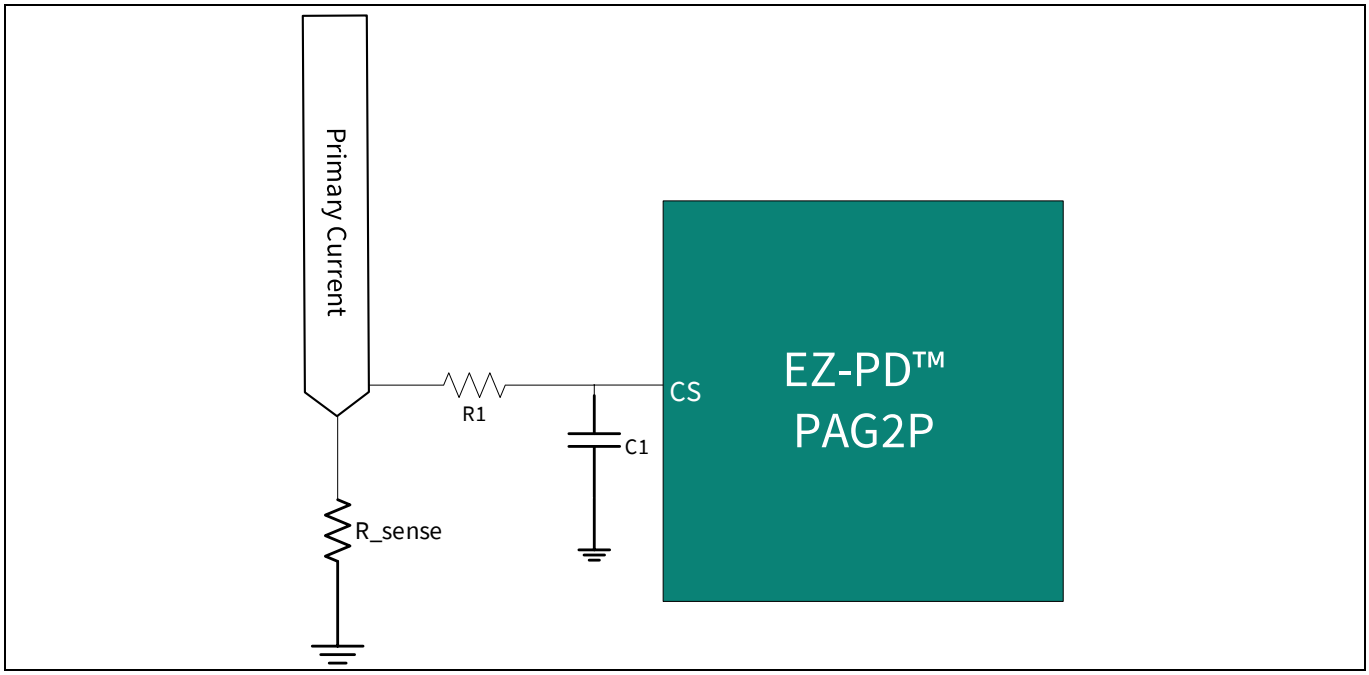


Figure 5 PAG2P OCP

The current sense resistor values should be chosen such that the voltage at the CS pin is well within 70% of V_CSTH1 during normal operation.

70% of V_CSTH1 ≥ Ipri_peak * Rsense

For example, consider a system with a peak primary current of 3 A during normal operation. This system's current sense resistor of approximately 85 mΩ would be optimal. It is also recommended to have an RC filter, as shown in Figure 5; the recommended values for R1 and C1 are 3.3 kΩ and 68 pF, respectively.

2.6 PAG2P high-side and low-side gate drivers

PAG2P drives the low-side MOSFET via the GDL pin and the external high-side gate driver via the GDH pin. The high-side gate driver is required only in applications supporting active clamp flyback (ACF). In non-ACF designs, the GDH pin must be grounded.

The low-side gate driver can drive both traditional silicon and newer GaN MOSFETs. See the System Design Guidelines for design details of the low-side MOSFET driver and high-side ACF circuits.

2.7 Feedback in secondary-controlled system

In a PAG2x system, the feedback from the secondary to the primary side is transferred via a pulse transformer. The PWM and ACF control signals are transferred from the secondary to the primary via the same pulse transformer. The pulse transformer is a critical component in the system design; it is recommended to use Infineon part CYPET121 [7]. Figure 6 shows a CYPET121 pulse transformer used in a PAG2x system with the recommended R1, R2, and C1 values at 2.8 kΩ, 50 Ω, and 100 pF, respectively.

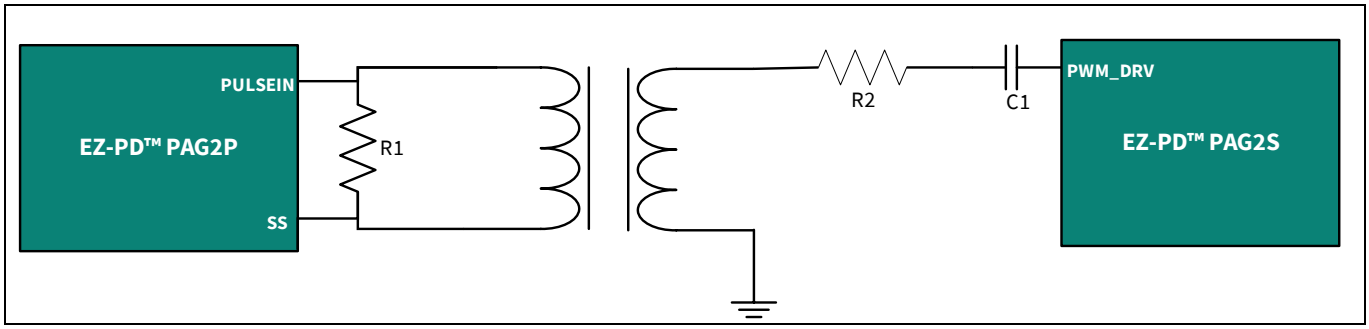


Figure 6 Pulse transformer

2.8 Feedback in primary-controlled system

PAG2S CYPAS213 can also work in a traditional primary-side-controlled flyback system using opto-feedback, as shown in Figure 7. In this case, an error amplifier similar to TL431 is integrated in PAG2S.

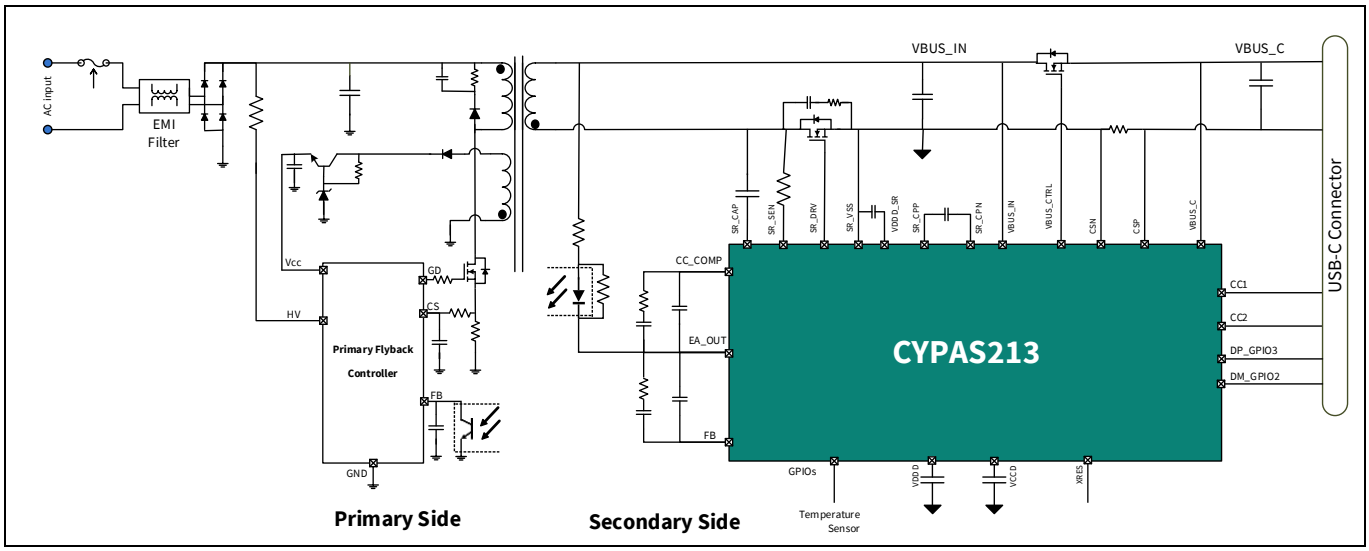


Figure 7 PAG2S in primary-controlled system

2.9 PAG2S power circuit

PAG2S integrates a high-voltage regulator, which is powered by the VBUS_IN rail; the regulator's output powers the VDDD rail. The input to the regulator can range from 3.3 V minimum to 30 V maximum. This regulator is intended to deliver PAG2S current consumption and is not expected to drive any external loads or ICs.

The regulated VDDD supply is either used to directly power some internal analog blocks or further regulated down to 1.8 V VCCD, which powers most of the core. VDDD and VCCD are brought to pins to connect external capacitors for regulator stability; these are not meant to be used as power supplies. Further, there is VDDD_SR and VSS_SR, the supply and ground for the internal SR driver. Figure 8 shows the recommended connection and decoupling capacitor values.

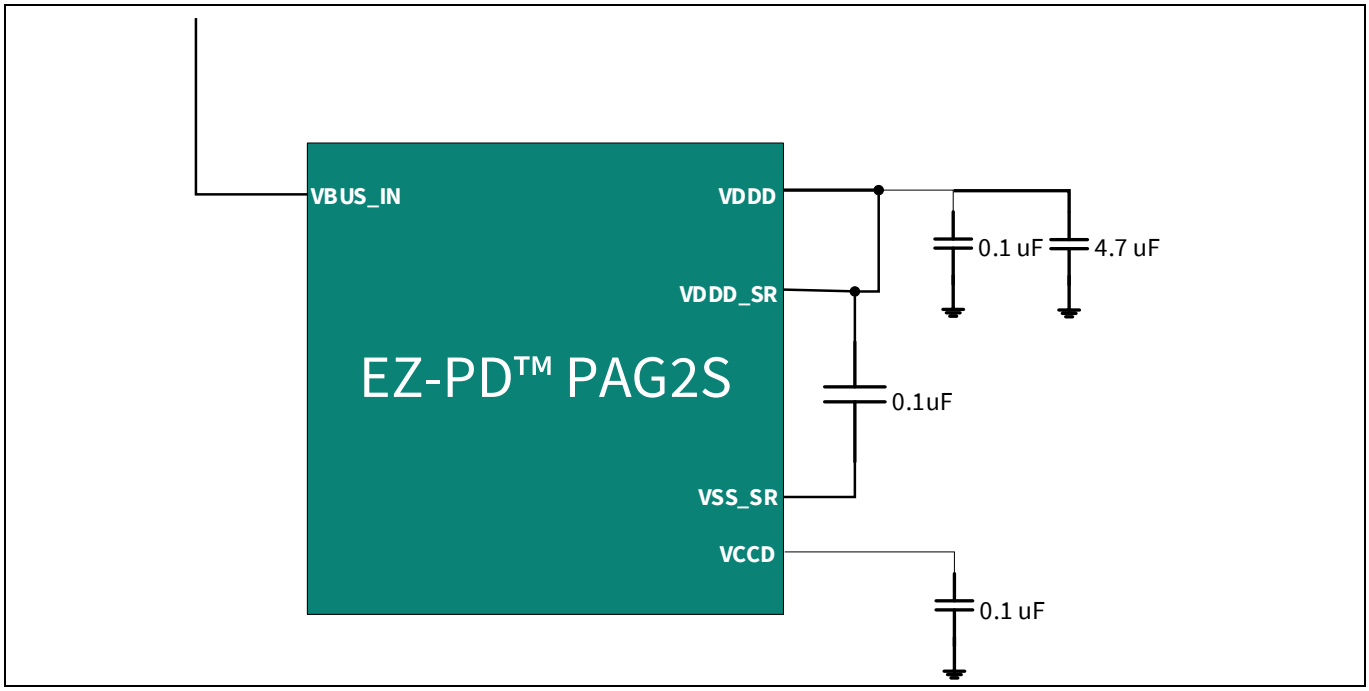


Figure 8 PAG2S power circuit

2.10 PAG2S SR gate driver

PAG2S senses the voltage across the synchronous rectifier NFET and appropriately controls the gate driver to achieve optimum efficiency. The voltage at the drain node of the external NFET is sensed on the SR_SEN pin connected via an external resistor. The gate driver (SR_GDRV) can be driven to the internal VDDD or twice the VDDD to achieve lower $R_{DS(on)}$ of the external NFET.

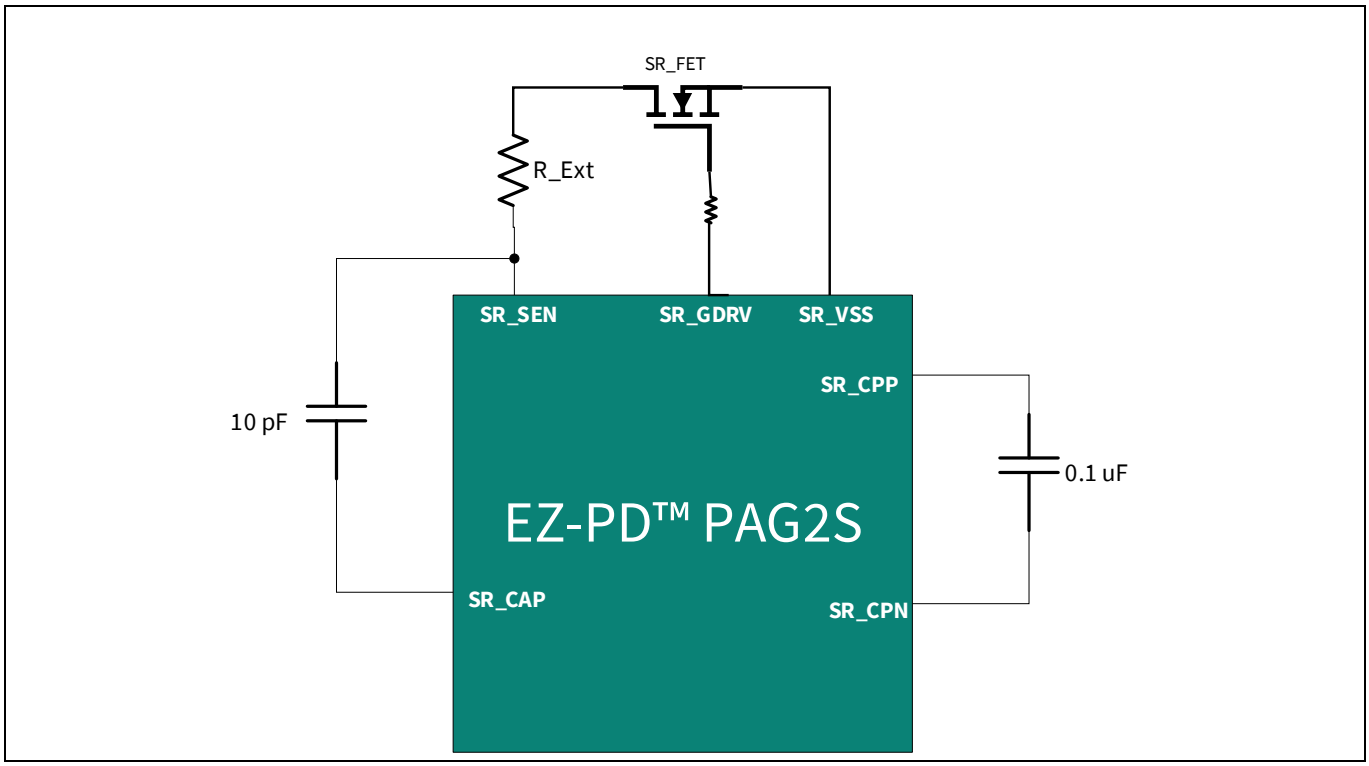


Figure 9 PAG2S SR driver

- The source terminal of the SR FET must be connected to the SR_VSS pin.
- The gate driver can be driven to twice the VDDD using an internal doubler circuit, with the doubler capacitor connected across the SR_CPP and SR_CPN pins. The recommended value for the doubler capacitor is 0.1 µF.
- For systems having resonance frequency on SR_DRAIN > 4 MHz, peak detect is sensed via the SR_CAP pin by coupling SR_DRAIN to SR_CAP via a 10-pF capacitor. If the resonance frequency < 4 MHz, the SR_CAP pin must be left floating.
- The external resistor (R_Ext) is required to restrict the voltage at the SR_SEN pin below 34 V. The external resistance on the SR_SEN pin depends on the turns ratio of the power transformer; see Table 1 for details.

Table 1 External resistance on SR_SN vs. turn ratio

Primary: Secondary turns ratio	Rext (Ω)
3:1	20 k
4:1	20 k
5:1	20 k
6:1	12 k
7:1	12 k
8:1	12 k

Primary: Secondary turns ratio	Rext (Ω)
9:1	12 k
10:1	12 k
11:1	12 k
12:1	12 k
13:1	12 k
14:1	12 k
15:1	12 k

2.11 PAG2S CV and CC compensation

PAG2S integrates two error amplifier blocks that handle secondary-output sensing and regulation for both constant voltage (CV) and constant current (CC) modes of operation. The error amplifier output feeds into the internal analog PWM block. The negative input of the error amplifier is the feedback (FB) pin, and the positive input is an internal voltage reference. Based on the desired VBUS output, the voltage at the FB pin will be changed using internal current source/sink IDACs.

An external compensation network is required between the FB and EA_OUT pins. The constant current operation uses an internal low-side current sense amplifier (LSCSA), the output of which feeds into an independent error amplifier, as shown in Figure 10. Constant current mode regulation requires an external compensation network between CC_COMP_GPIOx and EA_OUT. See the System Design Guidelines for details on designing the CV and CC compensation networks.

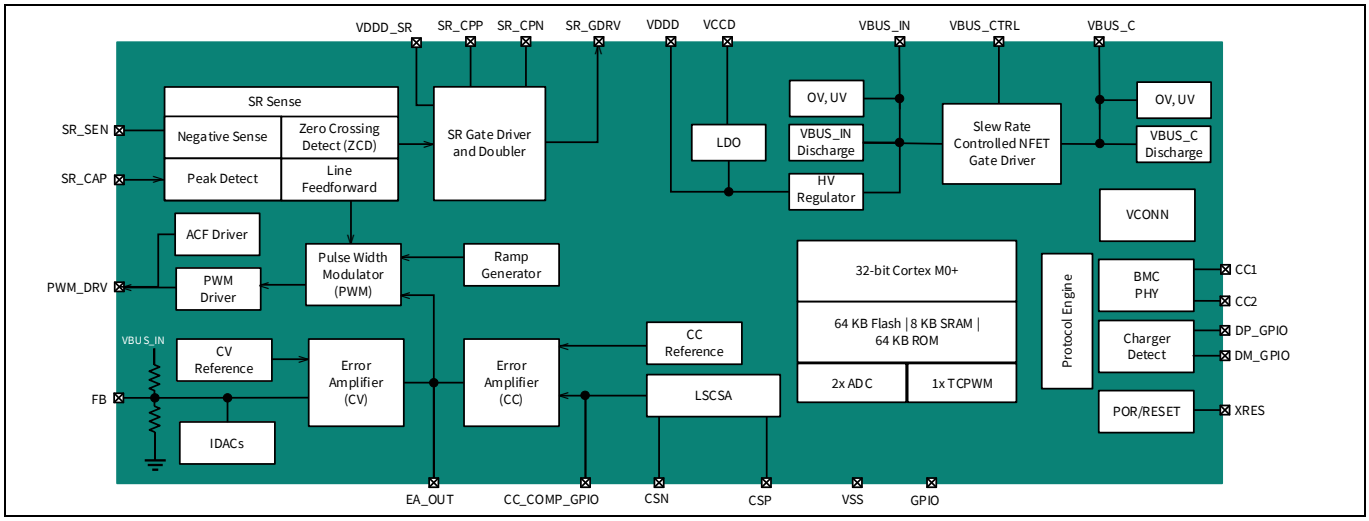


Figure 10 PAG2S functional block diagram

3 Layout guidelines

This section provides layout guidelines to be followed while designing a PAG2x system.

3.1 Primary-side ground loop

The primary-side has multiple ground points as highlighted in Figure 11– PAG2P IC GND (1), Boost GND (2), AUXIN capacitor GND (3), AUX winding GND (4), high-side driver GND (5), and bulk capacitor GND (6). It is recommended to hook up the multiple ground points in a star connection to the bulk capacitor GND as follows:

- AUXIN capacitor GND (3) and AUX winding GND (4) must be connected together and then connected to the bulk capacitor GND.
- PAG2P IC GND (1) and high-side driver GND (5) must be independently connected to the bulk capacitor GND.
- PAG2P IC GND (1) and boost GND (2) must be connected via a low-impedance path to the ground plane.
- The rest of the PAG2P circuit that are referenced to ground must be connected to PAG2P IC GND (1).
- Note that high-side driver GND is applicable for ACF designs only.

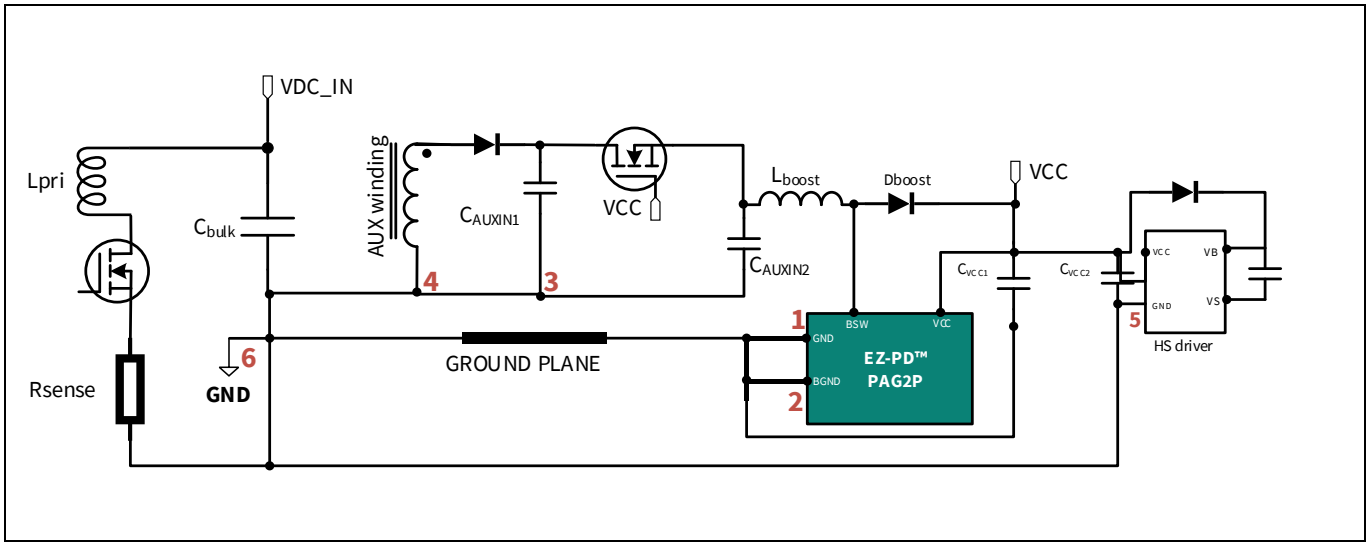


Figure 11 Primary ground loop

3.2 PAG2P boost circuit

PAG2P integrates a boost switch; the boost circuit can carry instantaneous high currents. The boost diode must be connected to the boost capacitor first and then to the PAG2P VCC pin as highlighted in Figure 12.

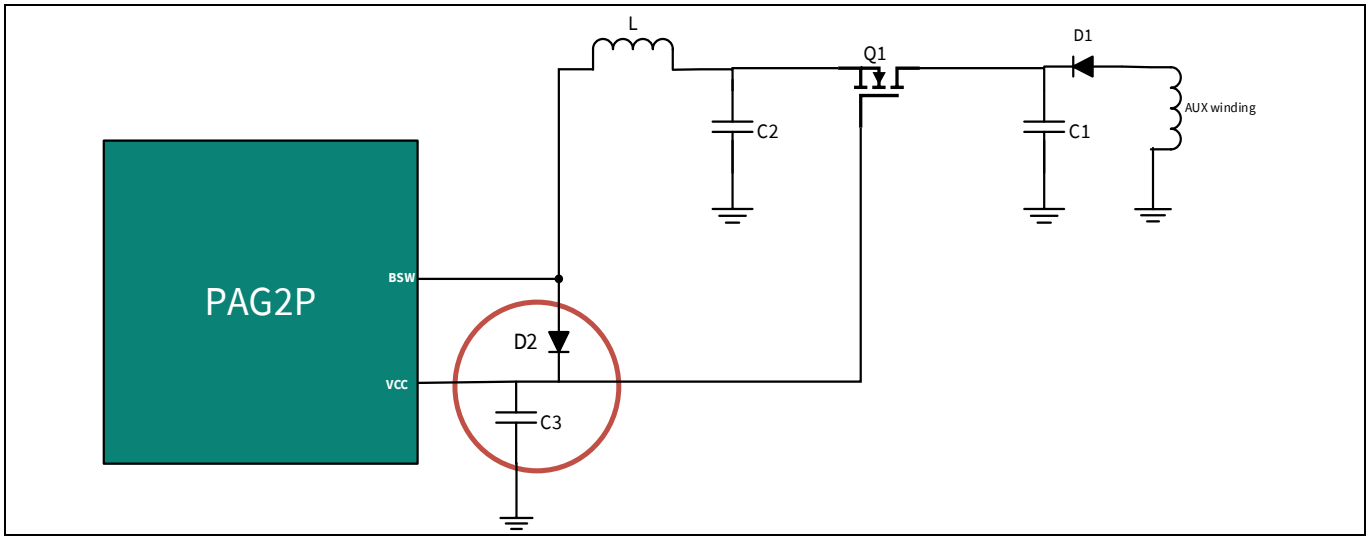


Figure 12 PAG2P boost circuit

3.3 PAG2S layout guidelines

Figure 13 shows a few layout guidelines as follows:

1. VDDD_SR and VSS_SR can be potentially noisy signals; a decoupling capacitor must be placed between these pins as close to the IC as feasible
2. Doubler capacitor between SR_CPP and SR_CPN must be placed as close to the IC as feasible
3. Shield the SR_SEN input signal with the ground
4. CSP/CSN input pair must follow Kelvin differential routing
5. Connect the output electrolytic capacitor ground and PAG2S ground VSS via a thick trace, and follow the same for the connection between the output electrolytic capacitor and the y-capacitor
6. PWM_DRV output to the pulse transformer must be as short as feasible and preferably shielded with the ground

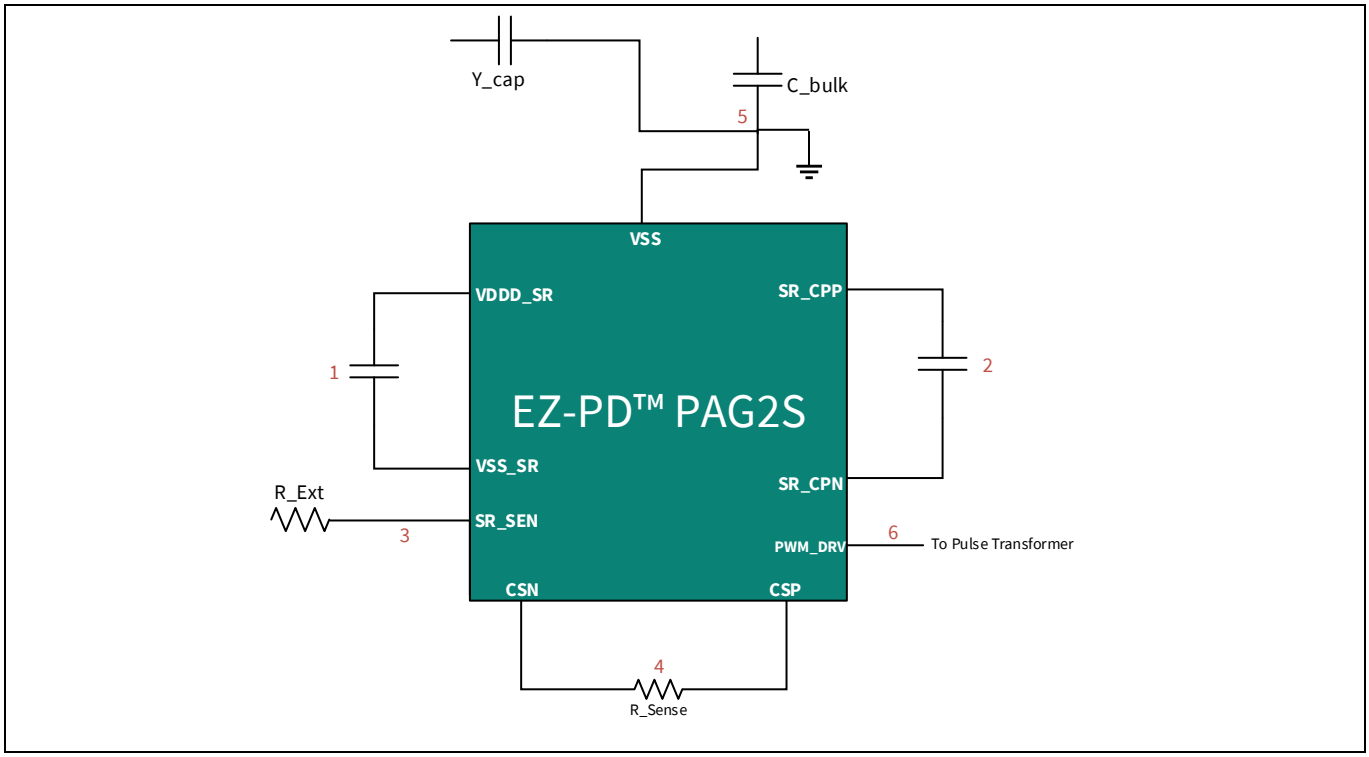


Figure 13 PAG2S layout guidelines

4 Hardware design calculator

The hardware design calculator tool is meant to assist customers in designing a flyback system using PAG2x. This tool requires system design parameters as input and provides guidelines in choosing critical hardware components. Contact Infineon support for more information on the design calculator.

5 Firmware development tools

PAG2S is a programmable secondary controller, with ModusToolbox™ software as the development environment. Infineon provides the base firmware required for each application, with the flexibility to further customize the firmware for each customer design. The first level of firmware customization can be done using the EZ-PD™ Configuration Utility; see Figure 14 for reference. The USB-PAT tool is required for configuring PAG2S via the EZ-PD™ Configuration Utility tool. The USB-PAT tool can be procured from here. Note that this option configures the high-level system parameters without accessing the base firmware.

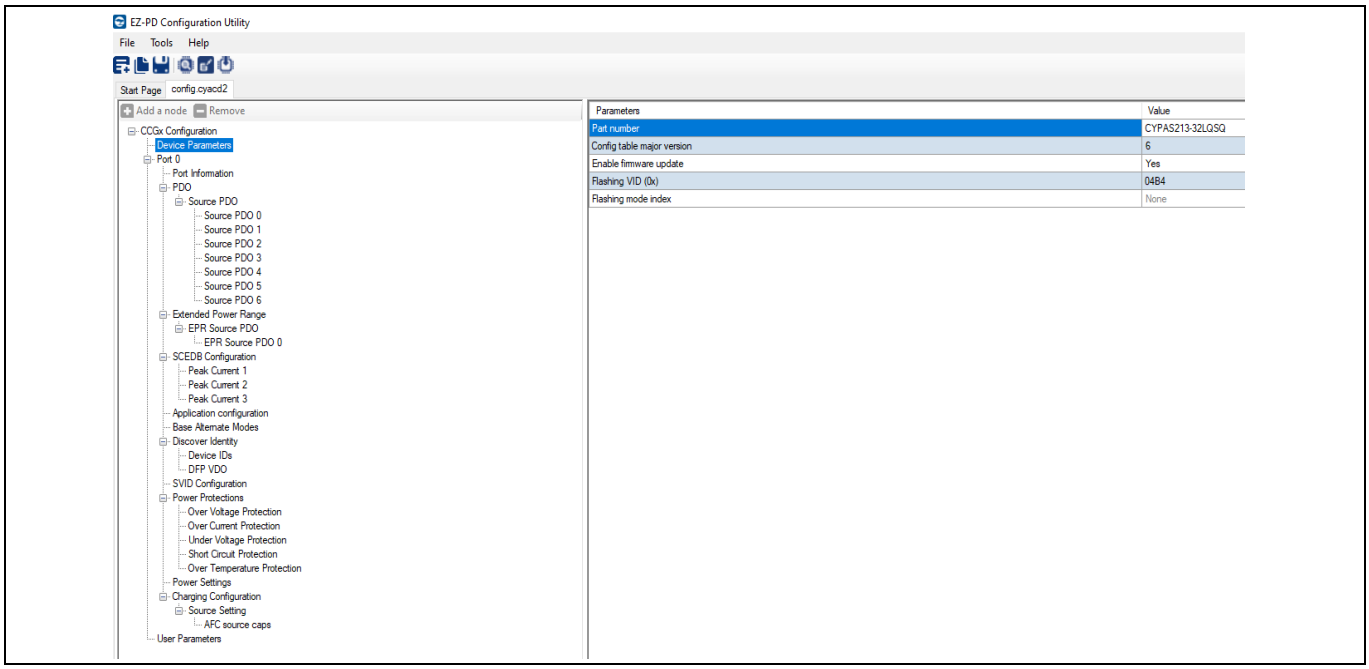


Figure 14 EZ-PD™ Configuration Utility

The next level of customization can be done by modifying the firmware using the ModusToolbox™ software. PAG2S supports a bootloader; the firmware can be updated on-the-fly. Firmware updates can be done using the EZ-PD™ Configuration Utility and USB-PAT tool. Contact Infineon support for more information on the firmware development tools and associated documents.

6 Reference designs

Multiple reference designs have been developed to showcase the capabilities of PAG2x controllers. These reference designs have gone through an extensive validation cycle and are also tested for USB PD compliance. The main intention of these reference designs is to enable the end customer with a well-tested design that can be used as starting point for their design. Contact Infineon support for more information on the available reference designs.

References

Contact Infineon support for these documents.

Application notes:

[1] Infineon Technologies AG: *AN236922 - EZ-PD™ PAG2x: Hardware design guidelines for ACF power adapters*

[2] Infineon Technologies AG: *AN238380 - EZ-PD™ PAG2x: Hardware design guidelines for quasi-resonant power adapters*

Datasheets:

[3] Infineon Technologies AG: *CYPAS213, EZ-PD™ PAG2S integrated USB PD and synchronous-rectification controller (Preliminary)*

[4] Infineon Technologies AG: *CYPAS211, EZ-PD™ PAG2S integrated USB PD and secondary-side ZVS controller (Preliminary)*

[5] Infineon Technologies AG: *CYPAS212, EZ-PD™ PAG2S integrated USB PD and secondary-side ACF controller (Preliminary)*

[6] Infineon Technologies AG: *CYPAP211/ CYPAP212, EZ-PD™ PAG2P primary-side startup controller*; Available online

[7] Infineon Technologies AG: *CYPET121, CYPET131, EZ-PD™ PAGxP-PAGxS Pulse edge transformer (PET) (Target)*

Revision history

Document revision	Date	Description of changes
**	2023-09-01	Initial release
*A	2024-03-26	Updated metadata

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