AIROC™ CYW89829 hardware design guidelines

About this document

Scope and purpose

This document provides hardware guidance on how to design with AIROC™ CYW89829 Bluetooth® & Bluetooth® LE system on chip.

Intended audience

This document is intended for hardware engineers creating PCB layout designs with CYW89829.

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1 Introduction

This document provides basic guidelines on the layout for CYW89829. This document is divided into the following sections:

- Basic layout guidelines include the board stackup and the impedance control requirements
- Component placements and recommended parts for the critical components
- Routing guidelines and the recommended trace width for various power traces

2 Basic layout guidelines

Most Bluetooth® devices use four-layer boards to minimize cost. Components are placed on the top layer; the top layer will also have the signal fanout from the CYW89829 chip. The second layer is a solid ground fill, power traces are routed on the third layer, and lastly, the digital signals and additional power traces that could not be routed on the third layer can be routed on the bottom layer.

For RF traces, use a 50-ohm transmission line to minimize mismatch losses and reflections, and therefore maximize the power transferred to the load.

There are two types of transmission lines: microstrip and stripline. The reference design uses the microstrip design.

Transmission lines require a proper geometry. Some parameters are highly dependent on the dielectric material – trace width, vertical distance to ground plane, and a solid ground plane as the reference. Different height and width solutions perform differently.

For the microstrip layer and its reference ground layer selections, the following two things should be considered:

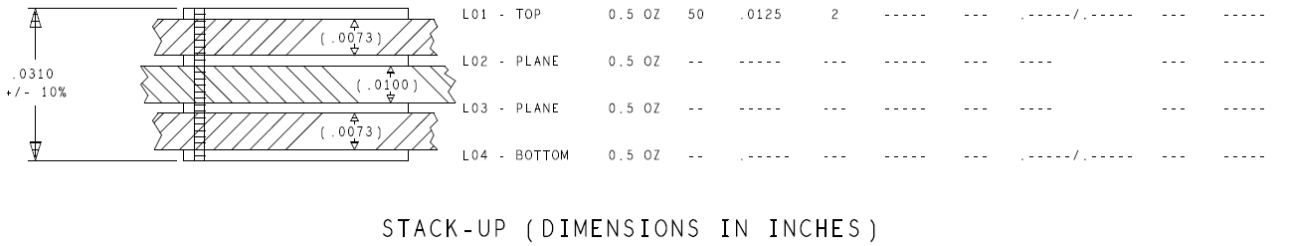
- Thinner traces have higher insertion loss, and PCB fabrication requires adequate trace width for reliability and repeatability. Heights between the microstrip and ground should be maintained per the stack up shown in Figure 1 to maintain 50-ohm impedance control.
- For microstrip lines, avoid sharp corners; use a smooth radius to change directions. The coplanar ground follows the contour of these traces with a clearance of two to three-line widths (2 W to 3 W). Connect the outer layer to the reference ground plane using vias so that they surround the microstrip trace.

The microstrip used in this reference design is on layer 1 with a trace width of 12.5 mils. The reference ground is layer 2.

This reference design uses a four-layer PCB with a stackup as shown in Figure 1:

- Layer 1: Components and main signal layer
- Layer 2: Solid ground layer
- Layer 3: Power signal layer

Layer 4: Digital signal layer. Additional power signals that could not be routed on layer 3 can be routed here. However, ensure that they do not overlap any of the power signals on layer 3.



LAYER DESCRIPTION	START COPPER WT	SE IMP OHMS	SE TRACE WIDTH	REF LAYER	CPW SPACE	DIFF IMP OHMS	DIFF TRACE WIDTH/SPACE	REF LAYER	CPW SPACE
L01 - TOP	0.5 OZ	50	.0125	2	-----	---	.-----/.-----	---	-----
L02 - PLANE	0.5 OZ	--	-----	---	-----	---	----	---	-----
L03 - PLANE	0.5 OZ	--	-----	---	-----	---	----	---	-----
L04 - BOTTOM	0.5 OZ	--	.-----	---	-----	---	.-----/.-----	---	-----

Figure 1 Typical board stackup used for CYW89829

3 Component placement

As a rule, follow the receive signal flow from the antenna to the antenna matching and filter circuits, then to the low-noise amplifier (LNA) chip input. Keep the radio front end (RF), power management unit (PMU), and baseband (BB) decoupling capacitors next to the CYW89829 pin pads.

NOTE: All components for CYW89829 (capacitors, inductors, XTAL, etc.) must be automotive AEC-Q200 Grade 2 certified.

3.1 PAVDD supply for CYW89829

- For CYW89829 Class 1.5, BT_PAVDD must be connected to VCCPA (PALDO_OUT (2.5 V)).
- For CYW89829 Class 2.0, BT_PAVDD must be connected to VCCRF (RFLDO_OUT (1.2 V)).

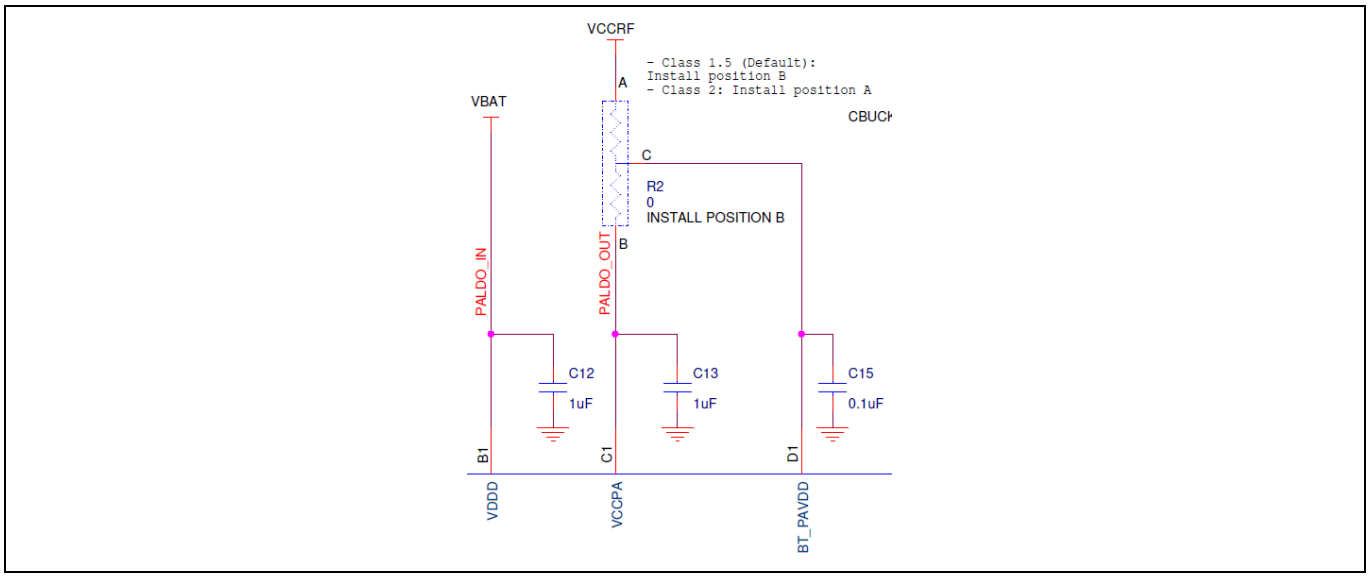


Figure 2 PAVDD supply configuration for CYW89829

3.2 PALDO input/output supply for CYW89829

VDDD (pin B1) is the PALDO input that requires a 1.0-µF decoupling capacitor. VCCPA (pin C1) is the PALDO output that require one 1.0µF decoupling capacitor with PAVDD supply strapping option.

Table 1 PALDO decoupling capacitor specification

Parameter	Conditions	Typ.	Unit
VDDD PALDO input capacitor (C12)	1µF ±20%, 10Vdc, X6S, AEC-Q200	1	µF
VCCPA PALDO output capacitor (C13)	1µF ±20%, 10Vdc, X6S, AEC-Q200	1	µF

3.3 Decoupling capacitor placement

The following schematic design shows the PMU and the RF front-end section. When making determinations about the part placements on the PCB, the following requirements must be met:

- VBAT inputs, which consist of VDDQ (Pin C3) and VCC_BUCK (Pin A6) must have a 0.1µF capacitor (C9) placed as close to pin C3 as possible and a 10µF capacitor (C35) placed as close to pin A6 as possible.
- Both the 4.7µH (L1) power inductor and 4.7µF capacitor (C11) must be placed as close to LX_BUCK (Pin A4) as possible.
- VCCI (Pin A3) must have a 0.1µF (C16) capacitor placed as close to the pin as possible.
- VCCRF (Pin A2) must have a 0.1µF capacitor (C17) and a 1.0µF capacitor (C18) placed as close to the pin as possible.
- BT_VCOVDD (Pin G2) must have a 10pF capacitor (C22) and a 0.1µF (C23) capacitor placed as close to the pin as possible.
- BT_LNAVDD (Pin G1) must have a 0.1µF capacitor (C19) placed as close to the pin as possible.
- BT_IFVDD (Pin D2) must have a 0.1µF capacitor (C20) placed as close to the pin as possible.
- BT_PLLVDD (Pin H2) must have a 0.1µF capacitor (C21) placed as close to the pin as possible.
- VCCPA (Pin C1) must have a 1µF capacitor (C13) placed as close to the pins as possible.
- BT_PAVDD (Pin D1) must have a 0.1µF capacitor (C15) placed as close to the pin as possible.
- VDDD (Pin B1) must have a 1µF capacitor (C12) placed as close to the pin as possible.

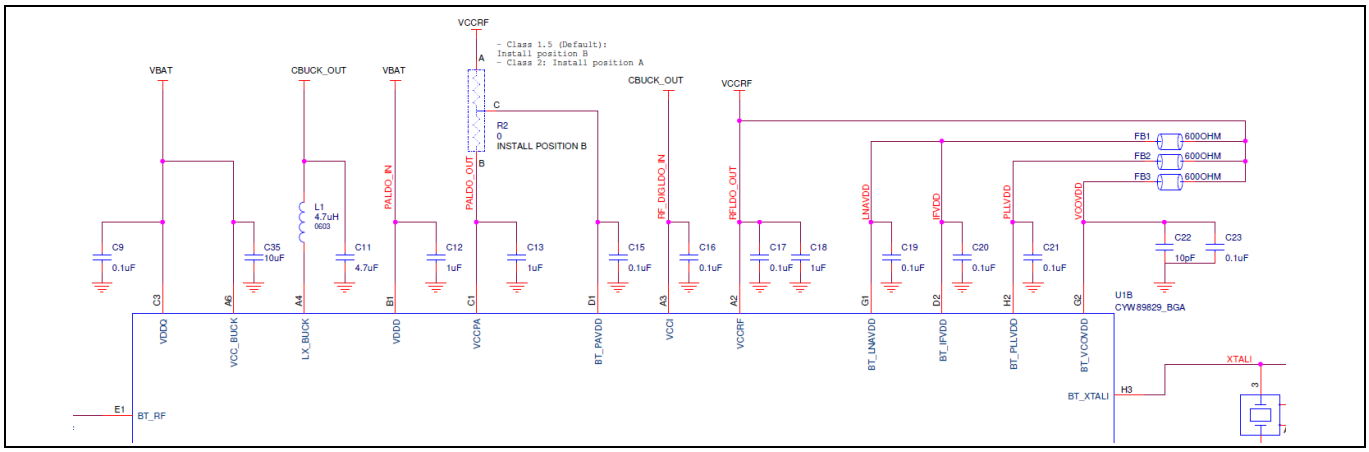


Figure 3 Decoupling capacitors in the PMU and RF front end area

Table 2 PMU and RF front-end decoupling capacitor specification

Parameter	Conditions	Typ.	Unit
VDDQ input capacitor (C9) PAVDD input capacitor (C15) VCCI input capacitor (C16) VCCRF output capacitor (C17) LNAVDD input capacitor (C19) IFVDD input capacitor (C20) PLLVDD input capacitor (C21) VCOVDD input capacitor (C23)	0.1µF ±10%, 10Vdc, X6S, AEC-Q200	0.1	µF

Component placement

Parameter	Conditions	Typ.	Unit
VCCRF output capacitor (C18)	1µF ±20%, 10Vdc, X6S, AEC-Q200	1	µF
LX_BUCK output capacitor (C11)	4.7µF ±20%, 10Vdc, X6S, AEC-Q200	4.7	µF
VCC_BUCK input capacitor (C35)	10µF ±20%, 6.3Vdc, X6S, AEC-Q200	10	µF
VCOVDD input capacitor (C22)	10pF ±1%, 25Vdc, C0G, AEC-Q200	10	pF

In the baseband area, the following component placement must also be met:

- VDDIO_A (Pin A7), VDDIO_0 (Pin H8), and VDDIO_1 (Pin G10) must have a 4.7µF capacitor (C38) that covers all 3 pins, and each pin must have a 0.1µF capacitor (C3, C4, C5). All capacitors must be placed as close to the pin as possible.
- VCCD (Pin B2) must have a 2.2µF capacitor (C29) and a 0.1µF capacitor (C2) placed as close to the pin as possible. Place 0.1µF capacitor (C2) closer to the pin.
- ADC_VDD (Pin C10) and VCC (Pin F10) must have a 0.1µF capacitor (C7, C28) placed as close to the pin as possible.

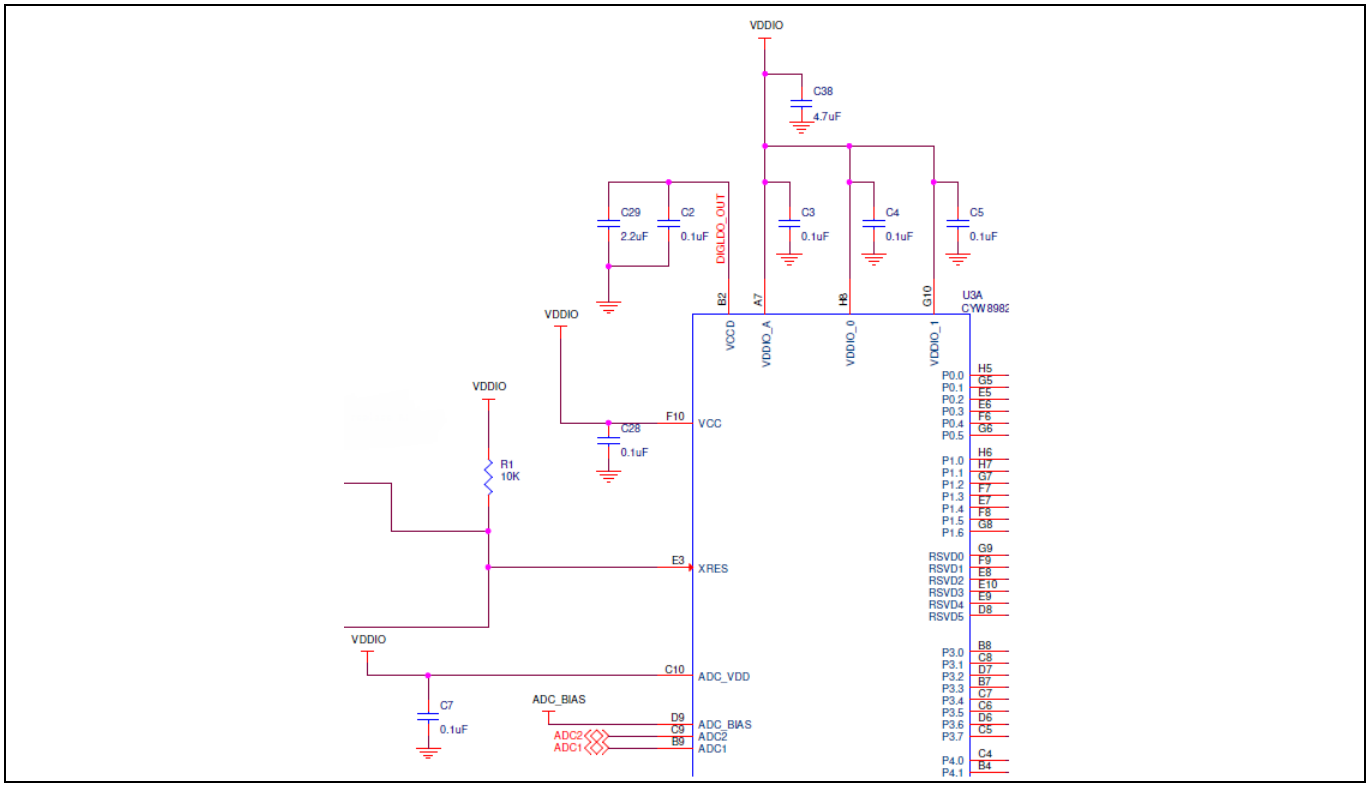


Figure 4 Decoupling capacitors in the baseband area

Table 3 Baseband decoupling capacitor specification

Parameter	Conditions	Typ.	Unit
VDDIO input capacitors (C3, C4, C5, C7, C28) VCCD output capacitor (C2)	0.1µF ±10%, 10Vdc, X6S, AEC-Q200	0.1	µF
VDDIO input capacitor (C38)	4.7µF ±20%, 10Vdc, X6S, AEC-Q200	4.7	µF
VCCD output capacitor (C29)	2.2µF ±10%, 6.3Vdc, X6S, AEC-Q200	2.2	µF

3.4 Antenna placement

Keep the antenna connection to the device as short as possible. Maintain a solid ground near the antenna and adequate ground clearance for the layers beneath the antenna.

In the reference design, the antenna is on the top layer on the left of the board next to the CYW89829 chip.

For more details on PCB antennas general guideline, see AN91445 - Antenna design and RF layout guidelines. For the associated Gerber file, click here.

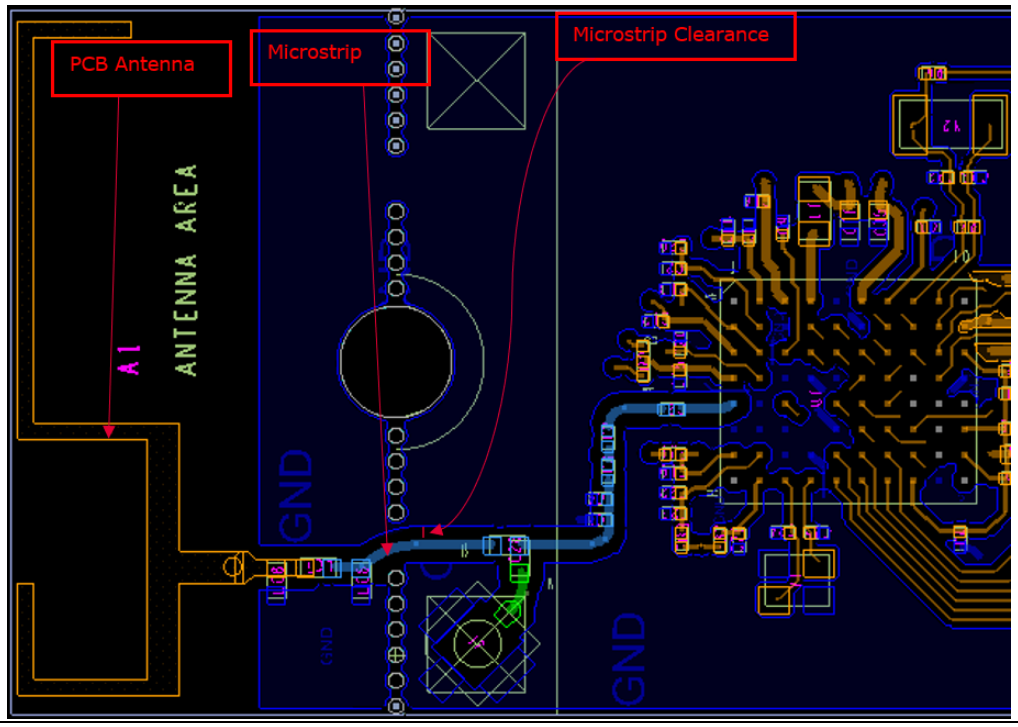


Figure 5 Antenna placement and microstrip clearance

3.5 4-Element Bandpass Filter

Place a 4-Element bandpass filter between the antenna matching components and the CYW89829 device to attenuate harmonics from CYW89829. The 4-Element bandpass filter used in the CYW89829 reference design is Murata LQP03TN3N6BZ2D for LC2, Murata GCQ0335C1H1R5BB01D for LC3, Murata GCQ0335C1H3R0BB01D for LC4, and Murata LQP03TN1N8BZ2D for LC5. The value of the inductors and capacitors may vary depending on the PCB and the board stackup. A microstrip is used for all connections of the bandpass filter.

Insertion loss and out-of-band attenuation performance depend on PCB component layouts and tolerances. Filter layout should follow general RF layout rules. In general, expect an insertion loss of around 1 dB at 2.4GHz. For the BPF attenuation, expect 25 dB attenuation for 4.8GHz, and 29 dB attenuation at 7.2GHz.

Table 4 4-Element bandpass filter component specification

Parameter	Conditions	Typ.	Unit
1st element LC2 inductor	3.6nH ±0.1nH, high Q, DCR 300mΩ, AEC-Q200	3.6	nH
2nd element LC3 capacitor	1.5pF ±0.1pF, high Q, 50Vdc, C0G, AEC-Q200	1.5	pF
3rd element LC4 capacitor	3.0pF ±0.1pF, high Q, 50Vdc, C0G, AEC-Q200	3.0	pF
4th element LC5 inductor	1.8nH ±0.1nH, high Q, DCR 150mΩ, AEC-Q200	1.8	nH

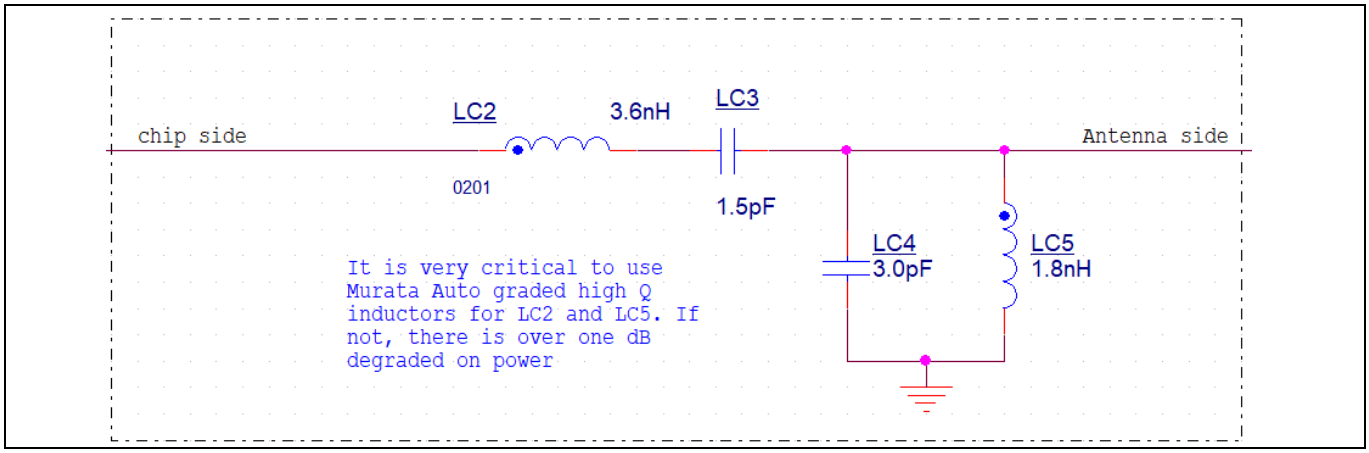


Figure 6 Schematic diagram of 4-Element bandpass filter

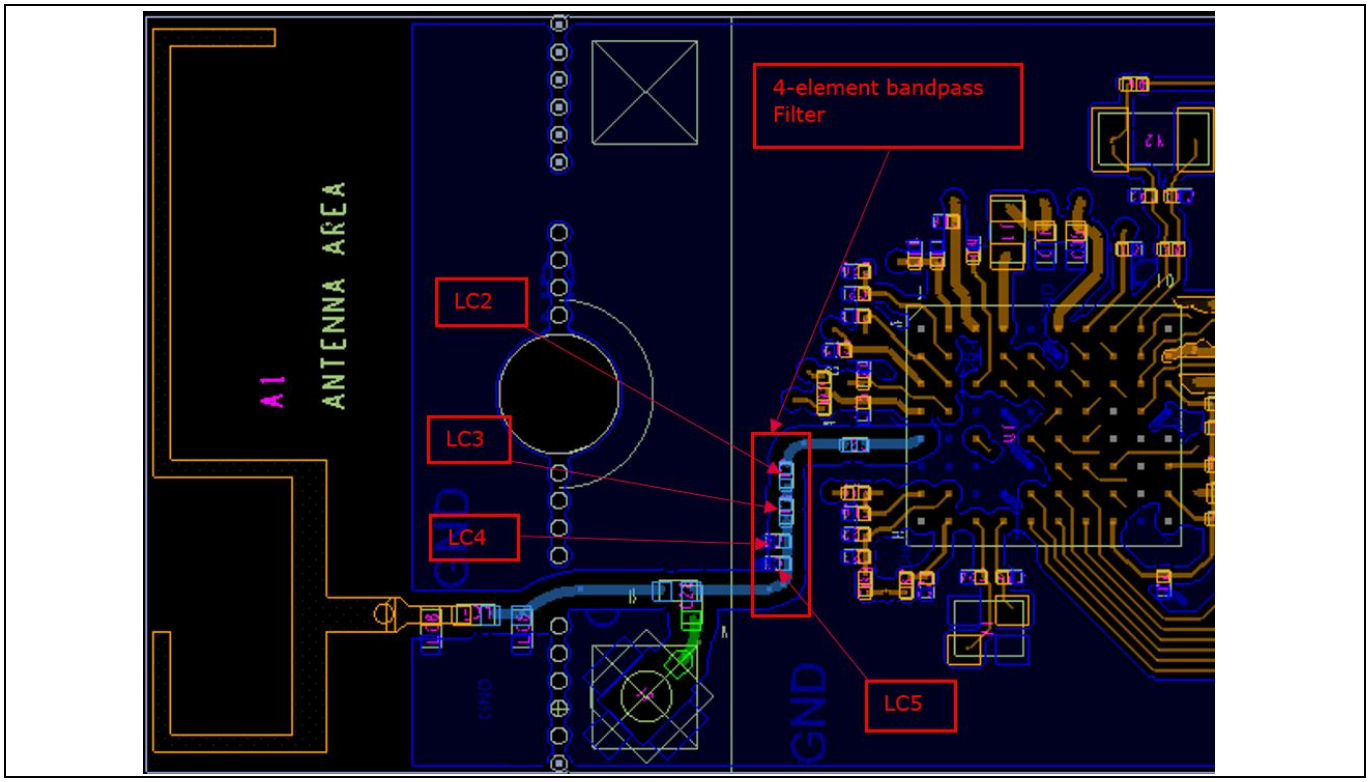


Figure 7 4-Element bandpass filter placement

3.6 Power inductor placement

The power inductor must have good isolation; this is done by surrounding it with as much ground as possible. The power inductor should also be placed as close to CBUCK_OUT pin (LX_BUCK, Pin A4) as possible. The inductor should be placed adjacent with the output capacitor (C11 in this design). The copper on the PCB top layer under this inductor should be cut out. Ensure the ground return path for output capacitors has the least resistance to VSSBUCK ground pin and is well isolated from the rest of the ground plane. This will prevent the noise coming from CBUCK switching regulator to be distributed to other ground; the noise will go directly back into the VSSBUCK ground pin. The power inductor part used in the CYW89829 reference design is ASCYFT1608084R7MCP.

Table 5 Power inductor specification

Parameter	Conditions	Typ.	Unit
External inductor, L1	4.7µH ±20%, DCR = 250 mΩ ±20% (for frequency < 1 MHz), AEC-Q200	4.7	µH

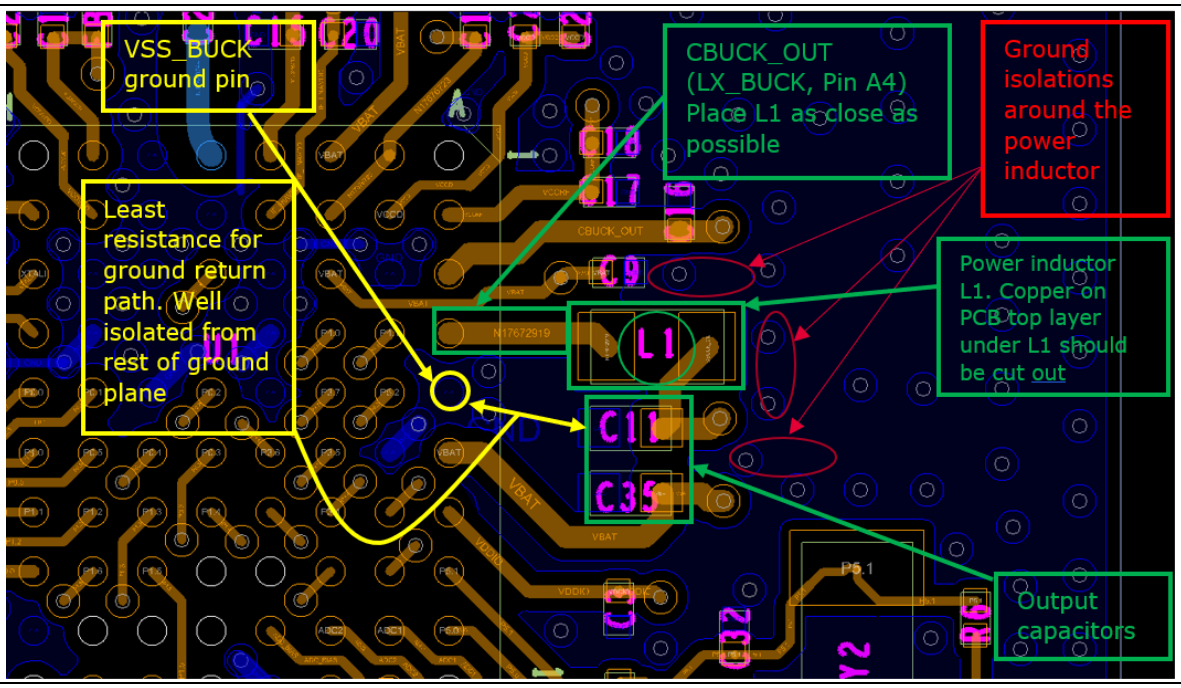


Figure 8 Power inductor isolation and placement

3.7 Crystal specifications and requirements

For the crystal parts, TXC AY24070304 is recommended for the 24 MHz main crystal, and TXC AH03270005 for the 32.768 kHz crystal.

Note: The 32.768-kHz crystal is optional and may be omitted. CYW89829 has an internal Precision Internal Low-speed Oscillator (PILO).

The 24-MHz crystal oscillator must have an accuracy as defined by the Bluetooth® specification. Two external load capacitors are required to work with the crystal oscillator. The selection of the load capacitors is crystal dependent (see Figure 9).

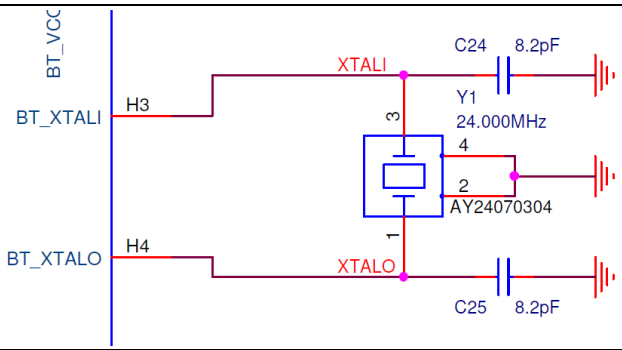


Figure 9 Recommended oscillator configuration for 24-MHz crystal

Crystal specifications and requirements for the 24-MHz crystal can be found in Figure 10.

	Parameters	Sym.	Electrical Spec.				Notes
			Min.	Typ.	Max.	Units	
1	Nominal Frequency	FL		24.000000		MHz	-
2	Oscillation Mode	-		Fundamental		-	-
3	Load Capacitance	CL		8		pF	-
4	Frequency Tolerance	-		±10		ppm	at 25 ℃ ± 3 ℃
5	Frequency Stability	-		±20		ppm	Over Operating Temp. Range (Reference 25℃)
6	Operating Temperature	-	-40	~	105	℃	-
7	Aging	-		±3		ppm	1st Year at 25 ℃ ± 3 ℃
8	Drive Level	DL	-	100	200	μW	-
9	Equivalent Series Resistance	RR	-	-	60	Ω	-
10	Shunt Capacitance	C0	-	-	2	pF	-
11	Insulation Resistance	-	500	-	-	MΩ	at DC 100V
12	Storage Temperature Range	-	-40	~	125	℃	-

Figure 10 Reference crystal electrical specifications for 24-MHz crystal

The optional 32.768-kHz crystal oscillator must have an accuracy of ±250 ppm or better per the Bluetooth® spec over temperature and including aging. The default component values are: C32 = C33 = ~6 pF. The values of C32 and C33 are used to fine-tune the oscillator. Figure 11 shows the 32.768 kHz XTAL oscillator with external components and Figure 12 lists the oscillator's characteristics.

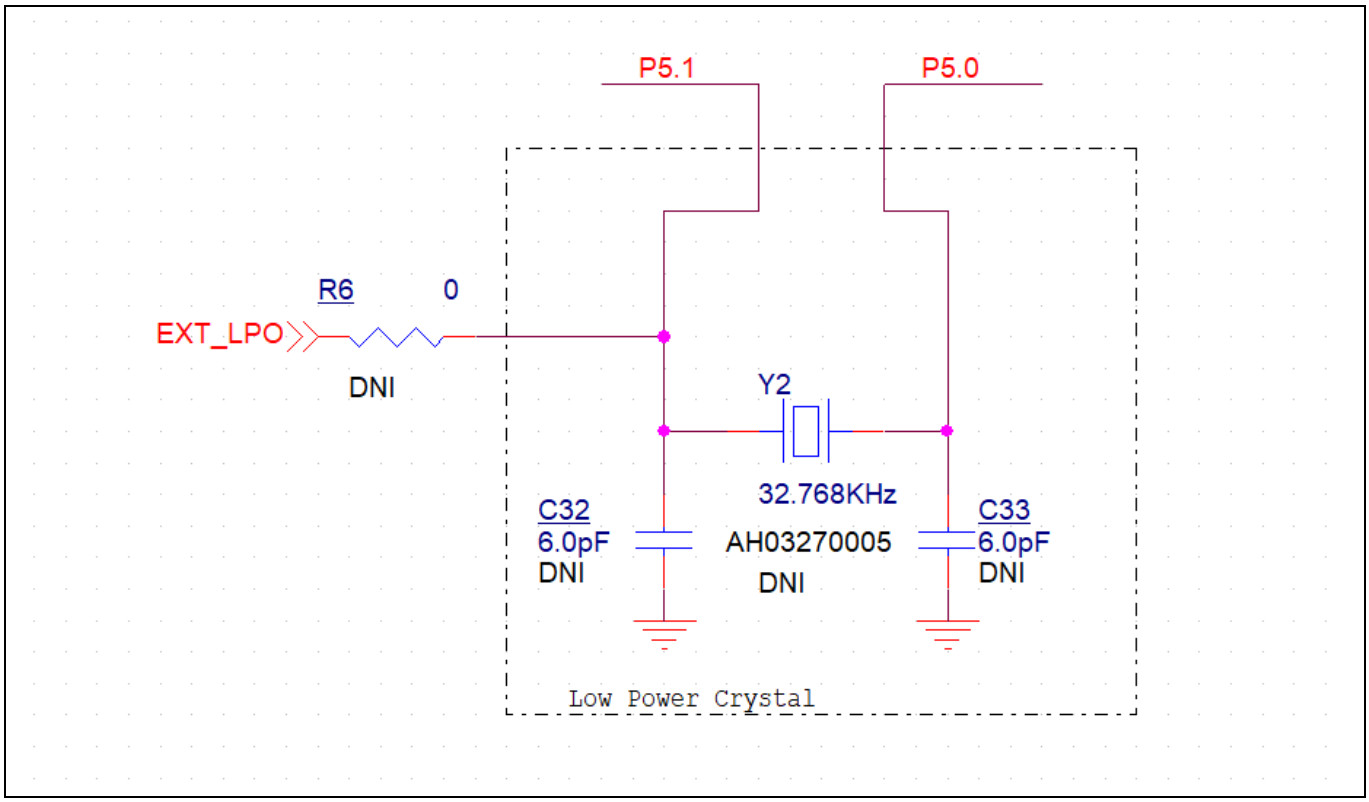


Figure 11 Recommended oscillator configuration for 32.768-kHz crystal

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output frequency	F_{oscout}	–	–	32.768	–	kHz
Frequency tolerance	–	Over temperature and aging	–	–	250	ppm
XTAL drive level	P_{drv}	For crystal selection	–	–	0.5	µW
XTAL series resistance	R_{series}	For crystal selection	–	–	70	kΩ
XTAL shunt capacitance	C_{shunt}	For crystal selection	–	–	2.2	pF

Figure 12 32.768-kHz XTAL oscillator characteristics

3.8 Crystal placement

Protect the crystal and related traces from noise sources and use a solid ground to separate the crystal from RF traces. The crystal ground plane should have direct vias to the reference ground plane.

The load capacitors placement as shown in Figure 13 is recommended, because this placement uses the least amount of PCB trace to connect the CYW89829 chip, the crystals, and the crystal load capacitors together which will minimize the parasitic capacitance.

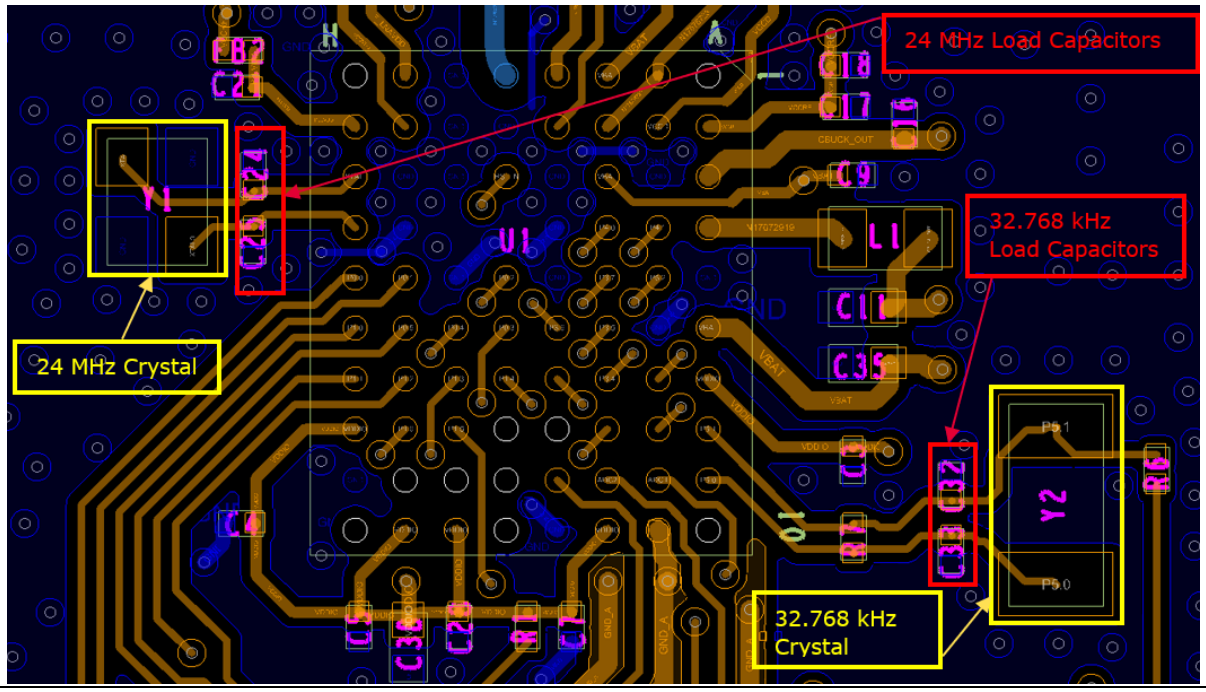


Figure 13 24-MHz and 32.768-kHz crystal placements

4 PCB layers and routing

4.1 Ground vias

Do not use long thin traces to connect components to ground vias; instead, cover entire ground pad with ground copper and place the ground vias as close to the ground pad as possible. Via on pad is required for the ground pad of CYW89829. Only use through hole vias in the open area to stitch the ground plane on all layers together. Ensure that there are enough ground pins near the ground pad of the CBUCK output capacitor (C11 in the reference design).

4.2 Layer 1: Components, signal fanout, and RF trace

All the passive components for the chip can be placed on the top layer. Signal fanout from the CYW89829 chip will also be done on the top layer.

The RF trace, shown as red, must be well isolated and have a solid ground plane along both sides of the trace. Ensure that this RF trace is 50-ohm impedance matched.

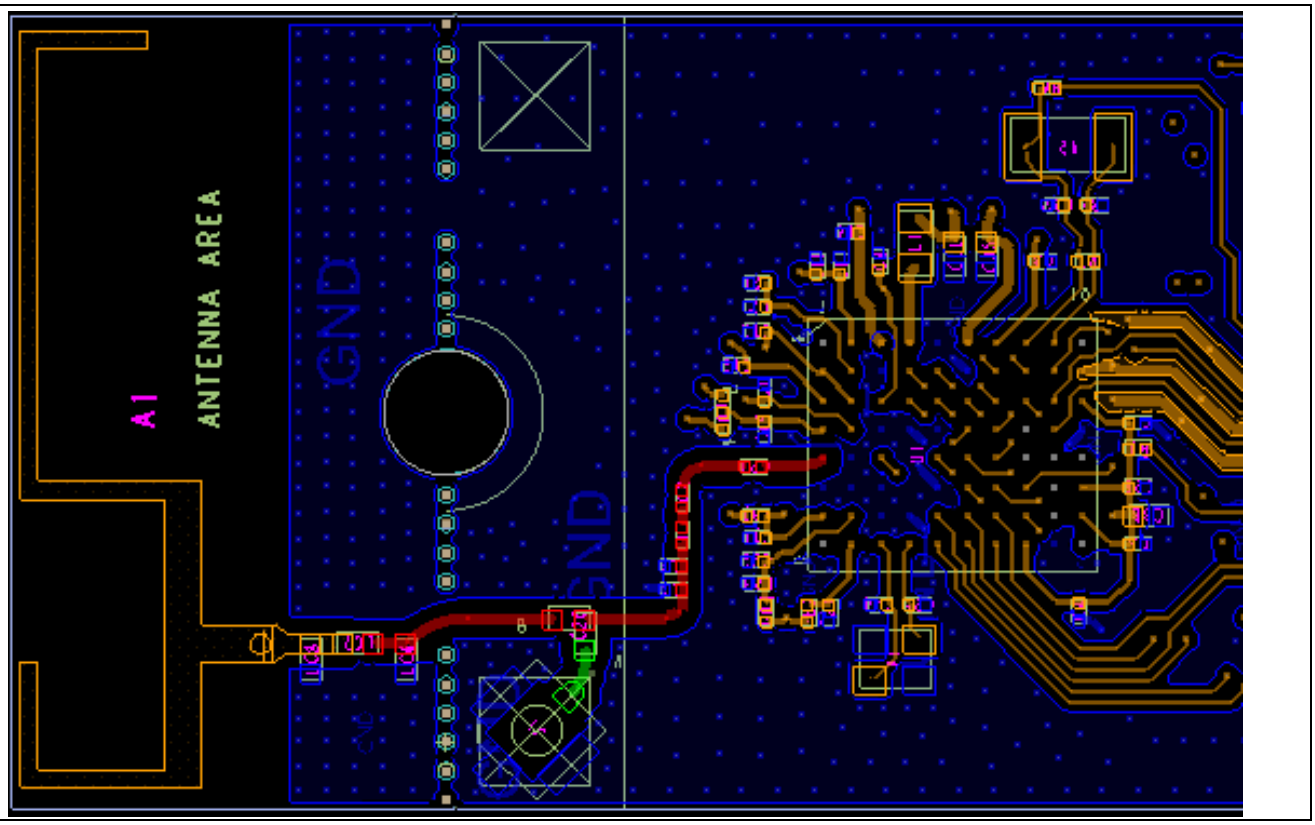


Figure 14 Layout 1, components and signal fanout

Have a dedicated analog ground plane for the ADC and use ground ties to connect analog ground and digital ground on the PCB to avoid analog ground noise from spreading.

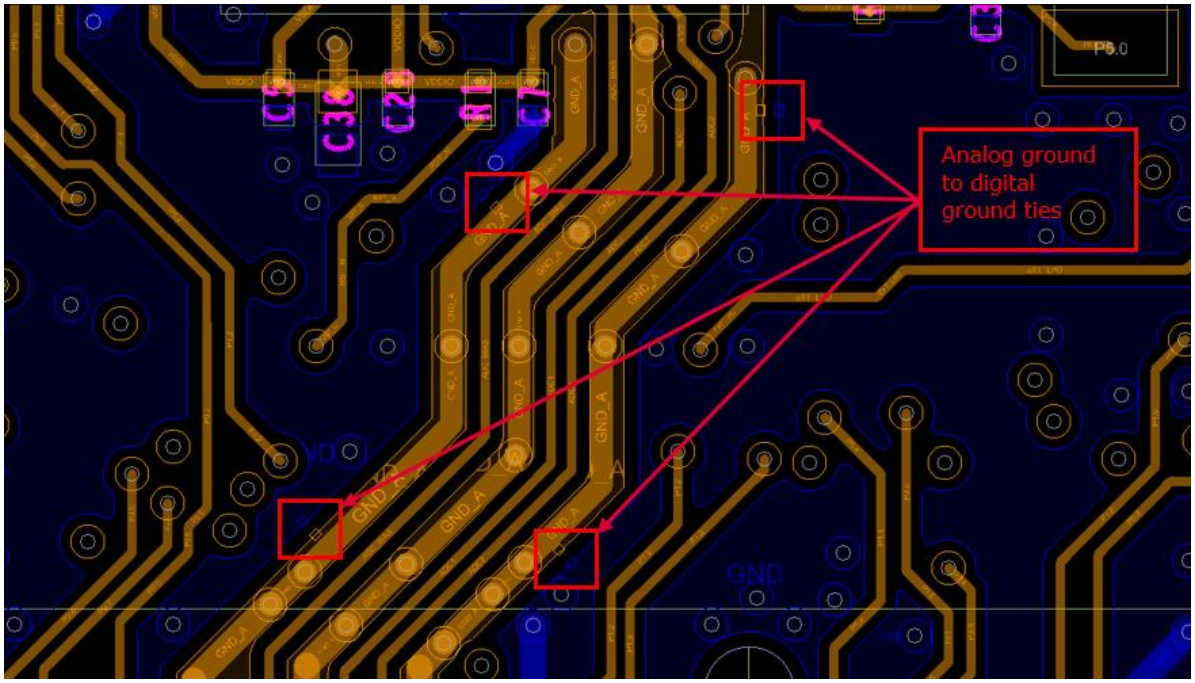


Figure 15 Layout 1, analog ground to digital ground ties

4.3 Layer 2: Solid ground plane

Fill the layer immediately below the layer where CYW89829 is located with the solid ground plane for the optimal ground return path. The green portion is for the analog ground plane.

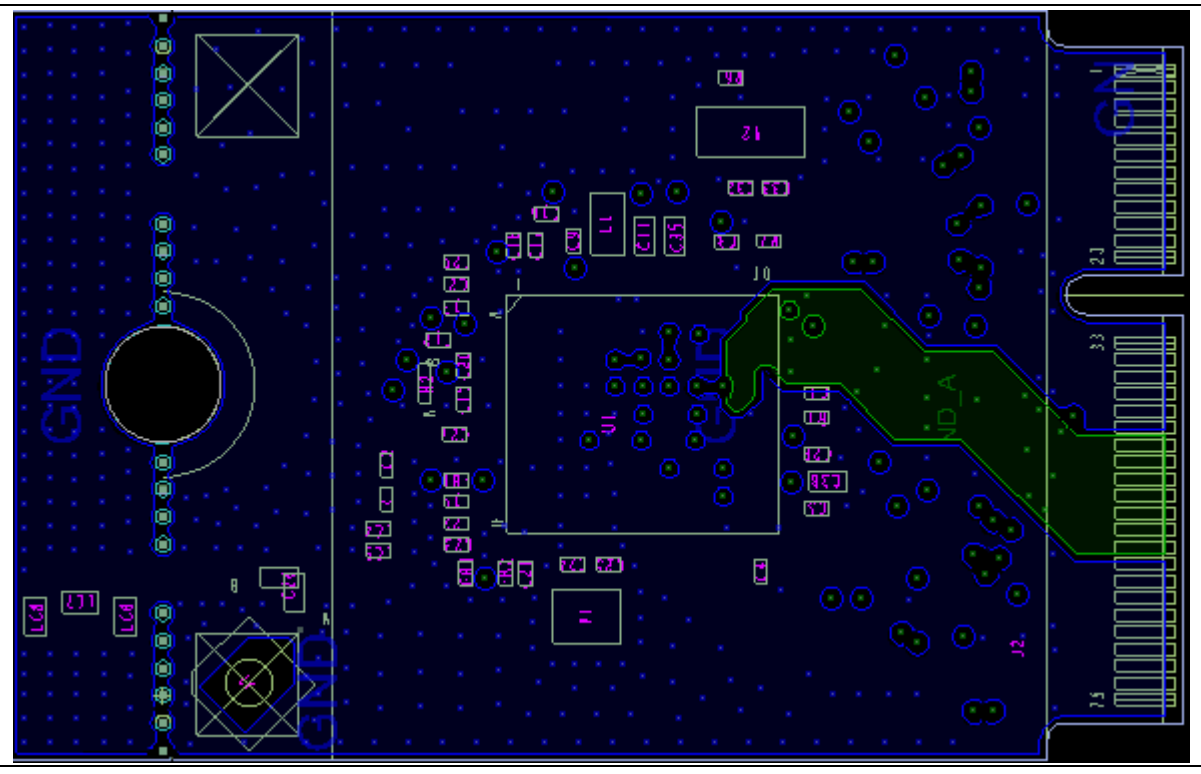


Figure 16 Layer 2, solid ground fill

4.4 Layer 3: Power traces

- Route the main DC power supply line up the middle of the board like a spine, branching off left and right as needed.
- Avoid routing DC power in a loop.
- Consider the current flow when routing the power traces to the chip. For input power pins, ensure that the power trace goes through the decoupling capacitors before going into the power pin. For output power pins, ensure that the power trace goes to the decoupling capacitors immediately before going to the load.
- Protect the RF power supply from main power, noisy signals, and digital power by separating with ground fill.
- Ensure that adequate power trace width and vias are available (or present) to minimize parasitic impedance.
- Crossing or overlapping power traces on adjacent layers is not recommended. In the case where power traces crossing cannot be avoided, have them cross in a perpendicular manner to minimize the overlapping area of the power traces. (See section 4.6)
- Recommended Trace width for the power signals are as follows:
  - CBUCK_OUT to LX_BUCK (Pin A4) - Minimum 10-mils trace width
  - CBUCK_OUT to VCCI (Pin A3) - Minimum 10-mils trace width
  - VDDIO - Minimum 8-mils trace width
  - VCCD (Pin B2) - Minimum 5-mils trace width
  - VBAT to VDDQ (Pin C3) - Minimum 5-mils trace width
  - VBAT to VCC_BUCK (Pin A6) - Minimum 12-mils trace width
  - VCCRF (Pin A2) to BT_LNAVDD (Pin G1)/ BT_PLLVDD (Pin H2) - Minimum 8-mils trace width
  - VCCRF (Pin A2) to BT_VCOVDD (Pin G2)/ BT_IFVDD (Pin D2)– Minimum 5-mils trace width
  - VDDD (Pin B1) to BT_PAVDD (Pin D1) - Minimum 8-mils trace width
  - VCCPA (Pin C1) to BT_PAVDD (Pin D1) - Minimum 8-mils trace width
  - ADC_BIAS (Pin D9) - Minimum 5-mils trace width

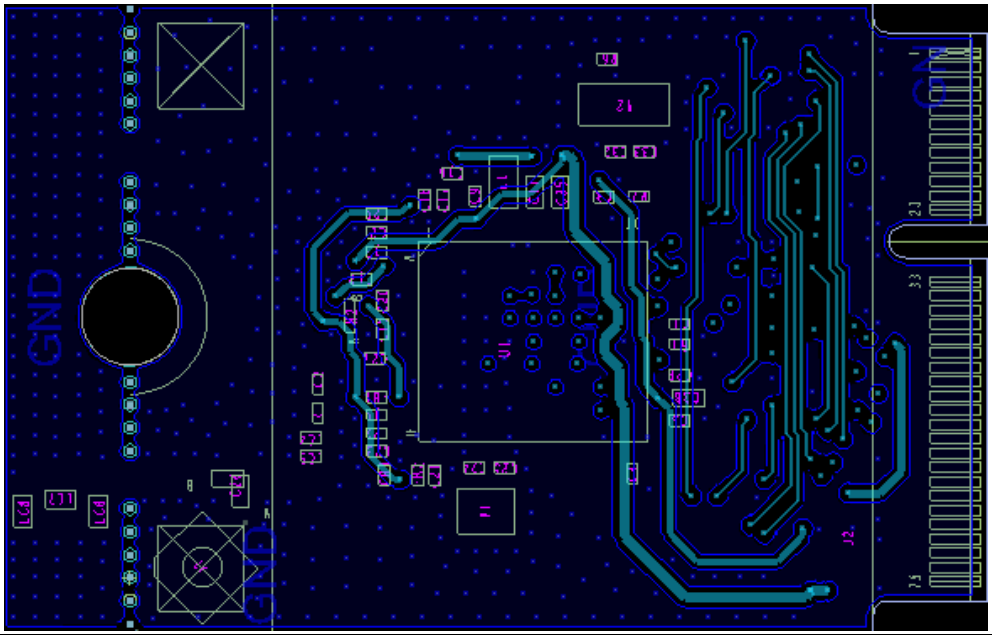


Figure 17 Power supply traces on layer 3

4.5 Layer 4: Power traces and non-critical signals

Use layer 4 for all non-critical signal routing and additional power traces that could not be routed on layer 3. Ensure that the power traces routed on layer 4 do not cross with the power traces that are on layer 3.

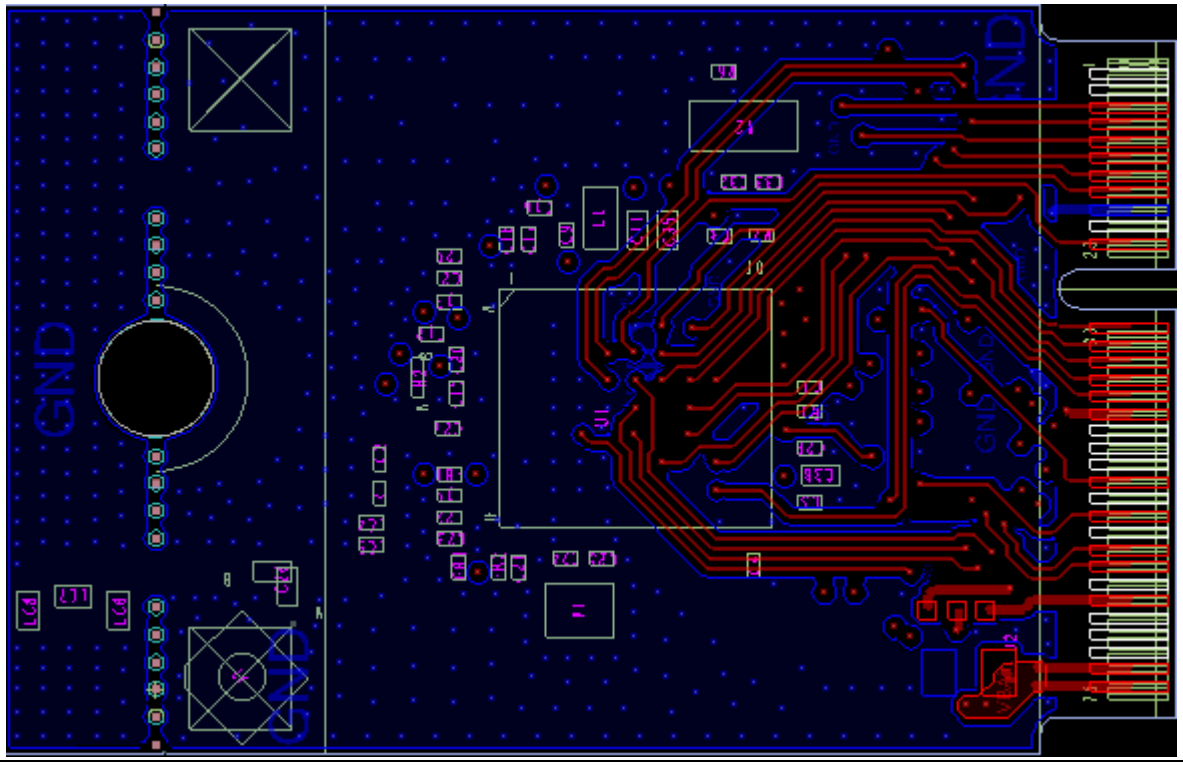


Figure 18 Layer 4, power traces and non-critical signals

4.6 Unavoidable power trace crossing on adjacent layers

If power traces crossing cannot be avoided, have them cross in a perpendicular manner to minimize the overlapping area of the power traces.

References

A wealth of data is available at www.infineon.com to help you to select the right device, and quickly and effectively integrate the device into your design.

[1] Datasheets

- 002-37795: CYW89829 AIROC™ Automotive Bluetooth® LE system, Ultra-low-power, Secure MCU

[2] Application note

- Antenna design and RF layout guidelines

Revision history

Document revision	Date	Description of changes
**	2023-05-19	Initial release.
*A	2023-07-14	Updated Figure 4, power inductor part number, and recommended trace width for power traces. Updated References: Added CYW89829 datasheet information. Added component specifications, BPF general insertion loss and attenuation specifications. Added Figure 6. Added Table title to all the tables in the document.

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