XMC7000: Setting the Clock Supervision (CSV) parameters

About this document

Scope and purpose

The Clock Supervision (CSV) feature in the XMC7000 family enables you to check the frequency of the monitored clock to ensure that it is within the allowed frequency window. To understand the functionality described and terminology used in this guide, see the “Clocking system” chapter in the architecture reference manual.

This guide describes how to calculate and set the CSV parameters using the CSV calculator.

Intended audience

This document is intended for anyone using the XMC7000 family to determine the CSV parameters.

Associated part family

XMC7000 family of XMC™ industrial microcontrollers

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1 Overview

Figure 1 shows the signal example of the CSV.

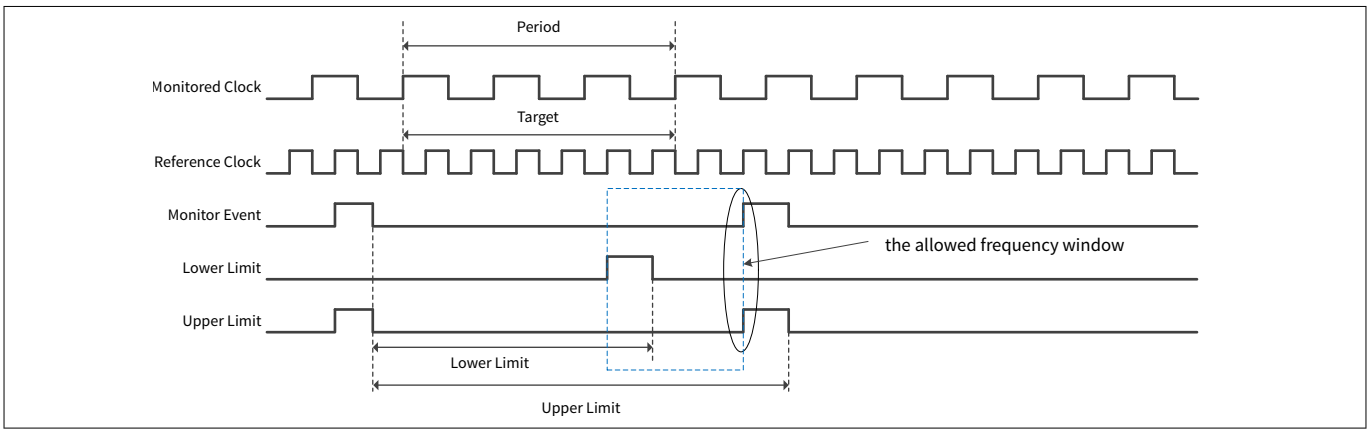


Figure 1 CSV operation signal example

The basic operation principle of the CSV circuit is as follows:

- Period is the monitored clock count while ‘target’ is the reference clock count. In an ideal case, the period value and the target value are same
- The monitored clock generates a monitor event (period), and the reference clock generates lower and upper limits
- The monitor event is compared against the lower and upper limits
- An error is reported if the monitor event ≤ Lower limit, or monitor event > upper limit

***Note**: The CLK_HF0 CSV must use the reset because the fault structure runs on CLK_HF0.*

2 Parameters related to CSV

2.1 Check the clock specifications

Check the following clock specifications:

- Reference clock frequency and tolerance (integer %)
- Monitored clock frequency and required tolerance (integer %). The required monitored clock tolerance should be equal to or larger than the reference clock tolerance
  - In case if the monitored clock is FLL, PLL200, or PLL400, set the nominal frequency (Fc) of configured VCO or PLL400 output for fractional mode, or SSCG in down spread mode to the monitor clock frequency. See SID341/SID341A(4)/SID341B(4)/SID351 in the device datasheet for the maximum frequency

    ***Note**: The maximum frequency is reduced in PLL400 with SSCG/fractional mode*

  - If the monitored clock is PLL200 or PLL400 without SSCG/fractional mode, set '3 or more' in consideration of the PLL jitter to monitored clock tolerance
  - If the monitored clock is PLL400 with SSCG/fractional mode, set '5 or more' in consideration of the PLL jitter to monitored clock tolerance as shown in Figure 2
  - If the monitored clock is PLL400 with SSCG mode, set the modulation depth according to your configuration

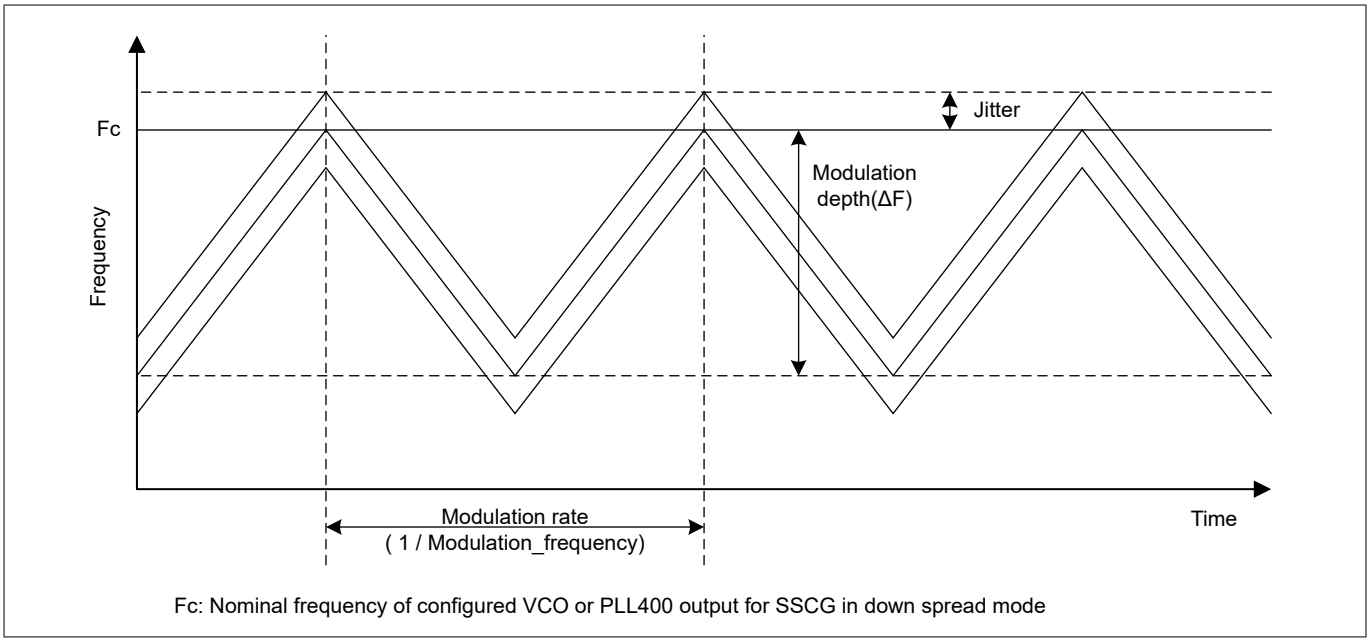


Figure 2 PLL clock frequency tolerance

- Maximum startup time for the monitored clock except for WCO. In the case of WCO, the startup time is unused (0). CSV should be enabled after WCO is started (BACKUP_STATUS.WCO_OK = 1)

In the CSV calculator, enter the values given in the column highlighted in grey in Table 1. If the monitored clock tolerance is smaller than the reference clock tolerance, the 'Value' cell of the monitored clock tolerance will be highlighted in red.

Table 1 Clock specification parameters

Parameters	Value	Unit	Remarks
Reference clock frequency	8000000	Hz	Nominal source clock frequency ILO: 32768 (SID320) IMO: 8000000 (SID310)
Reference clock tolerance	1	%	ILO: SID320 IMO: SID310
Monitored clock frequency	50000000	Hz	Nominal frequency, see SID341/SID341A(4)/ SID341B(4)/SID351 in the device datasheet
Monitored clock tolerance	3	%	≥ Reference clock tolerance (SID310/SID320) Minimum: 3 (when the Monitored clock is PLL200/400 without SSCG/fractional mode) Minimum: 5 (when the Monitored clock is PLL400 with SSCG/fractional mode)
Monitored clock tolerance (modulation depth)	0	%	Maximum: 3 (only for PLL400 with SSCG mode) 0 (others)
Maximum startup time for monitored clock	35	µs	ILO: 12 (SID321) IMO: 7.5 (SID311) PLL200: 35 (SID340) PLL400: 50 (SID340A) FLL: 5 (SID350) WCO: 0 (Unused)

2.2 Determine the target

Check the minimum target with (1) using the CSV calculator.

For example, for a tolerance of one percent, the target must be at least 200. Increasing the target increases the CSV accuracy; it also increases the latency.

$$Min \quad target = \frac{200}{Reference \quad clock \quad tolerance} \tag{1}$$

Determine and enter the target value shown in the cell highlighted in grey (Table 2) in the CSV calculator. The target should be greater or equal to the minimum target. If the target is smaller than the minimum target, the ‘Value’ cell of the target will be highlighted in red.

Table 2 Target parameters

Parameters	Value	Unit	Remarks
Minimum target (Calculated reference clock count)	200	Cycles	-
Target (Reference clock count for user definition)	200	Cycles	≥ Minimum target

2.3 Calculate the lower and upper limit

Calculate the lower limit with (2) using the CSV calculator.

$$Lower\quad limit = Period \times \frac{Reference\quad clock\quad frequency \times \left(1 - \frac{Reference\quad clock\quad tolerance}{100}\right)}{Monitored\quad clock\quad frequency \times \left(1 + \frac{Monitored\quad clock\quad tolerance}{100}\right)} \tag{2}$$

Calculate the Upper limit with (3) using the CSV calculator.

$$Upper\quad limit\quad = Period \times \frac{Reference\quad clock\quad frequency \times \left(1 + \frac{Reference\quad clock\quad tolerance}{100}\right)}{Monitored\quad clock\quad frequency \times \left(1 - \frac{Monitored\quad clock\quad tolerance}{100}\right)} \tag{3}$$

Only for PLL400 SSCG mode:

$$\begin{aligned}\text{Upper limit} &= \text{Period} \\ &\times \frac{\text{Reference clock frequency} \times \left(1 + \frac{\text{Reference clock tolernace}}{100}\right)}{\text{Monitored clock frequency} \times \left(1 - \frac{\text{Reference clock tolernace} + \text{Modulation depth}}{100}\right)}\end{aligned} \tag{4}$$

2.4 Calculate the period

Calculate the period with (5) using the CSV calculator. If the period value is less than one, increase the target value. To avoid the round-off error of the period value, the value should be as close to an integral value as possible and not a decimal value. This can be achieved by adjusting the target value.

$$Period\quad =\quad Target \times \left(\frac{Monitored\quad clock\quad frequency}{Reference\quad clock\quad frequency}\right) \tag{5}$$

2.5 Calculate the startup delay

Calculate the Startup Delay with (6) using the CSV calculator. In the case of WCO, the startup time is unused (0). CSV should be enabled after WCO is started (BACKUP_STATUS.WCO_OK = 1).

$$Startup\ \ Delay\ \ =\ \ Maximum\ \ startup\ \ time\ \ for\ \ monitored\ \ clock\ \ \times\ \ Refereence\ \ clock\ \ frequency \times\left(1+\frac{Reference\ \ clock\ \ tolerance}{100}\right) \tag{6}$$

2.6 Check the values for CSV register settings

The values should be obtained by subtracting 1 from the above-calculated values in the CSV register. The CSV calculator calculates these CSV register values based on the above parameters and automatically displays the values that are shown in Table 3, the column highlighted in grey. If the value is larger than 65535, the cell will be highlighted in red.

When determining the final CSV parameters, evaluate the CSV function sufficiently in the user system environment.

Table 3 Parameters for CSV registers

Parameters	Value	Unit	Remarks
Upper limit value for UPPER register	204	Cycles	Maximum: 255 (Only for CSV_ILO/LF/BAK) Maximum: 65535 (Others)
Lower limit value for LOWER register	195	Cycles	Maximum: 255 (Only for CSV_ILO/LF/BAK) Maximum: 65535 (Others)
Period value for PERIOD register	1249	Cycles	Minimum: 0 Maximum: 255 (Only for CSV_ILO/LF/BAK) Maximum: 65535 (Others)
Startup delay value for STARTUP register	282	Cycles	Maximum: 255 (Only for CSV_ILO/LF) Maximum: 65535 (Others)

3 CSV calculator examples

3.1 PLL200

An example of the PLL200 CSV calculator is demonstrated in this section with the following parameters:

- Reference clock frequency: 8 MHz (ECO)
- Reference clock tolerance: 1% (ECO)
- Target: 200 (use the same value as the calculated minimum target)
- Monitored clock frequency: 50 MHz (CSV_HF0/PLL200)
- Monitored clock tolerance: 3% (CSV_HF0/PLL200)
- Monitored clock tolerance (modulation depth): 0% (CSV_HF0/PLL200)
- Startup time for Monitored clock: 35 µs (PLL200)

In the CSV calculator, enter the values given in cells highlighted in grey in Table 4.

Table 4 Input parameters

Parameters	Value	Unit	Remarks
Reference clock frequency	8000000	Hz	Nominal source clock frequency ILO: 32768 (SID320) IMO: 8000000 (SID310)
Reference clock tolerance	1	%	ILO: SID320 IMO: SID310
Minimum target (calculated reference clock count)	200	Cycles	-
Target (reference clock count for user definition)	200	Cycles	≥ Minimum target
Monitored clock frequency	50000000	Hz	Nominal frequency
Monitored clock tolerance	3	%	≥ Reference clock tolerance (SID310/SID320) Minimum: 3 (when the monitored clock is PLL200/400 without SSCG/ fractional mode) Minimum: 5 (when the monitored clock is PLL400 with SSCG/ fractional mode)
Monitored clock tolerance (modulation depth)	0	%	Maximum: 3 (only for PLL400 with SSCG mode) 0 (others)
Maximum startup time for monitored clock	35	µs	ILO: 12 (SID321) IMO: 7.5 (SID311) PLL200: 35 (SID340) PLL400: 50 (SID340A) FLL: 5 (SID350) WCO: 0 (unused)

3 CSV calculator examples

The CSV calculator calculates the CSV register values based on the entered parameters and automatically displays the values shown in the column highlighted in grey in Table 5.

Table 5 Output parameters

Parameters	Value	Unit	Remarks
Upper limit value for UPPER register	208	Cycles	Maximum: 255 (only for CSV_ILO/LF/BAK) Maximum: 65535 (others)
Lower limit value for LOWER register	192	Cycles	Maximum: 255 (only for CSV_ILO/LF/BAK) Maximum: 65535 (others)
Period value for PERIOD register	1250	Cycles	Minimum: 0 Maximum: 255 (only for CSV_ILO/LF/BAK) Maximum: 65535 (Others)
Startup delay value for STARTUP register	283	Cycles	Maximum: 255 (only for CSV_ILO/LF) Maximum: 65535 (others)

3.2 PLL400 example

An example of the PLL400 CSV calculator is demonstrated in this section with the following parameters:

- Reference clock frequency: 8 MHz (ECO)
- Reference clock tolerance: 1% (ECO)
- Target: 400 (use twice the value of the calculated minimum target)
- Monitored clock frequency: 200 MHz (CSV_HF1/PLL400 with SSCG)
- Monitored clock tolerance: 5% (CSV_HF1/PLL400 with SSCG)
- Monitored clock tolerance (modulation depth): 3%
- Startup time for Monitored clock: 50 µs (PLL400)

In the CSV calculator, enter the values given in cells highlighted in grey in Table 6.

Table 6 Input parameters

Parameters	Value	Unit	Remarks
Reference clock frequency	8000000	Hz	Nominal source clock frequency ILO: 32768 (SID320) IMO: 8000000 (SID310)
Reference clock tolerance	1	%	ILO: SID320 IMO: SID310
Minimum target (calculated reference clock count)	200	Cycles	-
Target (reference clock count for user definition)	400	Cycles	≥ Minimum target
Monitored clock frequency	200000000	Hz	Nominal frequency

(table continues...)

Table 6 (continued) Input parameters

Parameters	Value	Unit	Remarks
Monitored clock tolerance	5	%	≥ Reference clock tolerance (SID310/SID320) Minimum: 3 (when the monitored clock is PLL200/400 without SSCG/fractional mode) Minimum: 5 (when the monitored clock is PLL400 with SSCG/ fractional mode)
Monitored clock tolerance (modulation depth)	3	%	Maximum: 3 (only for PLL400 SSCG mode) 0 (others)
Maximum startup time for monitored clock	50	µs	ILO: 12 (SID321) IMO: 7.5 (SID311) PLL200: 35 (SID340) PLL400: 50 (SID340A) FLL: 5 (SID350) WCO: 0 (unused)

The CSV calculator calculates the CSV register values based on the entered parameters and automatically displays the values shown in the column highlighted in grey in Table 7.

Table 7 Output parameters

Parameters	Value	Unit	Remarks
Upper limit value for UPPER register	439	Cycles	Maximum: 255 (only for CSV_ILO/LF/BAK) Maximum: 65535 (others)
Lower limit value for LOWER register	377	Cycles	Maximum: 255 (only for CSV_ILO/LF/BAK) Maximum: 65535 (Others)
Period value for PERIOD register	10000	Cycles	Minimum: 0 Maximum: 255 (only for CSV_ILO/LF/BAK) Maximum: 65535 (Others)
Startup delay value for STARTUP register	404	Cycles	Maximum: 255 (only for CSV_ILO/LF) Maximum: 65535 (others

3.3 FLL example

An example of the FLL CSV calculator is demonstrated in this section with the following parameters:

- Reference clock frequency: 8 MHz (IMO)
- Reference clock tolerance: 4% (IMO)

3 CSV calculator examples

- Target: 50 (use the same value as the calculated minimum target)
- Monitored clock frequency: 100 MHz (CSV_HF0/FLL)
- Monitored clock tolerance: 5% (Reference clock tolerance + SID352)
- Monitored clock tolerance (modulation depth): 0% (CSV_HF0/FLL)
- Startup time for Monitored clock: 5 µs (FLL)

In the CSV calculator, enter the values given in cells highlighted in grey in Table 8.

Table 8 Input parameters

Parameters	Value	Unit	Remarks
Reference clock frequency	8000000	Hz	Nominal source clock frequency ILO: 32768 (SID320) IMO: 8000000 (SID310)
Reference clock tolerance	4	%	ILO: SID320 IMO: SID310
Minimum target (calculated reference clock count)	50	Cycles	-
Target (reference clock count for user definition)	50	Cycles	≥ Minimum target
Monitored clock frequency	100000000	Hz	Nominal frequency
Monitored clock tolerance	4	%	≥ Reference clock tolerance (SID310/ SID320) Minimum: 3 (when the monitored clock is PLL200/400 without SSCG/ fractional mode) Minimum: 5 (when the monitored clock is PLL400 with SSCG/fractional mode)
Monitored clock tolerance (modulation depth)	0	%	Maximum: 3 (only for PLL400 SSCG mode) 0 (others)
Maximum startup time for monitored clock	5	µs	ILO: 12 (SID321) IMO: 7.5 (SID311) PLL200: 35 (SID340) PLL400: 50 (SID340A) FLL: 5 (SID350) WCO: 0 (unused)

The CSV calculator calculates the CSV register values based on the entered parameters and automatically displays the values shown in the column highlighted in grey in Table 9.

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Table 9 Output parameters

Parameters	Value	Unit	Remarks
Upper limit value for UPPER register	54	Cycles	Maximum: 255 (only for CSV_ILO/LF/BAK) Maximum: 65535 (others)
Lower limit value for LOWER register	46	Cycles	Maximum: 255 (only for CSV_ILO/LF/BAK) Maximum: 65535 (others)
Period value for PERIOD register	625	Cycles	Minimum: 0 Maximum: 255 (only for CSV_ILO/LF/BAK) Maximum: 65535 (Others)
Startup delay value for STARTUP register	42	Cycles	Maximum: 255 (only for CSV_ILO/LF) Maximum: 65535 (others)

References

Device datasheets

[1] Infineon Technologies: *XMC7100, XMC7000 microcontroller 32-bit Arm® Cortex®-M7*; Available online
[2] Infineon Technologies: *XMC7200, XMC7200D microcontroller 32-bit Arm® Cortex®-M7*;Available online

Device architecture reference manual

[3] Infineon Technologies: *XMC7000 MCU family architecture reference manual*; Available online

***Note**: Contact Technical support to obtain XMC7000 family references documents.*

Revision history

Document revision	Date	Description of changes
**	2021-12-06	Initial release.
*A	2023-06-05	• Updated the description in section 2.1 and 2.3. • Updated the remarks in Table 1 and Table 3. • Updated section 3. • Added the References section.
*B	2026-09-22	Migrated the document to prisma.

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