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Spec No: 001-33742

Spec Title: USER INTERFACE - ELECTROLUMINESCENT BACKLIGHT DISPLAY CONTROLLER WITH PSOC(R) - AN2244

Sunset Owner: Rajiv Vasanth Badiger (RJVB)

Replaced By: NONE

User Interface – Electroluminescent Backlight Display Controller with PSoC®

AN2244

Author: Steve Gerber
Associated Project: Yes
Associated Part Family: CY8C22xxx, CY8C24xxx, CY8C27xxx, CY8C29xxx
Software Version: PSoC® Designer™ 4.1
Associated Application Notes: None

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Application Note Abstract

Electro-Luminescent Backlight Displays (EL-Displays) are commonly used as the nighttime backlighting for vehicle instrument clusters. AN2244 details a useful microcontroller configuration of the EL-Backlight Reference Design. The reference design has been created in partnership between Rogers Corporation and Cypress MicroSystems. [Details of the DUREL® device and system level implementation are available in a separate Application Note within the reference design.]

Introduction

The basic configuration of the EL-Backlight Reference Design contains three primary components: The EL-Bulb, a driver, and a controller. The driver device is the Rogers-DUREL D306A EL lamp driver. This Application Note describes the functionality of the controller portion of the reference design.

The schematic included with the reference design package includes Integrated Circuit U2 (CY8C24143-24PI) as the controller mechanism for the EL-Backlight. This CY8C24143 PSoC® device contains configurable analog and digital resources, along with an 8-bit MCU, SRAM, 4KB of Flash, and a variety of additional features all in an 8-pin DIP package.

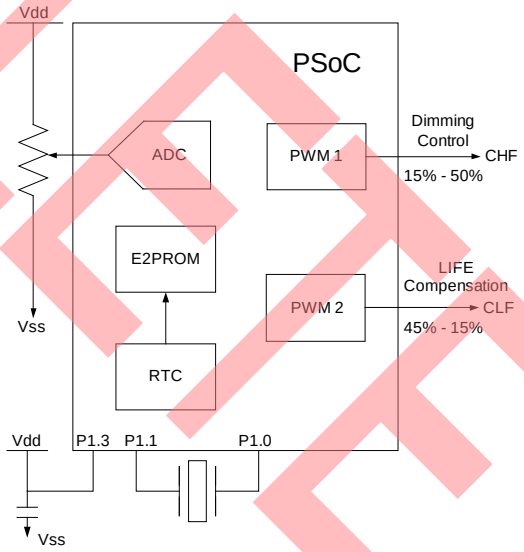
Implemented within the configurable resources of this device are the following functions:

- Dimming Control
- Life Compensation
- Elapsed Time Algorithm
- Data Storage in Flash
- Low Voltage Detection
- Watchdog Timer

PSoC Block Diagram

A Simplified block diagram is indicated in Figure 1. An ADC monitors a potentiometer voltage as an indication of the desired brightness by the user. This would be representative of a dashboard brightness control.

Figure 1. Simplified Block Diagram

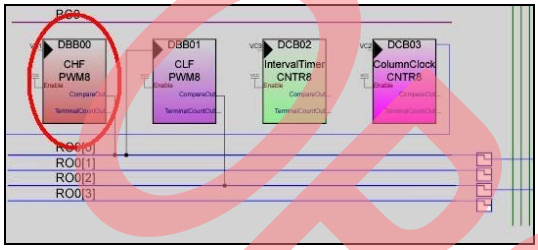


The Quartz Crystal and Real-time Clock (RTC) are used in the Life Compensation function. PWMs 1 and 2 are the controlled pulse-width modulation outputs directed to the DUREL D306A EL lamp driver. Not pictured in this simplified block diagram are the M8C CPU, SRAM, Internal Main Oscillator, etc.

Dimming Control

The Dimming Control output CHF of Figure 1 is a 54 kHz, 8-bit resolution PWM output that drives the DUREL D306A EL lamp driver at the CHF pin (9). The varying duty cycle of the PWM controls the device output power (the brightness of the EL-Lamp). This 8-bit hardware PWM in PSoC is set to vary from 15% to 50% duty cycle in this application.

Figure 2. Dimming Control PWM in PSoC

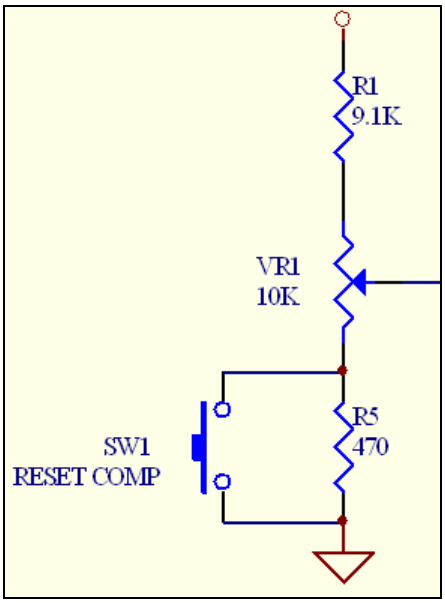


The actual configuration of the dimming control potentiometer is more complex than indicated in Figure 1. Figure 3 depicts the complete voltage divider circuit. The added resistors, R1 and R2, are the result of the FlashTemp User Module usage required for Flash writes. During Flash writes, the CPU measures the approximate die temperature in order to optimize the Flash writing process. The use of this FlashTemp module requires the use of the on-board Bandgap reference. Therefore, the Bandgap reference is to be utilized for the ADC measurement, as opposed to utilization of Vdd/2 +/- Vdd/2 as the ADC reference.

The subsequent use of the Bandgap reference with the ADC limits the valid input voltage range to the ADC. The available range is 0 to 2.6 V. High side and low side resistors are added to the 10 K potentiometer. This makes the lowest voltage 0.12 V and the highest 2.65 V. These resistor values may be modified, provided the same voltage range is maintained. A switch is also added for demonstration purposes. This switch is utilized during power-on to null the elapsed time counter.

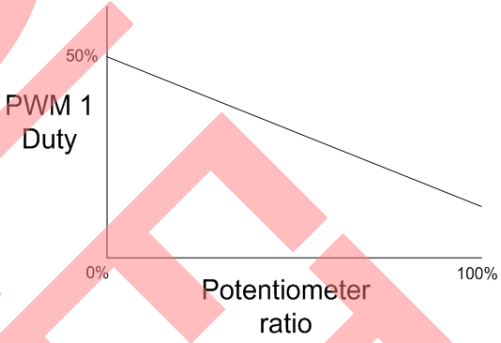
[At power-on, the input voltage is measured and checked. If it is less than 3 ADC counts, then the HundredHours variable is reset to 0 and the Flash is updated. So setting the brightness control to minimum and closing the switch before switching the power to the board ON, can reset the Life Compensation.]

Figure 3. Dimming Control Voltage Divider



The output duty cycle is inversely proportional to the potentiometer setting of 0 and 100% as shown in Figure 4.

Figure 4. PWM Output vs. Potentiometer Value



The transfer curve of Figure 4 reflects a linear relationship between the CHF PWM duty cycle and the potentiometer voltage. This linearity is implemented in firmware via a look-up table.

An equation implementation is an acceptable alternative; however, a look-up table approach avoids the use of general math libraries –reducing the final code size.

The potentiometer feeds an analog input pin, Port_0_3, of the PSoC device, through a mux and into ACB00, which is configured as a unity gain buffer (Figure 5). The output of the unity gain buffer is connected to the input of a Successive Approximation Register Analog-to-Digital Converter (SAR ADC) in block ASC10.

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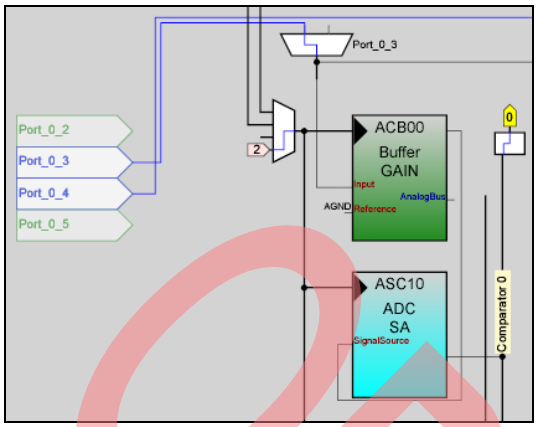
Figure 5. ADC Configuration in PSoC Designer



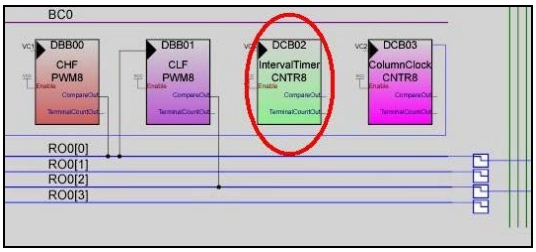
The result of the ADC is utilized to vary the output of the CHF output PWM. When the ADC measures 2.6V, the CHF PWM is set to 15% duty cycle, resulting in maximum brightness. The look-up table is listed in Code 1.

Code 1. CHF Dimming Control Look-up Table

```
TableCHF:
db 111, 110, 109, 107, 106, 105, 104, 102
db 101, 100, 99, 97, 96, 95, 94, 93
db 91, 90, 89, 88, 86, 85, 84, 83
db 81, 80, 79, 78, 76, 75, 74, 73
db 72, 70, 69, 68, 67, 65, 64, 63
db 62, 60, 59, 58, 57, 56, 54, 53
db 52, 51, 49, 48, 47, 46, 44, 43
db 42, 41, 39, 38, 37, 36, 35, 33
```

A counter named “IntervalTime” (pictured in Figure 6) provides the stimulus for the processor to perform the measurement of the potentiometer output and then update the PWMs. This stimulus is the counter’s interrupt, which has been configured to occur every 50 msec.

Figure 6. Flash Update Interval Timer in PSoC



Life Compensation

Electro-Luminescent lamps dim as they age. In most applications, it is important to maintain constant lamp brightness during the entire life of the product. The PSoC device implements a real-time clock to brighten the lamp over time. A PWM implements this brightening feature through control of the CLF input pin (10) of the DUREL D306A EL lamp driver.

The PWM that drives the CLF Life Compensation control is a 555 Hz, 8-bit PWM varying across a duty cycle of 36% to 15%. The variance is relative to the elapsed lifetime of the EL Display.

Figure 7. Life Compensation PWM in PSoC

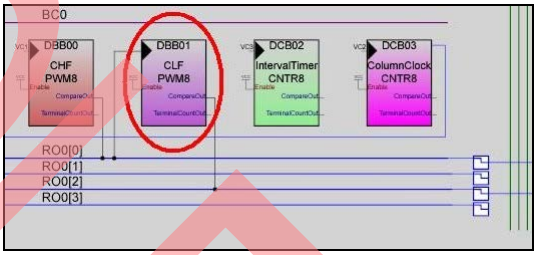


Figure 7 depicts the EL Life Compensation configuration described in this Application Note. Note that the CLF PWM duty cycle decreases over time to increase the drive level of the lamp. The actual Vrms will be higher due to the reduced (aged) EL lamp load.

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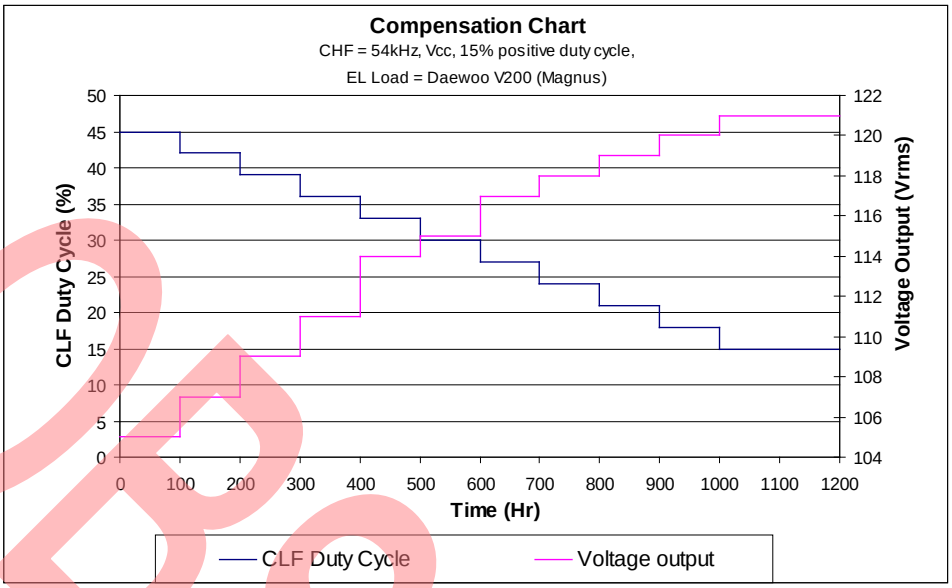
Figure 8. Life Compensation – CLF Duty Cycle and Output Voltage vs. Time



In order to implement this voltage change over time, an 8-bit PWM with maximum period of 255 is utilized. Column four of Table 1 below lists the necessary pulse width required to obtain the duty cycle shown in the last column. Again, for maximally efficient code, a look-up table technique is implemented using the pulse width and time values from columns four.

Additional values may be added to the table for a finer granularity of control.

Code 2. Life Compensation Look-up Table

```
TableCLF:
db 36, 34, 32, 30, 28, 26, 23, 21, 19, 17
```

Table 1. CLF PWM Characteristics Over Time

Time (Hours)	CLF PWM Duty Cycle Target (%)	D306 Voltage Output (Vrms)	Pulse Width (Assumes Period of 255)	CLF PWM Duty Cycle Actual (%)
0 ≤ 100	45	105	115	45.10
100 ≤ 200	42	107	108	42.35
200 ≤ 300	39	109	100	39.22
300 ≤ 400	36	111	92	36.08
400 ≤ 500	33	114	85	33.33
500 ≤ 600	30	115	77	30.30
600 ≤ 700	27	117	69	27.06
700 ≤ 800	24	118	61	23.92
800 ≤ 900	21	119	54	21.18
900 ≤ 1000	18	120	46	18.04
>1000	15	121	38	14.90

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Elapsed Time Algorithm

In order to maintain the constant brightness function of the Life Compensation, a high-accuracy clock is utilized to keep track of the approximate lamp life.

Figure 9 outlines the Elapsed Time implementation. This algorithm is designed to allow ~8,000 hours of elapsed EL Display usage, without violating the 50,000 erase/write lifetime specification of the Flash blocks at temperatures up to 85°C. For higher temperatures or longer elapsed time duration, see the **Application Variations** section of this Application Note.

The real-time clock is at the bottom of Figure 9. This clock is based upon a 32.768 kHz external quartz crystal connected to PSoC's Internal Low-speed Oscillator (ILO). At each 10-minute interval, the Flash is written in a fail-safe manner to keep track of total elapsed time.

The 10-minute interval is implemented via the Sleep Timer Interrupt Service Routine (ISR) with a software "seconds" counter. The Sleep Timer provides an interrupt every second.

When the "seconds" counter has decremented from 600 to 0, a 10-minute increment and validation signature is stored, first in RAM ("Ten minute counter" in the figure), then in two different Flash blocks ("Elapsed Time" and "Backup" in Figure 9). At this point, the Second Counter is reset to 599.

The main loop within the reference design code is very simple. With each loop, the Watchdog Timer is cleared. Subsequent to that, the code monitors the interval timer for the count down to 0. When the interval timer achieves 0 (every 50 msec), an update to the PWM values occurs. A constant checking of the temperature also occurs.

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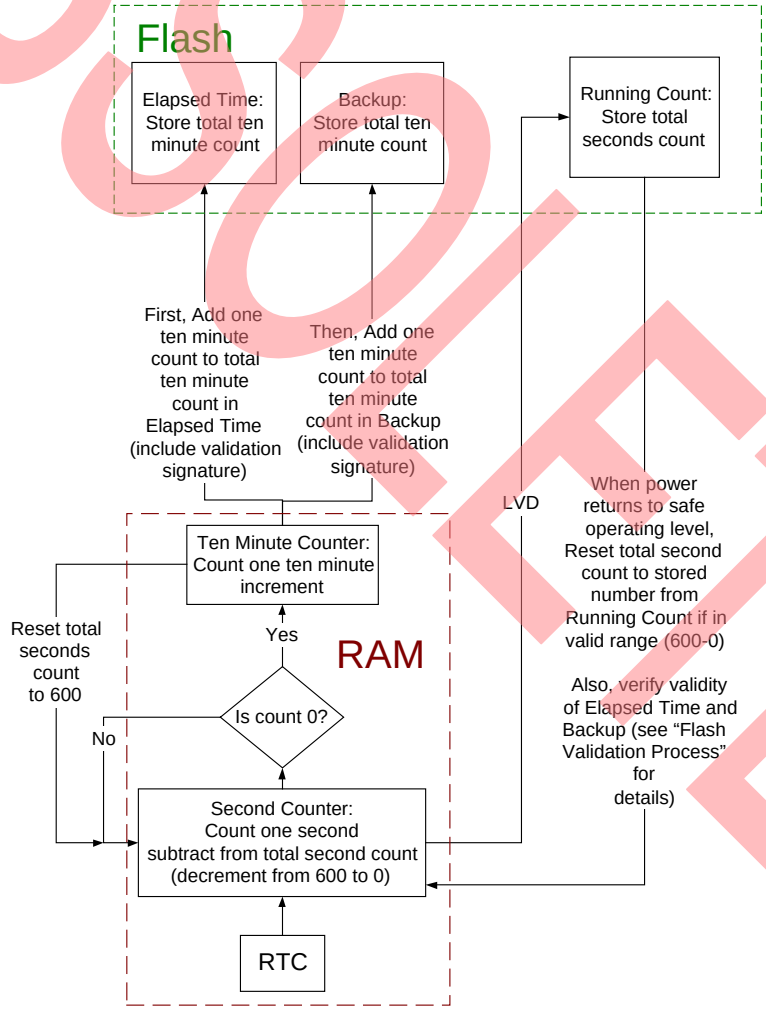
Figure 9. Elapsed Time Algorithm Flow Chart



[The comments have been removed from Code 3 for clarity.]

Code 3. MainLoop

```
; Infinite loop
MainLoop:
    M8C_ClearWDT
    tst [Flags],UPDATE_BRIGHTNESS
    jz MainLoop
    and [Flags],~UPDATE_BRIGHTNESS
    call UpdateBrightness
    call MeasureTemperature
    jmp MainLoop
```

Low Voltage Detection

When a Low Voltage Detection (LVD) occurs, an interrupt triggers the CPU to write the value in the Second Counter to a Flash block (Running Count). This safely stores the partial 10-minute increment while the system is turned off. When power returns to a safe operating level, the Second Counter will be restored to the value stored in Running Count. Also at this time, the Elapsed Time and Backup are verified for validity.

The system design must scale the Vdd bulk bypass capacitors to guarantee that the time between the LVD (~4.81 V) and the Power On Reset (POR) (~3.0 V) is greater than the Flash write time (~30 msec per block). The LVD value is adjustable in PSoC Designer. Figure 10 indicates that a 470-uF capacitor has been utilized as a bulk charge storage mechanism in this reference design. This capacitor value was chosen to provide 180 msec between LVD and POR. Only one block is being written to inside the LVD ISR, but in the worst-case scenario, three blocks may have to be written to – if the power fails at the moment the processor has entered the Sleep ISR then the LVD ISR will be serviced only after the Sleep ISR exits. Under this situation, three blocks will have to be written to upon LVD (the Elapsed Time and Backup blocks).

At ~30 msec per block, the 180 msec provides a 2x buffer for the required ~90 msec of necessary time between LVD and POR. This ensures that the algorithm will preserve the integrity of the Elapsed Time and Backup blocks even in the worst-case scenario.

This reference design utilizes a 12 MHz CPU speed, which is ideal, as it supports a low POR value and optimizes the power-down Flash write speed. The ISR routing is listed below in Code 4 (code comments are in green).

Code 4. LVD ISR

```
LVDISR:
    call StopResources
; Stop all resources and Switch off EL
; Store the Running Count to the E2PROM
    mov A,[Seconds+1]
    add A,[Seconds]
; Checksum = [Seconds+1] + [Seconds]
    cpl A
    add A,1
; 2's Complement of Checksum
    mov [Checksum1],A
; Update the Checksum for Second Counter
    mov [DataPointer],Seconds
; Point to Second Variable
    mov [DataCount],64
; 64 bytes to be written
    mov
[E2PromOffset],RUNNING_COUNT_BLOCK_OFFSET
; Set offset to Running Count Block of
E2PROM
    call WriteDataToE2Prom
; Write the Second Counter to E2PROM
; Wait till Vcc is good
    call TestForGoodVcc
; Loop till Vcc becomes good
    call LoadParameters
; Load the values from E2PROM
    call StartResources
; Start all the stopped resources
    reti
```

Note CPU speeds of >12 MHz require a CPU Clock throttle-back to 12 MHz for the power-down Flash write process. The designer should also be knowledgeable of the LVD and POR settings available in 105 °C and 125 °C PSoC devices.

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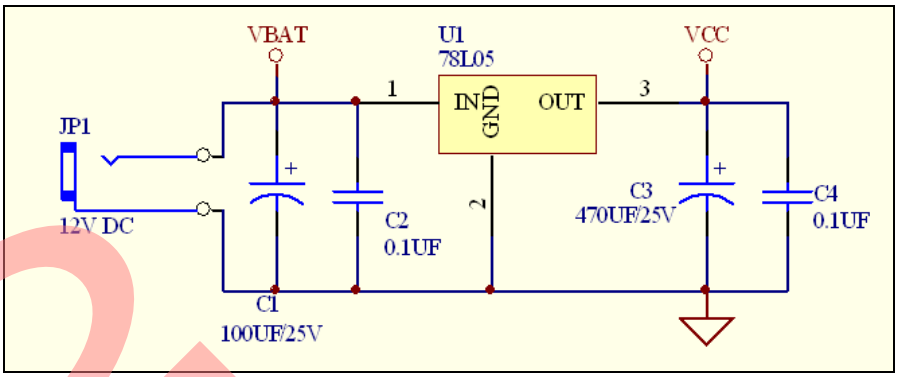
Figure 10. Power Supply Regulation and Bulk Capacitance Schematic



As demonstrated in the example code, it may be helpful to switch the ADC and PWMs off in order to reduce the charge consumption and increase the discharge time. This method allows the use of a lower value bulk capacitor.

Flash Validation Process

The Flash Validation process mentioned in the LVD description is comprised of four steps:

- Check validation signature in both the Elapsed Time block and Backup block.
- Compare Elapsed Time count value to Backup count value.
- If only one of the two blocks contains a validation signature, overwrite the invalid count value with the valid value from the other block.
- If both bocks are valid but have different count values, then overwrite the Backup block's value with the Elapsed Time block's value (because the Elapsed Time block was written first, it will contain the higher value, and therefore the most accurate value).

Application Variations

It is possible to extend the Elapsed Time Algorithm beyond ~8000 hours. This is accomplished by the use of rolling 64-byte blocks. A counter must be implemented to maintain compliance with the block-write count limit of the device. An alternative is to implement an interval of larger than 10 minutes.

Furthermore, it is possible to extend the lamp life with the addition of a voltage-monitoring algorithm. The lamp life degrades more slowly when the manual intensity setting remains low. In an instrument cluster, the driver rarely has the intensity set to maximum. Essentially, this enhancement would provide a Life-Voltage compensation; thereby further extending the life of the lamp.

In the event that a design requires 125 °C support, the number of Flash writes becomes limited. In this case, a low cost serial external Flash is suggested. An I2C block could be used to write to the serial Flash. Dynamic Re-configuration could also be used to temporarily replace a PWM block with an SPI block to write to the serial Flash during power-down.

For further cost reduction, it may be possible to implement this application with the CY8C21xxx device family.

A photo of the reference design appears in Figure 11.

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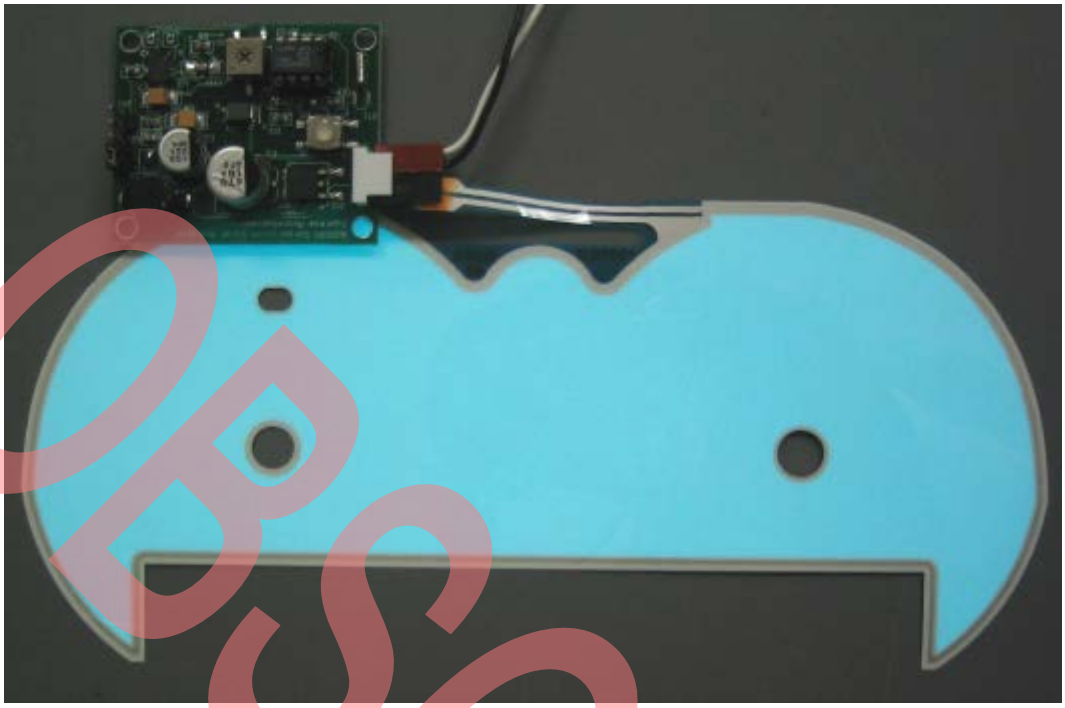
Figure 11. Reference Design with a Lotus Elise Lamp (Courtesy Rogers Corporation)



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Document History

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Document Number: 001-33742

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1499983	RJVB	09/24/2007	Re-catalogued application note.
*A	3196442	RJVB	03/15/2011	No change. Sunset review spec.
*B	4332327	RJVB	04/03/2014	Obsolete document. Completing Sunset Review.

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