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AN2224

PSoC® 1 - Lower Noise Continuous Time Signal Processing

Author: Dennis Seguine

Associated Project: No

Associated Part Family: CY8C24xxx, CY8C27xxx, CY8C28xxx, CY8C29xxx

Software Version: PSoC® Designer™ 5.1

Related Application Notes: "For a complete list of the application notes, click here."

AN2224 presents an introduction to semiconductor noise phenomena, specifics on PSoC® noise parameters and ways to optimize system design to minimize the effects of on-chip noise.

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1 Introduction

The PSoC®, Programmable System-on-Chip offers the opportunity to fit a wide array of signal processing techniques and topologies into a process primarily designed to accommodate flash memory for low cost microcontrollers.

The noise models discussed here are exactly that, models, based on testing of production devices and extensive simulations. Noise is a random process; certainly, deviations from the models due to process variations can be expected.

An understanding of CMOS noise basics and PSoC continuous time (CT) analog block and user module (UM) structures is essential to effective system design for noise. For a detailed understanding, read the entire Application Note. For quick noise numbers, use data from Table 2 and Table 3 and Equations 22 or 23. For design guidance, go straight to the section titled, Design Guidance.

2 PSoC Resources

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and quickly and effectively integrate the device into your design. In this document, PSoC refers to the PSoC 1 family of devices. To learn more about PSoC 1, refer to the application note AN75320 - *Getting Started with PSoC 1*.

The following is an abbreviated list for PSoC 1:

- **Overview:** PSoC Portfolio, PSoC Roadmap
- **Product Selectors:** PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP. In addition, PSoC Designer includes a device selection tool.
- **Datasheets:** Describe and provide electrical specifications for the PSoC 1 device family.
- **Application Notes and Code Examples:** Cover a broad range of topics, from basic to advanced level. Many of the application notes include code examples.
- **Technical Reference Manuals (TRM):** Provide detailed descriptions of the internal architecture of the PSoC 1 devices.
- **Development Kits:**
  - CY3215A-DK In-Circuit Emulation Lite Development Kit includes an in-circuit emulator (ICE). While the ICE-Cube is primarily used to debug PSoC 1 devices, it can also program PSoC 1 devices using ISSP.
  - CY3210-PSOCEVAL1 Kit enables you to evaluate and experiment Cypress's PSoC 1 programmable system-on-chip design methodology and architecture.
  - CY8CKIT-001 is a common development platform for all PSoC family devices.
- The MiniProg1 and MiniProg3 devices provide an interface for flash programming.

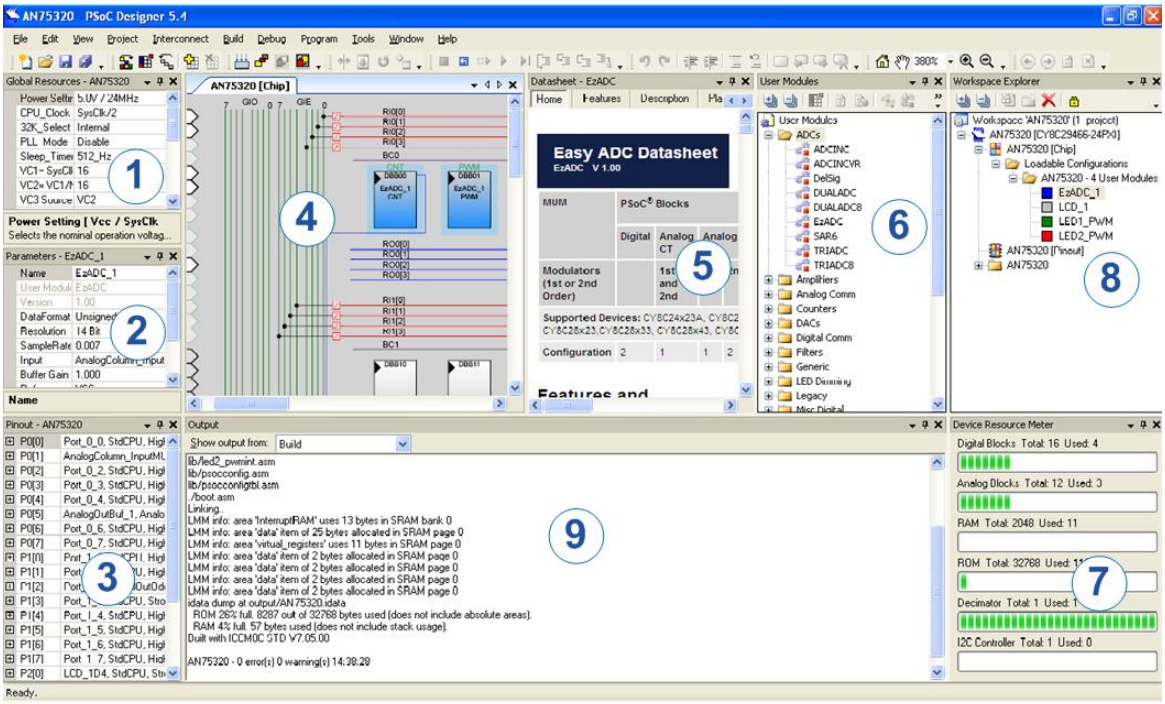
2.1 PSoC Designer

PSoC Designer is a free Windows-based Integrated Design Environment (IDE). Develop your applications using a library of pre-characterized analog and digital peripherals in a drag-and-drop design environment. Then, customize your design leveraging the dynamically generated API libraries of code. Figure 1 shows PSoC Designer windows. **Note:** This is not the default view.

1. **Global Resources –** all device hardware settings.
2. **Parameters –** the parameters of the currently selected User Modules.
3. **Pinout –** information related to device pins.
4. **Chip-Level Editor –** a diagram of the resources available on the selected chip.
5. **Datasheet –** the datasheet for the currently selected UM
6. **User Modules –** all available User Modules for the selected device.
7. **Device Resource Meter –** device resource usage for the current project configuration.
8. **Workspace –** a tree level diagram of files associated with the project.
9. **Output –** output from project build and debug operations.

Note: For detailed information on PSoC Designer, go to **PSoC® Designer > Help > Documentation > Designer Specific Documents > IDE User Guide**.

Figure 1. PSoC Designer Layout



2.2 Code Examples

The following webpage lists the PSoC Designer based Code Examples. These Code Examples can speed up your design process by starting you off with a complete design, instead of a blank page and also show how PSoC Designer User modules can be used for various applications.

http://www.cypress.com/go/PSoC1Code Examples

To access the Code Examples integrated with PSoC Designer, follow the path **Start Page > Design Catalog > Launch Example Browser** as shown in Figure 2.

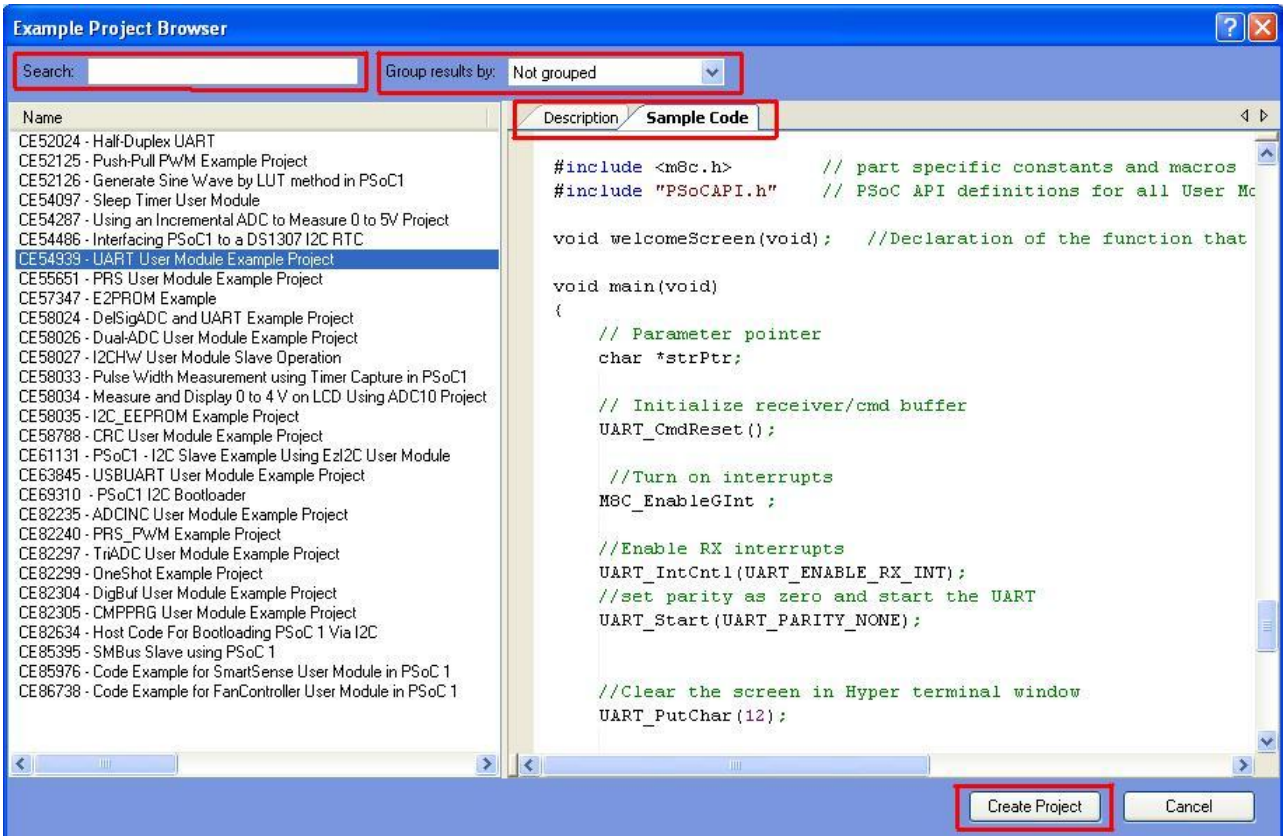
Figure 2. Code Examples in PSoC Designer



In the Example Projects Browser shown in Figure 3, you have the following options.

- Keyword search to filter the projects.
- Listing the projects based on Category.
- Review the datasheet for the selection (on the Description tab).
- Review the code example for the selection. You can copy and paste code from this window to your project, which can help speed up code development, or
- Create a new project (and a new workspace if needed) based on the selection. This can speed up your design process by starting you off with a complete, basic design. You can then adapt that design to your application.

Figure 3. Code Example Projects, with Sample Codes



2.3 Technical Support

If you have any questions, our technical support team is happy to assist you. You can create a support request on the Cypress Technical Support page.

You can also use the following support resources if you need quick assistance.

- Self-help
- Local Sales Office Locations

3 Noise Basics

Noise is a power phenomenon with independent noises summed across a bandwidth of interest. Adding two or more non-coherent noise sources together adds their power.

$$v_{n_{total}}^2 = v_{n_1}^2 + v_{n_2}^2 + v_{n_3}^2 + ... \quad \text{Equation 1}$$

The total noise is the sum of the power spectral density across the band of interest. Thus, in voltage terms, noise is:

$$v_n = n_0 \sqrt{Bandwidth} \quad \text{Equation 2}$$

where n_0, the noise voltage spectral density, is typically expressed in $nV/(Hz)^{1/2}$ or “nanovolts per root Hertz.” This applies to white noise, that is, when n_0 is constant over the whole band.

The noise sources are often independent of each other. To reduce the total noise, find and reduce the largest noise first.

Noise is a thermal and frequency related phenomenon, increasing with temperature and bandwidth. The noise of a simple resistor is:

$$v_n = \sqrt{4kTR\Delta f} \quad \text{Equation 3}$$

Where:

k is Boltzman's constant, $1.38e^{-23}$

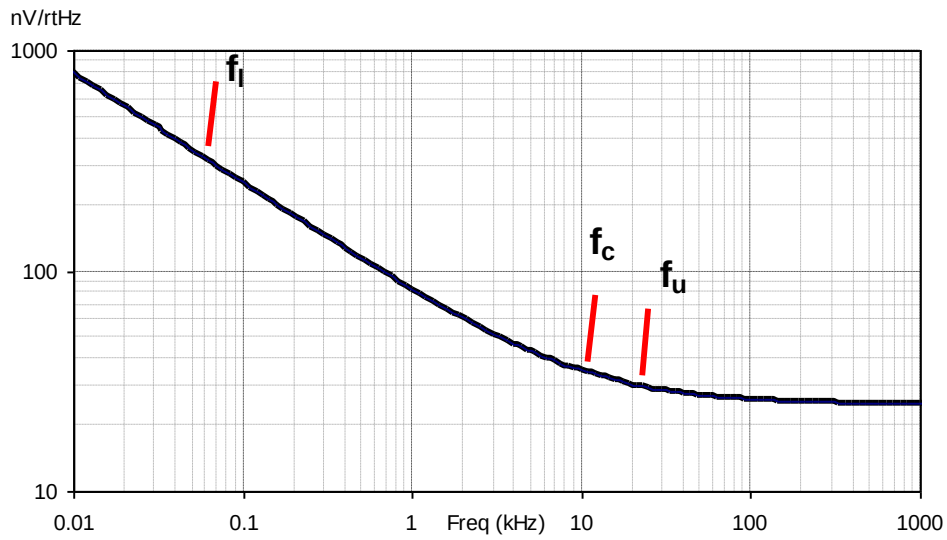
T is temperature in Kelvin

R is resistance in ohms

Δf is bandwidth in Hz

When the noise in a given band is not spectrally “flat,” the total noise must be determined from the shape of the noise over the bandwidth of interest. A typical noise curve is shown in Figure 4.

Figure 4. Generic Noise Curve



fl Lower frequency range, where the semiconductor noise power is generally inversely related to frequency, that is, proportional to 1/f

fu Upper frequency range, where semiconductor noise (and resistor noise) is generally constant and independent of frequency, also called flat-band noise

fc Corner frequency, where flat-band noise is equal to 1/f noise

The noise power follows the curve given by:

$$p_n(f) \propto 1 + \frac{fc}{f}$$ Equation 4

The noise is no longer a simple sum from the lower band-edge to the upper. Instead, we must integrate the noise over the band of interest.

$$v_{nt} = n_0 \left[\int_{fl}^{fu} n(f) df \right]^{\frac{1}{2}}$$ Equation 5

where n0 is the flat-band (upper frequency range) noise voltage spectral density.

$$v_{nt} = n_0 \left[\int_{fl}^{fu} (1 + \frac{f_c}{f}) df \right]^{\frac{1}{2}}$$ Equation 6

Integrating over the band we find:

$$v_{nt} = n_0 \left[f_u - f_l + f_c \ln\left(\frac{f_u}{f_l} \right) \right]^{\frac{1}{2}}$$ Equation 7

At frequencies below the 1/f corner frequency, the noise is clearly dominated by the 1/f term. For very low frequency systems, the input-referred noise voltage may be several orders of magnitude above a nominally specified level on a typical device datasheet. In most system analyses, the noise is referred to the input or the source of the signal. Later stage noises are reflected back to the input so that a signal-to-noise ratio (SNR) can be calculated and the system noise contributions can be evaluated in a common manner.

For example, in Figure 4 the flat-band noise is 25 nV/rtHz and the corner frequency is 10 kHz (this is not PSoC data, this is a model). The lower band-edge of this system design is 60 Hz; the upper band-edge is 20 kHz. If this was a flat noise system (not 1/f related), fc would be at zero frequency and the noise would simply be:

$$v_{nt} = n_0 (fu - fl)^{\frac{1}{2}}$$ Equation 8

$$v_{nt} = 25 * 10^{-9} (2 * 10^4 - 60)^{\frac{1}{2}}$$ Equation 9

$$v_{nt} = 3.53 \mu VRMS$$ Equation 10

This would seriously understate the noise level of the system. Plugging the same data into Equation 7 results in:

$$v_{nt} = 25 * 10^{-9} \left(2 * 10^{+4} - 60 + 10^4 \ln\left(\frac{2 * 10^4}{60} \right) \right)^{\frac{1}{2}}$$ Equation 11

$$v_{nt} = 6.98 \mu VRMS$$ Equation 12

This is nearly double the noise level from Equation 10, clearly demonstrating that the 1/f nature of semiconductor noise cannot be ignored.

4 CMOS Noise Basics

The input-referred noise of the MOSFET channel is a function of the channel resistance (a bulk effect) and the surface state noise (due to interactions between the silicon crystal structure and the adjacent non-conductive material (oxide, for example). MOS transistor thermal noise is given by:

$$v_{nT}^2 = \frac{8}{3}\frac{kT}{g_m}\Delta f \ , \qquad \text{Equation 13}$$

where transconductance, g_m, is:

$$g_m = \sqrt{\frac{2\mu_n C_{OX} W i_D}{L}} \ . \qquad \text{Equation 14}$$

The nature of “flicker” or 1/f noise is exceptionally well described in Gregorian and Temes:

“In an MOS transistor, extra electron energy states exist at the boundary between Si and SiO_2. These can trap and release electrons from the channel and hence introduce noise. Since the process is relatively slow, most of the noise energy will be at low frequencies. ... For devices fabricated with a ‘clean’ process, the gate-referred noise voltage is nearly independent and is given by the approximating formula”:

$$v_{nf}^2 = \frac{K}{C_{OX} W L}\frac{\Delta f}{f} \qquad \text{Equation 15}$$

C_{OX} and K are process dependent. The noise is inversely proportional to W and L, the width and length of the transistor's gate area. Thus, larger transistors have lower noise.

The total noise of the device is the sum of the thermal [Equation 13] and frequency dependent [Equation 15] noises. The noise at low frequency is dominated by the 1/f term, so the voltage noise is proportional to $1/(WL)^{1/2}$. The bandwidth of the MOSFET is determined by the capacitance of the device (area dependent) and its transconductance. Cutting the device noise in half requires quadrupling the device area. This, in turn, requires quadrupling the transconductance, which requires increasing the drain current by a factor of sixteen. Clearly, adjusting the devices and circuit designs to meet the low-noise requirements and operating current restrictions is a non-trivial effort.

5 PSoC Noise Sources

5.1 Thermal (Resistor) Noise

Resistor noise in the PSoC comes from two principal sources: the gain-setting resistance array in the CT block and the routing resistance of the signal paths.

For CY8C24/27/28/29xxx family devices, the unit resistor value in the gain-setting resistor network is 12.2 kΩ, for a noise spectral level of 14.2 nV/rtHz at room temperature. The highest gain-setting uses the lowest resistor value. The noise due to gain-setting resistors is significantly lower than the opamp and the ground reference noise.

The routing resistance, from P0[x] to the opamp input, is as much as 20 kΩ. The routing resistance from the CT block output to the analog buffer in each column is as much as 40 kΩ. The noise contribution of these resistances is still small compared to the opamp.

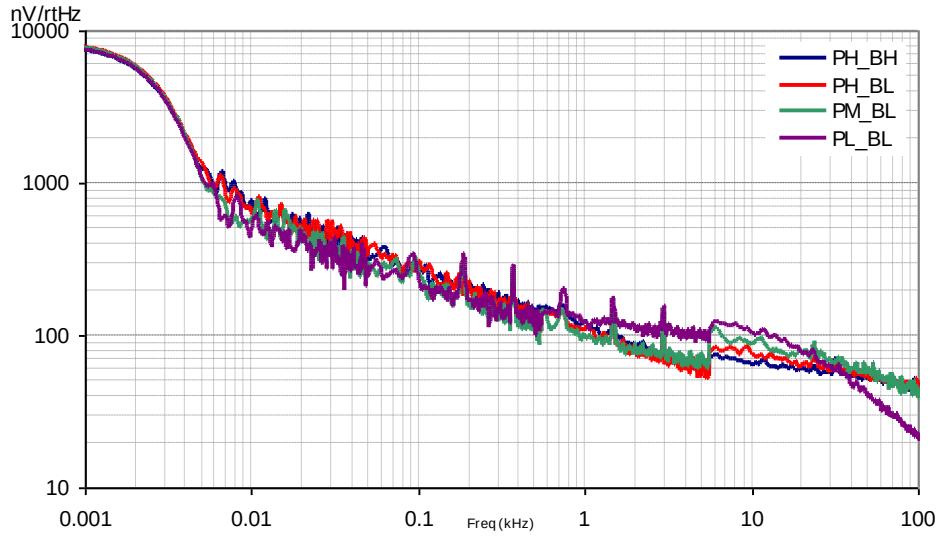
5.2 Opamp Noise

The basic analog structure of the PSoC CT user module (UM) functions is the opamp. The PSoC opamp was designed to optimize performance under conflicting constraints of noise, bandwidth, power consumption, die area, and the limitations of the Cypress SONOS IC fabrication process, which is adapted to efficient digital designs and flash memory requirements.

The opamp has an input noise, which is dominated at low frequency by 1/f, as in Equation 10. In this region, the noise level is very similar at all power levels. Above the 1/f corner frequency, the noise is determined by the thermal or flat-band noise. The noise corner frequency moves upward as the power and the bias levels are increased. This is because the flat-band noise drops with increasing power. There are six power levels in the PSoC. These are functions of power (Low, Med, High) and bias (Low, High). In each successive power level, the operating current is doubled. Increasing the power setting increases the transconductance and thus the noise spectrum level by the fourth root of the current increase. For example, increasing from Power = High, Bias = Low to Power = High, Bias = High reduces the noise level by a factor of 1/(2^(1/4) = 1/1.189).

The noise level roll-off at much higher frequencies (20 kHz at low power, low bias) is a function of finite opamp gain-bandwidth. The opamp noise for the CY8C24/27/28/29xxx families is shown for several power and bias settings in Figure 5. Given that most PSoC applications utilize ADCs and are at audio frequency and lower, noise below 10 kHz is most important.

Figure 5. Opamp Noise vs. Frequency



A few notes about the noise spectrum plots for the opamp, and later for the analog ground:

1. The “bump” in noise level below 10 Hz is an artifact of the finite minimum bandwidth (3.0 Hz) of the spectrum analyzer utilized to measure the noise. The actual noise follows the 1/f curve.
2. This data is tedious and time-consuming to gather over a wide frequency range and statistically significant number of samples.
3. Switching frequency/sensitivity ranges then compensating for them in post processing occasionally results in discontinuities in the noise curves. The “real” noise curve, when averaged over a large number of samples, is expected to be quite smooth.
4. Occasional external environmental noise spikes show up. This is particularly true in Figure 5, where the PL_BL (Power = Low, Bias = Low) curve has occasional 10 dB deviations from the average. These spikes are not in the PSoC but rather are an instrumentation artifact.

As with any noisy process, determination of the actual signal level is estimation. The data in Figure 5 were evaluated for each of the power and bias selections utilized. The opamp noise CY8C24/27/28/29xxx families is summarized in Table 2.

Table 1. Opamp Noise Summary

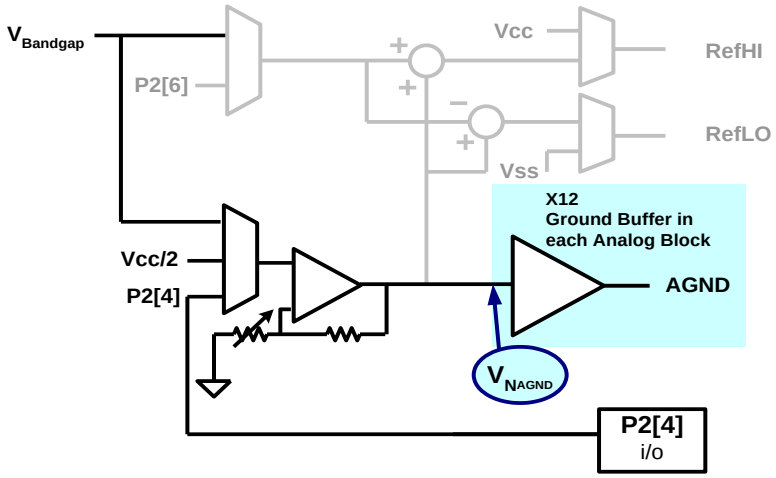
Power	Bias	n_0 (nV/rtHz)	fc kHz
High	High	55	4.5
High	Low	65	3.2
Med	Low	92	1.6
Low	Low	131	0.8

These values are plugged into Equation 7 to find the total opamp noise for a given application.

5.3 Ground Noise

With PSoC used in a single supply system, an artificial “ground” is established to provide a reference for bipolar or AC signals. This point is called analog ground (AGND) and is user selectable in the Global Resources window of PSoC Designer. See *AN2219 - PSoC® 1 Selecting Analog Ground and Reference* for a more detailed discussion of ground and reference structures. The basic analog ground structure is shown in Figure 6.

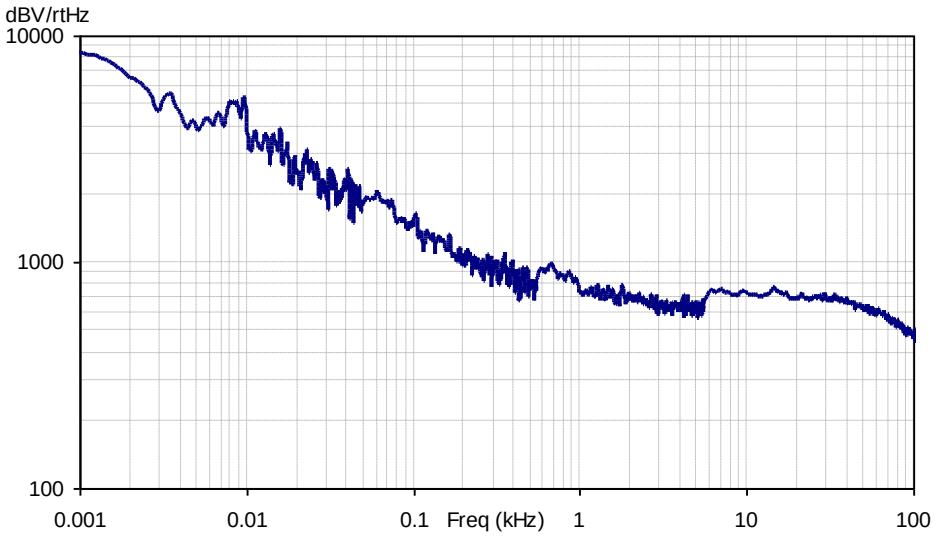
Figure 6. Basic Analog Ground Structure



The PSoC bandgap is intrinsically noisier than the PSoC opamp. The bandgap voltage is amplified in the reference generator. This, of course, multiplies the bandgap noise and adds the noise of the multiplying opamp. Thus, the noise of AGND = 2*Vbg is larger than the noise of AGND = 1.6*Vbg or AGND = Vbg. The noise curve for CY8C24/27/28/29xxx AGND = 2*Vbg is shown in Figure 7.

The noise of the bandgap circuit and the $V_{dd}/2$ reference generator is constant with the power level. That is, these circuits run at constant power, independent of the reference block power setting. The power setting of the opamps in the reference block is set in the Global Resources window of PSoC Designer. The power should be set equal to or higher than the power setting of the analog blocks.

Figure 7. CY8C24/27/28/29xxx AGND=2*Vbg Noise



The AGND noise level is summarized for CY8C24/27/28/29xxx in Table 2. The noise is determined by using the coefficients in Table 2 in calculations using Equation 7.

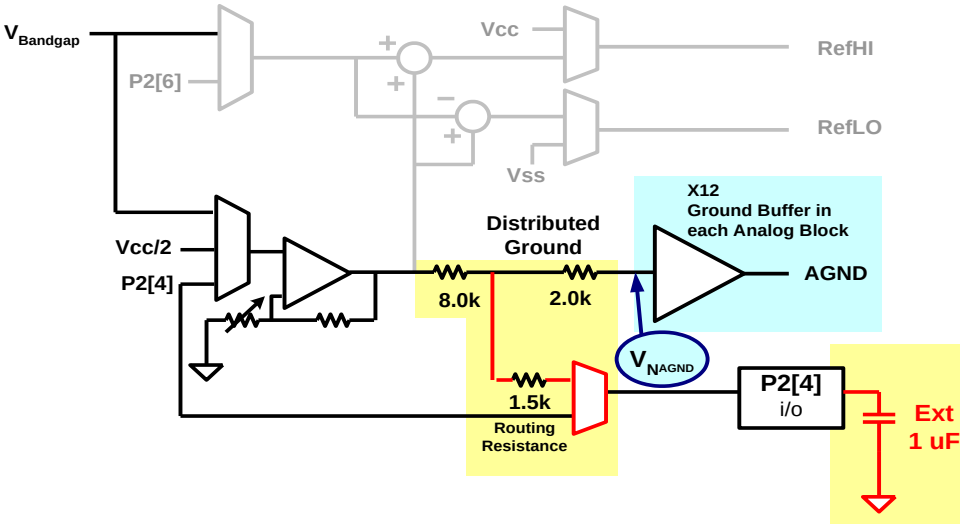
Table 2. AGND Noise Coefficients

	n_0 nV/rtHz	f_C kHz
$V_{dd}/2$	100	.5
Vbg	350	.5
P2[4]	12	0

The AGND on P2[4] is essentially noiseless (well, as noiseless a signal as the user cares to give). The small value listed in Table 2 accounts for the routing resistance from P2[4] to the input of the reference block ground buffer opamp.

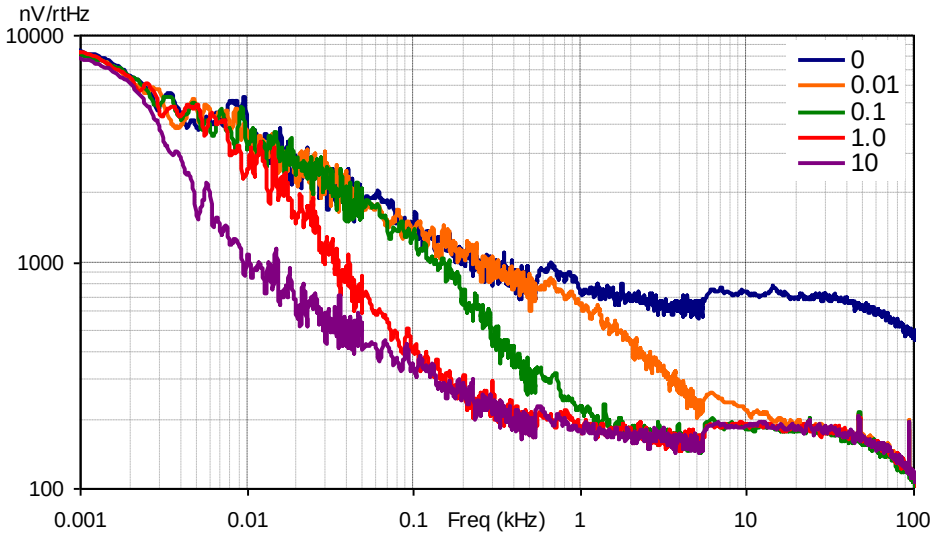
The CY8C24/27/28/29xxx series provides an additional means for reducing the ground noise: an external capacitor to bypass the internal distributed ground signal. P2[4] is routed to a resistive divider between the output of the ground reference generator and the distributed ground signal routed to each analog block, as shown in Figure 8.

Figure 8. CY8C24/27/28/29xxx Ground Structure



The maximum attenuation of the noise is determined by the ratio of the routing resistances. The 8.0 kΩ series resistance is set by stability considerations. The 1.5 kΩ resistance is set by minimum length routing considerations, multiplex switches, GPIO connections, and ESD protection resistors. The -3 dB point of the roll-off of the noise is determined by the 8.0 kΩ routing resistance and the external cap value on P2[4]. The analog ground noise for the case of AGND = 2.0*Vbg is shown for several capacitor values (in uF) in Figure 9.

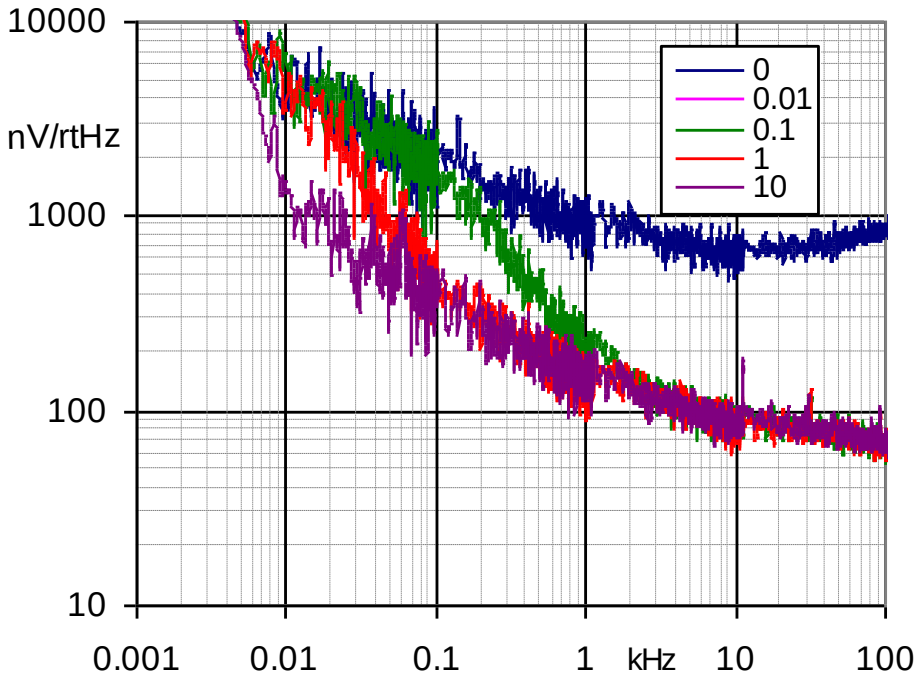
Figure 9. CY8C24/27/29xxx Ground Noise with Bypass



The AGND bypass works equally well for internal ground signals, $V_{dd}/2$ and Vbg-related. When the ground signal from P2[4] is used, the bypass connection is not available. The user should pick his ground reference (internal or external) with care considering biasing, noise, analog-to-digital converter (ADC) and digital-to-analog converter (DAC) range, and consumption of GPIO resources.

CY8C28xxx has a lower routing resistance from the output of the internal AGND buffer to P2[4]. This result in a significant reduction of the noise presented to the AGND buffers in each of the continuous time and switched capacitor blocks. The bypassed noise level is 6 dB lower in CY8C28xxx compared to CY8C24/27/29xxx.

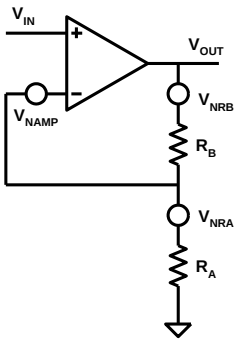
Figure 10. CY8C28xxx Ground Noise with Bypass



6 PGA Noise Models

In its simplest form, the programmable gain amplifier (PGA) is an opamp and two resistors, each of which is a noise source, as shown in Figure 11.

Figure 11. PGA Noise Model



This topology works at high gains only when the input is very close to V_{SS}. The maximum allowed DC or (DC+ peak AC) input is V_{dd}, divided .by the gain.

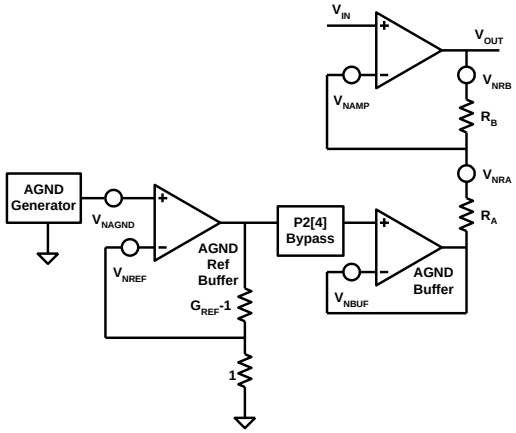
In CY8C24/27/28/29xxx family devices, R_{Base} (the unit resistor in the gain-setting resistor network) is approximately 12.2 kΩ. R_A is set to 1, 2, 3, 6 ... up to 48 (in steps of 3 units up to 16 * 3). R_B is 48*R_{Base}-R_A. This allows gains of 48, 24, 16, 8 . . . . to 1.

Deriving the gain equation using Ohms law, and so on, for the V_{SS}-referenced PGA, the noise is:

$$V_{NPGA} = \left[\begin{array}{l} \left(v_{NAMP} \frac{R_B + R_A}{R_A} \right)^2 \\ + \left(V_{NRA} \frac{R_B}{R_A} \right)^2 + V_{NRB}^2 \end{array} \right]^{\frac{1}{2}}$$ Equation 16

Common PSoC applications use PGAs with gain referenced to AGND as shown in Figure 12. Thus, the AGND noise becomes a part of the noise equation, Equation 17.

Figure 12. Full PGA Noise Model Block Diagram



$$V_{NPGA}^2 = \left[\begin{array}{l} \left(v_{NAMP} \frac{R_B + R_A}{R_A} \right)^2 + \left(v_{NAGND} G_{REF} G_{BYP} \frac{R_B}{R_A} \right)^2 \\ + \left(v_{NBUF} \frac{R_B}{R_A} \right)^2 + \left(v_{NREF} G_{REF} G_{BYP} \frac{R_B}{R_A} \right) \\ + \left(v_{NRA} \frac{R_B}{R_A} \right)^2 + V_{NRB}^2 \end{array} \right]$$ Equation 17

The noise in the AGND generator is amplified by the ground reference amplifier. When the AGND reference buffer gain is unity, that is when AGND = $V_{dd}/2$ or AGND = Vbg, the noise of the AGND source is not amplified. In this case, the noise of the AGND reference buffer is simply additive. When the gain is larger than one, the noise of the AGND reference buffer opamp is multiplied along with the noise of the AGND generator. Clearly the lowest noise will occur when the gain on the AGND generator is amplified by the minimum amount. In all cases, the noise of the internal AGND reference generator is larger than the noise of the AGND reference buffer.

Let us try a few examples. Common for all is a PGA gain = 16 and an audio bandwidth 200 Hz to 4.0 kHz.

Where P2[4] bypass is used, the cap value is 1.0 uF; this is large enough that the AGND noise attenuation is flat across the band of interest.

6.1 Example 1

Table 3. Example 1 Values

Part Family	CY8C27xxx
Power	Low
Bias	Low
AGND	2*Vbandgap*
Bypass	Not used

*Topology from Figure 11

At this power and bias level, the opamp noise level is calculated to be 11.1 uV_{RMS} and the bandgap noise level to be 27.2 uV_{RMS}. From Equation 17:

$$V_{NPGA}^{2} = \left[\begin{array}{l} \left(11.1uV\frac{45*12k+3*12k}{3*12k}\right)^2+\left(27.2uV*2.0*1.0\frac{45*12k}{3*12k}\right)^2 \\ +\left(11.1uV\frac{45*12k}{3*12k}\right)^2+\left(11.1uV2.0*1.0\frac{45*12k}{3*12k}\right) \\ +\left(1.5uV\frac{45*12k}{3*12k}\right)^2+(6.0uV)^2 \end{array} \right] \quad \text{Equation 18}$$

Adjusting for gain, the input noise referred to input (RTI) is:

$$V_{NPGA(RTI)} = 57.2uVRMS \quad \text{Equation 19}$$

6.2 Example 2

Table 4. Example 3 Values

Part Family	CY8C27xxx
Power	Med
Bias	Low
AGND	V_{dd}/2*
Bypass	Not used

*Topology from Figure 11

At this power and bias level, the opamp noise level is calculated to be 9.6 uV_{RMS} and the V_{dd}/2 noise level to be 7.8 uV_{RMS}. From Equation 17:

$$V_{NPGA}^{2} = \left[\begin{array}{l} \left(9.6uV\frac{45*12k+3*12k}{3*12k}\right)^2+\left(7.8uV*1.0*1.0\frac{45*12k}{3*12k}\right)^2 \\ +\left(9.6uV\frac{45*12k}{3*12k}\right)^2+\left(9.6uV*1.0*1.0\frac{45*12k}{3*12k}\right) \\ +\left(1.5uV\frac{45*12k}{3*12k}\right)^2+(6.0uV)^2 \end{array} \right] \quad \text{Equation 20}$$

Adjusting for gain, the input noise is:

$$V_{NPGA(RTI)} = 17.5uVRMS \quad \text{Equation 21}$$

6.3 Example 3

Table 5. Example 3 Values

Part Family	CY8C27xxx
Power	High
Bias	Low
AGND	1.6*Vbandgap*
Bypass	1.0 uF on P2[4]

*Topology from Figure 11

At this power and bias level, the opamp noise level is calculated to be 8.6 uV_{RMS} and the bandgap noise level 27.2 uV_{RMS}. From Equation 17:

$$V_{NPGA}^{2} = \begin{bmatrix} \left(8.6uV\frac{45*12k+3*12k}{3*12k}\right)^2 + \left(27.2uV*1.6*0.2\frac{45*12k}{3*12k}\right)^2 \\ +\left(8.6uV\frac{45*12k}{3*12k}\right)^2 + \left(8.6uV*1.6*0.2\frac{45*12k}{3*12k}\right) \\ +\left(1.5uV\frac{45*12k}{3*12k}\right)^2 + (6.0uV)^2 \end{bmatrix} \quad \text{Equation 22}$$

Adjusting for gain, the input noise is:

$$V_{NPGA(RTI)} = 14.3uVRMS \quad \text{Equation 23}$$

6.4 Example 4

Table 6. Example 4 Values

Part Family	CY8C27xxx
Power	High
Bias	High
AGND	Not used, PGA referenced to V_{SS}
Bypass	Not used

*Topology from Figure 10

At this power and bias level, the opamp noise level is calculated to be 8.3 uVRMS. The analog ground noise is, of course, zero. From Equation 16:

$$V_{NPGA}^{2} = \begin{bmatrix} \left(8.3uV\frac{45*12k+3*12k}{3*12k}\right)^2 \\ +\left(1.5uV\frac{45*12k}{3*12k}\right)^2 + (6.0uV)^2 \end{bmatrix}^{\frac{1}{2}} \quad \text{Equation 24}$$

Adjusting for gain, the input noise is:

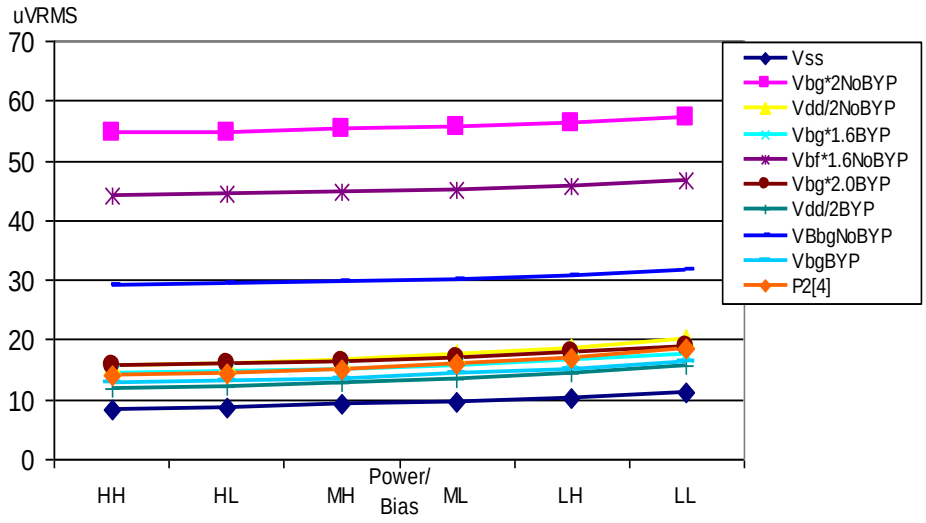
$$V_{NPGA(RTI)} = 8.6uVRMS \quad \text{Equation 25}$$

Note that the PGA noise (RTI) level is only slightly higher than the opamp input noise.

7 Evaluating Noise

The noise can be evaluated for this frequency range in Example 4 for all bias levels and all possible AGND selections; for this case, 60 Hz to 4.0 kHz. The noise RTI is shown in Figure 13.

Figure 13. PGA Noise vs. Reference and Power



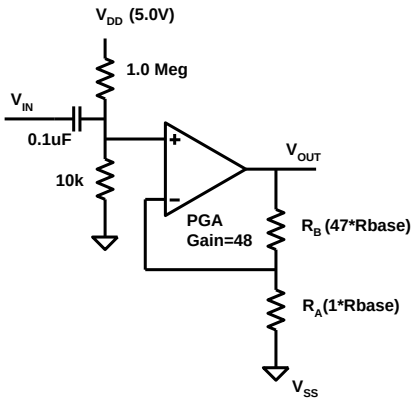
It could be expected that referencing AGND to P2[4] with a potentially zero noise source could result in very low ground noise. This is actually not the case since the P2[4] signal is routed through the AGND buffer in the reference block, through the 8.0 kΩ + 2.0 kΩ routing channel then the AGND buffer in the CT block. Thus, the ground has two more buffers (and noise sources) in the circuit than the V_{SS} referenced AGND.

Since the AGND input and the bypass connection on P2[4] share the pin, both functions are not available at the same time. It is not possible to provide an external AGND on P2[4] AND bypass this signal to reduce the effects of reference block AGND buffer noise.

Question: After all this detail, what is the lowest noise CT PGA pre-amplifier for processing audio or low frequency AC signals…?

Answer (as shown in the examples): The one with the fewest noise-adding components. Avoid AGND and set the gain relative to V_{SS}. This is done by using a resistive divider from V_{dd} to set the bias point, as shown in Figure 14. Alternatively, connect the bias network to an external reference, or a buffered AGND out on P0[2,3,4, or 5].

Figure 14. Lowest Noise CT PGA Pre-amplifier

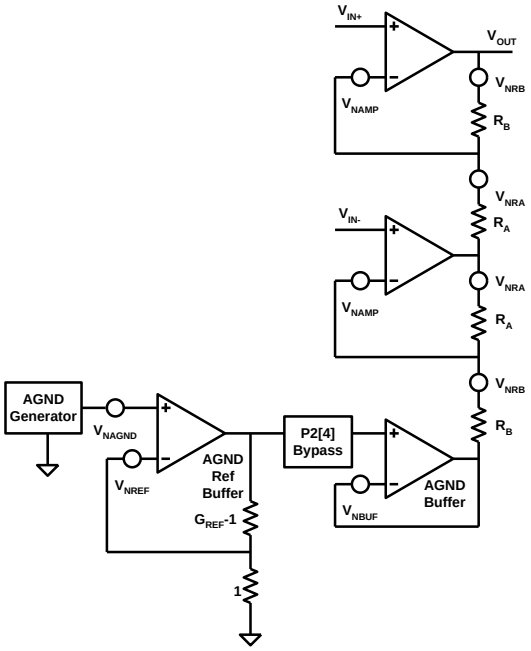


Splitting the 1.0 MΩ resistors and adding a bypass capacitor will reduce the noise from the power supply. The output may not be precisely set at AGND. This should not be a problem for an AC signal, simply add a high-pass filter. This can be done in hardware, coupling the PGA output through an analog column buffer to a capacitor then to an AGND referenced input. If digitized, the signal can be processed by a simple IIR high pass filter, as demonstrated in Application Note *AN2099, PSoC® 1, PSoC 3, and PSoC 5 - Single-Pole Infinite Impulse Response (IIR) Filters.*

7.1 INSAMP Noise Models

The two opamp version of the instrumentation amplifier, INSAMP, is actually two PGAs connected with complementing gains. The non-inverting input section has a gain of $(R_B+R_A)/R_A$; the inverting input section has a gain of $(R_B+R_A)/R_A$. The noise model of the INSAMP is shown in Figure 15.

Figure 15. INSAMP Noise Model



There are some noise advantages to this topology, compared to the PGA. The gain on the AGND signal at the output of the inverting stage is $-R_A/R_B$. This is amplified by the non-inverting stage gain of $-R_B/R_A$. Thus, the AGND noise gain is unity. This is much lower than the Gain-1 amplification of the AGND noise in the PGA.

Deriving the noise voltage for this topology, we find:

$$V_{NPGA}^{2} = \begin{bmatrix} \left(v_{NAMPNI}\frac{R_B+R_A}{R_A}\right)^2 + \left(v_{NAGND}G_{REF}G_{BYP}\right)^2 \\ +\left(v_{NAMPI}\frac{R_B+R_A}{R_A}\right)^2 + \left(v_{NREF}G_{REF}G_{BYP}\right) \\ +2*\left(v_{NRA}\frac{R_B}{R_A}\right)^2 + 2*V_{NRB}^2 \end{bmatrix} \quad \text{Equation 26}$$

8 System Noise Requirements

How low does the noise need to be? Most PSoC systems digitize data. There is, after all, a microcontroller connected to the analog array. The RMS quantization noise of any ADC is 0.288, that is $1/(12)^{1/2}$, times the voltage resolution. An 11-bit converter (delta-sigma type, typical of continuous signals) working on a 1.3 Volt (bandgap) reference has resolution of 1.27 mV/bit. The quantization noise is 0.288 times this value or 365 uV_{RMS}. The PGA can have an input noise as low as 8.6 uV_{RMS} (calculated in Equation 25), so the PGA can have a gain of up to 42 and still have its noise level lower than the quantization noise level of the ADC.

8.1 Design Guidance

So, that was more than you wanted to know about noise; you just wanted the quietest possible system. What are the simple rules to low the noise of the PSoC system design?

1. Run analog user modules and reference at the highest possible power to reduce opamp noise. This reduces the noise spectral level but increases bandwidth.

2. When referencing to internal AGND (not P2[4]), enable AGND bypass on P2[4] in the PSoC Designer Global Resources window and select the bypass capacitor suitable for frequency range of interest. 1.0 uF is sufficiently large for audio signals.
3. For signal processing on audio signals, or where absolute voltage reference of analog ground tied to Vbandgap is not necessary, set AGND = $V_{dd}/2$.
4. For PGAs on V_{SS} referenced signals, set PGA gain using V_{SS} as reference. Signals must always be positive.
5. For AC signals where a large amount of gain is required, bias the input above ground, at a value such that the sum of the bias voltage and the largest negative peak signal are still above V_{SS}.
6. When digitizing the data, average the results of several conversions if bandwidth considerations allow. This reduces the noise by the square root of the number of samples averaged.
7. Use correlated double sampling (CDS) techniques to reduce the effects of input voltage offset and 1/f noise. This is done by alternating measurements between the selected input and a quiet reference then filtering the difference, as described in Application Note *AN2226 - PSoC® 1 - Using Correlated Double Sampling to Reduce Offset, Drift, and Low Frequency Noise*.

9 Summary

The flexibility of the PSoC, Programmable System-on-Chip allows the designer to trade-off of power and noise, enabling solutions for a wide range of signal-level processing problems.

10 References

1. Analog MOS Integrated Circuits for Signal Processing, Roubik Gregorian, Gabor C. Temes, Wiley-Interscience, 1986.

11 Related Application Notes

- AN2099 - PSoC® 1, PSoC 3, and PSoC 5 - Single-Pole Infinite Impulse Response (IIR) Filters
- AN2219 - PSoC® 1 Selecting Analog Ground and Reference
- AN2226 - PSoC® 1 - Using Correlated Double Sampling to Reduce Offset, Drift, and Low Frequency Noise

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1499983	SEG	10/04/2007	New Application Note
*A	3173691	SEG	02/23/2011	Update title, deleted CY8C25/26xxx, add CY8C28xxx.
*B	3180198	SEG	02/23/2011	Document title updated
*C	3430192	SEG	11/04/2011	Corrected equation, clarified text. Updated template.
*D	4356722	SEG	04/22/2014	Updated links in Worldwide Sales and Design Support at the end of the document. No content update.
*E	4771627	DIMA	05/20/2015	Updated template Added PSoC Resources section Sunset review

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