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AN2199

Analog - DAC with Analog Modulator

Author: M. Ganesh Raaja

Associated Project: Yes

Associated Part Family: CY8C22xxx, CY8C24xxx, CY8C27xxx, CY8C29xxx

Software Version: PSoC® Designer™ 5.4

Related Application Notes: None

AN2199 explains the construction of a high resolution DAC using a 16-bit PWM, a switched capacitor block, and the analog modulator function.

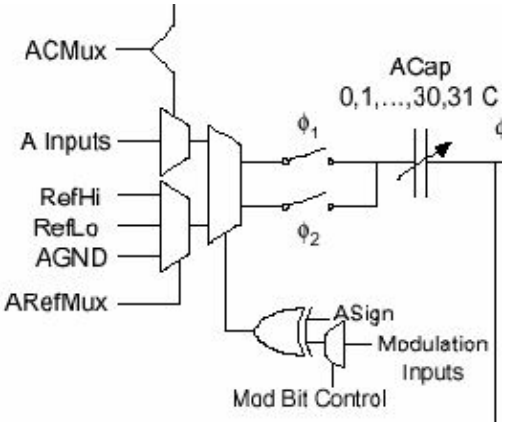
Introduction

PSoC® Designer already has DAC6, DAC8 and DAC9 User Modules. Any resolution beyond this is not possible using the existing topology. This Application Note discusses a method of using a 16-bit PWM, an SCBLOCK, and the analog modulator function to construct a higher resolution DAC. The example project has a 12-bit DAC incorporated. Theoretically, a 16 bit DAC can be designed using this technique. But the repeatability and effect of noise have to be studied for such high resolutions.

Analog Modulator

Figure 1 shows the modulation control section of a Type C Switched Capacitor block.

Figure 1. Modulation Control of a Switched Capacitor



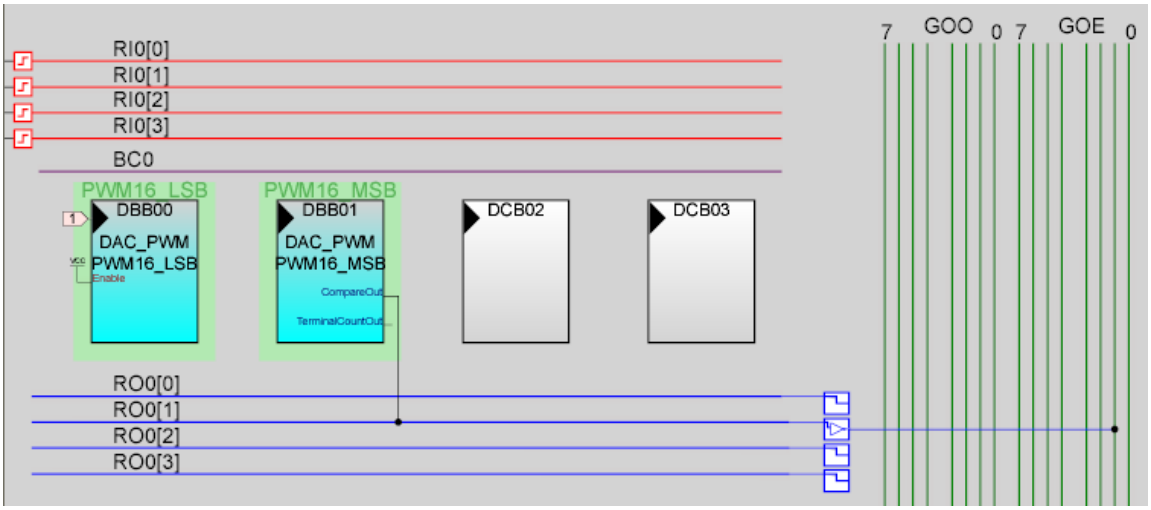
Type C Switched Capacitor blocks in ASC10, ASC21, ASC12, and ASC23 all have the function of analog modulation. There are eight possible signals that can be used to modulate the analog signal. These include the analog comparator bus outputs, two global outputs, and a digital block broadcast bus. The selection is done by modifying the bits in the AMD_CR0 and AMD_CR1 registers. The modulation signal is XOR'ed with the Sign bit of the switched capacitor block to determine the sign of the output.

Configuration

The user module placement and parameters are shown in Figure 2, Figure 3 and Figure 4.

A PWM16 User Module is placed. The output of the PWM16 is routed to the ROW_0 Broadcast Bus and the Global_Out_Even1 Bus after inversion using the LUT. The clock of the PWM is selected as SysClk direct. The period of the PWM is set to 4095. So the output frequency of the PWM is 5.86 kHz. The AMD_CRx register is updated to select the ROW_0 Broadcast line as the Analog Modulator. By varying the pulse width, the output voltage of the SCBLOCK can be controlled. As the PWM output level changes between 0 and 1, the output of the SCBLOCK switches between REFLO (Gain of -1) and REFHI (Gain of +1). A simple RC filter at the output of the SCBLOCK smoothes the modulated output to a stable DC voltage.

Figure 2. Digital Block Placement



The SCBLOCK User Module is placed in one of the type C blocks.

ACMux is selected as REFHI. ASign is Positive. FCap and ACap are set to 16 to set the gain to 1.

Figure 3. Analog Block Placement

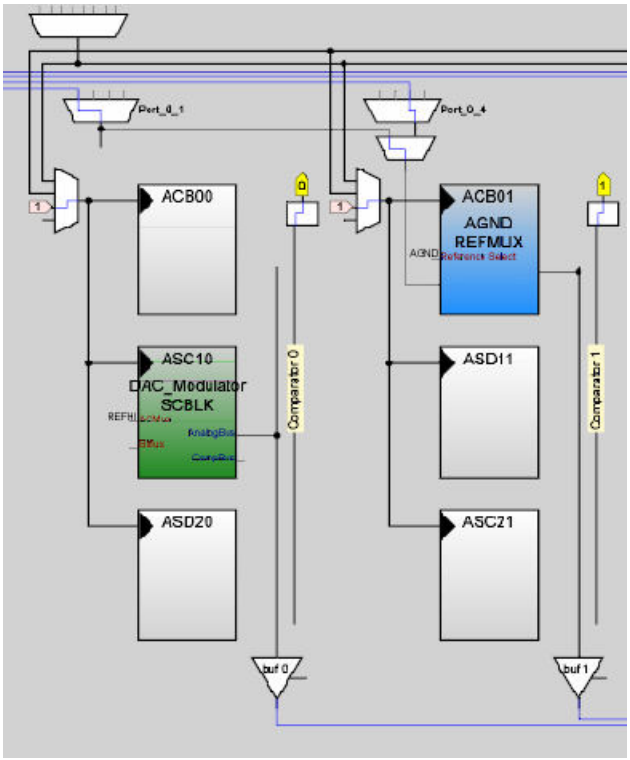


Figure 4. SCBLOCK Parameters

DAC_Modulator

User Module Parameters	
FCap	16
ClockPhase	Norm
ASign	Pos
ACap	16
ACMux	REFHI
BCap	0
AnalogBus	AnalogOutBus_0
CompBus	Disable
AutoZero	On
CCap	0
ARefMux	AGND
FSW1	On
FSW0	On
BMux	?
Power	High

The Program

Apart from the starting of the user modules, there is no CPU overhead involved. To update the DAC output, just change the pulse width value of the DAC_PWM User Module.

```
void main(void)
{

    // Start the Modulating PWM
    DAC_PWM_Start();

    // Start the SC Block
    DAC_Modulator_Start
    (DAC_Modulator_HIGHPOWER);

    // Turn On Analog Modulator and
    // select Global_Out_Even_1 bus
    // as modulator source
   AMD_CR0 = 0x01;

    // Start the AGND RefMux
    AGND_Start(AGND_HIGHPOWER);


    // Duty cycle as 25%
    iPulseWidth = 1024;


    // Update the Pulsewidth to change
    // the DAC output
    DAC_PWM_WritePulseWidth(iPulseWidth);


   while(1)
    {
        ;
    }
}
```

Effect of Offset and Gain and its Solution

Naturally, there will be error on the DAC output due to the offset and gain error of the SCBLOCK. This can easily be overcome by using offset and gain correction methods. One such method is explained in detail in Application Note AN2117 – Analog – DAC11. This involves calculating the DAC value for 0.00V output (offset zero) and the DAC value for another known output, say 1.000V (full scale). From the difference of full scale and span, the counts/volt calibration constant can be calculated. To get any other voltage, multiply the desired output with the counts/volt constant, add the offset zero, and update the PWM with this value to get the exact desired output.

Higher Resolutions

Higher resolutions can be achieved by changing the period of the PWM. By changing the period to 16384, you can construct a 14-bit DAC. But the output frequency of the PWM will now be 1.46KHz and the RC constant used to filter the output should be higher. To keep the output frequency high, the input of the PWM can be selected as SysClk*2.

Theoretically, with a 16-bit PWM, you can go up to a 16-bit DAC. But repeatability and noise issues should be studied.

Other Applications

Apart from using this setup as a DAC, you can also create an MDAC with a higher resolution. For this, the ACMux input should be routed to the external signal to be multiplied, instead of REFHI.

Summary

The rich set of analog switched capacitor blocks of PSoC 1 enables wide variety of options to implement a particular function. One such function was demonstrated in this application note to implement a 12-bit DAC using the modulation control of a switched capacitor block.

About the Author

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Document History

Document Title: Analog - DAC with Analog Modulator - AN2199

Document Number: 001-34561

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1505943	JVY	09/26/2007	Re-catalogued application note.
*A	3211722	PMAD / GRAA	03/31/2011	Upgraded and tested the project to PSoC Designer 5.1 SP1
*B	4339865	RJVB	04/10/2014	Updated to new template. Completing Sunset Review.
*C	4622198	ASRI	01/13/2015	Updated Software Version as “PSoC® Designer™ 5.4”. Updated attached associated project to PSoC Designer 5.4.

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