AN214962

Printed Circuit Board Layout Guidelines and Component Selection for Optimized PMU Performance

Associated Part Family: CYW4330/CYW4336/CYW43362

This Application Note covers the CYW4330/CYW43362 PMU section (i.e., CBUCK, LDO3P3/3P1, CLDO, LNLDO).

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1 About This Document

1.1 Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM4330	CYW4330
BCM43362	CYW43362

1.2 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use. For a more complete list of acronyms and other terms used in Cypress documents, go to: http://www.cypress.com/glossary.

2 Introduction

This Application Note covers the CYW4330/CYW4336/CYW43362 PMU section (i.e., CBUCK, LDO3P3/3P1, CLDO, LNLDO) and makes the following recommendations:

- Correct placement of components to facilitate optimal board routing and chip performance.
- Proper routing to components to account for noise coupling/EMI, current-flow capability, and PMU performance.
- Understanding the trade-offs in PMU component selection (e.g., different footprints/ratings) and the implications for overall PMU functionality and performance.

Reference boards from two different packages are used as board design examples in this document to demonstrate the best PMU section board layout practices: CYW43362 WLBGA and BCM94330CSPSDAGBB (CYW4330 WLCSP).

3 Board Layout Design Guidelines

3.1 CYW43362 WLBGA

3.1.1 Correct PMU Component Placement

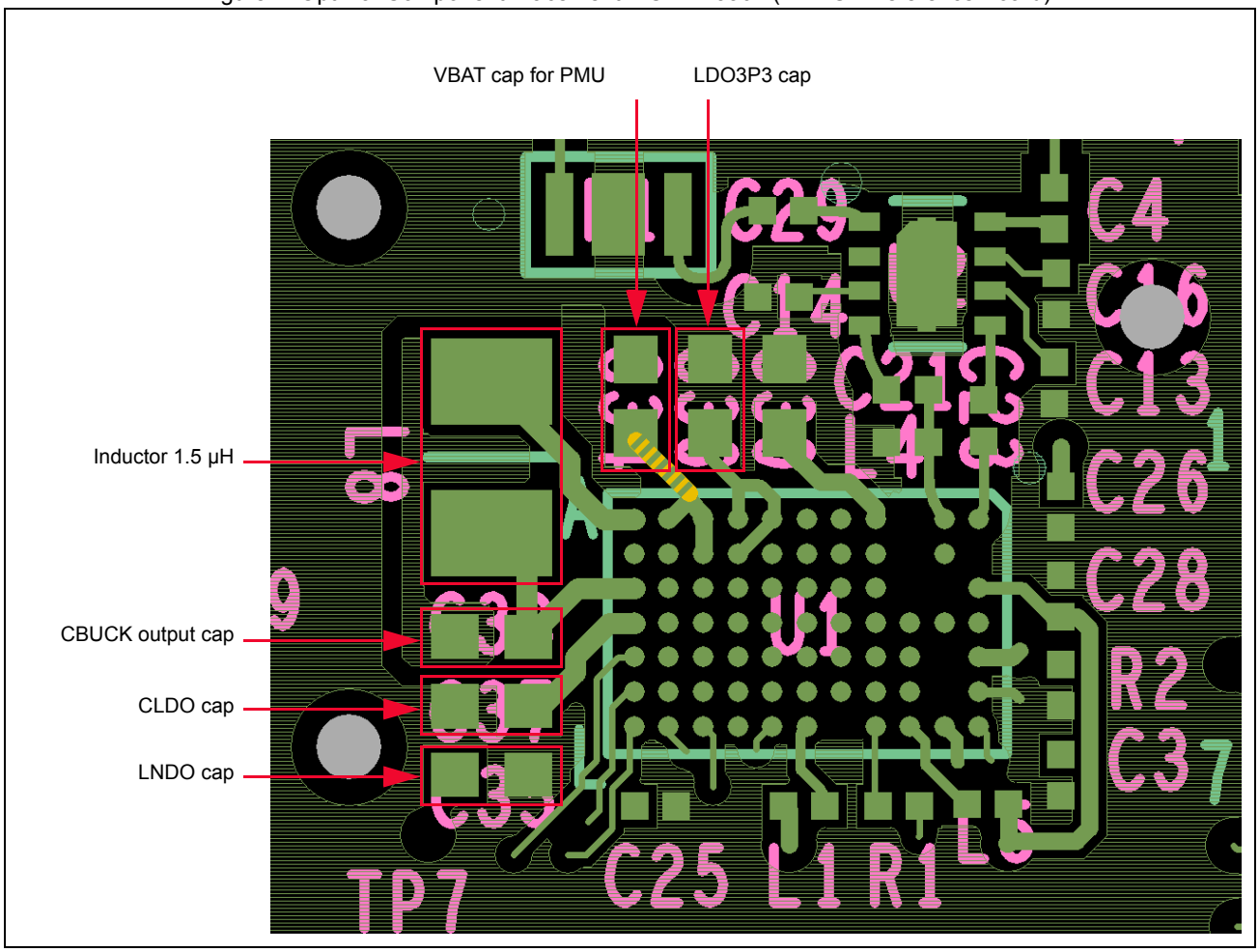
The PMU pins are arranged in a compact way, so that when components are placed close to their respective regulator pins, the board routing can be done easily without causing interference to other parts of the chip.

Figure 1 on page 2 shows an example of optimal component placement to their respective regulator pins.

The highlighted components are:

- L8 = 0806 size SR_VLX pin driving CBUCK inductor
- C34 = 0402 size VBAT shared cap for SR_VDDBAT1 & SR_VDDBAT2 pins
- C38 = 0402 size CBUCK output cap
- C37 = 0402 size VOUT_CLDO cap
- C35 = 0402 size VOUT_LNLDO cap
- C36 = 0402 size VOUT_3P3 cap

Figure 1. Optimal Component Placement—CYW43362 (WLBGA Reference Board)



Note: Refer to the full recommended BOM list for PMU components.

Based on the CYW43362 WLBGA Cypress reference board, the red boxes in Figure 1 outline all the critical PMU-related components. By placing these components close to their connecting pins, routing can be achieved with minimal length, as shown in Figure 1.

3.1.2 PMU Board Routing Considerations

Figure 2 on page 3 shows the routing using the top layer (i.e., the same layer as the footprints for components and CYW43362 WLBGA/CYW4330 WLSCP chip placement). Use of vias and routing layers other than the top layer is strongly discouraged for the following reasons:

- Microvias have lower current carrying capability.
  - The VLX signal and inductor must carry up to 500 mA DC with a ripple of 800 mA pk-pk.
  - The VBAT supply line must carry up to 600 mA of combined average current for CBUCK and LDO3P3.
  - LDO3P3 sources a maximum of 80 mA, CLDO max 150 mA, LNLDO1 max 150 mA (300 mA for the CYW4330).
- Microvias have high parasitic resistance and inductance. Any extra parasitic will add to power losses and higher switching noise spikes, causing interference.
- Using microvias and lower layers increases the CBUCK switching current loop area, which is directly proportional to the radiated EMI (see Figure 3 on page 4).

In Figure 2, all routings are the shortest and widest possible to minimize parasitic resistance and inductance. Regulators are sensitive to routing parasitics, which can cause instability, power efficiency losses, and in extreme cases may cause the regulator to lose voltage regulation. Extreme parasitics caused by long skinny traces can also lead to large switching voltage spikes ,which can lead to long-term chip reliability problems.

Figure 2. Mandatory PMU Component Routing – Length/Width Rules (WLBGA Reference Board)

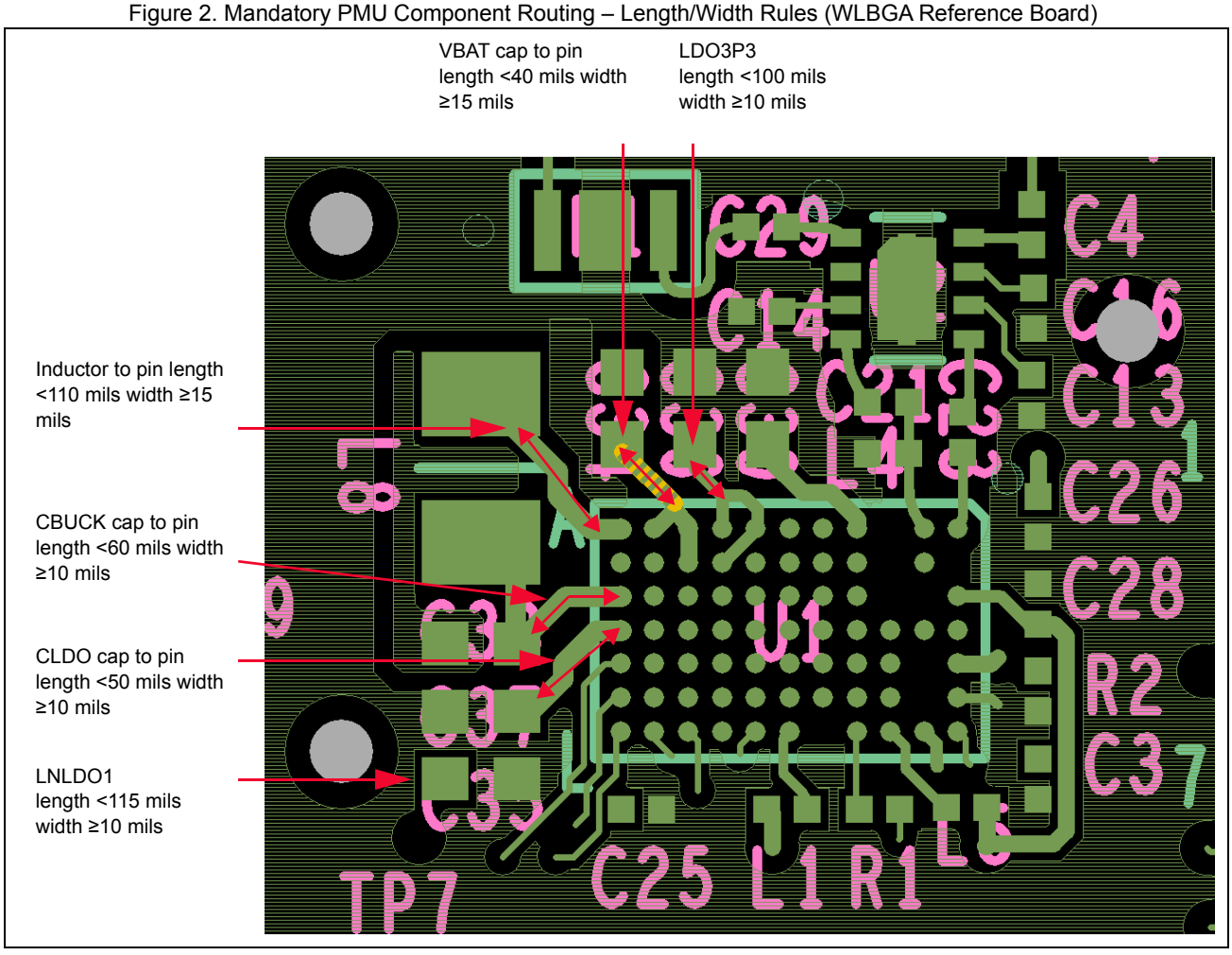


Figure 3 shows two current loops through the power MOSFETs of CBUCK. Each loop starts from a cap and ends at its ground terminal. The radiated EMI is proportional to the area within each loop. Routing of sensitive signals through the areas bounded by these two loops should be strictly avoided.

Figure 3. EMI Loops in Buck Switching Regulator (WLBGA Reference Board)

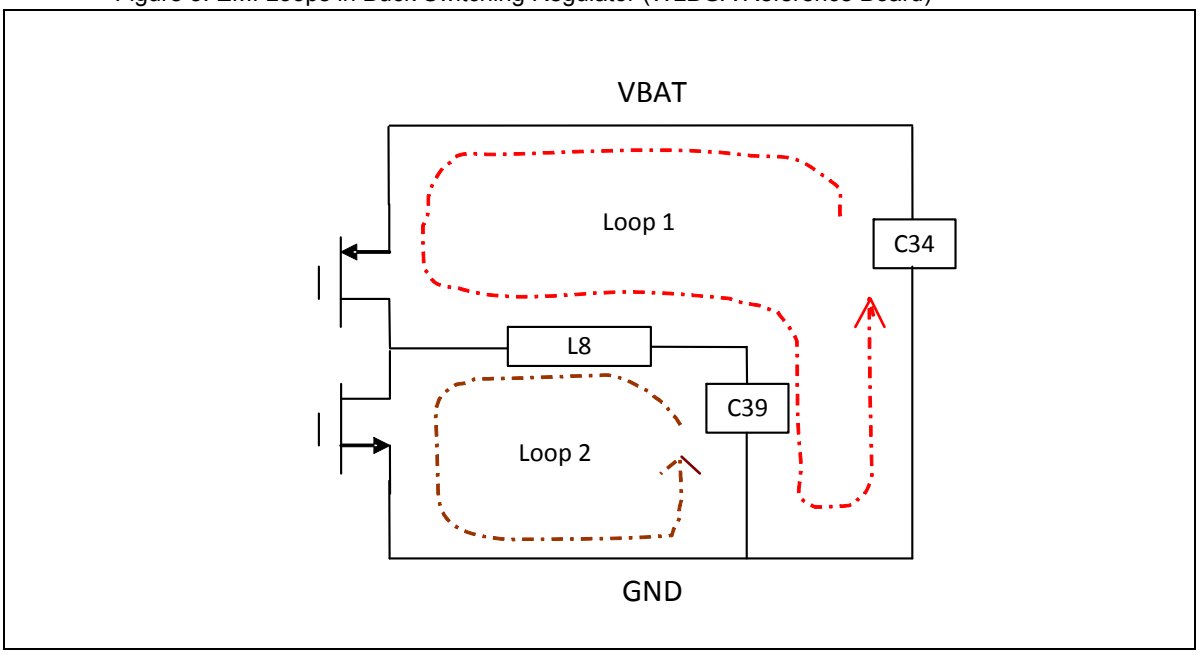


Figure 4 on page 5 shows how the four top layers are used around the PMU. Loop 1 from Figure 3 is shown as a red loop. Loop 2 from Figure 3 is shown as a yellow loop.

There is a separate ground island on layer 2 under L8 (top-right in Figure 4). This is also connected to the SR_PVSS (CBUCK power ground pin). This ground island helps contain the noise in the area within loop 1. The SR_VLX trace from pin SR_VLX to L8 runs on top of this layer 2 ground island to mirror the ground return path in loop 2.

The ground island under L8 on layer 2 is densely populated with vias (see Figure 5 on page 6) that connect to another ground island on layer 3, then to the main ground plane on layer 4. These vias can carry up to 500 mA of current; therefore, many vias must be used to reduce inductance and avoid ringing on the SR_PVSS pin during CBUCK switching.

Figure 4. Top Layers (WLBGA Reference Board)

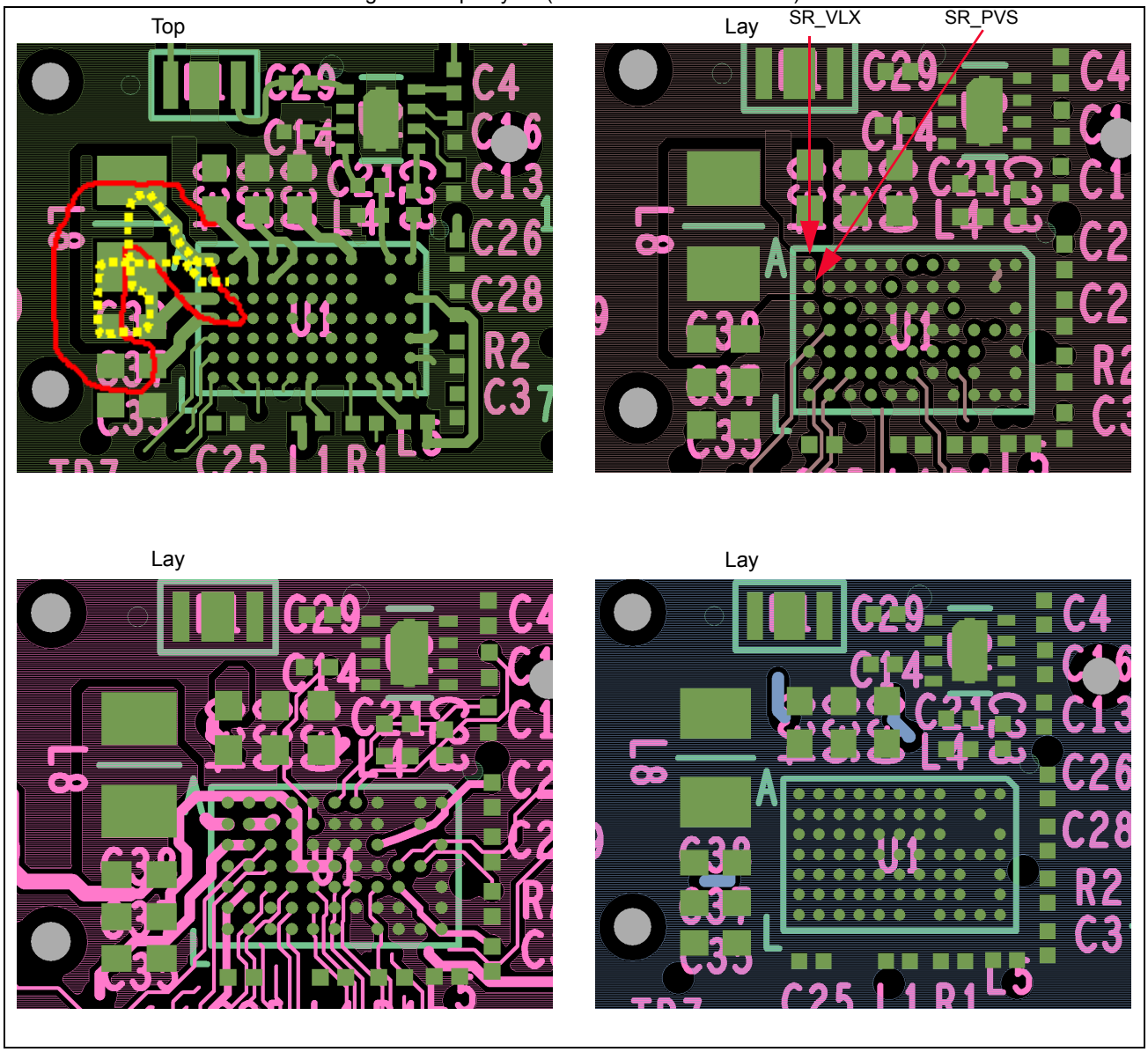


Figure 5 shows grounding on the top layer, covering the L8 inductor footprint and the regulator caps. This allows maximum coverage of ground for the PMU and allows more vias for the top layer ground plane to the underlying main ground plane.

Figure 5. Top Layer Grounding and Use of Ground Vias (WLBGA Reference Board)

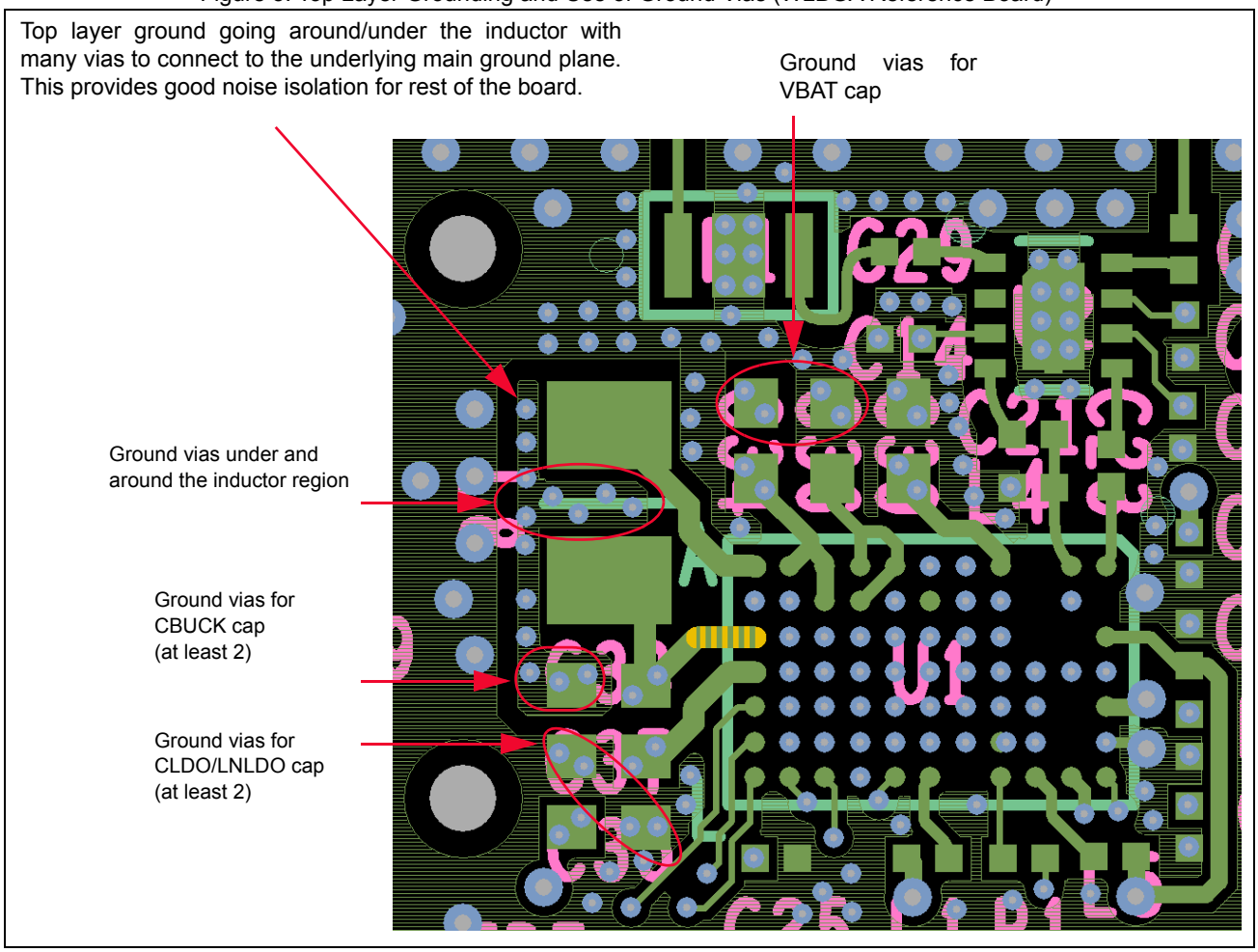
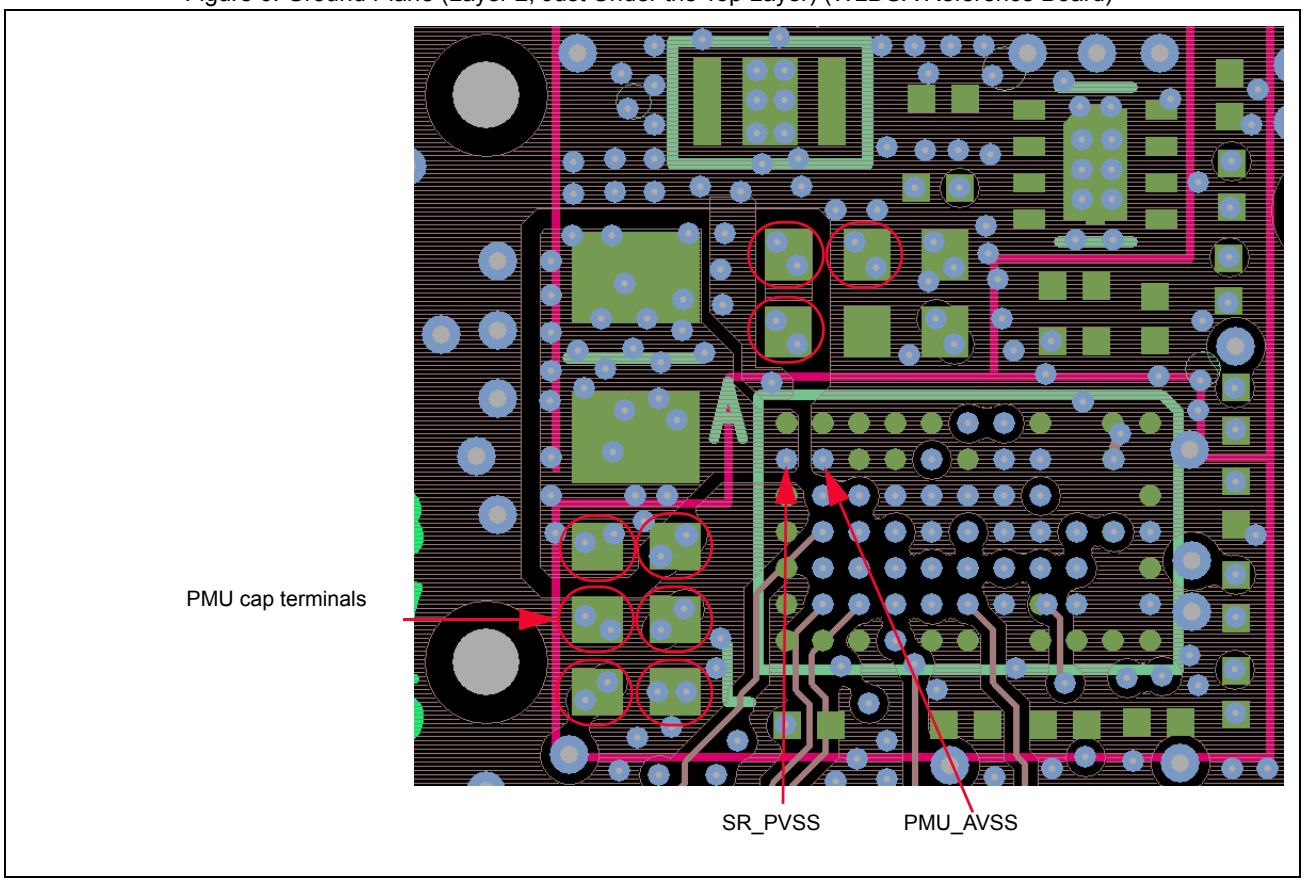


Figure 6 shows layer 2 with microvias added. The ground island under inductor L8 is populated by several vias for a good, low-parasitic connection to the ground plane at lower layers. Also, all PMU cap terminals are connected by at least two vias per terminal for low-parasitic connections to the main ground plane.

The main ground of CBUCK (SR_PVSS) and the quiet analog ground (PMU_AVSS) are connected by separate ground planes on layer 2, then they are ultimately joined in the main ground plane on layer 4. The separation of ground planes prevents the quiet ground from being contaminated by the large ground switching currents of SR_PVSS.

Figure 6. Ground Plane (Layer 2, Just Under the Top Layer) (WLBGA Reference Board)



3.2 CYW4330 WLCSP

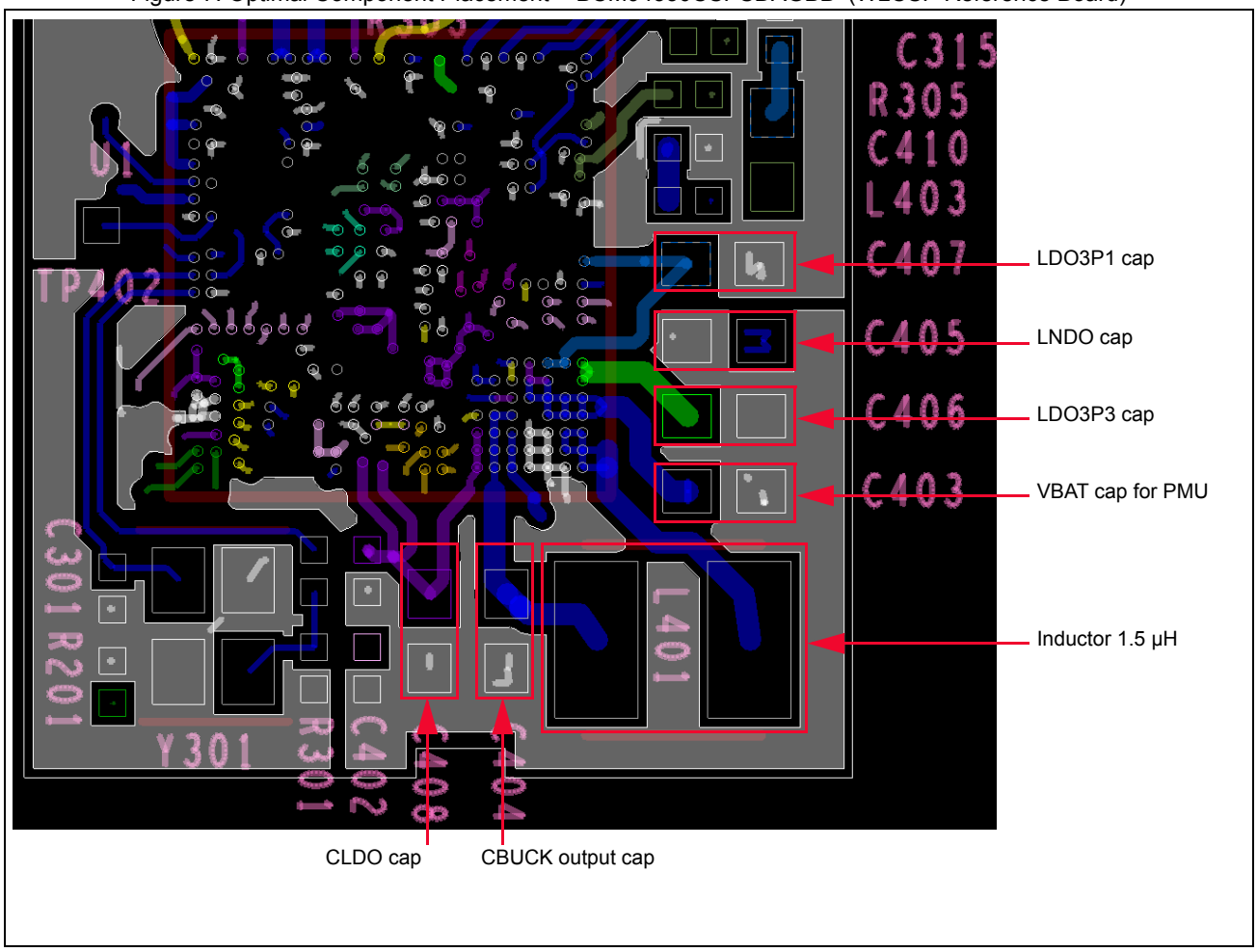
3.2.1 Correct PMU Component Placement

Figure 7 shows an example of optimal component placement to their respective regulator pins.

The highlighted components are:

- L401 = 0806 size SR_VLX pin driving CBUCK inductor
- C403 = 0402 size VBAT shared cap for SR_VDDBAT1 & SR_VDDBAT2 pins
- C404 = 0402 size CBUCK output cap
- C408 = 0402 size VOUT_CLDO cap
- C405 = 0201 size VOUT_LNLDO cap
- C406 = 0402 size VOUT_3P3 cap
- C407 = 0402 size VOUT_3P1 cap

Figure 7. Optimal Component Placement—BCM94330CSPSDAGBB (WLCSP Reference Board)



Note: Refer to the full recommended BOM list for PMU components.

Based on the BCM94330CSPSDAGBB Broadcom reference board, the red boxes in Figure 7 outline all the critical PMU-related components. By placing these components close to their connecting pins, routing can be achieved with minimal length, as shown in Figure 7.

3.2.2 PMU Board Routing Considerations

Figure 8 shows the routing using the top layer (i.e., the same layer as the footprints for components and CYW43362 WLBGA/CYW4330 WLSCP chip placement). Use of vias and routing layers other than the top layer is strongly discouraged for the following reasons:

- Microvias have lower current carrying capability.
- The VLX signal and inductor must carry up to 500 mA DC with a ripple of 800 mA pk-pk.
- The VBAT supply line must carry up to 600 mA of combined average current for CBUCK and LDO3P3.
- LDO3P3 sources a maximum of 80 mA, CLDO max 150 mA, LNLDO1 max 150 mA (300 mA for the CYW4330).
  - Microvias have high parasitic resistance and inductance. Any extra parasitic will add to power losses and higher switching noise spikes, causing interference.
  - Using microvias and lower layers increases the CBUCK switching current loop area, which is directly proportional to the radiated EMI (see Figure 9 on page 10).

In Figure 8, all routings are the shortest and widest possible to minimize parasitic resistance and inductance. Regulators are sensitive to routing parasitics, which can cause instability, power efficiency losses, and in extreme cases may cause the regulator to lose voltage regulation. Extreme parasitics caused by long skinny traces can also lead to large switching voltage spikes ,which can lead to long-term chip reliability problems.

Figure 8. Mandatory PMU Component Routing – Length/Width Rules (WLCSP Reference Board)

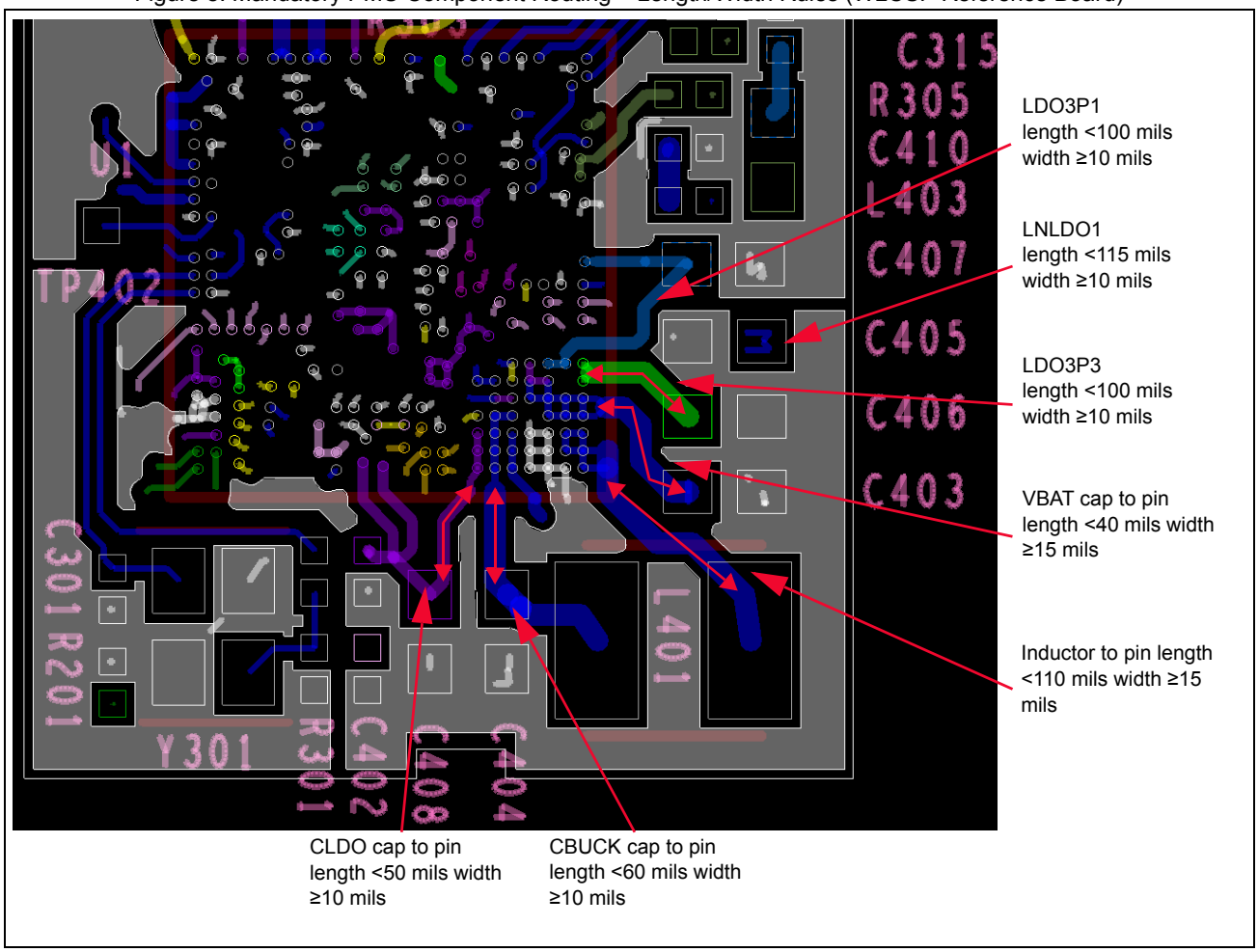


Figure 9 shows two current loops through the power MOSFETs of CBUCK. Each loop starts from a cap and ends at its ground terminal. The radiated EMI is proportional to the area within each loop. Routing of sensitive signals through the areas bounded by these two loops should be strictly avoided.

Figure 9. EMI Loops in Buck Switching Regulator (WLCSP Reference Board)

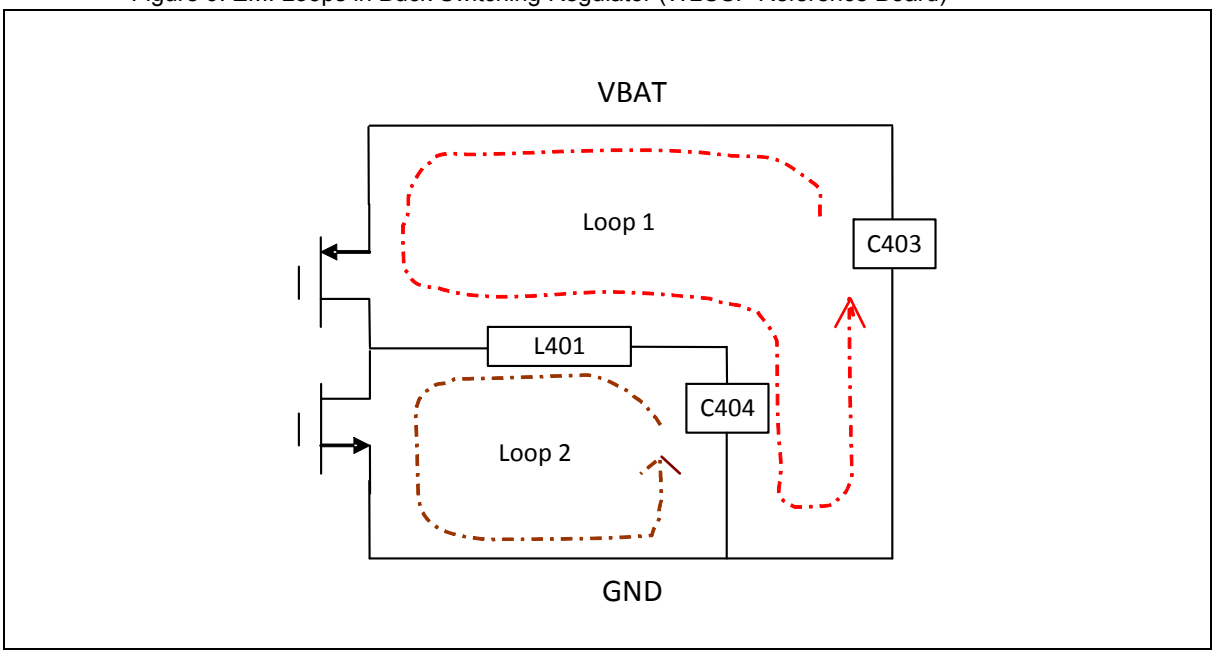


Figure 10 on page 11 shows how the four top layers are used around the PMU. Loop 1 from Figure 9 is shown as a red loop. Loop 2 from Figure 9 is shown as a yellow loop.

For the CYW4330 WLCSP board, layer 2 is a big solid ground plane that covers most of the layer (top-right in Figure 10). This layer has all the ground pins connected to it, including SR_PVSS (CBUCK power ground pin). This ground island helps contain the noise in the area within loop 1 and loop 2. The SR_VLX trace from pin SR_VLX to L401 runs on top of this layer 2 ground island to mirror the ground return path in loop 2.

The ground island under L401 on layer 2 is densely populated with vias (see Figure 11 on page 12) that connect to another ground island on layer 3, then to the main ground plane on layer 4 (bottom-left in Figure 10). These vias can carry up to 500 mA of current; therefore, many vias must be used to reduce inductance and avoid ringing on the SR_PVSS pin during CBUCK switching.

Figure 10. Top Layers (WLCSP Reference Board)

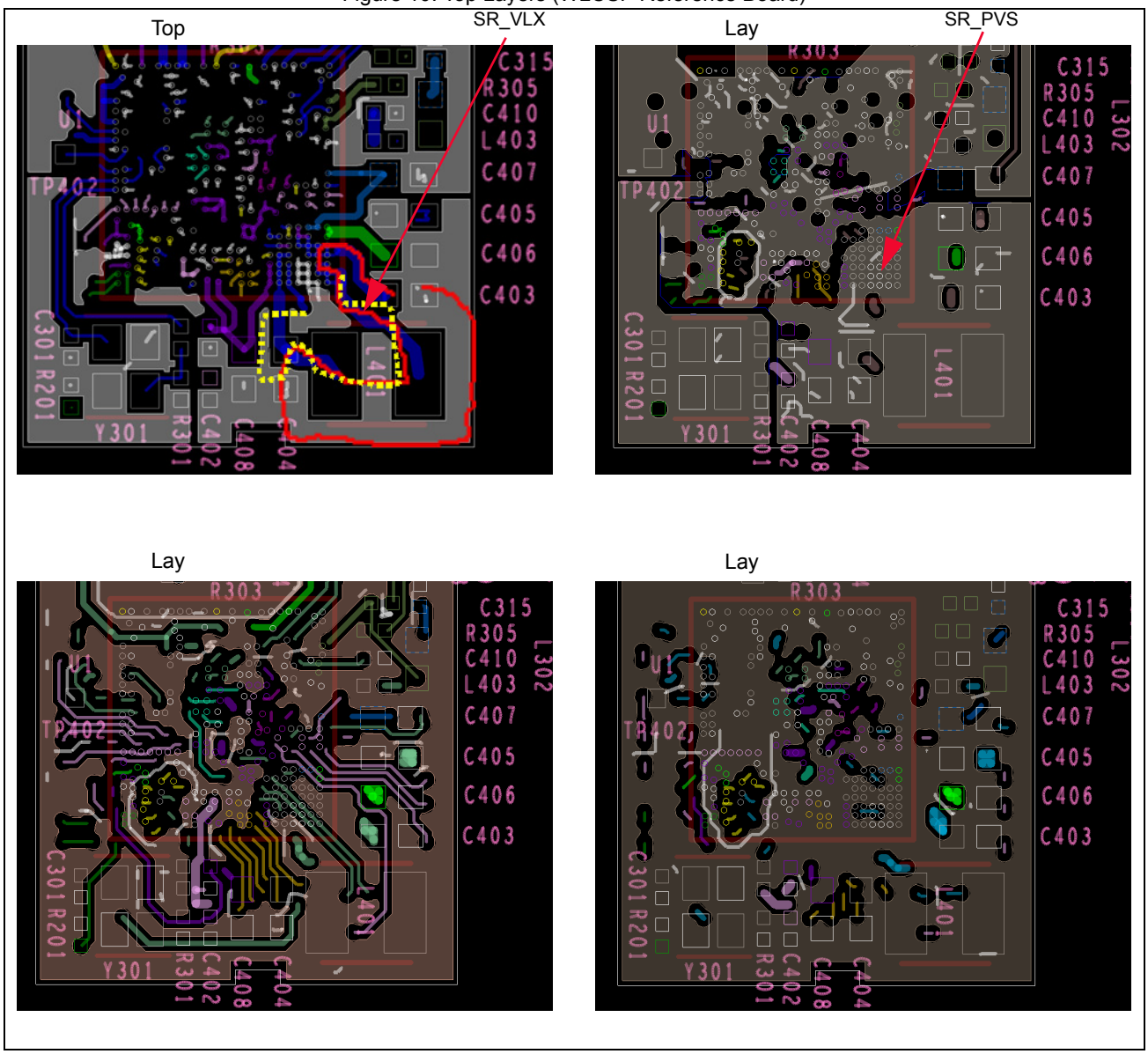


Figure 11 shows grounding on the top layer, covering the L401 inductor footprint and the regulator caps. This allows maximum coverage of ground for the PMU and allows more vias for the top layer ground plane to the underlying main ground plane.

Figure 11. Top Layer Grounding and Use of Ground Vias (WLCSP Reference Board)

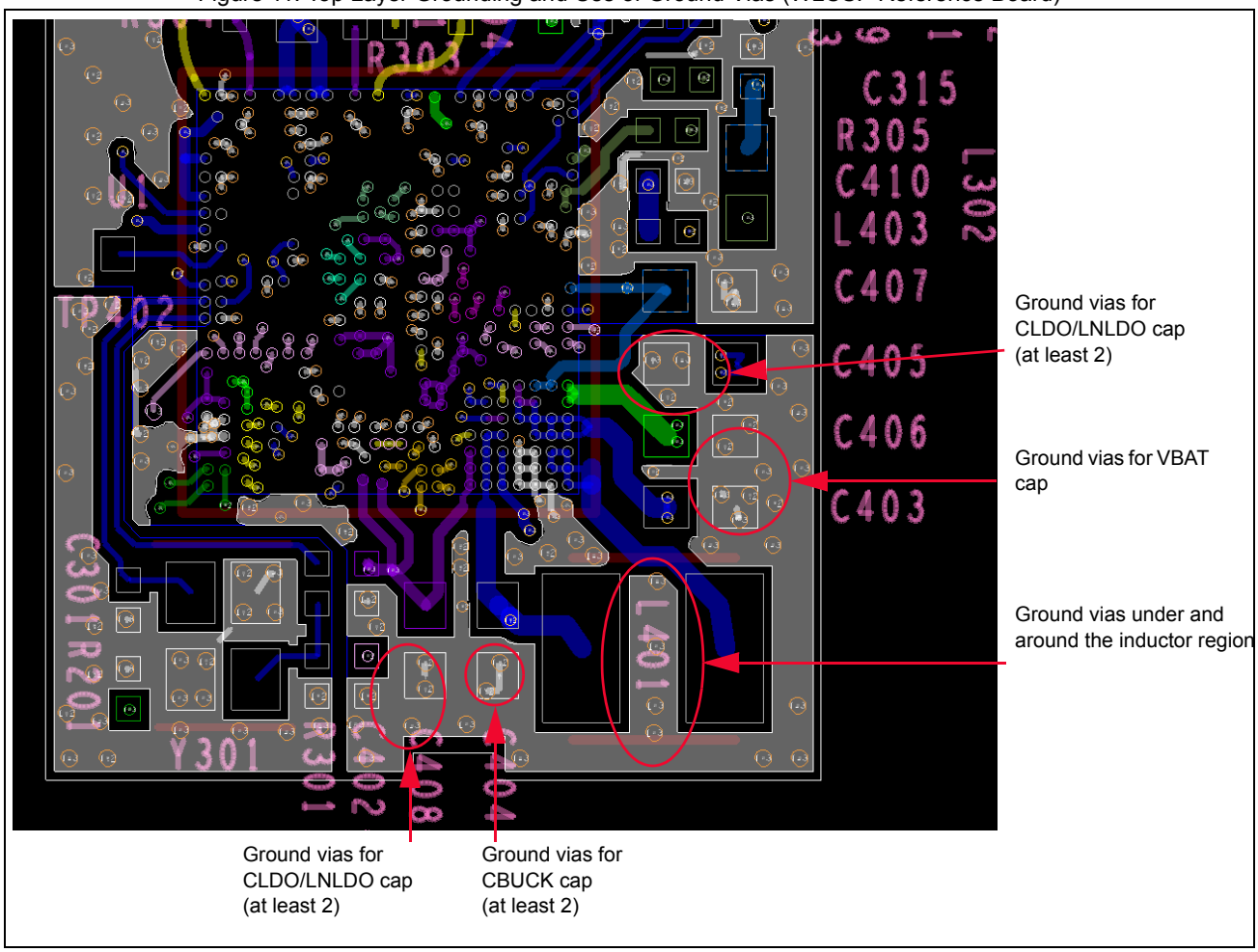
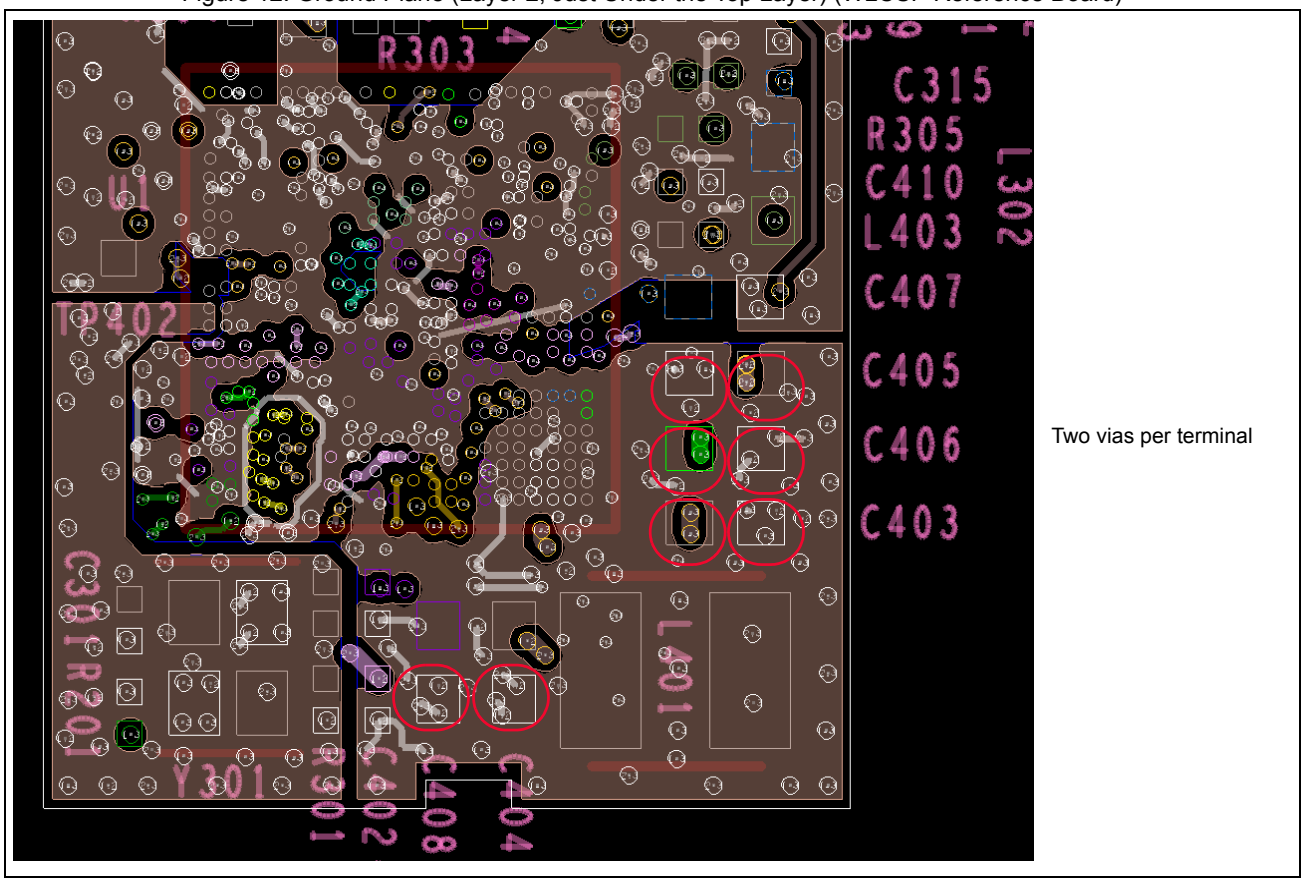


Figure 12 shows layer 2 with microvias added. The ground island under inductor L401 is populated by several vias for a good, low-parasitic connection to the ground plane at lower layers. Also, all PMU cap terminals are connected by at least two vias per terminal for low-parasitic connections to the main ground plane.

Layer 2 is the main ground plane for the PMU section-related ground (SR_PVSS and PMU_AVSS). This layer 2 is a big solid ground plane (shown as a brown area in Figure 12). It is able to contain noisy signals and provides low impedance return path for high PMU current to respective grounds (SR_PVSS and PMU_AVSS).

Figure 12. Ground Plane (Layer 2, Just Under the Top Layer) (WLCSP Reference Board)



4 Component Selection

This section explains the implications of selecting components that have inferior qualities.

Components that seem to have the same rating may not behave in the same manner due to different transient characteristics that cannot be fully described by their component ratings alone.

Always consult Cypress's PMU team for alternate choices of PMU components. The PMU team strongly advises designers to use **only the recommended PMU components**, since these components have been thoroughly validated in Cypress's system characterization.

4.1 Capacitors

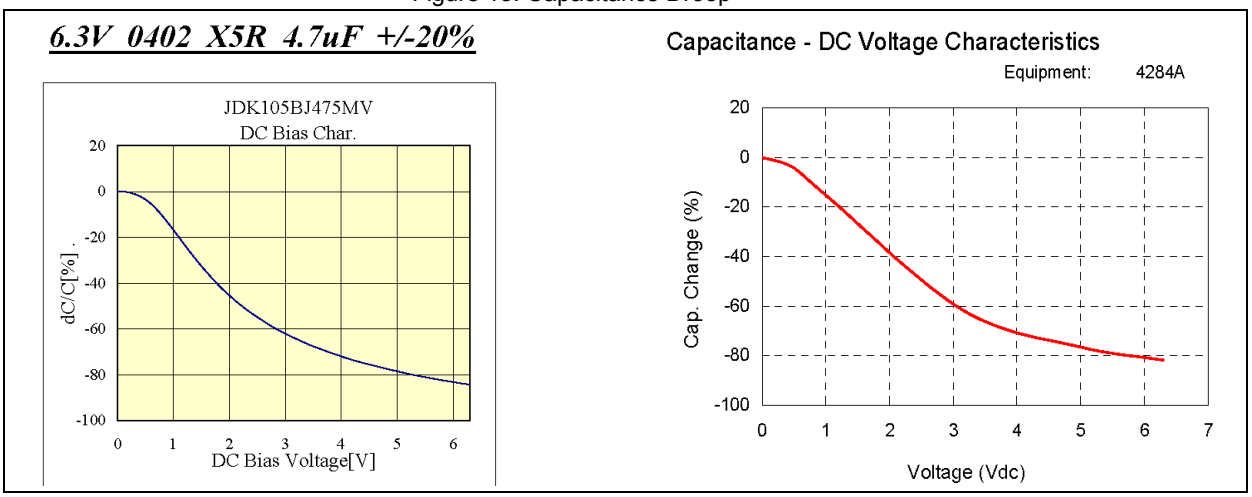
MLCC capacitors suffer from the following effects:

- Part-to-part tolerance
- Capacitance droop under DC-voltage bias
- Capacitance variation under temperature change (X5R)
- Aging effects

4.1.1 Capacitance Droop under DC Voltage Bias

Capacitors with the same part description may not necessarily show the same behavior. This is especially true for cap sizes smaller than 0603 (e.g., 0402 or 0201). The plots in Figure 13 show two 0402 size caps from two different manufacturers with significantly different performance. Both are 0402, X5R, 4.7 µF, ±20%, 6.3V ceramic caps.

Figure 13. Capacitance Droop



The cap on the left plot drops more at 1.5V bias compared to the cap shown on the right plot, even though both have the same 0402 size, 6.3V rating, nominal 4.7 µF value, and X5R. Users should always review the Capacitance vs. DC Bias Voltage plot for each capacitor.

4.1.2 Minimum Capacitance

The minimum capacitance (minC) for each regulator is the minimum design limit needed to ensure proper regulator functionality. Using caps that drop below minC in value causes regulators to malfunction. This minC rule cannot be compromised.

When using capacitors that tend to have smaller ESR/ESL and are outside of Cypress's recommended BOM list, you are strongly advised to consult your respective cap vendors on how to calculate the minimum capacitance caused by the combined effect of the following factors:

- Part-to-part tolerance
- Capacitance droop under DC-voltage bias
- Capacitance variation under temperature change (X5R)
- Aging effects

There is currently no standard method of adding up all these capacitor degradation factors.

The following formula can be used as a guide for choosing capacitors that are not part of the recommended cap list:

```
minC = TypC × (1–PartTol) × (1–DCBias) × (1–TempCo) × (1–Aging)
```

where:

- TypC—Typical capacitance.
- PartTol—Part-to-part tolerance (e.g., 0.2 is ±20%).
- DCBias—The amount of drop from TypC at target voltage (e.g., 0.2 is drop 20%).
- Target voltage is the default voltage of regulator output (e.g., CYW4330 CBUCK is 1.5 Vout).
- TempCo—The cap variation over X5R range of –55 ~ 85°C (e.g., 0.15 is ±15%).
- Aging—The amount of cap drop over time (e.g., 0.1 is 10% drop in 100,000 hours).

This formula is used only as a guide. The minimum capacitance value over a large volume for a particular capacitor should be guaranteed by the capacitor manufacturer. If their calculated capacitance for the part is lower than the minC for a regulator, or if the capacitor manufacturer cannot guarantee minC over volume, that part should not be used.

To choose a capacitor part with a higher minimum capacitance, try one or more of the following:

- Use 0603 instead of 0402 size.
- Use the highest voltage ratings possible (e.g., 16V or 10V instead of 6.3V).
- Use tighter ±10% instead of ±20% part-to-part tolerance.
- Use a larger cap nominal value (e.g., 10 µF instead of 4.7 µF).

After one or more of these attributes have been selected and the calculated minimum cap value based on the above formula meets the minC criteria, you should still ensure that the minC value is guaranteed by the capacitor manufacturer.

4.1.2.1 CBUCK Output Cap

- Nominal cap value is 4.7 µF.
- Capacitance should not drop more than 27% under 1.5V bias (i.e., output voltage).
- For the CYW43362, capacitance should not drop more than 36% under 1.8V bias.
- CBUCK stability for minC is 1.90 µF.
- Recommended caps:
  - GRM188R60J475ME84D (0603 X5R 4.7 µF 20% 6.3V Murata)
  - GRM188R60J475ME19D (0603 X5R 4.7 µF 20% 6.3V Murata)
  - GRM188R61A475KE15 (0603 X5R 4.7 µF 20% 10V Murata)
  - GRM155R60J475ME87D (0402 X5R 4.7 µF 20% 6.3V Murata)
  - GRM155R60J106ME44 (0402 X5R 10 µF 20% 6.3V Murata)

4.1.2.2 SR_VDDBAT1, SR_VDDBAT2, SR_VDDBAT3 Cap

- Nominal cap value is 4.7 µF.
- Capacitance should not drop more than 80% at extreme 5.5V VBAT level. It should not drop more than 73% at 4.3V VBAT level.
- Good VBAT noise suppression is 1.2 µF at 4.3 Vbat level.
- Strongly recommended caps:
  - GRM188R60J106ME84D (0603 X5R 10 µF 20% 6.3V Murata)
  - GRM188R60J106ME47D (0603 X5R 10 µF 20% 6.3V Murata)
  - GRM188R60J475ME84D (0603 X5R 4.7 µF 20% 6.3V Murata)
  - GRM188R60J475ME19D (0603 X5R 4.7 µF 20% 6.3V Murata)
  - GRM155R60J475M87D (0402 X5R 4.7 µF 20% 6.3V Murata)

4.1.2.3 CLDO Output Cap

- Nominal cap value is 4.7 µF (CYW4330); 2.2 µF (CYW43362).
- Capacitance should not drop more than 15% under 1.25V bias (i.e., CLDO output).
- CLDO stability for minC is 2.3 µF (CYW4330); 1.25 µF (CYW43362).
- Recommended caps for CYW4330:
  - GRM188R60J475ME84D (0603 X5R 4.7 µF 20% 6.3V Murata)
  - GRM188R60J475ME19D (0603 X5R 4.7 µF 20% 6.3V Murata)
  - GRM188R61A475KE15 (0603 X5R 4.7 µF 20% 10V Murata)
  - GRM155R60J475M87D (0402 X5R 4.7 µF 20% 6.3V Murata)
- Recommended cap for CYW43362:
  - GRM155R60J225ME15 (0402 X5R 2.2 µF 20% 6.3V Murata)

4.1.2.4 LNLDO1 Output Cap

- Nominal cap value is 4.7 µF (CYW4330); 2.2 µF (CYW43362).
- Capacitance should not drop more than 20% under 1.25V bias (i.e., LNLDO1 output).
- LNLDO1 stability for minC is 2.3 µF (CYW4330); 1.25 µF (CYW43362).
- Recommended caps for CYW4330:
  - GRM188R60J475ME84D (0603 X5R 4.7 µF 20% 6.3V Murata)
  - GRM188R60J475ME19D (0603 X5R 4.7 µF 20% 6.3V Murata)
  - GRM188R61A475KE15 (0603 X5R 4.7 µF 20% 10V Murata)
  - GRM155R60J475M87D (0402 X5R 4.7 µF 20% 6.3V Murata)
- Recommended cap for CYW43362:
  - GRM155R60J225ME15 (0402 X5R 2.2 µF 20% 6.3V Murata)

4.1.2.5 LDO3P3 Output Cap

- Nominal cap value is 4.7 µF (CYW4330); 1 µF (CYW43362).
- Capacitance should not drop more than 62% under 3.3V bias for 4.7 µF nominal value.
- Capacitance should not drop more than 28% under 3.3V bias for 1 µF nominal value.
- LDO3P3 stability for minC is 1.2 µF (CYW4330); 0.6 µF (CYW43362).
- Recommended caps for CYW4330 (0603 caps are better than 0402 due to less cap drop at 3.3V):
  - GRM188R60J475ME84D (0603 X5R 4.7 µF 20% 6.3V Murata)
  - GRM188R60J475ME19D (0603 X5R 4.7 µF 20% 6.3V Murata)
  - GRM188R61A475KE15 (0603 X5R 4.7 µF 20% 10V Murata)
  - GRM155R60J475M87D (0402 X5R 4.7 µF 20% 6.3V Murata)
- Recommended caps for CYW43362 (0603 caps are better than 0402 due to less cap drop at 3.3V):
  - GRM188R61C105KA93 (0603 X5R 1.0 µF 10% 16V Murata)
  - GRM155R61A105KE15 (0402 X5R 1.0 µF 10% 10V Murata)

4.1.2.6 LDO3P1 Output Cap

- Nominal cap value is 2.2 µF.
- Capacitance should not drop more than 41% under 2.5V bias.
- LDO3P1 stability for minC is 0.86 µF.
- Recommended caps (0603 caps are better than 0402 due to less cap drop at 2.5V):
  - GRM188R61A225KE34 (0603 X5R 2.2uF 10% 10V Murata)
  - GRM155R60J225ME15 (0402 X5R 2.2uF 20% 6.3V Murata)

4.2 Inductors

The following are the recommended default inductors:

- Murata LQM2MPN1R5NG0 or LQM2MPN2R2NG0 (for CYW43362 CBUCK)
- Murata LQM2MPN2R2NG0 (for CYW4330 CBUCK)

Table 2. Approved CBUCK Inductors

	Maker	*Part Name*	*Width (mm)*	*Length (mm)*	*Max Height (mm)*	*Lnom (uH)*	*Tol (±%)*	*DCR (mΩ)*	*DCR Tol (±%)*	*ACR @ 3 MHz, No-load (Ω)*	*+40°C Isat (mA)*	*L-30% Isat (mA)*	*Typ. L (uH) at 500 mA*	*Inductor type*	*Comments*
1	Murata	LQM21PN2R2NGC	2	1.25	1	2.20	30	230	25	1.80	800	500	1.700	multi-layered	
2	Murata	LQM2MPN2R2NG0	2	1.6	1	2.20	30	110	25	0.90	1200	450	1.500	multi-layered	Default part for CYW4330 CBUCK
3	Cyntec	PSD20161T-2R2MS	2	1.6	1	2.20	20	196	20	2.30	1300	1400	2.1	wire-wound	
4	TDK	VLS201610ET-2R2N	2	1.6	1	2.20	20	230	20	–	950	1050	2.125	wire-wound	
5	TDK	VLS2010ET-2R2N	2	1.25	1	2.20	20	190	20	–	1050	1000	2.300	wire-wound	
6	TDK	MLP2012S2R2M	2	1.25	1	2.20	20	230	30	1.5	800	700	1.8	multi-layered	
7	TDK	MLP2016V2R2M	2	1.6	1	2.20	20	110	30	1.00	1100	500	1.600	multi-layered	
8	TaiyoYuden	CKP2012N2R2M	2	1.25	1	2.20	20	150	33.33	1.25	800	570	1.500	multi-layered	
9	Murata	LQM2HPN2R2MG0	2.5	2	1	2.20	20	80	25	0.80	1300	530	1.700	multi-layered	
10	FDK	MIPSZ2012D2R2	2	1.25	1	2.20	30	230	30	0.87	700	650	1.750	multi-layered	
11	FDK	MLP2520S2R2M	2.5	2	1	2.20	20	90	30	–	1200	600	1.600	multi-layered	
12	TaiyoYuden	CKP2520N2R2M	2.5	2	1	2.20	20	75	20	–	1300	600	1.600	multi-layered	
13	TaiyoYuden	CKP2016N2R2M	2.5	2	1	2.20	20	110	30	–	900	500	1.500	multi-layered	

These are multi-layered inductors that exhibit more dynamic characteristics compared to wire-wound ones. Inductors that are not from the recommended BOM list must be assessed by Cypress's PMU team using the following parameters:

- Inductor part-to-part tolerance: should be ±20% (at most ±30%)
- DCR:
  - DCR vs. temperature
- ACR:
  - ACR vs. frequency under no-load, mid-load, max-load conditions
  - ACR vs. frequency under minimum, typical, max operating temperatures, at max-load
  - ACR vs. 3.2 MHz ripple current amplitude for no-load and max-load conditions
- Isat1: saturation current based on nominal inductance –30%
- Isat2: saturation current based on +40°C self-heating temperature rise

- Inductance under Isat2 vs. operating temperature range (i.e., –40°C to +125°C)
- Shielding

All the above characteristics must be known before an inductor can be assessed for its suitability for CBUCK.

4.2.1 DCR

DCR contributes to the conduction power losses of the CBUCK. Excessive DCR can lead to power losses up to 5%.

- For CYW43362 CBUCK supporting an output higher than the default 1.833V, DCR should be kept below 137.5 mΩ maximum to ensure voltage regulation under the high-duty cycle scenario (e.g., VBAT = 2.3V, Vout = 1.833V, max 500 mA load.

DCR over-operating temperature range should be kept below 170 mΩ maximum.

- For CYW4330 CBUCK (1.5 Vout), DCR should be ≤ 350 mΩ under all conditions to minimize power losses.

4.2.2 ACR

ACR contributes to switching power losses in the CBUCK.

- ACR should be <1Ω under no-load conditions to ensure lower switching losses at low-loads.
- ACR at 3.2 MHz over –40°C to +125°C at 500 mA load should be <2.3Ω.

4.2.3 Saturation Currents

4.2.3.1 Isat1

Multi-layered inductor data sheets usually do not display Isat1 explicitly due to lower current level. Isat1 is defined as the load current that causes the inductance to drop by 30% from the nominal value.

For CYW43362 CBUCK with a nominal value of 1.5 µH, the inductance must not drop below 0.8 µH nominal value at 500 mA load. This CBUCK can also take 2.2 µH value inductor (the same inductor as CYW4330 CBUCK). Inductance must stay above 0.6144 µH at 500 mA under all conditions.

For CYW4330 CBUCK with a nominal value of 2.2 µH, the inductance must not drop below 1.5 µH nominal at 500 mA load. Inductance must stay above 1.0 µH at 500 mA under all conditions.

4.2.3.2 Isat2

Isat2 is usually shown on multi-layered data sheets and is usually higher than Isat1. Isat2 is defined as the saturation current causes the inductor to self-heat by +40°C.

Isat2 should be much higher than 500 mA; preferably >700 mA.

Inductance under Isat2 vs operating temperature range (i.e., –40°C to +125°C)

Inductance should be characterized with Isat2 across the full operating temperature range of the inductor.

The recommended operating temperature range is –40°C to +125°C inclusive of the inductor self-rise temperature (i.e., +40°C).

The inductor operating temp up to +125°C (including inductor self-heating +40°C) corresponds to the customer product temperature maximum of 85°C.

Inductance should not vary more than ±4% over the operating temperature range (–40°C to +125°C) under Isat2.

Shielding

Magnetic shielding, ferrite drum shielding, or magnetic-resin coated shielding is highly recommended to prevent EMI issues.

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	06/11/2010	4330_4336_43362-AN100-R Initial release
			05/16/2011	4330_4336-AN100-R Added: CYW4330 WLCSP on page 7. Table 2, “Approved CBUCK Inductors,” on page 17. Updated: About This Document on page 1. Board Layout Design Guidelines on page 2. Component Selection on page 13.
*A	5463583	UTSV	10/07/2016	Updated in Cypress template Added Cypress part numbering scheme
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