AN214942

WLBGA Layout Design Guide

Associated Part Family: CYW43340

This application note provides important information about the CYW43340 that pertains to WLBGA package layout design. Such information includes trace routing restrictions, parts placement, descriptions of the six layers of the CYW43340, and guidelines for layout, routing, and component selection.

Contents

1 About this Document

1.1 Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM43340	CYW43340

1.2 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Cypress documents, go to: http://www.cypress.com/glossary

2 IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

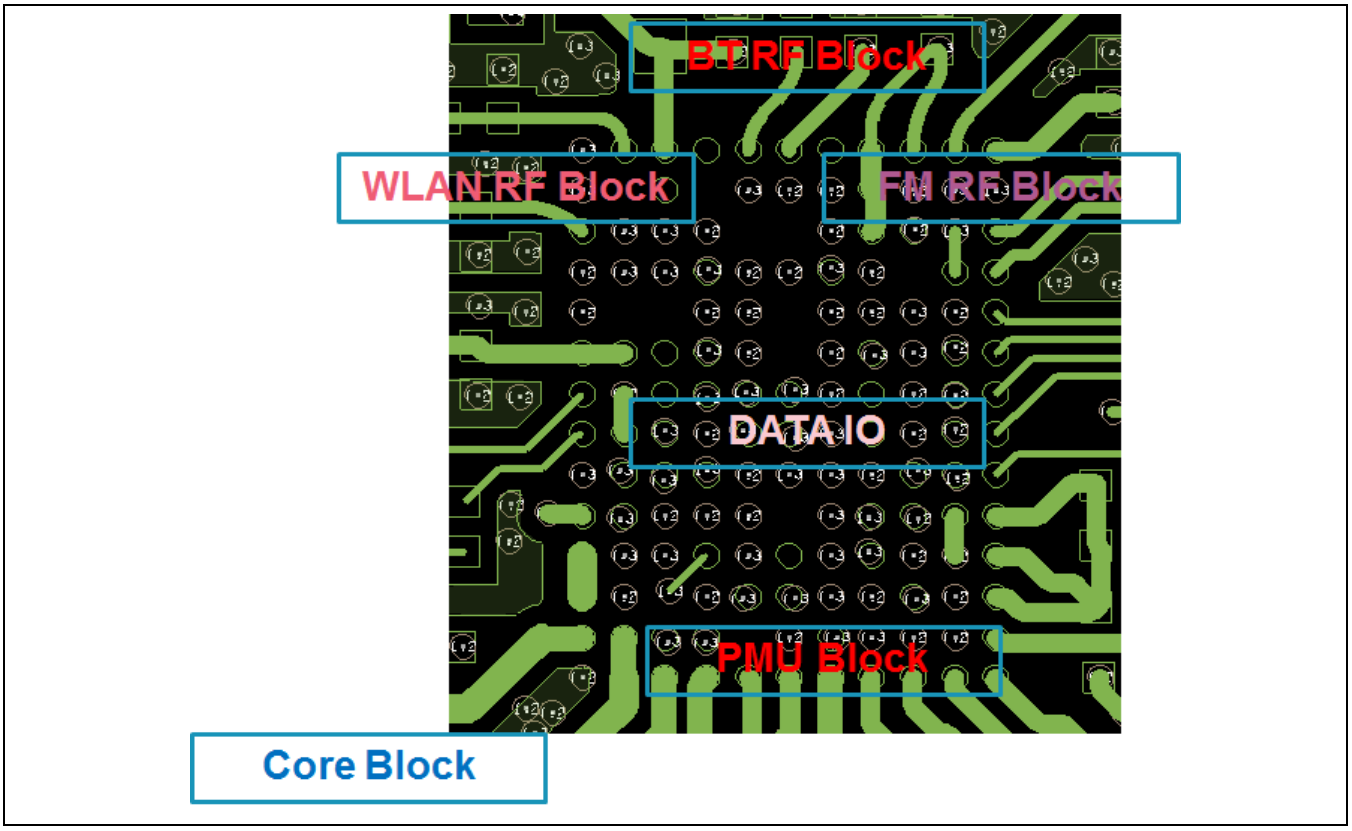
3 Introduction

The CYW43340 has the following layers:

- Layer 1: Part placement, RF signal
- Layer 2: GND
- Layer 3: Digital, I/O signals and clock
- Layer 4: GND
- Layer 5: Most of the power lines
- Layer 6: GND

The mechanical size of the CYW43340 is 4.47 mm × 5.67 mm. The various blocks are shown in Figure 1.

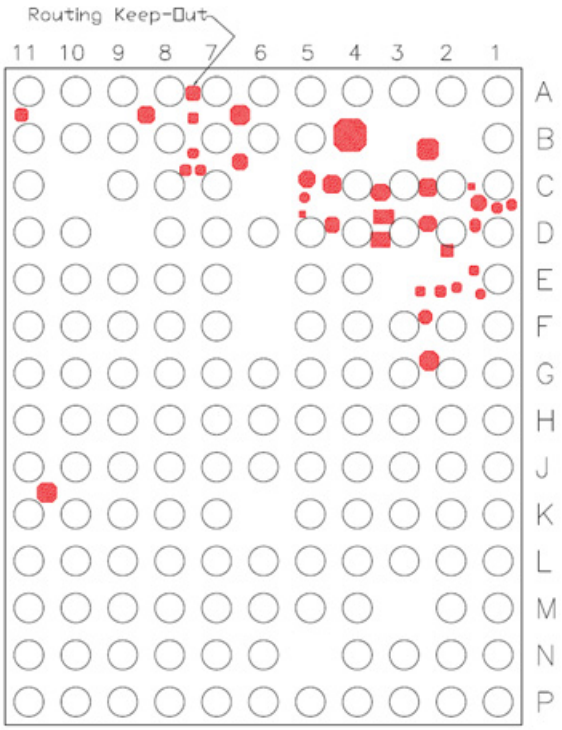
Figure 1: CYW43340 Pin Map



4 Trace Routing Restrictions

There are several keep-out areas on the CYW43340 WLBGA package, as shown in red in Figure 2. Do not route any traces below these areas on the top layer.

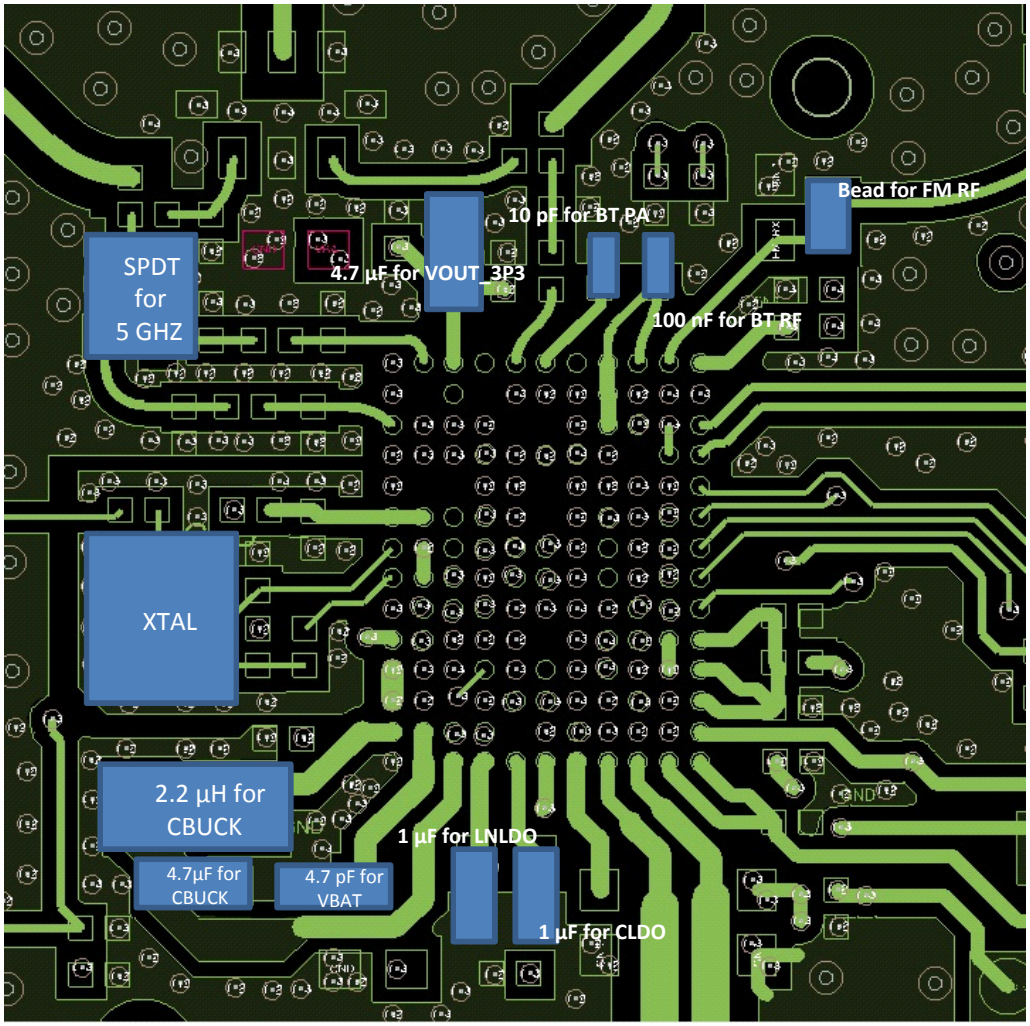
Figure 2. Keep-Out Areas



5 Parts Placement

The locations of the various parts that are placed on the CYW43340 are shown in Figure 3.

Figure 3. Part Placement

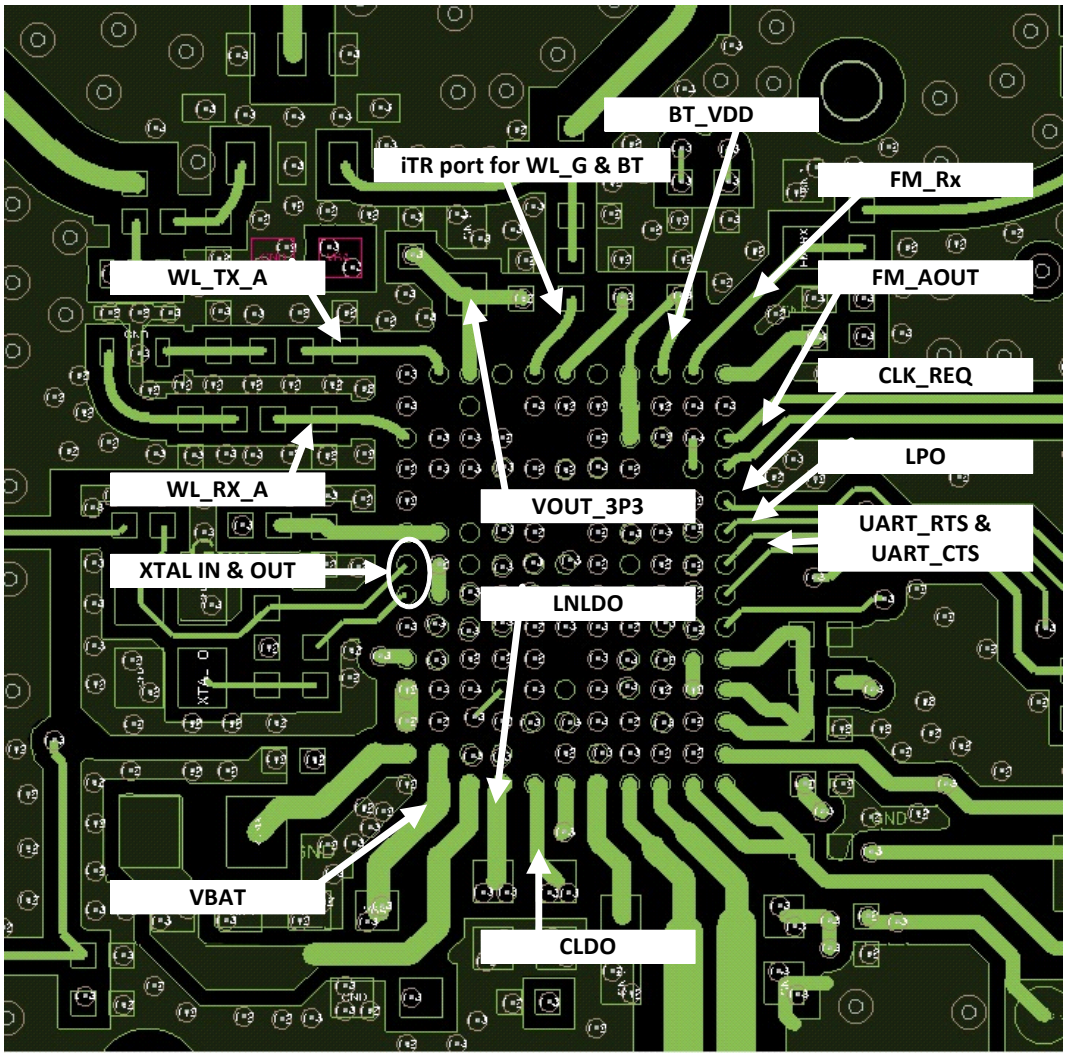


6 Layers

6.1 Top Layer

The top layer of the CYW43340 is shown in Figure 4.

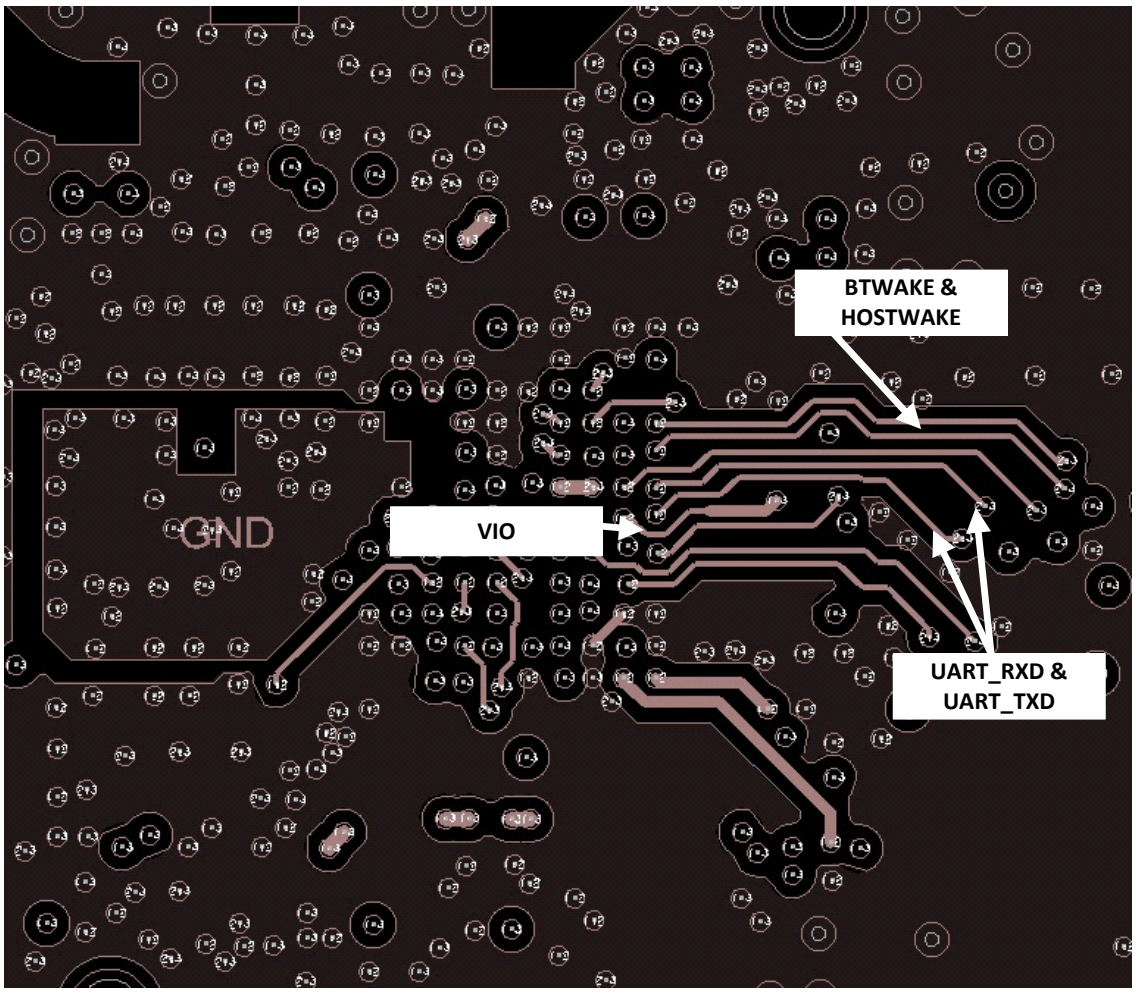
Figure 4. CYW43340 Top Layer



6.2 Second Layer

The second layer (GND) of the CYW43340 is shown in Figure 5.

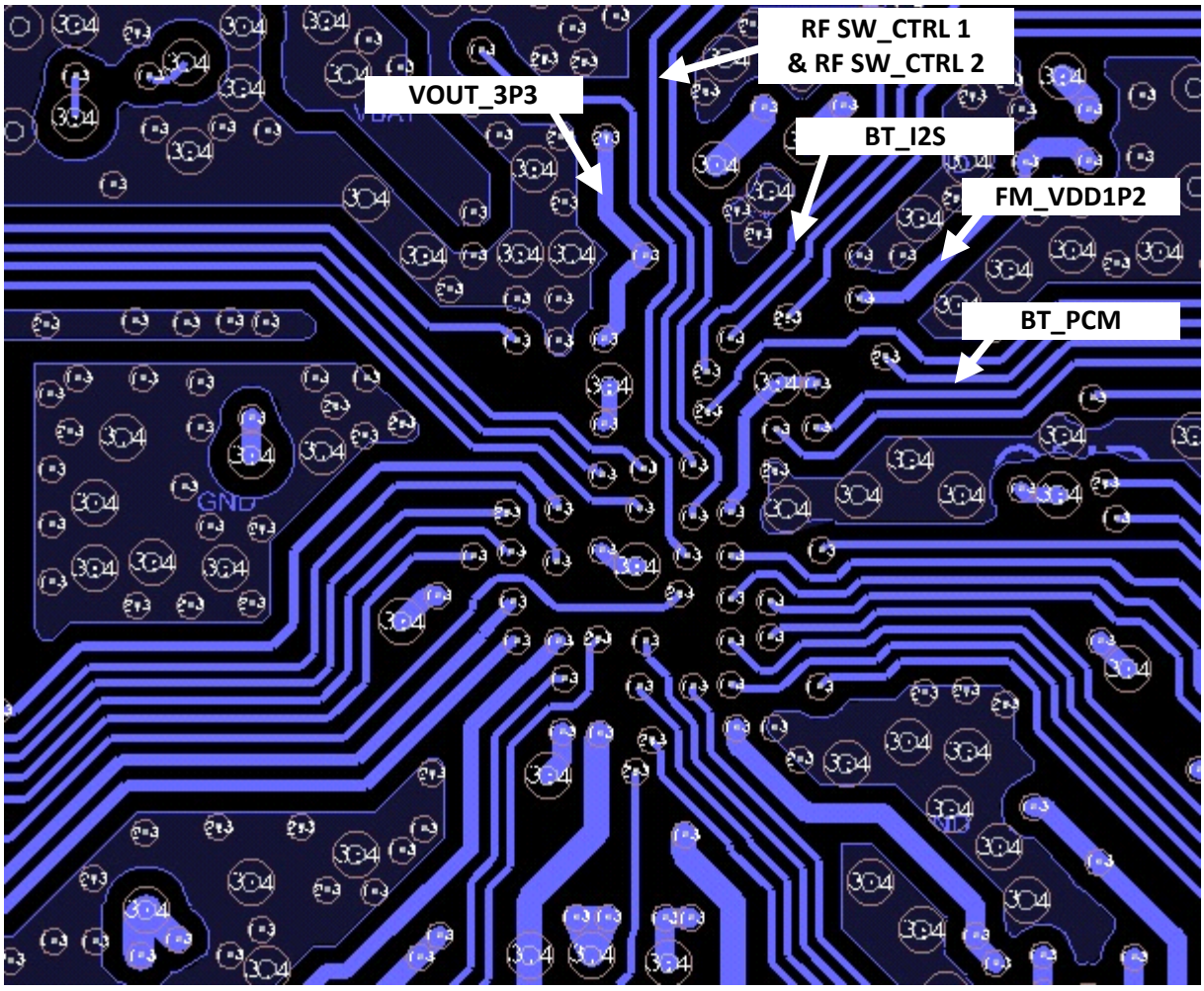
Figure 5. CYW43340 Second Layer (GND)



6.3 Third Layer

The third layer of the CYW43340 is shown in Figure 6.

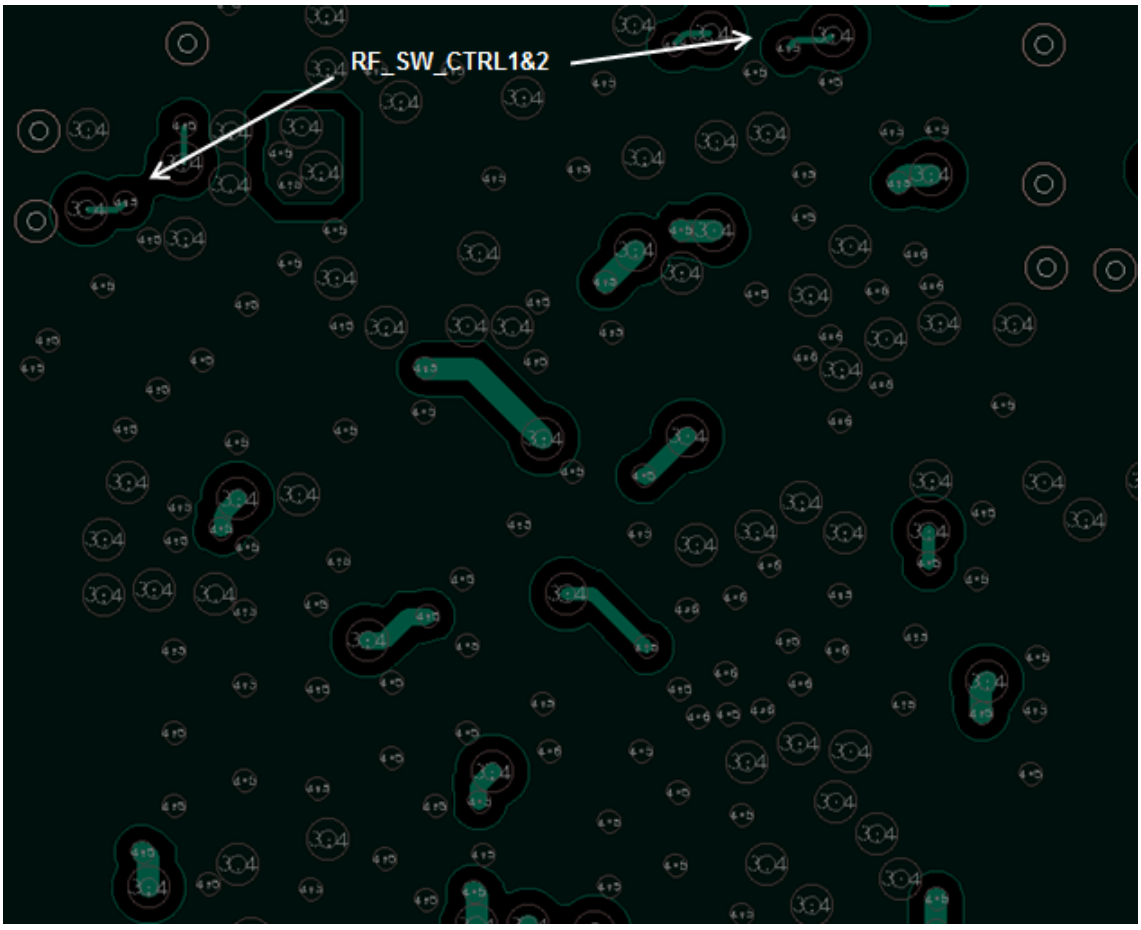
Figure 6. CYW43340 Third Layer



6.4 Fourth Layer

The fourth layer (GND) of the CYW43340 is shown in Figure 7.

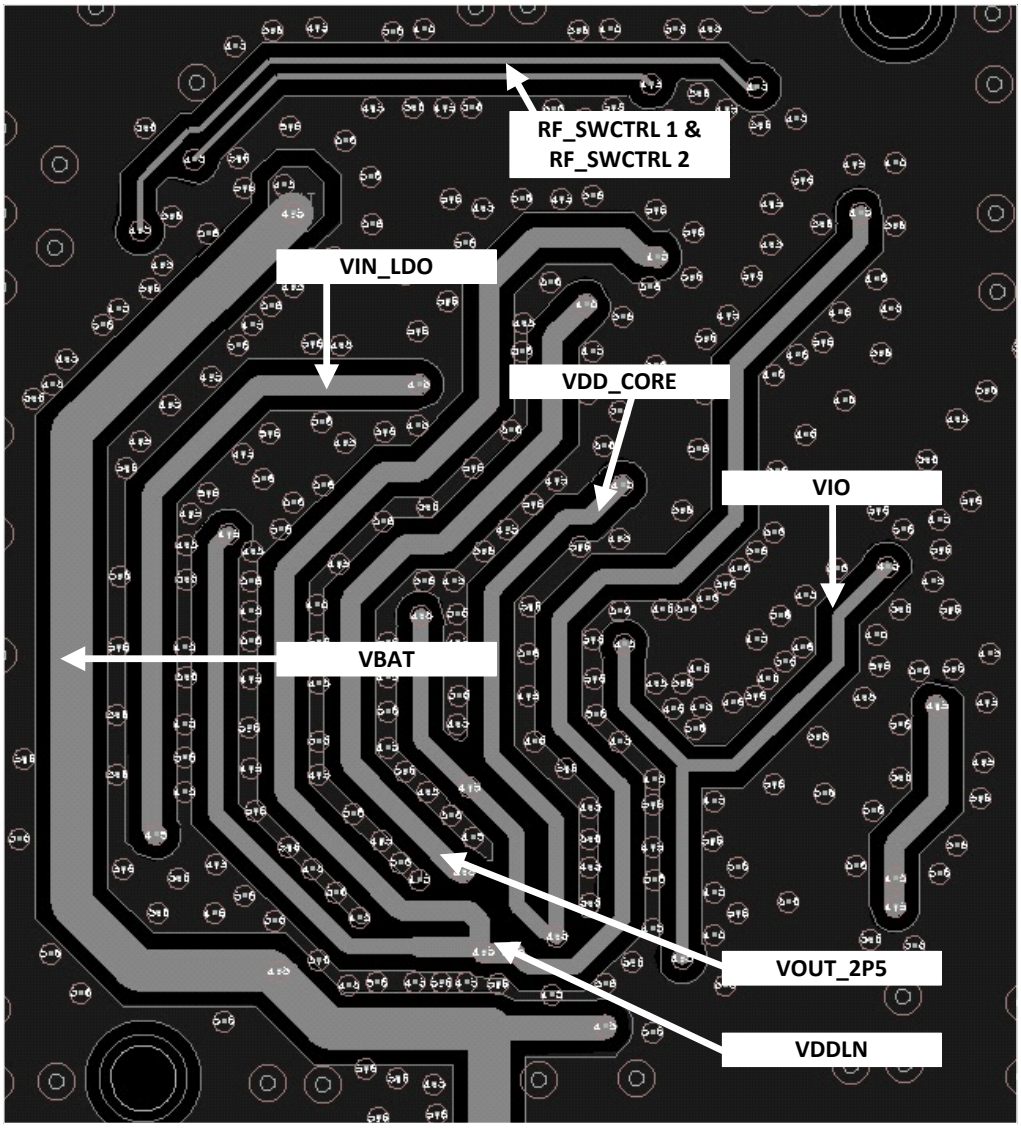
Figure 7. CYW43340 Fourth Layer



6.5 Fifth Layer

The fifth layer of the CYW43340 is shown in Figure 8.

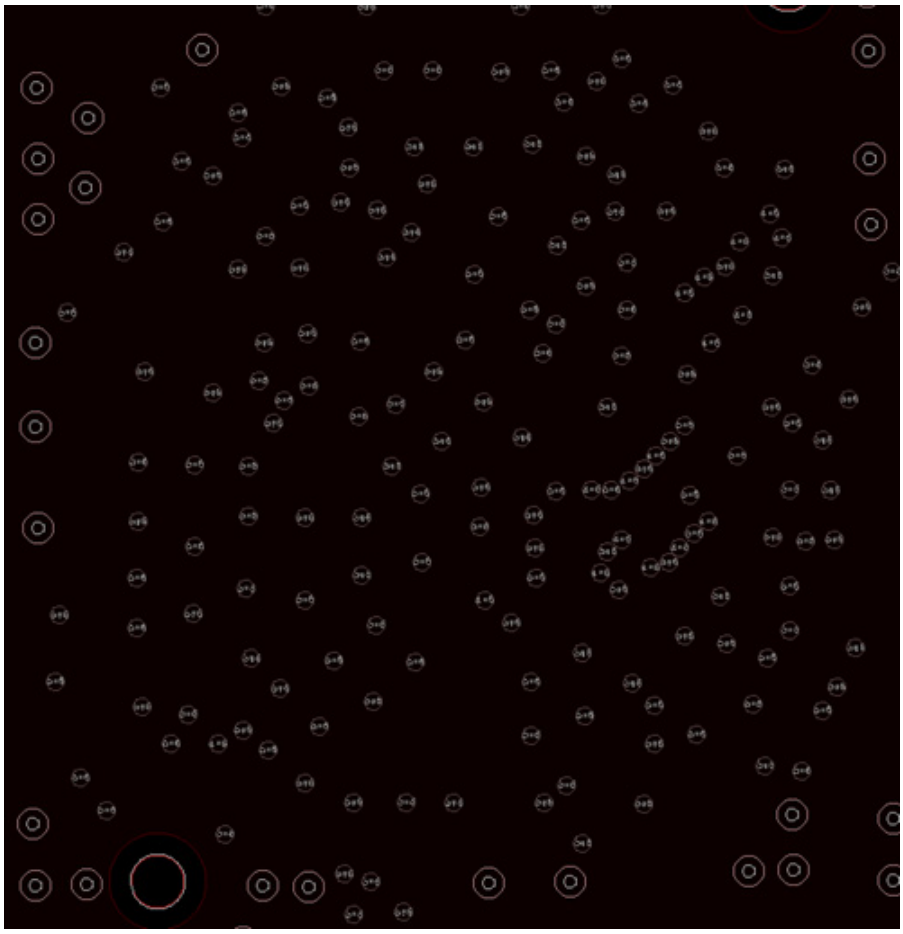
Figure 8. CYW43340 Fifth Layer



6.6 Sixth Layer

The sixth layer of the CYW43340 is shown in Figure 9.

Figure 9. CYW43340 Sixth Layer

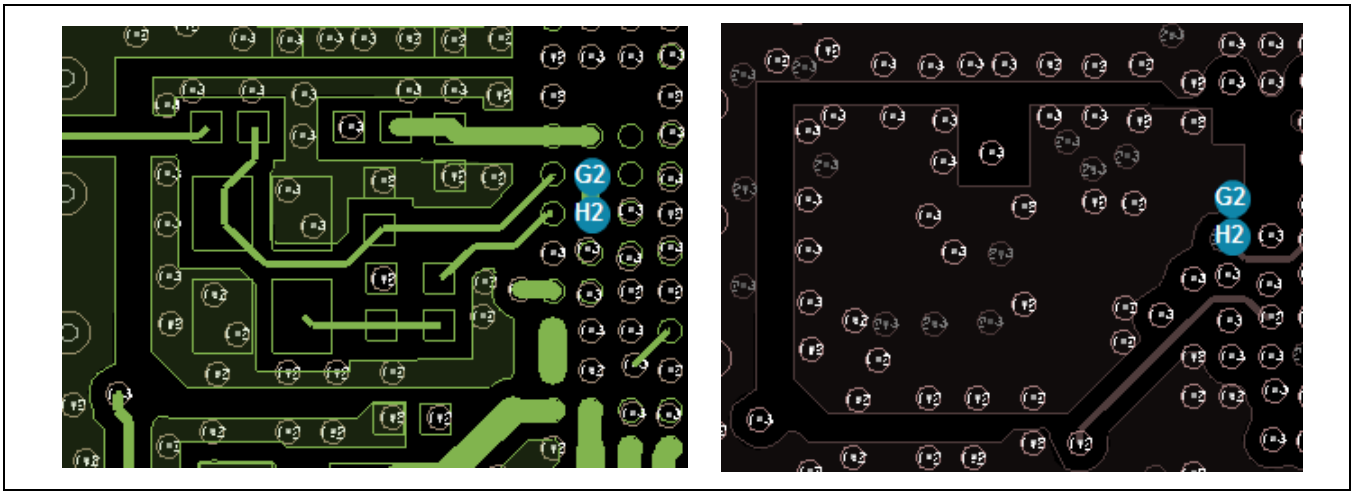


7 Guidelines

7.1 XTAL Layout Guidelines

- The GND and loading capacitors of the XTAL must have a low impedance and a direct path to pins G2 and H2 (see Figure 10).
- The XTAL GND plane should have a direct via to the reference GND plane.
- Isolate the XTAL GND from noisy lines to avoid coupling.
- Isolate the XTAL GND on the second and third layers.

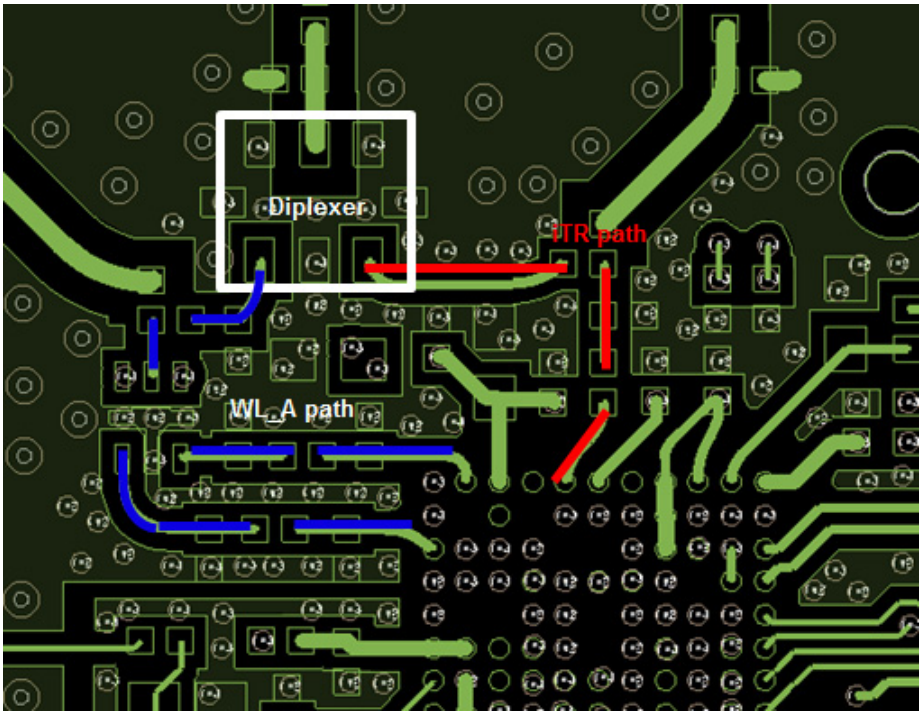
Figure 10. G2 and H2 Pins on Top Layer (Left) and Second Layer (Right)



7.2 RF Routing Guidelines

- When routing RF lines, try to keep them on the same layer on the component side to avoid using a via on the RF lines.
- Add GND stitches around RF lines and ensure that they are 50-ohm impedance.
- Provide adequate isolation and spacing on each RF trace.
- Regarding the distance of the RF traces between the CYW43340 and the FEM, make sure that the TX line is the shorter of the two (see Figure 11).

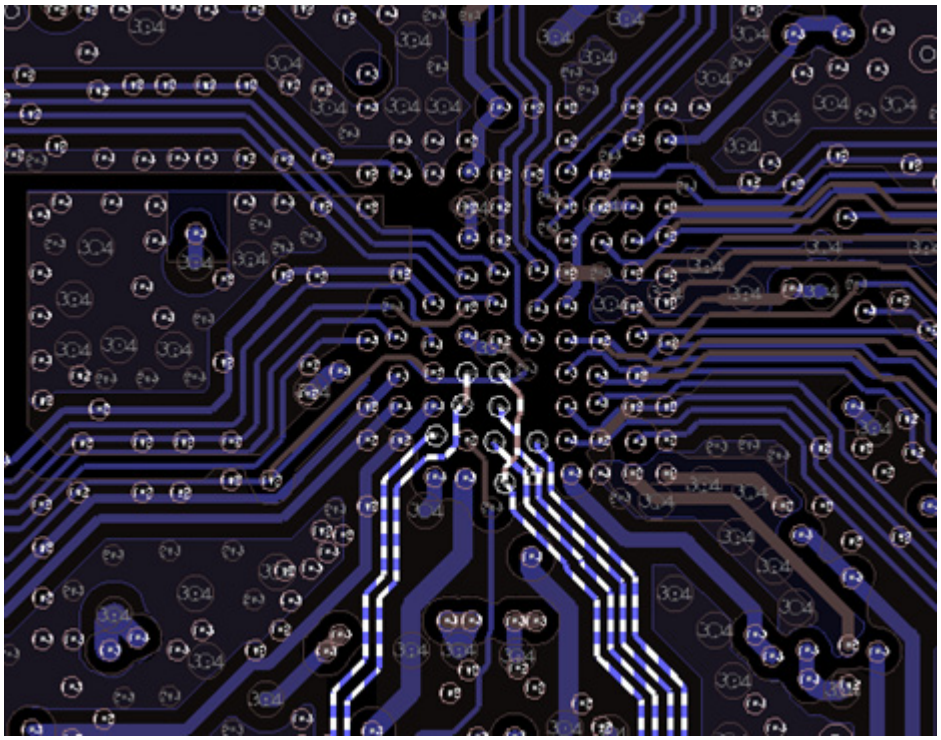
Figure 11. RF Traces



7.3 SDIO Layout Guidelines

- The characteristic impedance of the SDIO2.0 traces should be 50 ohms.
- Do not leave any stubs on traces and limit the length of DATA trace to not exceed that of the CLK trace.
- Match the lengths of the SDIO lines to within ±100 mils. Note that the time delay is about 16.7 ps for every 100 mils of length.
- Keep the SDIO_CLK line away from the SDIO CMD and DATA lines (use the 2:1 rule of thumb). Routing the SDIO_CLK line parallel and close to command and data lines can cause glitches on the bus, thus affecting SDIO operation.

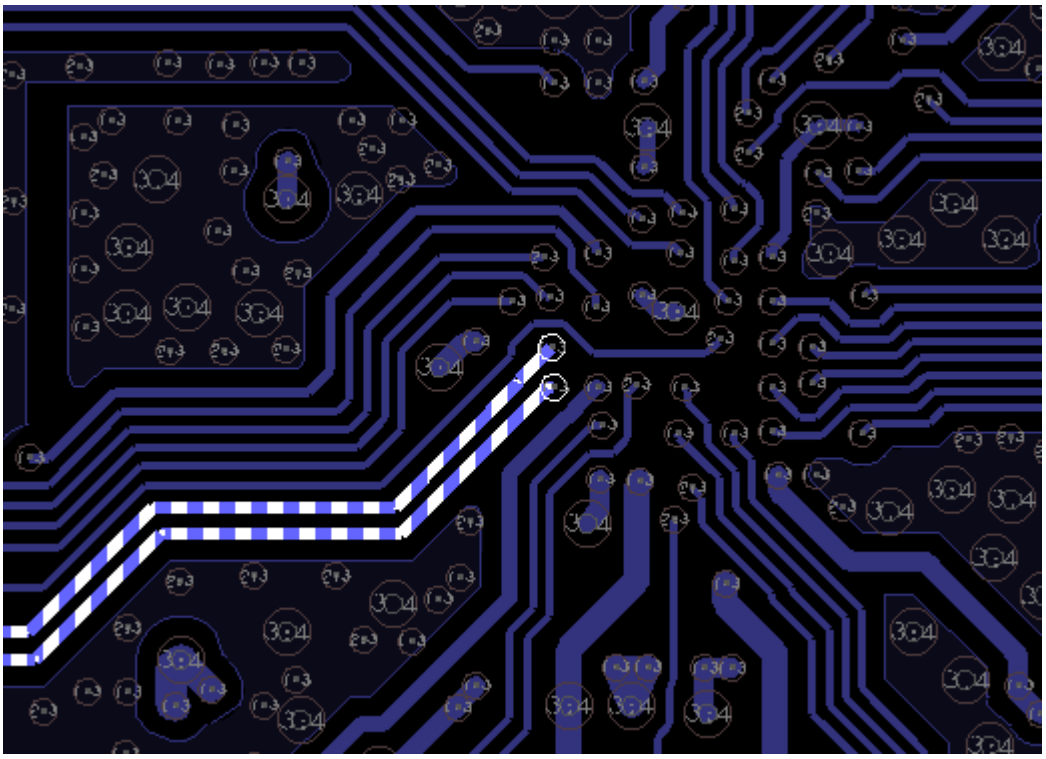
Figure 12. CYW43340 Layer 2 and 3 Showing SDIO Traces



7.4 HSIC Layout Guidelines

- Match the length of the traces to limit the time delay to less than 15 ps.
- The characteristic impedance of the traces should be 50 ohms.
- The trace length from the CYW43340 to the HOST chip should be less than 10 cm.

Figure 13. Layer 3 showing HSIC Traces



7.5 PMU—VBAT, CBUCK Guidelines

7.5.1 Component Selection

7.5.1.1 CBUCK Output Capacitor

The nominal capacitance value is 4.7 µF.

Effective capacitance should *not* drop more than 27% below its nominal value under 1.5V.

Minimum capacitance = 2 µF (only guarantees basic stability).

Recommended capacitors include:

- GRM188R60J475ME84D (0603 X5R 4.7 µF 20% 6.3V Murata)
- GRM188R60J475ME19D (0603 X5R 4.7 µF 20% 6.3V Murata)
- GRM188R61A475KE15 (0603 X5R 4.7 µF 20% 10V Murata)
- GRM155R60J475ME87D (0402 X5R 4.7 µF 20% 6.3V Murata)
- GRM155R60G106M (0402 X5R 10 µF 20% 4V Murata)

This capacitor has a typical self-resonance frequency = 3 MHz. Impedance/ESR = 2 mΩ. The ESR and ESL of the capacitor must be met to achieve good noise and transient performance.

7.5.1.2 SR_VDDBATP5V, SR_VDDBATA5V Shared Capacitor

The nominal capacitance value is 4.7 µF.

The effective capacitance should *not* drop more than 80% below its nominal value at 4.8V bias nor more than 73% below its nominal value at 4.3V bias.

For good VBAT performance, noise suppression is 1.2 µF at the 4.3Vbat level.

Recommended capacitors are:

- GRM188R60J475ME84D (0603 X5R 4.7 µF 20% 6.3V Murata)
- GRM188R60J475ME19D (0603 X5R 4.7 µF 20% 6.3V Murata)
- GRM155R60J475M 87D (0402 X5R 4.7 µF 20% 6.3V Murata)

This capacitor has a typical self-resonance frequency = 3 MHz. Impedance/ESR = 2 mΩ. The ESR and ESL of the capacitor must be met to achieve good noise and transient performance.

7.5.1.3 CBUCK Inductor

The nominal inductor value is 2.2 µH.

Table 2 lists the 0805/0806-inch inductors that have been qualified to work with the CYW43340 CBUCK.

Table 2. 0805/0806-inch Inductors Qualified to Work with the CYW43340 CBUCK

Inductor Data Sheet Specifications		Width	Length	Height	Typ L	L Tol	DCR Typ	DCR Tol	I_{dc} (mA)
Mfr	**Part No.**	**mm**	**mm**	**mm_Max**	**µH**	**%**	**m*W***	**%**	***D*T < 40°C**
Murata	LQM21PN2R2NGC	1.25	2	1	2.2	30	230	25	800
Murata	LQM2MPN2R2NG0L	1.6	2	1	2.2	30	110	25	1200

The inductors listed in Table 2 are multilayered inductors, which exhibit more dynamic characteristics compared to wire-wound inductors.

Inductors other than those listed in Table 2 must be assessed by the PMU team based on the following parameters:

- Inductor part-to-part tolerance preferably should be ±20% or, at most, ±30%.
- DCR
  - DCR versus temperature
- ACR
  - ACR versus frequency: Under no-load, mid-load, maximum-load conditions.
  - ACR versus frequency: Under minimum, typical, maximum operating temperatures, at maximum-load conditions.
  - ACR vs 4 MHz ripple current amplitude for no-load and maximum-load conditions.
- I_{sat1}: Saturation current based on nominal Inductance – 30%.
- I_{sat2}: Saturation current based on +40°C self-heating temperature rise.
- Inductance under Isat2 versus operating temperature range (i.e., –40°C to +125°C)
- Shielding

All the above characteristics must be known before an inductor can be assessed for its suitability for CBUCK.

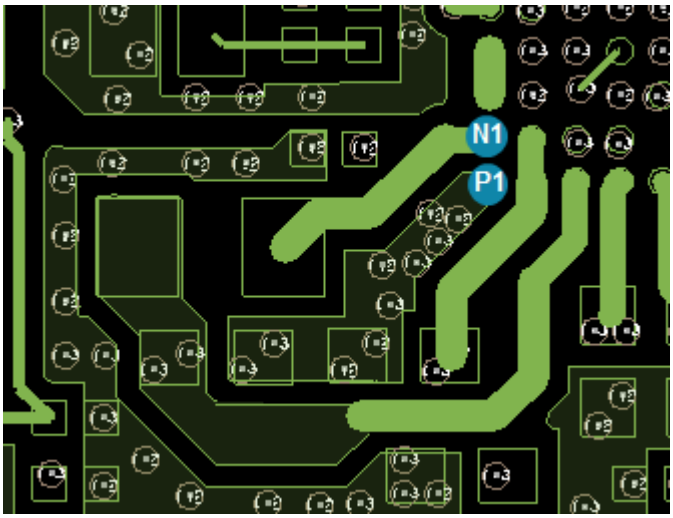
Other considerations:

- DCR
  - DCR contributes to the conduction power losses of the CBUCK.
  - Excessive DCR can lead to power loss by as much as 5%.

- ACR
  - ACR contributes to switching power losses in the CBUCK.
  - ACR should be < 1 ohm at a 4 MHz frequency under no-load conditions to ensure that lower switching losses occur at low loads. The ACR at a frequency of 4 MHz, within a temperature range of –40°C to +125°C, and under a 600 mA load should be less than 1 ohm.
- Saturation current I_{sat1}
  - Multilayered inductor data sheets usually do not display I_{sat1} explicitly due to its lower current level. I_{sat1} is defined as the load current that causes the inductance to drop by 30% from the nominal value.
  - An excessive drop in inductance can lead to more inductor losses due to a larger inductor ripple current through ACR. A larger inductor ripple current can also lead to more switching current injection into ground.
  - For PWM loop stability, effective inductance at a 600 mA load should be at least 0.6 µH across all parts (tolerance included).
  - For best peak PWM efficiency at a 200 mA load point, the effective inductance at a 200 mA load should be at least 2 µH for the nominal part.
- Saturation current I_{sat2}
  - I_{sat2} is usually shown on multilayered data sheets and is usually higher than I_{sat1}.
  - I_{sat2} is defined as the saturation current that causes the inductor to self-heat by +40°C.
  - I_{sat2} should be at least 750 mA.
- Inductance under I_{sat2} versus operating temperature range (i.e., –40°C to + 125°C)
  - The inductance of the inductor should be characterized with I_{sat2} across the full operating temperature range of the inductor.
  - The recommended operating temperature range is –40°C to +125°C, inclusive of the inductor self-rise temperature (i.e., +40°C).
  - The inductor operating temperature up to +125°C (which includes the inductor self-heating of +40°C) corresponds to the customer product temperature maximum value of 85°C.
  - The inductance should not vary by more than ±4% over the operating temperature range (–40°C to +125°C) under I_{sat2}.

7.5.1.4 Top Layer

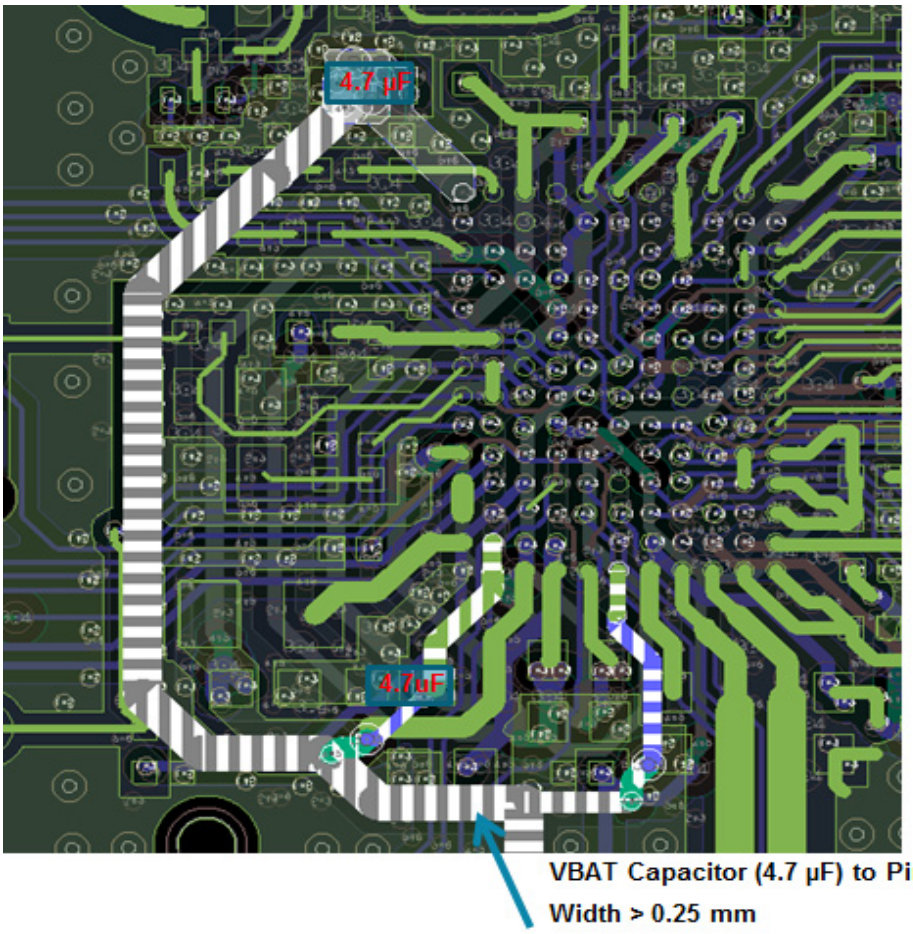
Figure 14. Top Layer Showing N1 and N2 Pins



- The bypass capacitor on VBAT and CBUCK should have many GND vias.
- Isolate the GND around CBUCK to avoid noise coupling.
- Use at least two vias on the bypass capacitor.
- To reduce EMI in the forward and return paths, the area enclosed by the following loops must be minimized:
  - SR_VLX1 (pin N1) to inductor and capacitor to SR_PVSS (pin P1).
  - SR_VBAT to supply bypass capacitors to SR_PVSS.

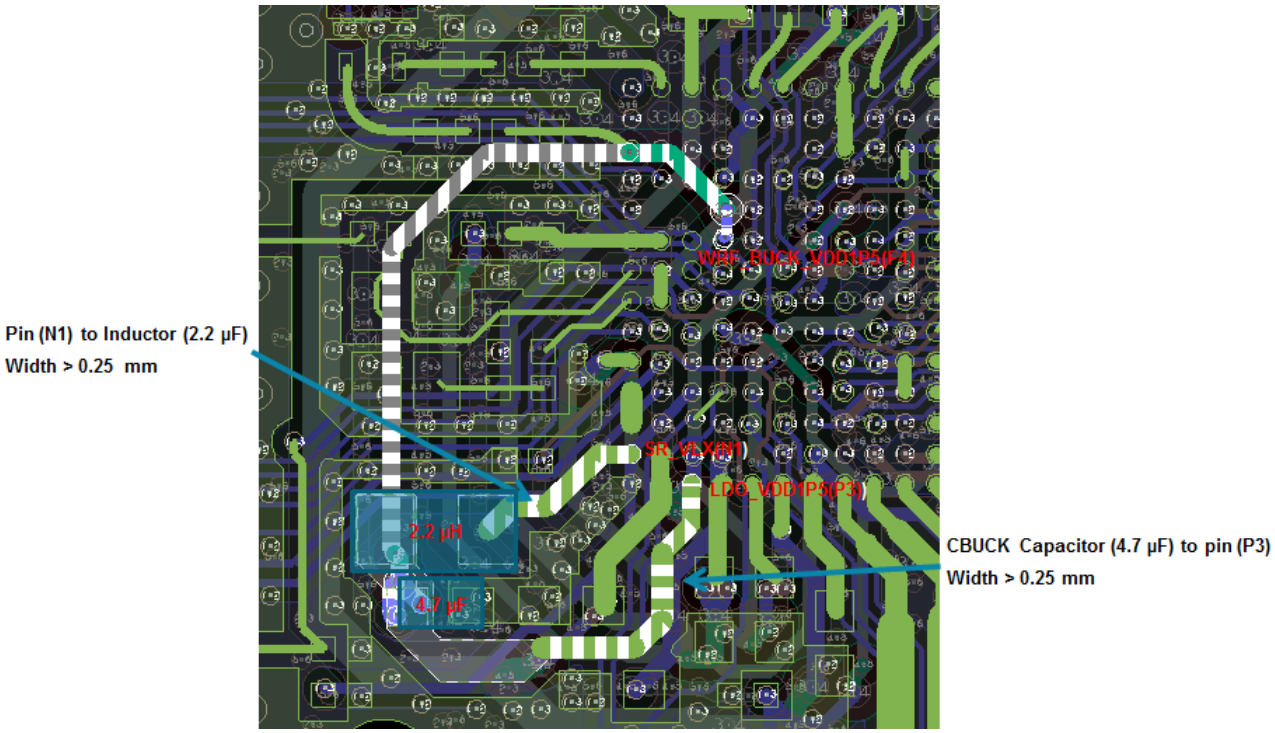
7.5.1.5 Power Rail: VBAT

Figure 15. Power Rail Showing VBAT Capacitor to Pin N2/P2/A1



7.5.1.6 Power Rail: CBUCK

Figure 16. Power Rail Showing CBUCK Capacitor Connection to Pin P3 and Pin N1 Connection to Inductor



7.6 PMU—VOUT_3P3

7.6.1 Component Selection

7.6.1.1 LDO3P3 Output Capacitor

The nominal capacitance value is 4.7 µF.

The effective capacitance should *not* drop more than 66% from the nominal value under 3.3V bias.

The minimum C= 1 µF.

Recommended capacitors include:

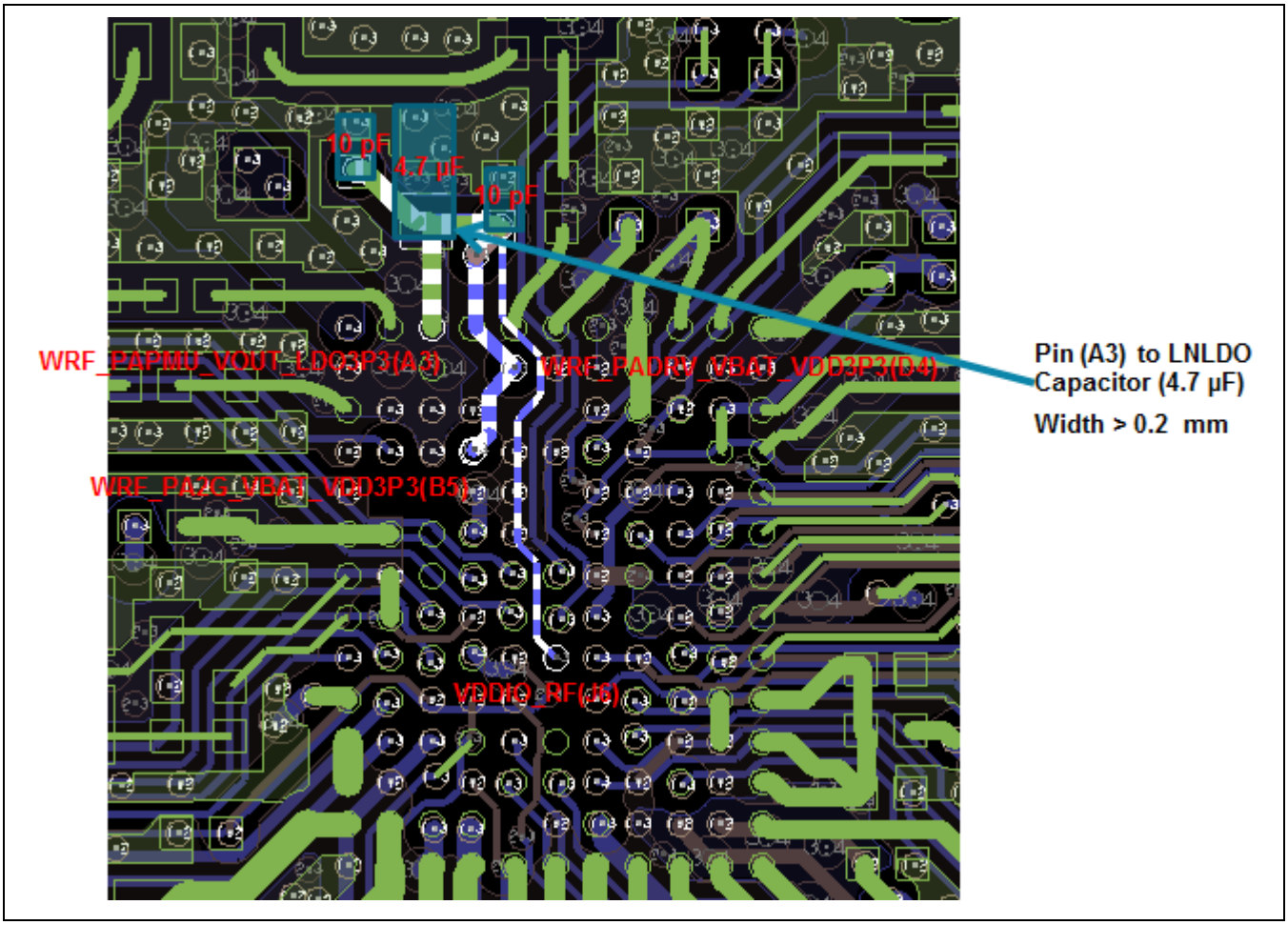
- GRM188R60J475ME84D (0603 X5R 4.7 µF 20% 6.3V Murata)
- GRM155R60J475ME87D (0402 X5R 4.7 µF 20% 6.3V Murata)

This capacitor has a typical self-resonance frequency = 3 MHz; impedance/ESR = 2 mohm. The ESR and ESL of the capacitor must be met to achieve good noise and transient performance.

7.6.1.2 Power Rail—VOUT_3P3

LDO_3P3 should have a star connection from each dedicated bypass capacitor to the pin.

Figure 17. Power Rail Showing Pin A3 to LNLDO Capacitor



7.7 PMU—PMU_CLDO

7.7.1 Component Selection

7.7.1.1 CLDO Output Capacitor

Nominal capacitance value is 1 µF.

- The effective capacitance should *not* drop more than 10% from the nominal value under 1.25V bias.
- The minimum C= 1 µF.

Recommended capacitors include:

- GRM188R60J105MA01 (0603 X5R 1 µF 20% 6.3V Murata)
- GRM155R60J105KE19D (0402 X5R 1 µF 20% 6.3V Murata)

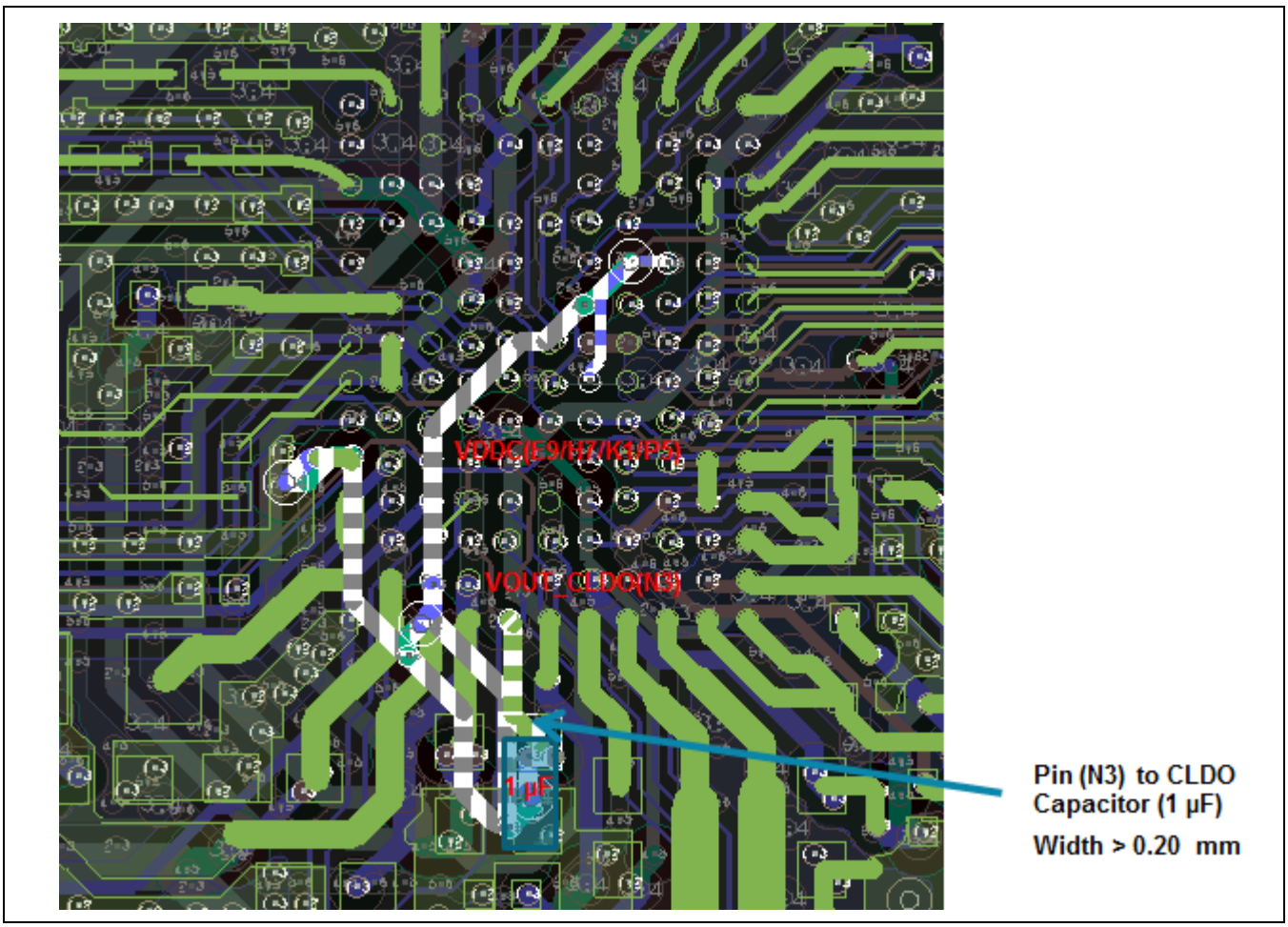
This capacitor has a typical self-resonance frequency = 3 MHz; impedance/ESR = 2 mohm. The ESR and ESL of the capacitor must be met to achieve good noise and transient performance.

7.8 Power Rail—CLDO

7.8.1 All Layer

The CLDO line should have a star connection routing from the source.

Figure 18. All Layer Showing Pin N3 to CLDO Capacitor



7.8.2 Component Selection

7.8.2.1 LNLDO Output Capacitor

The nominal capacitance value is 1 µF.

The effective capacitance should *not* drop more than 10% from the nominal value under 1.25V bias.

The minimum C = 1.22 µF.

Recommended capacitors include:

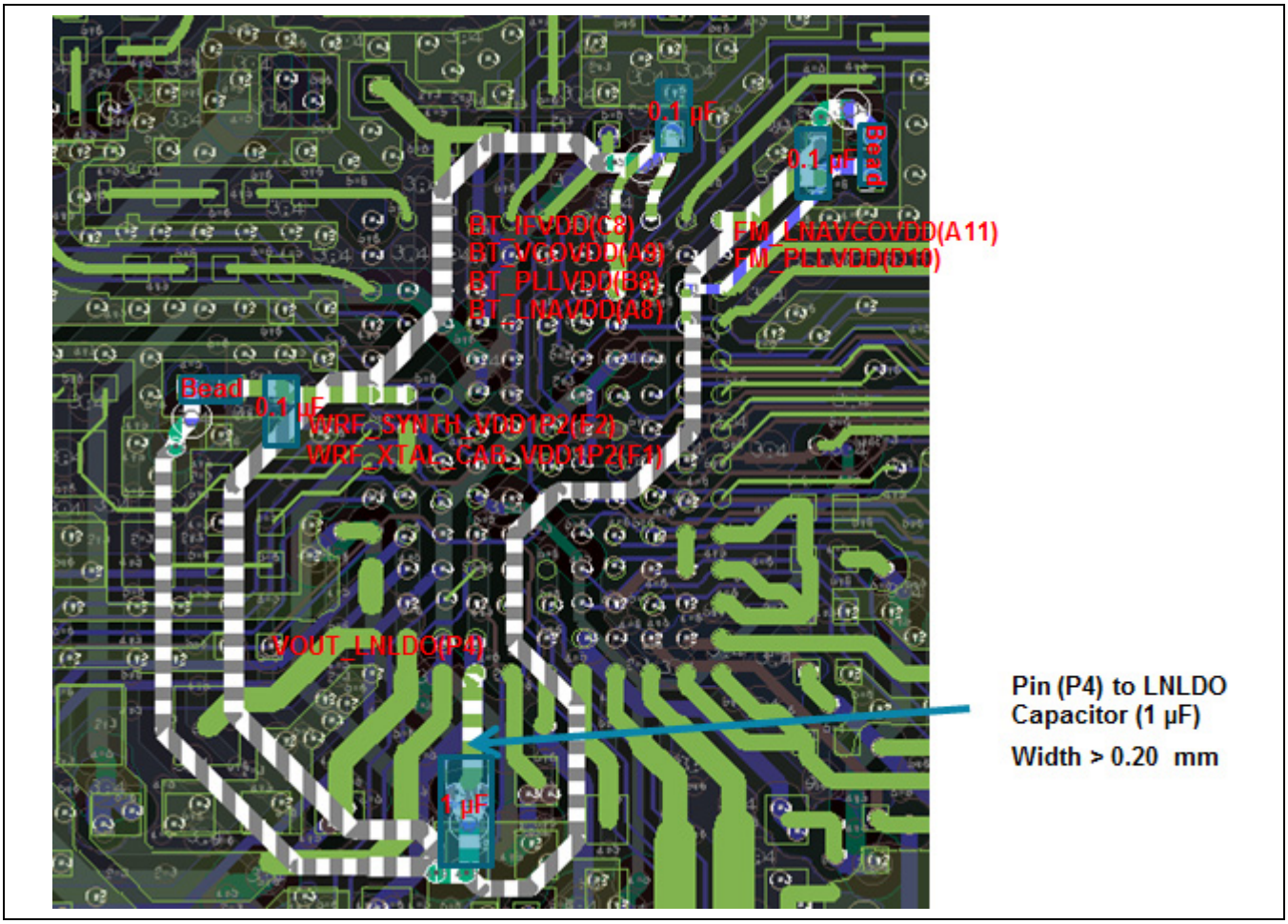
- GRM188R60J105MA01 (0603 X5R 2.2 µF 20% 6.3V Murata)
- GRM155R60J105KE19D (0402 X5R 2.2 µF 10% 6.3V Murata)

This capacitor has a typical self-resonance frequency = 4.8 MHz; impedance/ESR = 3.5 mohm. The ESR and ESL capacitance must be met to achieve good noise and transient performance.

7.9 Power Rail— VOUT_LNLDO

The LNLDO line should have a star connection routing from the source.

Figure 19. Power Rail Showing Pin 94 to LNLDO Capacitor



7.10 PMU—VOUT_2P5

7.10.1 Component Selection

7.10.1.1 LDO2P5 (VOUT_2P5) Output Capacitor

The nominal capacitance value is 2.2 µF.

The capacitance should *not* drop more than 41% from the nominal value under 2.5V bias.

The minimum C = 0.85 µF.

Recommended capacitors include:

- GRM188R61A225KE34 (0603 X5R 2.2 µF 10% 10V Murata)
- GRM155R60J225ME15 (0402 X5R 2.2 µF 20% 6.3V Murata)

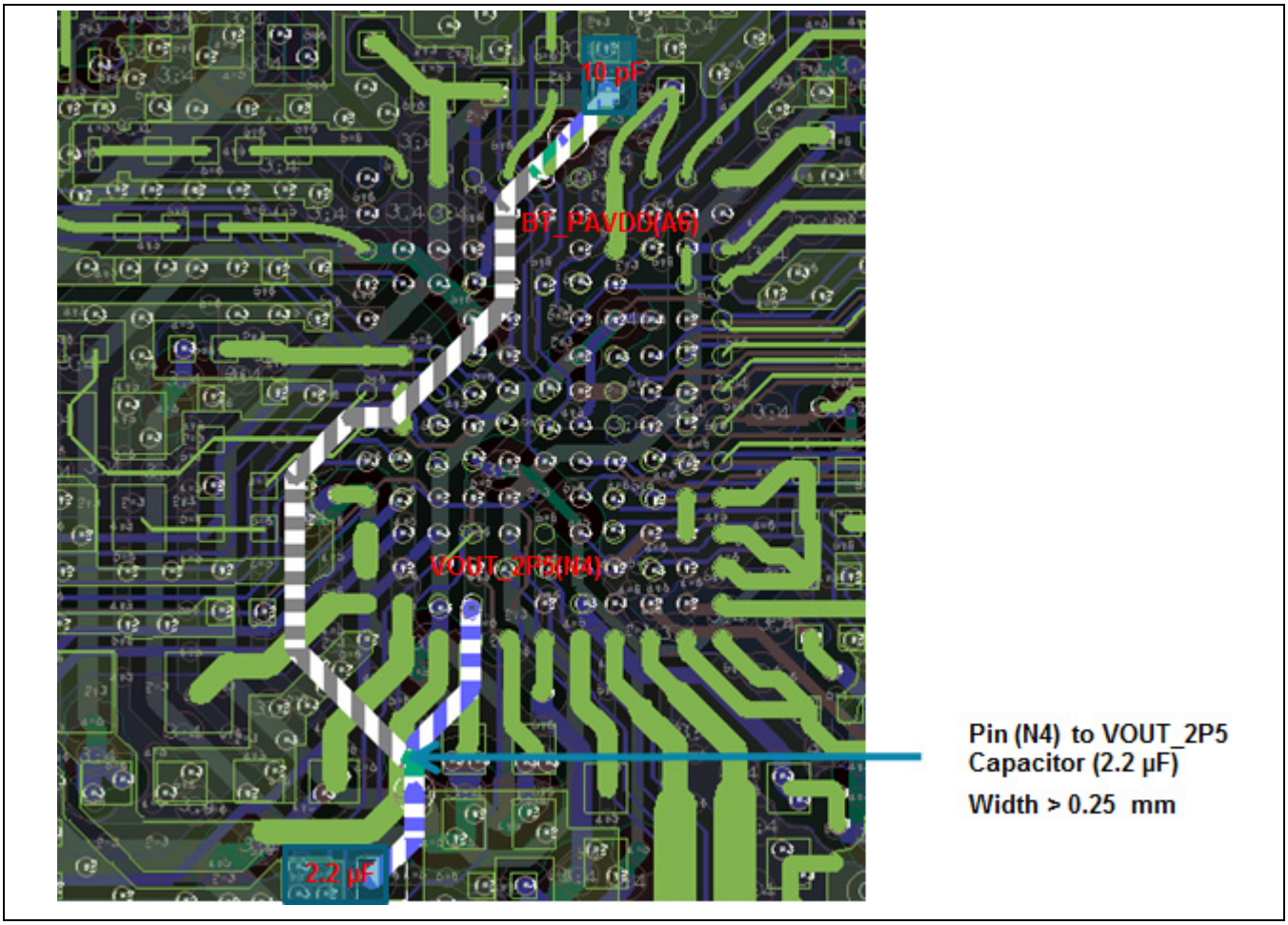
This capacitor has a typical self-resonance frequency = 4.8 MHz; impedance/ESR = 3.5 mohm. The ESR and ESL of the capacitor must be met to achieve good noise and transient performance.

7.11 PMU—BTLDO2P5

7.11.1 Power Rail—VOUT_2P5

The bypass capacitor (10 pF) should be placed close to pin A6 (BT_PAVDD).

Figure 20. Power Rail Showing Pin N4 to VOUT_2P5 Capacitor



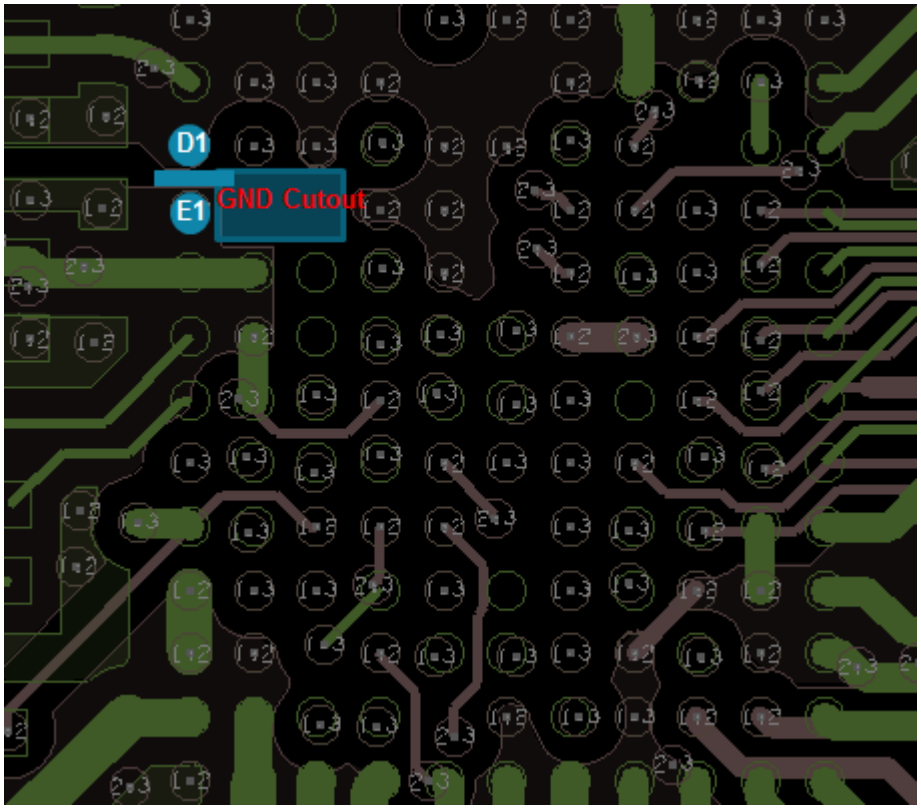
7.12 GND Cutout

A GND cutout is needed on layer 2, as shown in Figure 21.

On layer 2, pins D1 and E1 GND should be separated.

On layer 2, under Pin E2 and E3, GND should be cut out. If possible, the same GND cutting out on layer 3 is required.

Figure 21. GND Cutout on Layer 2



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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	03/05/2014	43340-AN300-R Initial release
*A	5478051	UTSV	10/17/2016	Updated in Cypress template. Added Cypress Part Numbering Scheme.
*B	5824595	AESATP12	07/19/2017	Updated logo and copyright.

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