AN214924

Printed Circuit Board and Module Layout Recommendations

Associated Part Family: CYW4329

This document provides key guidelines and recommendations for Cypress engineers and customers to follow when creating a CYW4329 layout.

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1 Introduction

This document provides key guidelines and recommendations to follow when creating a CYW4329 layout. It is strongly recommended that layouts be reviewed by the Cypress hardware applications engineering team before the PCB is released for fabrication.

Following the guidelines in this application note will lead to quicker reviews and fewer required corrections in the design. Designs that use the CYW4329 are typically portable devices with little PCB real estate. Therefore, the layouts can be challenging, and layout tradeoffs may have to be made between what is ideal and what is practical. Reviews with the Cypress application engineering team provide an excellent forum to discuss these design tradeoffs and their implications.

The following is a summary of the major items that are covered in detail in this application note. Each of these areas of the layout should be carefully reviewed against the provided recommendations before the PCB goes to fabrication.

- Top layout mistakes
- Power supply layout guidelines (including WLAN PA supply routing for PAA/PAG)
- System clock and sleep clock
- WLAN/Bluetooth RF placement and routing
- FM placement and routing

- Digital signal routing and integrity
- Special considerations for modules
- Other general layout guidelines
- Design for manufacturability (DFM)

1.1 Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM4329	CYW4329

1.2 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined upon first use. For a more complete list of acronyms and other terms used in Cypress documents, go to: http://www.cypress.com/glossary.

2 IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

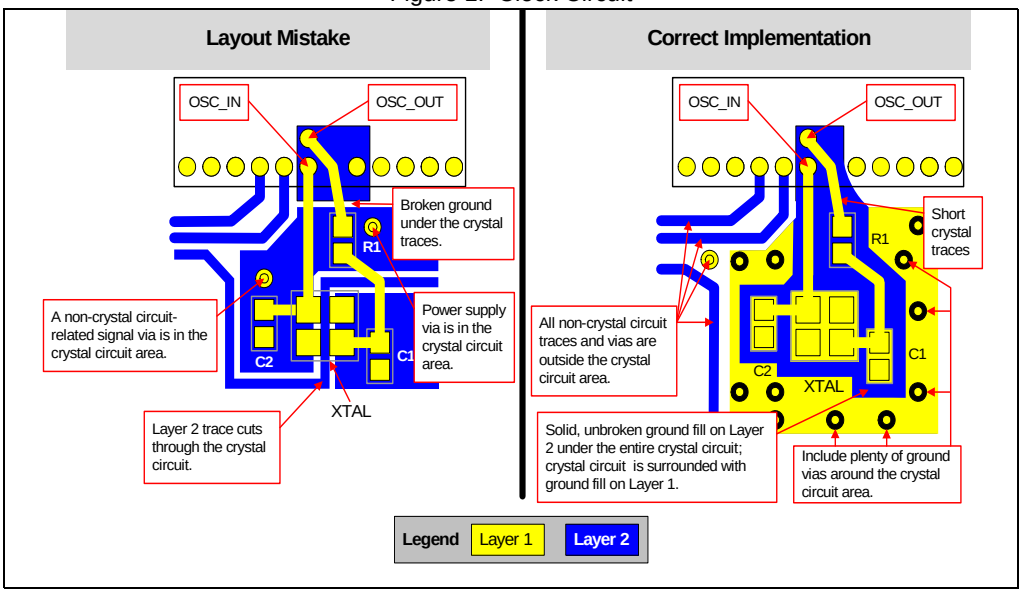
3 Top Layout Mistakes

This section describes some of the more common and serious layout mistakes. Some of the descriptions include illustrations that show both the mistakes and a recommended approach.

3.1 Common and Serious Layout Mistakes

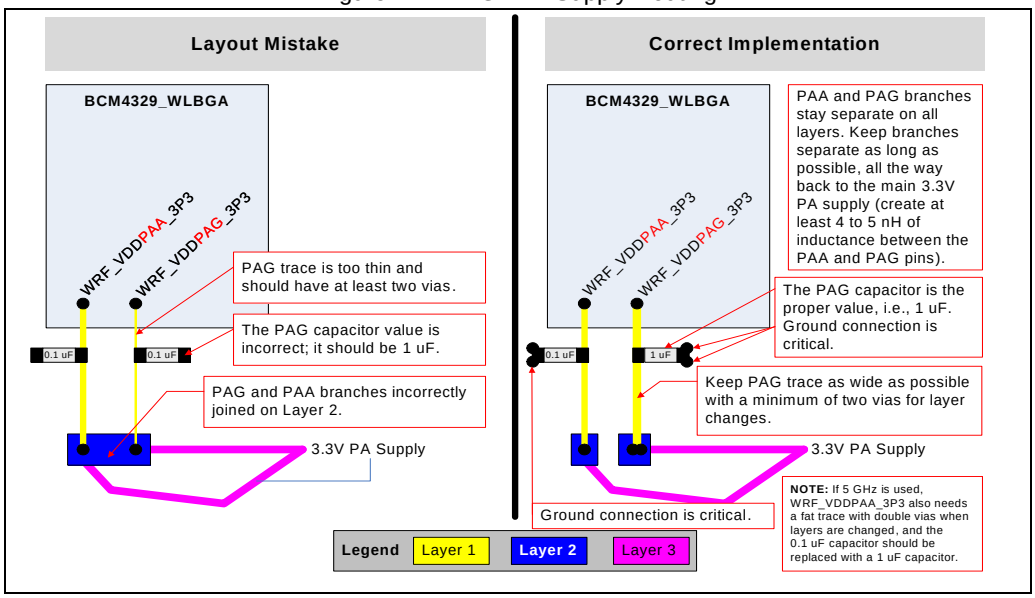
1. OSC_IN/OSC_OUT traces/circuits that are not completely isolated from noise sources or other sensitive signals with ground fill. Other issues are the crystal/TCXO not being adequately grounded, and designs where the crystal/TCXO is too far away from the CYW4329 (see Figure 2).

Figure 1: Clock Circuit



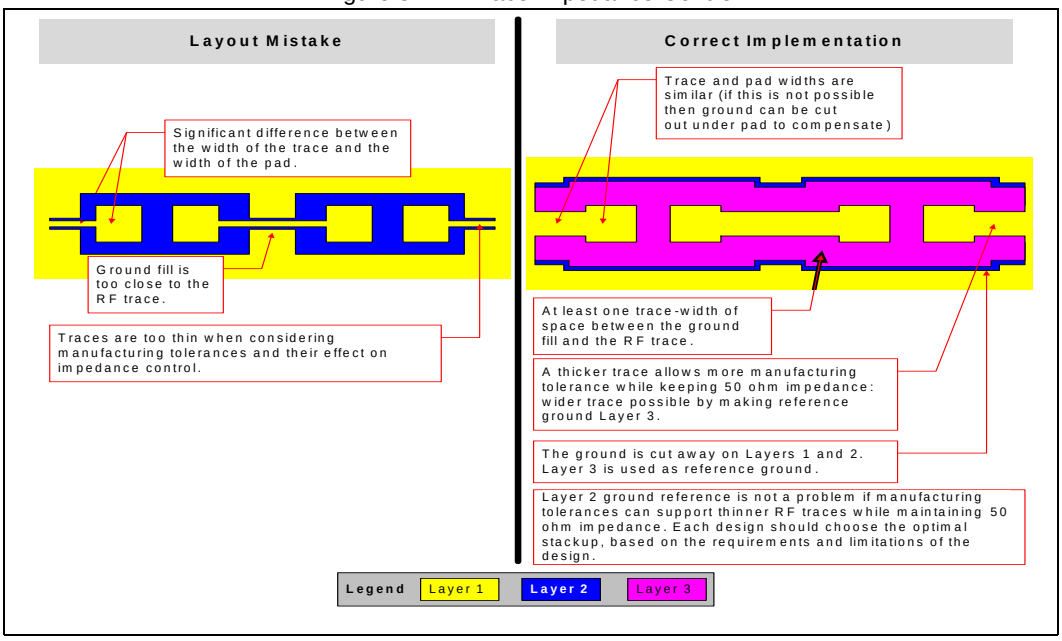
2. VDD_PAG_3P3 and VDD_PAA_3P3 that are not properly routed as branches from the 3.3V supply. One key mistake is branching on Layer 1, but then combining into a single net on Layer 2.
Other mistakes include not making the PAG trace wide enough or not having multiple vias if the PAG trace changes layers (see Figure 2).

Figure 2: WLBGA PA Supply Routing



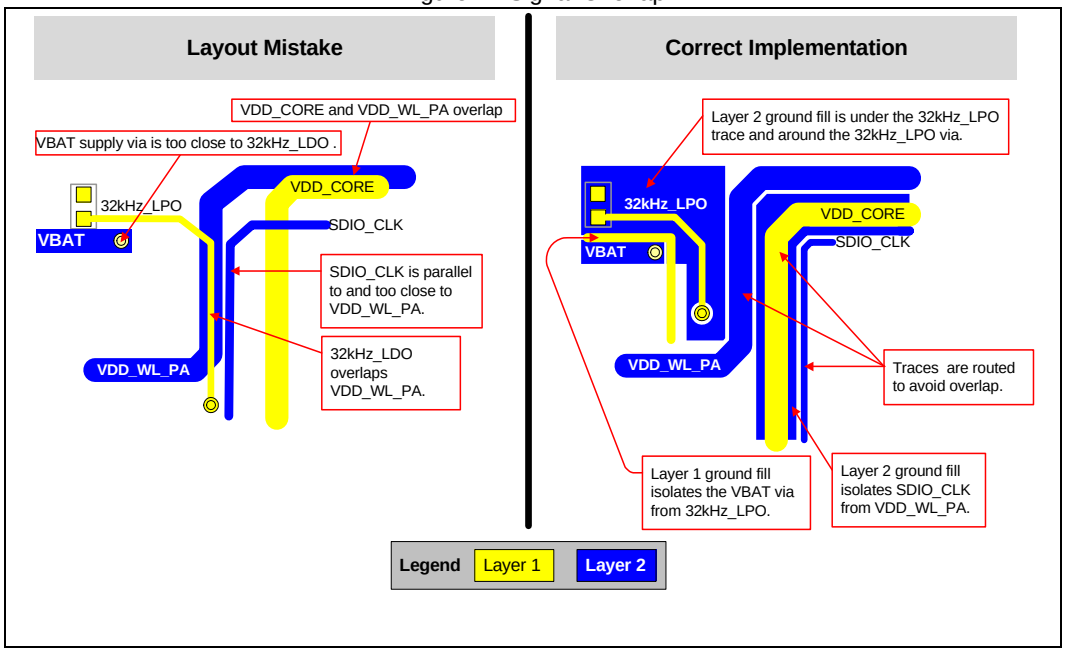
3. RF traces that are not truly 50 ohms because of stack-up mistakes, width differences between thin traces and wide pads, or because of the effect of manufacturing variances on extremely thin RF traces. Another detuning culprit is not having enough gap between an RF trace and the ground fill/shielding.

Figure 3: RF Trace Impedance Control



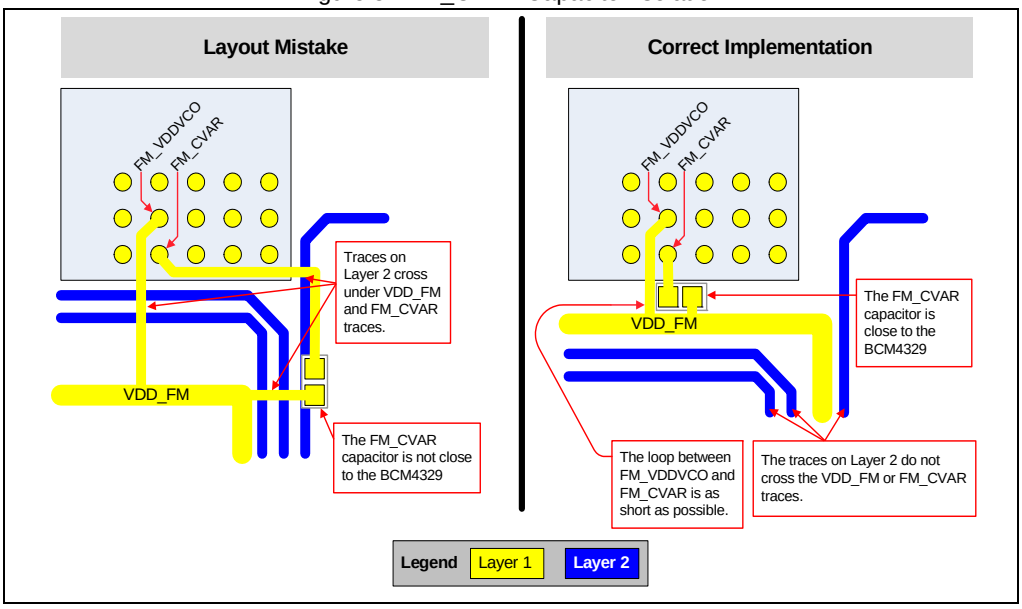
4. Overlap of sensitive signals or power supplies on adjacent layers. A common mistake is no isolation between a via of one supply/signal and the trace of another.

Figure 4: Signal Overlap



5. FM_CVAR capacitor is placed away from the chip and is not isolated from other signals.

Figure 5: FM_CVAR Capacitor Isolation



6. FM VDD lines cross other signals or are routed close to clock traces.
7. Power supply traces are not wide enough and use single vias when changing layers; see Power Supply Layout Guidelines on page 6 for recommendations. If the specified target width cannot be achieved because of size constraints in a given design, the traces should be made wide possible.
8. Power supply components (inductors and capacitors) are placed too far from the BCM4329; see Power Supply Layout Guidelines on page 6 for recommendations.
9. 32.768 KHz (LPO) clock traces/circuits are not completely isolated from noise sources or other sensitive signals with ground fill. TCXO itself is not grounded well. This issue is similar to mistake item #1 for the system clock.

4 Power Supply Layout Guidelines

4.1 EMI Reduction

To reduce EMI in the forward and return paths, the areas enclosed by the following loops must be minimized:

- SR_VLX1 to inductor and capacitor to SR_PVSS
- SR_PALDO to capacitor to SR_PAVSS
- SR_VBAT to supply bypass capacitors to SR_PVSS

These lines must be as wide and short as possible to maximize efficiency for large current flow (up to 1 amp transients are possible) and minimize line inductance.

Place the inductors and capacitors as close as possible to SR_VLX1 and SR_PALDO. Keep all RF, clock, and other sensitive analog lines as far away as possible from these lines.

4.2 CBUCK Inductor

- Use an inductor that meets the guidelines described in 4325-AN601-R.
- Keep the inductor as far away as possible from the RF section.
- Use the top layer for direct connection to SR_VLX1.
- Avoid using vias (they add excessive resistance and inductance).

4.3 CBUCK Output Capacitor

- Use a low ESR capacitor (less than 30-milliohms). A ceramic X5R capacitor is recommended.
- Ensure that the capacitor has a low-resistance connection to the ground plane by using more vias.
- Place the capacitor near the CBUCK output.

4.4 Switcher LDO Capacitor Connections

- Place one terminal of the SR_VSSPLDO capacitor close to the BCM4329 SR_VSSPLDO pin. The other terminal should have a short, low-resistance route to the SR_VDDBAT2 ball.
- Place one terminal of the SR_VDDNLDO capacitor close to the BCM4329 SR_VDDNLDO pin. Connect the other capacitor terminal to the ground plane with short, low-resistance traces.
- If vias are needed to access the supply/ground plane, use as many vias as possible.

4.5 PMU Grounding

Ground P13, R13, P11, P12, and P8 as a separate group; use multiple vias to ground the group to the common GND plane.

4.6 VBAT Input

- Use multiple module balls for VBAT, use a wide trace (0.5 mm or wider) for routing, use at least double-vias when changing PCB layers.
- Route VBAT from the module balls to the VBAT decoupling capacitor first (physically through its VBAT pin), and then route to any VBAT loads.
- The VBAT capacitor should be physically close to balls N13 and N14 and routed with wide, low-resistance, low-inductance traces to N13, N14, R12, R11,and T11. The purpose of placing this capacitor close to N13 and N14 is to absorb the switching current transients of the CBUCK switcher. In applications where the CBUCK switcher is not used (i.e., no external L & C), the VBAT capacitor should be placed physically close to balls R11 and T11 instead.Multiple Power/Ground Planes
- If large VBAT or ground planes are not possible, implement large, thick traces to avoid degrading the efficiency.
- If supply and ground balls must go through multiple planes, use as many vias as possible near the supply and ground chip balls.

4.7 Low-Noise LDO Band Gap Bypass Capacitor

- Keep the line from the VREF_LDO pin to its capacitor to the AVSS_LDO pin as short as possible and away or shielded from noisy signals. This signal is the low-noise reference for the low-noise LDOs.
- Use a thick route from VREF_LDO pin to its capacitor.
- Connect the capacitor to the ground plane directly. If vias are needed, use multiple vias.

4.8 PALDO Output (VDD_PA)

- Keep the VDD_PA decoupling capacitor as close as possible to the R10 and T10 balls on the BCM4329.
- Use wide traces (0.25 mm or wider) on the top layer for the trace from R10 and T10 to the VDD_PA capacitor; avoid layer changes.
- VDD_PA goes to the VDD_PA capacitor for decoupling and then goes to any loads. Use double-vias if layers are changed when routed away from the VDD_PA capacitor.
- VDD_PA is routed to VDDPAG (D1 ball), VDDPAA (A1 ball), BT PA (A12 ball), and VDDIO_RF (K7 and L7 balls). Try to use separate branches for these four different loads:
- VDDPAG and VDDPAA for WLAN PA: separate these branches as early as possible, use a 0.2 mm or wider trace for VDDPAG routing, and a 0.125 mm or wider trace for VDDPAA routing.
  The VDDPAG branch goes to a 1 μF capacitor for decoupling and then goes to the D1 ball. Put the 1 μF capacitor close to the D1 ball. The VDDPAA branch goes to a 0.1 μF capacitor for decoupling and then goes to the A1 ball. Put the 0.1 μF capacitor close to the A1 ball. Never short the D1 ball/1 μF capacitor branch with the A1 ball/0.1 μF capacitor branch; these two branches should be separated as much as possible.
- BT PA: use a 0.125 mm or wider trace for BT PA routing. This branch goes to a small-value decoupling capacitor and then goes to the A12 ball. Put the capacitor close to the A12 ball.
- VDDIO_RF: a 0.100 mm wide trace for this branch is sufficient. Ideally, the trace should go to its 0.1 μF decoupling capacitor first and then to balls K7 and L7.

4.9 CBuck Switcher Output

- Place the 3.3 uH inductor as close to the P14 and R14 balls as possible. Use a wide trace to connect the P14 and R14 balls to the 3.3 uH inductor. Avoid changing layers.
- Put the 4.7 μF capacitor close to the 3.3 uH inductor. Use a wide trace from the 3.3 uH inductor to the 4.7 μF decoupling capacitor before routing to the loads.
- Since the P14 and R14 balls, the 3.3uH inductor, and the 4.7 μF capacitor area has strong switching noise, keep other sensitive signals and power rails away from this area.
  Under this area, on layer 2, consider isolating the GND island for this area; use multiple vias to connect this GND island to the common GND plane.
  Try to avoid any traces on layer 3 (and deeper layers if possible) under this area.

4.10 2.5V LDO Output

Put the 1 μF capacitor close to the T12 ball and route power from the T12 ball to the 1 μF capacitor for decoupling before going to the load at the P4 ball.

4.11 CLDO Output

The VDD_CORE power rail is noisy and its traces need to be away from other sensitive signals and power rails.

- Place a 4.7 μF decoupling capacitor close to the T8 ball and route the power from the T8 ball to the decoupling capacitor for before going to a load.
- Use two branches:
- One for bt_vddc (L12 and M10 balls)
- One for wl_vdd (G8, L1,and T4 balls).
- For the E7 ball, use a small separate trace to add some isolation inductance.

4.12 LNLDO1 Output

The VDD_RADIO_PLL power rail is sensitive to noise and must be away from noisy signals (such as digital signals) and power rails (such as VDD_CORE).

- Place a 4.7 µF decoupling capacitor close to the T9 ball and route power from T9 to the decoupling capacitor for before going to a load.
- The trace going to A3 and B5 must be decoupled by a 0.1 µF capacitor, which must be close to the load (A3 and B5).

4.13 Power Rails From LNLDO1

The VDD_BT, VDD_PLL, and VDD_AFE power rails are branches from LNLDO1 and are all noise sensitive. Pay careful attention to their routing and put their decoupling capacitors close to the load balls; always decouple before going to the load.

4.14 LNLDO2 Output

The VDD_FM power rail is sensitive to noise and should be away from noisy signals (such as digital signals) and power rails (such as VDD_CORE).

- Place its 1 µF decoupling capacitor close to N11 and route the power trace from N11 to the capacitor before going to a load.
- Use two branches:
- one for E13 (fm_vddvco), FM TX DC bias, and the fm_cvar capacitor.
- One for the other FM power balls.

4.15 Other PMU balls

The P9, T13, and T14 balls should have their capacitors close to them and use wide traces. Keep the traces away from noise sources.

4.16 LDO Input and Output Capacitors

Place LDO input and output capacitors as close as possible to their respective balls. Otherwise, their ESR and any trace impedance may present stability and transient settling issues. These capacitors should have a good low-resistance connection to the supply/ground planes. If a via must be used, use multiple vias.

4.17 Switcher Output-to-Load Routing

For good load regulation, minimize the resistance of the power lines from the regulators to their respective loads by using wide, short power traces.

4.18 WLAN Power Amplifier Power Rails

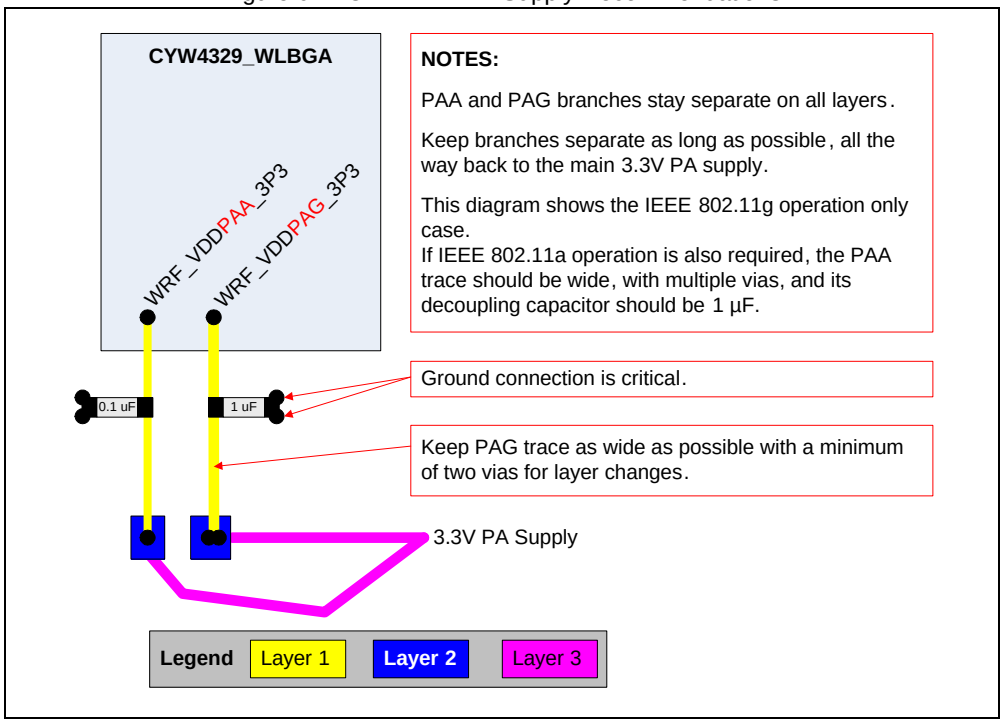
The routing of the 3.3V PA supply to the WRF_VDDPAA_3P3 (PAA) and WRF_VDDPAG_3P3 (PAG) balls is critical.

- The PAG balls are the main PA supply and require significant current. Therefore, make the traces to these balls as wide as possible and have at least two vias if changing layers is required. The PAA balls are lower current (approximately 30 mA), so a single via is adequate.

Note: If IEEE 802.11a operation is used, the PAA ball is also high current and should be fed with fat traces and multiple vias.

- Split the 3.3V source to these balls into two separate branches, one for the PAG ball, and one for the PAA ball. Start these two branches from the main 3.3V source as soon as possible so that there is as much distance/inductance between them as possible. The separation between the two branches should be long enough to create at least 4 to 5 nH of inductance.
- Place a 1 µF decoupling capacitor as close as possible to the CYW4329 PAG pin. Place a 0.1 µF decoupling capacitor as close as possible to the CYW4329 PAA pin. If IEEE 802.11a operation is used, then use a 1 µF capacitor for the PAA pin instead. See Figure 6 for more details. Make sure there is a good ground connection on the ground side of the decoupling capacitors. Use multiple vias where possible.

Figure 6: BCM WLAN PA Supply Recommendations



5 System Clock and Sleep Clock

Follow these steps to minimize the influence of noise on the crystal and phased locked loop (PLL) block. These items are also important to avoid spurs related to the clock from negatively impacting RF performance. Most of these recommendations are also applicable to the 32.768 kHz sleep (LPO) clock:

- Ideally the crystal/clock traces and associated components should be on the same layer as the CYW4329 so that there are no vias or layer changes. The layer adjacent to the circuit should be a solid ground plane that covers the entire clock circuit. The area surrounding the circuit (on the same layer as the circuit) should be ground filled with plenty of vias.
- Ensure that the system clock (e.g., 38.4 MHz) traces going to the CYW4329 (including the crystal itself) are well shielded by ground. There should be no cutoff or broken ground plane underneath the crystal or the system clock traces.
- Ensure that crystal traces are as short as possible.
- Make sure that coupling from noisy signals is minimized, as the crystal traces are extremely sensitive to noise. Check for vias on these traces coming close to noisy signals on other layers. Avoid noise currents on planes near these traces by placing decoupling capacitors to guide currents away from these traces. No digital signals should be routed near the crystal circuit.
- Minimize noise ingress from the digital ground plane by keeping the VSS_XTAL return close to the VSS_XTAL pin (trace to ground plane must be short) and separate this pin from other digital supply decoupling capacitor grounds.
- Place a bypass capacitor close to VDD_XTAL to reduce ripple on this supply pin. This will help minimize phase noise from coupling into the PLL block.

6 WLAN/Bluetooth RF Placement and Routing

6.1 General RF Guidelines

Follow these steps for optimal WLAN and Bluetooth performance.

1. Control Bluetooth and WLAN 50 ohm RF traces by doing the following:

- Route traces on the top layer as much as possible and use a continuous reference ground plane underneath them.
- Verify trace distance from ground flooding. At a minimum, there should be a gap equal to the width of one trace between the trace and ground flooding. Also keep RF signal lines away from metal shields (consider X, Y, and Z planes). This will ensure that the shield does not detune the signals or allow for spurious signals to be coupled in.
- Consider manufacturing tolerances when choosing trace widths. Generally RF traces will be on the top layer with the second layer used as a reference ground. Depending on the stack-up of the PCB, manufacturing tolerances may lead to very thin RF traces that cannot be controlled to 50 ohm. If this is the case, then consider using layer 3 as the reference ground, since this will allow for wider traces. If layer 3 is used as the reference ground, then make sure that layer 2 follows the same ground keep-outs as layer 1.
- For optimal impedance control, consider using a different reference ground layer for components with wide pads than that used for traces. For example, if layer 2 is used as the reference ground for thin RF traces, consider voiding layer 2 under components with wide pads and using layer 3 as the reference ground for these wide pads.
- Keep all trace routing inside the ground plane area by at least the width of a trace.
- Check for RF trace stubs, particularly when bypassing a circuit. This applies, for example, to a layout that provides the option for using an external LNA circuit or bypassing that circuit with series RF capacitors.

2. Keep RF traces properly isolated by doing the following:

- Do not route any digital or analog signal traces between the RF traces and the reference ground.
- Keep the balls and traces associated with RF inputs away from RF outputs. If two RF traces are close each other, then make sure there is enough room between them to provide isolation with ground fill.
- Use ground flooding on the top and bottom layers in the RF area with plenty of ground stitch vias. Use *stitching* in a staggered pattern with a minimum via spacing of 32 mil (via to via, 25-mil offset) and a maximum spacing of 100 to 150 mil. Also use flooding on sensitive trace layers. After ground flooding, terminate shapes and corners with vias to tie to other planes for improved EMI performance.
- Verify that there are plenty of ground vias in the shield attachment area. Also verify that there are no non-ground vias in the shield attachment area. Avoid traces crossing into the shield area on the shield layer.

3. Consider the following RF design practices:

- Confirm antenna ground keep-outs.
- Ensure that the shield attachment area is clear of solder mask and that it only has ground vias.
- Verify that the RF path is short, smooth, and neat. Use curved traces or microwave corners for all turns; never use 90-degree turns. Avoid width discontinuities over pads. If trace widths differ significantly from component pad widths, then the width change should be mitered. Verify there are no stubs.
- Do not use thermals on RF traces because of their high loss.

6.2 WLAN Receive Sensitivity

Follow these steps to optimize WLAN receive sensitivity:

- Place a bypass capacitor close to the WRF_VDDRX_1P2 pin to help reduce ripple into it.
- Place the filter capacitors on the RF switch control lines close to the RF switch component to form a good RC filter. Note that these capacitors may or may not be needed, depending on the layout.

6.3 Bluetooth Receive Sensitivity

Since Bluetooth and WLAN share a common RX Path, any issue affecting WLAN sensitivity will also affect Bluetooth sensitivity. For designs with external LNA, care must be taken when choosing external LNA gain and performance to ensure that all Bluetooth RX specifications (most importantly maximum input power and C/I) are met.

6.4 Bluetooth Transmit Sensitivity

To optimize the Bluetooth TX power level and power flatness, place the capacitor to ground very close to the BT_RFOP pin. The capacitor value may need to be tuned, depending on the layout.

The BT_VDDTF pin needs to be properly decoupled. For most designs, a 10 pF capacitor is adequate. An additional 0.1 µF capacitor might be needed, depending on the quality of the BT_VDDTF supply. Improper decoupling of this pin will cause degradation in DEVM.

6.5 FM Placement and Routing

To optimize FM sensitivity and SNR:

- The 32.768 KHz clock is the reference frequency for the FM VCO Block and should be clean and stable. Ensure that this clock trace is well isolated from all noisy signals. Shield this trace with ground planes on the top and bottom layers and ground pour around it. Keep the length of the trace as short as possible.
- Place the capacitor that is connected to FM_CVAR close to the pin. This capacitor is a critical part of the VCO circuitry and needs to be well isolated from all noisy signals.
- Make sure that the VDD_FM supply balls have appropriate decoupling capacitors close to their input balls. Values of.01 µF and.1 µF are recommended for most layouts.
- DC blocking capacitors are necessary on the FM_AUDIO_OUT1 and OUT2 balls. Their values must be adjusted to create the optimum low frequency audio coverage, based on the audio PA input impedance.
- Keep FM VDD and RF traces away from the system clock traces (i.e., 38.4 MHz clock) and all other noisy signals including: UART, PCM, I^2S, SDIO.
- Ensure that the amplitude of the 32.768 KHz clock is kept below 1.8V p-p. Exceeding this limitation will affect FM performance.
- The characteristic impedance recommended for FM antenna traces is 50 ohms.
- Shield the FM TX/RX audio signals, using ground fill on the same and adjacent layers; keep the grounds away from digital signals, clocks, and other noise sources.
- DC blocking capacitors and shunt bypass capacitors are necessary on the FM_TXADCIN1 and IN2 balls. All four capacitors should be placed close to these balls to optimize SNR.

6.6 RF Grounding

WLAN/Bluetooth/FM ground pins should not be connected to each other on the PCB top layer directly under the chip. These CYW4329 ground pins should be routed directly to the common ground layer of the PCB; layer two (immediately under the top PCB layer) is recommended for this purpose.

The following BCM4329 WLAN/BT/FM ground pins should be connected to the common ground layer:

- A2, A9, A10
- B6, B8
- C2, C3, C12
- D2, D5, D8, D9, D10, D11, D12
- E2, E6, E12
- F10, F11
- G1, G10, G13
- H4
- J7
- K10
- L13
- M4

If the WLAN 802.11a option is not used, then both pins A4 "WRF_RFINP_A1" and A5 "WRF_RFINN_A1_XFMR" should also be connected to the common ground layer.

If the FM option is used:

- Pin E12 "FM_VSSVCO" *must* be connected with the ground via directly to the common ground layer. Do not connect pin E12 to any other ground pins on the top layer.
- A clearance area (as shown in Figure 6.7) under the CYW4329 *must* be maintained. This area applies only to the top PCB layer directly beneath the CYW4329 between pins E12, E13, F12, and F13. The E12 GND via should be slightly offset away from the clearance area.

Figure 7: Clearance Area Under the CYW4329



6.7 Digital Signal Routing and Integrity

- If Layer 1 and Layer 2 are selected for digital signal routing, it is important that no signal traces are routed underneath external components such as bypass capacitors, power rail filtering beads, etc. Otherwise, noise coupling may occur.
- To improve SDIO signal integrity, ensure that at least one bypass capacitor is placed close to the VDDIO_SD power balls to help reduce ripple on the SDIO interface when operating in high-speed mode.
- Keep SDIO traces away from all clock lines and noisy power supply components such as the switcher inductors. Avoid crossing over power supplies or ground discontinuities. Ideally, the SDIO traces should have a solid ground on the layer adjacent to them. Of key importance is the SDIO clock routing.
- Keep I^2S, PCM, and Bluetooth UART signals away from noise sources or other sensitive signals.

7 Special Considerations for Modules

- In the case of modules, generally the top side of the substrate contains all the components, and the bottom side is used for module pins that allow connection of the module to the device motherboard. It is recommended that the layer adjacent to this bottom “pin layer” be kept free of sensitive and noisy signal routes. Ideally, it would be a ground plane. This is important so that the module will be more robust and immune to noise coupling with any routing on the motherboard that may need to run under the module. Ideally, the motherboard would be routed in such a way that all unrelated sensitive or noisy signals are routed away from where the module is located on the motherboard. If the motherboard only has a few layers, however, this type of routing may not be possible because of the limited routing layers.
- Make sure that routes on the layer adjacent to the bottom “pin layer” of the module do not route over module pins, thereby introducing potential noise coupling paths.
- When deciding on module pin-out, follow these recommendations:
- Optimize module pin locations not only for CYW4329 to module pin routing on the module substrate, but also consider motherboard routing and fan-out of signals from module pins.
- Where possible, surround RF and clock module pins with ground pins.
- Make sure the module has enough ground pins and/or ground lugs.

8 Additional General Layout Guidelines

Follow these guidelines to obtain good signal integrity and avoid EMI:

1. Place components and route signals using the following design practices:

- Keep analog and digital circuits in separate areas. Route noisy digital signals away from sensitive analog signals. Choose component placement locations carefully, since proper placement and isolation can help avoid many noise and EMI problems.
- Identify all high-bandwidth signals and their return paths. Treat all critical signals as current loops. Check each critical loop area before the board is built. A small loop area is more important than short trace lengths.
- Refrain from routing any signals (analog or digital) over non-contiguous power or ground planes to avoid impedance interruptions that result in reflections and possible EMI increases. Do not route a trace across a return-plane gap, since this may cause ringing and magnetic crosstalk problems.
- Orient adjacent-layer traces so that they are perpendicular to one another to reduce crosstalk.
- Keep critical traces on internal layers, where possible, to reduce emissions and improve immunity to external noise. However, RF traces should be routed on outside layers to avoid the use of vias on these traces.
- Keep all trace lengths to a practical minimum. Keep traces, especially RF traces, straight wherever possible. Where turns are necessary, use curved traces or two 45-degree turns. Never use 90-degree turns.

2. Consider the following with respect to ground and power supply planes:

- Route all supply voltages to minimize capacitive coupling to other supplies. Capacitive coupling can occur if supply traces on adjacent layers overlap. Supplies should be separated from each other in the stack-up by a ground plane, or they should be coplanar (routed on different areas of the same layer).
- If any power supply trace or shape needs to change layers from a layer referencing (adjacent to) the top ground plane to the bottom ground plane in the stack-up or vice versa, an equal number of ground vias should be interspersed with, or placed immediately adjacent to, the vias carrying the supply voltage. This minimizes noise coupling from the supply to nearby signals and other supplies.
- Give equal attention to respective current return paths. Always design current return paths for the best electromagnetic compatibility. Isolate analog and digital grounds, and connect them together only where common signals travel between the two groups.
- Provide an effective ground plane. Keep ground impedance as low as possible. Provide as much ground plane as possible and avoid discontinuities. Use as many ground vias as possible to connect all ground layers together. Also, use more than one via to connect large sections of ground pours together. Do not break up or split ground planes. Stack ground planes adjacent to the power planes to maximize the inner plane capacitance.
- Maximize the width of power traces. Verify that they are wide enough to support target currents, and that they can do so with margin. Verify that there are enough vias if the traces need to change layers.

3. Consider these power supply decoupling practices:

- Place decoupling capacitors near target power balls. If possible, keep them on the same side as the IC they decouple to avoid vias that add inductance. If a filter component cannot be directly connected to a given power pin with a very short and fat etch, do not connect it by a copper trace. Instead, make the connection directly to the associated planes using vias.
- Use appropriate capacitance values for the target circuit, and consider the self-resonant frequency of each capacitor. For example, 2.4 GHz decoupling must use capacitors that are less than 10 pF. Digital decoupling typically uses 0.1 μF and 1000 pF capacitors with bulk capacitors in the range of 10 μF.

9 Design for Manufacturability

- Review the layout with the contract manufacturer DFM expert as early as possible in the process. Some DFM requirements conflict with the circuit requirements and cannot be implemented. However, where possible, DFM considerations should be implemented early to avoid schedule disruption and to improve yield and quality.
- Verify that there is no solder mask on the RF shield attachment area (both top and bottom).
- Verify that there are no silk screen markings on vias or pads.
- Confirm that height requirements are not violated. Verify maximum height specifications in component data sheets. This is especially critical in the shield areas.
- Confirm correct pad sizes and sufficient spacing between components.
- Avoid using dual-function pads (i.e., a pad that supports both 0402 and 0603 components). While this type of pad provides procurement flexibility, it often leads to manufacturability and quality issues.

Document History Page

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	-	11/25/2008	4329-AN100-R Initial Release
*A	-	-	12/14/2010	4329-AN101-R **Added:RF Grounding**
*B	5453249	UTSV	09/28/2016	Added Cypress Part Numbering Scheme and Mapping Table. Updated in Cypress template
*C	5834576	BENV	07/27/2017	Updated logo and copyright

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