AN214856

Printed Circuit Board Layout Guidelines

Associated Part Family: CYW89071

This document describes the layout guidelines for a low-cost PCB based on the CYW89071 WLBGA.

1 About This Document

1.1 Purpose

This document describes the layout guidelines for a low-cost PCB based on the CYW89071 WLBGA.

1.2 Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM89071	CYW89071

1.3 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use. For a more complete list of acronyms and other terms used in Cypress documents, go to: http://www.cypress.com/glossary.

2 IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

3 PCB Stackup

The typical mobile stackup for an 8-layer board is shown in Figure 1.

Figure 1. Typical Mobile Stackup (8-Layer Board)

							Via in Pad	Through Hole
						Drill Hole Size	5	8
						Land Size	10	18
Copper	**Layer**	**Thickness (mils)**	**Dk**	**50 ohms Microstrip (mils)**	**50 ohms Microstrip (mils)**	**Sig/Plane**	**Drill 1**	**Drill 2**
0.5 oz Cu plate up to 1 oz	L1	2.1		6.5 (Ref to L2)	14.4 (Ref to L3)	Sig	L1	L1
	Substrate	4.4	4.3					
0.5 oz Cu	L2	0.7				Sig/GND	L2	
	Substrate	4.4	4.3					
0.5 oz Cu	L3	0.7				GND		
	Substrate	4.4	4.3					
0.5 oz Cu	L4	0.7				Sig/Pwr/GND		
	Substrate	4.4	4.3					
0.5 oz Cu	L5	0.7				GND		
	Substrate	4.4	4.3					
0.5 oz Cu	L6	0.7				Sig/GND		
	Substrate	4.4	4.3					
0.5 oz Cu	L7	0.7				GND		
	Substrate	4.4	4.3					
0.5 oz Cu plate up to 1 oz	L8	2.1				Sig		L8
Total Board Thickness		39.9						

4 SMO Opening

The recommended pad size is 9.8 mils with a solder mask opening (SMO) of 9.8 mils. These recommendations ensure that solder will not bridge over to neighboring pads.

5 Blind Vias

The CYW89071 WLBGA requires L1-to-L2 vias in the pads to fan out signals onto layer 2. The vias should be plated with copper to form a rigid via. The recommended via drill size is 5 mils with a land size of 10 mils.

6 Critical Part Placement Requirements

The schematic design shown in Figure 2 on page 3 bypasses the HV-LDO. When making determinations about part placement on the PCB, the following requirements must be met:

- The VDDTF pin (B7) must have capacitor C8 (10 pF) placed as close as possible to the pin. The capacitor should have its own GND via return that is close to the capacitor GND pad. This ensures optimum RX sensitivity performance. For more details, see Figure 2 on page 3 and Figure 3 on page 4.
- The VDDRF pin (E7) must have capacitor C7 (10 pF) as close as possible to the pin. The capacitor should have its own GND via return that is close to the capacitor GND pad. For more details, see Figure 2 on page 3 and Figure 3 on page 4.
- The VDDPX pin (F7) must have capacitor C6 (0.01 µF) as close as possible to the pin. The capacitor should have its own GND via return that is close to the capacitor GND pad. For more details, see Figure 2 on page 3 and Figure 3 on page 4.

- The VREG supply output from the main LDO requires C5 to be a minimum of 1 µF for the LDO to work properly. A ceramic type capacitor is preferred because of its low ESR value.
- The VDDC1 and VDDC2 pins require a bead to isolate the baseband noise from leaking into the VREG, VDDPX, and VDDRF supplies.
- The RES pin (D6) requires R1 (15 kΩ @ 1% tolerance) to be placed as close as possible to the pin. This is a high-impedance input that can pick up noise. The pin is used for the RF calibration.
- The TM2 pin must be grounded (see Figure 4 on page 4). It can be connected to the VSS pin (B6) on the top layer to minimize the GND via connection.

Figure 2. Circuit Schematic

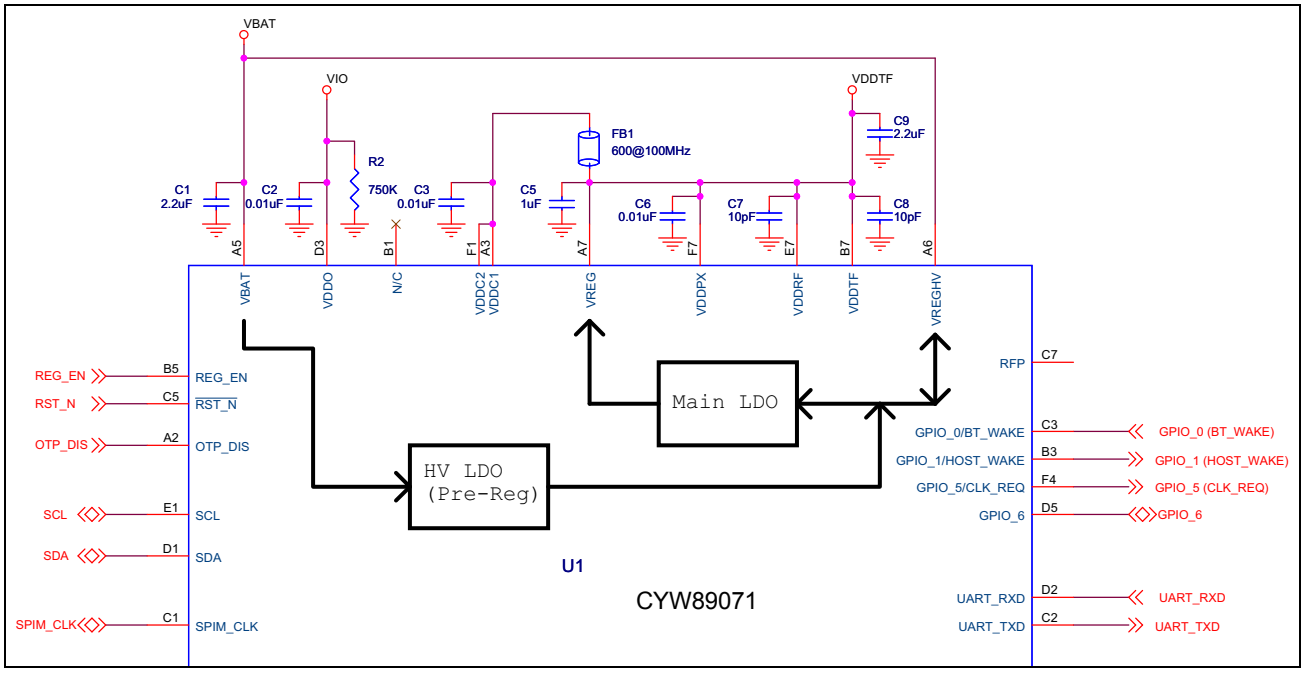


Figure 3. Vias on the PCB

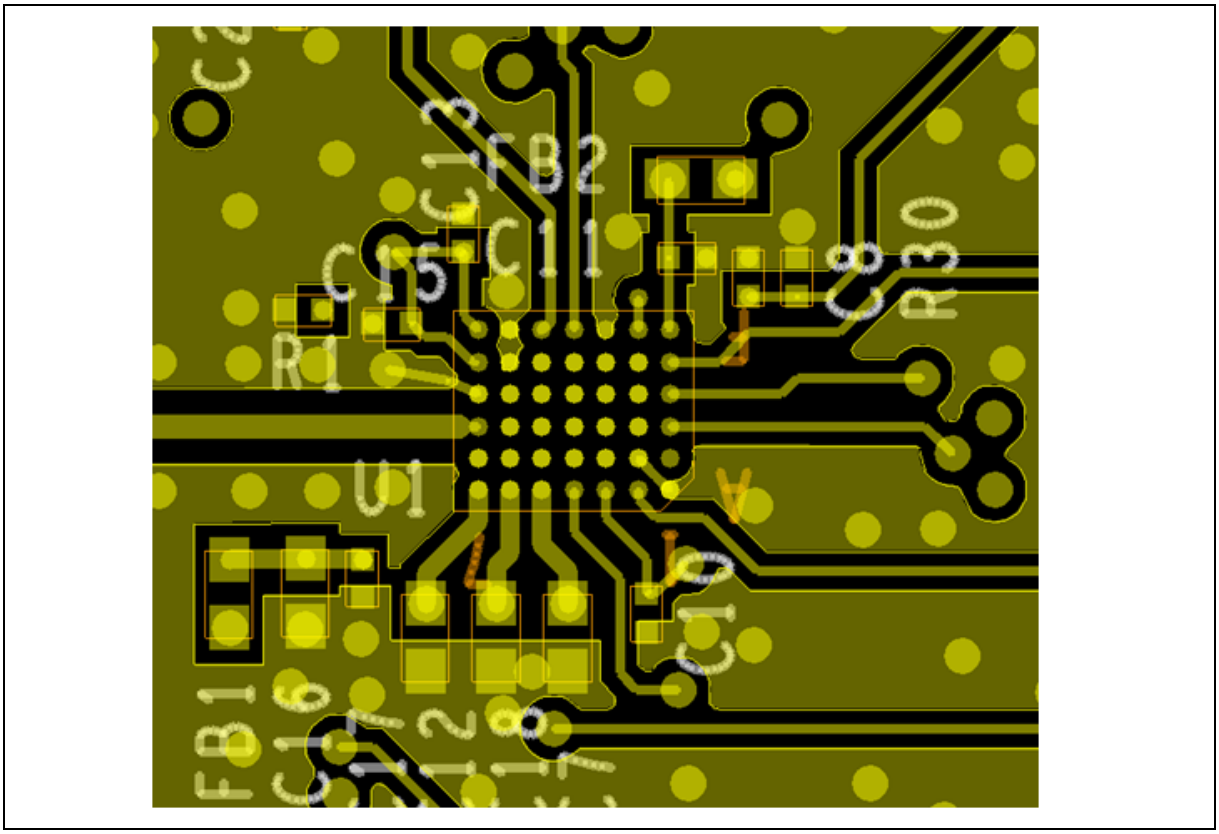
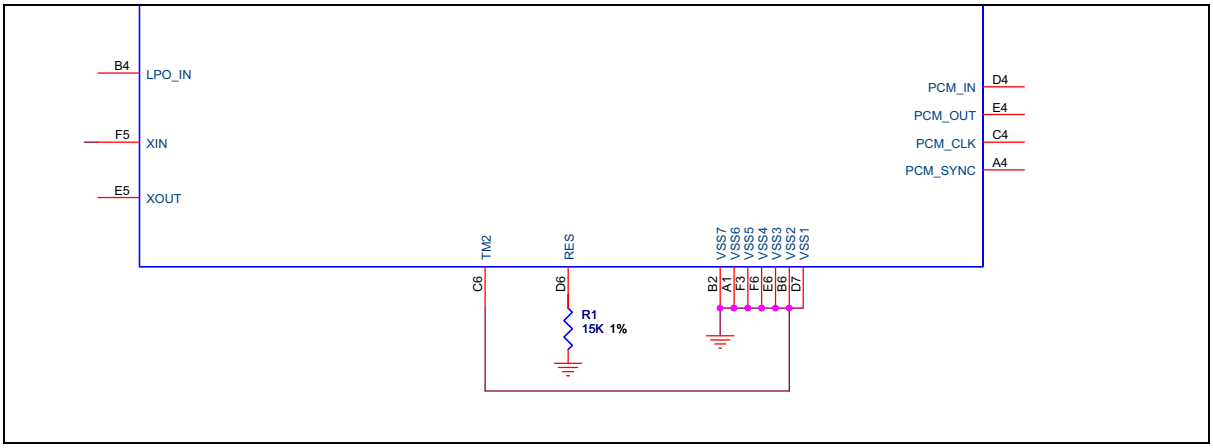


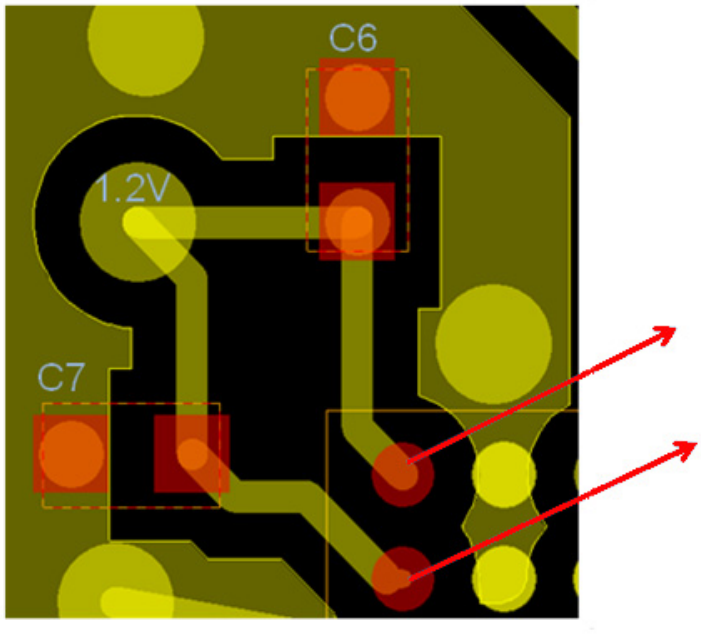
Figure 4. TM2 and VSS Pin Grounding



7 VDDRF and VDDPX Routing

VDDRF (pin E7) and VDDPX (pin F7) must be routed in a star configuration, which means each pin must be routed to its own decoupling capacitor before being connected to the 1.2V supply (VREG). This helps to optimize in-band spurious performance. See Figure 5 for details.

Figure 5. VDDRF and VDDPX Routing



8 Clock Routing

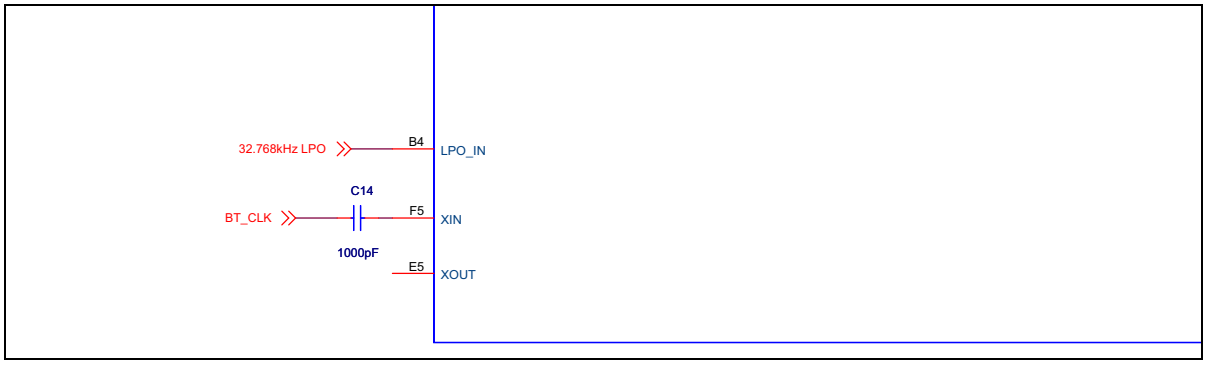
8.1 Clock Signal Input

The clock signal input into the XIN pin must be routed such that it does not interfere with or pick up noise from any other signals. If the clock is routed on the top layer, then layer 2 should be a solid ground plane underneath the clock trace. The top layer ground pull-back on the clock trace should have a minimum 1× the clock trace width to the ground. There should be ground stitching alongside the clock trace. If the clock is routed on layer 2, then there should be a ground plane on the top and lower layer to form a stripline. Keep a minimum of 3× the clock trace width to any other traces.

8.2 Sleep Clock

The sleep clock (32.768 kHz) must be routed such that it does not interfere with or pick up noise from any other signals. If the clock is routed on the top layer, then layer 2 should be a solid ground plane underneath the clock trace. The top layer ground pull-back on the clock trace should have a minimum 1× the clock trace width to the ground. There should be ground stitching alongside the clock trace. If the clock is routed on layer 2, then there should be a ground plane on the top and lower layer to form a stripline. Keep a minimum of 3× the clock trace width to any other traces.

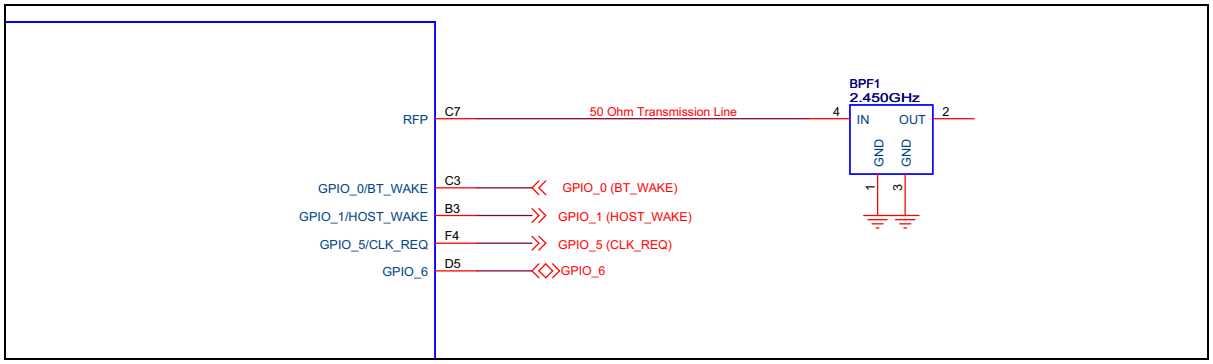
Figure 6. Clock Routing



9 RF Trace Routing

The RF trace routed out of the RFP pin (C7) is required to have an impedance of 50 ohms. It is preferable to keep the RF trace on the top layer and have the trace referenced to the ground plane on layer 3. Therefore, layer 2 is cut out under the RF trace. Referencing the RF trace to layer 3 allows a good trace width of 14.4 mils to run on the top layer. The 14.4-mil trace width helps minimize insertion loss of the trace compared to a thinner trace, and also minimize impedance transitions at the component pads.

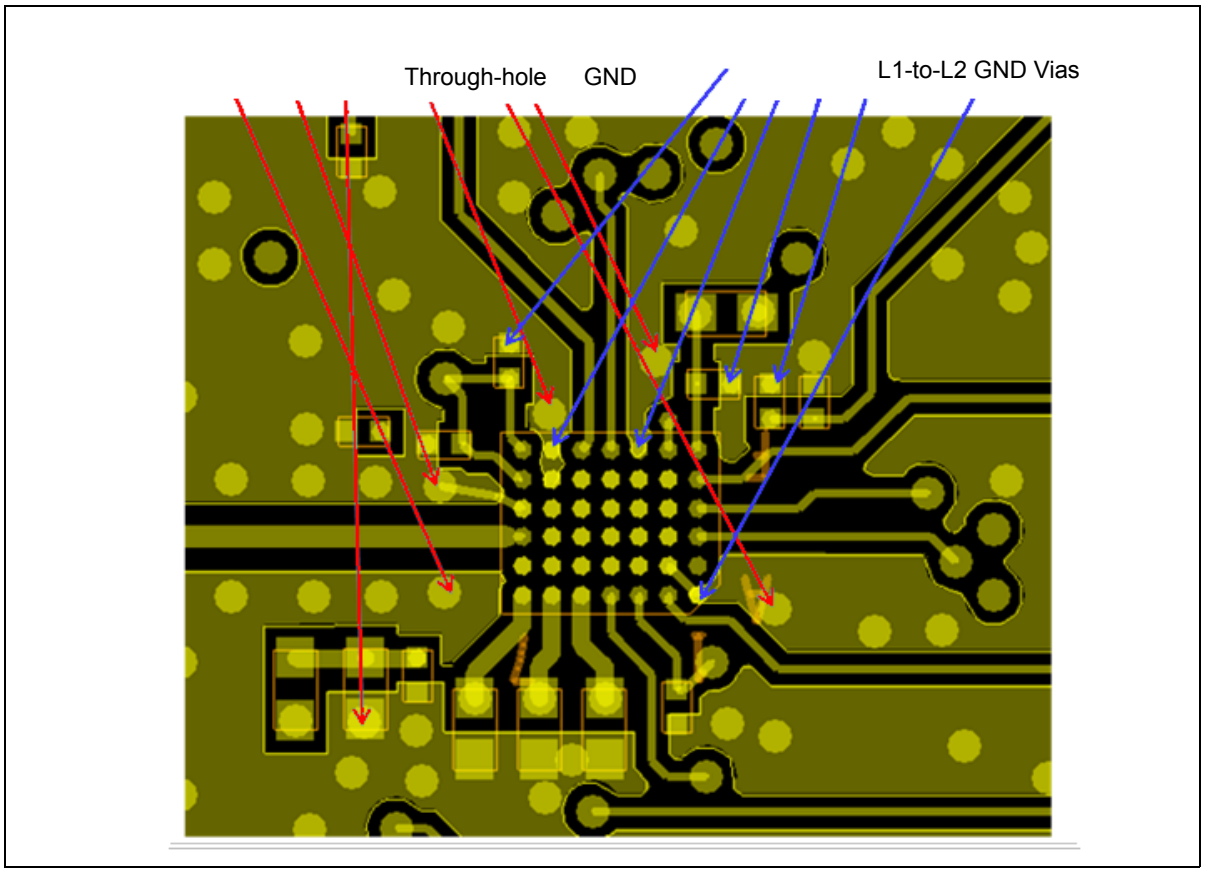
Figure 7. RF Trace Routing



10 GND Vias

Sufficient GND vias should be placed near the chip and on the GND via pads to minimize ground inductance presented to the CYW89071.

Figure 8. GND Vias



11 BPF Recommendations

Interference due to out-of-band blockers such as GSM and WCDMA signals will have an adverse affect on the CYW89071 RX sensitivity. To prevent these blockers from degrading the CYW89071 RX sensitivity, a band-pass filter (BPF) with good rejection must be used. The uplink (mobile-to-base station) frequencies will have more of an impact on the Bluetooth RX sensitivity because the transmitter is collocated on the mobile. The downlink (base station-to-mobile) frequencies will have less of an impact on the Bluetooth RX sensitivity because the signal received from the base station will be much lower than what the mobile is transmitting.

The CYW89071 TX and RX spurious emissions can have an adverse effect on the cell phone, FM radio, and GPS RX sensitivity. The recommended BPF rejection will mitigate these spurious emissions. The dominant filter requirement is primarily due to the uplink frequencies.

Table 2 shows the recommended BPF rejection for the CYW89071 The recommendations are derived from our internal system link budget, which factor in CYW89071 out-of-band blocking and spurious emissions performance. The recommended BPF rejection for each band is listed in column 3. The Murata® BPF part # LFB212G45CE5D035 specification is shown in column 4, which meets or exceeds the recommended filter rejection. The last column shows another Murata BPF that is smaller in size but does not meet specific cell band rejection requirements. This filter is included here as a comparison.

Table 2. Recommended BPF Rejection

Band	Frequency (MHz)	Recommended BPF Rejection	Murata BPF LFB212G45CE5D035[a] Size: 2.01 × 1.25 mm I.L. = 2.34 (Typ)	Murata BPF LFB182G45CG3C179[a] Size 1.6 × 0.8 mm I.L. = 2.15 (Typ)
GSM850	824–849	50	50.5	36.8
EGSM900	880–915	24	50.2	36.3
DCS1800	1710–1785	39	51.7	39.0
GSM850 (EDGE)	824–849	50	50.5	36.8
EGSM900 (EDGE)	880–915	19	50.2	36.3
DCS1800 (EDGE)	1710–1785	35	51.7	39.0
PCS1900(EDGE)	1850–1910	41	42.8	42.5
UMTS1900	1850–1910	37	42.8	42.5
UMTS2100 Tx	1920–1980	37	39.2	34.8
UMTS2100 Rx	2110–2170	20	36.9	29.2
CDMA700	740–794	19	35	35
CDMA850	824–849	42	50.5	36.8
CDMA1800	1850–1910	25	72.8	42.5
GPS	1572–1577	30	55.9	35.6
FM	76–108	25	50	50

a. All values in this column are typical.

Document History Page

Document Title: AN214856 - Printed Circuit Board Layout Guidelines Document Number: 002-14856				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	08/30/2013	89071-AN100-R Initial release
*A	5460045	UTSV	10/04/2016	Updated to Cypress template Added Cypress part numbering scheme
*B	5836748	AESATMP9	07/28/2017	Updated logo and copyright.

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