AN205552

F2MC-16FX Family, Clock Output

This application note describes the functionality of the Clock Output function and gives an example.

1 Introduction

This application note describes the functionality of the Clock Output function and gives an example.

1.1 Key Features

- All important internal MCU Clocks can be output to a Pin:
  - RC Clock (CLKRC)
  - Main Clock (CLKMC)
  - Sub Clock (CLKSC)
  - PLL Output Clock (CLKPLL)
  - Modulated PLL Clock (CLKMOD)
  - System Clock 1 (CLKS1)
  - System Clock 2 (CLKS2)
  - Bus Clock (CLKB)
  - Peripheral Clock 1 (CLKP1)
  - Peripheral Clock 2 (CLKP2)
  - VCO Clock of PLL (CLKVCO)
  - PLL Feedback Clock (CLKPLLFB)
- Clock Output Divisor selectable in 2^n-Steps from 1 to 128
- Synchronization Mechanism for Output Pin

2 Clock Output

The Basic Functionality of the Clock Output Function

2.1 Functionality

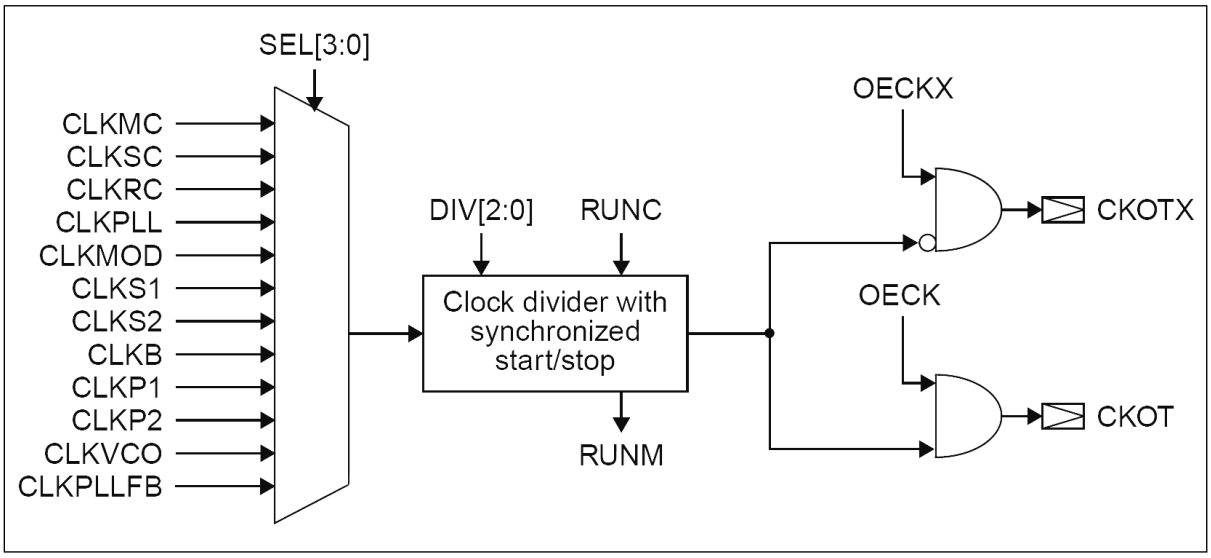
With the Clock Output Module all internal clocks can be output to two external pins. On one pin the normal clock is output while on the other pin the inverted signal is output. Furthermore the clock signal can be divided.

Up to two Clock Output Modules are available.

Please note that frequencies above 32 MHz will not be output correctly. This is because the I/O Ports are not designed for higher frequencies. If clocks with higher frequencies are to be output, please use the output clock division.

2.2 Block Diagram

Figure 1. Clock Output block diagram



2.3 Registers

2.3.1 Clock Configuration Register 0/1 (COCR0/1)

The COCR0/1 consists of the following bits:

Table 1. COCR0/1

Bit No.	Bit Name	Initial Value	Value	Description
15/7	–	X	0	*Reserved, always write "0" to this Bit*
14/6 … 12/4	DIV2 … DIV0	0, 0, 0	0, 0 ,0	No Output Clock Division
			0, 0, 1	Output Clock Division of 2
			0, 1, 0	Output Clock Division of 4
			0, 1, 1	Output Clock Division of 8
			1, 0, 0	Output Clock Division of 16
			1, 0, 1	Output Clock Division of 32
			1, 1, 0	Output Clock Division of 64
			1, 1, 1	Output Clock Division of 128
11/3 … 8/0	SEL3 … SEL0	0, 0, 0, 0	0, 0, 0, 0	No Clock is output
			0, 0, 0, 1	CLKRC, RC Clock is output
			0, 0, 1, 0	CLKMC, Main Clock is output
			0, 0, 1, 1	CLKSC, Sub Clock is output
			0, 1, 0, 0	CLKPLL, PLL Clock is output
			0, 1, 0, 1	CLKMOD, Modulated PLL Clock is output
			0, 1, 1, 0	CLKS1, System Clock 1 is output
			0, 1, 1, 1	CLKS2. System Clock 2 is output
			1, 0, 0, 0	CLKB, Bus clock is output
			1, 0, 0, 1	CLKP1, Peripheral Clock 1 is output
			1, 0, 1, 0	CLKP2, Peripheral Clock 2 is output
			1, 0, 1, 1	CLKVCO, VCO clock of PLL is output
			1, 1, 0, 0	CLKPLLFB, PLL Feedback Clock is output
			1, 1, 0, 1	*Reserved, Output is undefined*
			1, 1, 1, 0	*Reserved, Output is undefined*
			1, 1, 1, 1	*Reserved, Output is undefined*

COCR0 controls CKOT0/CKOTX0 pins and COCR1 controls CKOT1/CKOTX1 pins.

Please note, that if an output is enabled and the setting is changed, a spike can be output on the corresponding channel. Therefore setting should only be changed, if the corresponding RUNM Bit of the COAR is "0".

2.3.2 Clock Output Activation Register (COAR)

The COAR consists of the following bits:

Table 2. COAR

Bit No.	Bit Name	Initial Value	Value	Description
15	RUNM1	0	0	CKOT1/CKOTX1 clock is stopped (read only Bit)
			1	CKOT1/CKOTX1 clock is active (read only Bit)
14	RUNC1	0	0	Stops the CKOT1/CKOTX1 Clock
			1	Starts the CKOT1/CKOTX1 Clock
13	CKOXE1	0	0	CKOTX1 Clock Output Pin is disabled
			1	CKOTX1 Clock Output Pin is enabled
12	CKOE1	0	0	CKOT1 Clock Output Pin is disabled
			1	CKOT1 Clock Output Pin is enabled
11	RUNM0	0	0	CKOT0/CKOTX0 clock is stopped (read only Bit)
			1	CKOT0/CKOTX0 clock is active (read only Bit)
10	RUNC0	0	0	Stops the CKOT0/CKOTX0 Clock
			1	Starts the CKOT0/CKOTX0 Clock
9	CKOXE0	0	0	CKOTX0 Clock Output Pin is disabled
			1	CKOTX0 Clock Output Pin is enabled
8	CKOE0	0	0	CKOT0 Clock Output Pin is disabled
			1	CKOT0 Clock Output Pin is enabled

Please note that `CKOE` or `CKOXE` and the corresponding `RUNC` should be set at the same time or `RUNC` should be set after setting `CKOE` or `CKOXE`.

3 Clock Output Example

Example for the Clock Output Usage

3.1 Half Main Clock Output on CKOT0

The following sample code assigns the Main Clock (`CLKMC`) divided by 2 to `CKOT0` and waits until the clock is synchronized.

```
void Set_CLKMC_CKOT0 (void)
{
       COAR = 0x00;          // Stop all possible Clock Outputs
       COCR0 = 0x12;         // DIV [2:0] = 0, 0, 1; SEL [3:0] = 0, 0, 1, 0
       COAR = 0x05;          // RUNC0 = 1; CKOE0 = 1

       while (!COAR_RUNM0); // Wait for synchronization
}
```

4 Additional Information

Information about Cypress Microcontrollers can be found on the following Internet page:

http://www.cypress.com/cypress-microcontrollers

The software example related to this application note is:

96340_clk_out

It can be found on the following Internet page:

http://www.cypress.com/documentation/software-and-drivers/96340-clk-out-v11

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	NOFL	06/28/2006	Initial release
			02/23/2007	Reviewed the document and updated with review findings
			08/13/2007	Corrected some typos
*A	5074685	NOFL	03/04/2016	Migrated Spansion Application Note MCU-AN-300214-E-V12 to Cypress template.
*B	6079633	NOFL	02/23/2018	Updated Additional Information: Updated hyperlinks in this section. Updated to new template. Completing Sunset Review.

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